RoHS COMPLIANT

Giantplus Technology

Specification of LCD Module

Product No.: GPM959B1

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1. ENERAL DESCRIPTION

GPM959A0 is a trans-missive type color active matrix liquid crystal display (LCD), which uses amorphous thin film transistor (TFT) as switching devices. This product is composed of a TFT LCD panel, driver ICs, FPC, Bezel and a backlight unit.

2. FEATURES

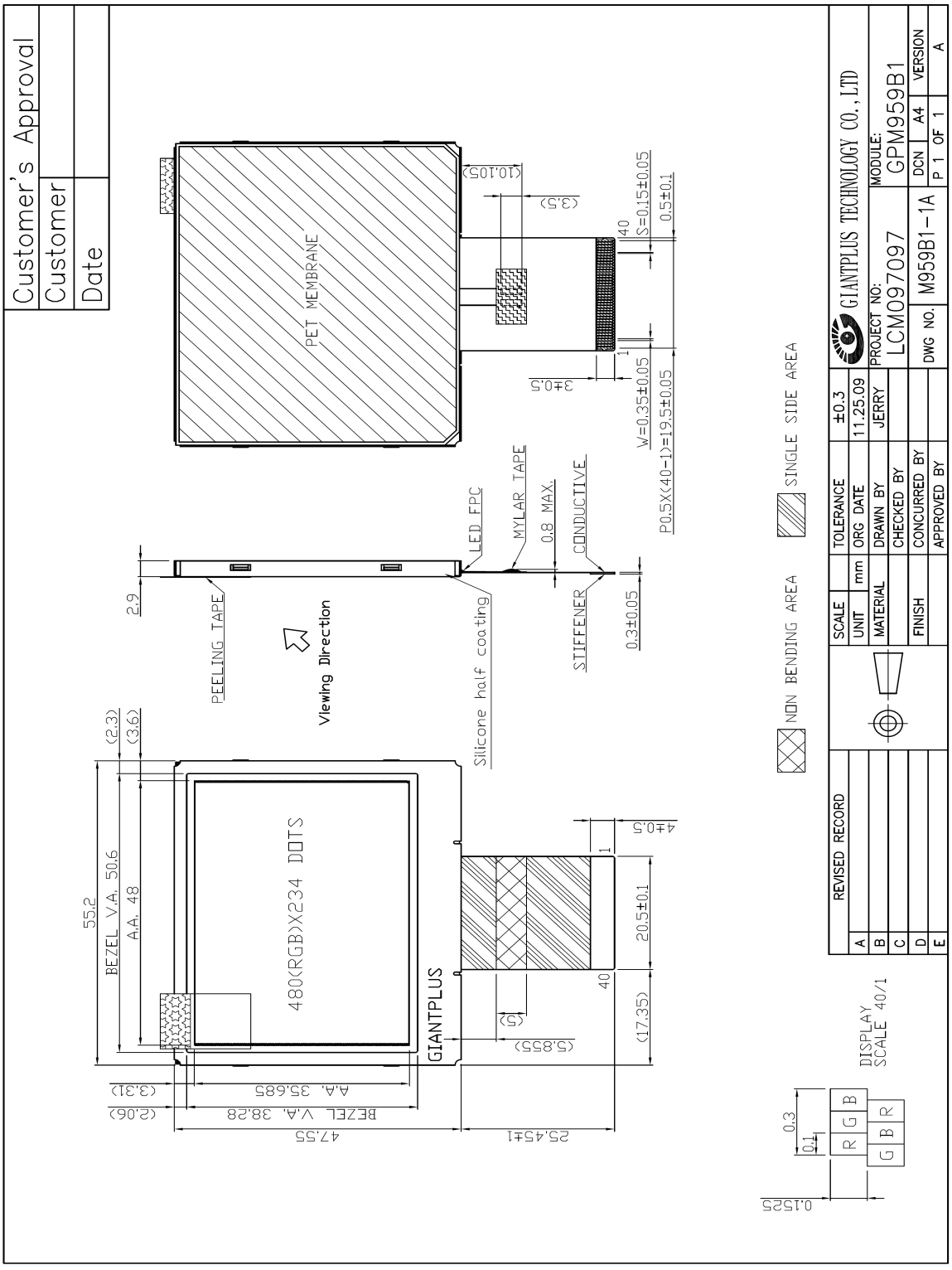
Display Mode	Transmissive Type
	TFT LCD, Positive mode
Screen Size	2.36 inch
Display Format	Graphic 480(RGB)*234 Delta type
Color	16.7M color
Input Data	8 bit serial(RGB) data input from controller / Raw data / CCIR 656,601
Interface	Digital RGB
Surface Treatment	AG, Hard coating
Backlight Color	White (LED*1)
Viewing Direction	6 O'clock

3. MECHANICAL SPECIFICATION

Item	Specifications	Unit
Dimensional outline	55.2(W)×47.55(H)*×2.9(D)	mm
Resolution	480(R, G, B)×234	dot
Active area	48.0(W)×35.69(H)	mm
Dot pitch	0.1 (W)×0.1525(H)	mm

＊ Without FPC

4. MECHANICAL DIMENSION



5. MAXIMUM RATINGS

If the operating condition exceeds the following absolute maximum ratings, the TFT LCD module may be damaged permanently. PGND=VSS=0V,Ta=25°C

Item	Symbol	Values		Unit	Condition
		Min.	Max.		
Power voltage	VDD	-0.5	7	V	
	VDDIO	-0.5	7	V	
Input signal voltage	VCOM	-2.9	5.2	V	
Digital Input Voltage	V_{IN}	-0.3	VDD+0.3	V	
Storage Temperature	T_{ST}	-25	80	℃	
Operating Temperature (Ambient Temperature)	T_{OP}	0	60	℃	
Maximum clock frequency	Fmax	--	27	MHz	
Humidity	-	-	90	%RH	Note1

Note1: $T_A \leqq 40℃$ Without dewing

6. ELECTRICAL CHARACTERISTIC

a. Typical operating conditions

Item		Symbol	Values			Unit	Remark
			Min.	Typ.	Max.		
Supply Voltage		VDD	3.0	3.3	3.6	V	
		VDDIO	3.0	3.3	3.6		Note6-1
Supply Voltage for Gate Driver	H level	VGH	16.5	18.5	20	V	Note6-1
	L Level	VGL	-7	-6	-5.5	V	
Digital input Voltage	H level	V_{IH}	0.7VDDIO	-	VDDIO	V	
	L Level	V_{IL}	GND	-	0.3VDDIO	V	
Digitaloutput t Voltage	H level	V_{OH}	VDDIO-0.4	-	VDDIO	V	
	L Level	V_{OL}	GND	-	VDDIO+0.4	V	
VCOM		V_{COMAC}	4.5	5	5.2	Vp-p	AC Component of VCOM
		V_{COMDC}	-	0.72	-	V	Note6-2

Note6-1: VGH and VGL supplied by internal setup-up circuit

Note6-2: Please adjust VCDC to make the flicker level be minimum. suggest R5 setting data 0x7d

b. Current consumption

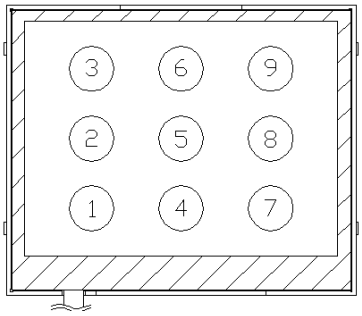
Parameter	Symbol	Condition	Typ.	Max.	Unit	Remark
Supply current	IDD	VDD=+3.3V	9	13.2	mA	-

7. BACKLIGHT CHARACETRISTIC

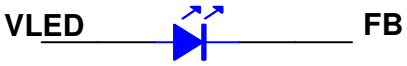
7.1. Characteristic

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Power Consumption	VLED	2.8	-	3.8	V	
LED Current	I_F	-	25	-	mA	
LCM Brightness		200	250	-	Cd/m^2	I_F=25mA

7.2. Lightguide Specification



a. Test Instrument: BM-7 (Distance =500mm; Field = 1°)
b. Light Source: LED * 1 (White)



c. Conditions: IF =25 mA, VLED (Typ.) = 3.3V
d. Measure Brightness: 1 ~ 9
e. Uniformity = (Min. Brightness / Max. Brightness)*100%
f. Uniformity ≧ 70%

8. MODULE FUNCTION DESCRIPTION

8.1. PIN Description

Pin	Symbol	I/O	Function	Remark
1	VCOM	I	Common electrode driving voltage	Note 8-1
2	NC	--	-	
3	VGL	O	power supply for gate off voltage	Note 8-2
4	C4P	C	Pins to connect capacitance for power circuitry	
5	C4N	C	Pins to connect capacitance for power circuitry	
6	VGH	O	power supply for gate on voltage	
7	FRP	O	Frame polarity output for VCOM	
8	VCAC	O	Define the amplitude of the VCOM swing	
9	VDD_25V	O	Intermediate voltage for charge Pump. Please connect the capacitor between VDD_25V and VSS.	
10	C3P	C	Pins to connect capacitance for power circuitry	
11	C3N	C	Pins to connect capacitance for power circuitry	
12	VDD3	O	Charge-pump circuit reference voltage. Please connect the capacitor between VCIOUT and VSS.	
13	C2P	C	Pins to connect capacitance for power circuitry	
14	C2N	C	Pins to connect capacitance for power circuitry	
15	NC	---	---	
16	C1P	C	Pins to connect capacitance for power circuitry	
17	C1N	C	Pins to connect capacitance for power circuitry	
18	GND	P	Charge Pump Power GND	
19	VDD	P	Charge Pump Power VDD	Note 8-3
20	DRV	O	Gate signal for the power transistor of the boost converter	Note 8-4
21	VLED	P	Supply voltage for LED backlight	
22	NC	--	DUMMY	

23	FB	I	Main boost regulator feedback input	Note 8-5
24	NC	--	DUMMY	
25	AGND	P	Ground terminal in the logic circuit.	
26	VDDIO	P	Power supply terminal in the logic circuit.	Note 8-3
27	CSB	I	Serial communication chip select	
28	SDA	I/O	Serial communication data input	
29	SCL	I	Serial communication clock input	
30	HSYNC	I	Horizontal sync input	Note 8-6
31	VSYNC	I	Vertical sync input	Note 8-7
32	DCLK	I	Clock Input	Note 8-8
33	D7	I	Data Input：MSB	
34	D6	I	Data Input：	
35	D5	I	Data Input：	
36	D4	I	Data Input：	
37	D3	I	Data Input：	
38	D2	I	Data Input：	
39	D1	I	Data Input：	
40	D0	I	Data Input：	

I: Input O: Output P: Power I/O: Serial communication data input/output C: Capacitor

Note 8-1:VCOM=+5.0 Vp-p.(Typ.)

Note 8-2: The external capacitor is required on those pins as following.

Symbol	Part standard		Notes
	Capacitance	Voltage	
VDD3	1 to 2.2uF	16V over	
VDDA	1 to 2.2uF	16V over	
VGH	1 to 2.2uF	25V over	
VGL	1 to 2.2uF	25V over	
VCAC	1 to 2.2uF	16V over	
C1P, C1N	1 to 4.7uF	16V over	
C2P, C2N	1 to 4.7uF	16V over	
C3P, C3N	1 to 4.7uF	16V over	
C4P, C4N	1 to 4.7uF	16V over	
FRP	1 to 2.2uF	16V over	
VDD_25V	1 to 2.2uF	16V over	

Note 8-3: VDD, VDDIO=+3.3V (Typ.)

Note 8-4: Outputs the control signal of switching regulator for LED. Duty cycle varies

according to FB input voltage

Note 8-5: Feedback signal of switching signal for LED. It controls DRV output duty cycle with 0.6V input level sense.

Note 8-6: Horizontal sync signal, it is a “L “active signal.

Note 8-7: Vertival sync signal, it is a “Low “active signal.

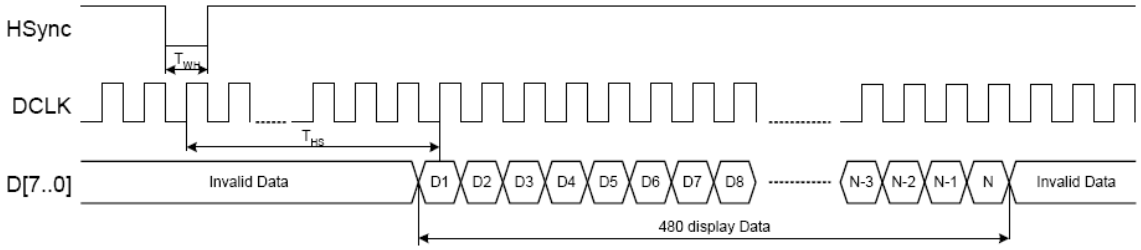
Note 8-8: Dot clock signal for RGB interface, timing for data loading defined at rising edge.

8.2. AC characteristics

AC characteristics (VDD=3.3V, AGND=GND=0V, TOPR = -30℃ to +85℃)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CLK pulse duty	Tcw		40	50	60	%
Delay between Hsync and DCLK	Thc		-	-	1.0	DCLK
Hsync width	Twh		1.0	-	-	DCLK
Hsync period	Th		60	63.56	67	us
Vsync setup time	Tvst		12	-	-	ns
Vsync hold time	Tvhd		12	-	-	ns
Hsync setup time	Thst		12	-	-	ns
Hsync hold time	Thhd		12	-	-	ns
Data set-up time	Tdsu	D00~D07 to DCLK	12	-	-	ns
Data hold time	Tdhd	D00~D07 to DCLK	12	-	-	ns
VSync to 1st gate Output	Tstv	Sel≠”111”;By HDL[3..0] settings	6	13	21	Th
CCIR V to 1st gate Output	Tstv	Sel=”111” NTCS (PAL=0); By HDL[3..0] settings	14	21	29	Th
CCIR V to 1st gate Output	Tstv	Sel=”111” PAL=1; By HDL[3..0] settings	20	27	35	Th
SD output stable time	Tst	30mV precision; CL=6.75pF, R=3.62K	-	25	30	us
GD output delay time	Tgd	CL=17.6pF, R=1.29K	-	900	1500	ns
GD output rise and fall time	Tgst	CL=17.6pF, R=1.29K 10% to 90%	-	900	1500	ns
Serial communication						
Serial clock period	Tsck		320	-	-	ns
Serial clock duty cycle	Tscw		40	50	60	%
Serial clock width low/high	Tssw		120			ns
Serial data setup time	Tist		120			ns
Serial data hold time	Tihd		120			ns
CSB setup time	Tcst		120			ns
CSB data hold time	Tchd		120			ns
Chip select distinguish	Tcd		1			us
Delay between CSB and Vsync	Tcv		1			us

8.2.1. RAW DATA MODE

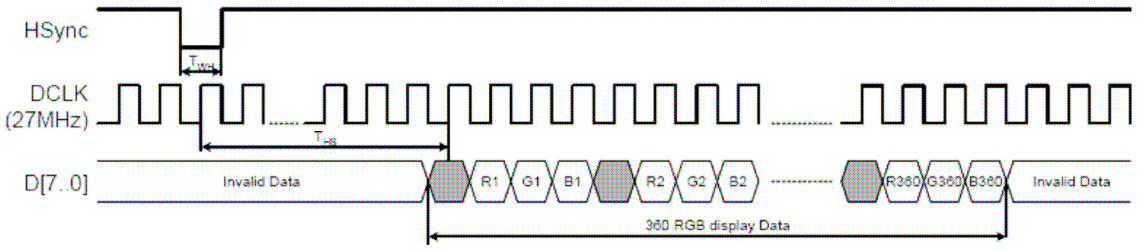


(VDDIO=1.8V~VDD, VDD=+3.0 to +3.6V, VSS=0V)

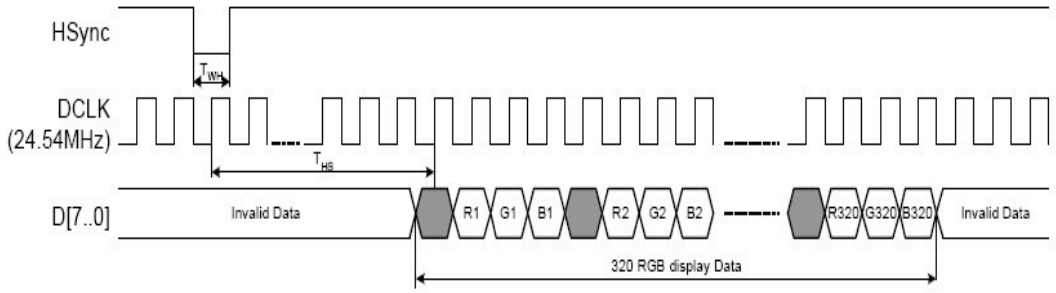
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DCLK frequency	Fclk		-	9.7	-	MHz
DCLK period	Tcph		-	103	-	ns
Delay from Hsync to Source Output	Thso		-	56	-	DCLK
Delay from Hsync to Gate Output	Thgo		-	45	-	DCLK
Delay from Hsync to Gate Output off	Thgz		-	19	-	DCLK
Delay from Hsync to Q1H	Thq		-	39	-	DCLK
Delay from Hsync to FRP	Thf			59		DCLK
Delay from Hsync to 1st data input	Ths	Function of DDL[5..0] settings	68	100	131	DCLK
DC converter osc. Frequency	Fosc	Fclk/32	-	303.1	-	kHz

8.2.2. SERIAL RGB MODE

A. 360mode (27Mhz) time specifications



B. 320mode (24.545Mhz) time specifications

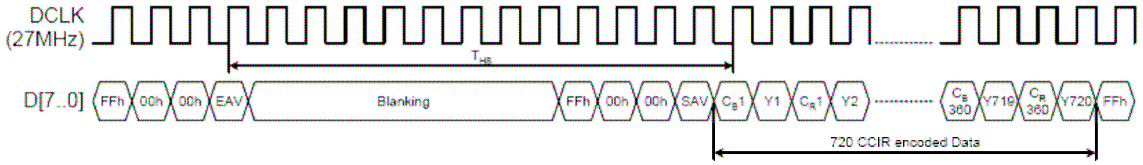


(VDDIO=1.8V~VDD, VDD=+3.0 to +3.6V, VSS=0V)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DCLK frequency	Fclk		-	24.54/27	-	MHz
DCLK cycle time	Tcph		-	40/37	-	ns
Delay from Hsync to Source Output	Thso		-	143	-	DCLK
Delay from Hsync to Gate Output	Thgo		-	113	-	DCLK
Delay from Hsync to Gate Output off	Thgz		-	48	-	DCLK
Delay from Hsync to Q1H	Thq		-	100	-	DCLK
Delay from Hsync to FRP	Thf			143		DCLK
Delay from Hsync to 1st data input	Ths	Function of DDL[5..0] settings	220	252	283	DCLK
DC converter osc. Frequency	Fosc	Fclk/64 = 383.4kHz / 421.9kHz	-	383.4 / 421.9	-	kHz

8.2.3. CCIR MODE(CCIR 656)

Timing Characteristic



(VDDIO=1.8V~VDD, VDD=+3.0 to +3.6V, VSS=0V)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DCLK frequency	Fclk		-	27	-	MHz
DCLK cycle time	Tcph		-	37	-	ns
CLK pulse duty	Tcw		40	50	60	%
Delay from EAV to Source Output	Thso		-	143	-	DCLK
Delay from EAV to Gate Output	Thgo		-	113	-	DCLK
Delay from EAV to Gate Output off	Thgz		-	48	-	DCLK
Delay from EAV to Q1H	Thq		-	100	-	DCLK
Delay from EAV to FRP	Thf			143		DCLK
Delay from EAV to 1st data input	Ths	Function of DDL[5..0] settings	241	273	304	DCLK
DC converter osc. Frequency	Fosc	Fclk/64	-	421.9	-	kHz

8.2.4. CPU Serial Transfer Timing Wave Form:

The register setting is done by 3-interface of chip select signal (CS_X), serial clock signal (SCL), and data input signal (SDA) from CPU etc.

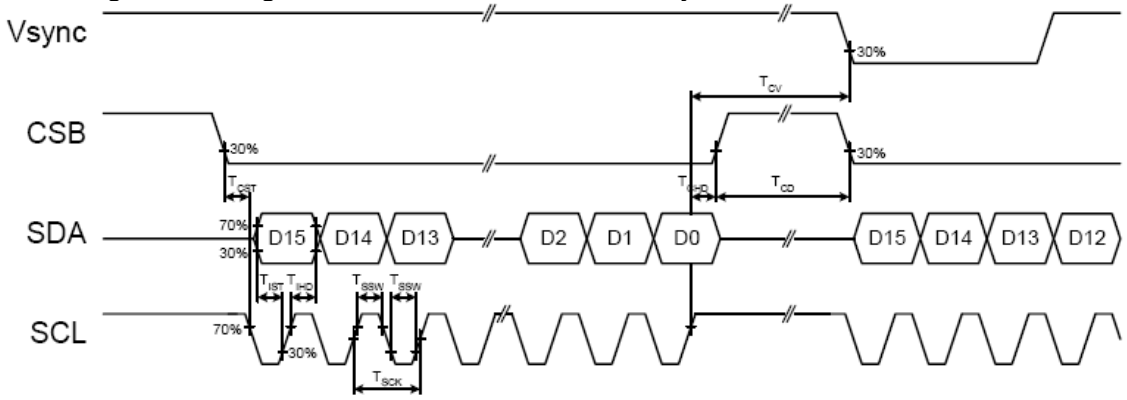
When CS_X=L, it is recognized forwarding to this chip, and takes the SDA signal by rising edge about the SCL signal. The forwarding ends with CS_X=H and only the data of the register corresponding to LSI holds. The forwarding bits is 16-bits and 3bits of the head becomes an address cord and 13 bits after those becomes register setting data. It is forwarded to the turn of LSB from MSB.

If less than 16-bits of SCL are input while CS_X=L, the transferred data is ignored.

If 16-bits or more of SCL are input while CS_X=L, the first 16-bits of transferred data before the rising edge of CS_X pulse are valid data.

After power-on reset is released, the command of the initial operation setting etc. can be forwarded.

The register setting can be received in the standby mode.



(VDD=+3.0 to +3.6V, VSS=0V)

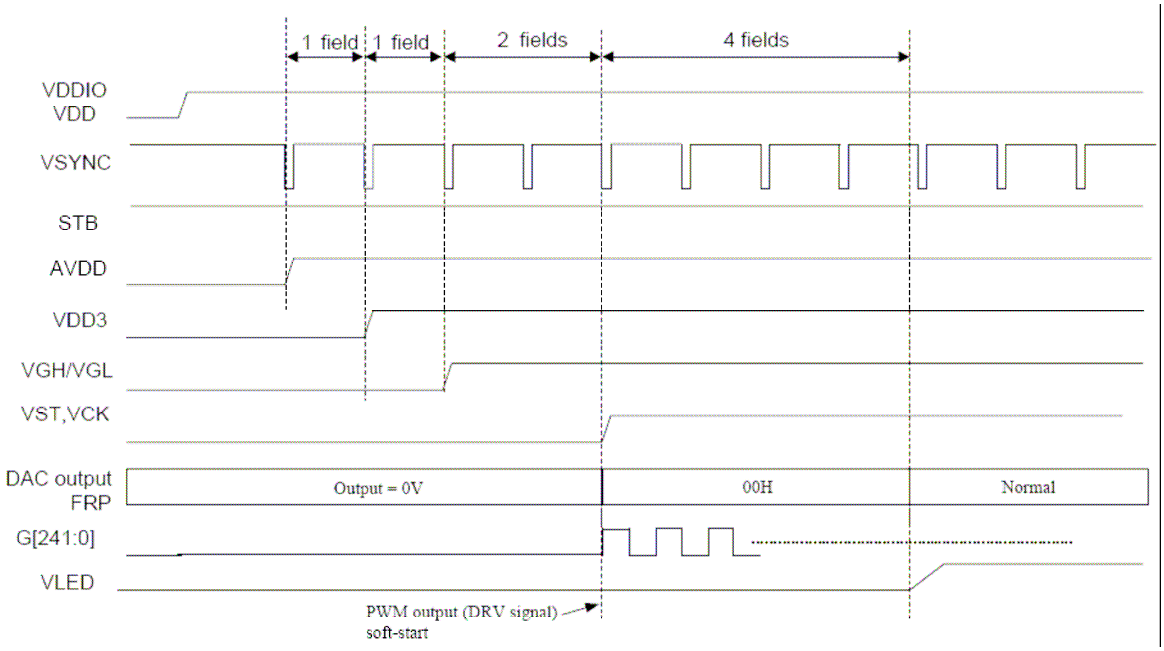
Serial communication						
Serial clock period	Tsck		320	-	-	ns
Serial clock duty cycle	Tscw		40	50	60	%
Serial clock width low/high	Tssw		120			ns
Serial data setup time	Tist		120			ns
Serial data hold time	Tihd		120			ns
CSB setup time	Tcst		120			ns
CSB data hold time	Tchd		120			ns
Chip select distinguish	Tcd		1			us
Delay between CSB and Vsync	Tcv		1			us

9. POWER ON/OFF SEQUENCE

Special care should be taken that the large current may cause a permanent damage to the LSI when voltage is applied to the LCD drive power supply terminals in the condition that the logic power supply terminals are floating.

9.1. Power Supply ON Sequence

The following sequences are recommended from the power supply ON to the image display.

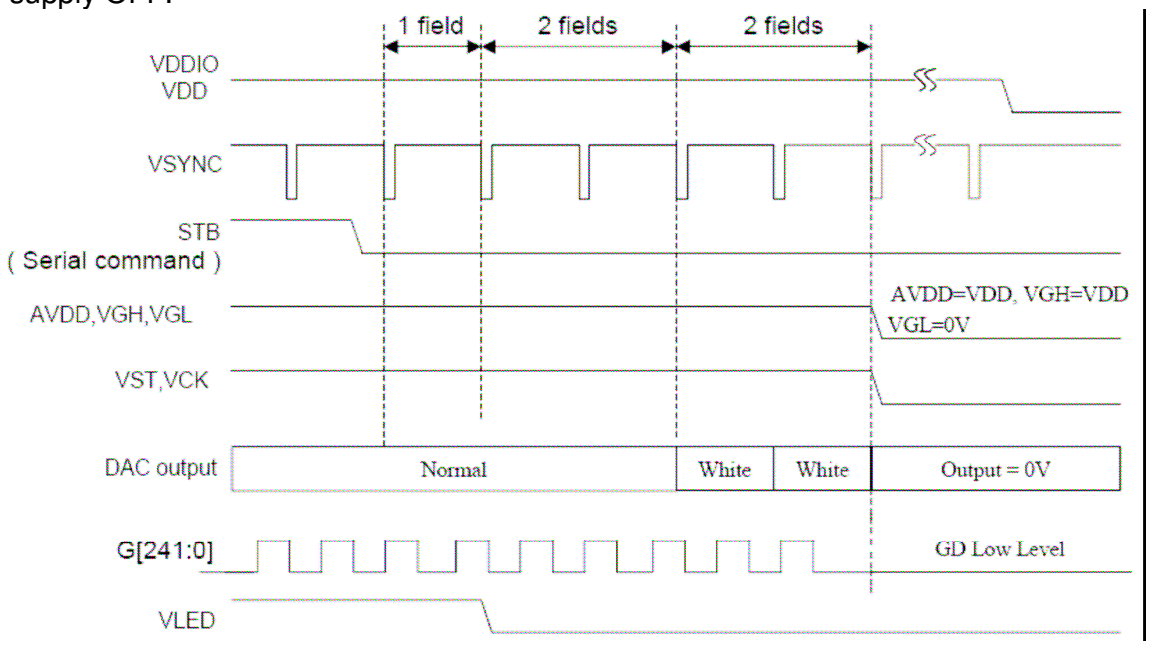


Note: 1.The software reset command by the GRB register is not cared about even if it doesn't send it because the initialization operation is done with LSI internal power-ON reset circuit when the power supply is turned ON.

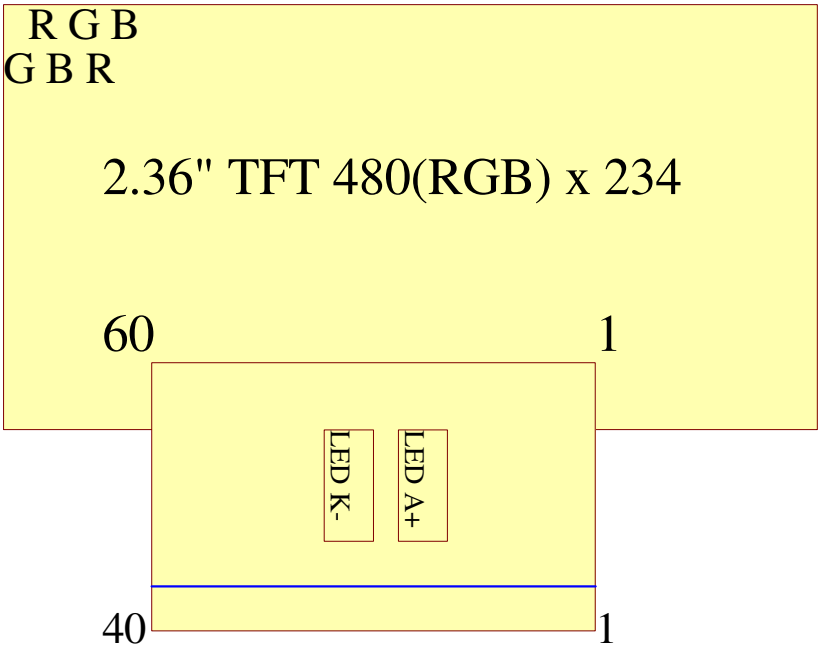
2.The setting of SHDB register and GRB register is sent at the same time and not cared about. However, LED is light4ed after the image data over 3-frmes is received.

9.2. Power Supply OFF Sequence

The following sequences are recommended from the image display to the power supply OFF.



Note: 1. IF the SHDB register is not set as 0 before stopping image data (DOTCLK), since the transistor of an external backlight LED control circuit may become being in ON state with as and may generate heat, please be sure to set SHDB as 0.

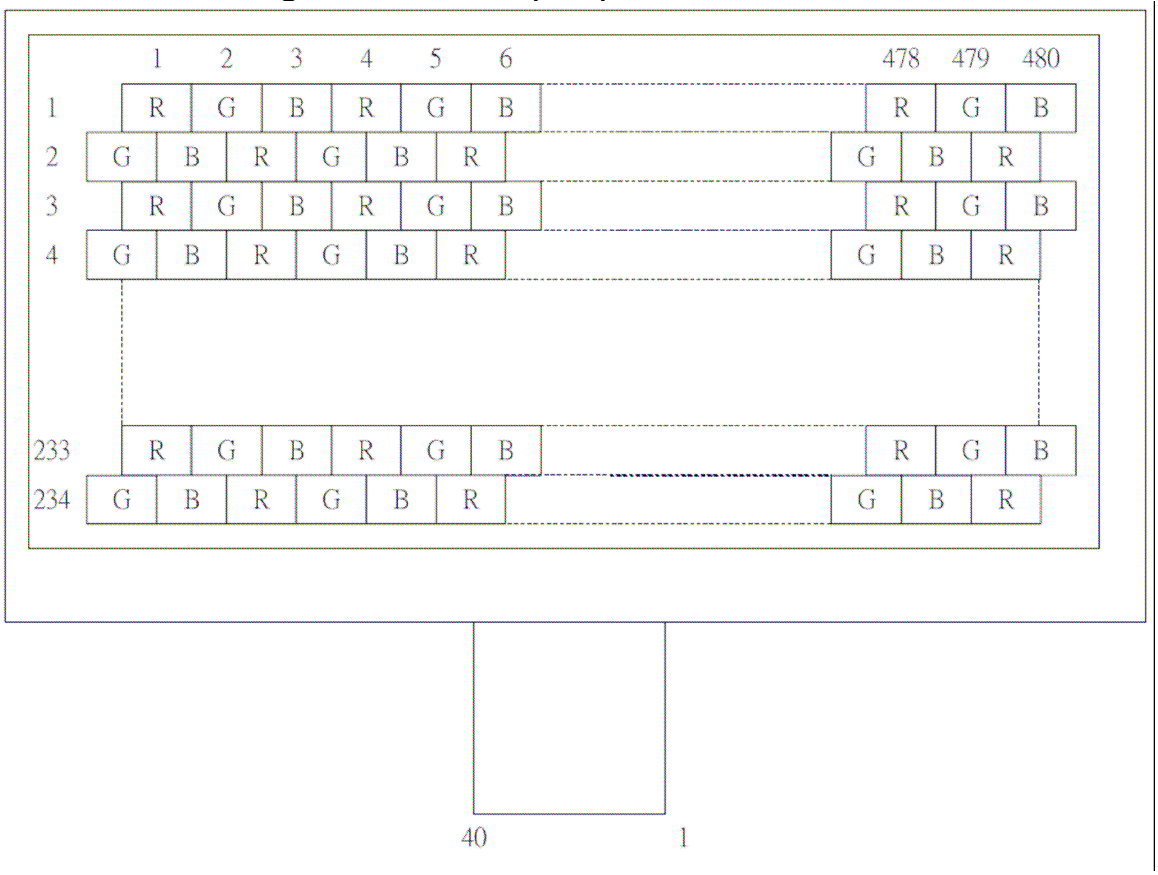


10. BLOCK DIAGRAM OF LCM

10.1. Display Color and Gray Scale Reference

Color		Input Color Data																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Red (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (01)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (02)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker																								
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																								
	Red (253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Green	Green (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (01)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	0	0	0	0	0	0	0
	Green (02)	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	Darker																								
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																								
	Green (253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green (254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Blue	Blue (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (01)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (02)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	Darker																								
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																								
	Blue (253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

10.2. Pixel arrangement and input pin connector No.



11. ELECTRO-OPTICAL CHARACTERISTICS

The following items are measured under stable conditions. The optical characteristics should be measured in dark room or equivalent state with the methods shown in Note 1,Note2,Note3.

Item		Symbol	Condition	Min	Typ	Max	Unit	Remark
Response time		T_R	Θ=0	-	6	12	ms	Note 4,6
		T_F		-	15	30	ms	
Contrast ratio		CR	At optimized viewing angle	-	400	-	-	Note 5,6
Viewing Angle	Hor.	Θ_R	CR≧ 10	-	(45)	-	Degree	Note 6,7
		Θ_L		-	(45)	-		
	Ver.	φ_H		-	(15)	-		
		φ_L		-	(35)	-		
Transmission		Y_L	Θ=0	-	8.0	-	%	Note8
R		X	Θ=0	-	(0.613)	-	-	
		Y		-	(0.330)	-		
G		X		-	(0.317)	-		
		Y		-	(0.549)	-		
B		X		-	(0.150)	-		
		Y		-	(0.190)	-		
White		X		-	(0.302)	-		
		Y		-	(0.348)	-		
Brightness			Θ=0	200	250	-	Cd/m^2	

Note1:Ambient temperature=25℃

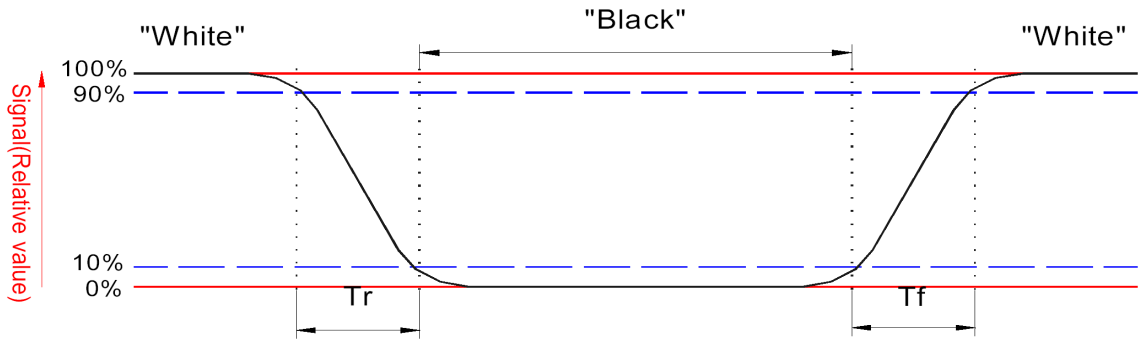
Note2:To be measured in the dark room.

Note3:To be measured on the center area of panel with a field angle of 1℃ by Topcon luminance meter BM-7,after 10 minutes operation.

Note4:Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black”to”white”(falling time) and from “white”to”black” (rising time),respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



Note5: Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness measured when LCD is at “white state”}}{\text{Brightness measured when LCD is at “black state”}}$$

Note6:White Vi=Vi50 $\overline{+}$1.5V

Black Vi=Vi50 ± 2.0V

“±”means that the analog input signal swings in phase with COM signal.

“$\overline{+}$”means that the analog input signal swings out of phase with COM signal.

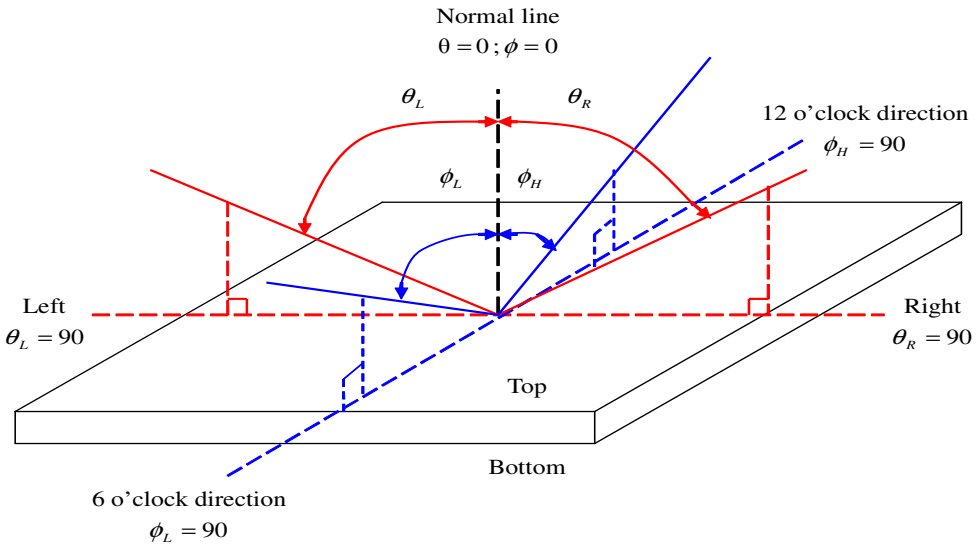
Vi50 :The analog input voltage when transmission is 50%

The 100% transmission is defined as the transmission of LCD panel when all

The input terminals of module are electrically opened.

Note7:Definition of viewing angle:

Refer to figure as below.



Note8:Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

12. RELIABILITY

12.1.MTTF

The LCD module shall be designed to meet a minimum MTTF value of 50,000 hours with normal condition. (25℃ in the room without sunlight; not include life time of backlight)

12.2.Tests

NO.	ITEM	CONDITION	CRITERION
1	High Temperature Operating	60℃ 240 hrs	No Defect Of Operational Function In Room Temperature Are Allowable. Leakage current should be below double of initial value.
2	Low Temperature Operating	0℃ 240 hrs	
3	High Temperature Non-Operating	80℃ 240 hrs	
4	Low Temperature Non-Operating	-25℃ 240 hrs	
5	High Temperature/ Humidity Non-Operating	60℃ ,90%RH 240 hrs	
6	Temperature Shock Non-Operating	-30℃ ⟷ 80℃ (30min) (5min) (30min) 100CYCLES	
7	Electrostatic Discharge Test Non-Operating	HBM:±2Kv	
8	Vibration test (Carton)	Random Frequency 5-500Hz 0.015G^2/Hz 2 ~5 、500-600Hz ± 6dB/oct(Slope) 2.95Grms ,1hrs for each direction of X,Y,Z	
9	Drop test (Carton)	One corner /three edge/ six face. Drop height：40cm	

Note 1: Test after 24 hours in room temperature.
Note 2: The sampling above is individually for each reliability testing condition.
Note 3: The color fading of polarizing filter should not care.
Note 4: All of the reliability testing chamber above, is using D.I. water.(Min value: 1.0Mohm-cm)
Note 5: In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.

12.3. Color performance

No.	ITEM	Criterion (initial)
1	Luminance	>50%
2	NTSC	>70%
3	Contrast Ratio	>50%

13. INSPECTION CRITERIA

13.1. Inspection Conditions

13.1.1. Environmental conditions

The environmental conditions for inspection shall be as follows

Room temperature: 23±5℃

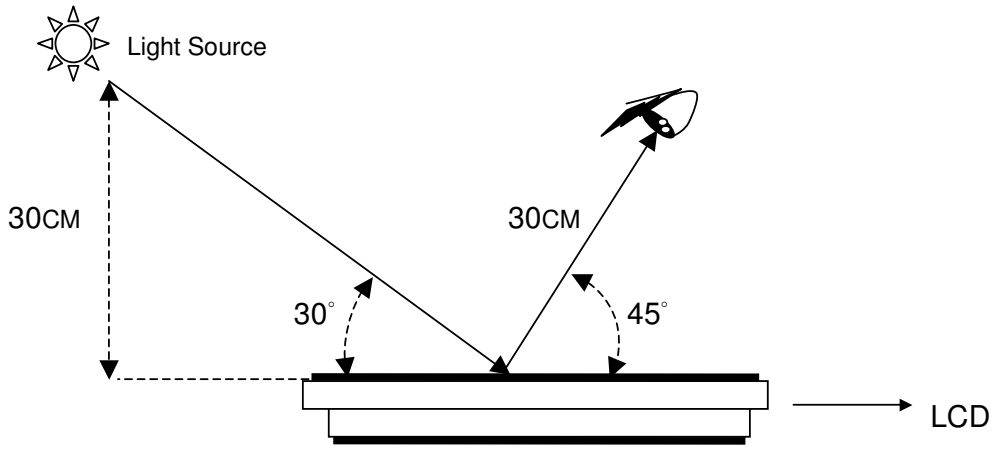
Humidity: 50±20%RH

13.1.2. The external visual inspection

With 1000±200 lux fluorescent lamp as the light source, the inspection was in the distance of 30cm or more from the LCD to the inspector's eyes .

13.2. Light Method

1. Inspection is implemented over 30cm vertical distance and 30° incidence under 1000±200 lux. (As showed below)
2. Viewing direction for inspection over 30㎝ far and is 45° against from LCD (As showed below)



13.3. Classification Of Defects

13.3.1. Major defect

A major defect refers to a defect that may substantially degrade usability for product applications.

13.3.2. Minor defect

A minor defect refers to a defect which is not considered to be able substantially degrade the product application or a defect that deviates from existing standards almost unrelated to the effective use of the product or its operation.

Notes: If the LCD/LCM's cosmetic and display performance do not specify in "inspection criterion", it should be based on these delivered samples.

13.4. Sampling & Acceptable Quality Level

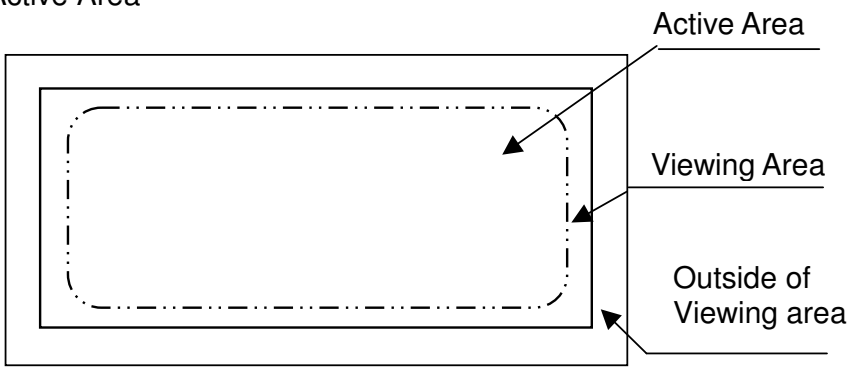
Level II, MIL-STD-105E

Inspection Item	Major defect	Minor defect
Appearance	0.4 %	0.65 %
Electrical test	0.4 %	0.65 %

13.5. Definition Of Inspection Area

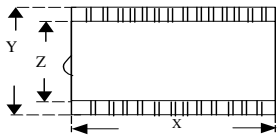
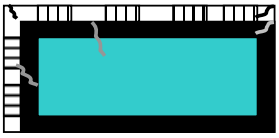
V.A: Viewing Area

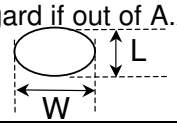
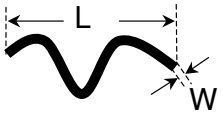
A.A: Active Area



13.6. Items And Criteria

13.6.1. Visual inspection criterion in cosmetic

Glass defect			
No	Item	Criteria	Remark
1	Dimension (Minor)	By engineering diagram	
2	Crack (Major)	Extensive crack 【Reject】	

LCD appearance defect				
No	Item	Criteria		Remark
1	Round type (Minor)	Defect Spec.	Permissible Q'ty	1: ϕ =(L+W)/2, L: Length, W: Width 2: Disregard if out of A.A. 
		$\phi \leqq$0.2mm	Disregard	
		0.2mm< $\phi \leqq$0.3mm	2	
		ϕ >0.3mm	0	
2	Line type (Minor)	Defect Spec.	Permissible Q'ty	1: L: Length, W: Width 2: Disregard if out of A.A 
		W$\leqq$0.5mm, L$\leqq$2.0mm	2	
		W$\leqq$0.5mm, L>2.0mm	0	
3	Polarizer bubble (Minor)	Defect Spec.	Permissible Q'ty	1: ϕ =(L+W)/2, L: Length, W: Width.
		Out of A.A	Disregard	
		Within A.A	0	

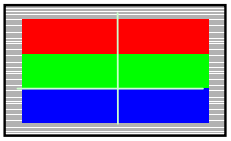
FPC			
No	Item	Criteria	Remark
1	Copper peeling (Minor)	Copper peeling 【Reject】	
2	No release film or Peeling (Minor)	No release film or peeling 【Reject】	

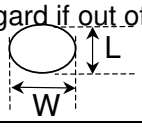
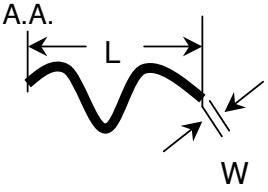
FPC				
3	Finger Spots, Impurities defect (Minor)	Defect Spec.	Permissible Q'ty	1.No bridge 2. Disregard if the dirty removed
		$\phi \leqq$0.35mm	2	
		ϕ >0.35mm	0	

Silicon			
No	Item	Criteria	Remark
1	Amount of silicon (Minor)	ITO exposed 【Reject】	

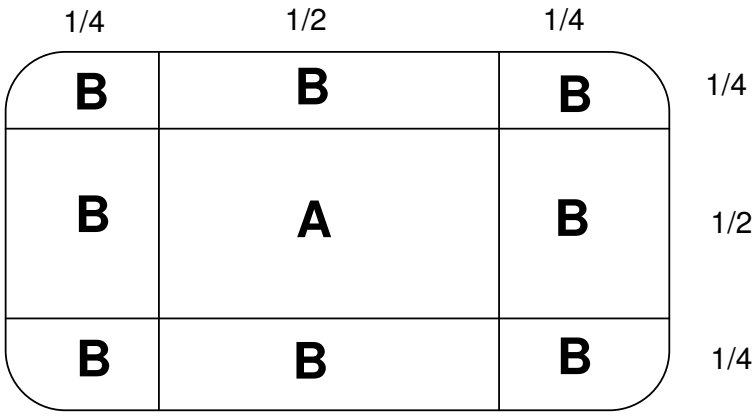
Bezel			
No	Defect	Criteria	Remark
1	Oxidized spot (Minor)	Oxidized spot, rust 【Reject】	
2	Outline deformation (Minor)	By engineering diagram	
3	Greasiness (Minor)	Greasiness 【Reject】	
4	Spots, round Type (Minor)	H$\leqq$By engineering diagram 【Disregard】	H=Total height (thickness)
5	Plating (Minor)	Bubble, peeling 【Reject】	

13.6.2. Visual inspection criterion in electrical display

No	Defect	Criteria	Remark
1	No display (Major)	Not allowed	
2	Missing line (Major)	Not allowed	
3	Darker or lighter line (Major)	Not allowed	

<table>
<tr><th>No</th><th>Defect</th><th colspan="4">Criteria</th><th>Remark</th></tr>
<tr><td>4</td><td>Weak line (Minor)</td><td colspan="4">By limit sample</td><td></td></tr>
<tr><td rowspan="4">5</td><td rowspan="4">Bright / Dark point (Minor)</td><td></td><td>A Area</td><td>B Area</td><td>Total</td><td rowspan="4">1:1sub-pixel: 1R or 1G or 1B 2:Point defect area≧1/2 sub pixel.
2.Point distance≧ 5mm
3.Refere to Note 1</td></tr>
<tr><td>Bright point</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>Dark dot point</td><td>1</td><td>1</td><td>2</td></tr>
<tr><td>Bright +Dark point</td><td>1</td><td>2</td><td>3</td></tr>
<tr><td rowspan="4">6</td><td rowspan="4">Round type (Minor)</td><td colspan="3">Spec.</td><td>Permissible Qty</td><td rowspan="4">1. ϕ =(L+W)/2, L: Length, W: Width
2. Disregard if out of A.A.
  </td></tr>
<tr><td colspan="3">ϕ ≦0.2mm</td><td>Disregard</td></tr>
<tr><td colspan="3">0.2mm< ϕ ≦0.3mm</td><td>2</td></tr>
<tr><td colspan="3">ϕ >0.3mm</td><td>0</td></tr>
<tr><td rowspan="3">7</td><td rowspan="3">Line type (Minor)</td><td colspan="3">Spec.</td><td>Permissible Qty</td><td rowspan="3">1. L: Length, W: Width
2. Disregard if out of A.A.
  </td></tr>
<tr><td colspan="3">W≦0.5mm, L≦2.0mm</td><td>2</td></tr>
<tr><td colspan="3">W≦0.5mm, L>2.0mm</td><td>0</td></tr>
<tr><td>8</td><td>Mura (Minor)</td><td colspan="4">By 5% ND filter invisible</td><td></td></tr>
</table>

Note 1

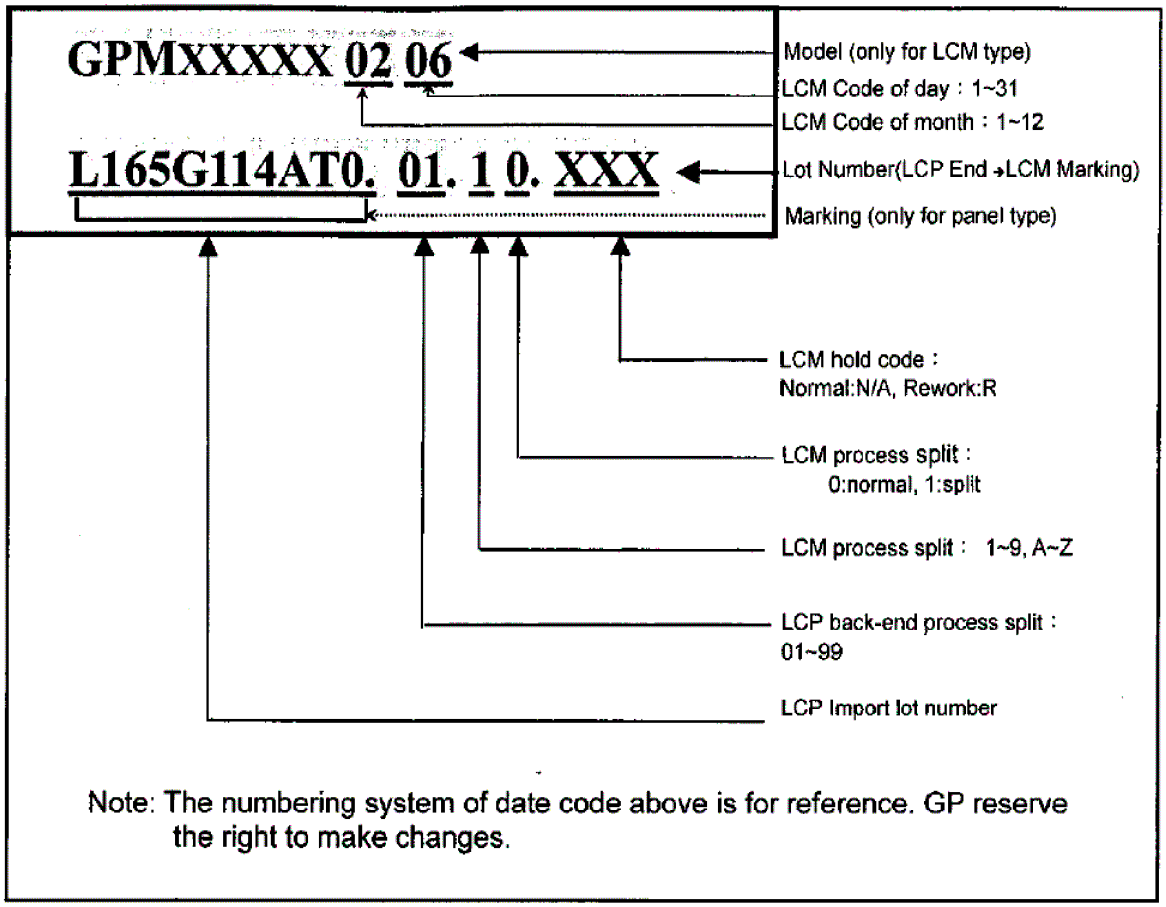


Please Follow the section separate to judgment the Bright or Dark Dots

13.6.3. Others

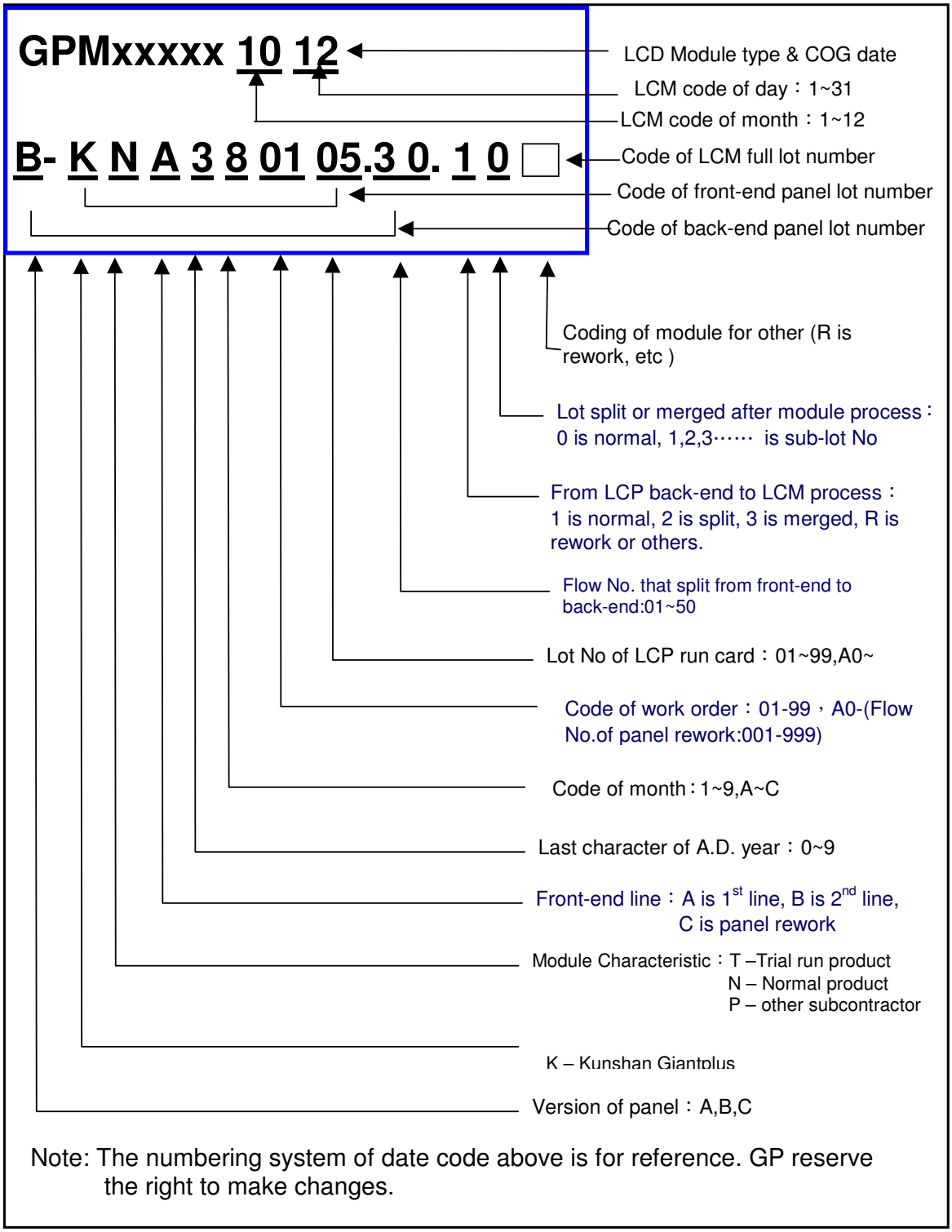
1. Issues that are not defined in this document shall be discussed and agreed with both parties. (Customer and supplier)
2. Unless otherwise agreed upon in writing, the criteria shall be applied to both parties. (Customer and supplier)

14. ILLUSTRATION OF LCD DATE CODE(GP)



Note: The numbering system of date code above is for reference. GP reserve the right to make changes.

15. ILLUSTRATION OF LCD DATE CODE(KGP)



Note: The numbering system of date code above is for reference. GP reserve the right to make changes.

16. RoHS COMPLIANT WARRANTY

RoHs Hazardous substances including:

- Cd< 100 ppm
- Pb< 1000 ppm
- Hg< 1000 ppm
- Cr +6 < 1000 ppm
- PBDE < 1000 ppm
- PBB < 1000 ppm

17. PRECAUTIONS FOR USE

17.1.Safety

(1) Do not swallow any liquid crystal, even if there is no proof that liquid crystal is poisonous.

(2) If the LCD panel breaks, be careful not to get liquid crystal to touch your skin.

(3) If skin is exposed to liquid crystal, wash the area thoroughly with alcohol or soap.

17.2.Storage Conditions

(1) Store the panel or module in a dark place where the temperature is 23±5℃ and the humidity is below 50±20%RH.

(2) Store in anti-static electricity container.

(3) Store in clean environment, free from dust, active gas, and solvent.

(4) Do not place the module near organics solvents or corrosive gases.

(5) Do not crush, shake, or jolt the module.

(6) Do not exposed to direct sun light of fluorescent lamps.

17.3.Installing LCD Module

Attend to the following items when installing the LCM.

(1) Cover the surface with a transparent protective plate or touch panel to protect the polarizer and LC cell.

(2) When assembling the LCM into other equipment, the spacer to the bit between the LCM and the fitting plate should have enough height to avoid causing stress to the module surface, refer to the individual specifications for measurements. The measurement tolerance should be ±0.1mm.

17.4.Precautions For Operation

(1) Viewing angle varies with the change of liquid crystal driving voltage (Vo). Adjust

Vo to show the best contrast.

(2) Driving the LCD in the voltage above the limit will shorten its lifetime.

(3) Response time is greatly delayed at temperature below the operating temperature range. However, this does not mean the LCD will be out of the order. It will recover when it returns to the specified temperature range.

(4) When turning the power on, input each signal after the positive/negative voltage becomes stable.

(5) Do not apply water or any liquid on product which composed of T/P.

17.5. Handling Precautions

(1) Avoid static electricity which can damage the CMOS LSI; please wear the wrist strap when handling.

(2) The polarizing plate of the display is very fragile. so, please handle it very carefully.

(3) Do not give external shock.

(4) Do not apply excessive force on the surface; it may cause display abnormal .

(5) Do not wipe the polarizing plate with a dry cloth, as it may easily scratch the surface of plate.

(6) Do not use ketonics solvent & Aromatic solvent, use with a soft cloth soaked with a cleaning naphtha solvent.

(7) Do not operate it above the absolute maximum rating.

(8) Do not remove the panel or frame from the module.

(9) Do not apply water or any liquid on product, which composed of T/P.

17.6. Warranty

(1) The period is within 12 months since the date of shipping out under normal using and storage conditions.

(2) The warranty will be avoided in case of defect induced by customer.

18. FACTORY

For the consideration of mass production convenience, this model will be manufactured in the factories listed below.

FACTORY NAME: GIANTPLUS TECHNOLOGY CO., LTD
FACTORY ADDRESS: No.15 Industrial Rd., Lu-Chu Li, Toufen Town
351 Miao-Li County, Taiwan, R.O.C..
FACTORY PHONE: TEL: 886-37-611-611 FAX: 886-37-613-166
FACTORY ADDRESS: No.1127,Heping Rd.,Bade City,Taoyuan,334, Taiwan, R.O.C..
FACTORY PHONE: TEL: 886-3-3679978 FAX: 886-3-3670661

FACTORY NAME: KUNSHAN GIANTPLUS OPTOELECTRONICS
TECHNOLOGY CO., LTD.
FACTORY ADDRESS: No.88,HuanQing Rd., Hitech Industrial Park, Cheng-Bei Town,
KunShan City, JiangShu Province, China.
FACTORY PHONE: TEL:86-512-57780-988 FAX : 86-512-57780-503

FACTORY NAME: SHENZHEN GIANTPLUS OPTOELEC. DISPLAY CO., LTD.
FACTORY ADDRESS: Building A, Distict A ,MinZhu99 Industrial City,
ShaJing Industrial Park, BaoAn District, ShenZhen, China
FACTORY PHONE: TEL: 86-755-29720-088 FAX : 86-755-29720-828

19. REVISION HISTORY

Version	Revise record	Date
A	New version	2010/1/19