8MMINID4-CPU

(i.MX8M Mini Reference Board)

Table of Content

Revision History

Rev. Code	Date	By	Description
A	2018-07-27	Joshua	Initial version
B	2018-11-02	Joshua	1. Change WIFI/BT module to LBEE5HY1MW (CYW43455 based) 2. Add R134, R135 for BOOT_MODE3 option to TESTMODE for compatible design with i.MX8M Nano; 3. Change J4_Pin56 from GND to TESTMODE(BOOT_MODE3) for compatible design with i.MX8M Nano; 4. Remove R62, R107, R128 to simplify the optional design; 5. Remove C7 for NVCC_3V3; 6. Update the symbol of i.MX8M Mini: > Correct naming for AB13 from PVCC0_1V8 to PVCC0_1P8; > Correct power domain for B27, C26 from NVCC_CLK To VDD_24M_XTAL_1P8; > Correct power domain for J23, J24 from VDDA_1P8 to VDD_ANA1_1P8; > Correct power domain for A22, B22, F22, A23, B23, F23 to VDD_USB_3P3; > Correct power domain for D22, E19, D23, E22 to VDD_USB_1P8, and also adjust the pin locations.
B1	2019-06-21	Joshua	1. Change U4 to NAND Flash socket only, without NAND Flash device installed; 2. Populate R106, as external PU is necessary for Boundary Scan Mode, also update the note; 3. Update U8 Part Number BD71847MWV-E2 to BD71847AMWV-E2; 4. Update the Min/Typ/Max operating range for I.MX8M Mini power supplies; 5. Add note for changing BD71847 BUCK1/2/5 output voltage according to the new operation range; 6. Add note for all IOs that internal pull up/down is not supported in 3.3V mode; 7. Add note for Boundary Scan mode: BOOT_MODE0, BOOT_MODE1, JTAG_MOD and TEST_MODE must be pulled to "1101" for i.MX8M Mini to enter Boundary Scan mode;

1. Interrupted lines coded with the same letter or letter combinations are electrically connected.

2. Device type number is for reference only. The number varies with the manufacturer.

3. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

4. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

Preliminary - Subject to Change without Notice!

This board was designed for maximum flexibility in software development and demonstrates multiple functions possible with i.MX processors. Although best design practices have been applied, some areas may not be suitable for a mass-production design.

Microcontroller Product Group
6501 William Cannon Drive West
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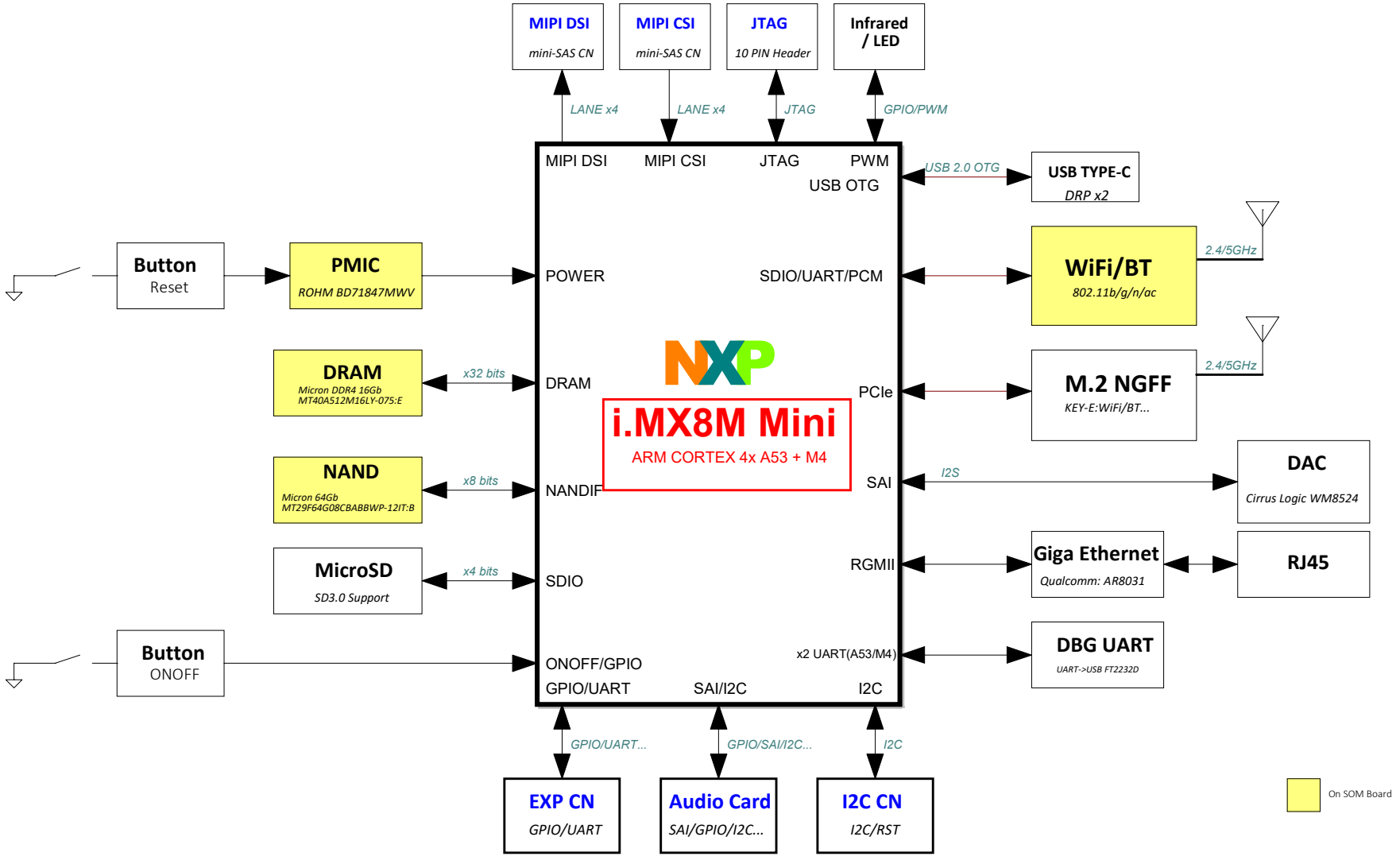
ICAP Classification: CP: IUO: X PUBI:

Designer: Joshua Wu	Drawing Title: 8MMINID4-CPU	
Drawn by: Joshua Wu	Page Title: Title and Rev History	
Approved: <Approver>	Size C / Document Number SCH-35104 PDF: SPF-35104	Rev B1
	Date: Friday, June 21, 2019	Sheet 1 of 14

8MMINID4-EVK Block Diagram



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Drawn by: Joshua Wu	Page Title: Block Diagram	
Approved: <Approver>	Size C	Document Number SCH-35104 PDF: SPF-35104 Rev B1
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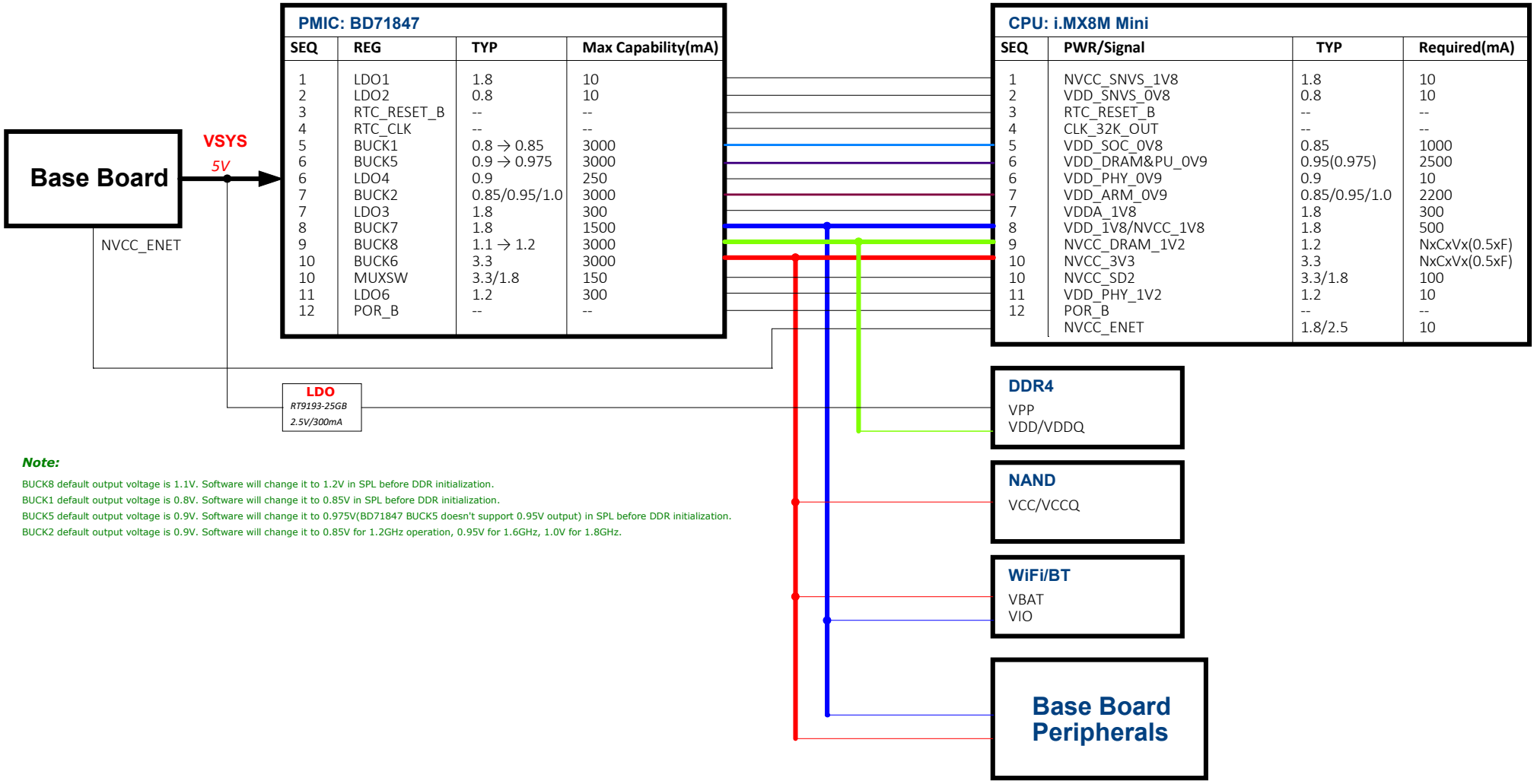
8MMINID4-EVK PWR TREE



PMIC: BD71847

SEQ	REG	TYP	Max Capability(mA)
1	LDO1	1.8	10
2	LDO2	0.8	10
3	RTC_RESET_B	--	--
4	RTC_CLK	--	--
5	BUCK1	0.8 → 0.85	3000
6	BUCK5	0.9 → 0.975	3000
6	LDO4	0.9	250
7	BUCK2	0.85/0.95/1.0	3000
7	LDO3	1.8	300
8	BUCK7	1.8	1500
9	BUCK8	1.1 → 1.2	3000
10	BUCK6	3.3	3000
10	MUXSW	3.3/1.8	150
11	LDO6	1.2	300
12	POR_B	--	--

CPU: i.MX8M Mini

SEQ	PWR/Signal	TYP	Required(mA)
1	NVCC_SNVS_1V8	1.8	10
2	VDD_SNVS_0V8	0.8	10
3	RTC_RESET_B	--	--
4	CLK_32K_OUT	--	--
5	VDD_SOC_0V8	0.85	1000
6	VDD_DRAM&PU_0V9	0.95(0.975)	2500
6	VDD_PHY_0V9	0.9	10
7	VDD_ARM_0V9	0.85/0.95/1.0	2200
7	VDDA_1V8	1.8	300
8	VDD_1V8/NVCC_1V8	1.8	500
9	NVCC_DRAM_1V2	1.2	NxCxVx(0.5xF)
10	NVCC_3V3	3.3	NxCxVx(0.5xF)
10	NVCC_SD2	3.3/1.8	100
11	VDD_PHY_1V2	1.2	10
12	POR_B	--	--
	NVCC_ENET	1.8/2.5	10

Note:

BUCK8 default output voltage is 1.1V. Software will change it to 1.2V in SPL before DDR initialization.
BUCK1 default output voltage is 0.8V. Software will change it to 0.85V in SPL before DDR initialization.
BUCK5 default output voltage is 0.9V. Software will change it to 0.975V(BD71847 BUCK5 doesn't support 0.95V output) in SPL before DDR initialization.
BUCK2 default output voltage is 0.9V. Software will change it to 0.85V for 1.2GHz operation, 0.95V for 1.6GHz, 1.0V for 1.8GHz.

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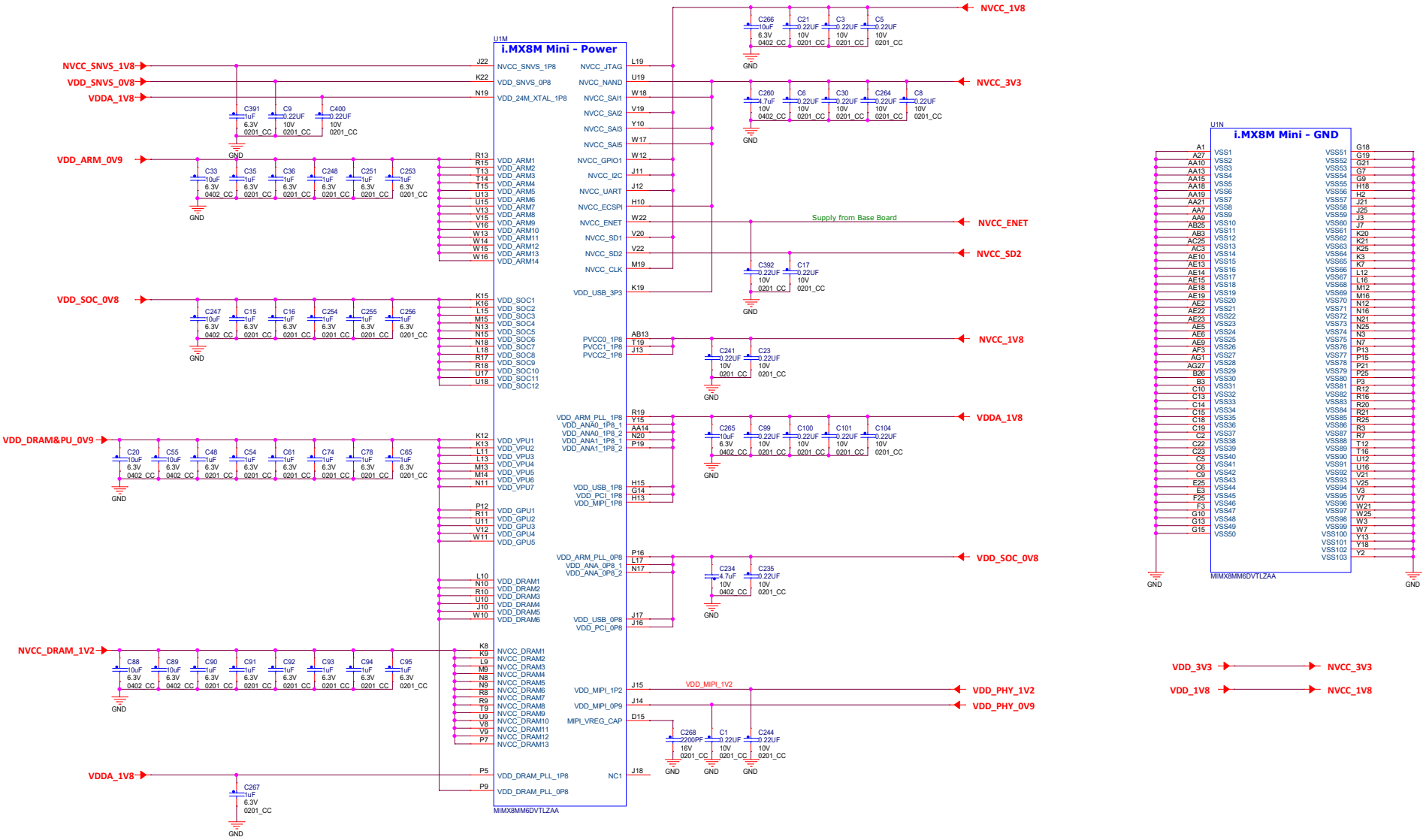
Approved: <Approver>	Size C	Document Number SCH-35104 PDF: SPF-35104 Rev B1
	Date: Friday, June 21, 2019	Sheet 3 of 14

i.MX8M Mini PWR



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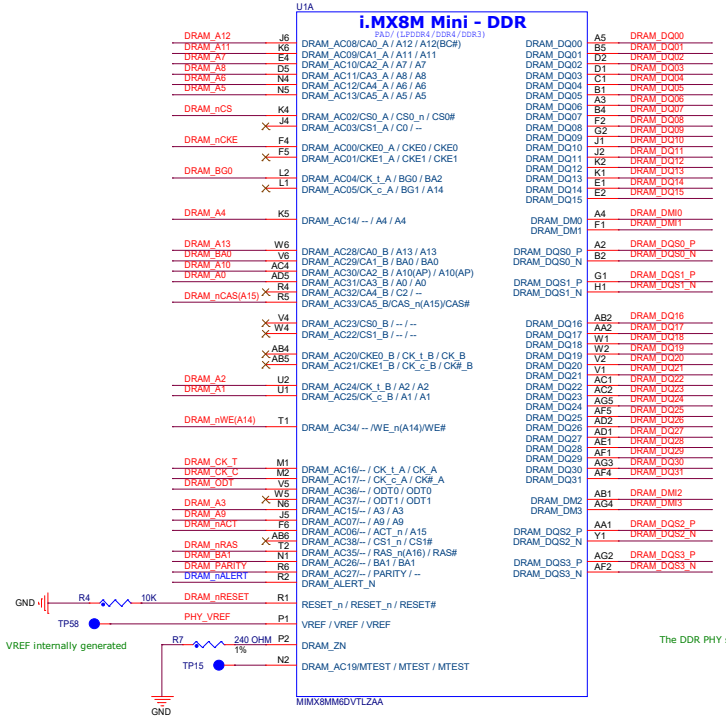
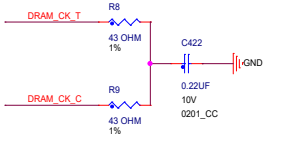
Drawn by: Joshua Wu	Page Title: CPU PWR	
Approved: <Approver>	Size: C; Document Number: SCH-35104 PDF: SPF-35104; Rev: B1	
	Date: Friday, June 21, 2019; Sheet 4 of 14	

DDR4 2GB

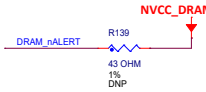
Power supply voltage ramp:

RESET_n is held LOW.
VPP should be powered up before VDD/VDDQ

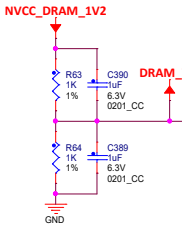


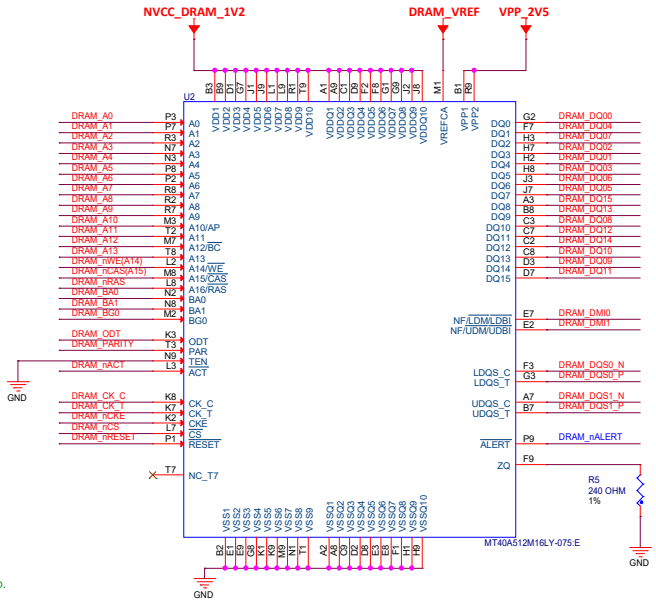


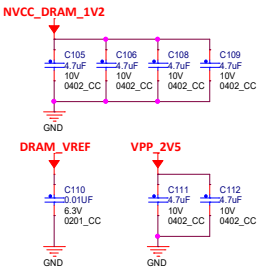
CK is routed as 85 Ohm differential trace and references GND.

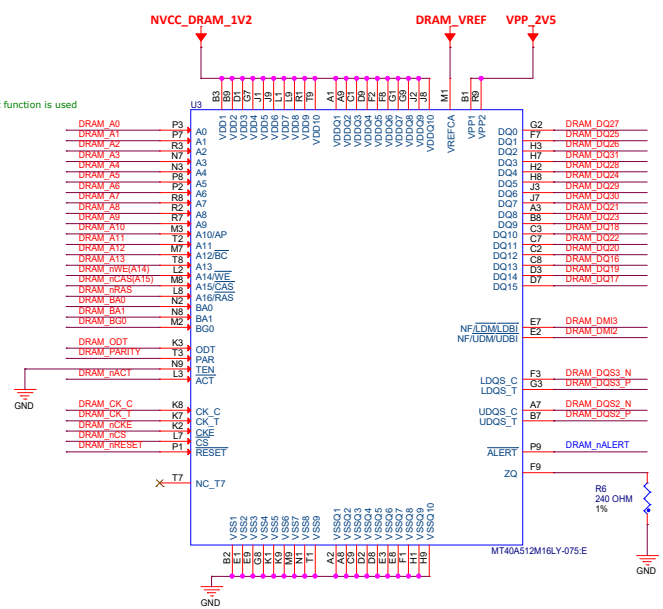


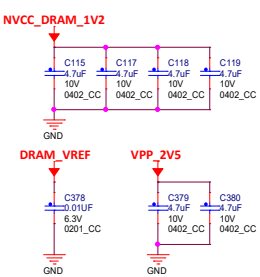
The DDR PHY should enable 48 Ohm internal pull-up termination on DRAM_nALERT if alert function is used









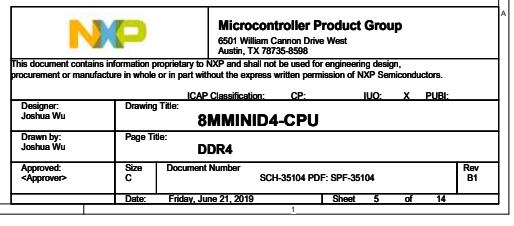


Data Bus

Pin Name	LPDDR4	DDR4
DRAM_DQS0_P	DQS0_t_A	DQSL_t_A
DRAM_DQS0_N	DQS0_c_A	DQSL_c_A
DRAM_DM0	DMI0_A	DML_n_A / DBIL_n_A
DRAM_DQ00	DQ0_A	DQL0_A
DRAM_DQ01	DQ1_A	DQL1_A
DRAM_DQ02	DQ2_A	DQL2_A
DRAM_DQ03	DQ3_A	DQL3_A
DRAM_DQ04	DQ4_A	DQL4_A
DRAM_DQ05	DQ5_A	DQL5_A
DRAM_DQ06	DQ6_A	DQL6_A
DRAM_DQ07	DQ7_A	DQL7_A
DRAM_DQS1_P	DQS1_t_A	DQSU_t_A
DRAM_DQS1_N	DQS1_c_A	DQSU_c_A
DRAM_DM1	DMI1_A	DMU_n_A / DBIU_n_A
DRAM_DQ08	DQ8_A	DQU0_A
DRAM_DQ09	DQ9_A	DQU1_A
DRAM_DQ10	DQ10_A	DQU2_A
DRAM_DQ11	DQ11_A	DQU3_A
DRAM_DQ12	DQ12_A	DQU4_A
DRAM_DQ13	DQ13_A	DQU5_A
DRAM_DQ14	DQ14_A	DQU6_A
DRAM_DQ15	DQ15_A	DQU7_A
DRAM_DQS2_P	DQS0_t_B	DQSL_t_B
DRAM_DQS2_N	DQS0_c_B	DQSL_c_B
DRAM_DM2	DMI0_B	DML_n_B / DBIL_n_B
DRAM_DQ16	DQ0_B	DQL0_B
DRAM_DQ17	DQ1_B	DQL1_B
DRAM_DQ18	DQ2_B	DQL2_B
DRAM_DQ19	DQ3_B	DQL3_B
DRAM_DQ20	DQ4_B	DQL4_B
DRAM_DQ21	DQ5_B	DQL5_B
DRAM_DQ22	DQ6_B	DQL6_B
DRAM_DQ23	DQ7_B	DQL7_B
DRAM_DQS3_P	DQS1_t_B	DQSU_t_B
DRAM_DQS3_N	DQS1_c_B	DQSU_c_B
DRAM_DM3	DMI1_B	DMU_n_B / DBIU_n_B
DRAM_DQ24	DQ8_B	DQU0_B
DRAM_DQ25	DQ9_B	DQU1_B
DRAM_DQ26	DQ10_B	DQU2_B
DRAM_DQ27	DQ11_B	DQU3_B
DRAM_DQ28	DQ12_B	DQU4_B
DRAM_DQ29	DQ13_B	DQU5_B
DRAM_DQ30	DQ14_B	DQU6_B
DRAM_DQ31	DQ15_B	DQU7_B

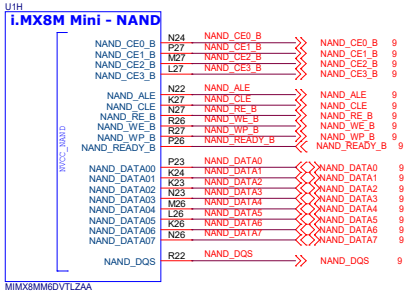
Command/Address

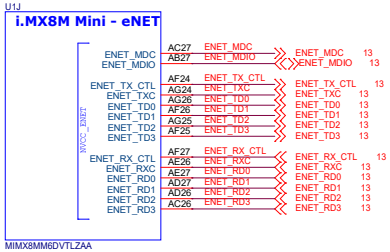
Pin Name	LPDDR4	DDR4
DRAM_RESET_N	RESET_N	RESET_n
DRAM_ALERT_N	MTEST1	ALERT_n / MTEST1
DRAM_AC00	CKE0_A	CKE0
DRAM_AC01	CKE1_A	CKE1
DRAM_AC02	CS0_A	CS0_n
DRAM_AC03	CS1_A	C0
DRAM_AC04	CK_t_A	BG0
DRAM_AC05	CK_c_A	BG1
DRAM_AC06	/	ACT_n
DRAM_AC07	/	A9
DRAM_AC08	CA0_A	A12
DRAM_AC09	CA1_A	A11
DRAM_AC10	CA2_A	A7
DRAM_AC11	CA3_A	A8
DRAM_AC12	CA4_A	A6
DRAM_AC13	CA5_A	A5
DRAM_AC14	/	A4
DRAM_AC15	/	A3
DRAM_AC16	/	CK_t_A
DRAM_AC17	/	CK_c_A
DRAM_AC19	MTEST	MTEST
DRAM_AC20	CKE0_B	CK_t_B
DRAM_AC21	CKE1_B	CK_c_B
DRAM_AC22	CS1_B	/
DRAM_AC23	CS0_B	/
DRAM_AC24	CK_t_B	A2
DRAM_AC25	CK_c_B	A1
DRAM_AC26	/	BA1
DRAM_AC27	/	PARITY
DRAM_AC28	CA0_B	A13
DRAM_AC29	CA1_B	BA0
DRAM_AC30	CA2_B	A10 / AP
DRAM_AC31	CA3_B	A0
DRAM_AC32	CA4_B	C2
DRAM_AC33	CA5_B	CAS_n / A15
DRAM_AC34	/	WE_n / A14
DRAM_AC35	/	RAS_n / A16
DRAM_AC36	/	ODT0
DRAM_AC37	/	ODT1
DRAM_AC38	/	CS1_n
DRAM_ZN	ZQ	ZQ
DRAM_VREF	VREF	VREF

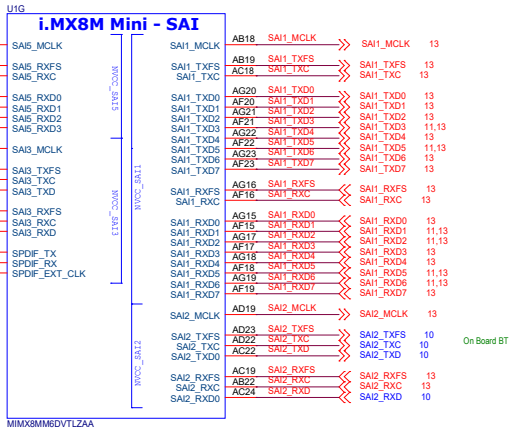


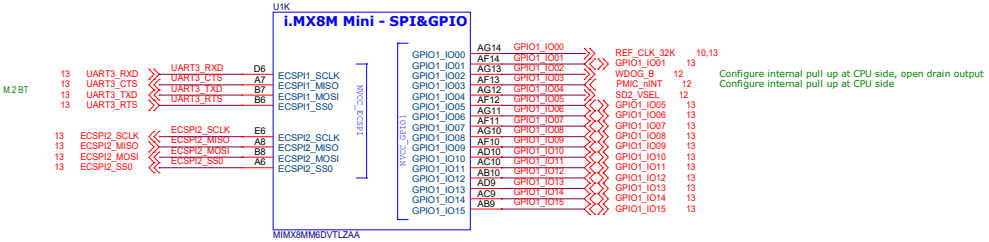
i.MX8M Mini IO Interface

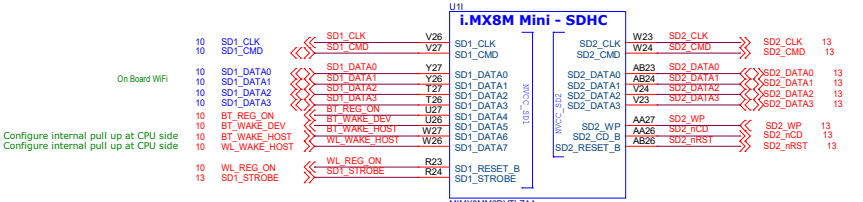
Caution:
IO internal pull up/down is not supported in 3.3V mode, must disable the internal pull up/down via software and use external pull up/down resistors instead.
All IO pin groups are impacted except for XTAL, DDR, PCI, USB and MIPI PHY IO's.
See Errata e50080 for detailed information.

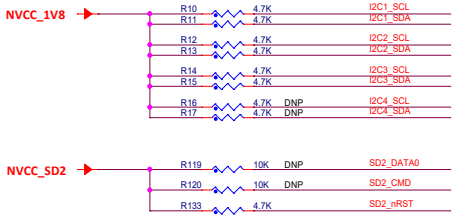


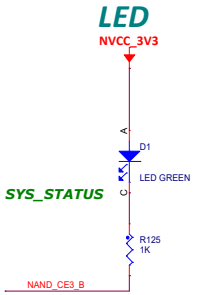


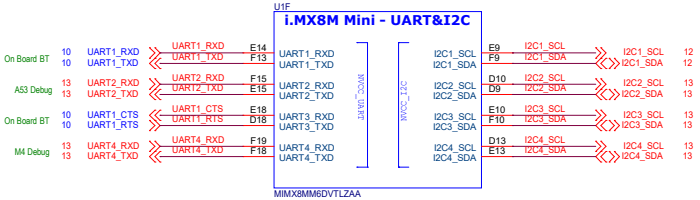












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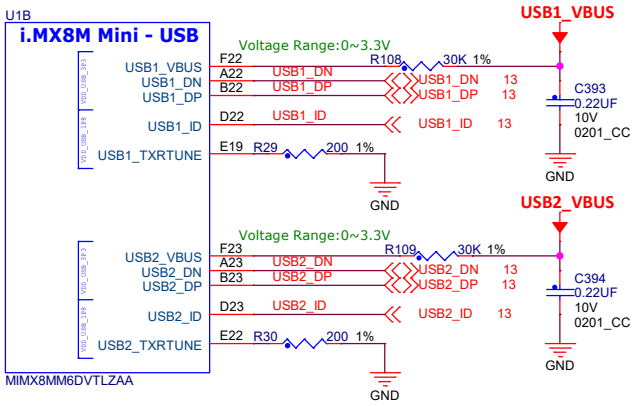
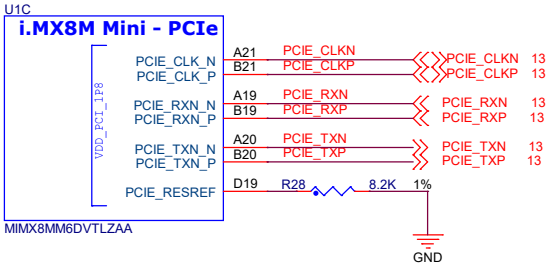
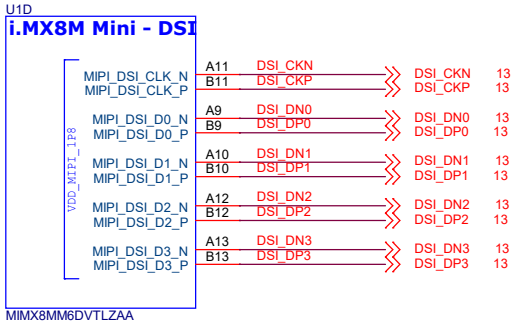
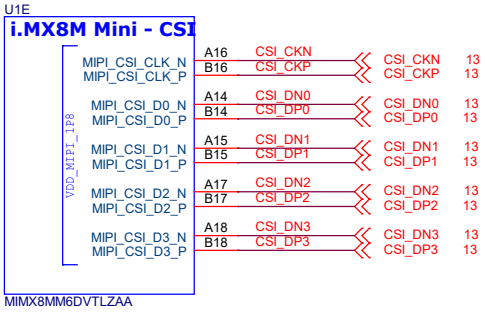
i.MX8M Mini PHYs









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Drawn by: Joshua Wu	Page Title: CPU PHY	
Approved: <Approver>	Size B	Document Number SCH-35104 PDF: SPF-35104 Rev B1
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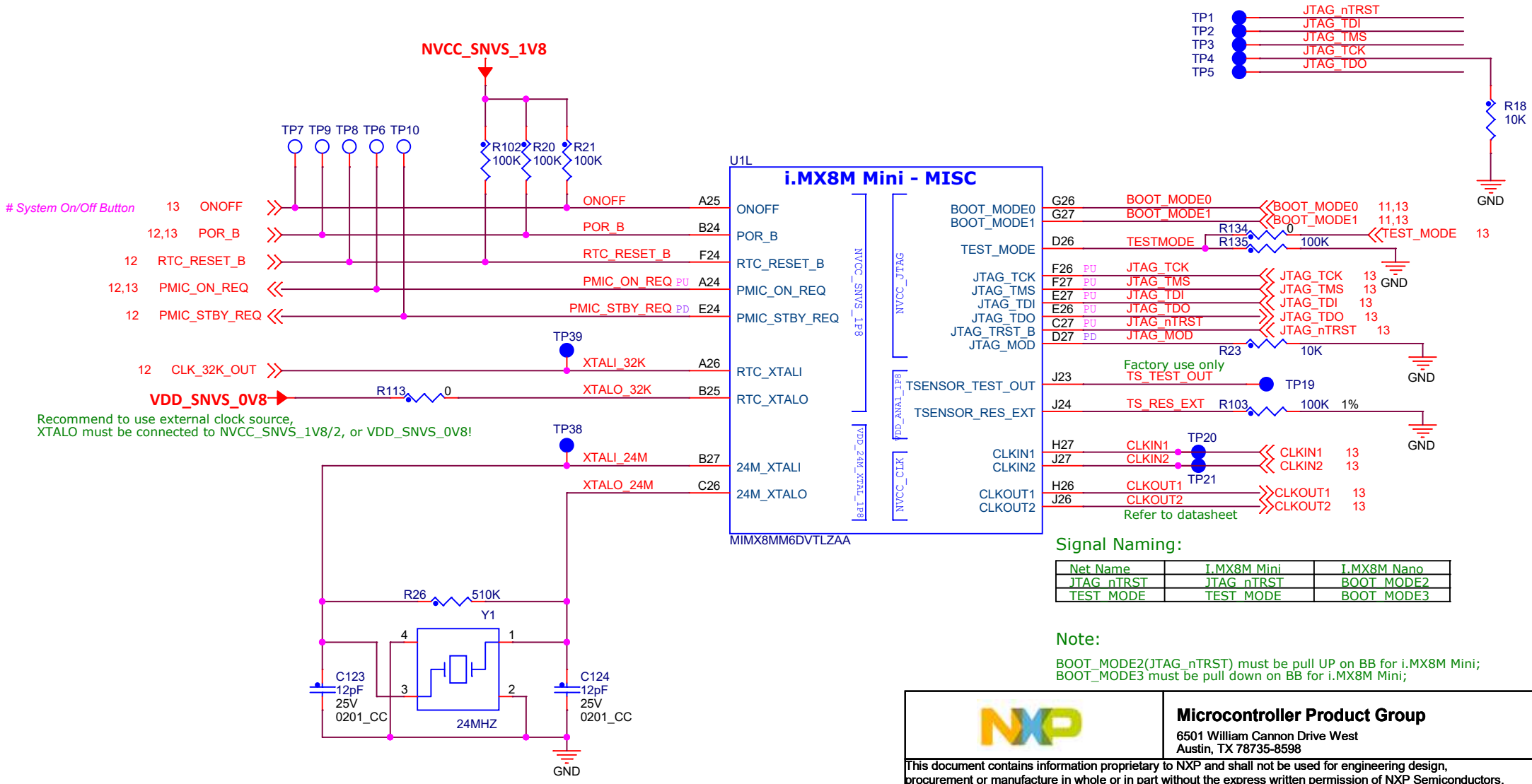
i.MX8M Mini MISC

JTAG Debug



Signal Naming:

Net Name	I.MX8M Mini	I.MX8M Nano
JTAG_nTRST	JTAG_nTRST	BOOT_MODE2
TEST_MODE	TEST_MODE	BOOT_MODE3

Note:

BOOT_MODE2(JTAG_nTRST) must be pull UP on BB for i.MX8M Mini;
BOOT_MODE3 must be pull down on BB for i.MX8M Mini;

Caution:

BOOT_MODE0, BOOT_MODE1, JTAG_MOD and TEST_MODE must be pulled to "1101" for i.MX8M Mini to enter Boundary Scan mode.

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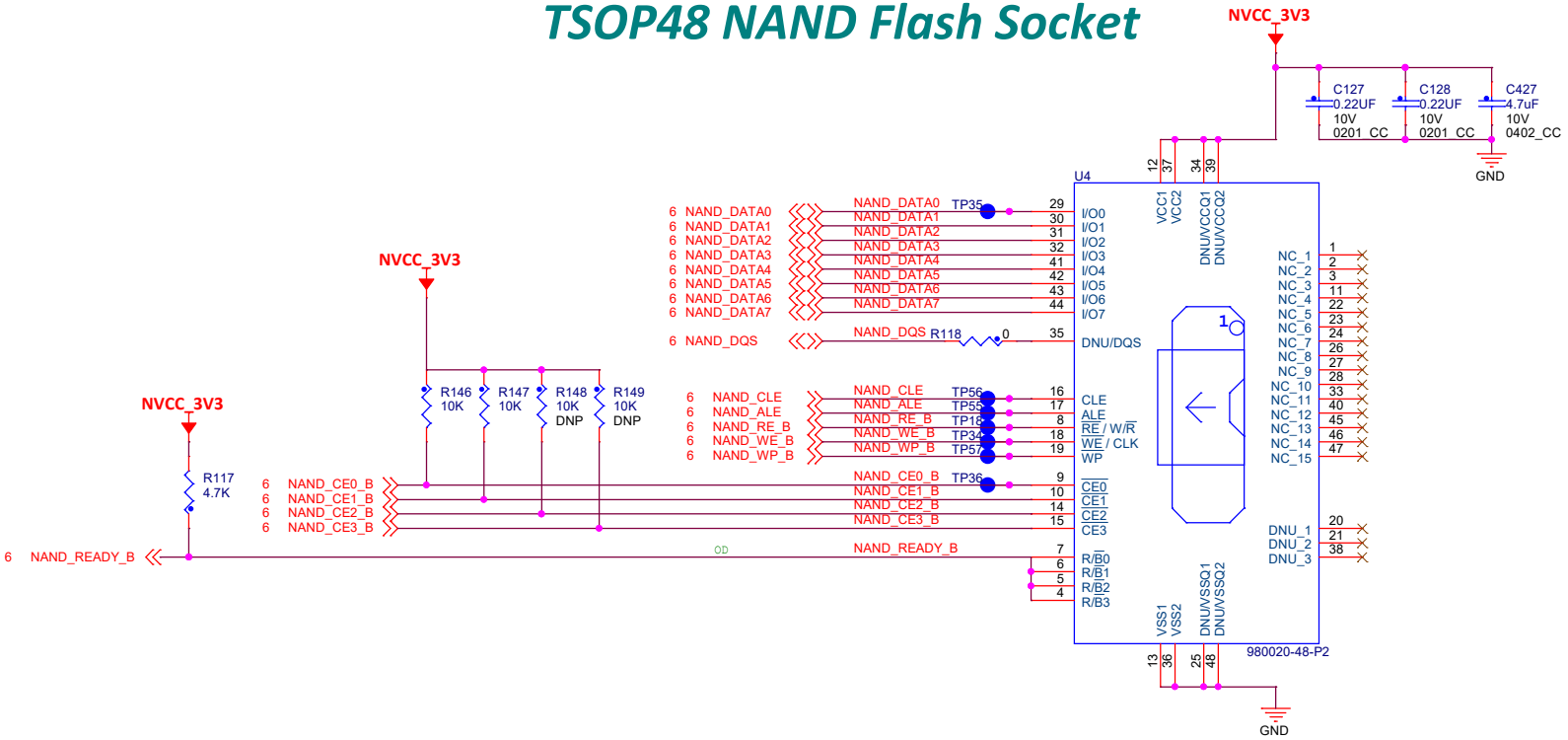
Storage

TSOP48 NAND Flash Socket



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Drawn by: Joshua Wu	Page Title: **NAND**	
Approved: <Approver>	Size B	Document Number SCH-35104 PDF: SPF-35104 Rev B1
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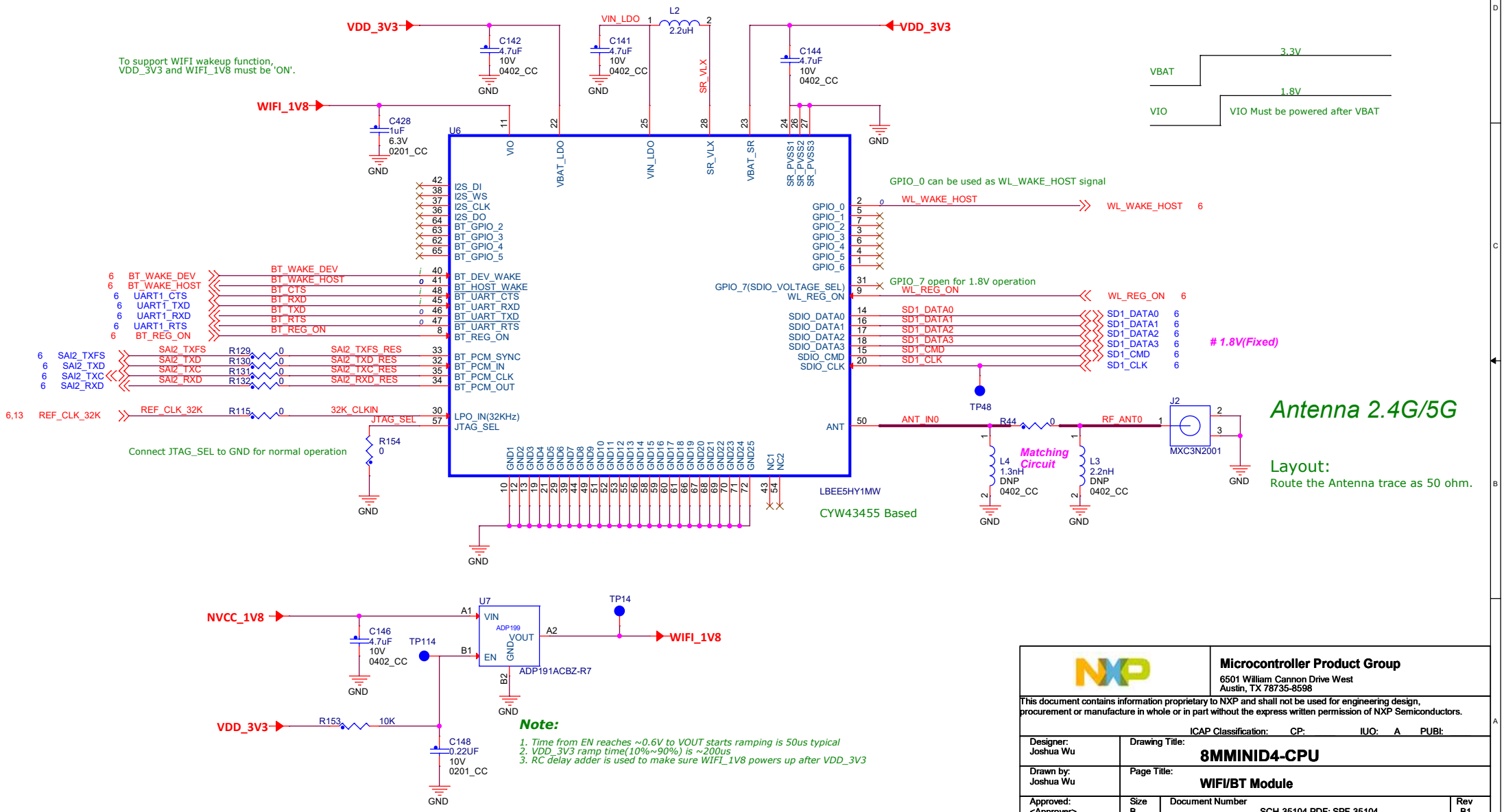
2.4G/5G WIFI/BT Module



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Drawn by: Joshua Wu	Page Title: WIFI/BT Module		
Approved: <Approver>	Size B	Document Number SCH-35104 PDF: SPF-35104	Rev B1
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Boot Mode and CFG Switch

Caution:
IO internal pull up/down is not supported in 3.3V mode, must disable the internal pull up/down via software and use external pull up/down resistors instead.
All IO pin groups are impacted except for XTAL, DDR, PCI, USB and MIPI PHY IO's.
See Errata e50080 for detailed information.

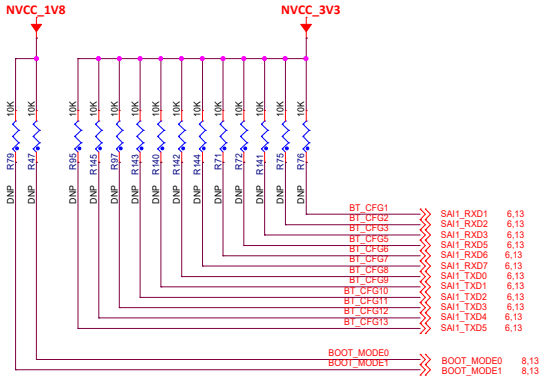
i.MX8M Mini ROM Fuse

	Address	7	6	5	4	3	2	1	0
	0x470[15:8]	**BOOT_CFG[15]**	**BOOT_CFG[14]**	**BOOT_CFG[13]**	**BOOT_CFG[12]**	**BOOT_CFG[11]**	**BOOT_CFG[10]**	**BOOT_CFG[9]**	**BOOT_CFG[8]**
	0x470[15:8]	Infinit-Loop (Debug USE only) 0 - Disable 1 - Enable	001 - SD/eSD			Port Select: 00 - uSDHC1 01 - uSDHC2 10 - uSDHC3		Power Cycle Enable '0' - No power cycle '1' - Enabled via	SD Loopback Clock Source Sel (for SDR50 and SDR104 only) '0' - through SD pad '1' - direct
	0x470[15:8]		010 - MMC/eMMC						
	0x470[15:8]		011 - NAND			Pages In Block: 00 - 128 01 - 64 10 - 32 11 - 256		Nand_Row_address_bytes: 00 - 3 01 - 2 10 - 4 11 - 5	
	0x470[15:8]		100 - QSPI			Flash Auto Probe	FLASH_TYPE 000-Device supports 3B read by default 001-Device supports 4B read by default 010-HyperFlash 1V8 011-HyperFlash 3V3 100-MXIC Octal DDR		
	0x470[15:8]		110 - SPI NOR			Port Select: 000 - eCSPI1 001 - eCSPI2 010 - eCSPI3			SPI Addressing: 0 - 3-bytes (24-bit) 1 - 2-bytes (16-bit)
	0x470[15:8]	Others - Reserved for future use							
		BOOT_CFG[7]	**BOOT_CFG[6]**	**BOOT_CFG[5]**	**BOOT_CFG[4]**	**BOOT_CFG[3]**	**BOOT_CFG[2]**	**BOOT_CFG[1]**	**BOOT_CFG[0]**
SD/eSD	0x470[7:0]	Fast Boot: 0 - Regular 1 - Fast Boot	Reserved	Reserved	Bus Width: 0 - 1-bit 1 - 4-bit	Speed 000 - Normal/SDR12 001 - High/SDR25 010 - SDR50 011 - SDR104 101 - Reserved for DDR50 Others - Reserved			Reserved
MMC/eMMC	0x470[7:0]		Bus Width: 000 - 1-bit 001 - 4-bit 010 - 8-bit 101 - 4-bit DDR (MMC 4.4) 110 - 8-bit DDR (MMC 4.4) Else - reserved.			Speed 00 - Normal 01 - High 10 - Reserved for HS200 11 - Reserved		USDHC IO VOLTAGE SELECTION For Normal Boot Mode 0 - 3.3V 1 - 1.8V	USDHC IO VOLTAGE SELECTION For Manufacture Mode 0 - 3.3V 1 - 1.8V
NAND	0x470[7:0]	BT_TOGGLEMODE	BOOT_SEARCH_COUNT: 00 - 2 01 - 2 10 - 4 11 - 8		Toggle Mode 33MHz Preamble Delay, Read Latency: '000' - 16 GPMICLK cycles. '001' - 1 GPMICLK cycles. '010' - 2 GPMICLK cycles. '011' - 3 GPMICLK cycles. '100' - 4 GPMICLK cycles. '101' - 5 GPMICLK cycles. '110' - 6 GPMICLK cycles. '111' - 7 GPMICLK cycles. '1111'- 15 GPMICLK cycles.			Reserved
FlexSPI	0x470[7:0]	HOLD TIME: 00 - 500us 01 - 1ms 10 - 3ms 11 - 10ms		FLASH Auto Probe Type		FlexSPI FLASH Dummy Cycle			
SPINOR	0x470[7:0]	CS select SPI only: 00 - CS#0 default 01 - CS#1 10 - CS#2 11 - CS#3	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

BT_CFG Pins:

SAI1_RXD0 BT0_CFG0
SAI1_RXD1 BT0_CFG1
SAI1_RXD2 BT0_CFG2
SAI1_RXD3 BT0_CFG3
SAI1_RXD4 BT0_CFG4
SAI1_RXD5 BT0_CFG5
SAI1_RXD6 BT0_CFG6
SAI1_RXD7 BT0_CFG7

SAI1_TXD0 BT0_CFG8
SAI1_TXD1 BT0_CFG9
SAI1_TXD2 BT0_CFG10
SAI1_TXD3 BT0_CFG11
SAI1_TXD4 BT0_CFG12
SAI1_TXD5 BT0_CFG13
SAI1_TXD6 BT0_CFG14
SAI1_TXD7 BT0_CFG15



Note:

1. Bootcfg/SAI1 singals have internal PD before and after POR_B reset is deasserted!

2. Standalone SOM board can support NAND boot by populating some of the pull-up resistors.
- For original intalled NAND flash, populate R79, R95, R97, R143, R145
- For other NAND flash parts, populate according to specific part configuration

3. When using Base Board for Multi boot selection, you must keep the resistors DNP on SOM board!

Boot Mode

BOOT_MODE1	BOOT_MODE0

BOOT TYPE:

00 Boot From Fuses
01 Serial Downloader
10 Internal Boot (Development)
11 Reserved

Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

ICAP Classification: CP: IUO: X PUBI:

Designer: Joshua Wu	Drawing Title: 8MMINID4-CPU	
Drawn by: Joshua Wu	Page Title: BOOT_CFG	
Approved: <Approver>	Size C	Document Number SCH-35104 PDF: SPF-35104 Rev B1
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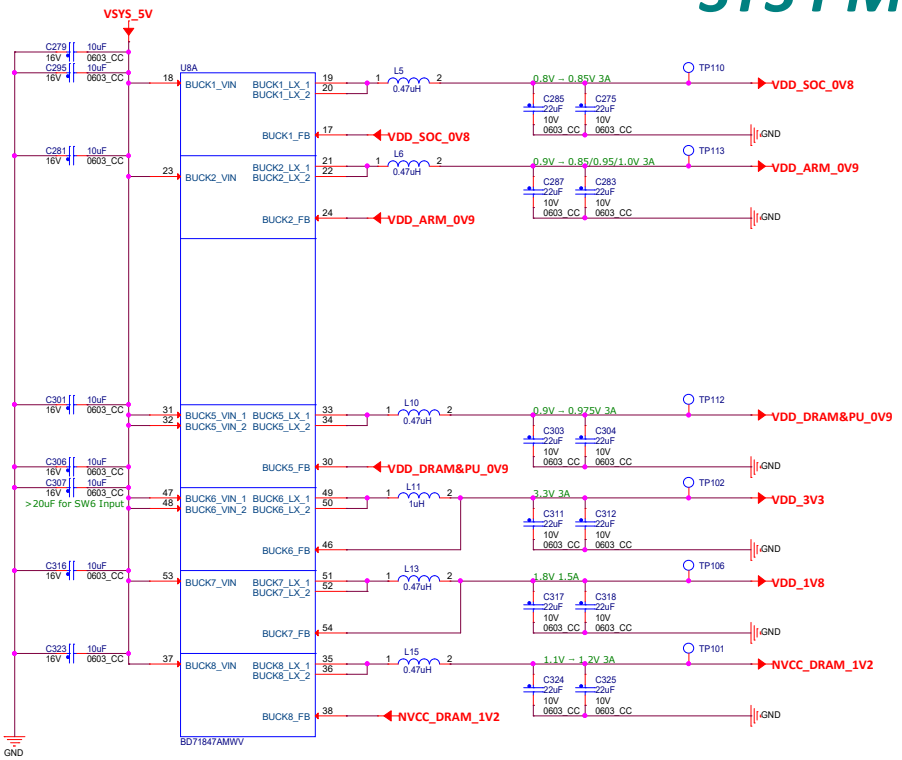
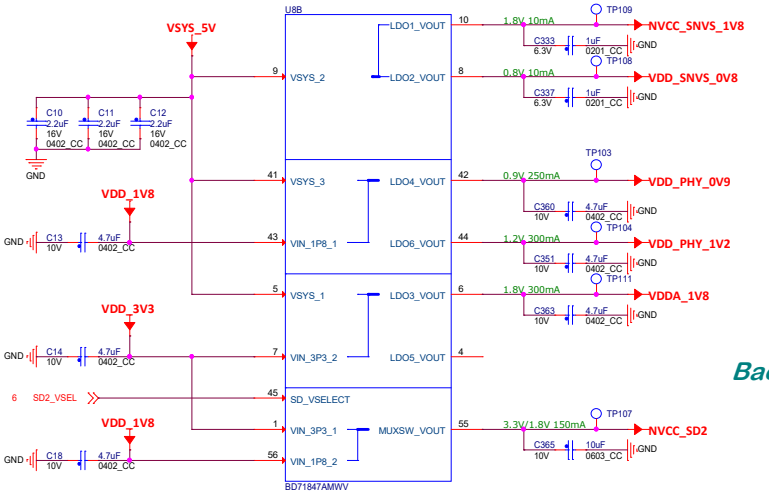
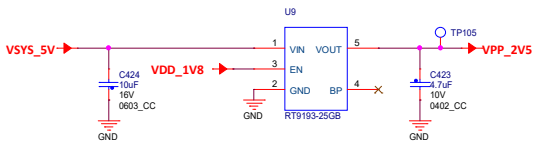
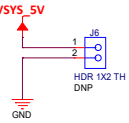
SYS PMIC







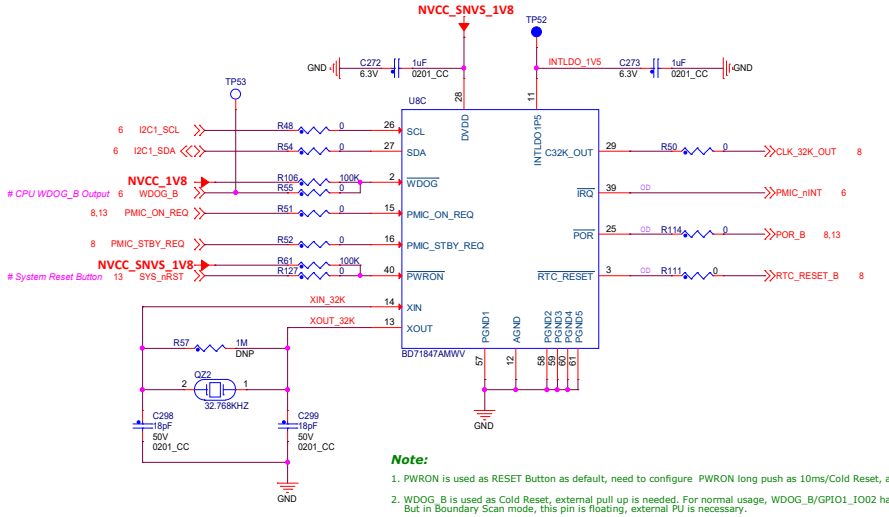
Backup PWR Supply



GND Testpoints

Note:

BUCK8 default output voltage is 1.1V. Software will change it to 1.2V in SPL before DDR initialization.
BUCK1 default output voltage is 0.8V. Software will change it to 0.85V in SPL before DDR initialization.
BUCK5 default output voltage is 0.9V. Software will change it to 0.975V(BD71847 BUCK5 doesn't support 0.95V output) in SPL before DDR initialization.
BUCK2 default output voltage is 0.9V. Software will change it to 0.85V for 1.2GHz operation, 0.95V for 1.6GHz, 1.0V for 1.8GHz.



Note:

1. PWRON is used as RESET Button as default, need to configure PWRON long push as 10ms/Cold Reset, and disable short push detect!

2. WDOG_B is used as Cold Reset, external pull up is needed. For normal usage, WDOG_B/GPIO1_IO02 has internal pull up, don't need the external PU resistor. But in Boundary Scan mode, this pin is floating, external PU is necessary.

i.MX8M Mini DDR4 EVK Power Sequence

SEQ	PWR/Signal	REG	MIN	TYP	MAX	Curr(mA)
1	NVCC_SNVS_1V8	LDO1	1.62	1.8	1.98	10
2	VDD_SNVS_0V8	LDO2	0.76	0.8	0.9	10
3	RTC_RESET_B	RTC_RESET_B	--	--	--	--
4	CLK_32K_OUT	RTC_CLK	--	--	--	--
5	VDD_SOC_0V8	BUCK1	0.78/0.805	0.82/0.85	0.9	3000
6	VDD_DRAM&PU_0V9	BUCK5	0.805/0.855	0.85/0.95	0.9/1.0	3000
6	VDD_PHY_0V9	LDO4	0.855	0.9	1.0	250
7	VDD_ARM_0V9	BUCK2	0.805/0.9/0.95	0.85/0.95/1.0	0.95/1.0/1.05	3000
7	VDDA_1V8	LDO3	1.71	1.8	1.89	300
8	VDD_1V8/NVCC_1V8	BUCK7	1.65	1.8	1.95	1500
9	VPP_2V5	RT9193-25GB	2.375	2.5	2.75	300
10	NVCC_DRAM_1V2	BUCK8	1.14	1.2	1.26	3000
11	NVCC_3V3	BUCK6	3	3.3	3.6	3000
11	NVCC_SD2	MUXSW	3.0/1.65	3.3/1.8	3.6/1.95	150
12	VDD_PHY_1V2	LDO6	1.14	1.2	1.26	300
13	POR_B	POR_B	--	--	--	--

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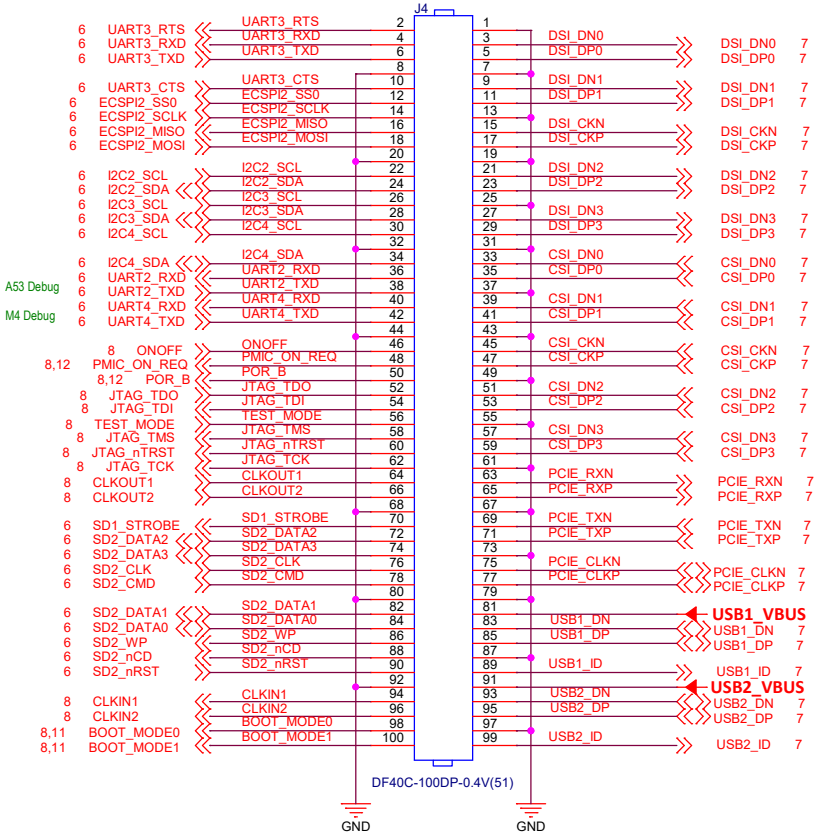
B2B Connector for CPU Board

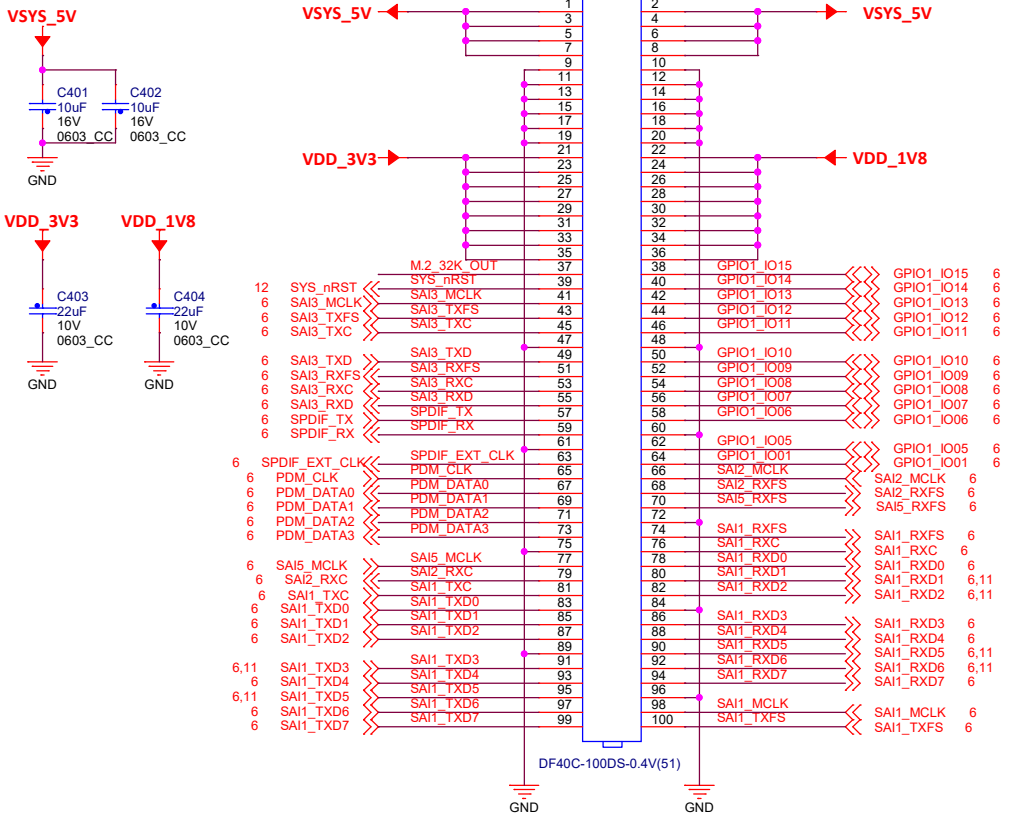
Caution:

IO internal pull up/down is not supported in 3.3V mode, must disable the internal pull up/down via software and use external pull up/down resistors instead.
All IO pin groups are impacted except for XTAL, DDR, PCI, USB and MIPI PHY IO's.
See Errata e50080 for detailed information.

Header



Receptacle



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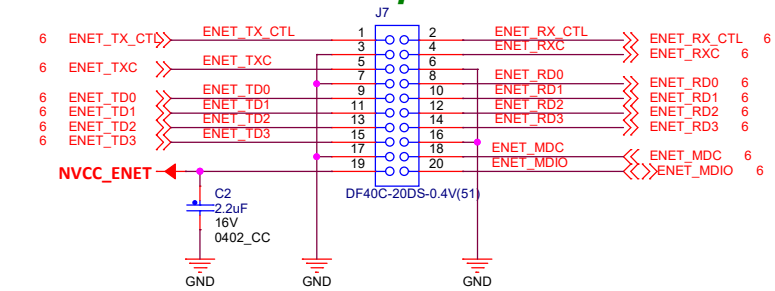

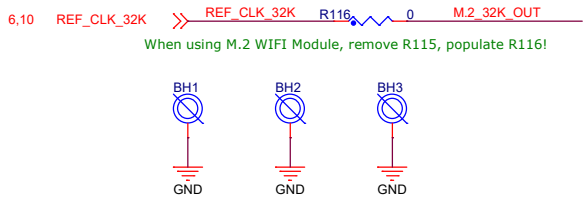

NXP	**Microcontroller Product Group** 6501 William Cannon Drive West Austin, TX 78735-8598

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Designer: Joshua Wu	Drawing Title: **8MMINID4-CPU**		
Drawn by: Joshua Wu	Page Title: **SOM Interface**		
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	Date: Friday, June 21, 2019	Sheet 13 of 14	