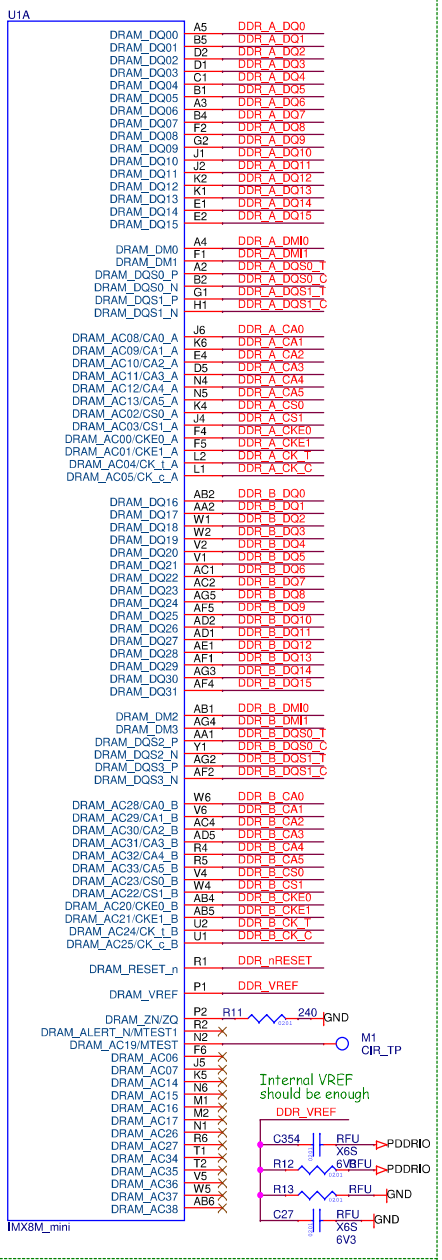
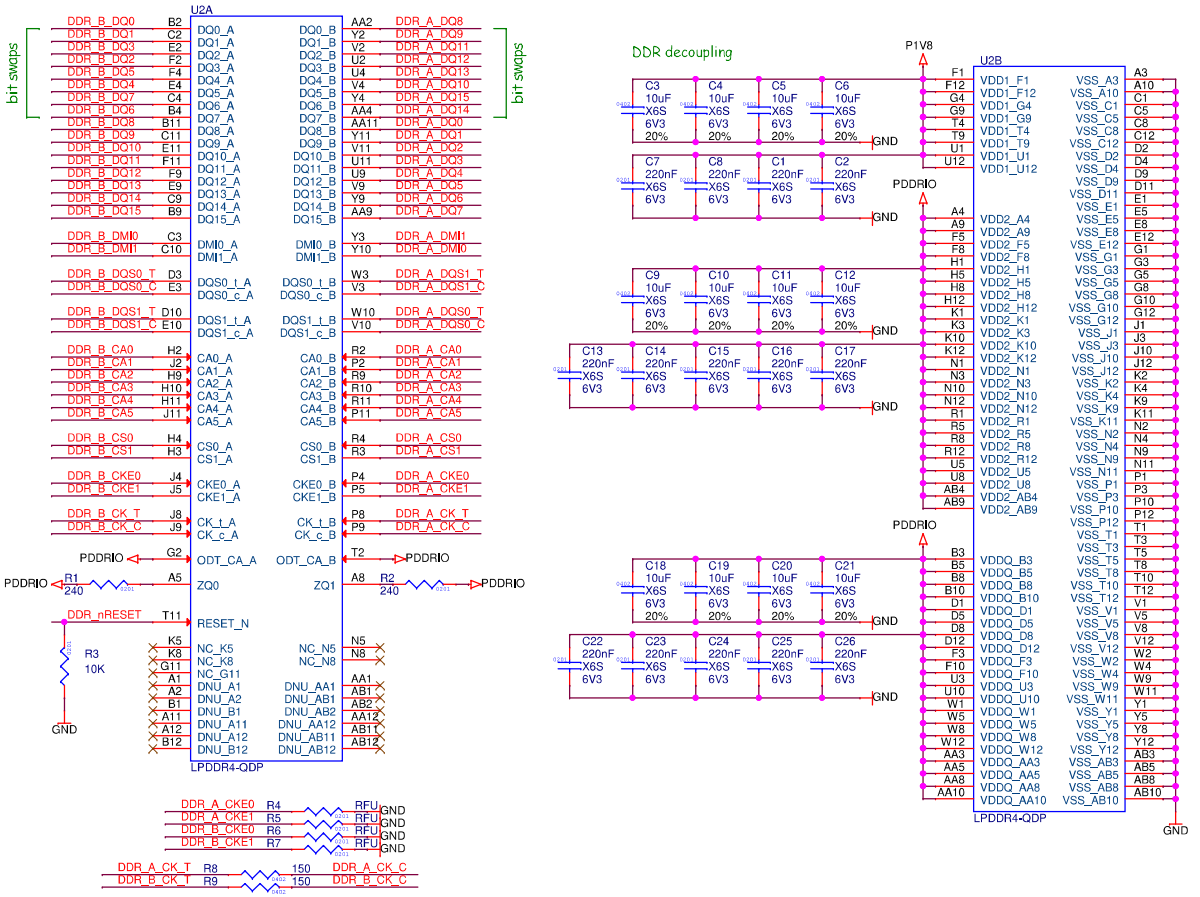
## Processor - DDR interface




## LPDDR4




Compatible dual-die or quad-die into the same package

The layout of this part is exactly identical to eval SOM board.

Bytes are physically swapped, so this configuration can't work with 1 die / 1 channel (16bits bus).

Swap :
- CPU_DQ[0..7] connected to DDR_DQB[8..15]
- CPU_DQ[8..15] connected to DDR_DQB[0..7] + bit swaps inside the byte
- CPU_DQ[16..23] connected to DDR_DQA[0..7] + bit swaps inside the byte
- CPU_DQ[24..31] connected to DDR_DQA[8..15]

## Sheet 04: DDR

| | | |
|---|---|---|
| **Qeedji** | ZAC Atalante champeaux<br>5A rue Pierre Joseph Colin<br>35000 RENNES - FRANCE | |
| Project : Tablet G2 | Ref : MD-1000034B | O.DAVID |
| CONFIDENTIAL | January 2020 | Sheet : 04 /13 |