

About Board routing restrictions of LPDDR4

**【Question】**

The documentation provides recommended routing requirements.  
(Table 21. i.MX 8M Mini LPDDR4-3000 routing recommendations)  
Only DQS  $\pm$  10ps is recommended for the data byte lane.

However, Table.23 can be found within 1ps in the data group.  
Does the data group need to match within 1ps like CLK / DQS?

- i.MX 8M Mini Hardware Developer's Guide :  
i.MX 8M Mini Hardware Developer's Guide, User's Guide  
IMX8MMHDG Rev. 1, 08/2019

**Table 21. i.MX 8M Mini LPDDR4-3000 routing recommendations**

LPDDR4-3000				
LPDDR4 signal (each 16-bit channel)	Group	PCB + package prop delay		Considerations
		Min	Max	
CK_t/CK_c	Clock	Short as possible	200 ps	Match the true/complement signals within 1 ps.
CA[5:0]	Address/ Command/ Control	CK_t - 25 ps	CK_t + 25 ps	
CS[1:0]				
CKE[1:0]				
DQS0_t/DQS0_c	Byte 0 - DQS	CK_t - 85 ps	CK_t + 85 ps	Match the true/complement signals of DQS within 1 ps.
DM0	Byte 0 - Data	DQS0_t - 10 ps	DQS0_t + 10 ps	
DQ[7:0]				
DQS1_t/DQS1_c	Byte 1 - DQS	CK_t - 85 ps	CK_t + 85 ps	
DM1	Byte 1 - Data	DQS1_t - 10 ps	DQS1_t + 10 ps	
DQ[15:8]				

**Table 23. LPDDR4 length matching example (byte lane 1 signals)**

Net name	PCB delay (ps)	Pkg delay (ps)	Comments
DRAM_SDQS1_T_A	84.2	48.6	Vias are L1-> L8->L1
	132.8		Total Net Delay
DRAM_SDQS1_C_A	84.8	47.2	Vias are L1-> L8->L1
	132.0		Total Net Delay
DRAM_DMI1_A	75.6	58.6	Routed on top layer, no via
	134.2		Total Net Delay
DRAM_DATA8_A	89.0	45.0	Routed on top layer, no via
	134.0		Total Net Delay
DRAM_DATA9_A	83.9	50.1	Routed on top layer, no via
	134.0		Total Net Delay
DRAM_DATA10_A	87.9	46.2	Routed on top layer, no via
	134.1		Total Net Delay
DRAM_DATA11_A	86.9	47.2	Routed on top layer, no via
	134.1		Total Net Delay
DRAM_DATA12_A	94.3	40.3	Routed on top layer, no via
	134.7		Total Net Delay
DRAM_DATA13_A	86	48.8	Routed on top layer, no via
	134.8		Total Net Delay
DRAM_DATA14_A	76.4	58.4	Routed on top layer, no via
	134.8		Total Net Delay
DRAM_DATA15_A	81.8	52.4	Routed on top layer, no via
	134.2		Total Net Delay

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