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1. Interrupted lines coded with the same letter or letter combinations are electrically connected.

2. Device type number is for reference only. The number varies with the manufacturer.

3. Special signal usage:
 _B Denotes - Active-Low Signal
 <> or [] Denotes - Vectored Signals


4. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

Preliminary - Subject to Change without Notice!

This board was designed for maximum flexibility in software development and demonstrates multiple functions possible with i.MX processors. Although best design practices have been applied, some areas may not be suitable for a mass-production design.

Revision History

Rev. Code	Date	By	Description
A	2018-03-16	Javen	1 initial version
B	2018-05-09	Javen	1 Add D308, D309, D310, U312, C337, R355, C338, D312, D313 to enable always 'ON' LDO 2 Add U311, R356, R357, R358, R359, R343, D311, C341 to get accurate VBUS2 threshold 3 Change U303, U306 part number to PTN5110NHQ to reduce the EN_SNK output debounce time 4 Remove backup resistor R347, R348 and add C342-C344 for VBUS detect circuit 5 Change U702 to NXP part:NX3P191, add TP701, TP704 6 Install R502 to make the ENET IO voltage default to 1.8V 7 Add R349, R350, R353, R354 for Type-C circuit debug 8 Change C113 to 0.22uF, Add C161 to increase the time delay of PTN5110 VBUS/VDD 9 Remove R712, D701, Q704, R716, R715 for PWM_LED. 10 Add R216, R217, R218, R219 for SD2_nCD alternative design 11 Add Q1001-Q1003, R1029-R1033, C1004 to control the audio board power sequence. 12 Update bootcfg pull up resistors R1101/R1103/R1105/R1107/R1109/R1111/R1113/R1115/R1117/ R1119/R1121/R1123/R1125/R1127/R1129/R1131/R1133/R1135 to 4.7K OHM 13 Add R1034 for power backup
C	2018-09-10	Javen	1 Update the Block Diagram and Power Tree; 2 Change C301,C321 from 10uF to 4.7uF; 3 DNP R315, R316; 4 Add R632,DNP R626, D603 for PCIe L1SS support 5 Add R1137-R1140, Change SW1101, SW1102 for BOOT_MODE2/3 6 Update J201 PIN56 from GND to TEST_MODE net 7 Change R101 from 1.5M OHM to 1.4M OHM to support VBUS < 5V case 8 DNP R614,R615, Install R610,R611,R616,R617
C1	2018-11-29	Javen	1 Update L401,L501,L503,L601,L602,L901 to BLM18PG121SN1 2 Change U702 to ADP191ACBZ-R7, U701 to IRM-V538M3/TR1 due to EOL
C2	2019-2-11	Javen	1 Update the Min/Typ/Max operating range for I.MX8M Mini power supplies; 2 Add note for all IOs that internal pull up/down is not supported in 3.3V mode;
C3	2019-6-18	Javen	1 Change R105 from 41.2K to 43K, increasing DCDC_5V to 5.2V to keep USB VBUS output higher than 4.75V in PD SPT.1 Load Test; 2 Add R301(47K) and DNP C303 for better discharge of USB1_OTG_VBUS, otherwise PD SPT.1 Load Test might fail.

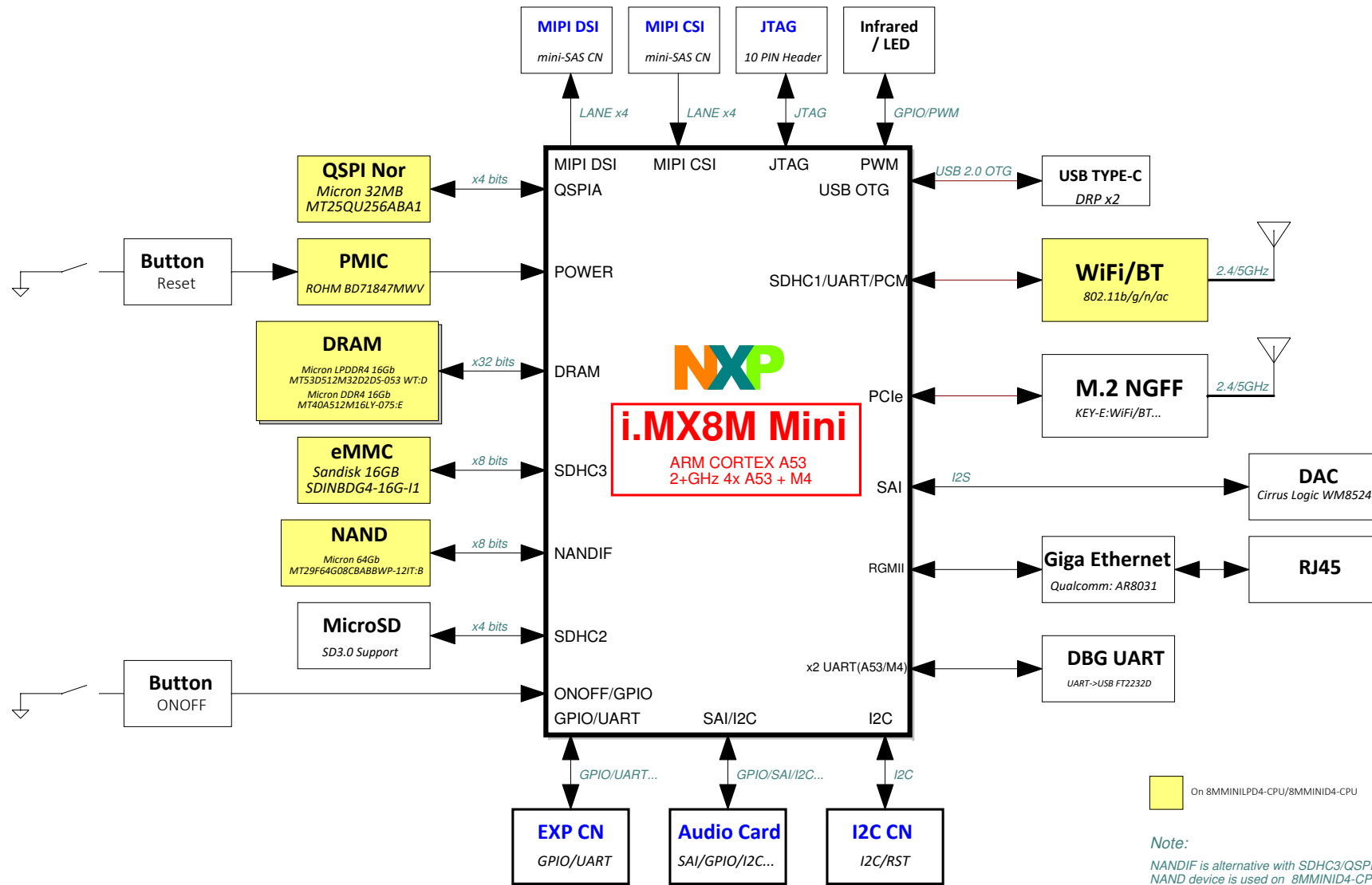
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Drawn by: <-W/->	Page Title: Title and Rev History		
Approved: <-Approver>	Size C	Document Number SCH-31407 PDF: SPF-31407	Rev CS
Date: Tuesday, June 18, 2019	Sheet 1 of 16		

8MMINI-EVK

Block Diagram

8MMINILPD4-EVK	31409
└ 8MMINILPD4-CPU	31399
└ 8MMINI-BB	31407

8MMINID4-EVK	35105
└ 8MMINID4-CPU	35104
└ 8MMINI-BB	31407

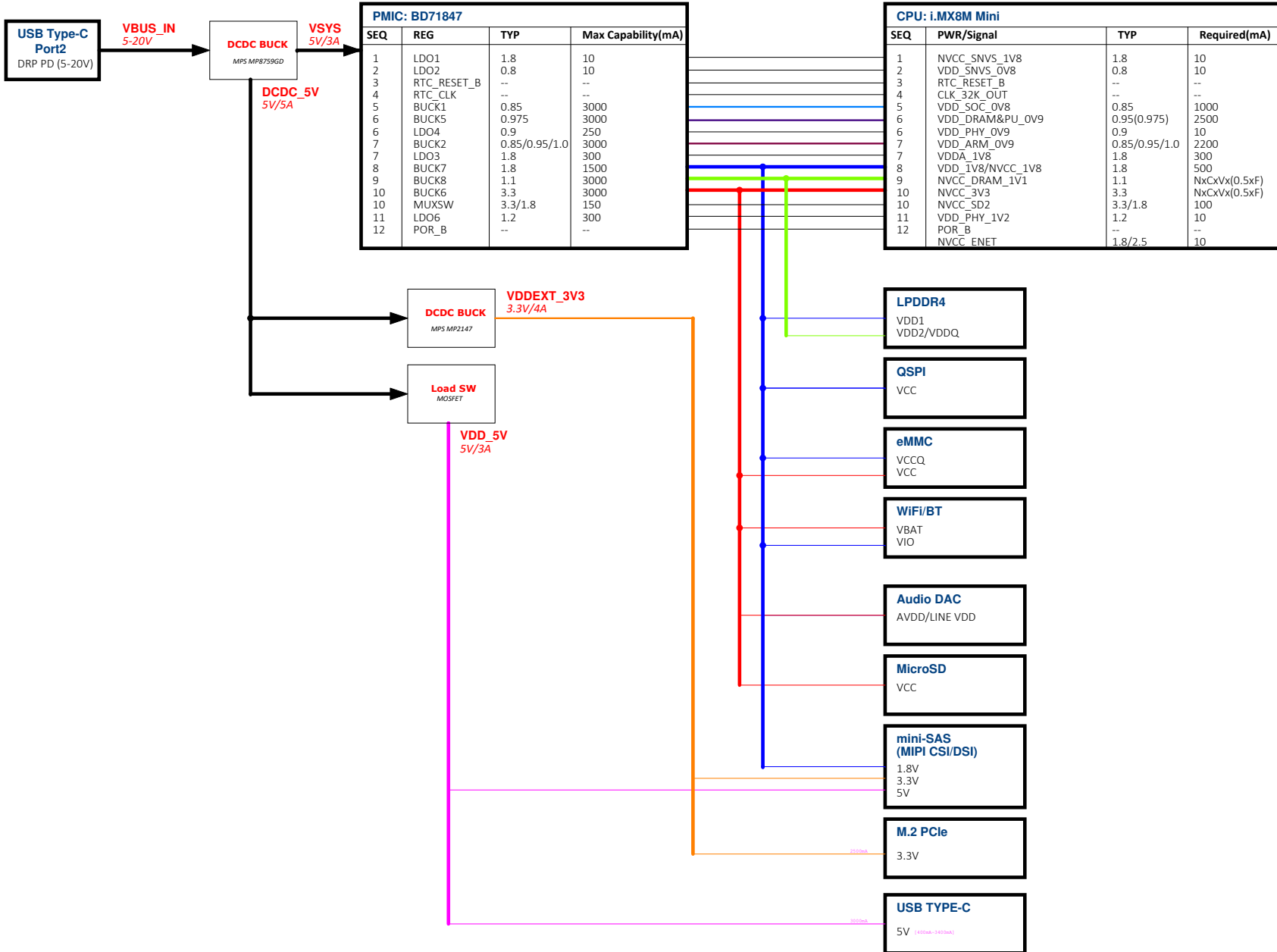


On 8MMINILPD4-CPU/8MMINID4-CPU

Note:
 NANDIF is alternative with SDHC3/QSPIA interface,
 NAND device is used on 8MMINID4-CPU.

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Drawn by: ~ W ~ Page Title: Block Diagram		Approved: ~ A ~ Size C Document Number SCH-31407 PDF: SPF-31407 Rev CS	
Date: Tuesday, June 18, 2019		Sheet 2 of 16	

8MMINILPD4-EVK PWR TREE



PMIC: BD71847

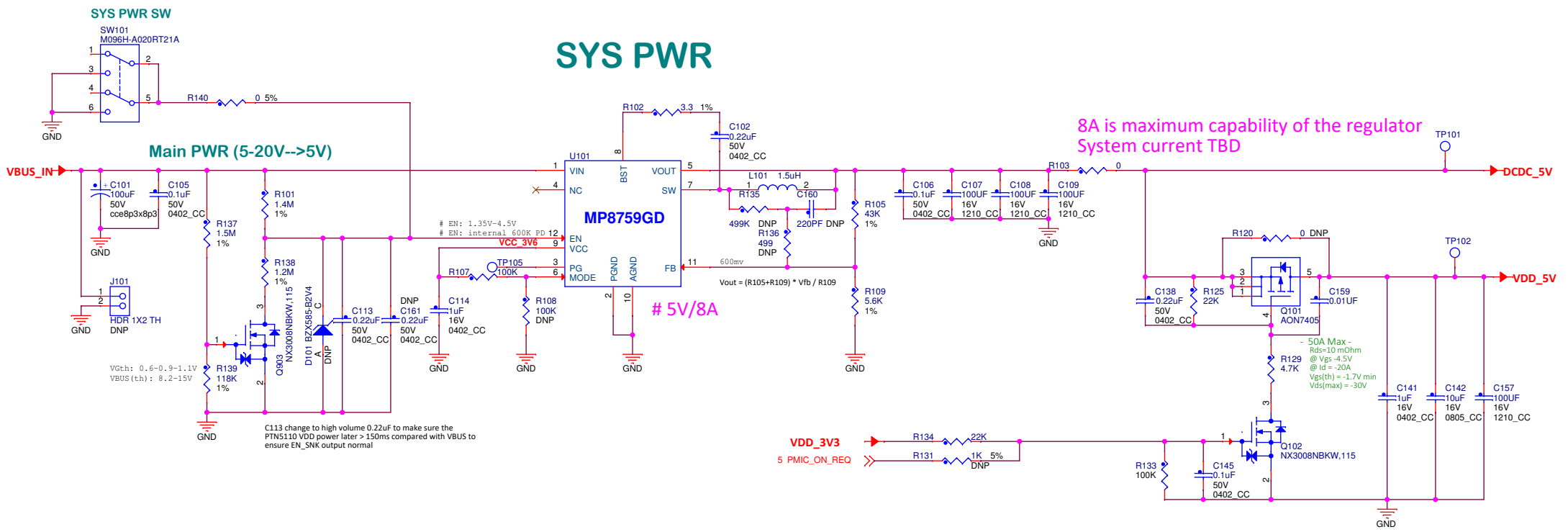
SEQ	REG	TYP	Max Capability(mA)
1	LDO1	1.8	10
2	LDO2	0.8	10
3	RTC_RESET_B	--	--
4	RTC_CLK	--	--
5	BUCK1	0.85	3000
6	BUCK5	0.975	3000
6	LDO4	0.9	250
7	BUCK2	0.85/0.95/1.0	3000
7	LDO3	1.8	300
8	BUCK7	1.8	1500
9	BUCK8	1.1	3000
10	BUCK6	3.3	3000
10	MUXSW	3.3/1.8	150
11	LDO6	1.2	300
12	POR_B	--	--

CPU: i.MX8M Mini

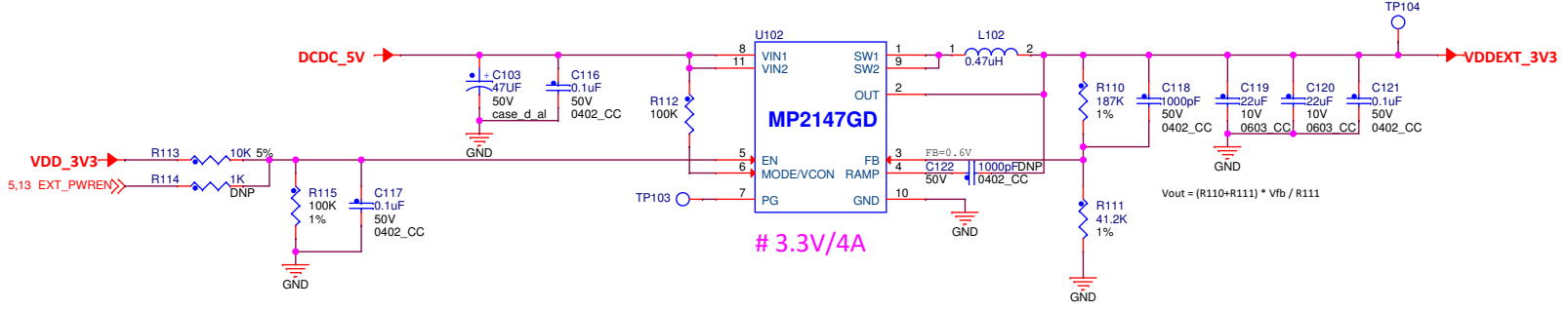
SEQ	PWR/Signal	TYP	Required(mA)
1	NVCC_SNV5_1V8	1.8	10
2	VDD_SNV5_0V8	0.8	10
3	RTC_RESET_B	--	--
4	CLK_32K_OUT	--	--
5	VDD_SOC_0V8	0.85	1000
6	VDD_DRAM&PU_0V9	0.95(0.975)	2500
6	VDD_PHY_0V9	0.9	10
7	VDD_ARM_0V9	0.85/0.95/1.0	2200
7	VDDA_1V8	1.8	300
8	VDD_1V8/NVCC_1V8	1.8	500
9	NVCC_DRAM_1V1	1.1	NxCxVx(0.5xF)
10	NVCC_3V3	3.3	NxCxVx(0.5xF)
10	NVCC_SD2	3.3/1.8	100
11	VDD_PHY_1V2	1.2	10
12	POR_B	--	--
12	NVCC_ENET	1.8/2.5	10

- LPDDR4**
VDD1
VDD2/VDDQ
- QSPI**
VCC
- eMMC**
VCCQ
VCC
- WiFi/BT**
VBAT
VIO
- Audio DAC**
AVDD/LINE VDD
- MicroSD**
VCC
- mini-SAS (MIPI CSI/DSI)**
1.8V
3.3V
5V
- M.2 PCIe**
3.3V
- USB TYPE-C**
5V (100mA-1400mA)

SYS PWR



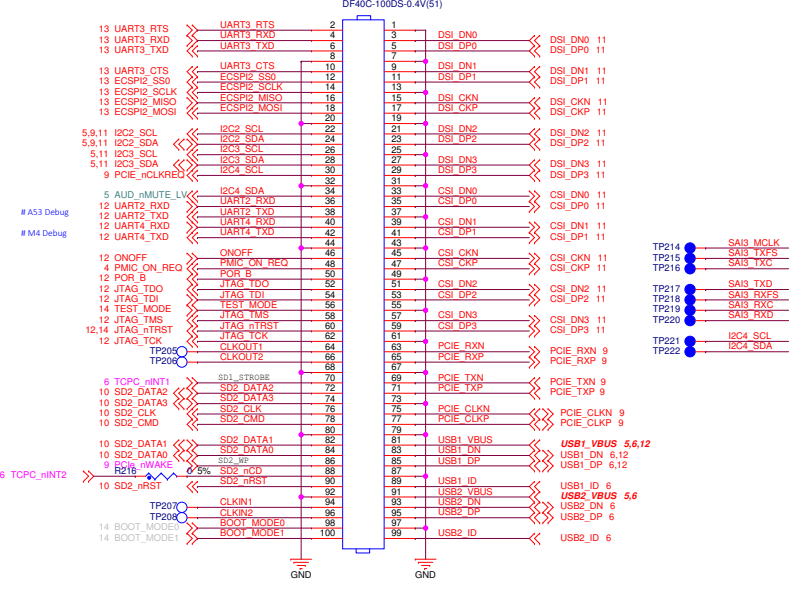
Ext 3.3V for Peripherals



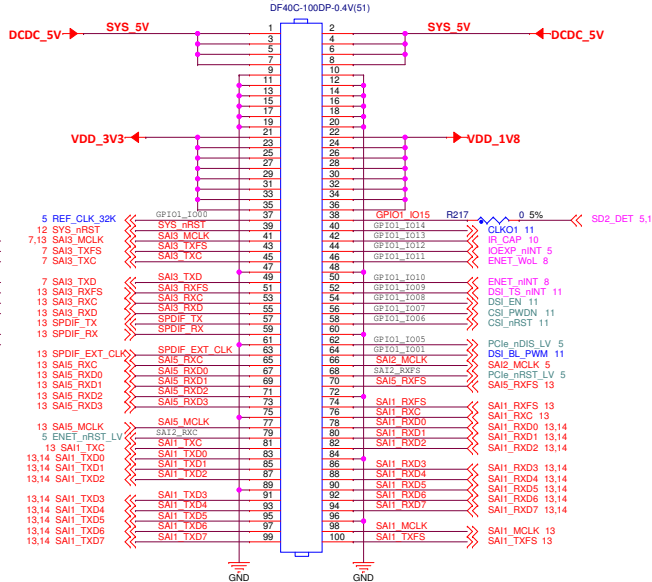
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Drawn by: <JW>	Page Title: PWR		
Approved: <Approver>	Size A3	Document Number SCH-31407 PDF: SPF-31407	Rev C3
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IO connector

B2B Receptacle

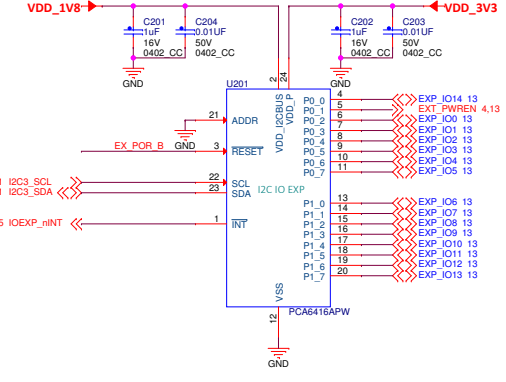


B2B Header

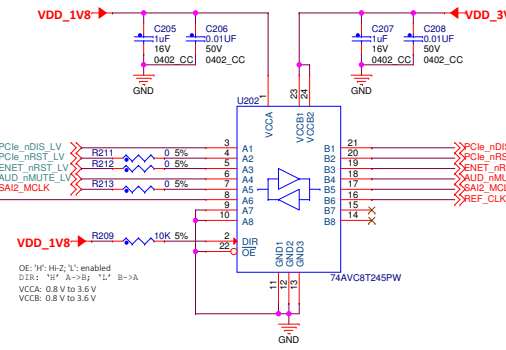
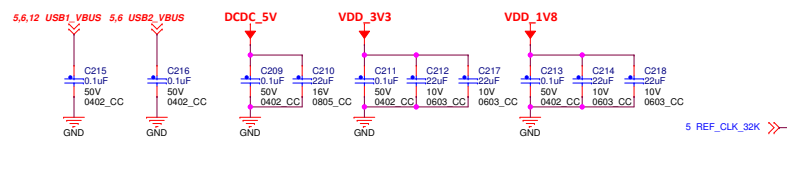
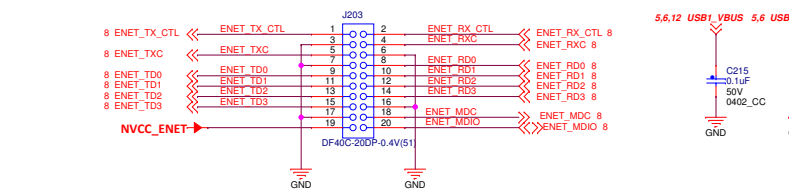


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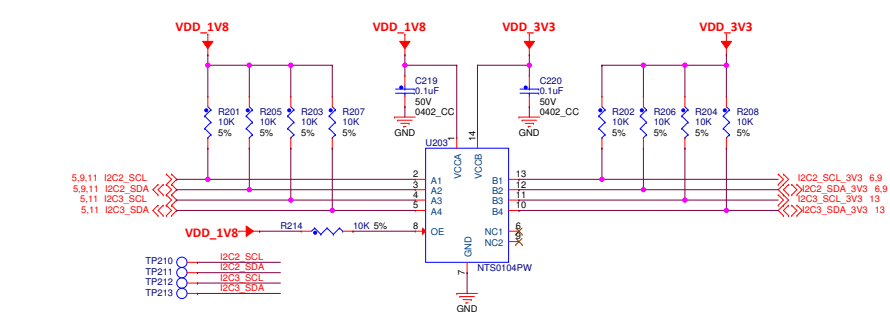
IO internal pull up/down is not supported in 3.3V mode, must disable the internal pull up/down via software and use external pull up/down resistors instead.
All IO pin groups are impacted except for XTAL, DDR, PCI, USB and MIPI PHY IO's.
See Errata e50080 for detailed information.



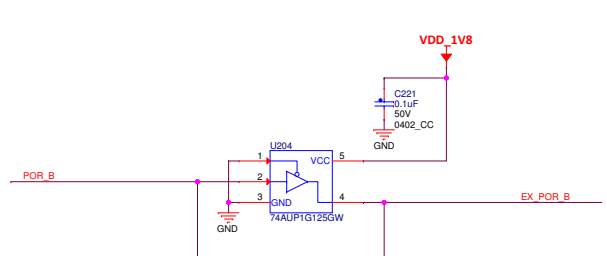
B2B Header



I2C2/3 Level shifter



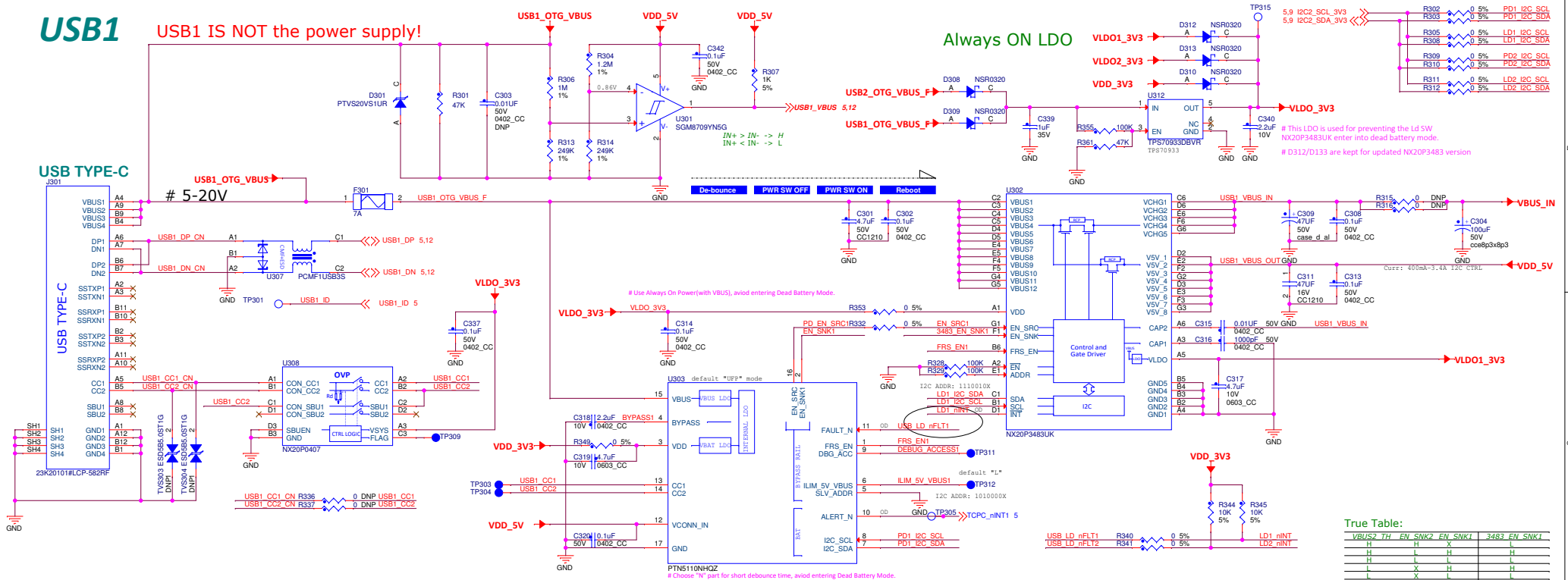
POR_B Buffer



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Drawn by: ~/W/	Page Title: CPU IO Interface	Size C	Document Number SCH-31407 PDF: SPF-31407
Approved: ~/Approver/	Date: Tuesday, June 18, 2019	Sheet 5 of 16	Rev CS

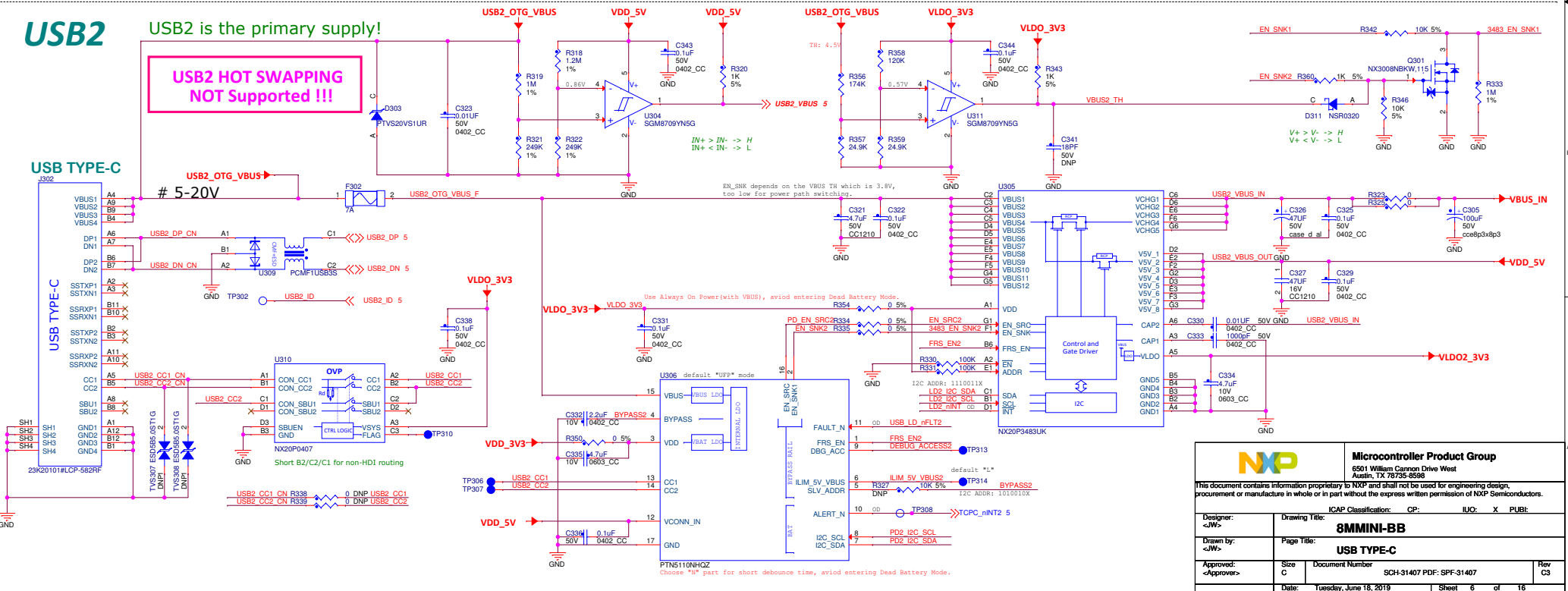
USB1

USB1 IS NOT the power supply!



USB2

USB2 is the primary supply!



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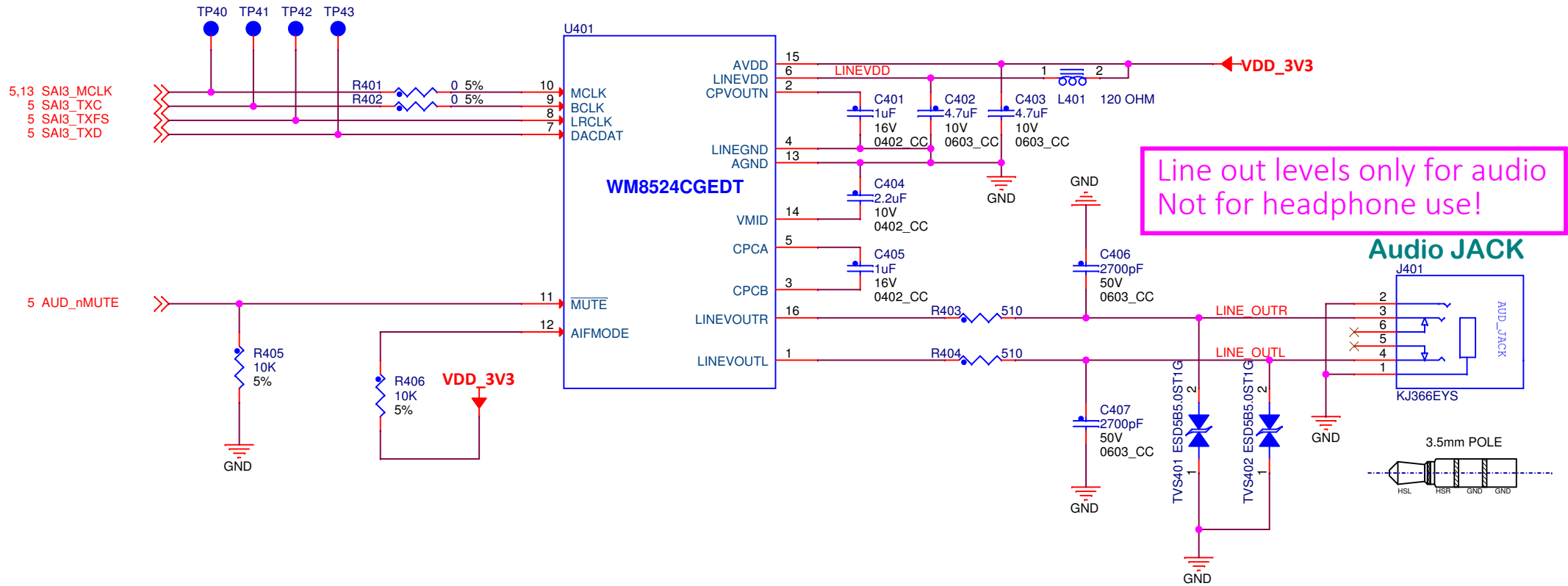
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Approved: ~Approver	Document Number SCH-31407 PDF: SFP-31407
Date: Tuesday, June 18, 2019	Sheet 6 of 16

Caution:

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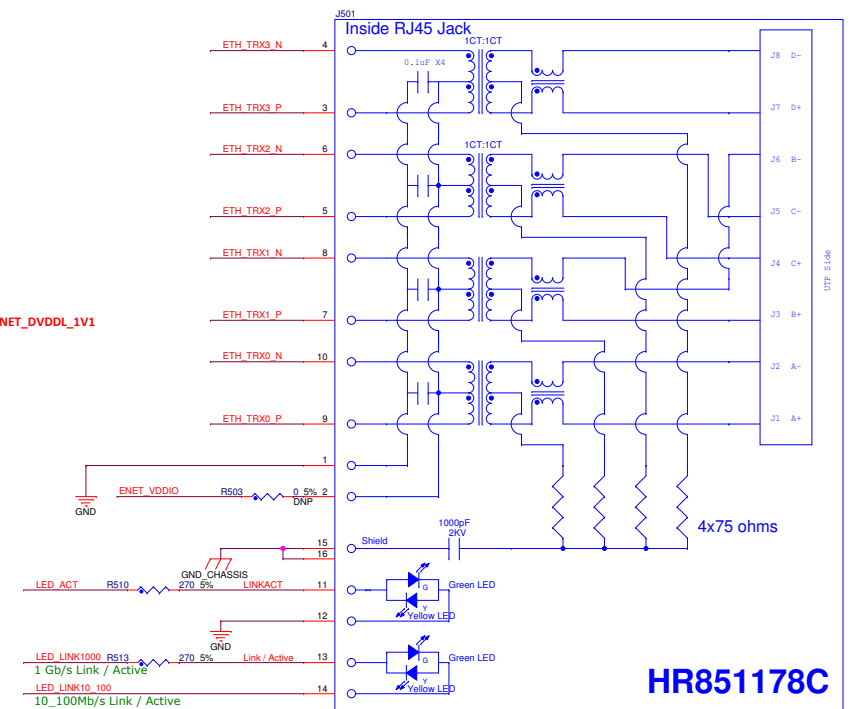
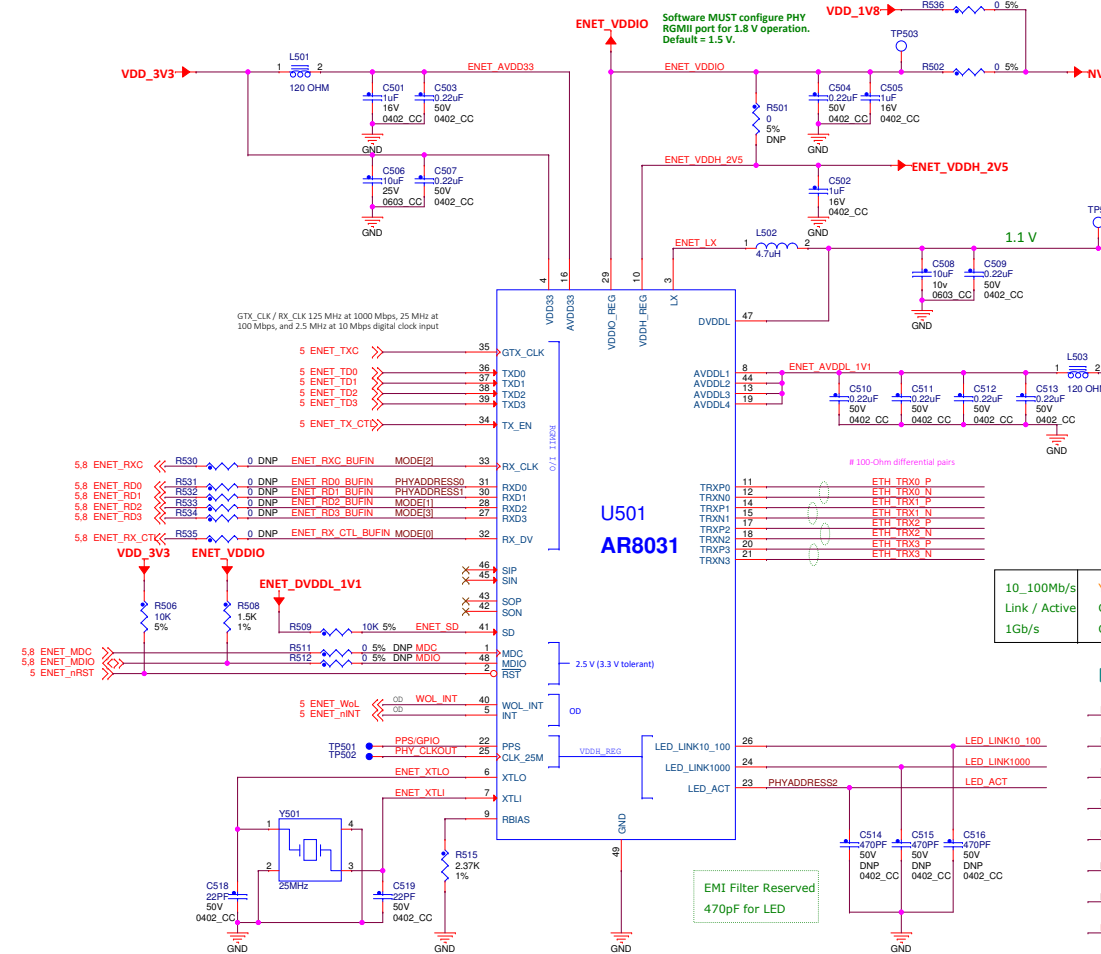
Audio DAC

24-bit 192kHz Stereo DAC 2Vrms Line Out



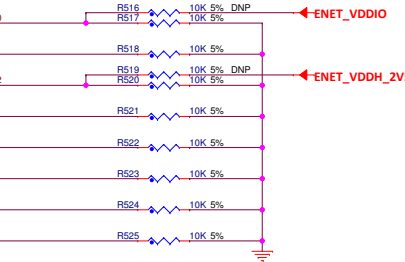
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Approved: <Approver>	Size A4	Document Number SCH-31407 PDF: SPF-31407	Rev C3
Date:	Tuesday, June 18, 2019	Sheet	7 of 16

RGMII 10/100/1000Mbps Ethernet

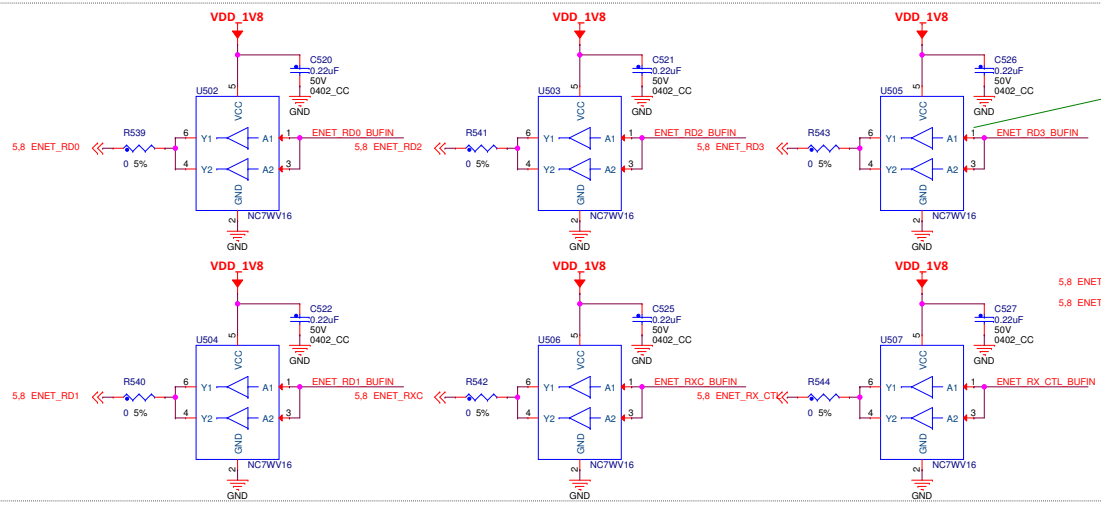
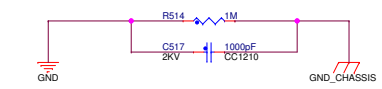


10_100Mb/s Link / Active	YELLOW
1Gb/s Link / Active	GREEN
1Gb/s	GREEN

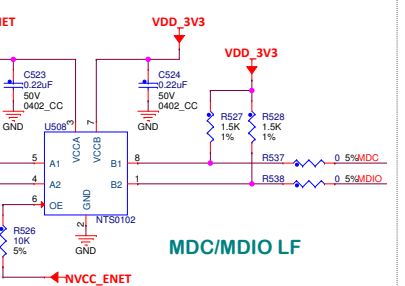
Power-on Strapping Pins CFG



Low Profile Tab-UP RJ45 with Magnetics / LED



Drivers are included in the receive path due to long signal paths and board-to-board connector. Adapters should place the PHY and processor on the same board, and eliminate the drivers. Refer to Atheros documentation for additional guidance.



Power-on Strapping Pins

PHY PIN	PHY CFG	Default	Definition
RXD0	PHYADDRESS0	0	LED_ACT and RXD1-0 set the lower three bits of the physical address. The upper two bits of the physical address are set to the default, '00'.
RXD1	PHYADDRESS1	0	
LED_ACT	PHYADDRESS2	1	
RX_DV	MODE[0]	0	0000 1000 Base-T, SGMAII 0001 1000 Base-T, SGMAII 0010 1000 Base-X, RGMII, SGMII, SGMII, SGMII 0011 1000 Base-X, RGMII, SGMII, SGMII, SGMII 0010 1000 Base-X, RGMII, SGMII, SGMII, SGMII 0110 1000 Base-X, RGMII, SGMII, SGMII, SGMII 0111 1000 Base-X, RGMII, SGMII, SGMII, SGMII 1011 1000 Base-X, RGMII, SGMII, SGMII, SGMII 1110 1000 Base-X, RGMII, SGMII, SGMII, SGMII 1111 1000 Base-X, RGMII, SGMII, SGMII, SGMII Others Reserved
RXD2	MODE[1]	0	
RXD3	MODE[3]	0	
LED_LINK1000	INT_SELECT	1	0: INT ; 1: GPIO

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ICAP Classification: CP- IUC: X PUB: B

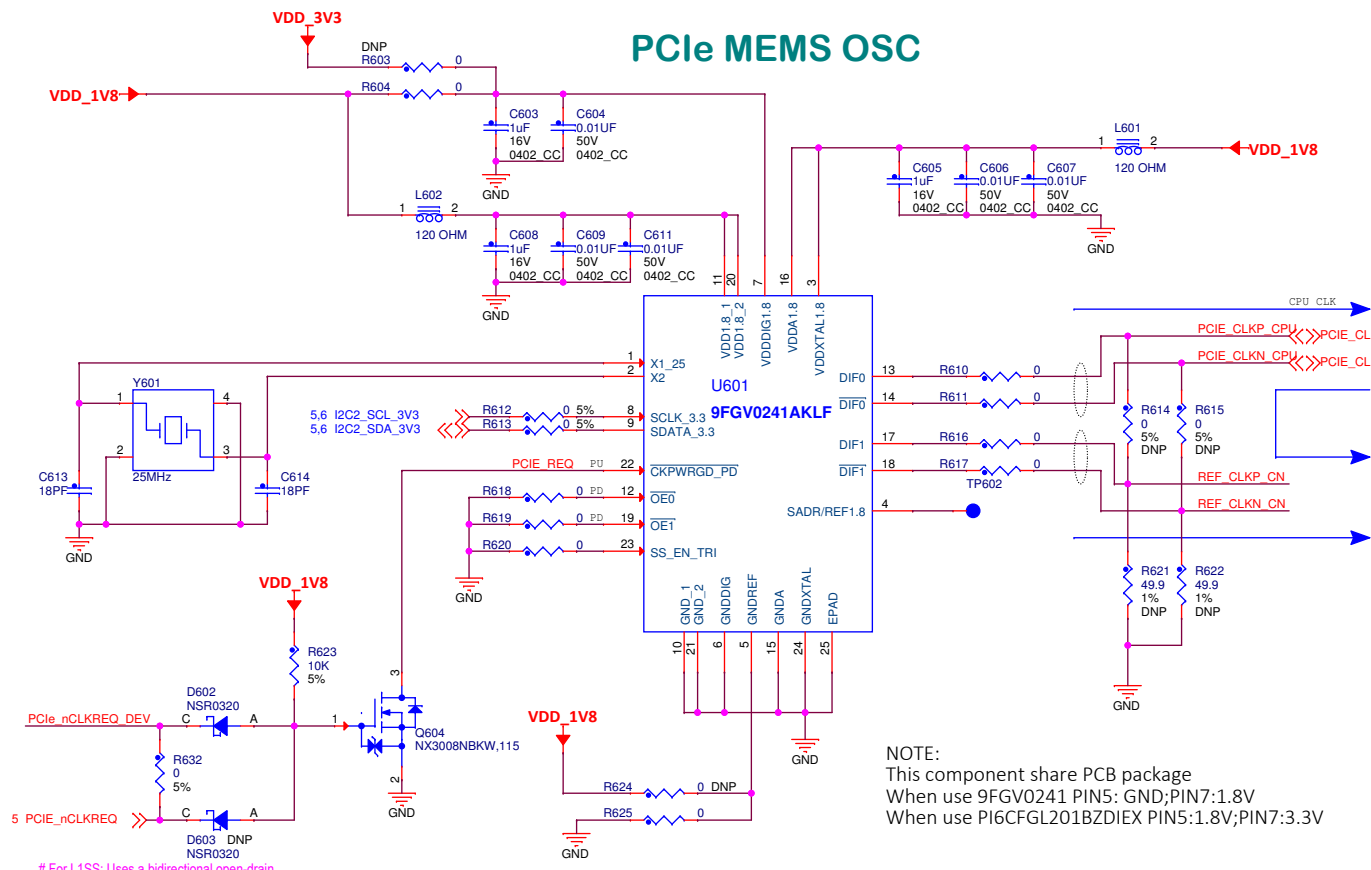
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Drawn by: ~W/-
Page Title: **Ethernet**

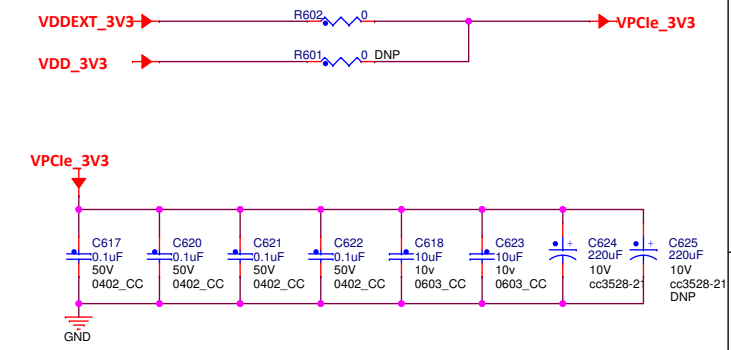
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Size C Document Number: SCH-31407 PDF: SPF-31407

Date: Tuesday, June 18, 2019 Sheet 8 of 16

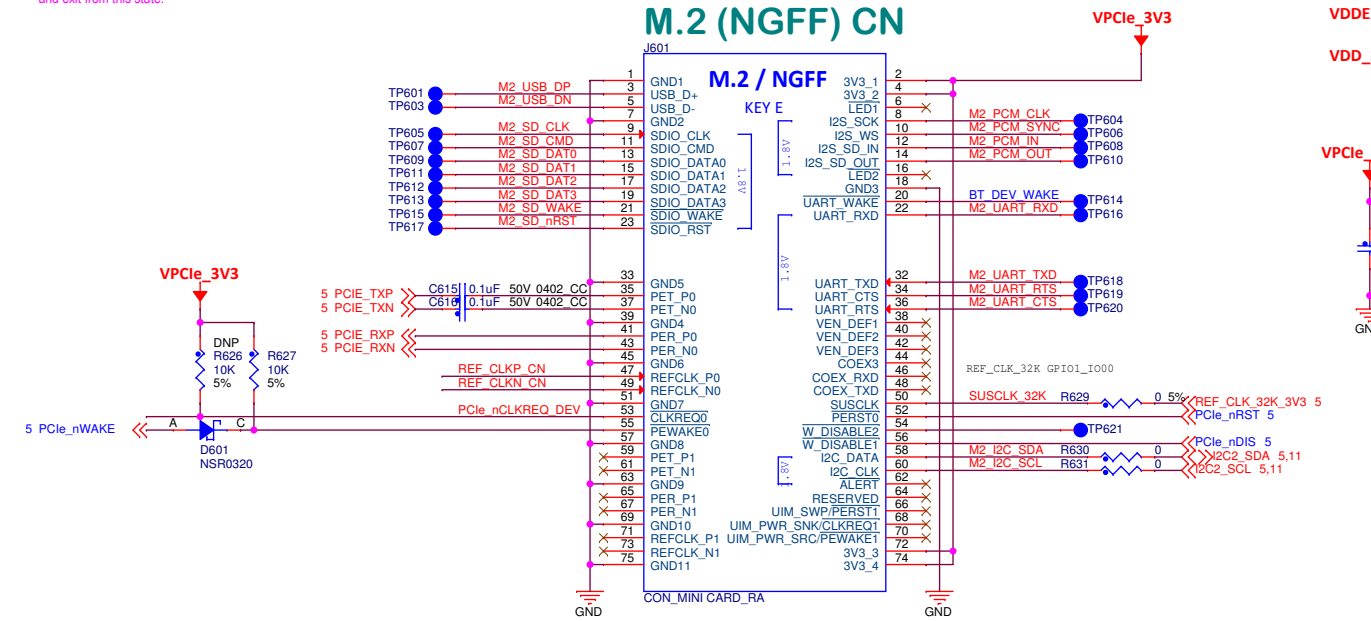
PCIe M.2/NGFF



PCIe PWR



M.2 (NGFF) CN



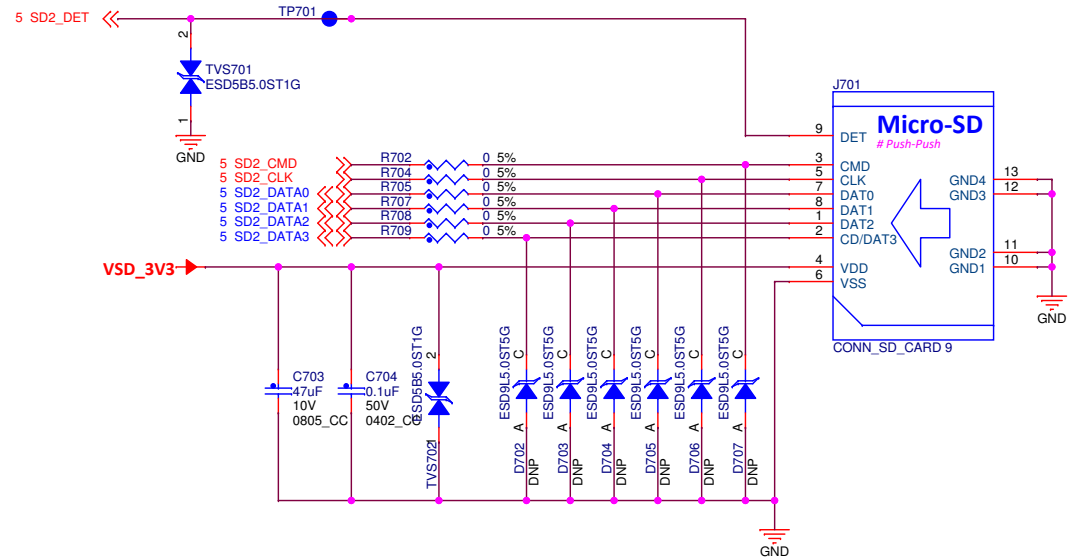
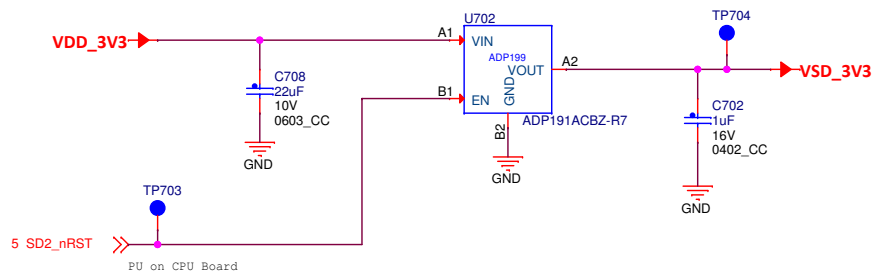
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Drawing Title: 8MMINI-BB		Page Title: M.2 PCIe	
Drawn by: <JW>		Document Number SCH-31407 PDF: SPF-31407	
Approved: <Approver>		Size A3	
Date: Tuesday, June 18, 2019		Sheet 9 of 16	

MicroSD/Infrared/LED

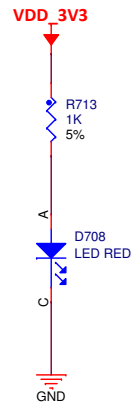
Caution:

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See Errata e50080 for detailed information.

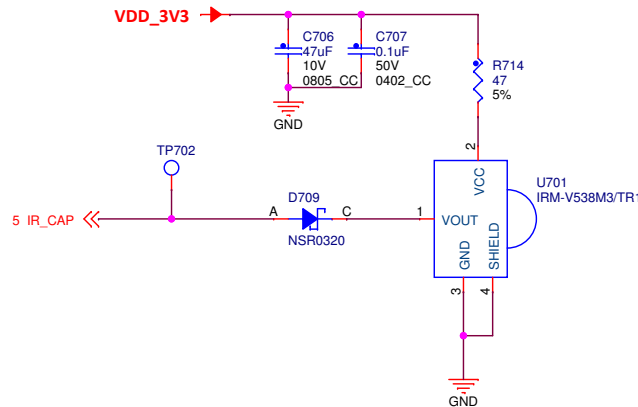
SD3.0 PWR



STATUS/PWR LED

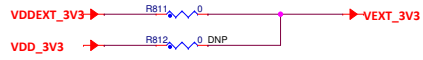


Infrared Remote Control

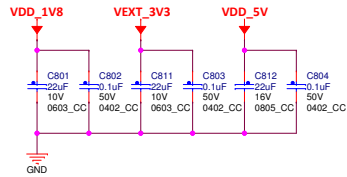
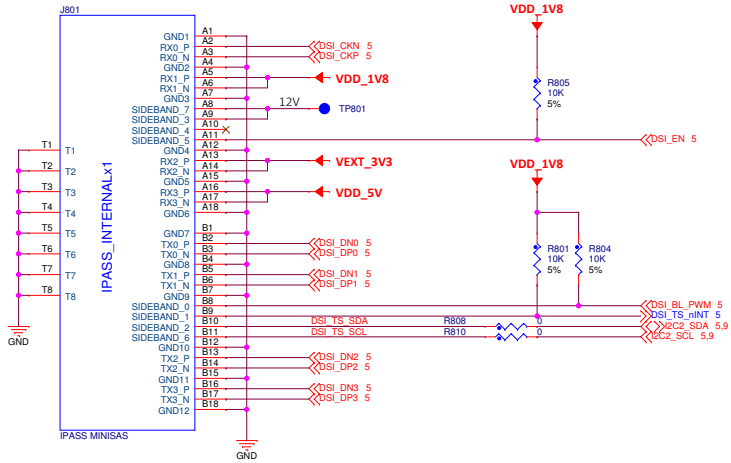


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Date: Tuesday, June 18, 2019		Sheet 10	of 16
		Rev C3	

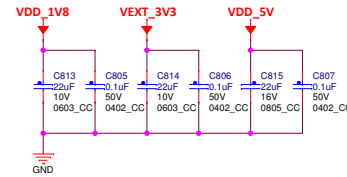
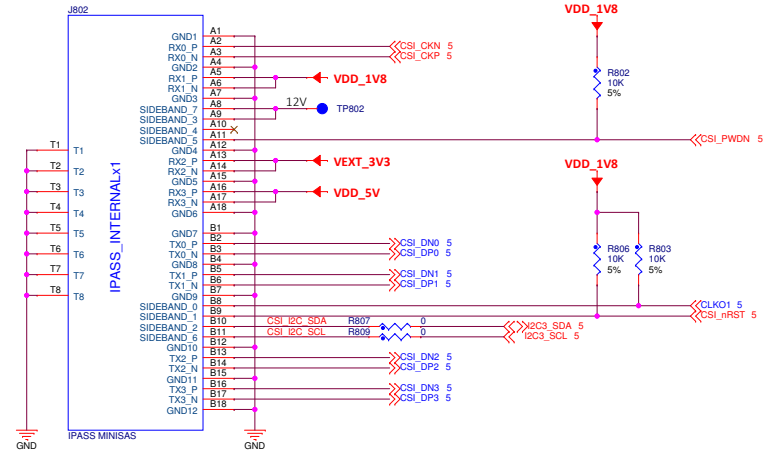
Camera/DSI LCD



DSI LCD

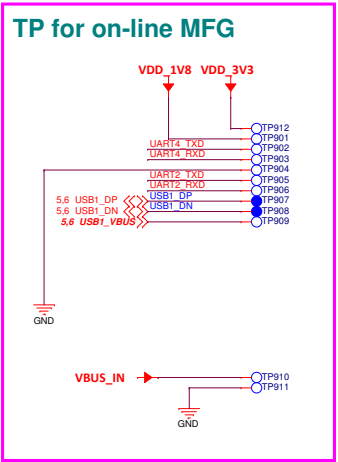
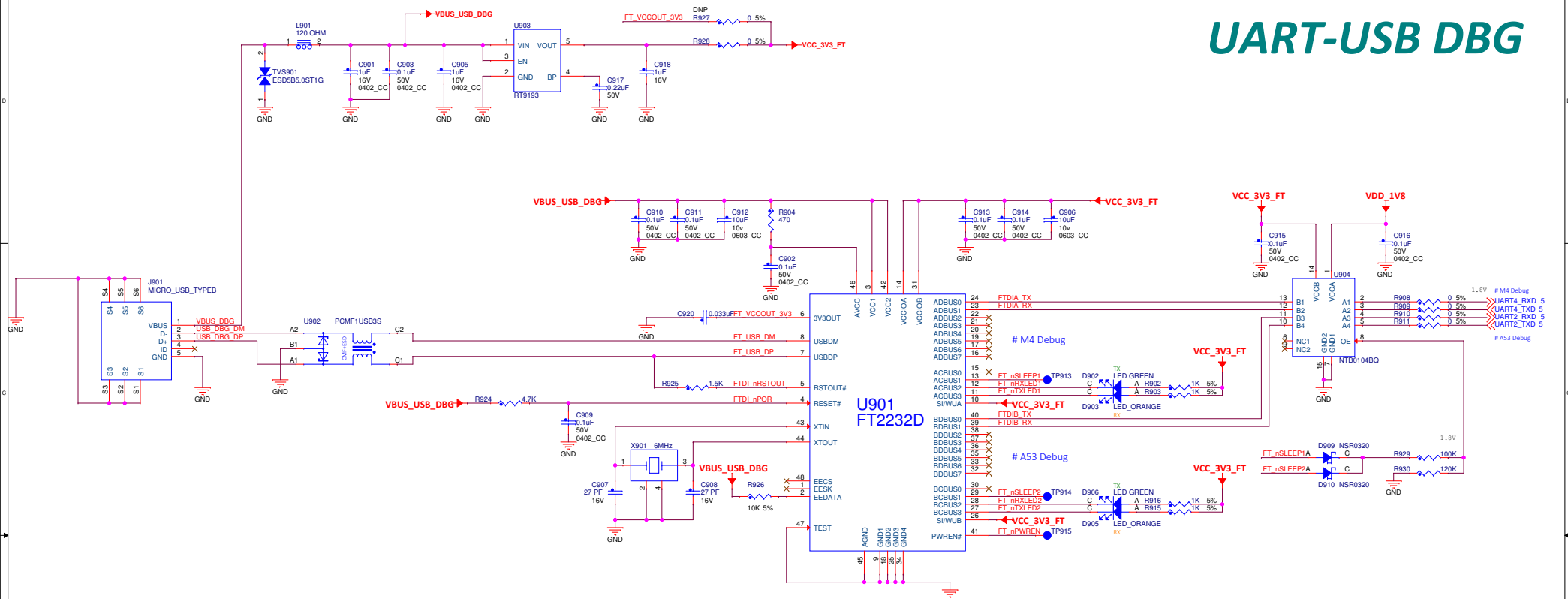


Camera

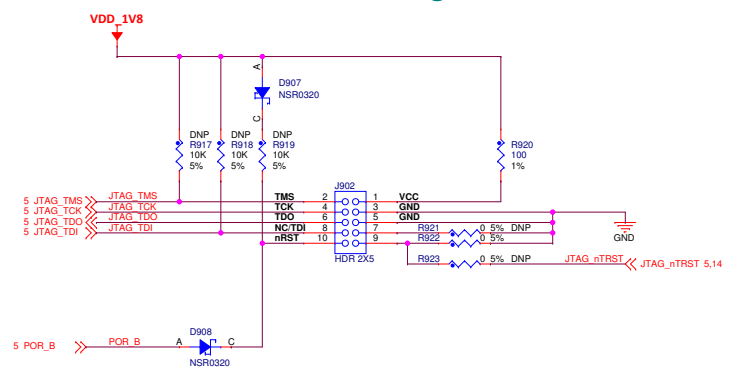


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Approved: ~Approver~	Size C	Document Number SCH-31407 PDF: SPF-31407	Rev CS
Date: Tuesday, June 18, 2019		Sheet 11 of 16	

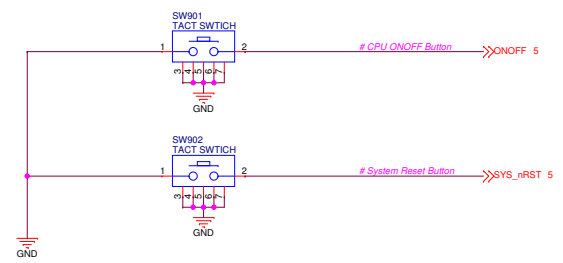
UART-USB DBG



JTAG Debug



Buttons

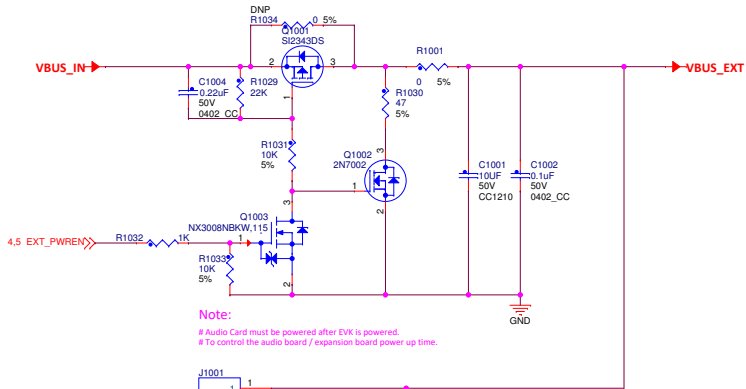


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Drawn by: ~W~		Page Title: Debug UART	
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Date: Tuesday, June 18, 2019		Sheet 12 of 16	Rev CS

Ext CN

Caution:

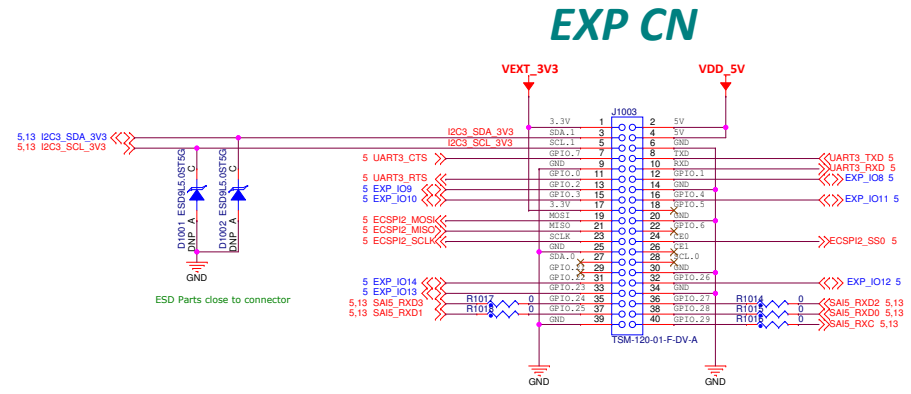
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See Errata e50080 for detailed information.



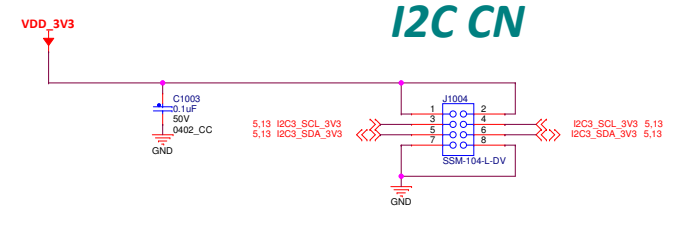
Note:
Audio Card must be powered after EVK is powered.
To control the audio board / expansion board power up time.



Audio Card CN



EXP CN



I2C CN

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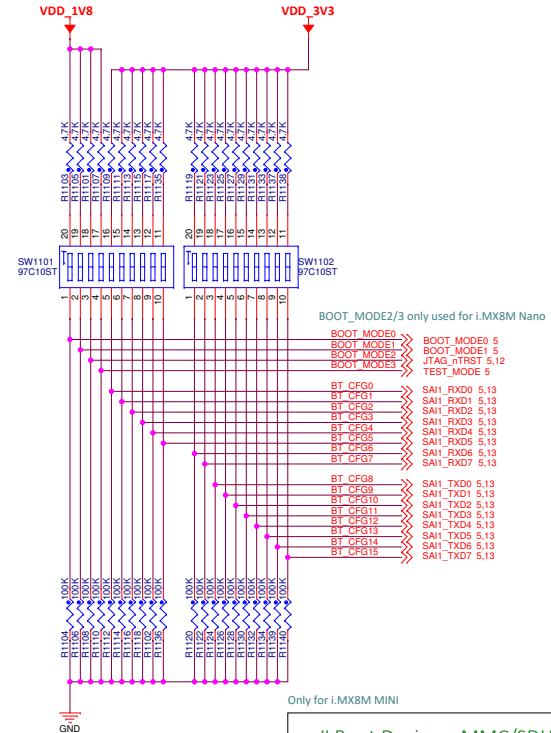
Boot Mode and CFG Switch

Caution:

IO internal pull up/down is not supported in 3.3V mode, must disable the internal pull up/down via software and use external pull up/down resistors instead.
All IO pin groups are impacted except for XTAL, DDR, PCI, USB and MIPI PHY IO's.
See Errata e50080 for detailed information.

i.MX8M MINI ROM Fuse

Address	7	6	5	4	3	2	1	0
0x470[15:8]	BOOT_CFG[15]	BOOT_CFG[14]	BOOT_CFG[13]	BOOT_CFG[12]	BOOT_CFG[11]	BOOT_CFG[10]	BOOT_CFG[9]	BOOT_CFG[8]
0x470[15:8]	Infinite-Loop (Debug USE only) 0 - Disable 1 - Enable	001 - SD/eSD		Port Select: 00 - uSDHC1 01 - uSDHC2 10 - uSDHC3		Power Cycle Enable '0' - No power cycle '1' - Enabled via		SD Loopback Clock Source Sel (for SDR50 and SDR104 only) '0' - through SD pad '1' - direct
0x470[15:8]		010 - MMC/eMMC		011 - NAND		Pages in Block: 00 - 128 01 - 64 10 - 32 11 - 256		Nand_Row_address_bytes: 00 - 3 01 - 2 10 - 4 11 - 5
0x470[15:8]		100 - QSPI		Flash Auto Probe	FLASH_TYPE 000 - Device supports 3B read by default 001 - Device supports 4B read by default 010 - HyperFlash 1V8 011 - HyperFlash 3V3 100 - MXIC Octal DDR			
0x470[15:8]		110 - SPI NOR		Port Select: 000 - eCSP1 001 - eCSP2 010 - eCSP3		SPI Addressing: 0 - 3-bytes (24-bit) 1 - 2-bytes (16-bit)		
0x470[15:8]		Others - Reserved for future use						
	BOOT_CFG[7]	BOOT_CFG[6]	BOOT_CFG[5]	BOOT_CFG[4]	BOOT_CFG[3]	BOOT_CFG[2]	BOOT_CFG[1]	BOOT_CFG[0]
SD/eSD	0x470[7:0]	Reserved	Reserved	Bus Width: 0 - 1-bit 1 - 4-bit	Speed 000 - Normal/SDR12 001 - High/SDR25 010 - SDR50 011 - SDR104 101 - Reserved for DDR50 Others - Reserved		Reserved	
MMC/eMMC	0x470[7:0]	Bus Width: 000 - 1-bit 001 - 4-bit 010 - 8-bit 101 - 4-bit DDR (MMC 4.4) 110 - 8-bit DDR (MMC 4.4) Else - reserved.		Speed 00 - Normal 01 - High 10 - Reserved for HS200 11 - Reserved		USDHC IO VOLTAGE SELECTION For Normal Boot Mode 0 - 3.3V 1 - 1.8V	USDHC IO VOLTAGE SELECTION For Manufacture Mode 0 - 3.3V 1 - 1.8V	
NAND	0x470[7:0]	BT_TOGGLEMODE	BOOT_SEARCH_COUNT: 00 - 2 01 - 2 10 - 4 11 - 8		Toggle Mode 33MHz Preamble Delay, Read Latency: '000' - 16 GPMICLK cycles. '001' - 1 GPMICLK cycles. '010' - 2 GPMICLK cycles. '011' - 3 GPMICLK cycles. '100' - 4 GPMICLK cycles. '101' - 5 GPMICLK cycles. '110' - 6 GPMICLK cycles. '111' - 7 GPMICLK cycles. '1111' - 15 GPMICLK cycles.			Reserved
FlexSPI	0x470[7:0]	HOLD TIME: 00 - 500us 01 - 1ms 10 - 3ms 11 - 10ms		FLASH Auto Probe Type		FlexSPI FLASH Dummy Cycle		
SPINOR	0x470[7:0]	CS select SPI only: 00 - CS#0 default 01 - CS#1 10 - CS#2 11 - CS#3		Reserved	Reserved	Reserved	Reserved	Reserved

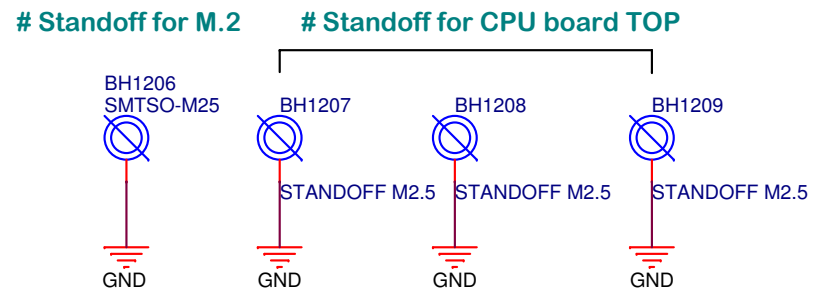
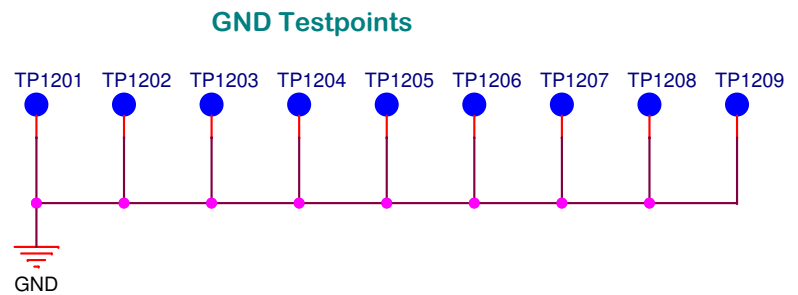
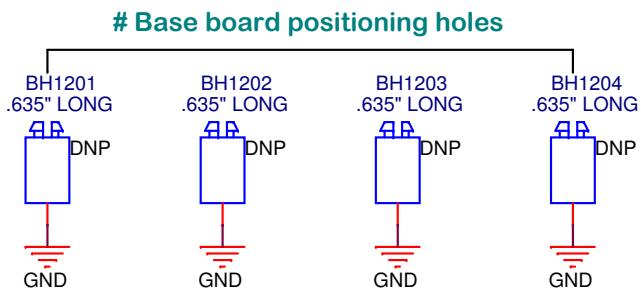



BMODE

BOOT_MODE1	BOOT_MODE0
BOOT TYPE:	
00 Boot From Fuses	
01 Serial Downloader	
10 Internal Boot (Development)	
11 Reserved	

Boot Device: eMMC/SDHC3
SW1101 [1-10]: 0110110001
SW1102 [1-10]: 0001010100
Boot Device: MicroSD/SDHC2
SW1101 [1-10]: 0110110010
SW1102 [1-10]: 0001101000
Boot Device: NAND
SW1101 [1-10]: 0110000000
SW1102 [1-10]: 1000111100
Download Mode
SW1101 [1-10]: 1010xxxxxx
SW1102 [1-10]: xxxxxxxx0

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