

8MMINILPD4-CPU

(i.MX8M Mini Reference Board)

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1. Interrupted lines coded with the same letter or letter combinations are electrically connected.
2. Device type number is for reference only. The number varies with the manufacturer.
3. Special signal usage:
 _B Denotes - Active-Low Signal
 <> or [] Denotes - Vectored Signals
4. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.


Preliminary - Subject to Change without Notice!

This board was designed for maximum flexibility in software development and demonstrates multiple functions possible with i.MX processors. Although best design practices have been applied, some areas may not be suitable for a mass-production design.

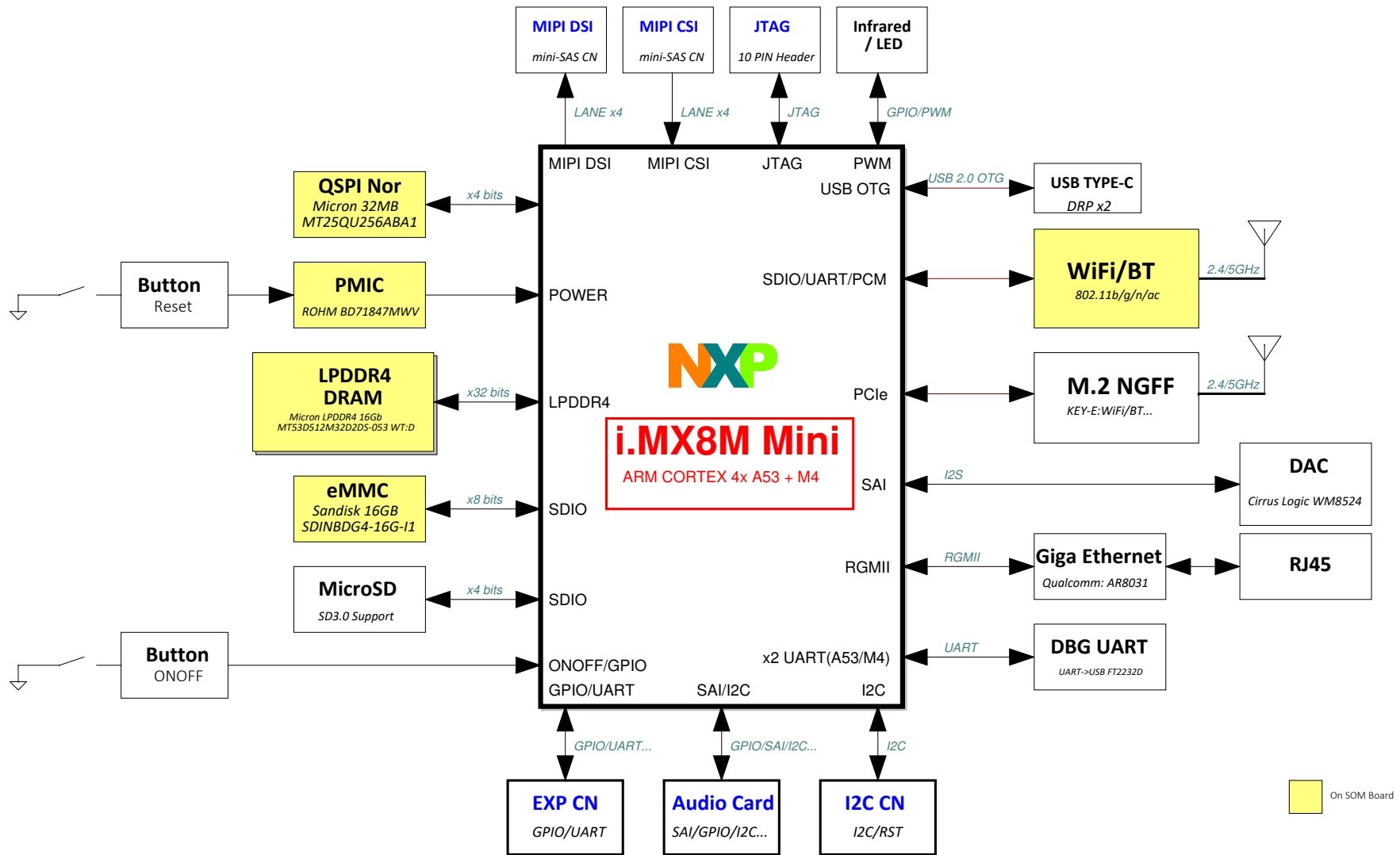
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Revision History

Rev. Code	Date	By	Description
A	2018-03-12	Frank	Initial version
A1	2018-03-27	Frank	1. Update U1 I.MX8M Mini symbol naming.
B	2018-05-01	Frank	1. Change PMIC U8 to BD71847; 2. Add external PU resistor R133 for SD2_nRST, as internal is PD and ROM won't pull it to high; 3. DNP R63,R64,C389,C390, as internal VREF works well;
B1	2018-06-19	Frank	1. Remove the IOMUX table;
C	2018-09-12	Frank	1. Remove optional 32K Crystal Circuit for i.MX8M Mini; 2. Remove external DDR VREF Circuit as Internal works well; 3. Add R134, R135 for BOOT_MODE3 option to TESTMODE for compatible design with i.MX8M Nano; 4. Change J4_Pin56 from GND to TESTMODE(BOOT_MODE3) for compatible design with i.MX8M Nano; 5. Remove R50, R62, R107, R128 to simplify the optional design; 6. Remove C7 for NVCC_3V3; 7. Update the symbol of i.MX8M Mini: > Correct naming for AB13 from PVCC0_1V8 to PVCC0_1P8; > Correct power domain for B27, C26 from NVCC_CLK to VDD_24M_XTAL_1P8; > Correct power domain for J23, J24 from VDDA_1P8 to VDD_ANA1_1P8; > Correct power domain for A22, B22, F22, A23, B23, F23 to VDD_USB_3P3; > Correct power domain for D22, E19, J23, E22 to VDD_USB_1P8, and also adjust the pin locations. 8. Update the description of the Block Diagram and Power Tree; 9. Update some descriptions of the schematic; 10. Add R136, C405 on VDD_MIP1_1V2 for compatible design with i.MX8M Nano;
C1	2018-11-29	Frank	1. Remove the note for R136;
C2	2019-1-31	Frank	1. Update the Min/Typ/Max operating range for I.MX8M Mini power supplies; 2. Add note for changing BD71847 BUCK1/2/5 output voltage according to the new operation range; 3. Add note for all IOs that internal pull up/down is not supported in 3.3V mode;
C3	2019-6-18	Frank	1. Update U8 Part Number BD71847MWV-E2 to BD71847AMWV-E2; 2. Populate R106, as external PU is necessary for Boundary Scan Mode, also update the note; 3. Add note for Boundary Scan mode: BOOT_MODE0, BOOT_MODE1, JTAG_MOD and TEST_MODE must be pulled to "1101" for i.MX8M Mini to enter Boundary Scan mode;

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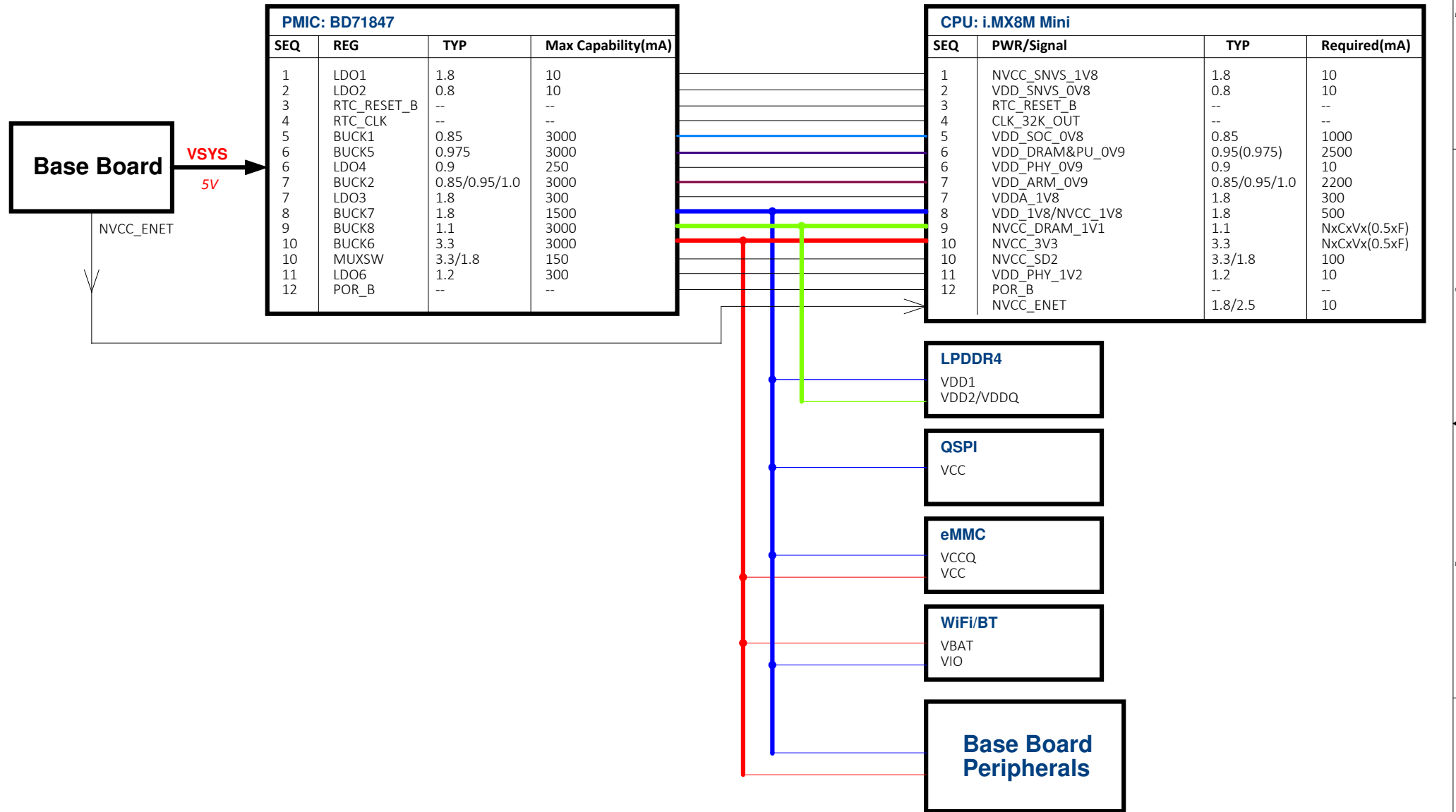
8MMINILPD4-EVK Block Diagram



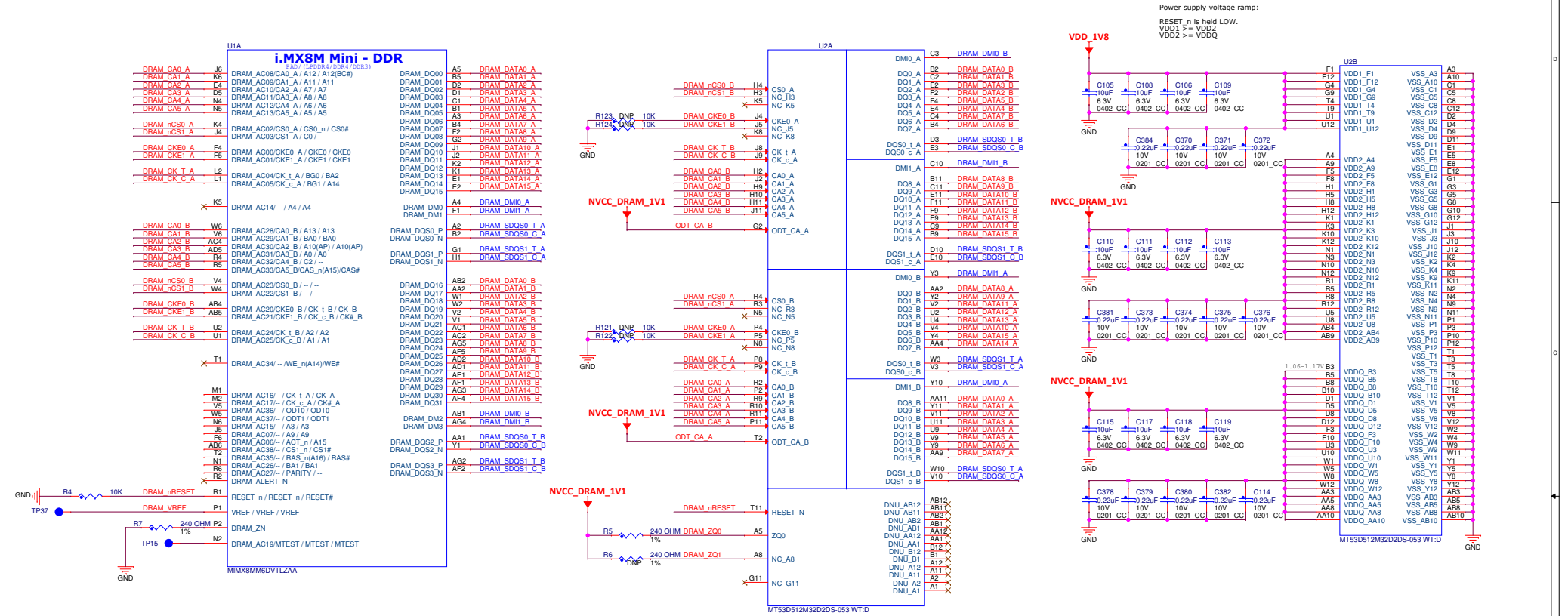
On SOM Board

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8MMINILPD4-EVK PWR TREE



LPDDR4 2GB

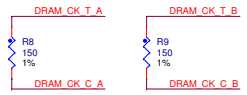


Data Bus

Pin Name	LPDDR4	DDR4
DRAM_DQ0_P	DQ0_0	DQ0_0
DRAM_DQ0_N	DQ0_1	DQ0_1
DRAM_DM0	DM0_0	DM0_0
DRAM_DQ1	DQ1_0	DQ1_0
DRAM_DQ2	DQ2_0	DQ2_0
DRAM_DQ3	DQ3_0	DQ3_0
DRAM_DQ4	DQ4_0	DQ4_0
DRAM_DQ5	DQ5_0	DQ5_0
DRAM_DQ6	DQ6_0	DQ6_0
DRAM_DQ7	DQ7_0	DQ7_0
DRAM_DS0_P	DS0_0	DS0_0
DRAM_DS0_N	DS0_1	DS0_1
DRAM_DM1	DM1_0	DM1_0
DRAM_DQ8	DQ8_0	DQ8_0
DRAM_DQ9	DQ9_0	DQ9_0
DRAM_DQ10	DQ10_0	DQ10_0
DRAM_DQ11	DQ11_0	DQ11_0
DRAM_DQ12	DQ12_0	DQ12_0
DRAM_DQ13	DQ13_0	DQ13_0
DRAM_DQ14	DQ14_0	DQ14_0
DRAM_DQ15	DQ15_0	DQ15_0
DRAM_DS1_P	DS1_0	DS1_0
DRAM_DS1_N	DS1_1	DS1_1
DRAM_DM2	DM2_0	DM2_0
DRAM_DQ16	DQ16_0	DQ16_0
DRAM_DQ17	DQ17_0	DQ17_0
DRAM_DQ18	DQ18_0	DQ18_0
DRAM_DQ19	DQ19_0	DQ19_0
DRAM_DQ20	DQ20_0	DQ20_0
DRAM_DQ21	DQ21_0	DQ21_0
DRAM_DQ22	DQ22_0	DQ22_0
DRAM_DQ23	DQ23_0	DQ23_0
DRAM_DS2_P	DS2_0	DS2_0
DRAM_DS2_N	DS2_1	DS2_1
DRAM_DM3	DM3_0	DM3_0
DRAM_DQ24	DQ24_0	DQ24_0
DRAM_DQ25	DQ25_0	DQ25_0
DRAM_DQ26	DQ26_0	DQ26_0
DRAM_DQ27	DQ27_0	DQ27_0
DRAM_DQ28	DQ28_0	DQ28_0
DRAM_DQ29	DQ29_0	DQ29_0
DRAM_DQ30	DQ30_0	DQ30_0
DRAM_DQ31	DQ31_0	DQ31_0

Command/Address

Pin Name	LPDDR4	DDR4
DRAM_RESET_N	RESET_n	RESET_n
DRAM_ALERT_N	ALERT_n	ALERT_n / MTEST1
DRAM_DM0	DM0_0	DM0_0
DRAM_DM1	DM1_0	DM1_0
DRAM_DM2	DM2_0	DM2_0
DRAM_DM3	DM3_0	DM3_0
DRAM_DM4	DM4_0	DM4_0
DRAM_DM5	DM5_0	DM5_0
DRAM_DM6	DM6_0	DM6_0
DRAM_DM7	DM7_0	DM7_0
DRAM_DM8	DM8_0	DM8_0
DRAM_DM9	DM9_0	DM9_0
DRAM_DM10	DM10_0	DM10_0
DRAM_DM11	DM11_0	DM11_0
DRAM_DM12	DM12_0	DM12_0
DRAM_DM13	DM13_0	DM13_0
DRAM_DM14	DM14_0	DM14_0
DRAM_DM15	DM15_0	DM15_0
DRAM_DS0_P	DS0_0	DS0_0
DRAM_DS0_N	DS0_1	DS0_1
DRAM_DS1_P	DS1_0	DS1_0
DRAM_DS1_N	DS1_1	DS1_1
DRAM_DS2_P	DS2_0	DS2_0
DRAM_DS2_N	DS2_1	DS2_1
DRAM_DS3_P	DS3_0	DS3_0
DRAM_DS3_N	DS3_1	DS3_1
DRAM_DS4_P	DS4_0	DS4_0
DRAM_DS4_N	DS4_1	DS4_1
DRAM_DS5_P	DS5_0	DS5_0
DRAM_DS5_N	DS5_1	DS5_1
DRAM_DS6_P	DS6_0	DS6_0
DRAM_DS6_N	DS6_1	DS6_1
DRAM_DS7_P	DS7_0	DS7_0
DRAM_DS7_N	DS7_1	DS7_1
DRAM_DS8_P	DS8_0	DS8_0
DRAM_DS8_N	DS8_1	DS8_1
DRAM_DS9_P	DS9_0	DS9_0
DRAM_DS9_N	DS9_1	DS9_1
DRAM_DS10_P	DS10_0	DS10_0
DRAM_DS10_N	DS10_1	DS10_1
DRAM_DS11_P	DS11_0	DS11_0
DRAM_DS11_N	DS11_1	DS11_1
DRAM_DS12_P	DS12_0	DS12_0
DRAM_DS12_N	DS12_1	DS12_1
DRAM_DS13_P	DS13_0	DS13_0
DRAM_DS13_N	DS13_1	DS13_1
DRAM_DS14_P	DS14_0	DS14_0
DRAM_DS14_N	DS14_1	DS14_1
DRAM_DS15_P	DS15_0	DS15_0
DRAM_DS15_N	DS15_1	DS15_1



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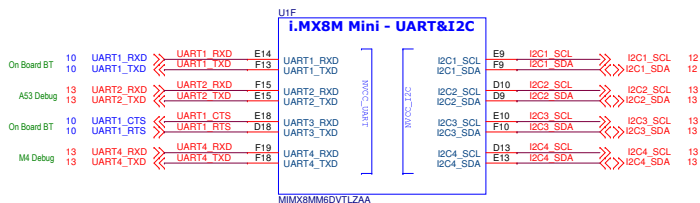
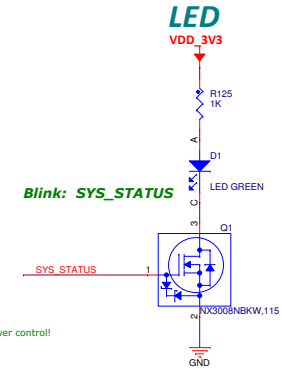
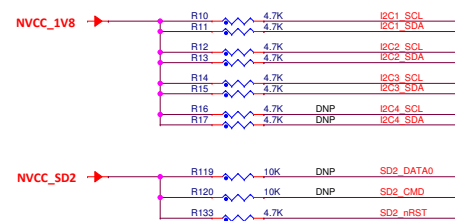
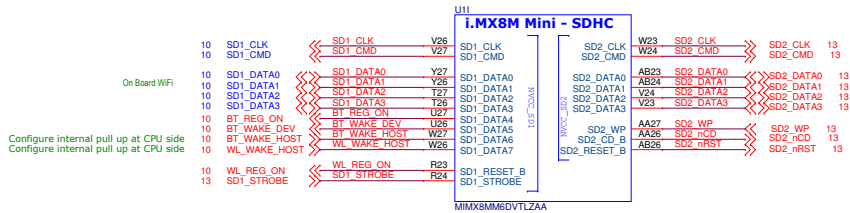
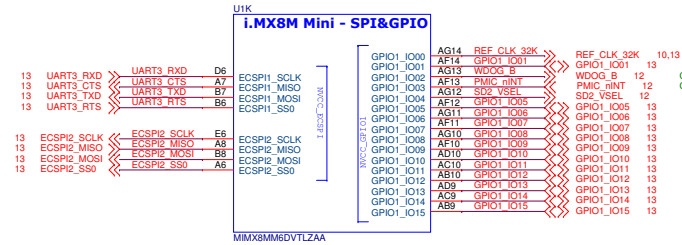
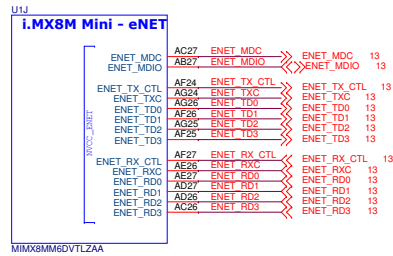
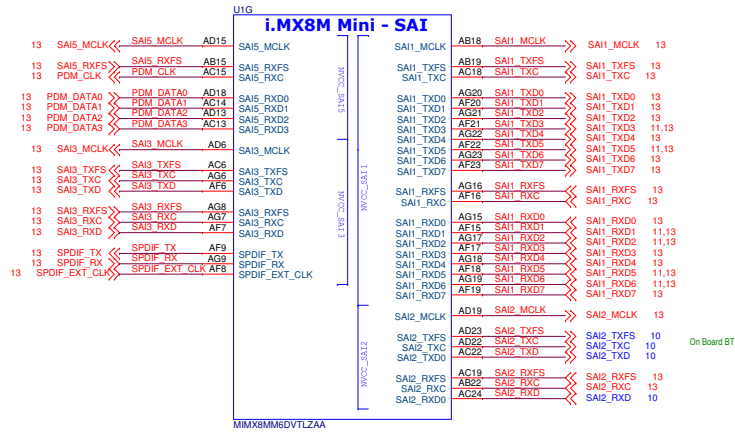
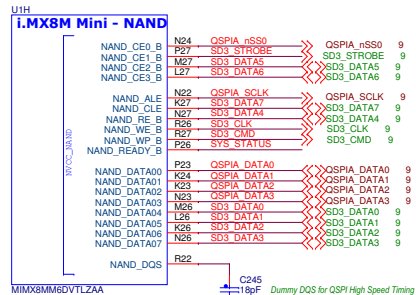
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i.MX8M Mini IO Interface

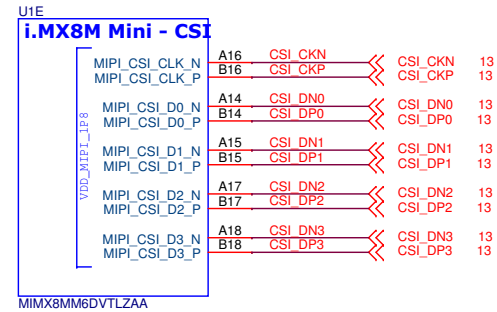
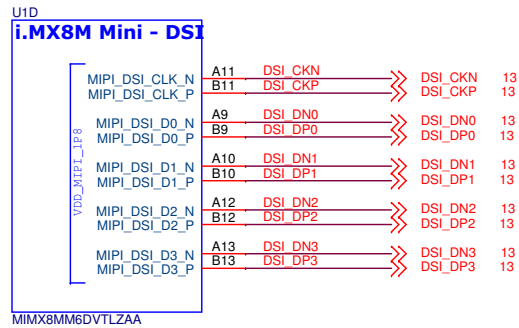
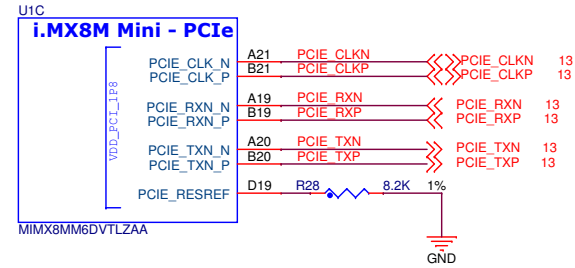
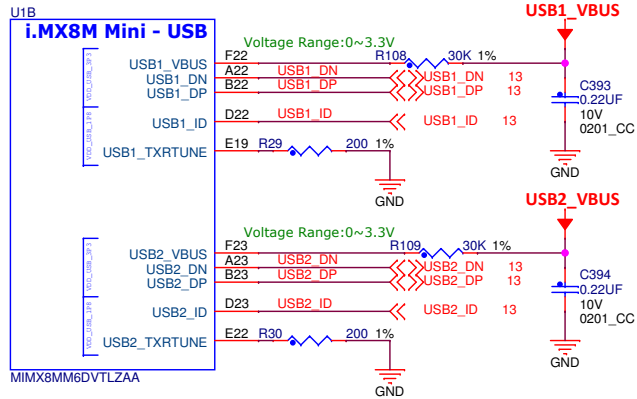
Caution:

IO internal pull up/down is not supported in 3.3V mode, must disable the internal pull up/down via software and use external pull up/down resistors instead.
All IO pin groups are impacted except for XTAL, DDR, PCI, USB and MIPI PHY IO's.
See Errata e50080 for detailed information.



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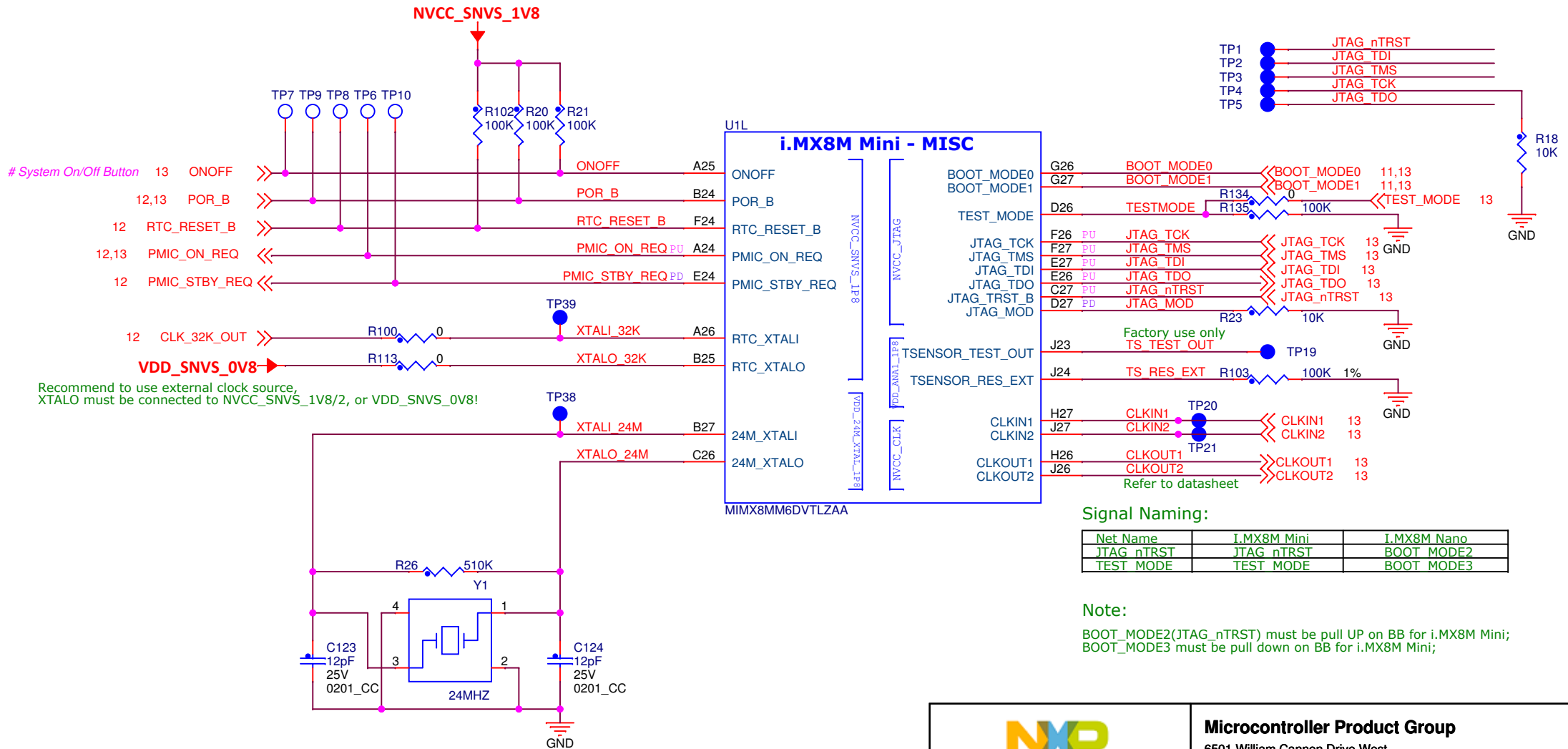
i.MX8M Mini PHYs



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i.MX8M Mini MISC

JTAG Debug



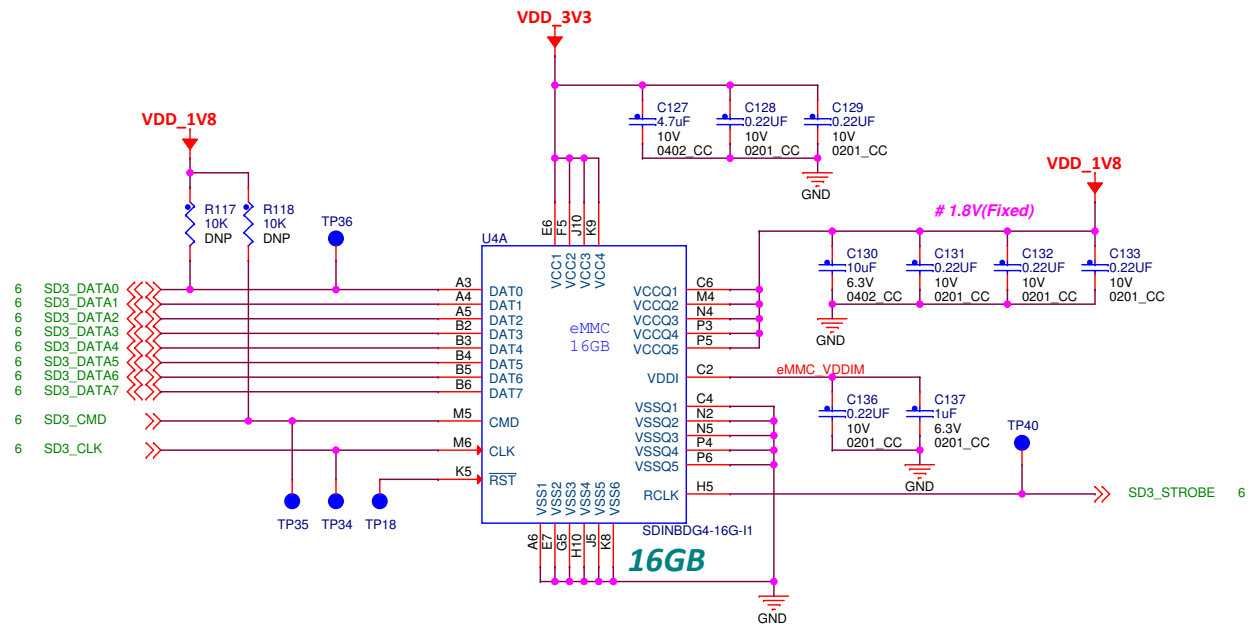
Caution:

BOOT_MODE0, BOOT_MODE1, JTAG_MOD and TEST_MODE must be pulled to "1101" for i.MX8M Mini to enter Boundary Scan mode.

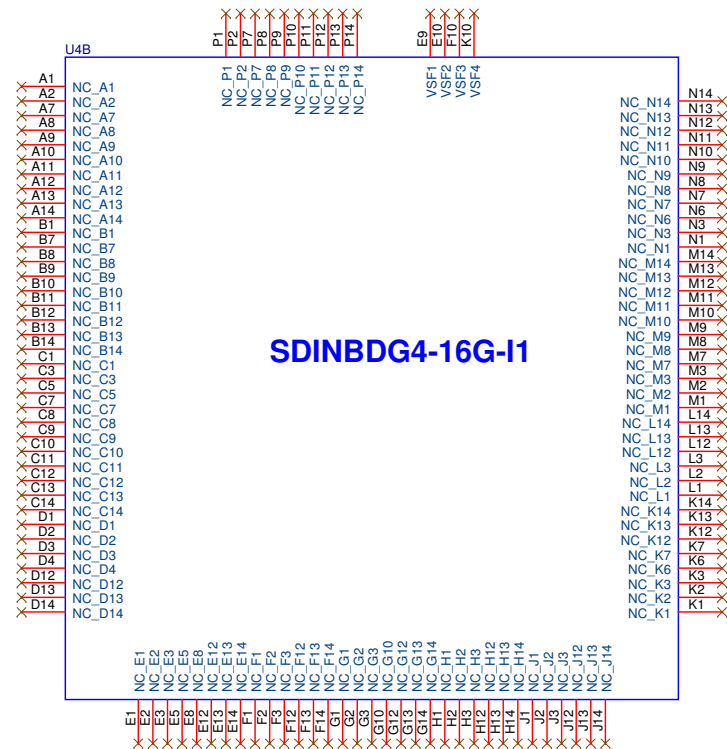
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Storage

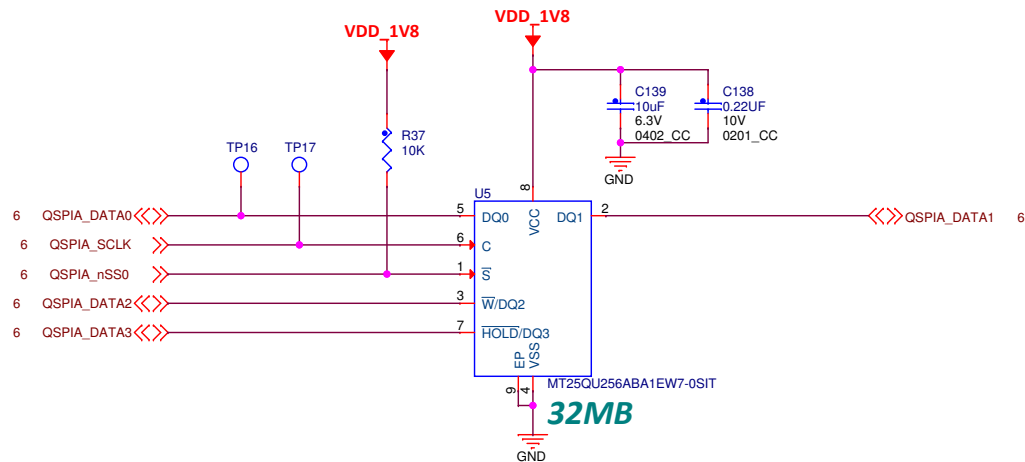
eMMC



SDINBDG4-16G-I1

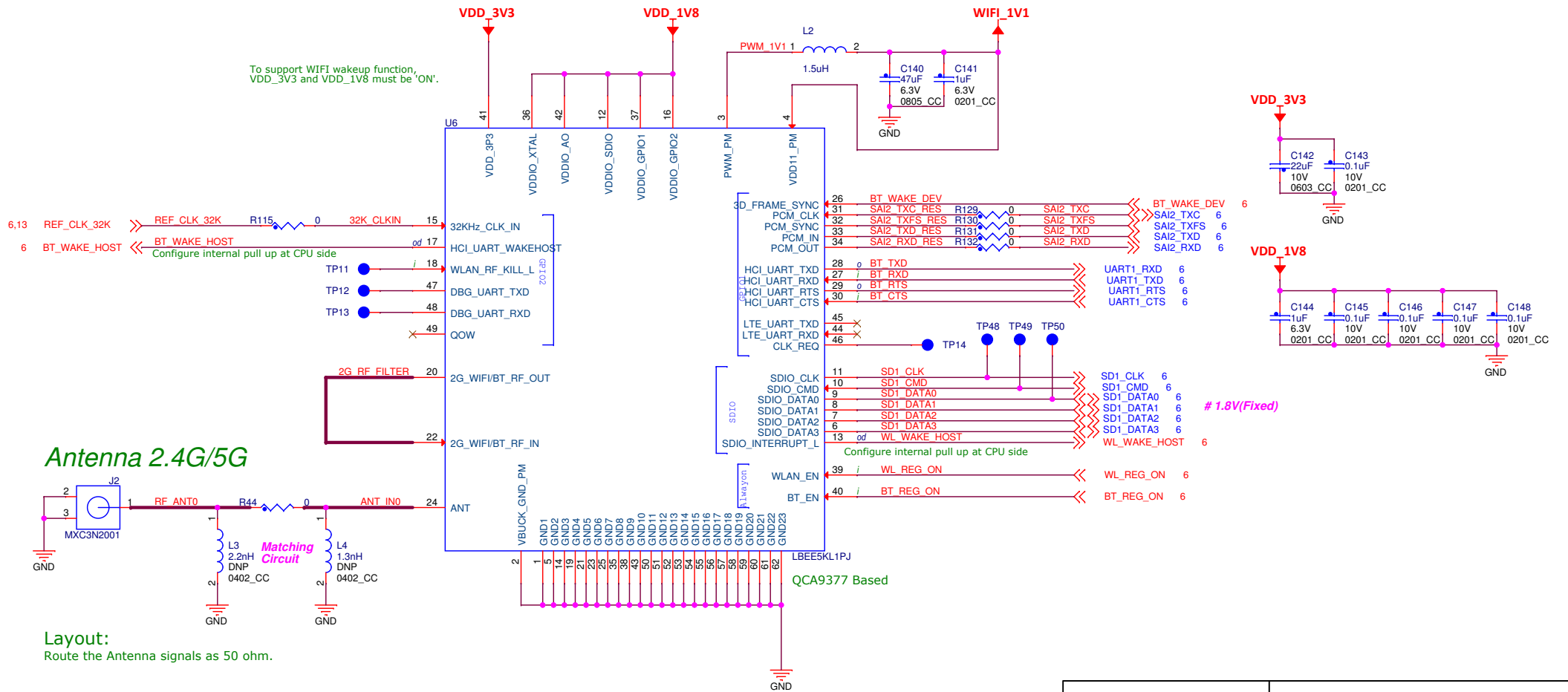


QSPI Flash



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2.4G/5G WIFI/BT Module



To support WIFI wakeup function, VDD_3V3 and VDD_1V8 must be 'ON'.

Antenna 2.4G/5G

Layout:
Route the Antenna signals as 50 ohm.

Power Sequence



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Boot Mode and CFG Switch

Caution:

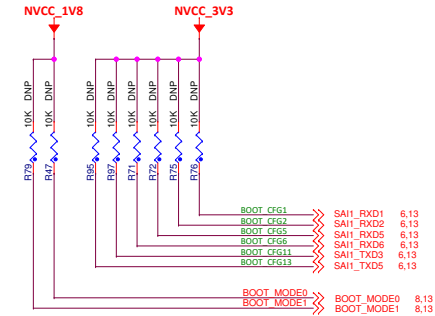
IO internal pull up/down is not supported in 3.3V mode, must disable the internal pull up/down via software and use external pull up/down resistors instead.
All IO pin groups are impacted except for XTAL, DDR, PCI, USB and MIPI PHY IO's.
See Errata e50080 for detailed information.

i.MX8M Mini ROM Fuse

Address	7	6	5	4	3	2	1	0	
0x470[15:8]	BOOT_CFG[15]	BOOT_CFG[14]	BOOT_CFG[13]	BOOT_CFG[12]	BOOT_CFG[11]	BOOT_CFG[10]	BOOT_CFG[9]	BOOT_CFG[8]	
0x470[15:8]	Infini-Loop (Debug USE only) 0 - Disable 1 - Enable	001 - SD/eSD	010 - MMC/eMMC		Port Select: 00 - USDHC1 01 - USDHC2 10 - USDHC3	Power Cycle Enable '0' - No power cycle '1' - Enabled via		SD Loopback Clock Source Sel. (for SDR50 and SDR104 only) '0' - through SD pad '1' - direct	
0x470[15:8]		011 - NAND	Pages In Block: 00 - 128 01 - 64 10 - 32 11 - 256		Nand_Row_address_bytes: 00 - 3 01 - 2 10 - 4 11 - 5				
0x470[15:8]		100 - QSPI	Flash Auto Probe	FLASH_TYPE 000-Device supports 3B read by default 001-Device supports 4B read by default 010-HyperFlash 1V8 011-HyperFlash 3V3 100-MXIC Octal DDR					
0x470[15:8]		110 - SPI NOR	Port Select: 000 - eCSP#1 001 - eCSP#2 010 - eCSP#3		SPI Addressing: 0 - 3-bytes (24-bit) 1 - 2-bytes (16-bit)				
0x470[15:8]		Others - Reserved for future use							
	BOOT_CFG[7]	BOOT_CFG[6]	BOOT_CFG[5]	BOOT_CFG[4]	BOOT_CFG[3]	BOOT_CFG[2]	BOOT_CFG[1]	BOOT_CFG[0]	
SD/eSD	0x470[7:0]	Reserved	Reserved	Bus Width: 0 - 1-bit 1 - 4-bit	Speed 000 - Normal/SDR12 001 - High/SDR25 010 - SDR50 011 - SDR104 101 - Reserved for DDR50 101 - Reserved	Reserved		Reserved	
MMC/eMMC	0x470[7:0]	Fast Boot: 0 - Regular 1 - Fast Boot	Bus Width: 000 - 1-bit 001 - 4-bit 010 - 8-bit 101 - 4-bit DDR (MMC 4.4) 110 - 8-bit DDR (MMC 4.4) Else - reserved.		Speed 00 - Normal 01 - High 10 - Reserved for HS200 11 - Reserved	USDHC IO VOLTAGE SELECTION For Normal Boot Mode 0 - 3.3V 1 - 1.8V	USDHC IO VOLTAGE SELECTION For Manufacture Mode 0 - 3.3V 1 - 1.8V		
NAND	0x470[7:0]		BT_TOGGLEMODE	BOOT_SEARCH_COUNT: 00 - 2 01 - 2 10 - 4 11 - 8	Toggle Mode 33MHz Preamble Delay, Read Latency: '000' - 16 GPMICKL cycles. '001' - 1 GPMICKL cycles. '010' - 2 GPMICKL cycles. '011' - 3 GPMICKL cycles. '100' - 4 GPMICKL cycles. '101' - 5 GPMICKL cycles. '110' - 6 GPMICKL cycles. '111' - 7 GPMICKL cycles. '1111' - 15 GPMICKL cycles.		Reserved		
FlexSPI	0x470[7:0]	HOLD TIME: 00 - 500us 01 - 1ms 10 - 3ms 11 - 10ms		FLASH Auto Probe Type	FlexSPI FLASH Dummy Cycle				
SPINOR	0x470[7:0]	CS select SPI only: 00 - CS#0 default 01 - CS#1 10 - CS#2 11 - CS#3	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	

BT_CFG Pins:

SAI1_RXD0	BOOT_CFG0
SAI1_RXD1	BOOT_CFG1
SAI1_RXD2	BOOT_CFG2
SAI1_RXD3	BOOT_CFG3
SAI1_RXD4	BOOT_CFG4
SAI1_RXD5	BOOT_CFG5
SAI1_RXD6	BOOT_CFG6
SAI1_RXD7	BOOT_CFG7
SAI1_RXD8	BOOT_CFG8
SAI1_RXD9	BOOT_CFG9
SAI1_RXD10	BOOT_CFG10
SAI1_RXD11	BOOT_CFG11
SAI1_RXD12	BOOT_CFG12
SAI1_RXD13	BOOT_CFG13
SAI1_RXD14	BOOT_CFG14
SAI1_RXD15	BOOT_CFG15



Note:

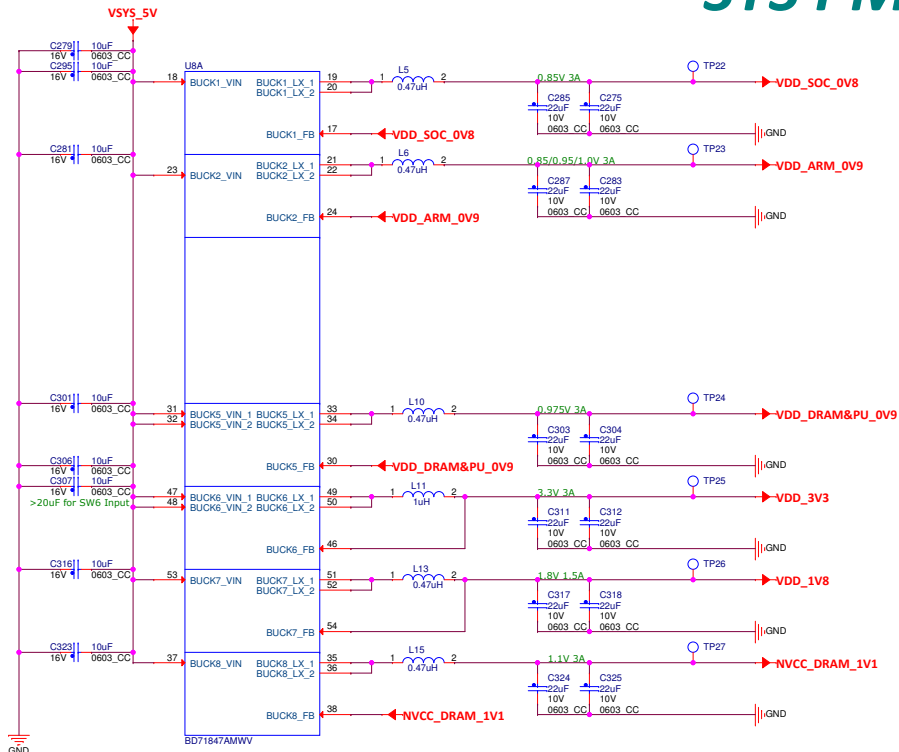
- Bootfg/SAI1 signals have internal PD before and after POR_B reset is deasserted!
- Standalone SOM board can support eMMC/SDHC3 boot, by populating R71, R72, R75, R76, R79, R95, R97!
- When using Base Board for Multi boot selection, you must keep the resistors DNP on SOM board!

Boot Mode

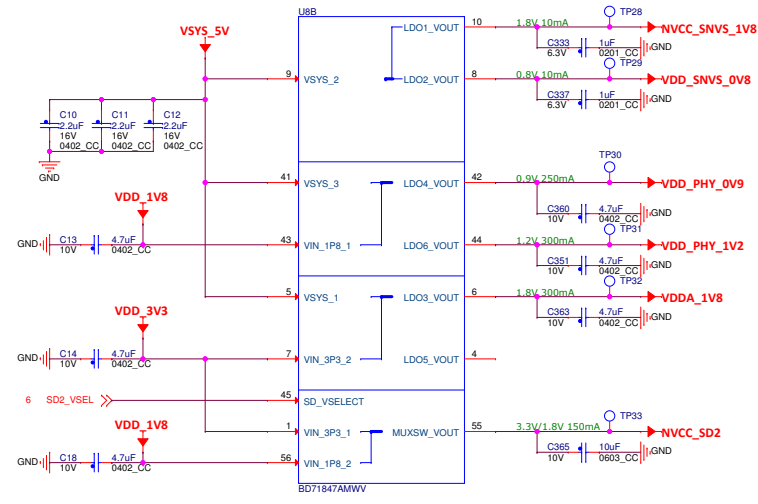
BOOT_MODE1	BOOT_MODE0
BOOT TYPE:	
00 Boot From Fuses	
01 Serial Downloader	
10 Internal Boot (Development)	
11 Reserved	

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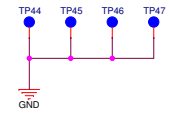
SYS PMIC



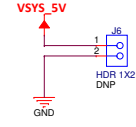
Note:
 BUCK1 default output voltage is 0.8V. Software will change it to 0.85V in SPL before DDR initialization.
 BUCK5 default output voltage is 0.9V. Software will change it to 0.975V(BD71847 BUCK5 doesn't support 0.95V output) in SPL before DDR initialization.
 BUCK2 default output voltage is 0.9V. Software will change it to 0.85V for 1.2GHz operation, 0.95V for 1.6GHz, 1.0V for 1.8GHz.



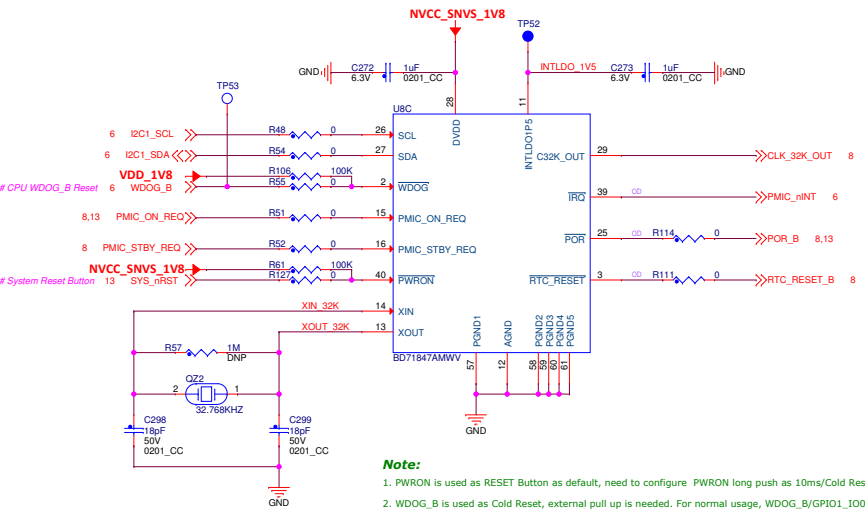
GND Testpoints



Backup PWR Supply



SEQ	PWR/Signal	REG	MIN	TYP	MAX	Max Current(mA)
1	NVCC_SNV5_1V8	LDO1	1.62	1.8	1.98	10
2	VDD_SNV5_0V8	LDO2	0.76	0.8	0.9	10
3	RTC_RESET_B	RTC_RESET_B	--	--	--	--
4	CLK_32K_OUT	RTC_CLK	--	--	--	--
5	VDD_SOC_0V8	BUCK1	0.78/0.805	0.82/0.85	0.9	3000
6	VDD_DRAM&PU_0V9	BUCK5	0.805/0.855	0.85/0.95	0.9/1.0	3000
6	VDD_PHY_0V9	LDO4	0.855	0.9	1.0	250
7	VDD_ARM_0V9	BUCK2	0.805/0.9/0.95	0.85/0.95/1.0	0.95/1.0/1.05	3000
7	VDDA_1V8	LDO3	1.71	1.8	1.89	300
8	VDD_1V8/NVCC_1V8	BUCK7	1.65	1.8	1.95	1500
9	NVCC_DRAM_1V1	BUCK8	1.06	1.1	1.14	3000
10	VDD_3V3/NVCC_3V3	BUCK6	3	3.3	3.6	3000
10	NVCC_SD2	MUXSW	3.0/1.65	3.3/1.8	3.6/1.95	150
11	VDD_PHY_1V2	LDO6	1.14	1.2	1.26	300
12	POR_B	POR_B	--	--	--	--



Note:
 1. PWRON is used as RESET Button as default, need to configure PWRON long push as 10ms/Cold Reset, and disable short push detect!
 2. WDOG_B is used as Cold Reset, external pull up is needed. For normal usage, WDOG_B/GPIO1_I002 has internal pull up, don't need the external PU resistor, but in Boundary Scan mode, this pin is floating, external PU is necessary.

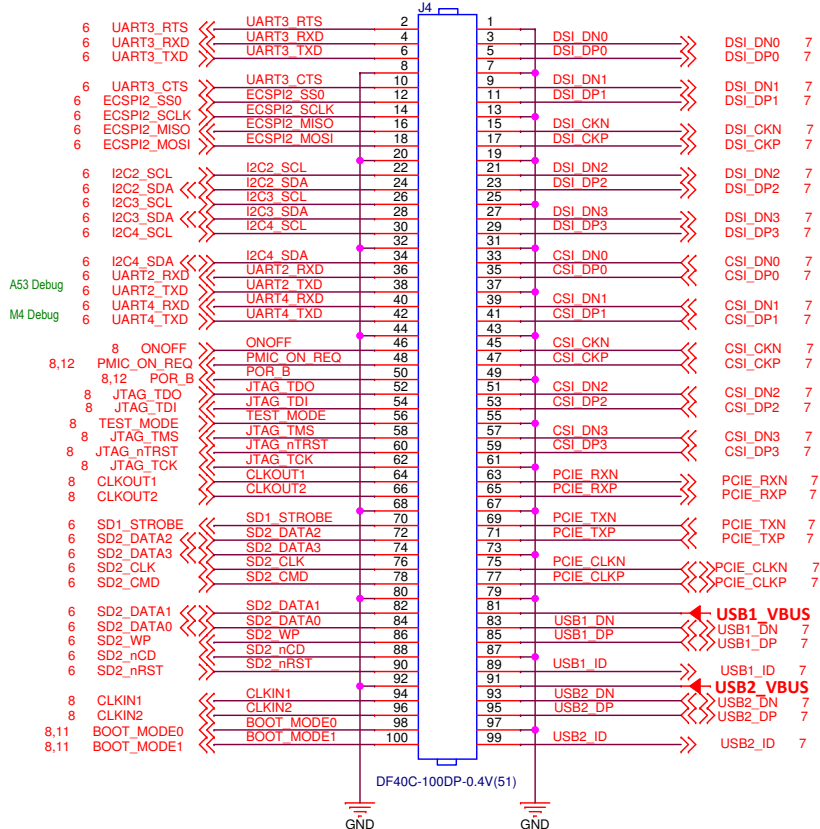
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Approved: <Approver>		Size C	Document Number SCH-31399 PDF: SPF-31399
Date: Monday, June 10, 2019		Sheet 12 of 18	Rev CS

B2B Connector for CPU Board

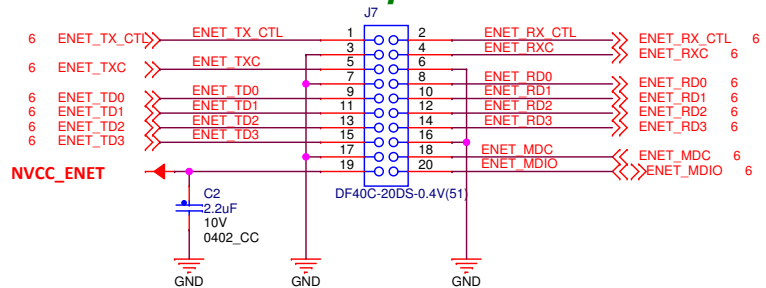
Caution:

IO internal pull up/down is not supported in 3.3V mode, must disable the internal pull up/down via software and use external pull up/down resistors instead.
All IO pin groups are impacted except for XTAL, DDR, PCI, USB and MIPI PHY IO's.
See Errata e50080 for detailed information.

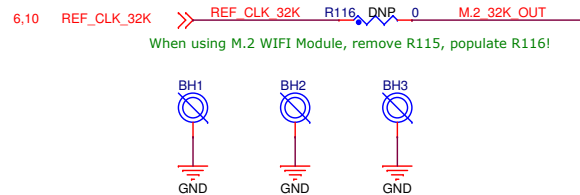
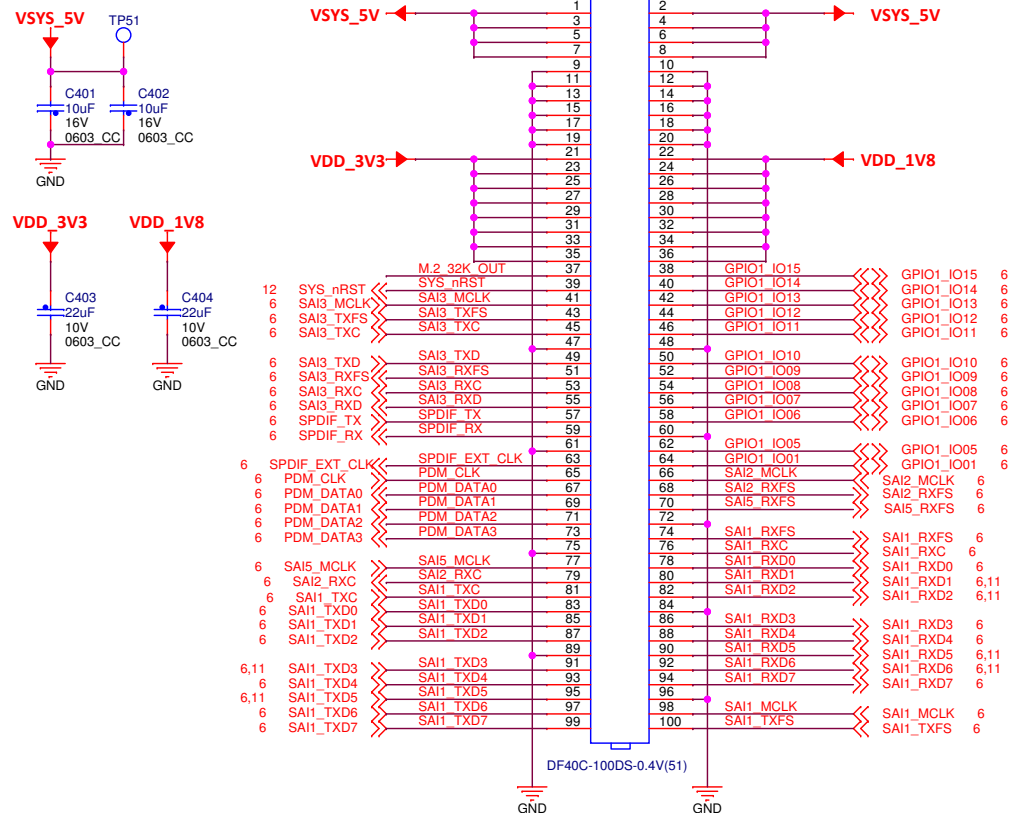
Header



Receptacle



Receptacle



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Drawn by: Frank Liu		Size B Document Number SCH-31399 PDF: SPF-31399		Rev C3
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