

MCIMX8M-EVK

(i.MX8M Customer Board)

Schematics DevBoard

Table of Content

Page 1	Cover
Page 2	Block Diagram
Page 3	PWR TREE
Page 4	CPU PWR
Page 5	LPDDR4
Page 6	CPU IO
Page 7	CPU PHY
Page 8	CPU MISC
Page 9	eMMC/NAND/TF/QSPI
Page 10	PMIC
Page 11	BOOT CFG
Page 12	USB
Page 13	HDMI
Page 14	CODEC
Page 15	Ethernet
Page 16	WiFi/BT
Page 17	PCIe
Page 18	MIP/D/CSI
Page 19	MicroSD/IR/LED/BTN
Page 20	Debug
Page 21	EXP CN
Page 22	NOTE
Page 23	IOMUX
Page 24	MESH
Page 25	
Page 26	
Page 27	
Page 28	
Page 29	

Revision History

Rev. Code	Date	By	Description
A	2016-12-09	Javen	1 Revision preliminary version
A1	2017-05-26	Javen	1 Change J1401 M2 connector from sink type to non-sink type 2 Update U1001 schematic lib 3 Add R760 to control the VDD_SNVS_OV9 power up sequence 4 DNP D903, R915, change R936 to 442K, Add R942, R943, D910 5 Change R715 to 10K, add R761 44.2K OHM, D402, C799 1uF0402 6 Add Q1402-Q1404, R1458-R1462, C1439-C1441 to prevent current drop during power up due to CAP, DNP C1418, C1419 7 Add R1802, R1803 to keep VIO voltage for IO REF 8 J801 change to female header 9 Change D1702, D1703 connection to reduce the CP2105 Program step 10 Change R934 to 1K OHM 11 Add R846, R846 for backup 12 Add C778, C929-C932 13 J1201 PIN2 change to 2.5V 14 Add R510, R511, R512, R513 as back up of different HCSL OSC 15 Exchange UART1 and UART2 on CP2105 due to ECI support special input 16 DNP R909, R910, R911, R912, install R905, R906, R907, R908 17 Add L104 FB for PLL to reduce noise 18 Add R764, O704, R763 to support over drive mode
B1	2017-07-24	Javen	1 Change WiFi to QCA6174A 2 Change USB TYPE-C connector 3 Change R1004, R1009 PU to DDCD_5V_CN 4 Add C714 to prevent ARM voltage drop when DVFS from 1.0V to 0.9V 5 DNP R1227 6 Add R1427, Q1405, R1483, D1483, D403 7 Change R1459 to PCIe_rDIS 8 Install R1411, R1442, R1448, C401 9 Change C913 to 1rF 10 Change R842 to 1M OHM 11 DNP C727 add C781 to prevent the power up sequence
B2	2017-08-14	Javen	1 Add C781 2 Add R1484, D1404, D1405 for WiFi enable backup 3 DNP D1609 to prevent the SDIO power on later than POR_B 4 Install R409 4.7K, change R401 to 0 OHM 5 Add R821 for backup
B3	2017-10-26	Javen	1 Update U907 PTN51100HQ agile number 2 Change SIMTSSO BH1406 Part, DNP BH1405
B4	2018-03-07	Javen	1 Add D706, D1704 as backup. 2 Add TP901 for test 3 Add U1501, U1502 for I2C level shifter, change J1502, J1503 I2C port, remove Q1503, Q1504 4 Update J1101 audio jack 3/4-seg to GND, remove TVS1102, TVS1102 5 Add D1510, R1531, R1530, DNP R621, D1507
B4.1	2018-05-21	Javen	1 DNP D1704 2 Update J1601, U601 PN
B5	2018-08-16	Javen	1 Add note to support PCIe L1.1 substrate

1. Unless Otherwise Specified:

- All resistors are in ohms, 10%, 1/8 Watt, 0603
- All capacitors are in uF, 20%, 50V, 0603
- All voltages are DC
- All polarized capacitors are aluminum electrolytic

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.


4. Special signal usage:

- _B Denotes - Active-Low Signal
- <-> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

Preliminary - Subject to Change without Notice!

This board was designed for maximum flexibility in software development and demonstrates multiple functions possible with i.MX processors. Although best design practices have been applied, some areas may not be suitable for a mass-production design.

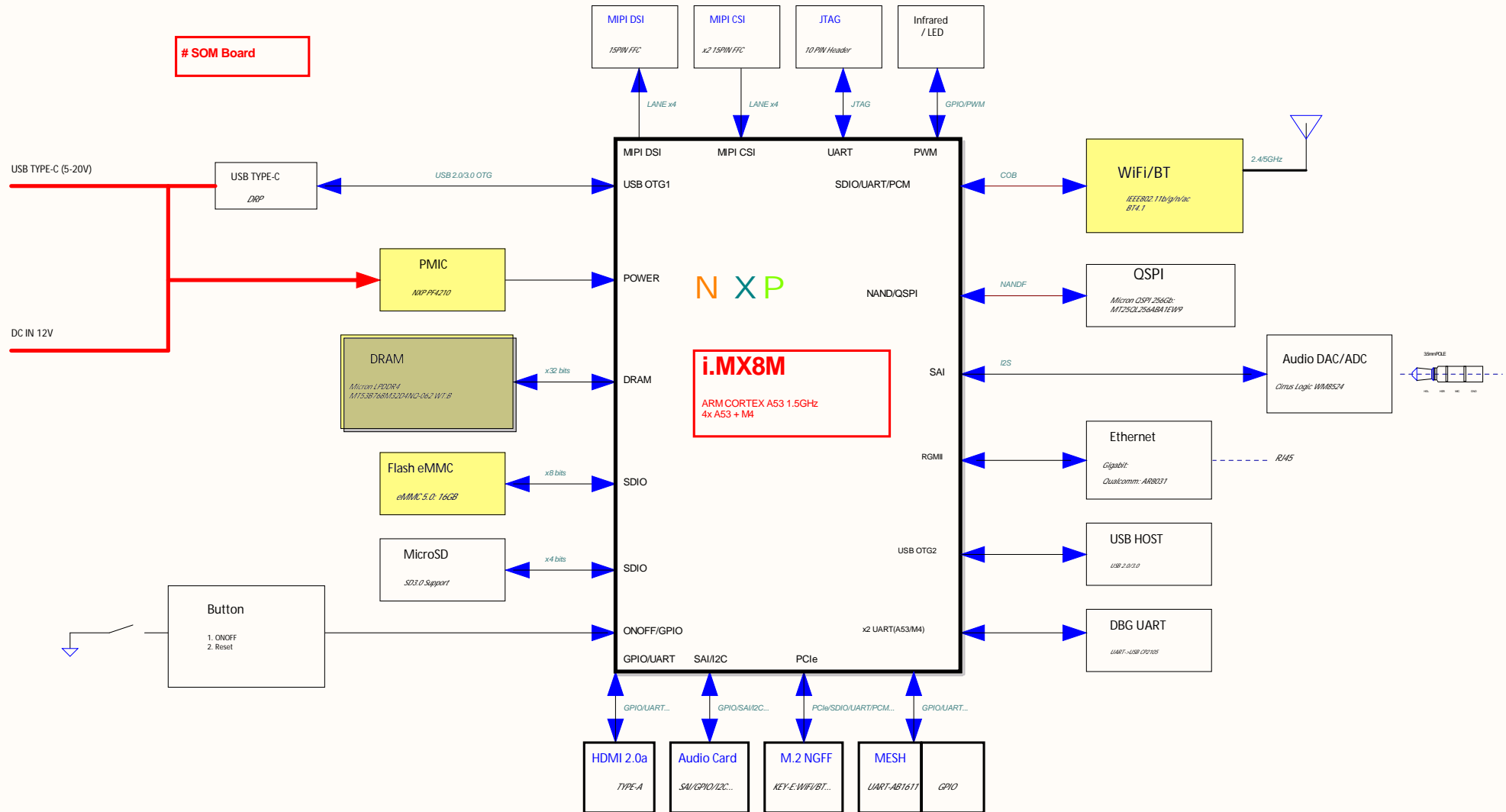
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Quantity -> JAV	Page Title	Title and Rev History	
Approved	Rev	Document Number	Rev
	HC	ICM328155DF-BF-2015	01
Date		Sheet	1 of 25

i.MX8M EVK BLOCK DIAGRAM

MCIMX8M-EVK
MCIMX8M-AUD

SoC: MIMX8MQ6DVAJ2AA

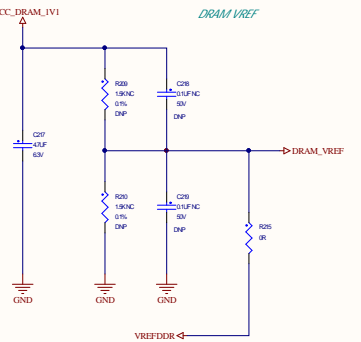
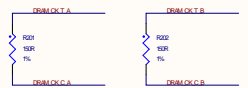
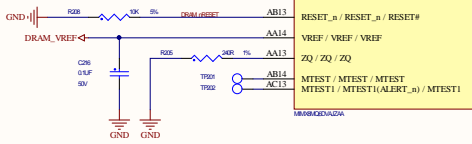
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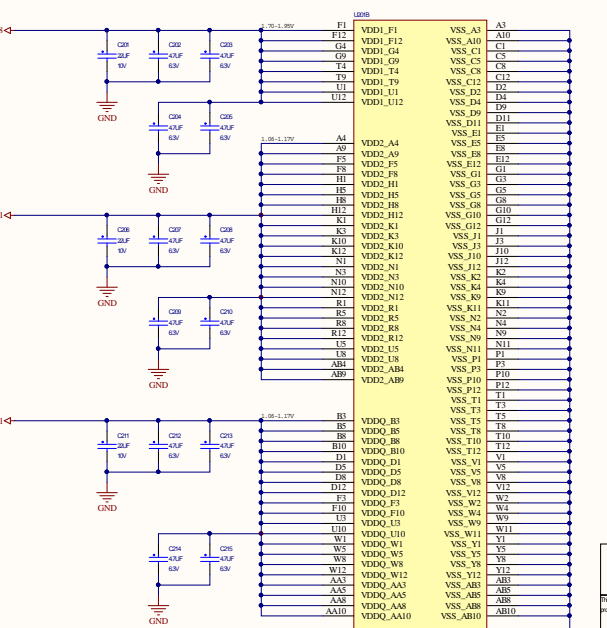
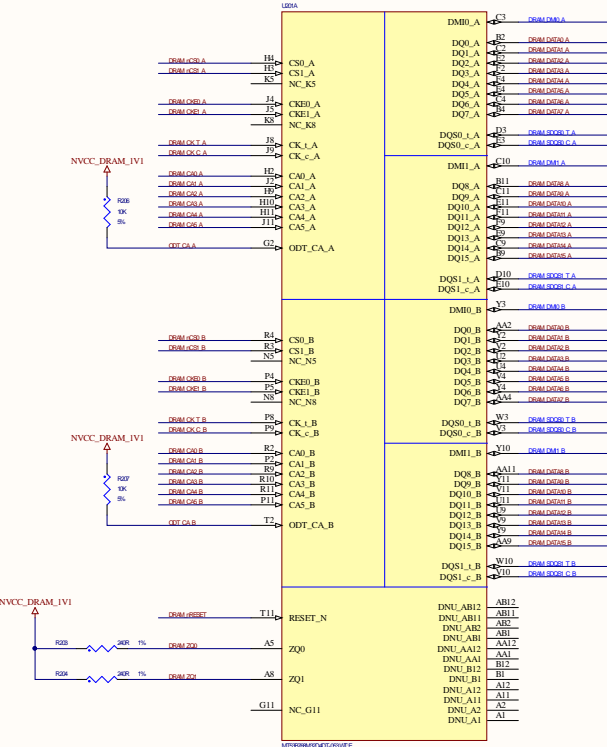
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Drawn by -s3p-	Page Title Block Diagram					
Approved	Doc No.	Document Number	iM8MSEPDF-BF-2015		File No.	
Date	Rev	2	of	25	16	

LMX8M - DDR

DRAM_C0.A	AE17	CA0_A / A12 / A12(BCP)	DRAM_DQ00	AE23	DRAM_DQ0A
DRAM_C0.B	AE16	CA1_A / A11 / A11	DRAM_DQ01	AE24	DRAM_DQ0B
DRAM_C0.C	AE15	CA2_A / A7 / A7	DRAM_DQ02	AE25	DRAM_DQ0C
DRAM_C0.D	AE10	CA3_A / A8 / A8	DRAM_DQ03	AE22	DRAM_DQ0D
DRAM_C0.E	AE19	CA4_A / A6 / A6	DRAM_DQ04	AA24	DRAM_DQ0E
DRAM_C0.F	AE19	CAS_A / A5 / A5	DRAM_DQ05	Y35	DRAM_DQ0F
DRAM_C0.G	AE18	CS0_A / CS0_n / CS0#	DRAM_DQ06	AA25	DRAM_DQ0G
DRAM_C0.H	AC18	CS1_A / CD / --	DRAM_DQ07	AE25	DRAM_DQ0H
DRAM_C0.I	AC16	CKE0_A / CKE0 / CKE0	DRAM_DQ08	AA22	DRAM_DQ0I
DRAM_C0.J	AE17	CKE1_A / CKE1 / CKE1	DRAM_DQ09	AA23	DRAM_DQ0J
DRAM_C0.K	AD14	CK_L_A / BG0 / BA2	DRAM_DQ10	AA18	DRAM_DQ0K
DRAM_C0.L	AE14	CK_c_A / BG1 / A14	DRAM_DQ11	AA20	DRAM_DQ0L
DRAM_C0.M	AB16	-- / A1 / A4	DRAM_DQ12	AA19	DRAM_DQ0M
DRAM_C0.N	AE8	CA0_B / C2 / --	DRAM_DQ13	AA19	DRAM_DQ0N
DRAM_C0.O	AE9	CA1_B / CAS_n(A15) / CAS#	DRAM_DQ14	AA17	DRAM_DQ0O
DRAM_C0.P	AE7	CAC_B / BA0 / BA0	DRAM_DQ15	AD23	DRAM_DQ0P
DRAM_C0.Q	AE6	CAI_B / A10(AP) / A10(AP)	DRAM_DM0	AE30	DRAM_DM0
DRAM_C0.R	AD6	CAS_B / A0 / A0	DRAM_DM1	AC24	DRAM_DM1
DRAM_C0.S	AC9	CS0_B / -- / --	DRAM_DM2	AC25	DRAM_DM2
DRAM_C0.T	AD8	CS1_B / -- / --	DRAM_DM3	AE3	DRAM_DM3
DRAM_C0.U	AD10	CKE0_B / CK_L_B / CK_B	DRAM_DM4	AE2	DRAM_DM4
DRAM_C0.V	AE10	CKE1_B / CK_c_B / CKF_B	DRAM_DM5	AE4	DRAM_DM5
DRAM_C0.W	AD12	CK_L_B / A2 / A2	DRAM_DM6	AA2	DRAM_DM6
DRAM_C0.X	AE12	CK_c_B / A1 / A1	DRAM_DM7	Y1	DRAM_DM7
DRAM_C0.Y	AC10	-- / WE_n(A14) / WE#	DRAM_DM8	AA1	DRAM_DM8
DRAM_C0.Z	AD15	-- / CK_c_A / CKF_A	DRAM_DM9	AA4	DRAM_DM9
DRAM_C1.A	AE15	-- / CK_L_A / CK_A	DRAM_DM10	AA3	DRAM_DM10
DRAM_C1.B	AE11	-- / ODT0 / ODT0	DRAM_DM11	AA6	DRAM_DM11
DRAM_C1.C	AE11	-- / ODT1 / ODT1	DRAM_DM12	AA8	DRAM_DM12
DRAM_C1.D	AC15	-- / A3 / A3	DRAM_DM13	AA7	DRAM_DM13
DRAM_C1.E	AE13	-- / A9 / A9	DRAM_DM14	AA9	DRAM_DM14
DRAM_C1.F	AC11	-- / ACT_n / A15	DRAM_DM15	AC2	DRAM_DM15
DRAM_C1.G	AE10	-- / CS_L_n / CS#	DRAM_DM16	AC1	DRAM_DM16
DRAM_C1.H	AE12	-- / RAS_n(A16) / RAS#	DRAM_DM17	AE5	DRAM_DM17
DRAM_C1.I	AE10	-- / BA1 / BA1	DRAM_DM18	AC5	DRAM_DM18
DRAM_C1.J	AE12	-- / PARITY_n / --	DRAM_DM19		
DRAM_C1.K	AE12		DRAM_DM20		
DRAM_C1.L	AE12		DRAM_DM21		
DRAM_C1.M	AE12		DRAM_DM22		
DRAM_C1.N	AE12		DRAM_DM23		
DRAM_C1.O	AE12		DRAM_DM24		
DRAM_C1.P	AE12		DRAM_DM25		
DRAM_C1.Q	AE12		DRAM_DM26		
DRAM_C1.R	AE12		DRAM_DM27		
DRAM_C1.S	AE12		DRAM_DM28		
DRAM_C1.T	AE12		DRAM_DM29		
DRAM_C1.U	AE12		DRAM_DM30		
DRAM_C1.V	AE12		DRAM_DM31		
DRAM_C1.W	AE12		DRAM_DM32		
DRAM_C1.X	AE12		DRAM_DM33		
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DRAM_C1.Z	AE12		DRAM_DM35		

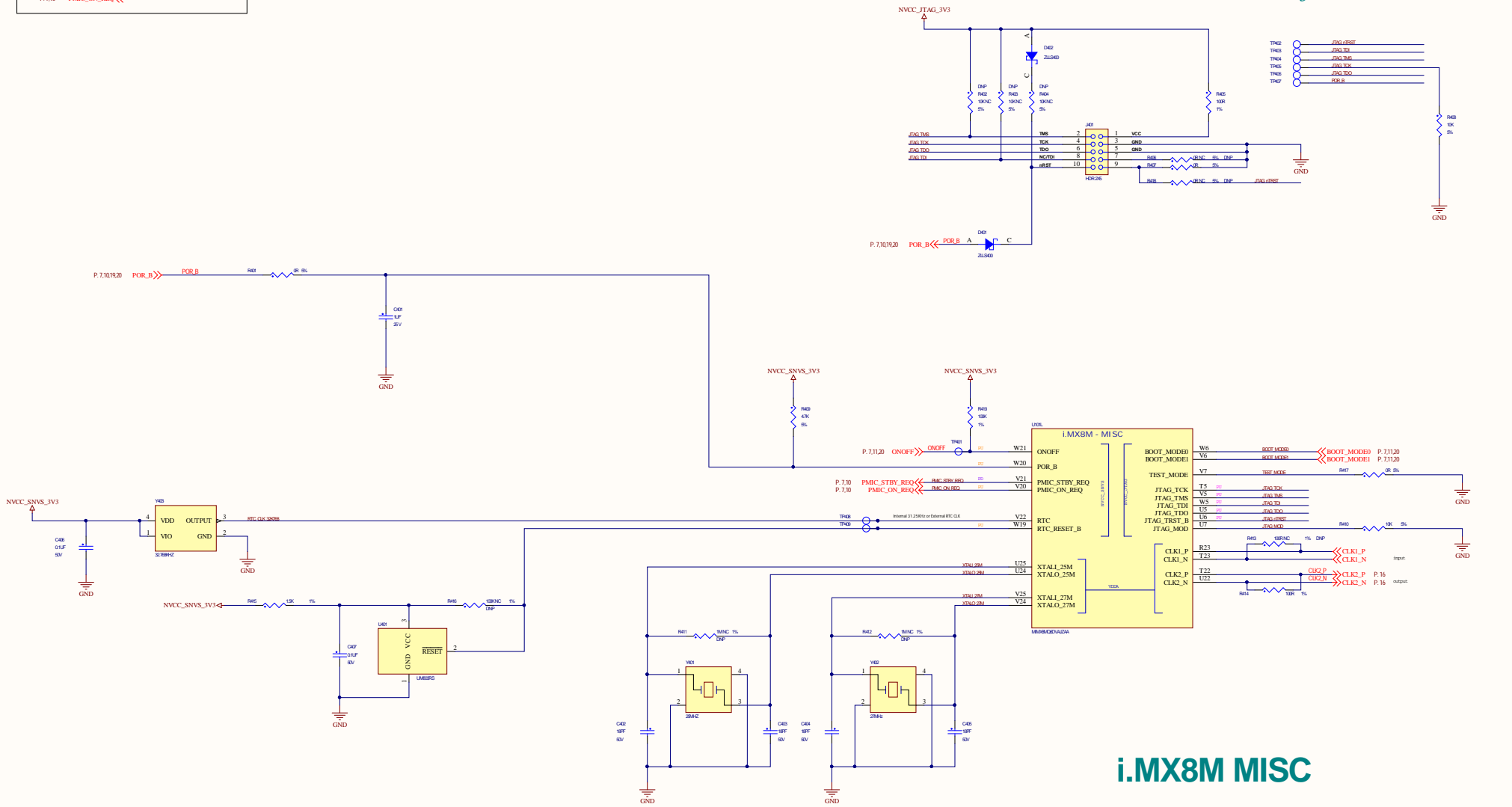


LPDDR4 Power supply voltage clamp
 R02F 20k Ohm Low VDD1 - VDD5
 VDD1 - VDD5



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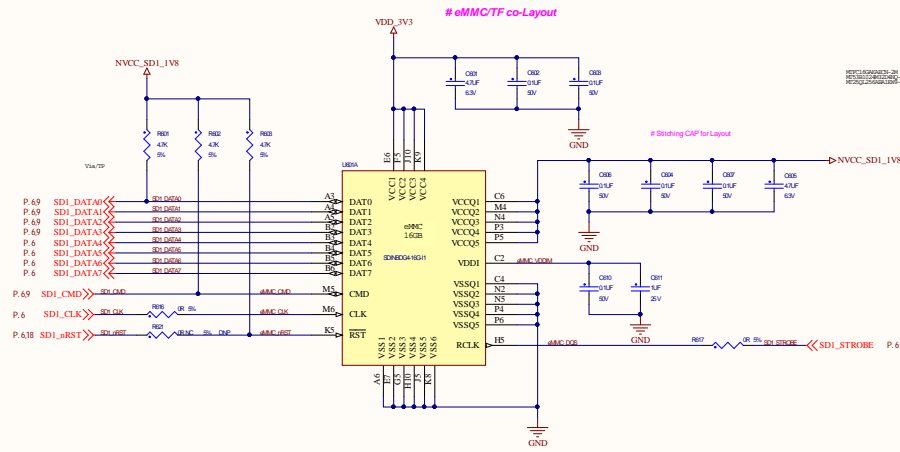
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P.7.11.20	BOOT_MODE1	BOOT_MODE1
P.7.11.20	ONOFF	ONOFF
P.7.10	PMIC_STBY_REQ	PMIC_STBY_REQ
P.7.10	PMIC_ON_REQ	PMIC_ON_REQ



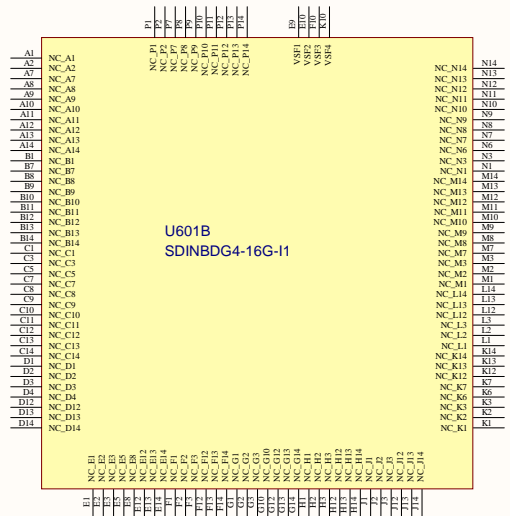
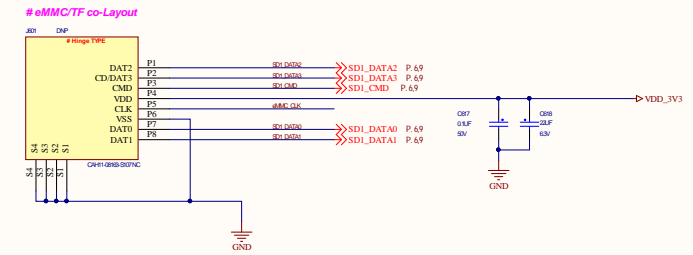
i.MX8M MISC

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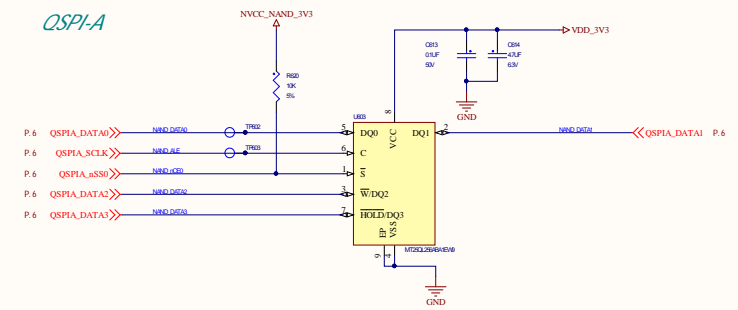
eMMC 5.0 Footprint



Hinge Type MicroSD



QSPI-A



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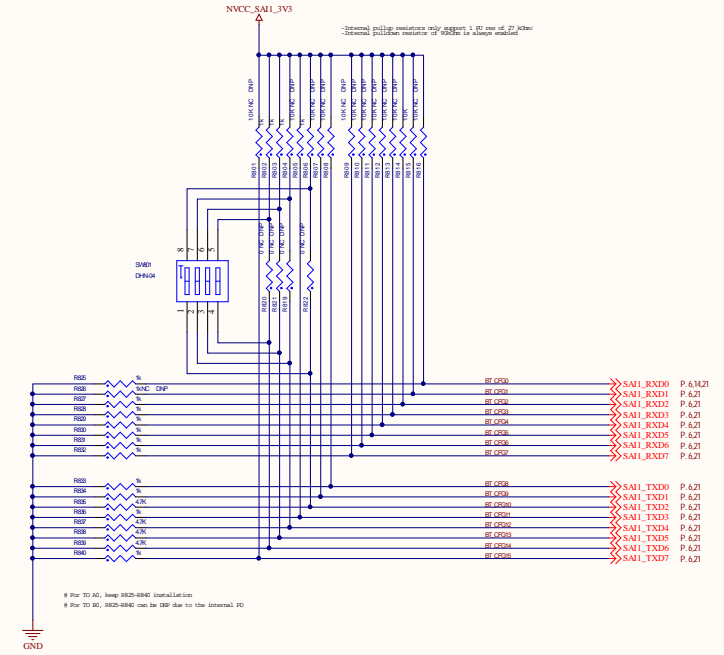
Boot ROM Fuse

Default: eMMC BOOT, CSPI boot is not supported by ROM

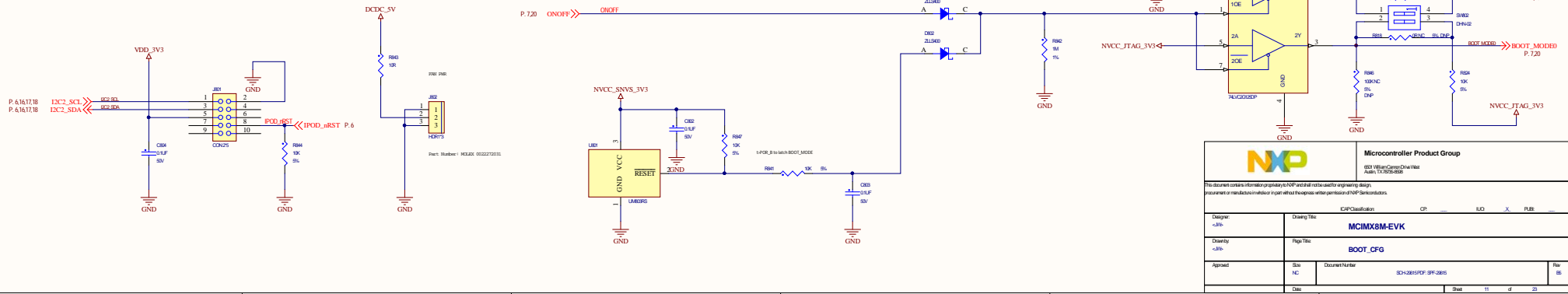
Address	7	6	5	4	3	2	1	0	
0x470[15:8]	BOOT_CFG[15]	BOOT_CFG[14]	BOOT_CFG[13]	BOOT_CFG[12]	BOOT_CFG[11]	BOOT_CFG[10]	BOOT_CFG[9]	BOOT_CFG[8]	
0x470[15:8]	Inhibit Loop (Disable USE only) 0 - Disable 1 - Enable	001 - SD/eSD	010 - MMC/eMMC	011 - NAND	100 - CSPI	110 - SPI NOR	Port Select: 00 - eSDHC1 01 - eSDHC2	Power Cycle Enable: '0' - No power cycle '1' - Enabled via	SD Loopback Clock Source Sel. (For SDR50 and SDR104 only) '0' - through SD pad '1' - direct
0x470[15:8]		00 - 128	01 - 64	10 - 32	11 - 256	Page1 In Block: 00 - 3 01 - 4 10 - 4 11 - 5	SDR SDR: "000" - Default "001-111"	Hand_Raw_address1_bytes: 00 - 3 01 - 2 10 - 4 11 - 5	
0x470[15:8]		0 - QuadSPI	1 - Reserved	0 - QuadSPI	1 - Reserved	0 - QuadSPI	1 - Reserved	0 - 3 bytes (24-bit)	1 - 2 bytes (16-bit)
0x470[15:8]		0 - Regular	1 - Fast Boot	0 - Regular	1 - Fast Boot	0 - Regular	1 - Fast Boot	0 - 3.3V	1 - 1.8V
0x470[15:8]		0 - Regular	1 - Fast Boot	0 - Regular	1 - Fast Boot	0 - Regular	1 - Fast Boot	0 - 3.3V	1 - 1.8V
0x470[15:8]	Others - Reserved for future use								
0x470[7:0]	BOOT_CFG[7]	BOOT_CFG[6]	BOOT_CFG[5]	BOOT_CFG[4]	BOOT_CFG[3]	BOOT_CFG[2]	BOOT_CFG[1]	BOOT_CFG[0]	
SD/eSD	Fast Boot: 0 - Regular 1 - Fast Boot	Reserved	Reserved	Bus Width: 0 - 1-bit 1 - 4-bit	Speed: 000 - Normal/SDR12 001 - High/SDR25 010 - SDR50 011 - SDR104 101 - Reserved for DDR50 Others - Reserved	Reserved	Reserved	Reserved	
MMC/eMMC		Bus Width: 000 - 1-bit 001 - 4-bit 010 - 8-bit 101 - 4-bit DDR (MMC 4.0) 110 - 8-bit DDR (MMC 4.0) Else - reserved.	Speed: 000 - Normal 001 - High 10 - Reserved for HS200 11 - Reserved	USDHCI1 IO VOLTAGE SELECTION: 0 - 3.3V 1 - 1.8V	USDHCI2 IO VOLTAGE SELECTION: 0 - 3.3V 1 - 1.8V				
NAND	BT_TOGGLEMODE	BOOT_SEARCH_COUNT: 00 - 2 01 - 2 10 - 4 11 - 8	Toggle Mode 33MHz Preamble Delay, Read Latency: '000' - 16 GPMMCLK cycles '001' - 1 GPMMCLK cycles '010' - 2 GPMMCLK cycles '011' - 3 GPMMCLK cycles '100' - 4 GPMMCLK cycles '101' - 5 GPMMCLK cycles '110' - 6 GPMMCLK cycles '111' - 7 GPMMCLK cycles '1111' - 15 GPMMCLK cycles					Reserved	
CSPI	HSPHS: Half Speed Phase Selection 0: select sampling at non-inverted clock 1: select sampling at inverted clock	HSDDL: Half Speed Delay selection 0: one clock delay 1: two clock delay	FSPHS: Full Speed Phase Selection 0: select sampling at non-inverted clock 1: select sampling at inverted clock	FSDDL: Full Speed Delay selection 0: one clock delay 1: two clock delay	Reserved	Reserved	Reserved	Reserved	
SPI NOR	CS select (SPI only): 00 - CS#0 (default) 01 - CS#1 10 - CS#2 11 - CS#3	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	

BMODE[1:0]	BOOT TYPE
00	Boot From Fuses
01	Serial Downloader
10	Internal Boot (Development)
11	Reserved

Boot Device: eMMC/MicroSD



Item	Power Mode	ONOFF	RES	CE	DIP SW	BA1	BA0	Note	Description
1	Startup Power Up	0 (By default)	L	H	1-4: OFF 2-3: ON	0	1	Serial Downloader	Item 1/2 for system development
2	Startup Power Up	1 (By default)	L	L	1-4: ON 2-3: OFF	0	1	Serial Downloader	Item 2/2 for system development
3	Startup Power Up	0 (By default)	L	L	1-4: ON 2-3: OFF	0	0	Serial Downloader	Normal power-up function
4	After Power Up	0 (By default)	H	H	/	/	/	Power key event	
5	After Power Up	1 (By default)	H	H	/	/	/	System power down	
6	After Power Up	0 (By default)	H	H	/	/	/		



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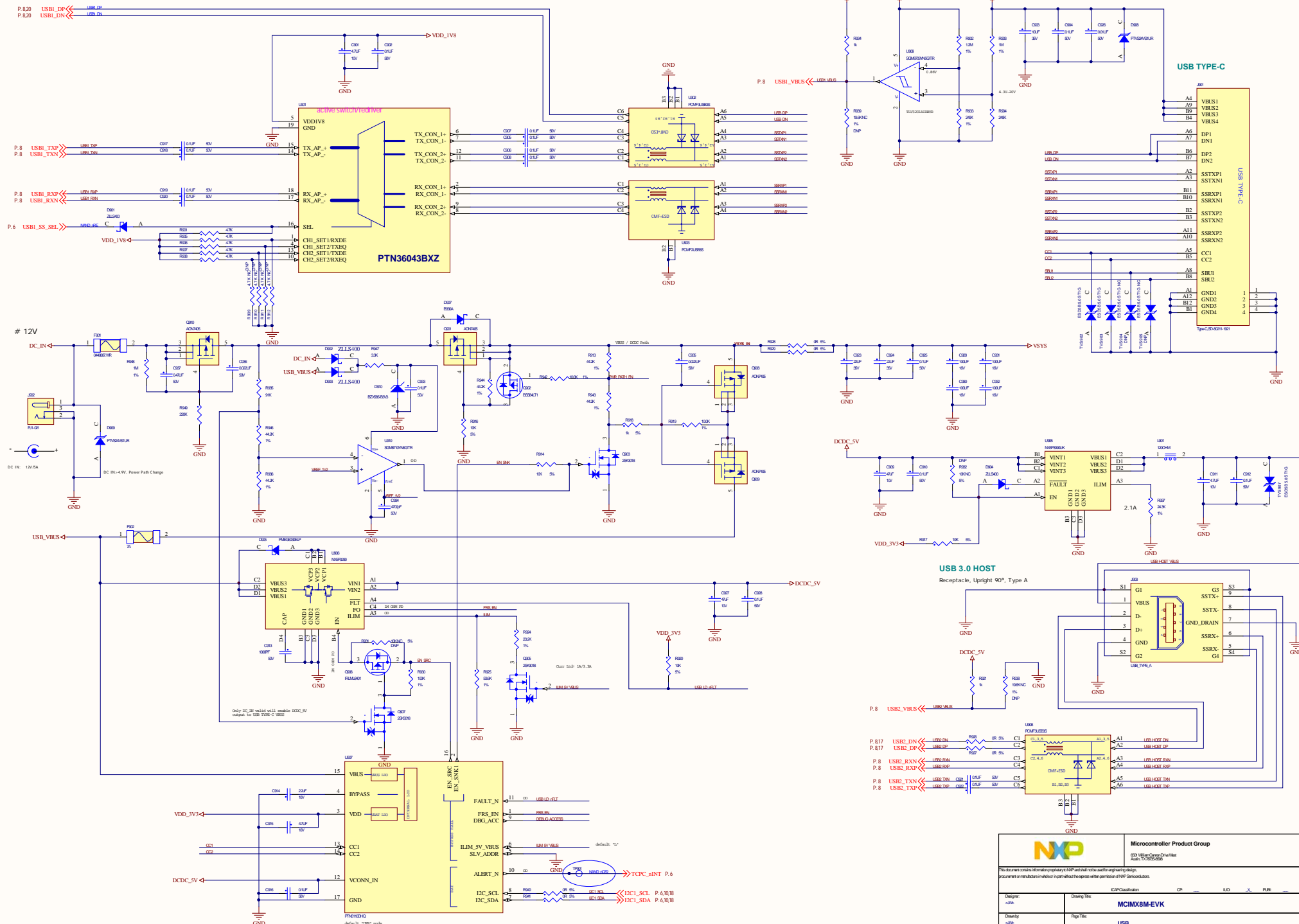
MCIMX8M-EVK

BOOT_CFG

Doc ID: 62585

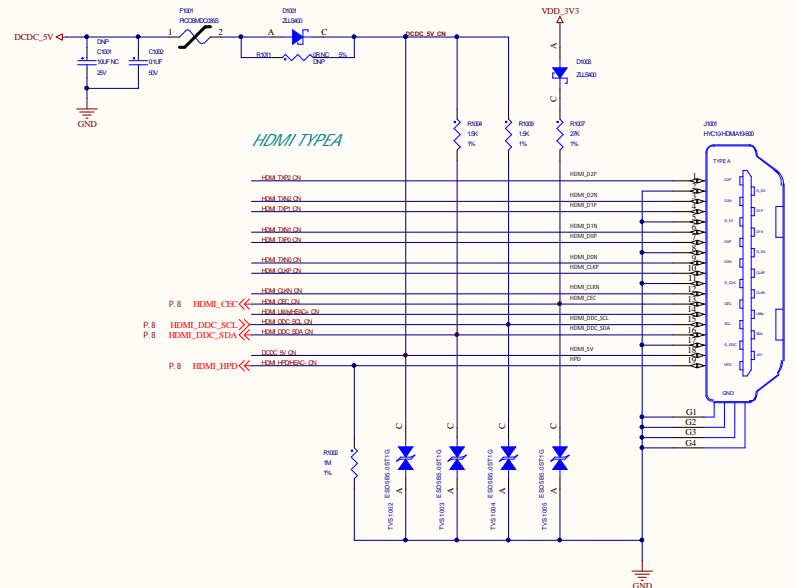
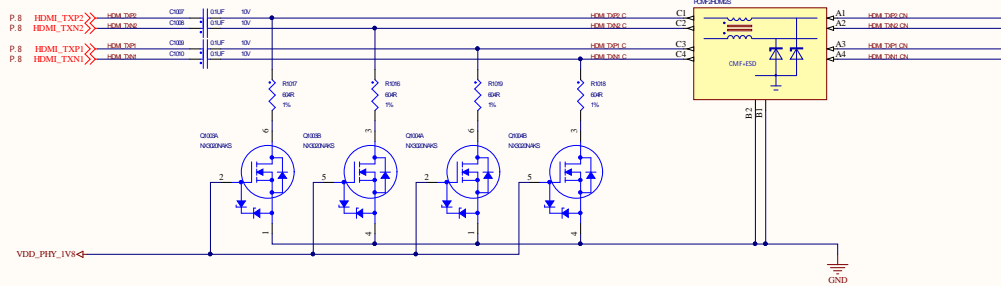
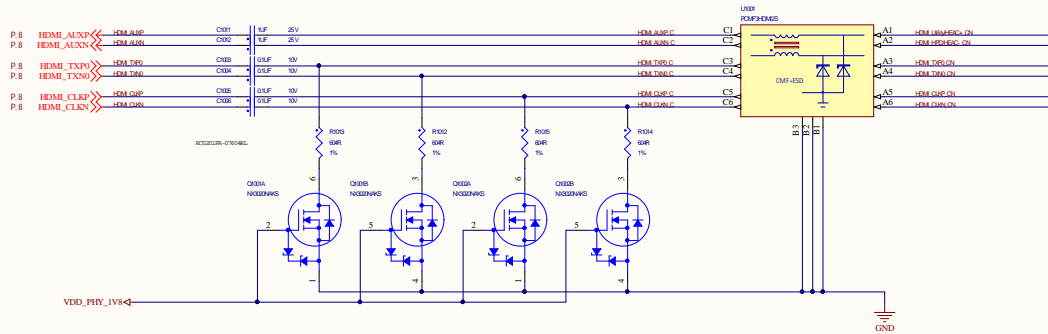
Rev: 1.0

USB3.0/2.0 TYPE-C/HOST



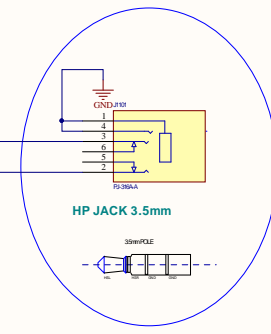
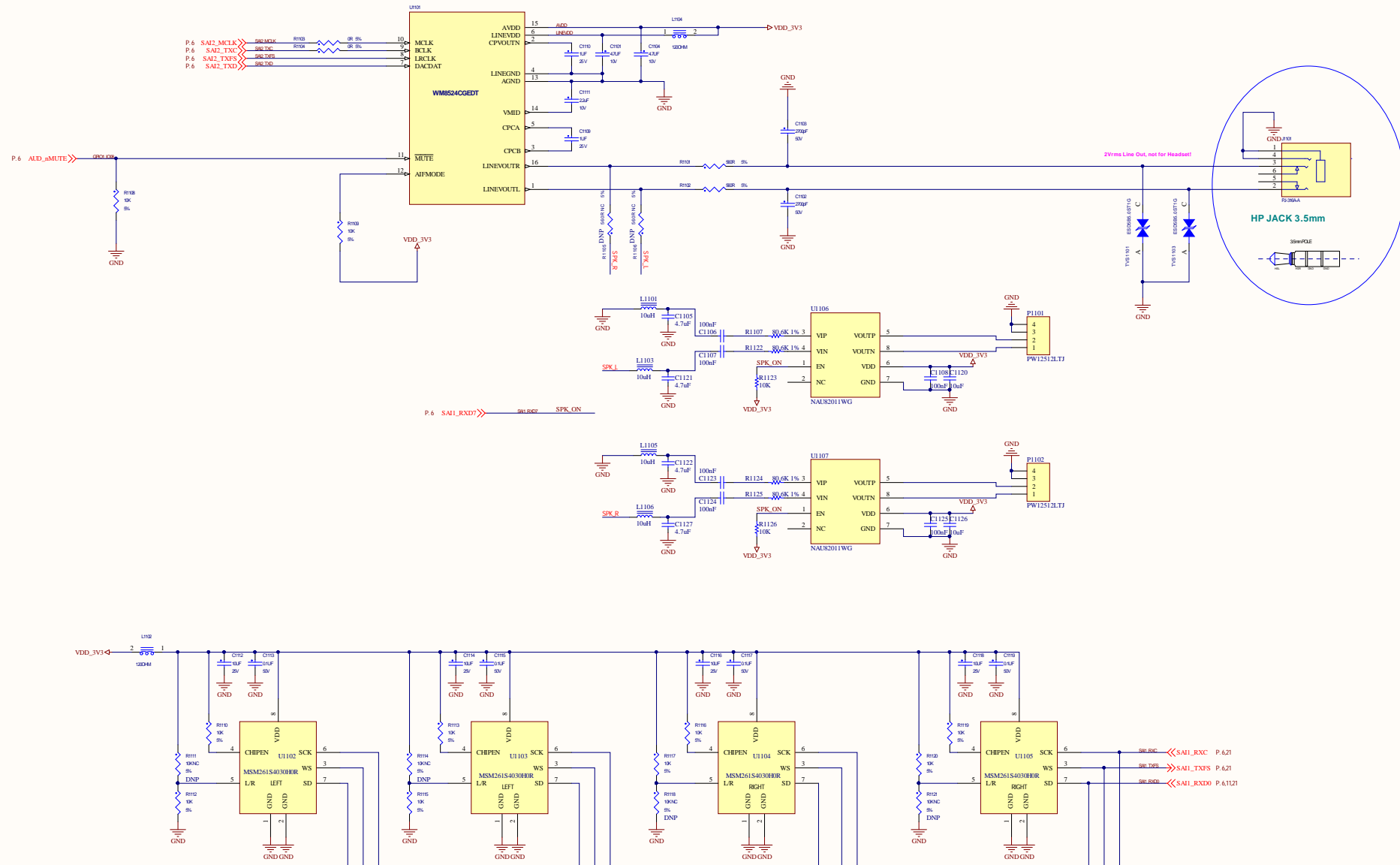
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Designer: -a3-		Page Title: USB	
Approved:		Doc. Number: ICH328155F01-BF-2015	
Date:		Rev: 01	

HDMI data EMI/ESD



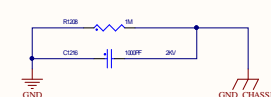
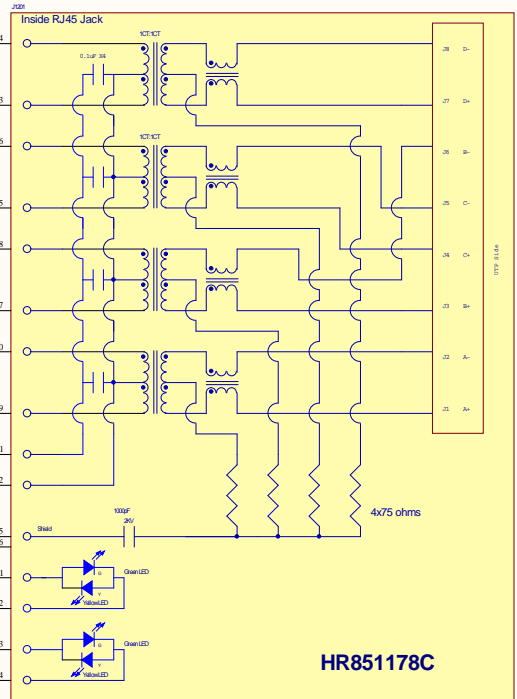
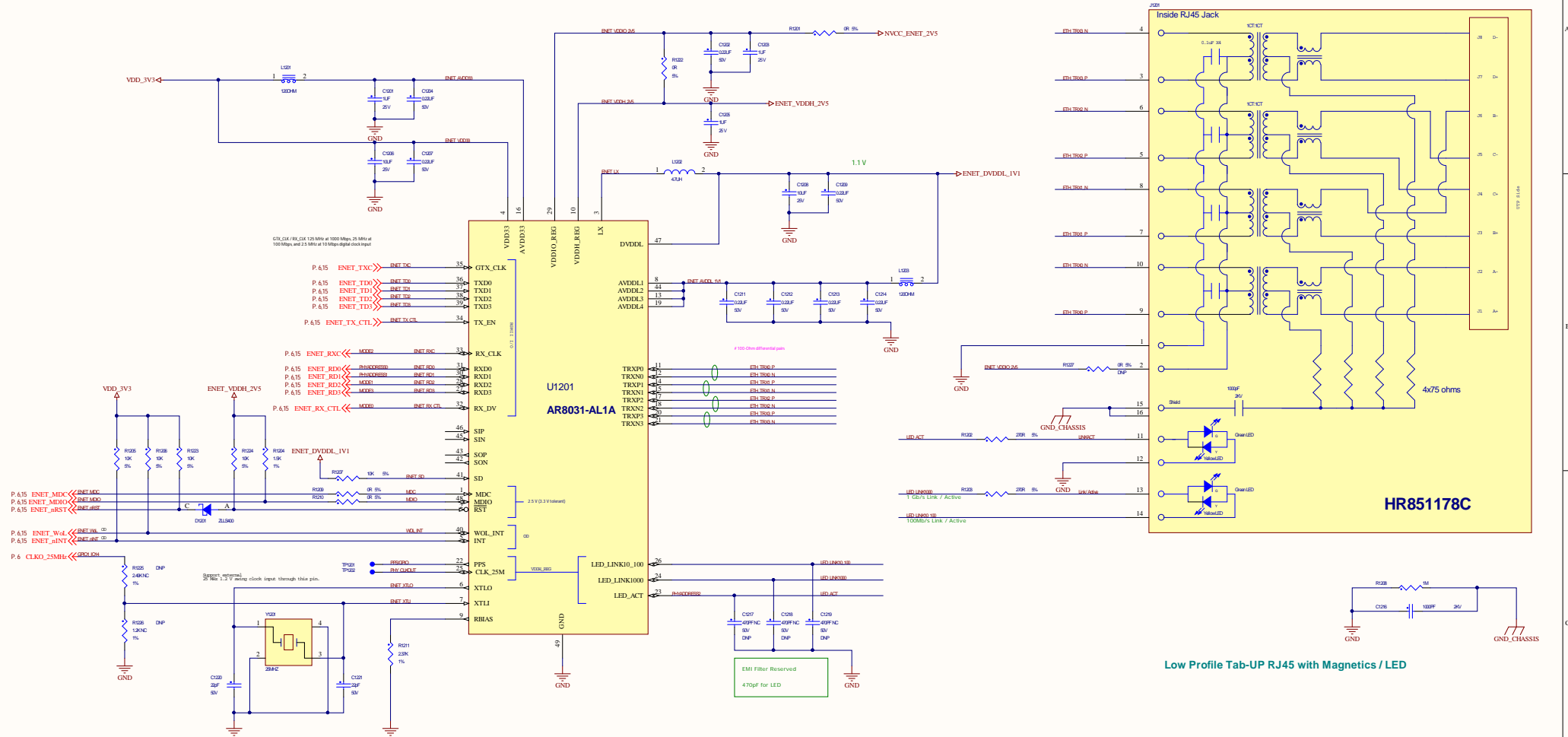
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Approved:	Size:	Document Number: 624328155DF-08F-2005	Rev: 01
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24-bit 192kHz Stereo DAC 2Vrms Line Out



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Approved	Rev	Document Number IC4138155DF-01F-2015	File 01
Date		Sheet	14 of 25

RGMII 10/100/1000 Ethernet

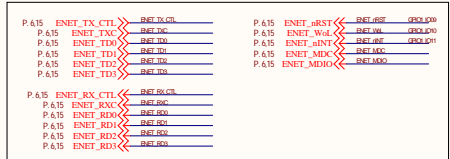
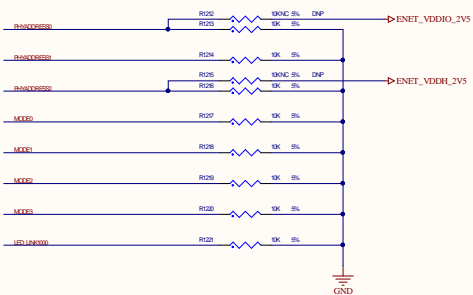


Low Profile Tab-UP RJ45 with Magnetics / LED

Power-on Strapping Pins

PHY PIN	PHY CFG	Default	Definition
RXD0	PHYADDRESS0	0	LED_ACT and RST02 set the laser through this physical address. The upper two bits of the physical address are set to the default "00".
RXD1	PHYADDRESS1	0	
LED_ACT	PHYADDRESS2	1	
RX_DIV	MODE0	0	0000 1000 Base 1 (1000)
RXD2	MODE1	0	0001 1000 Base 1000 (100)
RX_CLK	MODE2	0	0100 1000 Base 1000 (100)
RXD3	MODE3	0	0000 1000 Base 1000 (100)
LED_LINK1000	INT_SELECT	1	0 INT 1 GPHY

Power-on Strapping Pins CFG



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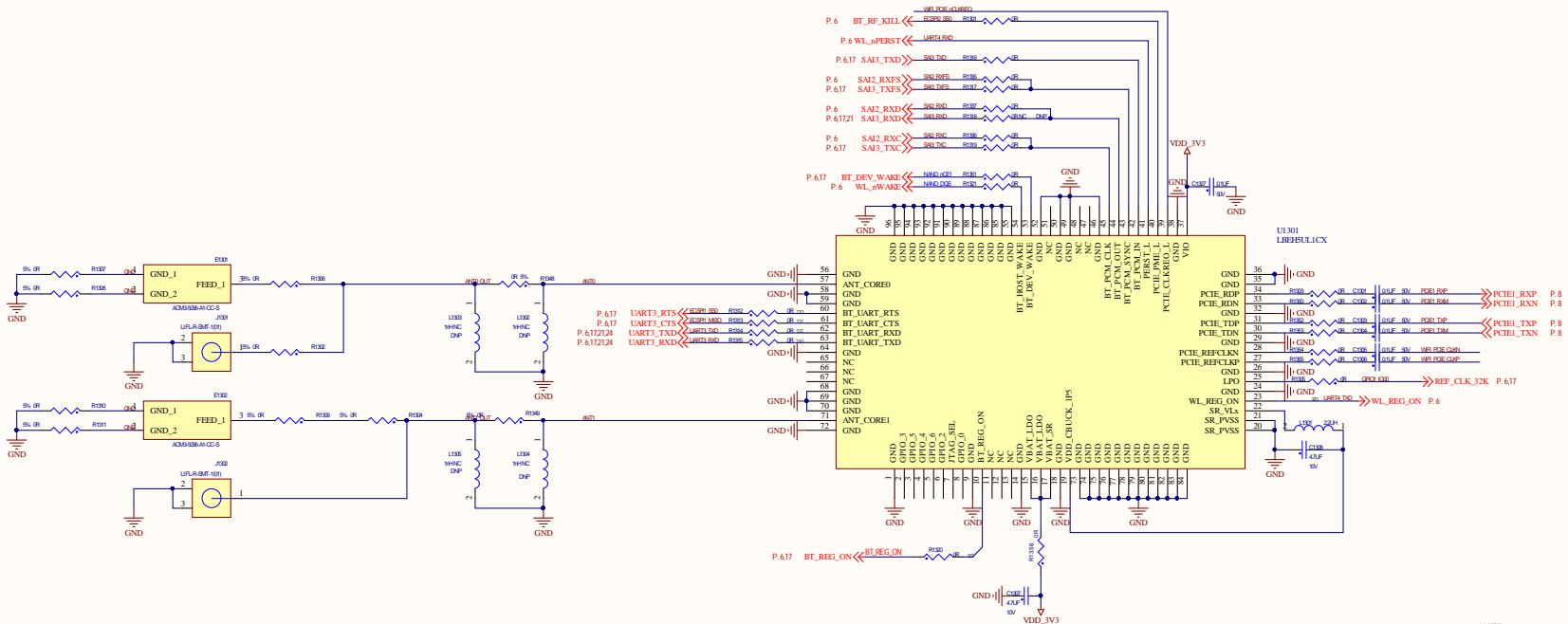
68K V850 Core/PowerPC
Part Number: MCMX8M-EVK

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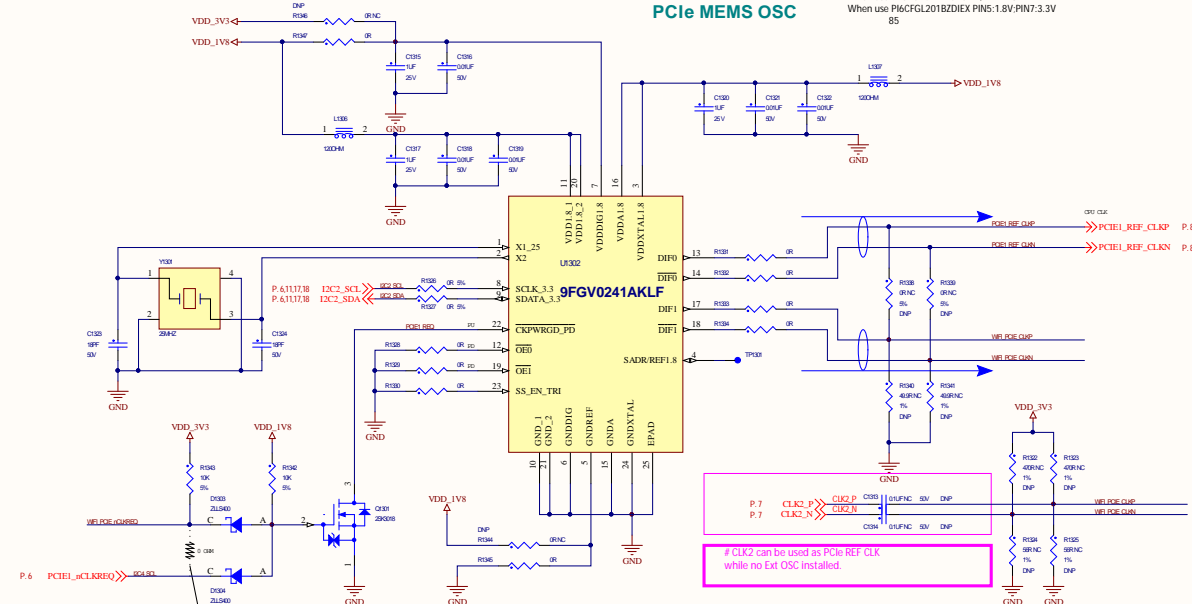
CAP Classification: CP ILO X PLB

Designer: -a3b	Drawing Title: MCMX8M-EVK	Date: _____	Rev: 01
Quantity: -a3b	Page Title: Ethernet	Document Number: ICH328155DF-01F-2005	Date: _____

WiFi/BT



PCIe MEMS OSC



NOTE:
This component share PCB package
When use 9FGV0241 PINS: GND:PIN7:1.8V
When use P16CFG1201BZDIEX PINS:1.8V:PIN7:3.3V
85

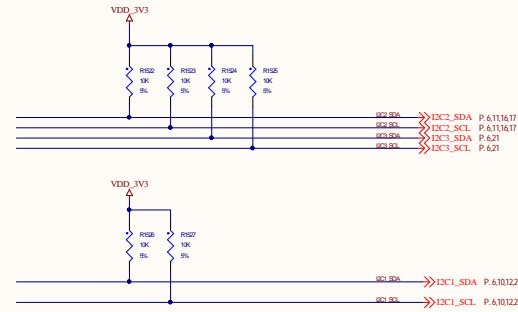
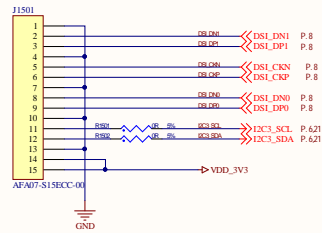
P.7 CLK2_P >> CLK2_P
P.7 CLK2_N >> CLK2_N

If CLK2 can be used as PCIe REF_CLK while no Ext OSC installed.

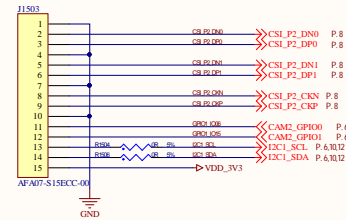
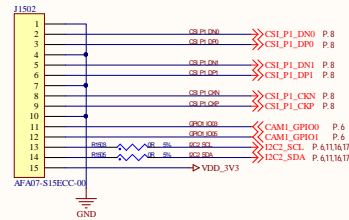
To support P16CL1.1, the data pin directional sense from CLKREF must be connected on both the Upstream and Downstream Ports of the Link, please refer to the U68501-1055.

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Designer: 		Page Title: WiFi/BT	
Approved: 		Document Number: IC4328155DF-BF-2005	
Date: 		Rev: 	

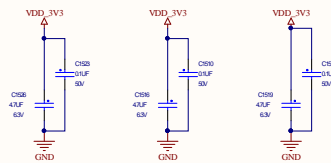
DSI LCD IF / TS



Camera Interface

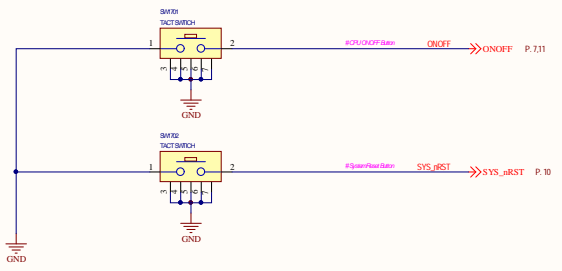
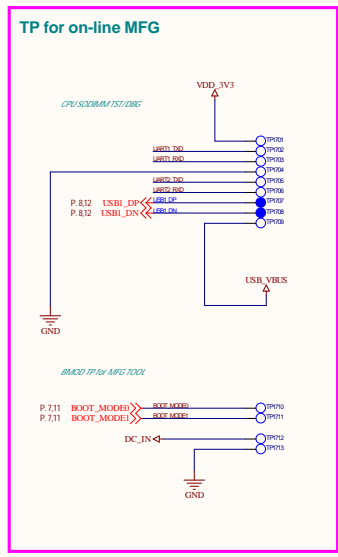
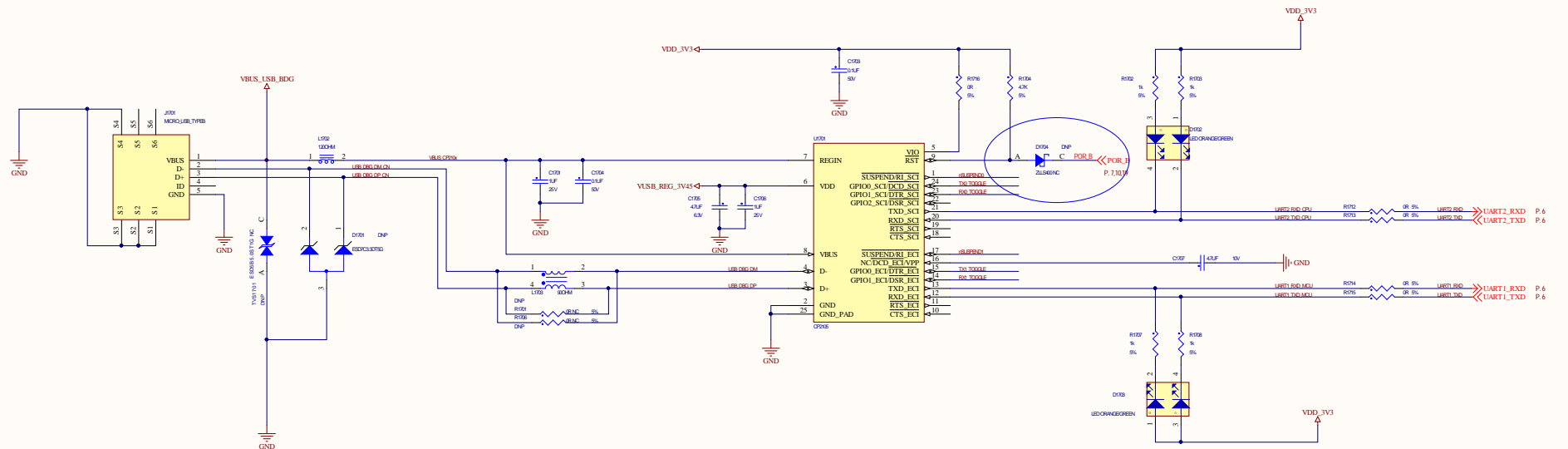


NOTE: If Dual Camera worked at the same time with the same sensor, I2C need to be different port to aviode I2C ADDR conflict !!!



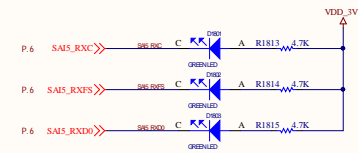
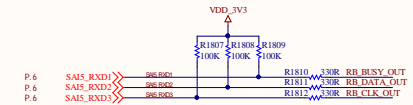
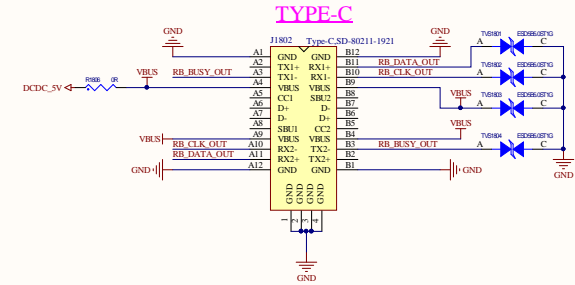
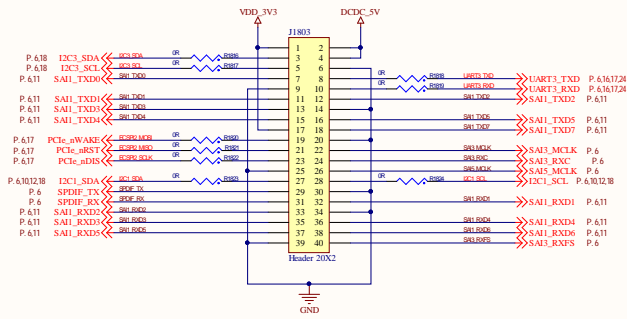
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Designer		Page Title	
-s3s-		MPIDSWCSI	
Approved		Doc. Number	Rev.
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UART-USB DBG

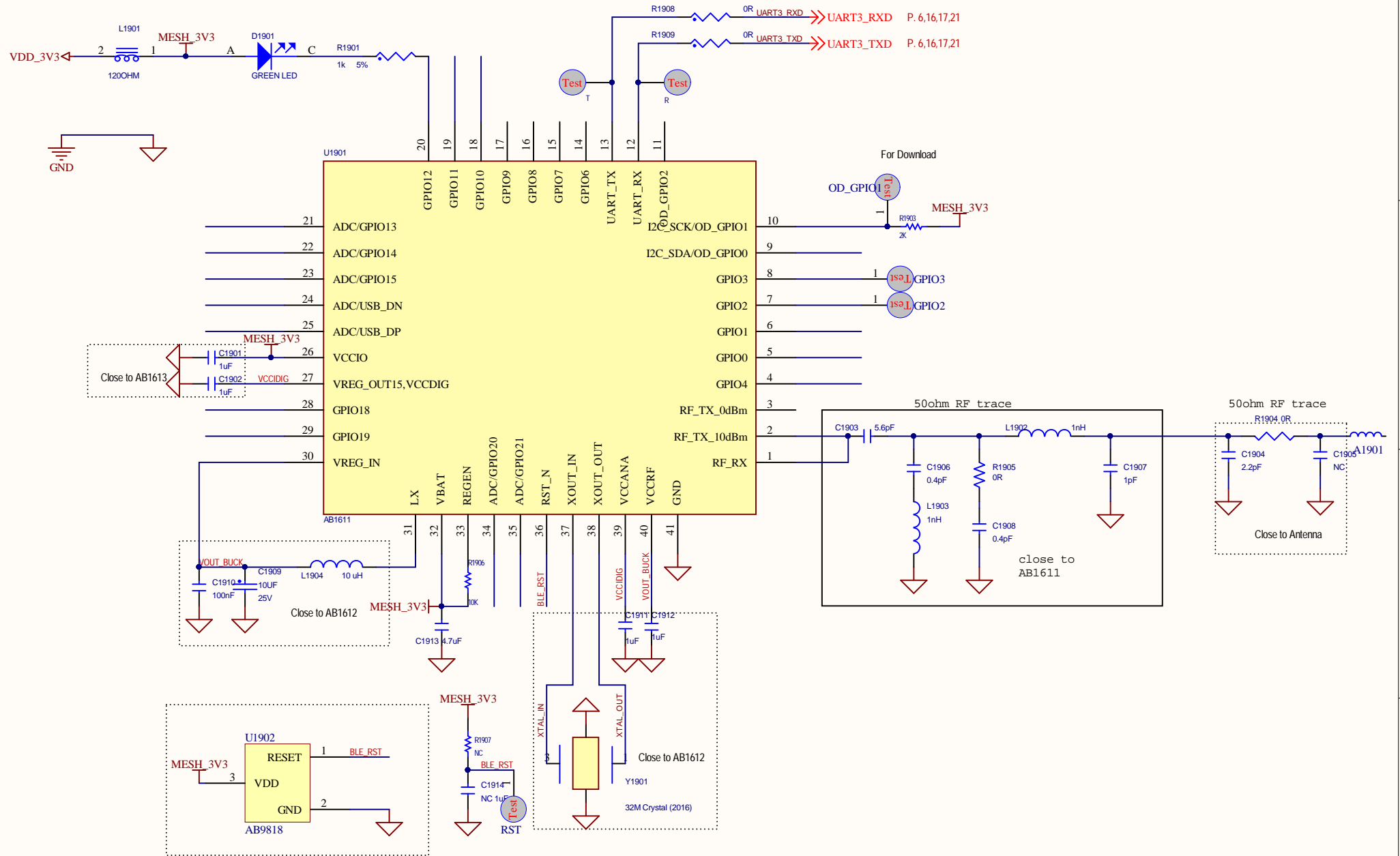


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Designer	Drawing Title	MCIMX8M-EVK	
Designer	Page Title	Debug UART	
Approved	Rev	Document Number	File
	Rev	IC4328155DF: BF-2895	BF
Date	Date	20	23


EXP CN



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Designer		Drawing Title		CP	
-a-30		MCIMX8M-EVK		ILO X PLE	
Designer		Page Title			
-a-30		Expansion CN			
Approved		Rev	Document Number	ICM138155DF-01F-2015	File
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NOTE:

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Designer -s-af-	Drawing Title MCIMX8M-EVK		
Designer -s-af-	Page Title NOTE		
Approved	Size A4	Document Number SCH32815PDF-DF-2005	File E
Date	Date		22 of 23

i.MX8M IOMUX

NAME	Default	ALTO	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	ALT10	ALT11	ALT12	ALT13	ALT14	ALT15	ALT16	ALT17	ALT18	ALT19	ALT20	ALT21	ALT22	ALT23	ALT24	ALT25	ALT26	ALT27	ALT28	ALT29	ALT30	ALT31	ALT32	ALT33	ALT34	ALT35	ALT36	ALT37	ALT38	ALT39	ALT40	ALT41	ALT42	ALT43	ALT44	ALT45	ALT46	ALT47	ALT48	ALT49	ALT50	ALT51	ALT52	ALT53	ALT54	ALT55	ALT56	ALT57	ALT58	ALT59	ALT60	ALT61	ALT62	ALT63	ALT64	ALT65	ALT66	ALT67	ALT68	ALT69	ALT70	ALT71	ALT72	ALT73	ALT74	ALT75	ALT76	ALT77	ALT78	ALT79	ALT80	ALT81	ALT82	ALT83	ALT84	ALT85	ALT86	ALT87	ALT88	ALT89	ALT90	ALT91	ALT92	ALT93	ALT94	ALT95	ALT96	ALT97	ALT98	ALT99	ALT100	ALT101	ALT102	ALT103	ALT104	ALT105	ALT106	ALT107	ALT108	ALT109	ALT110	ALT111	ALT112	ALT113	ALT114	ALT115	ALT116	ALT117	ALT118	ALT119	ALT120	ALT121	ALT122	ALT123	ALT124	ALT125	ALT126	ALT127	ALT128	ALT129	ALT130	ALT131	ALT132	ALT133	ALT134	ALT135	ALT136	ALT137	ALT138	ALT139	ALT140	ALT141	ALT142	ALT143	ALT144	ALT145	ALT146	ALT147	ALT148	ALT149	ALT150	ALT151	ALT152	ALT153	ALT154	ALT155	ALT156	ALT157	ALT158	ALT159	ALT160	ALT161	ALT162	ALT163	ALT164	ALT165	ALT166	ALT167	ALT168	ALT169	ALT170	ALT171	ALT172	ALT173	ALT174	ALT175	ALT176	ALT177	ALT178	ALT179	ALT180	ALT181	ALT182	ALT183	ALT184	ALT185	ALT186	ALT187	ALT188	ALT189	ALT190	ALT191	ALT192	ALT193	ALT194	ALT195	ALT196	ALT197	ALT198	ALT199	ALT200	ALT201	ALT202	ALT203	ALT204	ALT205	ALT206	ALT207	ALT208	ALT209	ALT210	ALT211	ALT212	ALT213	ALT214	ALT215	ALT216	ALT217	ALT218	ALT219	ALT220	ALT221	ALT222	ALT223	ALT224	ALT225	ALT226	ALT227	ALT228	ALT229	ALT230	ALT231	ALT232	ALT233	ALT234	ALT235	ALT236	ALT237	ALT238	ALT239	ALT240	ALT241	ALT242	ALT243	ALT244	ALT245	ALT246	ALT247	ALT248	ALT249	ALT250	ALT251	ALT252	ALT253	ALT254	ALT255	ALT256	ALT257	ALT258	ALT259	ALT260	ALT261	ALT262	ALT263	ALT264	ALT265	ALT266	ALT267	ALT268	ALT269	ALT270	ALT271	ALT272	ALT273	ALT274	ALT275	ALT276	ALT277	ALT278	ALT279	ALT280	ALT281	ALT282	ALT283	ALT284	ALT285	ALT286	ALT287	ALT288	ALT289	ALT290	ALT291	ALT292	ALT293	ALT294	ALT295	ALT296	ALT297	ALT298	ALT299	ALT300	ALT301	ALT302	ALT303	ALT304	ALT305	ALT306	ALT307	ALT308	ALT309	ALT310	ALT311	ALT312	ALT313	ALT314	ALT315	ALT316	ALT317	ALT318	ALT319	ALT320	ALT321	ALT322	ALT323	ALT324	ALT325	ALT326	ALT327	ALT328	ALT329	ALT330	ALT331	ALT332	ALT333	ALT334	ALT335	ALT336	ALT337	ALT338	ALT339	ALT340	ALT341	ALT342	ALT343	ALT344	ALT345	ALT346	ALT347	ALT348	ALT349	ALT350	ALT351	ALT352	ALT353	ALT354	ALT355	ALT356	ALT357	ALT358	ALT359	ALT360	ALT361	ALT362	ALT363	ALT364	ALT365	ALT366	ALT367	ALT368	ALT369	ALT370	ALT371	ALT372	ALT373	ALT374	ALT375	ALT376	ALT377	ALT378	ALT379	ALT380	ALT381	ALT382	ALT383	ALT384	ALT385	ALT386	ALT387	ALT388	ALT389	ALT390	ALT391	ALT392	ALT393	ALT394	ALT395	ALT396	ALT397	ALT398	ALT399	ALT400	ALT401	ALT402	ALT403	ALT404	ALT405	ALT406	ALT407	ALT408	ALT409	ALT410	ALT411	ALT412	ALT413	ALT414	ALT415	ALT416	ALT417	ALT418	ALT419	ALT420	ALT421	ALT422	ALT423	ALT424	ALT425	ALT426	ALT427	ALT428	ALT429	ALT430	ALT431	ALT432	ALT433	ALT434	ALT435	ALT436	ALT437	ALT438	ALT439	ALT440	ALT441	ALT442	ALT443	ALT444	ALT445	ALT446	ALT447	ALT448	ALT449	ALT450	ALT451	ALT452	ALT453	ALT454	ALT455	ALT456	ALT457	ALT458	ALT459	ALT460	ALT461	ALT462	ALT463	ALT464	ALT465	ALT466	ALT467	ALT468	ALT469	ALT470	ALT471	ALT472	ALT473	ALT474	ALT475	ALT476	ALT477	ALT478	ALT479	ALT480	ALT481	ALT482	ALT483	ALT484	ALT485	ALT486	ALT487	ALT488	ALT489	ALT490	ALT491	ALT492	ALT493	ALT494	ALT495	ALT496	ALT497	ALT498	ALT499	ALT500	ALT501	ALT502	ALT503	ALT504	ALT505	ALT506	ALT507	ALT508	ALT509	ALT510	ALT511	ALT512	ALT513	ALT514	ALT515	ALT516	ALT517	ALT518	ALT519	ALT520	ALT521	ALT522	ALT523	ALT524	ALT525	ALT526	ALT527	ALT528	ALT529	ALT530	ALT531	ALT532	ALT533	ALT534	ALT535	ALT536	ALT537	ALT538	ALT539	ALT540	ALT541	ALT542	ALT543	ALT544	ALT545	ALT546	ALT547	ALT548	ALT549	ALT550	ALT551	ALT552	ALT553	ALT554	ALT555	ALT556	ALT557	ALT558	ALT559	ALT560	ALT561	ALT562	ALT563	ALT564	ALT565	ALT566	ALT567	ALT568	ALT569	ALT570	ALT571	ALT572	ALT573	ALT574	ALT575	ALT576	ALT577	ALT578	ALT579	ALT580	ALT581	ALT582	ALT583	ALT584	ALT585	ALT586	ALT587	ALT588	ALT589	ALT590	ALT591	ALT592	ALT593	ALT594	ALT595	ALT596	ALT597	ALT598	ALT599	ALT600	ALT601	ALT602	ALT603	ALT604	ALT605	ALT606	ALT607	ALT608	ALT609	ALT610	ALT611	ALT612	ALT613	ALT614	ALT615	ALT616	ALT617	ALT618	ALT619	ALT620	ALT621	ALT622	ALT623	ALT624	ALT625	ALT626	ALT627	ALT628	ALT629	ALT630	ALT631	ALT632	ALT633	ALT634	ALT635	ALT636	ALT637	ALT638	ALT639	ALT640	ALT641	ALT642	ALT643	ALT644	ALT645	ALT646	ALT647	ALT648	ALT649	ALT650	ALT651	ALT652	ALT653	ALT654	ALT655	ALT656	ALT657	ALT658	ALT659	ALT660	ALT661	ALT662	ALT663	ALT664	ALT665	ALT666	ALT667	ALT668	ALT669	ALT670	ALT671	ALT672	ALT673	ALT674	ALT675	ALT676	ALT677	ALT678	ALT679	ALT680	ALT681	ALT682	ALT683	ALT684	ALT685	ALT686	ALT687	ALT688	ALT689	ALT690	ALT691	ALT692	ALT693	ALT694	ALT695	ALT696	ALT697	ALT698	ALT699	ALT700	ALT701	ALT702	ALT703	ALT704	ALT705	ALT706	ALT707	ALT708	ALT709	ALT710	ALT711	ALT712	ALT713	ALT714	ALT715	ALT716	ALT717	ALT718	ALT719	ALT720	ALT721	ALT722	ALT723	ALT724	ALT725	ALT726	ALT727	A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PIN LIST

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 i.MX8M IOMUX
 Design: MCHM8M-EVK
 Part: IOMUX
 Rev: 1.0