Technical Note

Migrating 1Gb 48nm and 2Gb/4Gb 57nm SLC NAND Flash Memory to 34nm

Introduction

This technical note provides guidelines for migrating 1Gb 48nm and 2Gb/4Gb 57nm SLC, large-page NAND Flash memory to 34nm technology.

This technical note should be read in conjunction with the 1Gb 48nm and 2Gb/4Gb 57nm technology data sheets and the 1Gb, 2Gb, and 4Gb 34nm technology data sheets.

Features Comparison and Differences

Technology differences are shown in bold.

Table 1: Features Comparison

Feature	1Gb 48nm, 2Gb/4Gb 57nm	1Gb, 2Gb, 4Gb 34nm
Density	1Gb 2Gb 4Gb	1Gb 2Gb 4Gb
Lithography	1Gb 48nm, 2Gb/4Gb 57nm	34nm
Voltage	1.7–1.95V 2.7–3.6V	1.7–1.95V 2.7–3.6V
Bus width	x8	x8
Package type	48-pin TSOP 63-ball VFBGA	48-pin TSOP 63-ball VFBGA
Block size	128KB	128KB
Page size	2KB	2KB
Spare size	64B	64B
Planes	1 (1Gb) 2 (2Gb, 4Gb)	1 (1Gb) 2 (2Gb, 4Gb)
ECC	**1 bit per 528 bytes**	**4 bits per 528 bytes or on-die ECC**
Valid blocks	1Gb: 1004 (MIN) 1024 (MAX) 2Gb: 2008 (MIN) 2048 (MAX) 4Gb: 4016 (MIN) 4096 (MAX)	1Gb: 1004 (MIN) 1024 (MAX) 2Gb: 2008 (MIN) 2048 (MAX) 4Gb: 4016 (MIN) 4096 (MAX)

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Table 1: Features Comparison (Continued)

Feature	1Gb 48nm, 2Gb/4Gb 57nm	1Gb, 2Gb, 4Gb 34nm
NOP	4	4
ONFI	1.0	1.0
PROGRAM/ERASE cycles	100,000	100,000
Data retention	10 years	10 years
Vendor ID/ Manufacturer code	**20h**	**2Ch**
$^{t}RC/^{t}WC$	**25ns (3V), 45ns (1.8V)**	**20ns (3V), 25ns (1.8V)**
^{t}R[1]	25µs	25µs
$^{t}PROG$	200µs (TYP)	200µs (TYP)[2]
$^{t}BERS$	**1Gb: 1500µs (TYP) 2Gb: 2000µs (TYP)**	**700µs (TYP)**
Command set	**ONFI and legacy**	**ONFI**
Unique ID	Under NDA	ONFI command (EDh) + under NDA
Block 0	**Valid at shipment 1 bit/528 bytes ECC**	**Valid at shipment 1 bit/528 bytes ECC up to 1K PROGRAM/ERASE cycles**
RESET at power-on	**Not required**	**Required**
Temperature	Commercial and industrial	Commercial and industrial
RoHS compliance	Yes	Yes

Notes: 1. With ECC enabled: ^{t}R (TYP) = 45µs, ^{t}R (MAX) = 70µs.
2. $^{t}PROG$ = 220µs (TYP) with on-die ECC enabled.

Table 2: Overview of Differences

Item	Description	Customer Action
Read ID	From 20h to 2Ch	Check new ID
ONFI RESET command at power-on	Mandatory in 34nm devices	Implement RESET command
Command set	ONFI multi-plane operations guaranteed only in 34nm devices	Use ONFI multi-plane operations
Parameter page	Different parameters between technologies	Process new value
EDC	Not available in 1Gb 48nm and all 34nm devices	Disable EDC
UNIQUE ID	Different access sequence and structure (disclosed under NDA for 48nm and 57nm devices); 34nm devices implement ONFI UNIQUE ID	Implement new UNIQUE ID usage procedure
OTP area	Different access sequence and size (disclosed under NDA for 48nm and 57 nm devices); 34nm devices use ONFI command to access	Implement new OTP usage procedure
Pin/ball connections	Some pins/balls labeled as NC in 48nm and 57nm devices are DNU or LOCK in 34nm devices	Verify that DNU or LOCK pins/balls in 34nm devices are really not connected; otherwise, change connections
ECC 4-bit on 34nm	4-bit ECC per 528 bytes or on-die ECC	Support 4-bit Use on-die ECC

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Device ID (Electronic Signature)

To process the new values, customers need to modify their software when migrating from 48nm and 57nm to 34nm devices.

Refer to the device data sheets for more information about electronic signature bytes.

Table 3: Electronic Signature

RPN	Description	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5
NAND01GR3B2C	1Gb, 1.8V, x8, 48nm	20h	A1h	00h	15h	–
MT29F1G08ABBDA	1Gb, 1.8V, x8, 34nm	2Ch	A1h	80h	15h	–
NAND01GW3B2C	1Gb, 3V, x8, 48nm	20h	F1h	00h	1Dh	–
MT29F1G08ABADA	1Gb, 3V, x8, 34nm	2Ch	F1	80h	95h	–
NAND01GR4B2C	1Gb, 1.8V, x16, 48nm	20h	B1h	00h	55h	–
MT29F1G16ABBDA	1Gb, 1.8V, x16, 34nm	2Ch	B1	80h	55h	–
NAND01GW4B2C	1Gb, 3V, x16, 48nm	20h	C1h	00h	5Dh	–
NAND02GW3B2D	2Gb, 3V, x8, 57nm	20h	DAh	10h	95h	44h
MT29F2G08ABAEA	2Gb, 3V, x8, 34nm	2Ch	DAh	90h	95h	06h
NAND02GR3B2D	2Gb, 1.8V, x8, 57nm	20h	AAh	10h	15h	44h
MT29F2G08ABBEA	2Gb, 1.8V, x8, 34nm	2Ch	AAh	90h	15h	06h
NAND04GW3B2D	4Gb, 3V, x8, 57nm	20h	DCh	10h	95h	54h
MT29F4G08ABADA	4Gb, 3V, x8, 34nm	2Ch	DCh	90h	95h	56h

Parameter Page

Different parameter page values in the 34nm technology devices are due to different manufacturers and different features. Customers need to process new parameter page values when migrating to 34nm devices.

Power-On Requirements

Power-on requirements for the 34nm devices follow ONFI specifications/procedures. See 34nm product data sheets for procedure.

Alternative Initialization Methods

Micron provides NAND_INIT on a number of discrete and MCP/PoP packages for processors that do not issue a RESET as the first command after power-up. See TN-29-34, Initializing Micron ONFI-Compliant NAND Flash, for more information. If another method is needed, contact the factory.

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Commands

The following table shows the differences between the commands. See the product data sheets for more details.

Table 4: Command Set

1Gb 48nm, 2Gb/4Gb 57nm	1Gb, 2Gb, 4Gb 34nm	Command		Notes
READ	READ PAGE	00h 30h		
RANDOM DATA OUTPUT or RANDOM DATA READ	RANDOM DATA READ	05h E0h		
CACHE READ SEQUENTIAL	READ PAGE CACHE SEQUENTIAL	31h		
Enhanced cache read - random	READ PAGE CACHE RANDOM	00h 31h		
Exit cache read	READ PAGE CACHE LAST	3Fh		
Page Program	PROGRAM PAGE	80h 10h		
N/A	PROGRAM PAGE CACHE	80h 15h		
Random Data Input	RANDOM DATA INPUT	85h		
Multi-plane Page Program 1	N/A	80h 11h 81h 10h		1
Multi-plane Page Program 2	PROGRAM PAGE TWO-PLANE	80h 11h 80h 10h		1
Copy Back Read	READ FOR INTERNAL DATA MOVE	00h 35h		
Copy Back Program	PROGRAM FOR INTERNAL DATA MOVE	85h 10h		
Multi-plane Copy Back Program 1	N/A	85h 11h 81h 10h		1
Multi-plane Copy Back Program 2	PROGRAM FOR INTERNAL DATA MOVE TWO-PLANE	85h 11h 85h 10h		1
Block Erase	ERASE BLOCK	60h D0h		
Multi-plane Block Erase 1	ERASE BLOCK TWO-PLANE	60h 60h D0h		1
Multi-plane Block Erase 2	ERASE BLOCK TWO-PLANE	60h D1h 60h D0h		1
Reset	RESET	FFh		
Read Status Register	READ STATUS	70h		
Read Status Enhanced	READ STATUS ENHANCED	78h		
Read Parameter Page	READ PARAMETER PAGE	ECh		2
Read EDC Status Register	N/A	78h		3
READ UNIQUE ID	READ UNIQUE ID	57nm	29h 16h 02h 19h	4
		48nm, 34nm	EDh	

Notes:
1. No multi-plane operations available on 1Gb 48nm or 1Gb 34nm.
2. Parameter page values are different.
3. EDC is not supported on 1Gb 48nm.
4. Command and UNIQUE ID length are different.

Error Detection Code (EDC)

An automatic EDC feature is supported on 57nm devices. As a result, an external ECC that detects copyback operation errors is not necessary. On the 57nm devices, read error occurrences are detected by checking the EDC status register.

EDC is not supported on 34nm devices. Customers migrating from 57nm to 34nm need to disable EDC by software.

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Package Compatibility

A form factor and size compatibility is guaranteed for TSOP and VFBGA packages when migrating from 48nm and 57nm to 34nm devices. The lead frame of TSOP package changes when migrating from 48nm and 57nm to 34nm. For complete lead frame information, contact factory.

Some pins/balls labeled as NC (not connected internally) in the 48nm and 57nm devices are labeled as DNU or LOCK in the 34nm devices. DNU and LOCK pins/balls should be verified as not connected in the 34nm devices.

Table 5: Differences on Pin/Ball Connections

Package	1Gb 48nm, 2Gb/4Gb 57nm	1Gb, 2Gb, 4Gb 34nm	Replacement Action or Alert
48-pin TSOP 12 x 20mm (x8 devices)	25 = NC 34 = NC 39 = NC 48 = NC 26 = NC 38 = NC 47 = NC	25 = V_{SS} 34 = V_{CC} 39 = V_{CC} 48 = V_{SS} 26 = NC 38 = DNU/NC 47 = DNU	Pins 25, 34, 39, 48 can be left as NC. The connection to either V_{SS} or V_{CC} is recommended (for ONFI compliance) but not mandatory in 34nm devices. DNU pins must be left unconnected. Pin 38 (LOCK) is disabled on 3V devices and therefore can be treated as NC even though it is bonded internally (no issues with V_{CC}/GND on this pin)
63-ball VFBGA 9 x 11mm (x8 devices)	D3 = NC F7 = NC G3 = NC G4 = NC G5 = NC G8 = NC	D3 = V_{CC} F7 = V_{SS} G3 = DNU (NAND_INIT) G4 = V_{CC} G5 = DNU (LOCK) G8 = DNU	- Balls D3, F7, G4 can be left as NC. The connection to either V_{SS} or V_{CC} is recommended (for ONFI compliance) but not mandatory in 34nm devices - G3 is bonded to NAND_INIT; therefore, it must be DNU - G5 (Lock) is enabled only on 2Gb and 4Gb 1.8V devices, NC on 1.8V 1Gb - DNU pins must be left unconnected

Error Management and Recommended ECC

34nm devices offer a 4-bit internal ECC feature. For details, see product data sheets and technical note TN-29-45, Internal ECC Feature in Mobile SLC NAND Flash Devices.

Table 6: Error Management and Recommended ECC

Description	1Gb 48nm, 2Gb/4Gb 57nm	1Gb, 2Gb, 4Gb 34nm
Minimum required ECC	1 bit per 528 bytes	4 bit per 528 bytes

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Timings

Refer to product data sheets for the most current specification values.

Table 7: AC Characteristics

Symbol	Parameter		1Gb 48nm	2Gb/4Gb 57nm	1Gb 34nm	2Gb/4Gb 34nm	Unit
^{t}PROG	Program time	Typ	200	200	200[1]	200[1]	µs
		Max	700	700	600	600	
	Multi-plane program time[2]	Typ	N/A	200	N/A	200[1]	µs
		Max	N/A	700	N/A	600	
^{t}BERS	Erase busy time	Typ	2	1.5	0.7	0.7	ms
		Max	3	2	3	3	
^{t}IPBSY/ ^{t}DBSY	Multi-plane program busy time[2]	Typ	N/A	0.5	N/A	0.5	µs
		Max	N/A	1	N/A	1	
^{t}IEBSY/ ^{t}DBSY	Multi-plane erase busy time[2]	Typ	N/A	0.5	N/A	0.5	µs
		Max	N/A	1	N/A	1	
^{t}RCBSY	Cache read busy time	Typ	3	3	3	3	µs
		Max	25	25	25	25	
^{t}CBSY	Cache program busy time	Typ	N/A	N/A	3	3	µs
		Max	N/A	N/A	600	600	

Notes: 1. 220µs with ECC enabled.
2. Multi-plane operations are not available on 1Gb 48nm and 1Gb 34nm.

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Table 8: DC Characteristics

Symbol	Parameter		1Gb 48nm, 2Gb/4Gb 57nm		1Gb, 2Gb, 4Gb 34nm		Unit
			1.8V	3V	1.8V	3V	
I_{DD1}	Operating current (sequential read, program, erase)	Typ	10	15	13[2]	25	mA
I_{DD2}, I_{DD3}					10		
I_{CC1}, I_{CC2}, I_{CC3}		Max	20	30	20	35	
I_{DD4}	Standby current (TTL)	Max	1	1	1	1	mA
I_{SB1}							
I_{DD5}	Standby current (CMOS)	Typ	10	10	10	10	µA
I_{SB2}		Max	50	50	50	50	
I_{LI}, I_{LO}	Input/output leakage current	Max	±10	±10	±10	±10	µA
V_{IH}	Input high voltage	Min	0.8 x VCC	0.8 x VCC	0.8 x VCC	0.8 x VCC	V
		Max	VCC + 0.3V	VCC + 0.3V	VCC + 0.3V	VCC + 0.3V	
V_{IL}	Input low voltage	Min	-0.3V	-0.3V	-0.3V	-0.3V	V
		Max	0.2 x VCC	0.2 x VCC	0.2 x VCC	0.2 x VCC	
V_{0H}	Output high voltage level	Min	VCC - 0.1	2.4	VCC - 0.1	0.67 x VCC1	V
V_{0L}	Output low voltage level	Max	0.4	0.4	0.4	0.4	V
I_{OL}	Output low current	Min	3	8	3	8	mA
		Typ				10	
		Max	4	10	4		
V_{LKO}	Supply voltage – erase and program lockout	Max	1.1	1.8			V

Notes:
1. If V_{CC} = 2.7V, V_{0H} = 1.8V.
2. $I_{DD}1$ Changed from 10mA to 13mA; no change for $I_{DD}2$ or $I_{DD}3$.

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Table 9: AC Characteristics for Command, Address, Data Input

Symbol	Parameter		1Gb 48nm, 2Gb/4Gb 57nm		1Gb, 2Gb, 4Gb 34nm		Unit
			1.8V	3V	1.8V	3V	
^{t}ALS	ALE setup time	Min	**25**	**12**	**10**	**10**	ns
^{t}CLS	CLE setup time	Min	**25**	**12**	**10**	**10**	ns
^{t}DS	Data setup time	Min	**20**	**12**	**10**	**7**	ns
^{t}CS	CE# setup time	Min	**35**	**20**	**20**	**15**	ns
^{t}ALH, ^{t}CLH, ^{t}DH, ^{t}CH	ALE, CLE, data, CE# hold time	Min	**10**	5	**5**	5	ns
^{t}WH	WE# HIGH hold time	Min	**15**	**10**	**10**	**7**	ns
^{t}WP	WE# pulse width	Min	**25**	12	12	12	ns
^{t}WC	WRITE cycle time	Min	**45**	**25**	**25**	**20**	ns
^{t}AR	ALE LOW to RE LOW	Min	10	10	10	10	ns
^{t}RR	RB# HIGH to RE LOW	Min	20	20	20	20	ns
^{t}R	Read busy time	Max	25	25	25	25	µs
^{t}RST	Reset busy time during ready	Max	5	5	5	5	µs
	Reset busy time during read	Max	5	5	5	5	µs
	Reset busy time during program	Max	10	10	10	10	µs
	Reset busy time during erase	Max	500	500	500	500	µs
^{t}CLR	CLE LOW to RE LOW	Min	10	10	10	10	ns
^{t}IR	Data High-Z to RE LOW	Min	0	0	0	0	ns
^{t}CHZ	CE HIGH to output High-Z	Max	**30**	**30**	**50**	**50**	ns
^{t}CSD	CE HIGH to ALE/CLE “Don’t Care”	Min	**10**	10			ns
^{t}RHZ	RE HIGH to Output High-Z	Max	**100**	100	**65**	100	ns
^{t}CEA	CE LOW to Output valid	Max	**45**	25	**25**	25	ns
^{t}REH	RE HIGH to RE LOW	Min	**15**	**10**	**10**	**7**	ns
^{t}COH, ^{t}RHOH	CE/RE HIGH to output hold	Min	15	15	15	15	ns
^{t}RLOH	RE LOW to output hold (EDO mode)	Min	**5**	5	**3**	5	ns
^{t}RP	RE LOW to RE HIGH	Min	**25**	12	**12**	**10**	ns
^{t}RC	RE LOW to RE LOW	Min	**45**	**25**	**25**	20	ns
^{t}REA	RE LOW to output valid	Max	**30**	20	**22**	16	ns
tR	WE HIGH to RB# HIGH (tR)	Max	25	25	25	25[1]	ns
^{t}WB	WE HIGH to RB# LOW	Max	100	100	100	100	ns
^{t}WHR	WE HIGH to RE LOW	Min	**60**	60	**80**	60	ns
^{t}RHW	RE HIGH to WE LOW	Min	100	100	100	100	ns
^{t}ADL	Last address latched to data loading during program	Min	**100**	70	–	–	ns
^{t}WW	Write protection time	Min	100	100	100	100	ns

Notes: 1. With ECC enabled, ^{t}R (TYP) = 45µs; ^{t}R (MAX) = 70µs.

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Revision History

Rev. C 9/10

- Updated values in Timings
- Updated I_{DD1} value in DC Characteristics Table

Rev. B 7/10

- Changed title from Migrating 2Gb and 4Gb SLC NAND Flash Memory from 57nm to 34nm to Migrating 1Gb 48nm and 2Gb/4Gb 57nm SLC NAND Flash Memory to 34nm.
- Added all references to 1Gb 48nm and 2Gb/4Gb 57nm.
- Added 1Gb part numbers to Table 3, “Electronic Signature,” on page 3.

Rev. A 6/10

- Initial release

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