（H2C）

TC9590XBG

Functional Specification

Revision 1.0

2018-12

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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Revision History

Revision	Date	Note
Rev 0.01	12/12/2017	Initial Release
Rev 0.02	06/26/2018	Correction (Fig 5-3, 9.4 HDMI RX input spec.)
1.0	2018-12-11	Changed header, footer and revised the cover page. Changed corporate name. Added descriptions of the trademark and the service mark. Modified section number, Table number and Figure number. Corrected typos. Modified Table 3-1. Modified tables. Added weight in section 7. Revised the last page "RESTRICTIONS ON PRODUCT USE" and added URL.

REFERENCES

1. MIPI® D-PHY℠, “MIPI_D-PHY_specification_v01-00-00, May 14, 2009"
2. MIPI® CSI-2℠, "MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2) Version 1.01 Revision Nov 2010"
3. VESA® Mobile Display Digital Interface Standard (Version 1.2, Type II)
4. I^2C bus specification, version 2.1, January 2000, Philips Semiconductor

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1. Overview

The HDMI®-RX to MIPI CSI-2-TX (TC9590XBG) is a bridge device that converts HDMI stream to MIPI CSI-2 TX for automotive application.

The current and next generation Application Processors and Baseband chips have been designed without video streaming input port except CSI-2 for Camcorder input. Smart Phone Processors are being used in several applications that required Video Input

TC9590XBG takes in HDMI input and converts to CSI-2 that looks like a Camcorder input.

TC9590XBG System Overview block diagram is shown below.

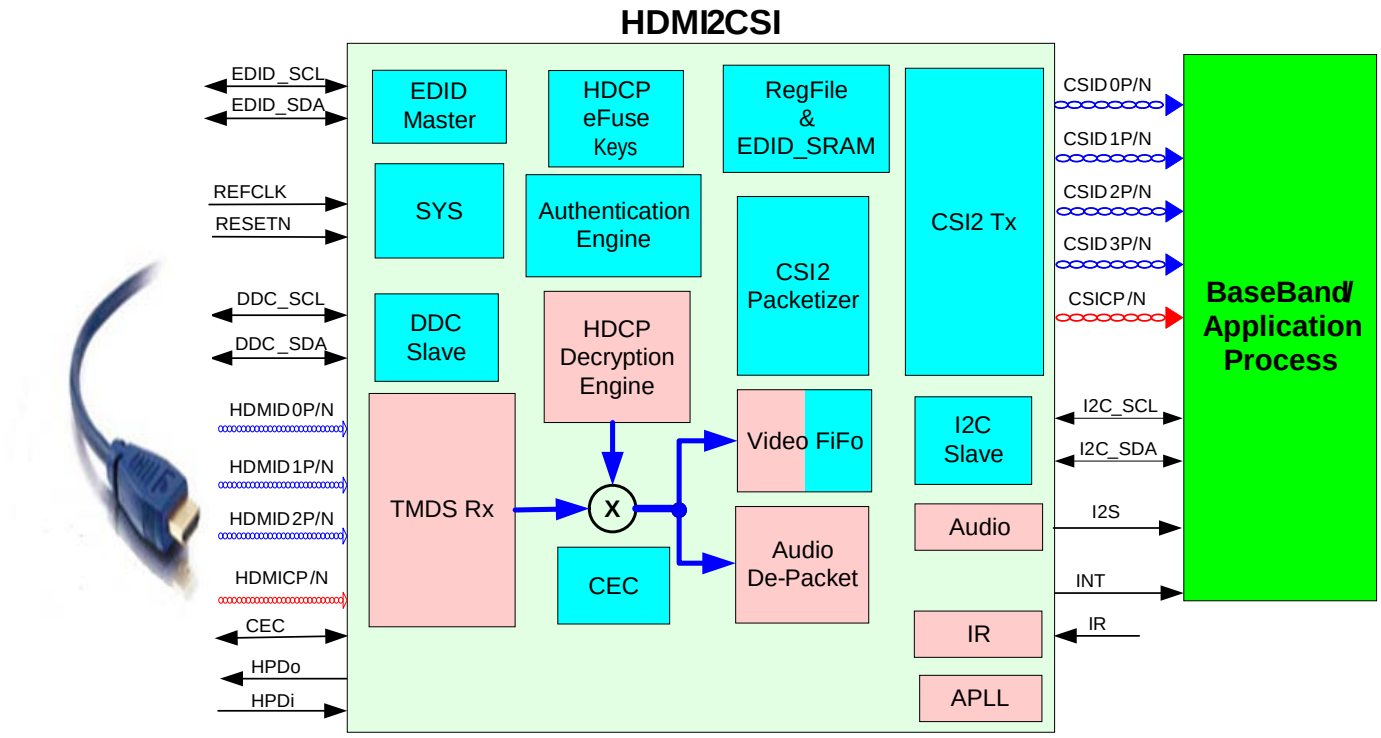


Figure 1.1 TC9590XBG System Overview

2. Features

Below are the main features supported by TC9590XBG.

HDMI-RX Interface

- ✧ HDMI 1.4
  - Video Formats Support (Up to 1080P @60fps)
    - ➢ RGB, YCbCr444: 24-bpp (bits per pixel) @60fps
    - ➢ YCbCr422 24-bpp @60fps
    - ➢ Interlaced video supported
      - ✧ Limitation: YCbCr422 16-bpp interlaced video format cannot be supported.
  - Audio Supports
    - ➢ Internal Audio PLL to track N/CTS value transmitted by the ACR packet.
  - 3D Support
  - Support HDCP (optional)
  - DDC Support
  - EDID Support
    - ➢ Release A, Revision 1 (Feb 9, 2000)
    - ➢ First 128 byte (EDID 1.3 structure)
    - ➢ First E-EDID Extension: 128 bytes of CEA Extension version 3 (specified in CEA-861-D)
    - ➢ Embedded 1K-byte SRAM (EDID_SRAM)
  - Maximum HDMI clock speed: 165 MHz
- ✧ Does not support Audio Return Path and HDMI Ethernet Channels

CSI-2 TX Interface

- ✧ MIPI CSI-2 compliant (Version 1.01 Revision 0.04 – 2 April 2009)
- ✧ Supports up to 1 Gbps per data lane
  - Video, Audio and InfoFrame data can be transmit over MIPI CSI-2
- ✧ Supports up to 4 data lanes

I^2C Slave Interface

- ✧ Support for normal (100 kHz) and fast mode (400 kHz)
- ✧ Support ultra-fast mode (2 MHz)
- ✧ Configure all TC9590XBG internal registers

Audio Output Interface

Either I2S or TDM Audio interface available (pins are multiplexed)

I2S Audio Interface

- ✧ Single data lane for stereo data
- ✧ Support Master Clock mode only
- ✧ Support 16, 18, 20 or 24-bit data (depend on HDMI input stream)
- ✧ Support Left or Right-justify with MSB first
- ✧ Support 32 bit-wide time-slot only
- ✧ Output Audio OverSampling clock (256fs)

TDM (Time Division Multiplexed) Audio Interface

- ✧ Fixed to 8 channels (depend on HDMI input stream)
- ✧ Support 32 bit-wide time slot only
- ✧ Support Master Clock mode only
- ✧ Support 16, 18, 20 or 24-bit PCM audio data word (depend on HDMI input stream)
- ✧ Output Audio Over Sampling clock (256fs)

InfraRed (IR)

- ✧ Support NEC InfraRed protocol.

System

- ✧ Internal core has two power domains (VDDC1 and VDDC2)
  - VDDC1 is always on power domain
  - VDDC2 can be shut-off during deep sleep mode

Power supply inputs

- ✧ Core and MIPI D-PHY: 1.2V
- ✧ I/O: 1.8V – 3.3V
- ✧ HDMI: 3.3V
- ✧ APLL: 3.3V/2.5V

Power Consumption during typical operations

- ✧ 720P: 0.48 W
- ✧ 1080P @30fps: 0.48 W
- ✧ 1080P @60fps: 0.54 W

		VDDC1	VDDC2	VDDIO1	VDDIO2	VDDMIPI	AVDD33	AVDD12	AVDD25	Total Power	Unit
		1.2	1.2	3.3	1.8	1.2	3.3	1.2	2.5		
720P @60Frames	Current (A)	0.0472		0	0.0009	0.0178	0.0879	0.0656	0.0128	480.47	mW
	Power (W)	0.05664		0	0.0017	0.0214	0.2901	0.0787	0.032		
1080P @60Frames	Current (A)	0.0766		0	0.0009	0.0228	0.0881	0.0829	0.0128	543.19	mW
	Power (W)	0.09192		0	0.0017	0.0274	0.2907	0.0995	0.032		
Sleep 0x0002 = 0x0001	Current (µA)	0.91		0.002	0.0430	0.0490	32.3700	0.3200	0.2	108.94	µW
	Power (µW)	1.092		0.0066	0.0774	0.0588	106.8210	0.3840	0.5		

Note:

- Attention about ESD. This product is weak against ESD. Please handle it carefully.
- TC9590XBG does not perform YCbCr <-> YUV conversion. In this document they are used interchangeably.

3. External Pins

TC9590XBG resides in BGA64 pin packages. The following table gives the signals of TC9590XBG and their function.

Table 3-1 TC9590XBG Functional Signal List

Group	Pin Name	I/O	Init. (O)	Type	Function	Voltage Supply	Note
System: Reset & Clock (4)	RESETN	I	-	Sch	System reset input, active low	VDDIO2	1.8V -3.3V
	REFCLK	I	-	N	Reference clock input (27/26 MHz or 42 MHz)	VDDIO2	1.8V -3.3V
	TEST	I	-	N	TEST mode select 0: Normal mode 1: Test mode	VDDIO2	1.8V -3.3V
	INT	O	L	N	Interrupt Output signal – active high (Level)	VDDIO2	1.8V -3.3V
CSI-2 TX (10)	CSICP	-	H	CSI-PHY	MIPI-CSI clock positive	VDD_MIPI	1.2V
	CSICN	-	H	CSI-PHY	MIPI-CSI clock negative	VDD_MIPI	1.2V
	CSID0P	-	H	CSI-PHY	MIPI-CSI Data 0 positive	VDD_MIPI	1.2V
	CSID0N	-	H	CSI-PHY	MIPI-CSI Data 0 negative	VDD_MIPI	1.2V
	CSID1P	-	H	CSI-PHY	MIPI-CSI Data 1 positive	VDD_MIPI	1.2V
	CSID1N	-	H	CSI-PHY	MIPI-CSI Data 1 negative	VDD_MIPI	1.2V
	CSID2P	-	H	CSI-PHY	MIPI-CSI Data 2 positive	VDD_MIPI	1.2V
	CSID2N	-	H	CSI-PHY	MIPI-CSI Data 2 negative	VDD_MIPI	1.2V
	CSID3P	-	H	CSI-PHY	MIPI-CSI Data 3 positive	VDD_MIPI	1.2V
	CSID3N	-	H	CSI-PHY	MIPI-CSI Data 3 negative	VDD_MIPI	1.2V
HDMI-RX (8)	HDMICP	-	-	HDMI-PHY	HDMI Clock channel positive	AVDD33	3.3V
	HDMICN	-	-	HDMI-PHY	HDMI Clock channel negative	AVDD33	3.3V
	HDMID0P	-	-	HDMI-PHY	HDMI Data 0 channel positive	AVDD33	3.3V
	HDMID0N	-	-	HDMI-PHY	HDMI Data 0 channel negative	AVDD33	3.3V
	HDMID1P	-	-	HDMI-PHY	HDMI Data 1 channel positive	AVDD33	3.3V
	HDMID1N	-	-	HDMI-PHY	HDMI Data 1 channel negative	AVDD33	3.3V
	HDMID2P	-	-	HDMI-PHY	HDMI Data 2 channel positive	AVDD33	3.3V
	HDMID2N	-	-	HDMI-PHY	HDMI Data 2 channel negative	AVDD33	3.3V
DDC (2)	DDC_SCL	IO	-	N (Note2)	DDC Slave Clock	VDDIO1	3.3V (Note1)
	DDC_SDA	IO	-	N (Note2)	DDC Slave data	VDDIO1	3.3V (Note1)
EDID (2)	EDID_SCL	IO	-	N (Note2)	EDID Master Clock	VDDIO2	1.8V -3.3V
	EDID_SDA	IO	-	N (Note2)	EDID Master Data	VDDIO2	1.8V -3.3V
CEC	CEC	IO	-	N (Note2)	CEC signal	VDDIO1	3.3V
HPD (2)	HPDI	I	-	N	Hot Plug Detect Input	VDDIO1	3.3V (Note1)
	HPDO	O	L	N	Hot Plug Detect Output	VDDIO1	3.3V
Audio (4)	A_SCK	O	L	N	I2S/TDM Bit Clock signal	VDDIO2	1.8V -3.3V
	A_WFS	O	L	N	I2S Word Clock or TDM Frame Sync signal	VDDIO2	1.8V -3.3V
	A_SD	O	L	N	I2S/TDM data signal	VDDIO2	1.8V -3.3V
	A_OSCK	O	L	N	Audio OverSampling Clock	VDDIO2	1.8V -3.3V
IR	IR	I	-	Sch	InfraRed signal	VDDIO2	1.8V -3.3V
I^2C (2)	I2C_SCL	IO	-	N (Note2)	I^2C serial clock	VDDIO2	1.8V -3.3V
	I2C_SDA	IO	-	N (Note2)	I^2C serial data	VDDIO2	1.8V -3.3V

Group	Pin Name	I/O	Init. (O)	Type	Function	Voltage Supply	Note
APLL (4)	BIASDA	O	L	-	BIAS signal Connect to AVSS through 0.1µF when not used	-	-
	DAOUT	O	H	-	Audio PLL clock Reference Output clock Please leave open when not used	-	-
	PCKIN	I	-	-	Audio PLL Reference Input clock Connect to AVSS through 0.1µF when not used	-	-
	PFIL	O	L	-	Audio PLL Low Pass Filter signal Connect to AVSS through 0.1µF when not used	-	-
POWER (12)	VDDC1, VDDC2	-	-	-	VDD for Internal Core (3)	-	1.2V
	VDDIO1	-	-	-	VDDIO1 IO power supply (1)	-	3.3V
	VDDIO2	-	-	-	VDDIO2 IO power supply (1)	-	1.8V - 3.3V
	VDD_MIPI	-	-	-	VDD for the MIPI CSI-2 (2)	-	1.2V
	AVDD12	-	-	-	HDMI Phy 1.2V power supply (2)	-	1.2V
	AVDD33	-	-	-	HDMI Phy 3.3V power supply (2)	-	3.3V
	AVDD25	-	-	-	APLL 2.5V power supply (1)	-	2.5V
Ground (10)	VSS	-	-	-	Ground	-	-
Misc (2)	REXT	-	-	-	External Reference Resistor, Please connect to AVDD33 with a 2kΩ resistor (± 1%)	-	-
	VPGM	-	-	-	eFuse program power supply, please tie to ground	-	-

Total 64 pins

Note1: These IO are 5V tolerant.
Note2: Bi-directional IO with Schmitt triggered input.

Buffer Type Abbreviation:

N: Normal IO
N_{PD}: Normal IO with weak Internal Pull-Down
N_{PU}: Normal IO with weak Internal Pull-Up
FS-SOD: Failed Safe Pseudo open-drain output, Schmitt input
FS: Failed Safe IO
Sch: Schmitt input buffer
CSI-PHY: front-end analog IO for CSI
HDMI-PHY: front-end analog IO for HDMI

3.1. TC9590XBG BGA64 Pin Count Summary

Table 3-2 BGA64 Pin Count Summary

Group Name	Pin Count	Note
SYSTEM	4	-
CSI-2 TX	12	Include Power pins
HDMI RX	13	Include Power, External Resistor pins.
DDC	2	-
EDID	2	-
CEC	1	-
Audio	4	-
I^2C	2	-
IR	1	-
HPD	2	-
APLL	5	Audio PLL – Include Power pin
POWER	6	IO, Core, eFuse
GROUND	10	IO, Core, Analog
TOTAL	**64**	-

3.2. Pin Layout

A1 REXT	A2 VSS	A3 VPGM	A4 BIASDA	A5 DAOUT	A6 PFIL	A7 CSID3N	A8 CSID3P
B1 AVDD33	B2 AVDD12	B3 INT	B4 IR	B5 AVDD25	B6 PCKIN	B7 CSID2N	B8 CSID2P
C1 HDMICP	C2 HDMICN	C3 VDDC2	C4 VSS	C5 VSS	C6 VDD_MIPI	C7 CSICN	C8 CSICP
D1 HDMID0P	D2 HDMID0N	D3 AVDD12	D4 VSS	D5 VSS	D6 VSS	D7 CSID1N	D8 CSID1P
E1 HDMID1P	E2 HDMID1N	E3 VSS	E4 VSS	E5 TEST	E6 VSS	E7 CSID0N	E8 CSID0P
F1 HDMID2P	F2 HDMID2N	F3 AVDD33	F4 VDDIO1	F5 VDDC2	F6 VDD_MIPI	F7 A_SCK	F8 A_SD
G1 CEC	G2 VDDC1	G3 DDC_SDA	G4 I2C_SDA	G5 RESETN	G6 EDID_SDA	G7 A_WFS	G8 A_OSCK
H1 HPDO	H2 HPDI	H3 DDC_SCL	H4 I2C_SCL	H5 REFCLK	H6 EDID_SCL	H7 VDDIO2	H8 VSS

Figure 3.1 TC9590XBG 64-Pin Layout (Top View)

4. Major Functional Blocks

TC9590XBG consists of the following major blocks: HDMI-RX, CSI-2-TX, CSI-2 Rx, EDID, DDC, CEC, I2S, INT and I^2C i/f.

DDC, CEC and I^2C slave controller are always enabled which is required for configure the TC9590XBG chip and to wake up TC9590XBG chip.

The following sections describe each block in detail. Addition, there is a section describes Clock generation block.

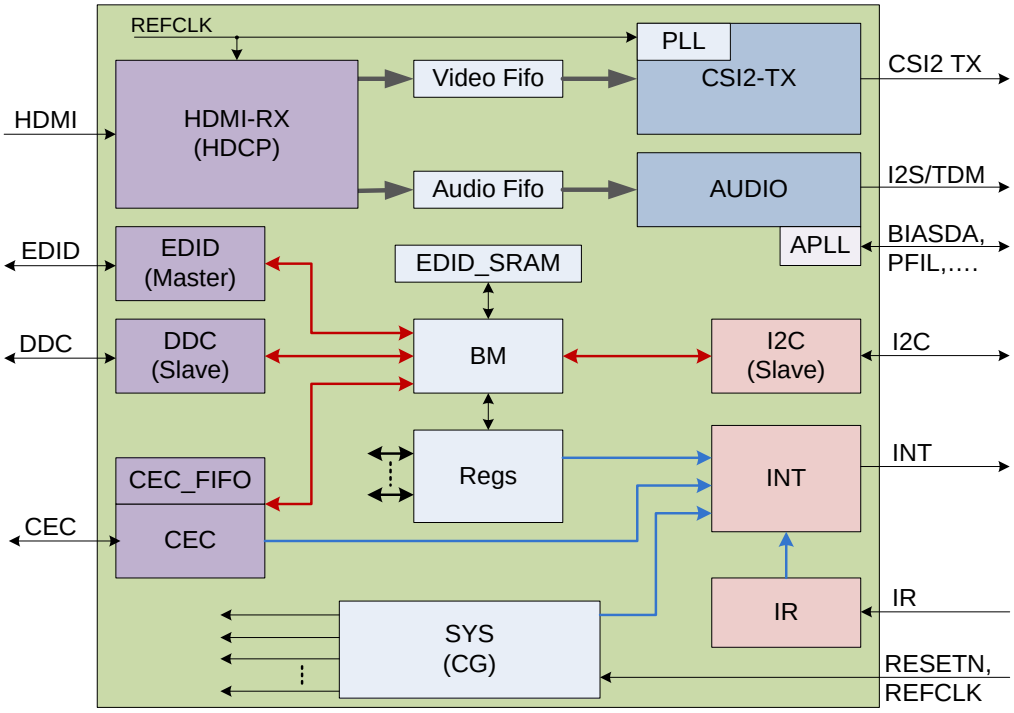


Figure 4.1 Block Diagram of TC9590XBG

4.1. HDMI-RX

Primary features

- HDMI 1.4
- Video Format support: Progressive and Interlaced
  - RGB, YCbCr444: 24-bpp @60fps
  - YCbCr422 24-bpp @60fps
  - Does not support Interlaced YCbCr422 16-bpp video
- Audio
- 3D Support
- Support HDCP (1.3)

4.1.1. 3D Support

HDMI 3D feature supports the following 3D structures.

Table 4-1 HDMI 3D Structure

Value	Meaning
0000	Frame packing
0001 ~ 0101	Reserved for future use
0110	Top-and-Bottom
0111	Reserved for future use.
1000	Side-by-Side (Half)
1001 ~ 1111	Reserved for future use

4.1.1.1. Frame Packing Structure

Block diagram below showed Frame Packing structure for progressive format:

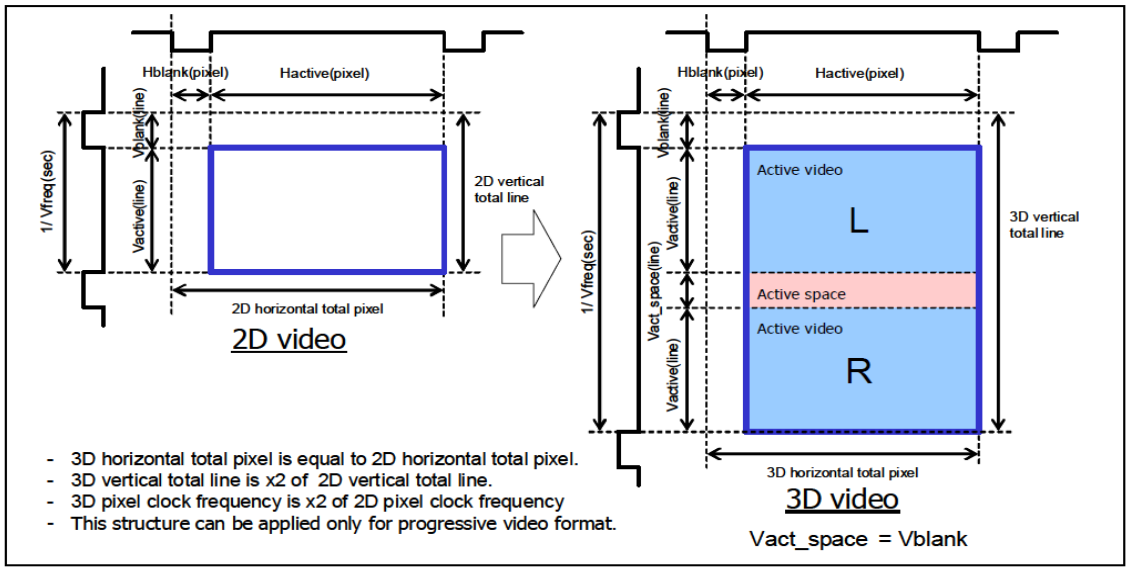


Figure 4.2 3D structure (Frame packing for progressive format)

4.1.1.2. Side-by-Side

Block diagram below showed Side-by-Side structure (Half)

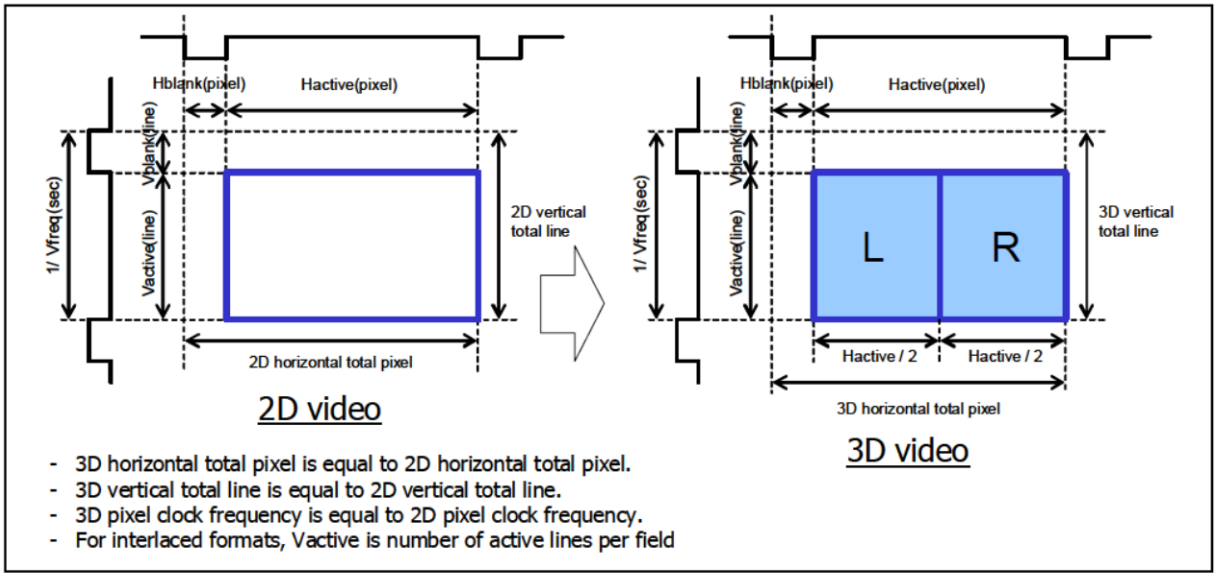


Figure 4.3 3D structure (Side-by-Side (Half))

4.1.1.3. Top-and-Bottom

Block diagram below showed Top-and-Bottom structure.

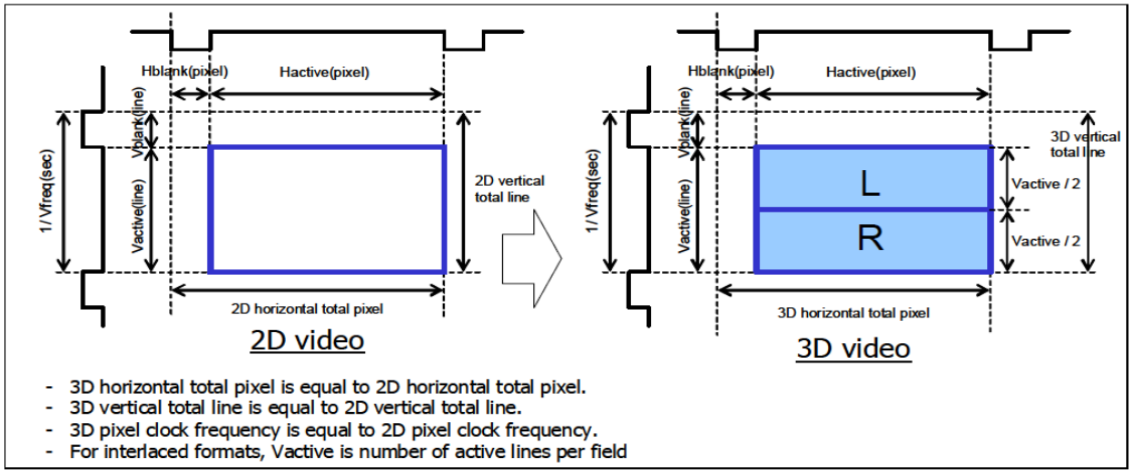


Figure 4.4 3D structure (Top-and-Bottom)

4.1.2. InfoFrame data

In HDMI stream, there are InfoFrame data. There are two methods at that the Application processor can get the InfoFrame data.

1) By reading TC9590XBG registers.
   a. When TC9590XBG detected there are a change in the InfoFrame data, it asserts the INT so that Application processor can get the InfoFrame data by reading the registers.
2) By transmit InfoFrame data over CSI-2 protocol.
   a. InfoFrame packet will be send over CSI-2 bus right after every FS packet. Total there are 224 bytes of InfoFrame data.

Below are the order that InfoFrame data send over CSI-2 protocol and it also showed the register offset.

Table 4-2 InfoFrame Data Registers Summary

CSI-2 Byte#	Register Address Offset	Register name	Description
0	0x8710	AVI_0HEAD	861B AVI_info packet – Header byte 0 (= type)
1	0x8711	AVI_1HEAD	861B AVI_info packet – Header byte 1 (= version)
2	0x8712	AVI_2HEAD	861B AVI_info packet – Header byte 2 (= data length)
3	0x8713	AVI_0BYTE	861B AVI_info packet – Data byte 0 (= checksum)
19 – 4	0x8722 – 0x8714	AVI_xHEAD	861B AVI_info packet – Data byte 15 -1
31 – 20	0x872F – 0x8723	Reserved	Reserved
32	0x8730	AUD_0HEAD	861B AUD_info packet – Header byte 0 (= type)
33	0x8731	AUD_1HEAD	861B AUD_info packet – Header byte 1 (= version)
34	0x8732	AUD_2HEAD	861B AUD_info packet – Header byte 2 (= data length)
35	0x8733	AUD_0BYTE	861B AUD_info packet – Data byte 0 (= checksum)
45 – 36	0x873D – 0x8734	AUD_xBYTE	861B AUD_info packet – Data byte 10 – 1
47 – 46	0x873F – 0x873E	Reserved	Reserved
48	0x8740	MS_0HEAD	861B MS_info packet – Header byte 0 (= type)
49	0x8741	MS_1HEAD	861B MS_info packet – Header byte 1 (= version)
50	0x8742	MS_2HEAD	861B MS_info packet - Header byte 2 (= data length)
51	0x8743	MS_0BYTE	861B MS_info packet – Data byte 0 (= checksum)
61 – 52	0x874D – 0x8744	MS_xBYTE	861B MS_info packet – Data byte 10 – 1
63 – 62	0x874F – 0x874E	Reserved	Reserved
64	0x8750	SPD_0HEAD	861B SPD_info packet – Header byte 0 (= type)
65	0x8751	SPD_1HEAD	861B SPD_info packet – Header byte 1 (= version)
66	0x8752	SPD_2HEAD	861B SPD_info packet – Header byte 2 (= data length)
67	0x8753	SPD_0BYTE	861B SPD_info packet – Data byte 0 (= check sum)
94 – 68	0x876E – 0x8754	SPD_xBYTE	861B SPD_info packet – Data byte x
95	0x876F	Reserved	Reserved
96	0x8770	VS_0HEAD	861B VS_info packet – Header byte 0 (= byte)
97	0x8771	VS_1HEAD	861B VS_info packet – Header byte 1 (= version)
98	0x8772	VS_2HEAD	861B VS_info packet – Header byte 2 (= data length)
99	0x8773	VS_0BYTE	861B VS_info packet – Data byte 0 (= checksum)
126 – 100	0x878E – 0x8774	VS_xBYTE	861B VS_info packet – Data byte x
127	0x878F	Reserved	Reserved
128	0x8790	ACP_0HEAD	ACP packet – Header byte 0 (= type)
129	0x8791	ACP_1HEAD	ACP packet – Header byte 1
130	0x8792	ACP_2HEAD	ACP packet – Header byte 2
131	0x8793	ACP_0BYTE	ACP packet – Data byte 0
156 – 132	0x87AE – 0x8794	ACP_xBYTE	ACP packet – Data byte x
157	0x87AF	Reserved	Reserved
160	0x87B0	ISRC1_0HEAD	ISRC1 packet – Header byte 0
161	0x87B1	ISRC1_1HEAD	ISRC1 packet – Header byte 1
162	0x87B2	ISRC1_2HEAD	ISRC1 packet – Header byte 2
178 – 163	0x87C2 - 0x87B3	ISRC1_xBYTE	ISRC1 packet – Data byte x
191 – 179	0x87CF – 0x87C3	Reserved	Reserved
192	0x87D0	ISRC2_0HEAD	ISRC2 packet – Header byte 0
193	0x87D1	ISRC2_1HEAD	ISRC2 packet – Header byte 1
194	0x87D2	ISRC2_2HEAD	ISRC2 packet – Header byte 2
222 – 195	0x87EE – 0x87D3	ISRC2_xBYTE	ISRC2 packet – Data byte x
223	0x87EF	Reserved	Reserved

AVI: Auxiliary Video Information InfoFrame, InfoFrame_type = 0x02, HDMI Packet Type = 0x82
AUD: Audio InfoFrame, InfoFrame_type = 0x04, HDMI Packet Type = 0x84
MS: MPEG Source InfoFrame, InfoFrame_type = 0x05, HDMI Packet Type = 0x85
SPD: Source Product Description InfoFrame, InfoFrame_type = 0x03, HDMI Packet Type = 0x83
VS: Vendor Specific InfoFrame, InfoFrame_type = 0x01, HDMI Packet Type = 0x81
ACP: Audio Content Protection Packet, HDMI Packet Type = 0x4
ISRC1: HDMI Packet Type = 0x5
ISRC2: HDMI Packet Type = 0x6

4.1.3. Color Space Conversion

TC9590XBG provides color space conversion to transfer RGB888 data format to YUV444 or YUV422. It also provides conversions between YUV422 and YUV444. The register settings requirement for each conversion is listed below.

4.1.3.1. RGB888 to YUV422

0x8574 [3]	= 1'b1	(Enable 0x8573 [7])
0x8573 [7]	= 1'b1	(YUV 422 out selected)
0x8573[6:4]	= 3'b100	
0x8573[1:0]	= 1'b 01	(Use Internal default setting)
0x8576 [7:5]	= 3'b 011 or 101	(Output color space setting)
0x0004 [7:6]	= 2'b11	(For CSITx)

4.1.3.2. RGB888 to YUV444

0x8574[3]	= 1'b1	(Enable 0x8573[7])
0x8573 [7]	= 1'b0	(YUV444 output selected)
0x8573 [1:0]	= 3'b01	(Use Internal default setting)
0x8576 [7:5]	= 3'b011 or 101	(Output color space setting)
0x0004 [7:6]	= 2'b00	(For CSITx)

4.1.3.3. YUV444 to YUV422

0x8574[3]	= 1'b1	(Enable 0x8573[7])
0x8573 [7]	= 1'b1	(YUV 422 output selected)
0x0004 [7:6]	= 2'b11	(For CSITx)

4.1.3.4. YUV422 to YUV444

0x8574[3]	= 1'b1	(Enable 0x8573[7])
0x8573 [7]	= 1'b0	(YUV 444 output selected)
0x0004 [7:6]	= 2'b00	(For CSITx)

4.2. CSI-2 TX Protocol

In addition to data formats specified by CSI-2 specification, TC9590XBG supports more data formats from HDMI input, including its data island data. Table below shows how TC9590XBG supports/allocates DataType for non-CSI-2 packets.

1. For interlace video, users should program their desired interlace stream DataID in register field PacketID1.VPID0 and PacketID1.VPID1 for top and bottom field, respectively.
   - Limitation: YCbCr422 16bpp interlaced output video can Not be supported.
2. For CSI-2 specified data formats, DataType follows CSI-2 standard
3. For non-CSI-2 supported YCbCr progressive data formats:
   - YCbCr444 (24bpp) uses 0x24, which is the same as that of RGB888.
   - YCbCr422 (24bpp) uses the value programmed in register field PacketID3.VPID2.
   - The DataType for YCbCr422 (16bpp) depends on register bits set in ConfCtl[YCbCrFmt]
     - o ConfCtl[YCbCrFmt] = 2'b10, uses the one in PacketID3.VPID2
     - o ConfCtl[YCbCrFmt] = 2'b11, CSI-2 standard specified 0x1E will be used.

Table 4-3 Supported Data Types and Their Data ID fields

DataType ID Register	Description
0x00	Frame Start Code
0x01	Frame End Code
VPID0	For Interlaced frame Top field
VPID1	For Interlaced frame Bottom field
VPID2 (Register PacketID3)	- YCbCr422 24bpp data format packed as CSI-2 RAW12 data format. Data ID is specified in VPID2 - Internal generated pattern, e.g. color bar, uses VPID2 to indicate its data format, which is independent of color format
APID	Audio packet. Audio CSI-2 Packet ID is defined in PACKETID2 register (APID parameter)
IFPID	InfoFrame packet. CSI-2 packet ID is defined in PacketID2 register (IFPID parameter)

Note: YCbCr444 24bpp uses the same Data ID as that of RGB888, 0x24.

VSYNC, HSYNC and Line# signals in figure below shows conceptual how frame start/end and line start/end related to HSYNC, VSYNC and Line#.

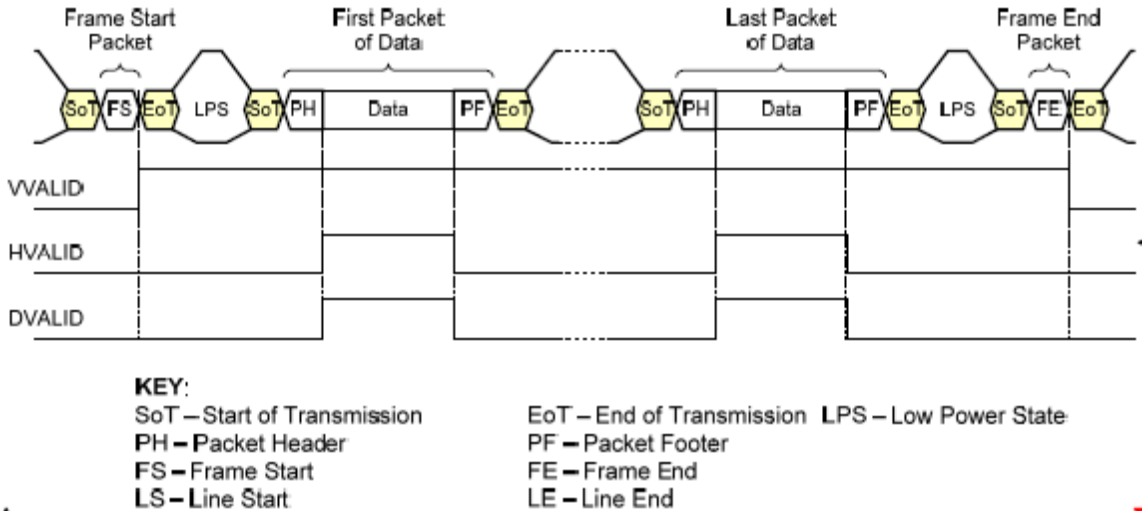


Figure 4.5 Multiple Packet Example

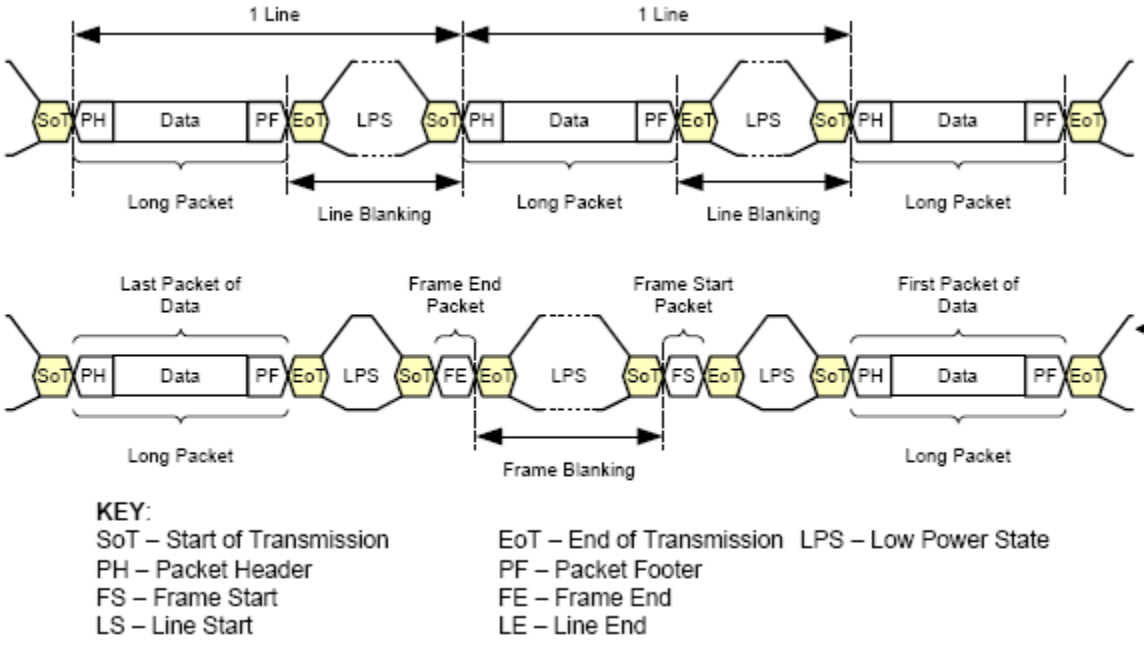


Figure 4.6 Line and Frame Blanking Definitions

CSI-2 terminology:

- Line Blanking Period is the period between the Packet Footer of one long packet and the Packet Header.
- Frame Blanking Period is the period between the Frame End packet in frame N and the Frame Start packet in frame N+1.

The Line Blanking Period is not fixed and may vary in length.

In Serial link, video data is transferred in byte oriented with LSB shifted out first for transmission. The data transmission format of each of video formats in Serial link are shown in Figures below.

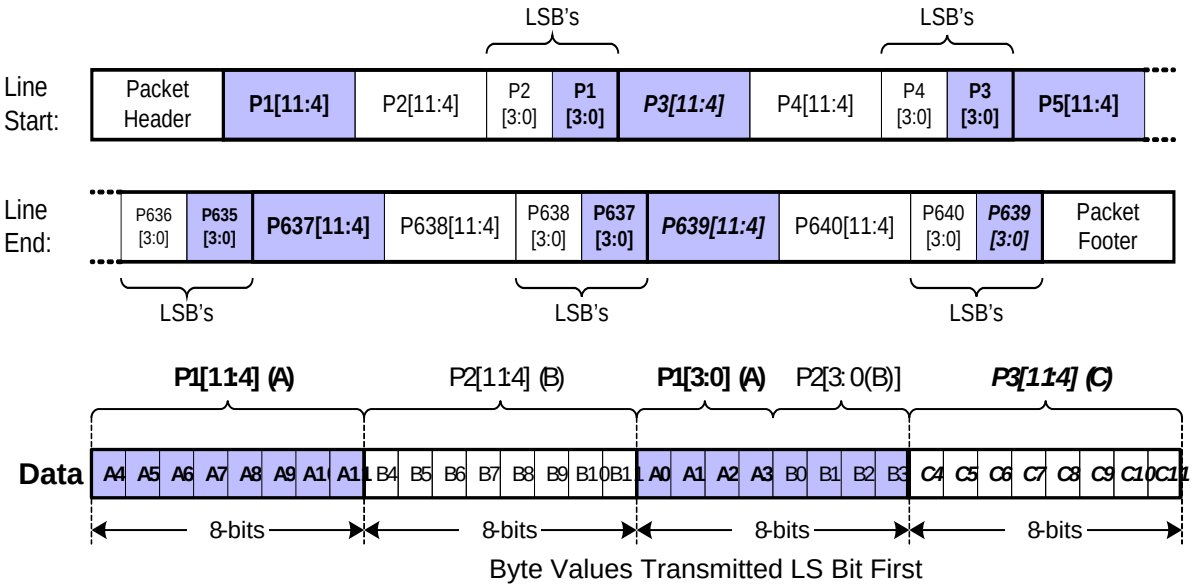


Figure 4.7 RAW12 Data Transmission

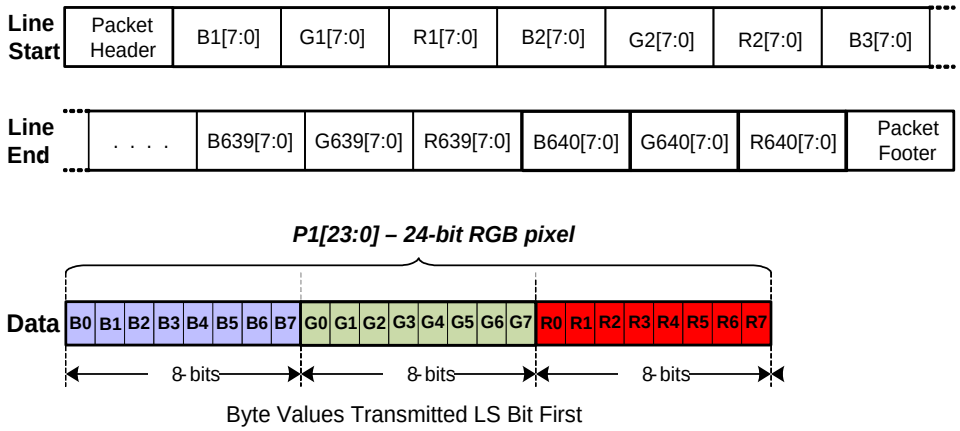


Figure 4.8 RGB888 Data Transmission

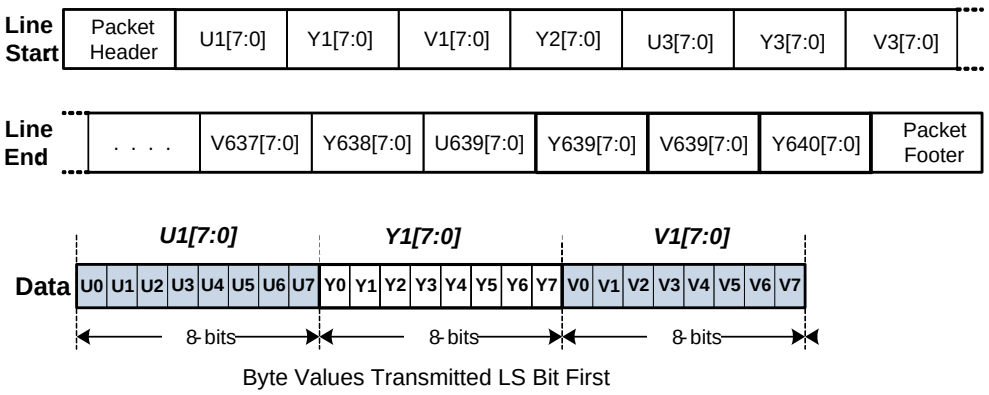


Figure 4.9 YCbCr422 8-bit Data Transmission

All serial byte data will be pack into 32-bit word data before write into the video fifo.

4.3. CSI-2 TX Interface Block

The CSI-2 TX consists of CSI-2 D-PHY and Transmit Serial Protocol Layer blocks. The CSI-2 TX supports one clock lane and up to four data lanes which interface with a quad lane Serial Interface.

CSI-2 Tx supports the following video data format

- RGB888 used for RGB, YCbCr444: 24-bpp
- RAW12 used for YCbCr422 12-bit
- YCbCr422 8-bit used for YCbCr 422 12-bit – discard last 4 data bits

A lane merger block in Serial Protocol layer is fetching the 32-bit data from VB module and splitting data to two to four data lanes - CSI-2 D- PHY.

The CSI-2 TX serial video data format is transferred in byte oriented with LSB shifted out first for transmission.

Enable Audio data to send over CSI-2 instead of I2S/TDM.

- Audio data send out during Horizontal and Vertical blank period. During the Horizontal blank period, if only there are no data in the Video fifo then audio data will be transmit out.

Enable InfoFrame data to send over CSI-2 instead of Host reads Info Frame data over I^2C i/f

- All InfoFrame data will send out right after FrameStart packet. Total there are 128 bytes of InfoFrame data.

HDMI YCbCr444 data format (used RGB888 data format)

- Y mapped to G
- Cr mapped to R
- Cb mapped to B

HDMI YCbCr422 12-bit data format (used RAW12 data format)

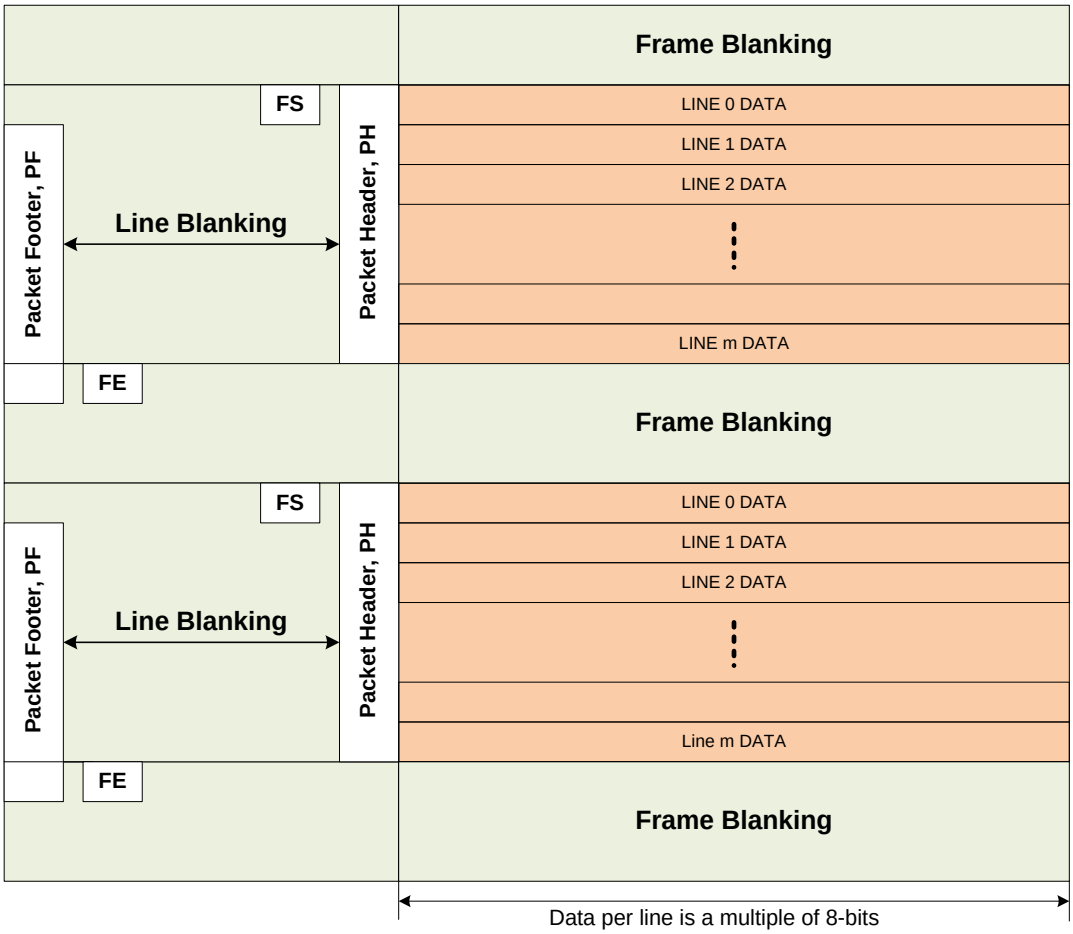
- Cb0 = P1, Cb2 = P5, ….
- Y0 = P2, Y2 = P6,…
- Cr0 = P3 Cr2 = P7,
- Y1 = P4 Y3 = P8

Need to add YCbCr 8-bit diagram

Cb = U
Cr = V
Y = Y

4.4. CSI-2 TX Packet Format

The CSI-2 TX packet data formats are showed in Figure 4.5 and Figure 4.6. The Frame format is showed in below Figure.



KEY:
PH – Packet Header
PF – Packet Footer
FS – Frame Start
FE – Frame End

Figure 4.10 Frame Format

4.5. Frame Count

Frame count # can be embedded into Frame Start and Frame End packet (in WC field).

Frame count maximum value is defined in FCCtl register.

- When FrCnt = 0, WC field = 0
- When FrCnt = 1, WC field = 1, 1, 1, 1, 1,
- When FrCnt = 2, WC field = 1, 2, 1, 2, 1, 2, ….
- When FrCnt = 3, WC field = 1, 2, 3, 1, 2, 3, ….
- …

Frame count is increment at every HDMI Vsync.

4.6. Checksum Generation

Checksum is calculated over each data packet. The checksum is realized as 16-bit CRC. The generator polynomial is $x^{16} + x^{12} + x^5 + x^0$.

The transmission of the checksum is showed in below Figure.

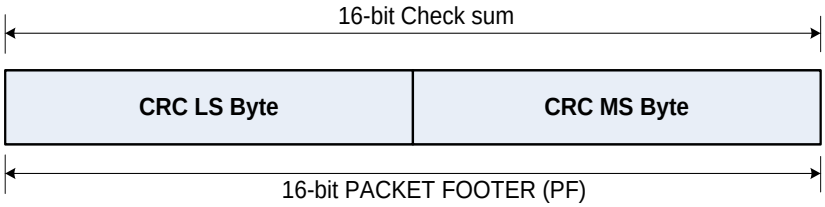


Figure 4.11 Checksum Transmission

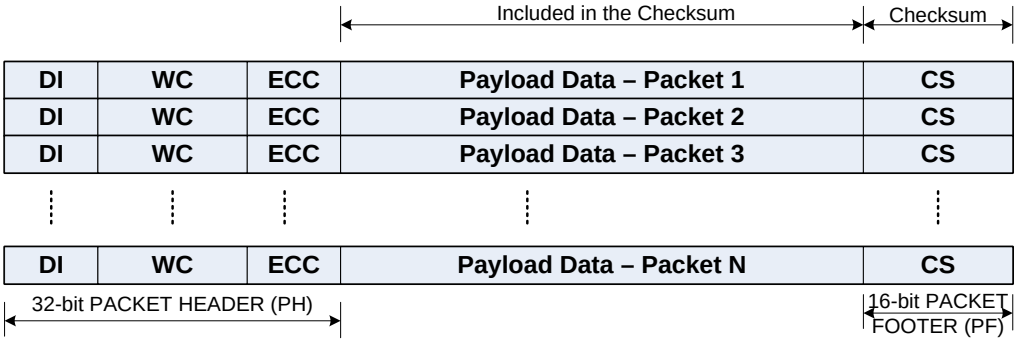


Figure 4.12 Checksum Generation for Packet Data

The 16-bit checksum sequence is transmitted as part of the Packet Footer. When Word Count is zero, the CRC shall be 0xFFFF.

4.7. CSI-2 TX One Frame Operation

Below describes the TC9590XBG sequence for transmit out the video data onto CSI-2 TX.

1) Enable CSI-2 TX and HDMI RX port.
2) TC9590XBG wait for assertion of VSYNC (indicates beginning of frame).
3) TC9590XBG wait for the Line buffer reaches the programmable “FIFO Level”.
4) Then transmit “FS” packet for 1st line only.
5) Transmit “PH” packet – follow by Line Data until “pixel count” reached.
6) Transmit “PF” packet then
   a. Wait Line buffer reaches the programmable FIFO level then loop back to step “5” if Vsync is not active.
   b. If Vsync is active, go to step “7”.
7) Transmit “FE” packet, then loop back to step “3”.

4.8. DDC Controller

DDC Interface is same as I^2C slave protocol. DDC module supports the following features.

- Up to 400 kHz fast mode operation
- Supports 7 bit slave addresses recognition
- No support for general call address

Main purpose of DDC interface is for HDMI-TX to read the EDID_SRAM contents and to perform HDCP authentication TC9590XBG. TC9590XBG designed in a 1Kx8 EDID_SRAM.

- TC9590XBG has two data paths that can write the data into EDID_SRAM

1) EDID controller fetch data from external EPROM and store them into EDID_SRAM
2) Baseband Application processor write the data into EDID_SRAM

After reset, EDID_SRAM will be filled with valid data either by the EDID controller through EDID interface or by Baseband Application processor through I^2C interface.

4.9. EDID Controller

EDID Interface is same as I^2C master protocol. EDID module supports the following features.

- Up to 400 kHz fast mode operation
- Programmable 7 bit slave address
- No multiple master support

EDID controller is capable of fetching the EDID data from external memory device. It can fetch up to 1024 byte of data.

To download the external EPROM data into EDID_SRAM, Application processor need to writes into EDID configuration to trigger the EDID master controller to download the external Eprom data into EDID_SRAM.

4.10. CEC Controller

CEC uses a single line to transfer data between TC9590XBG bridge and a HDMI source. Messages are transferred as a single frame, which is built out of a start bit followed by data bits. The bit timing is clearly defined with different timings for the start bit and data bit period. Fixed bit timing is required, because no clock information is transferred over the CEC line.

Each transferred message starts with the transmission of a start bit, which is used to indicate the start of a message and which is also used for arbitration as several device could try to start a transfer. Once arbitration is won, the following information is transmitted in blocks (header block, opcode block and operand block). Each block consists of 8 data bits, one EOM – End Of Message indicator and an acknowledge bit period, where the acknowledge will be used by the addressed device to indicate successful transmission of each block.

The HDMI-to-CSI bridge (TC9590XBG) supports the Consumer Electronics Control Protocol as defined in HDMI specification. TC9590XBG offers the physical interface and low level support for data parsing.

4.10.1. Receive Operation Sequence

The following are the sequences for CEC Receive operation

- TC9590XBG collects CEC byte data into Receive FIFO (maximum 16 bytes)
- TC9590XBG asserts INT once it received a valid byte data in the Receive FIFO or after entire message has been received or there is an error condition on the CEC signal protocol.
- TC9590XBG will keep INT at High level until Host complete read out all the Receive data in the FIFO.

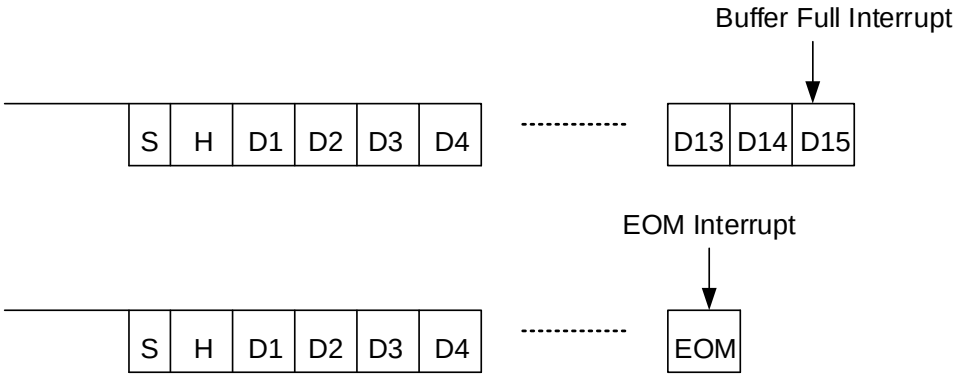


Figure 4.13 CEC reception overview

4.10.1.1. Noise cancellation time

The noise cancellation time is configurable with the CECHNC and CECLNC registers. The CEC line is monitored at each rising edge of the sampling clock. In the case that the CEC line has changed from “1” to “0”, the change is fully recognized if “0”s of the same number as specified in the CECLNC bit are monitored. In the case that the CEC line has changed from ”0” to “1”, the change is fully recognized if “1”s of the same number as specified in the CECHNC bit are sampled.

The following figure illustrates the operation when the noise canceling is configured as CECHNC = 10 (3 samplings) and CECLNC = 011 (4 samplings). By canceling the noise, a signal “1” shift to “0” after “0” is sampled four times. The signal “0” shifts to “1” after “1” is sampled three times.

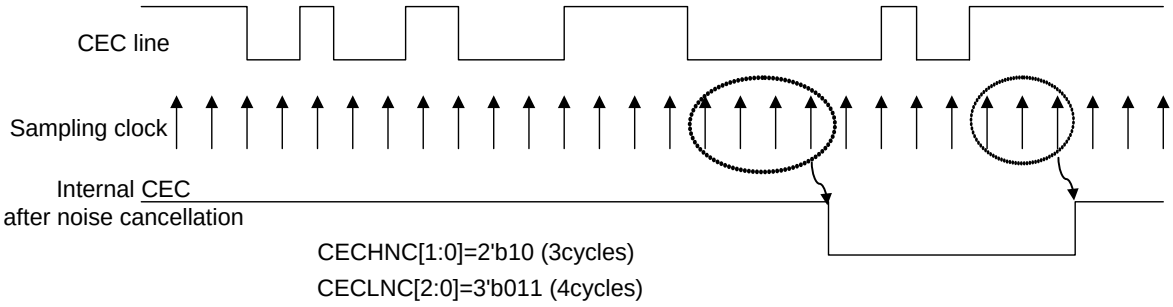


Figure 4.14 CEC noise cancellation example

4.10.1.2. Start bit detection

The following registers used to detect the start bit of CEC line.

CECSWAV0 is used to specify the fastest start bit rising timing.
CECSWAV1 specifies the latest start bit rising timing ((1) in the figure shown below).
CECSWAV2 is used to specify the minimum number of cycles of a start bit (corresponds to the length of a start bit measured in sampling clock cycles).
CECSWAV3 specifies the maximum cycle of a start bit ((2) in the figure shown below).

The start bit is considered to be valid if a rising edge during the period (1) and a falling edge during the period (2) are detected.

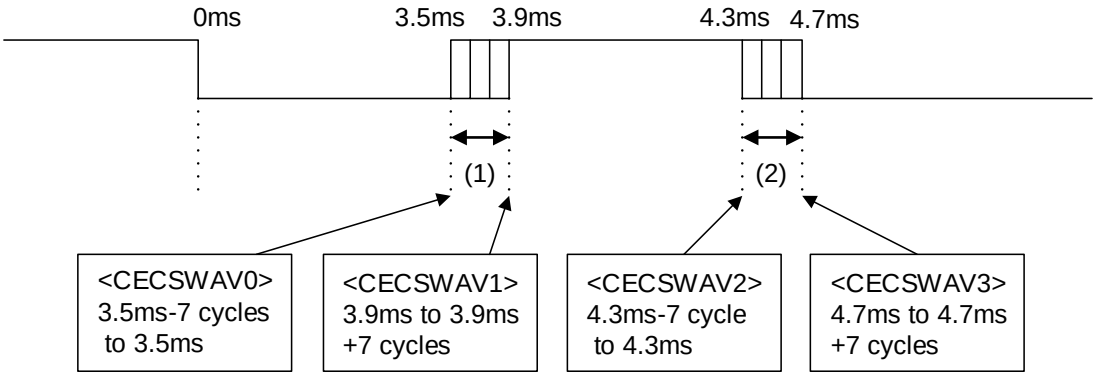


Figure 4.15 CEC start bit detection

4.10.1.3. Waveform Error Detection

The following registers CECWAV0, CECWAV1, CECWAV2 and CECWAV3 are used to detect logic transition on CEC line.

A waveform error interrupt is generated if a rising edge is detected during the period (1) or (2) shown below, or if no rising edge is detected in the timing described in (3).

(1) – period between the beginning of a bit and the fastest logical “1” rising timing
(2) - period between the latest logical “1” rising timing and the fastest logical “0” rising timing
(3) - the latest logical “0” rising time

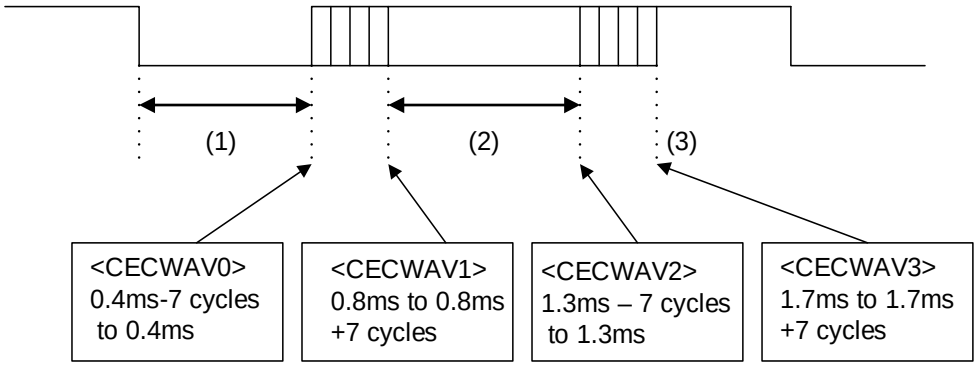


Figure 4.16 waveform error detection

4.10.1.4. Data sampling timing

The figure shown below illustrates a data sampling timing. The CECDAT register specifies the data sampling point per two sampling clock cycles within the range of + or - 6 cycles from the reference point (approx. 1.05 ms).

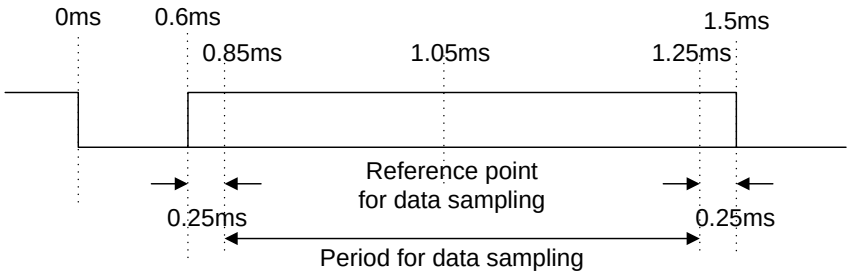


Figure 4.17 sampling time example

4.10.2. Transmit Operation Sequence

The following are the sequence for CEC transmit operation

- Write all transmit CEC byte data into Transmit FIFO (maximum 16 bytes)
- Enable CEC transmission feature by writing “1” to register bits 0x0600[0] and 0x0620[0]
- TC9590XBG asserts INT once CEC transmit operation is completed or there is an error condition on the CEC signal protocol.
- Host must read the CEC_Status register to know the status of the transmitting operation and take appropriate action.

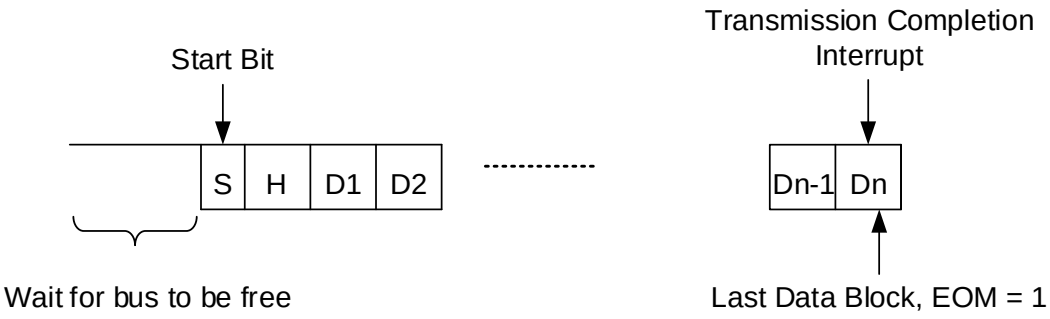


Figure 4.18 CEC transmission example

4.10.2.1. Wait Time for Bus to be Free

The wait time for a bus free check at transmission start is configured with the CECFREE register. It can be specified in a range from 1 to 16 sample clock cycles. Start point to check if a bus is free is the end of final bit. If a bus is free for specified bit cycles of “1”, transmission starts.

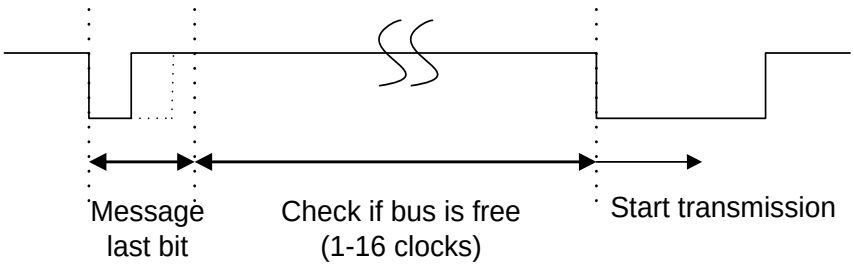


Figure 4.19 Transmission starts

4.10.2.2. Transmission Timing

The timing of the start and data bits can be adjusted with the registers as shown in the figure below.

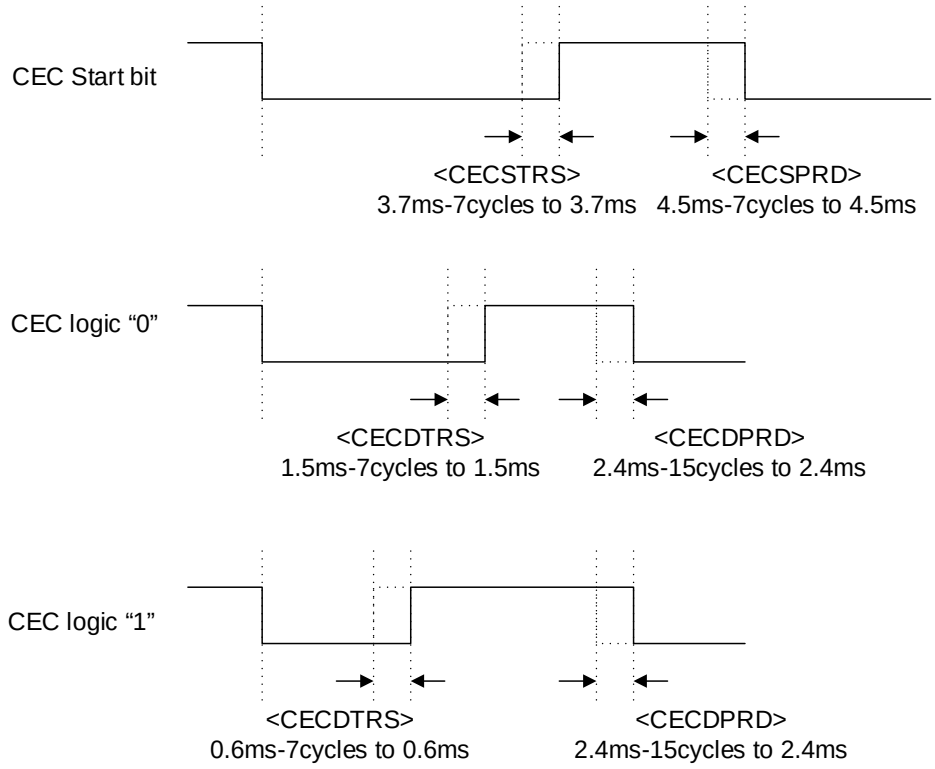


Figure 4.20 Transmission timing

4.10.3. Arbitration lost

An arbitration lost error occurs when CEC module detects “0” during the detection windows as shown in the figure below.

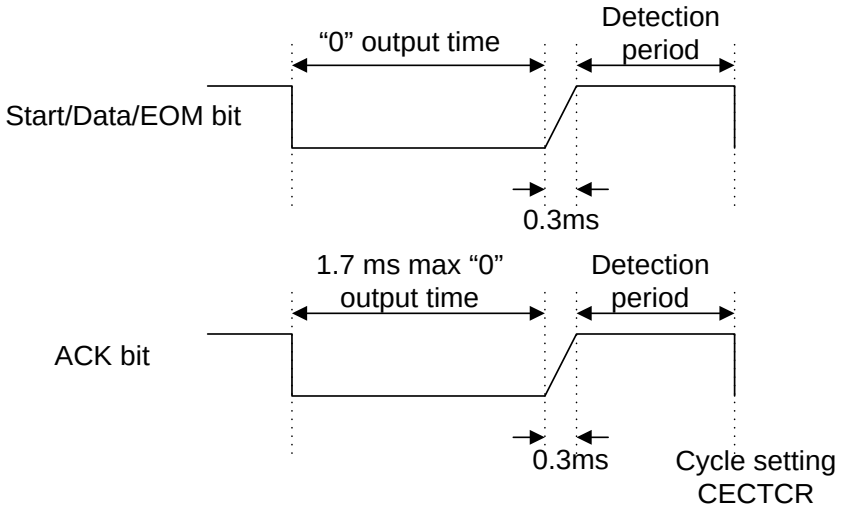


Figure 4.21 Arbitration Error check

4.10.4. Low level functions

In order to ensure transmission on the CEC line, the bridge serves the following low-level functions in accordance to the CEC standard:

- Monitoring of CEC line at all times for any incoming message except when CEC module is off (SET_CEC_ENABLE command).
- Line detection (free/occupied). This function tests the line if it is free to be used.
- Data/Frame parsing. Details of the CEC Frames (header, data blocks, EOM, ACK) will be split and stored.
- Acknowledgment of messages (positive/negative). Success or failure of message transmission will be notified to sender.
- Frame retransmission. Conditional retransmission of lost frames,
- Line error handling. Notification mechanism to inform about spurious pulses on the control signal line.
- Line Arbitration. Collision prevention mechanism.

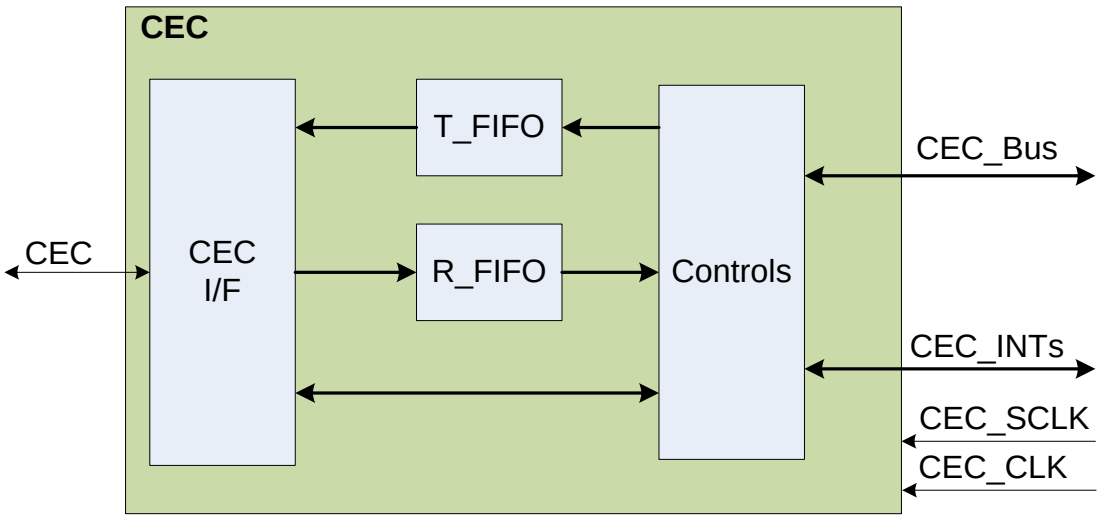


Figure 4.22 CEC Block diagram

4.11. Audio Output Function

TC9590XBG is capable of output audio data via I2S I/F, including TDM format.

The sampling frequency fs can be 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz and 192 kHz.

TC9590XBG output OverSampling clock (A_OSCK), A_OSCK frequency equal to 256fs.

4.11.1. I2S Interface

The basic features of the I2S are outlined below:

- Single output channel (2Audio channel only)
- Support 16, 18, 20 or 24 bits data
- Support Left or Right-justify with MSB first
- Support 32 bit-wide time slot only.
- Support only Master Clock option

I2S bus is a 3-pin serial link consisting of a line for two time multiplexed data channels (left and right), a word select line and a clock line. Since the transmitter and receiver have the same clock signal for data transmission, the transmitter as the master, has to generate the bit clock (SCK), and word-select (WS).

When Audio Fifo reaches certain (programmable) level, I2S controller will begin to fetch the data and transfer them over I2S interface. Once the Audio Fifo is empty, I2S controller will finish transfer the last bit of Audio data then it will keeps SCL LOW until it has more data.

Note:

1) The time-slot is 32 bit-wide. Input data could be 16, 18, 20 or 24 bits and could be left- or right-justify with MSB first or LSB first. There are three formats show in the below figures. Figure xx(a) illustrates Standard Data Format (Sony Format) with Left-Channel “H” and Right-channel “L”, (b) Left Justified Format with Left-channel “L” and Right-channel “H”. For I2S data format, there is one clock delay to latch the data bit.
2) I2S signals are multiplexed with TDM signal. Only one interface can be enables at a time.

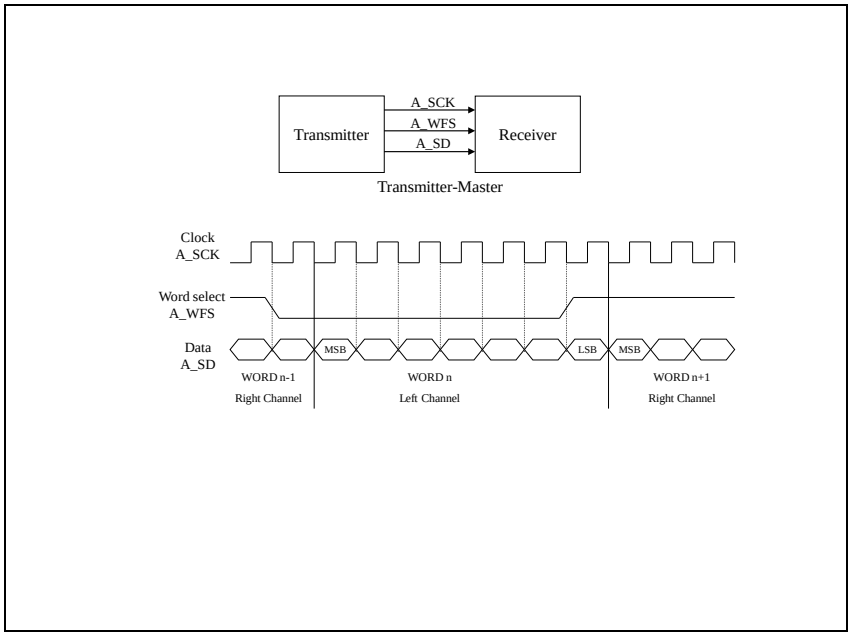


Figure 4.23 I2S Interface

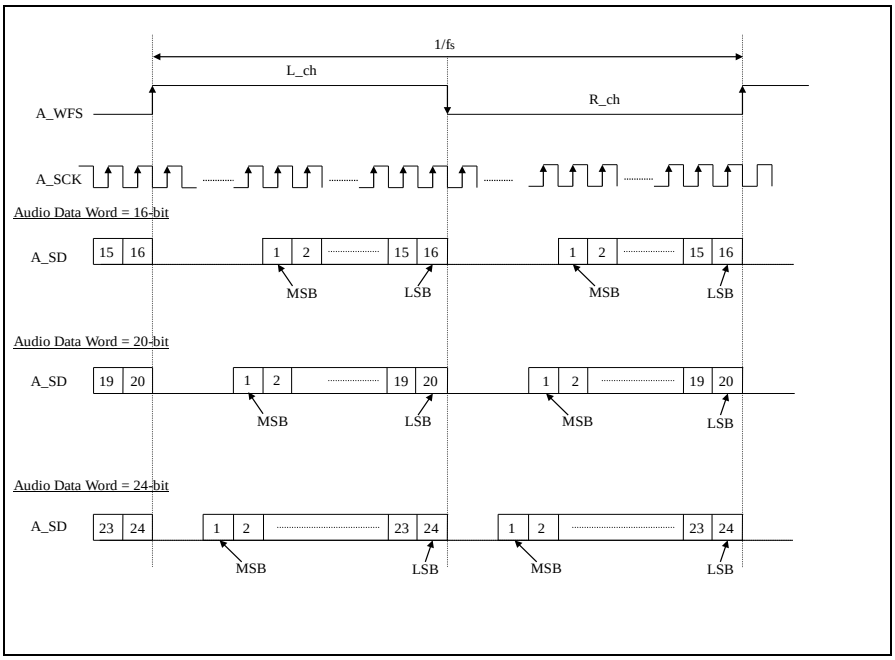


Figure 4.24 Data input timing of standard format (Sony format); L_ch = H, R_ch = L (SDO_MODE1.SDO_FMT = 2'b00, ConfCtl.I2SDlyopt = 1'b0, SDO_MODE0.LR_POL = 1'b1)

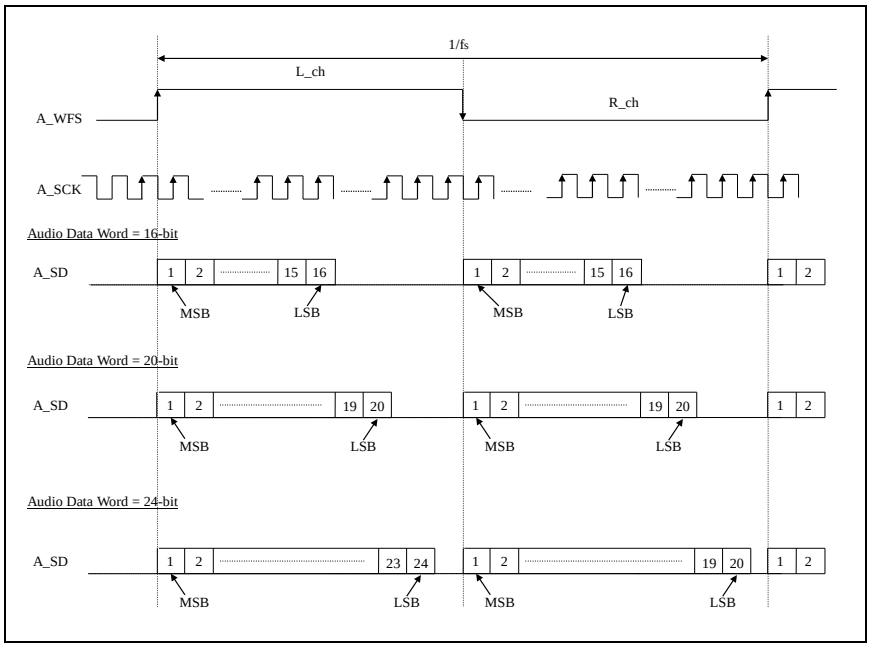


Figure 4.25 Data input timing of Left-Justified format; L_ch = H, R_ch = L (SDO_MODE1.SDO_FMT = 2'b01, ConfCtl.I2SDlyopt = 1'b0, SDO_MODE0.LR_POL = 1'b1)

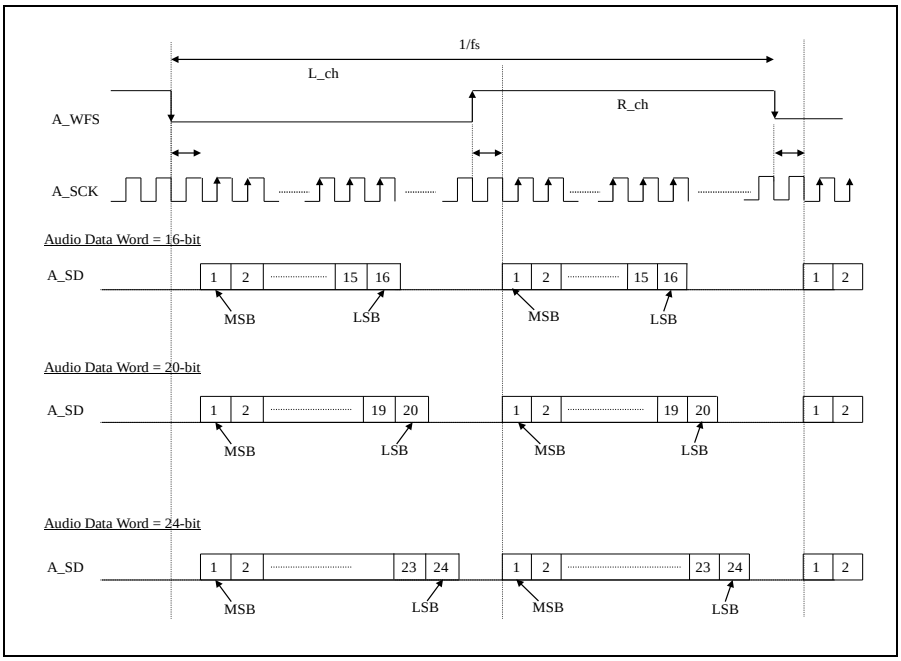


Figure 4.26 Data input timing of I2S data format (Phillips format); L_ch = L, R_ch = H (SDO_MODE1.SDO_FMT = 2'b10, ConfCtl.I2SDlyopt = 1'b1, SDO_MODE0.LR_POL = 1'b0)

4.11.2. TDM (Time Division Multiplexed) Audio Interface

The basic features of the TDM are outlined below:

- Single output channel
- Support 16, 18, 20 or 24 bits data
- Support up to 8 channels
  - ➢ TDM output fixed at 8 channels
  - ➢ Fixed at 32 bit-time slot
- Support Master clock only

TDM interface allows multiple channels of data to be transmitted on a single data line. TDM interface is comprised of three signals: a frame synchronization pulse (WFS), serial clock (SCK) and serial audio data (SD).

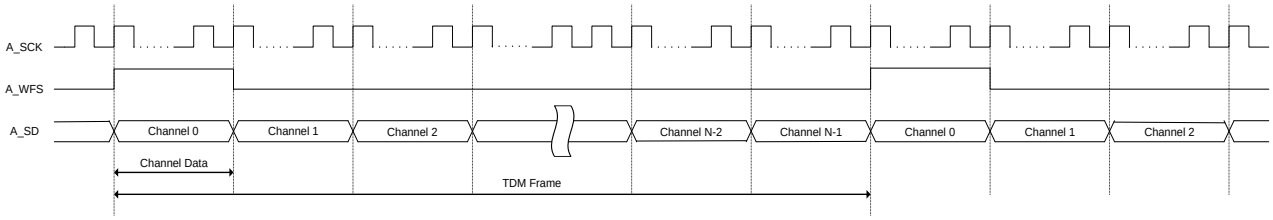


Figure 4.27 I2S N-Channel TDM timing

4.11.3. Audio PLL LPF Configuration

The Audio PLL external terminal connections used in the Audio clock generation are shown in be Figure.

In DAOUT output (PLL input), a low pass filter is installed in the LSI external area.

In addition, a low pass filter for cutting unnecessary components in phase comparator output in the PLL is also installed in the LSI external area.

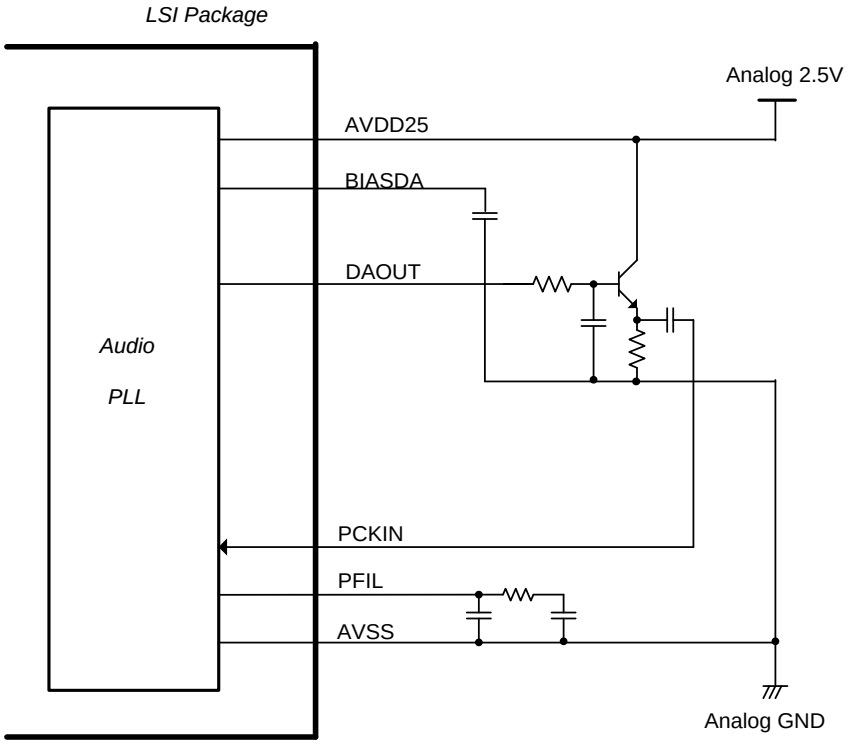


Figure 4.28 Audio Clock External LPF circuit block diagram

4.12. InfraRed (IR) Interface

The basic features of the IR are outlined below:

- Support NEC IR protocol
- Store up to 4 byte IR data
- Interrupt Host when IR address match and detect “end of message” transmission pulse.
- Programmable timing for Leading High time, Leading Low time, Logical “0” H and L time, Logical “1” H and L time.

Supports NEC IR transmission protocol, which uses pulse distance encoding of the message bits. Below figures describes NEC InfraRed protocol.

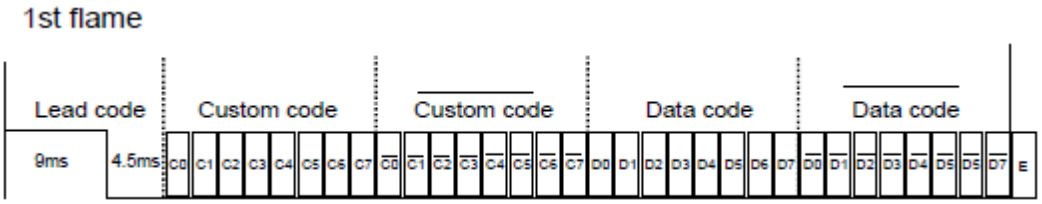


Figure 4.29 NEC Configuration of Frame

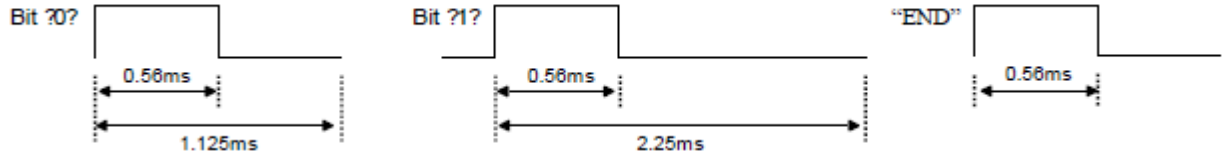


Figure 4.30 NEC Bit Description

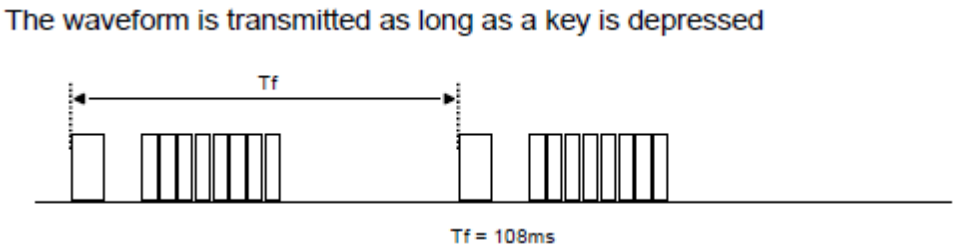


Figure 4.31 NEC Frame Interval (Tf)

4.12.1. Sampling Clock

IR lines are sampled by divide down Refclk (ir_clk).
ir_clk clock is generated from Refclk with divide option for High time and Low time.

There are two parameters.

1) reg_cech[10:0] contains the cec_clk HIGH time count (counts with RefClk). HIGH time has range of 1 to 2048 RefClk clock.
2) reg_cecl[10:0] contains the cec_clk LOW time count (counts with RefClk). LOW time has range of 1 to 2048 RefClk clock.

There are 12-bit counter to count the IR H time and L time with IR sampling clock. Host can configures the appropriate frequency for the IR sampling clock (ir_clk).

4.12.2. Programmable timing

There are four programming timing parameters. IR modules use these timing parameters to detect Lead code, Bit H logic, Bit L logic and “END” flag. Below describes these four timing parameters.

1) Detect Lead code when:
   a. H count value is greater than LCHmin parameter (lchmin[11:0]) and smaller than LCHmax parameter (lchmax[11:0]).
   b. L count value is greater than LCLmin parameter (lclmin[11:0]) and smaller than LCLmax parameter (lclmax[11:0]).
2) Detect “L” bit when:
   a. H count value is greater than BitHHmin parameter (bhhmin[11:0]) and smaller than BitHHmax parameter (bhhmax[11:0]).
   b. L count value is greater than BitHLmin parameter (bhlmin[11:0]) and smaller than BitHLmax parameter (bhlmax[11:0]).
3) Detect “H” bit when:
   a. H count value is greater than BitLHmin parameter (blhmin[11:0]) and smaller than BitLHmax parameter (blhmax[11:0]).
   b. L count value is greater than BitLLmin parameter (bllmin[11:0]) and smaller than BitLLmax parameter (bllmax[11:0]).
4) Detect “END” flag when:
   a. After received Lead code – Custom code - /Custom code – Data code - /Data code
   b. H count value is greater than EndHmin parameter (IR_EndHMIN[11:0]) and smaller than EndHmax parameter (IR_EndHMAX[11:0]).

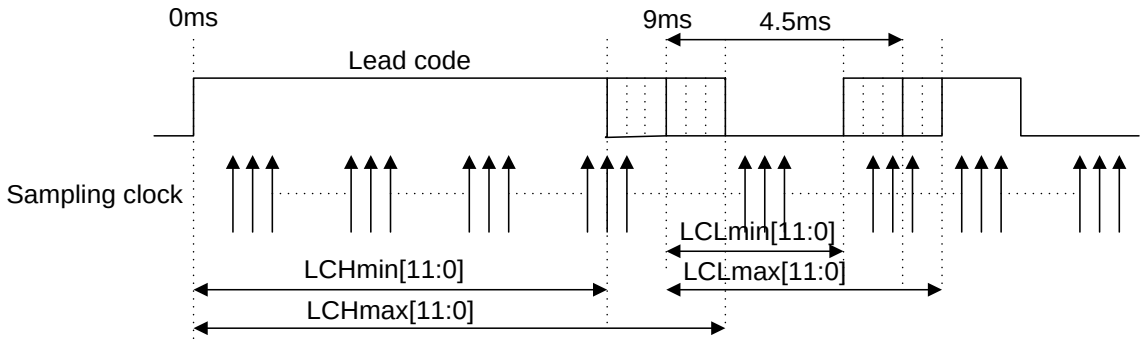


Figure 4.32 Example of Lead Code min/max values for H and L detection

4.12.3. Basic Operation

The following shows the IR sequences:

1) Detect Lead code
2) Receive 8-bit Custom code
3) Receive 8-bit / Custom code
4) IR logic compare the Receive Custom code against the programmable custom code in IR_ccode register. If they are match then IR controller continues to collect the data code. Otherwise it will ignore the IR data.

   (Step 5 – 9 assumes Custom code match)
5) Receive 8-bit Data code
6) Receive 8-bit / Data code
7) Receive “End” code
8) After IR controller receive the “End” code, INT pin will be set (provided that IR_INT is not mask).
   a. If “End” code is not receive – “End” code error flag will be set. INT pin will be set (provided that IR_Err is not mask)
9) Host need to read the 8-bit Data code through the I^2C interface. Once the all the IR data code has been read host needs to clear the interrupt by writing “1” to the respective bit of the Interrupt Status register

Note: IR controller has buffer to store maximum 4 bytes of IR Data code and one 8-bit Custom code (for debugging purpose).

4.13. I²C

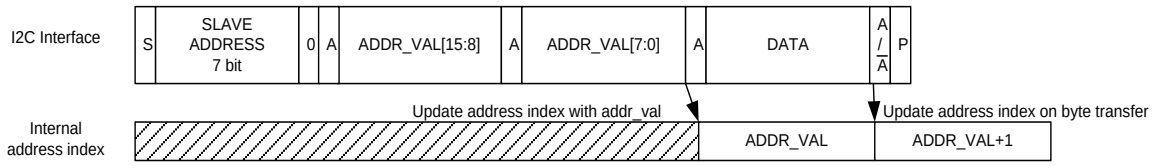
TC9590XBG supports an I²C slave function. The I²C module supports the following features:

- Fail safe I²C pad operation
- Up to 400 kHz fast mode operation
- Support special mode – Ultra fast mode 2 MHz
- Supports 7 bit slave addresses recognition (slave address = 7'b000_1111)
- No support for general call address
- Supports 16 bit index value for TC9590XBG I²C slave access

The I²C slave function supports a fixed slave address only and does not support general call address. The I²C slave function does not require any programmable configuration parameters.

4.13.1. Providing Register Address over I²C Bus

The I²C slave function requires the interfacing I²C master to provide the register address of the TC9590XBG register to be accessed. The I²C slave function loads the first two bytes following a write command as the register address (address index) to be accessed (see Figure 4.33 and Figure 4.34).



S = Start condition
Sr = Repeated start condition
A = Acknowledge
Ã = Not Acknowledge
P = Stop bit

Figure 4.33 Register Write Transfer over I²C Bus

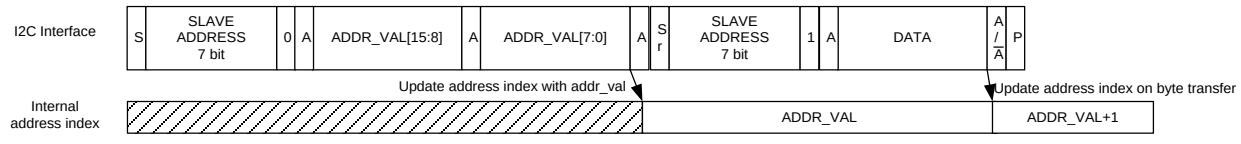


Figure 4.34 Random Register Read Transfer over I²C Bus

I²C slave function supports random write accesses and both random and continuous read accesses (see Figure 4.35).

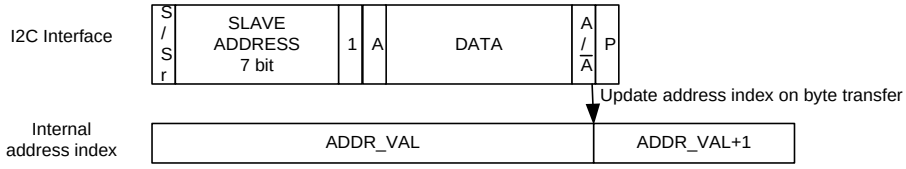


Figure 4.35 Continuous Register Read Transfer over I²C Bus

4.13.2. I²C Write Access Translation

Registers in TC9590XBG are 8, 16 and 32 bit aligned. This implies that I²C accesses to registers should always be done on 8, 16 or 32 bit boundaries depend on register group. The I²C slave controller is always operated in byte boundary. Bus management controller will pack the data to either 8, 16 or 32-bit and write into the register group accordingly.

Note that data transferred on the I²C bus is sent LSB first.

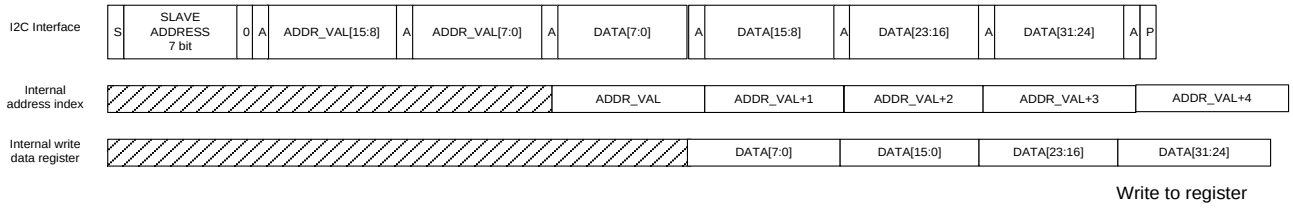


Figure 4.36 I²C Write Transfers Translated to Register Write Accesses

4.13.3. I²C Read Access Translation

Registers in TC9590XBG are 8, 16 and bit aligned. This implies that I²C accesses to registers should always be done on 8, 16 or 32 bit boundaries depend on register group. The I²C slave controller is always operated in byte boundary. Bus management controller will read the 8, 16 or 32 bit data, un-pack the data to 8-bit and send to I²C controller.

Note that data transferred on the I²C bus is sent LSB first.

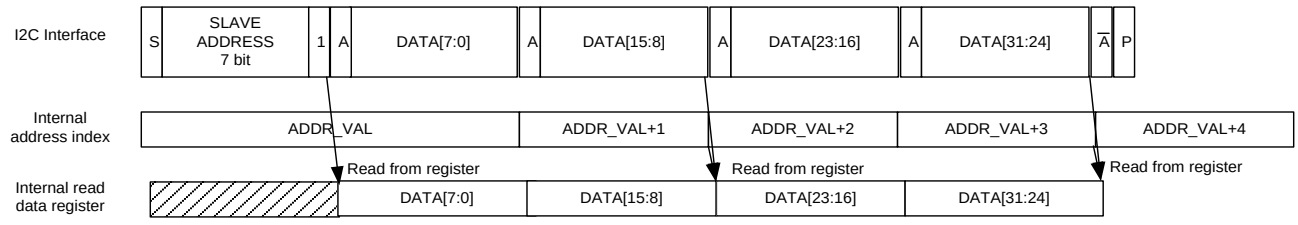


Figure 4.37 I²C Read Transfers to Register Read Accesses

5. Clock and System

The clock generation unit (CG) makes use of a single PLL and the clock are generated for the camera interface. CG supports three powers states RESET, FULLY ACTIVE and SLEEP where clocks are disabled or PLL is disabled to reduce power consumption. SLEEP state is controlled by register bit (reg_sleep).

In RESET: PLL is disabled and no clocks are output. During this state, TC9590XBG will not be able to function.

In FULLY ACTIVE: PLL and TC9590XBG system clock are enabled. Depending on the configuration, I2S controllers may also be enabled.

In SLEEP: PLL is disabled and no clocks are output.
During this state,

- Only I^2C slave, IR, DDC and CEC interface are enabled.
- To wake up TC9590XBG
  - Application processor must wake up TC9590XBG by program “0” to SLEEP bit (reg_sleep).
  - During Sleep state, TC9590XBG will Interrupt Host if either DDC or CEC accesses to TC9590XBG
- This state may be used by TC9590XBG to safely update PLL parameters when required by the application processor.

The block diagram of CG is shown below.

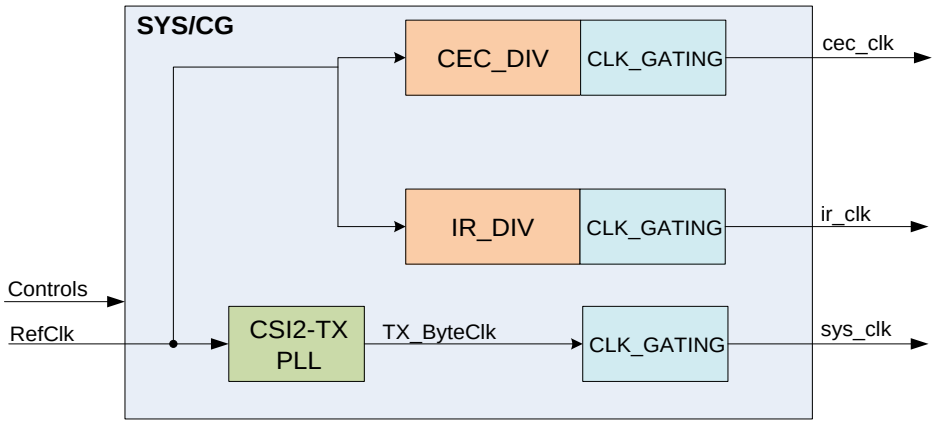


Figure 5.1 CG Block diagram

CG uses an external input clock REFCLK (27/26 MHz or 42 MHz) to generate clocks required by internal controllers.

5.1. Example of PLL Generated Clock Frequency

The possible clock frequencies generated from the PLL are achieved by varying the values in registers PLLFBD and PLLDiv.

*pll_clk = RefClk * [(FBD + 1)/ (PRD + 1)] * [1 / (2^FRS)]*

Table 5-1 provides possible frequencies that may be used in TC9590XBG.

Table 5-1 Possible PLL parameters

Reference clock (MHz)	FBD	PRD	FRS	pll_clk (MHz)
26	255	7	1	416.00
	319	5	2	346.67
	319	6	2	297.14
	319	7	2	260.00

5.2. Output Clocks Generation

SYS_DIV:

sys_clk clock is same as CSI-2 TX Byte clock.

CEC_DIV:

cec_clk clock is generated from Refclk with divide option for High time and Low time.
There are two parameters.

1) reg_CecHclk[10:0] contains the cec_clk HIGH time count (counts with RefClk). HIGH time has range of 1 to 2048 RefClk clock.
2) reg_CecLclk[10:0] contains the cec_clk LOW time count (counts with RefClk). LOW time has range of 1 to 2048 RefClk clock.

IR_DIV:

ir_clk clock is generated from Refclk with divide option for High time and Low time.
There are two parameters.

3) reg_IrHclk[10:0] contains the cec_clk HIGH time count (counts with RefClk). HIGH time has range of 1 to 2048 RefClk clock.
4) reg_IrLclk[10:0] contains the cec_clk LOW time count (counts with RefClk). LOW time has range of 1 to 2048 RefClk clock.

Table 5-2 Controllers' Operating Frequency

Controllers	Operating Frequency		Source
---	Min (MHz)	Max (MHz)	---
HDMI-RX	---	165	TDM clock
CSI-2-TX	---	125	CSI-2-TX byte clock
af and vf controller	---	125	CSI-2-TX byte clock
EDID, DDC, CEC, EDID_SRAM, REG, BM, I2C and INT	27/26	42	RefClk

5.3. TC9590XBG Deep Sleep Mode

TC9590XBG exhibits a power isolation circuit, which is shown in Figure 5.2 below. The yellow color blocks powered by VDDIO1, VDDIO2 and VDDC1 are always on to monitor IO changes. The green color blocks power suppliers, AVDD33, AVDD12, VDD_MIPI and VDDC2, can be turned off when both register bits ConfCtl.PWRISO and SysCtl.SLEEP are asserted.

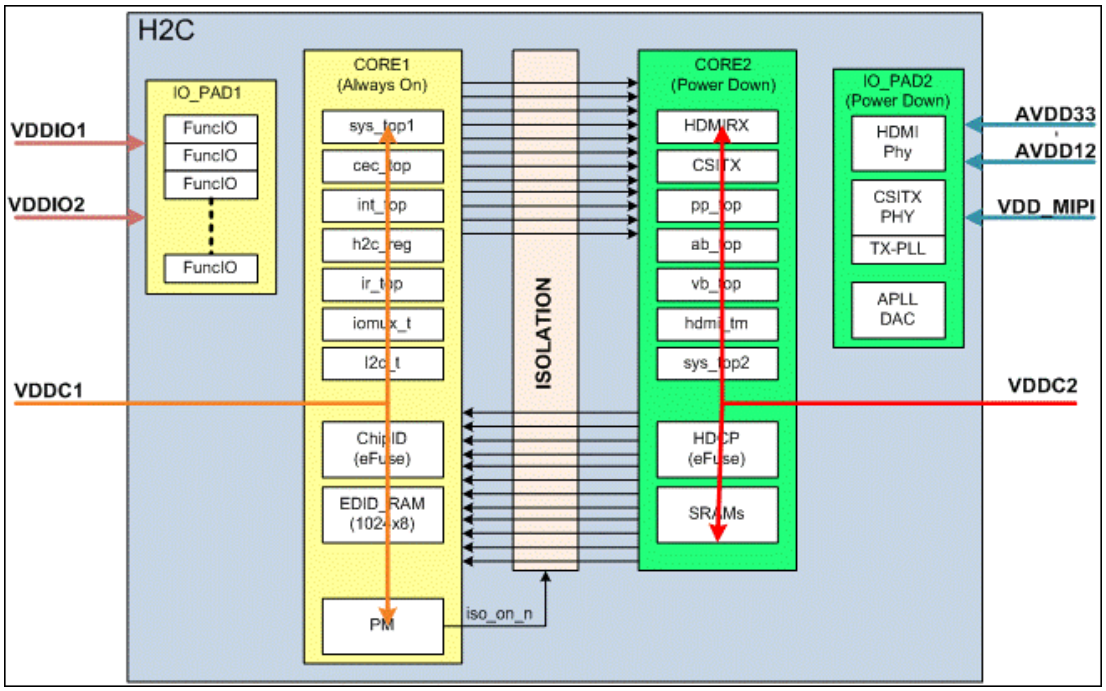


Figure 5.2 Power Isolation Diagram

Enter Deep Sleep State:

1A) Turn on Power Isolation bit (ConfCtl.PWRISO = 1)
2A) Make sure there is no activity in TC9590XBG
3A) Turn on Sleep bit (SysCtl.SLEEP = 1)
4A) Shut down the CORE2 power on the board

Exit Deep Sleep State:

1B) Turn on the CORE2 power on the board
2B) Turn off Sleep bit (SysCtl.SLEEP = 0)
3B) Wait 1ms for PLL to lock
4B) Re-program all CSI2TX and HDMIRX registers
5B) Start operation

Note: Sleep State is entered by setting (SysCtl.SLEEP = 1 and ConfCtl.PWRISO = 0), during this state TC9590XBG keeps all its registers settings. Deep Sleep Mode is achieved by programming (SysCtl.SLEEP = 1 and ConfCtl.PWRISO = 1), Host is required to re-initiate TC9590XBG after exiting Deep Sleep State.

5.4. TC9590XBG Power Up Procedure

The following sequence should happen before TC9590XBG is able to operate properly:

1. Provide voltage and clock sources to TC9590XBG.
   - Please keep all the input signals at either “Hi-z” or “logic low” state before powering on TC9590XBG.
2. For voltage source, it is desired to turn on core power (1.2) source first, then Analog PHY and IO (1.8V) power as shown in Figure 5.3 Power On Sequence.
3. REFCLK clock source can be either 27/26 MHz or 42 MHz.
4. The timing parameters for Figure 5.3 are tabulated in Table 5-3.

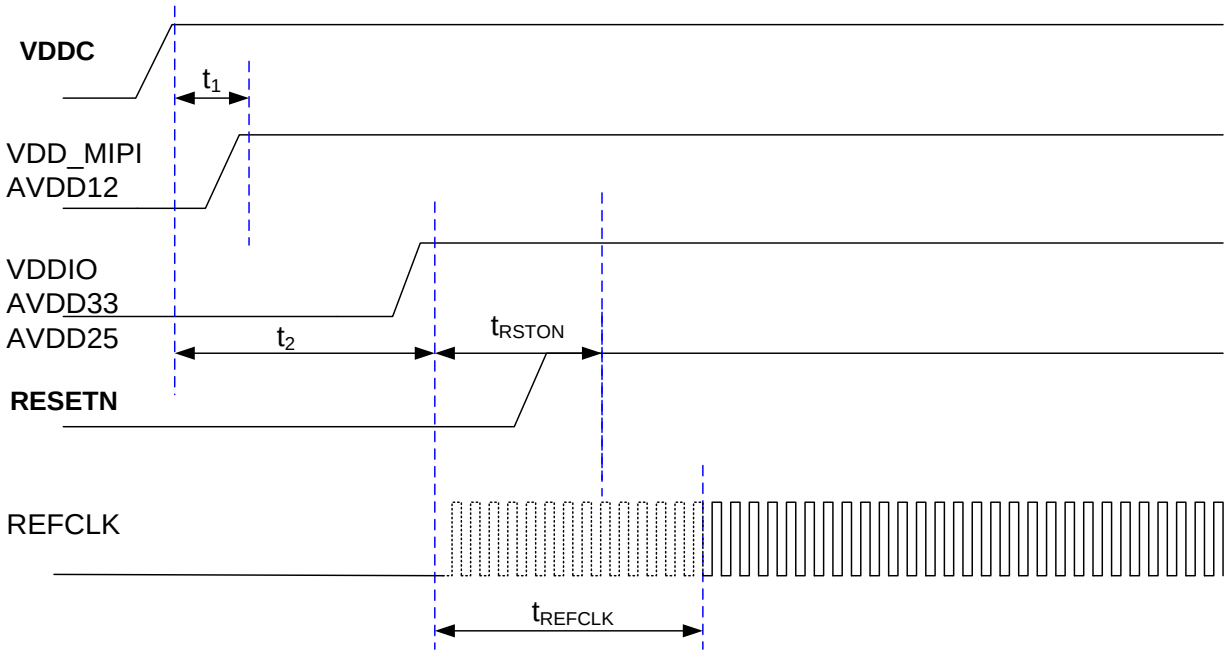


Figure 5.3 Power On Sequence

Table 5-3 Power On Sequence Timing

Parameters	Description	Min	Typ.	Max	Unit
RefClk	Reference clock frequency	26	---	42	MHz
t_1	VDD_MIPI, AVDD12 on delay from VDDC.	0	---	10	ms
t_2	VDDIO, AVDD33, AVDD25 on delay from VDDC	0	---	10	ms
t_{RSTON}	RESET width period	200	---	---	ns
T_{REFCLK}	RefClk can be applied only when VDDIO is asserted	0	---	---	ms

5.5. TC9590XBG Power Down Procedure

Figure 5.4 Power Down Sequence

Table 5-4 Power Down Sequence Timing

Parameters	Description	Min	Typ.	Max	Unit
t_1	VDDC off delay from VDDIO/AVDD33/AVDD25	0	---	10	ms
t_2	VDD_MIPI and AVDD12 off delay from VDDC off	0	---	10	ms

6. RegFile Block (Reg)

The application processor (ISP) accesses TC9590XBG RegFile block to read status and/or write control registers through the I^2C slave interface.

6.1. Register Map

The Overall I^2C Offset address map table is provided in below Tables.

Table 6-1 Global Register Map

Segment Address	Module
0x0000 – 0x00FF	Global Control Register
0x0100 – 0x01FF	CSI-2-TX PHY Register
0x0200 – 0x03FF	CSI-2-TX PPI Register
0x0400 – 0x05FF	Reserved
0x0600 – 0x06FF	CEC Register
0x0700 – 0x84FF	Reserved
0x8500 – 0x85FF	HDMIRX System Control Register
0x8600 – 0x86FF	HDMIRX Audio Control Register
0x8700 – 0x87FF	HDMIRX InfoFrame packet data Register
0x8800 – 0x88FF	HDMIRX HDCP Port Register Note: The LSB two bytes indicates the HDCP Offset Registers, e.g. 0x88_15 → HDCP Ainfo Register (x015)
0x8900 – 0x8BFF	Reserved
0x8C00 – 0x8FFF	HDMIRX EDID-RAM (1024 bytes)
0x9000 – 0x90FF	HDMIRX GBD Extraction Control
0x9100 – 0x92FF	HDMIRX GBD RAM read
0x9300 -	Reserved

Table 6-2 Detail Register Map

Group	Address	Register	Description
Global (16-bit addressable)	0x0000	ChipID	TC9590XBG Chip and Revision ID
	0x0002	SysCtl	System Control Register
	0x0004	ConfCtl	Configuration Control Register
	0x0006	FIFOCtl	FIFO Control Register
	0x0008	AWCnt	Audio Word Count Register
	0x000A	VWCnt	Video Word Count Register
	0x000C	PacketID1	Packet ID Register 1
	0x000E	PacketID2	Packet ID Register 2
	0x0010	PacketID3	Packet ID Register 3
	0x0012	FCCtl	Frame Count Ctrl Register
	0x0014	IntStatus	Interrupt Status Register
	0x0016	IntMask	Interrupt Mask Register
	0x0018	IntFlag	Interrupt Flag Register
	0x001A	IntSYSStatus	SYS Interrupt status register
	0x0020	PLLCtl0	PLL control Register 0
	0x0022	PLLCtl1	PLL control Register 1
	0x0028	CecHclk	CEC Clock High Time register
	0x002A	CecLclk	CEC Clock Low Time register
	0x002C	IrHclk	IR Clock High Time register
	0x002E	IrLclk	IR Clock Low Time register
	0x0034	LCHmin	IR Lead Code Hmin register
	0x0036	LCHmax	IR Lead Code HMax register
	0x0038	LCLmin	IR Lead Code LMin register
	0x003A	LCLmax	IR Lead Code LMax register
	0x003C	BHHmin	IR Bit “H” Hmin register
	0x003E	BHHmax	IR Bit “H” Hmax register
	0x0040	BHLmin	IR Bit “H” Lmin register
	0x0042	BHLmax	IR Bit “H” Lmax register
	0x0044	BLHmin	IR Bit “L” Hmin register
	0x0046	BLHmax	IR Bit “L” Hmax register
	0x0048	BLLmin	IR Bit “L” Lmin register
	0x004A	BLLmax	IR Bit “L” Lmax register
	0x004C	EndHmin	IR “END” Hmin register
	0x004E	EndHmax	IR “END” Hmax register
	0x0050	RCLmin	IR Repeat Code LMin register
	0x0052	RCLmax	IR Repeat Code LMax register
	0x0058	IRCtl	IR Control register
	0x005A	IRRData	IR Receive Data register
CSI-2 TX PHY/PPI (32-bit addressable)	0x0100	CLW_DPHYCONTTX	Clock Lane D-PHY Tx Control Register
	0x0104	D0W_DPHYCONTTX	Data Lane0 D-PHY Tx Control Register
	0x0108	D1W_DPHYCONTTX	Data Lane1 D-PHY Tx Control Register
	0x010C	D2W_DPHYCONTTX	Data Lane2 D-PHY Tx Control Register
	0x0110	D3W_DPHYCONTTX	Data Lane3 D-PHY Tx Control Register
	0x0140	CLW_CNTRL	Clock Lane D-PHY Control Register
	0x0144	D0W_CNTRL	Data Lane 0 D-PHY Control Register
	0x0148	D1W_CNTRL	Data Lane 1 D-PHY Control Register
	0x014C	D2W_CNTRL	Data Lane 2 D-PHY Control Register
	0x0150	D3W_CNTRL	Data Lane 3 D-PHY Control Register
	0x0204	STARTCNTRL	CSI2TX Start Control Register
	0x0208	STATUS	CSI2TX Status Register
	0x020C	Reserved	-
	0x0210	LINEINITCNT	CSI2TX Line Initialization Control Register
	0x0214	LPTXTIMECNT	SYSLPTX Timing Generation Counter
	0x0218	TCLK_HEADERCNT	TCLK_ZERO and TCLK_PREPARE Counter
	0x021C	TCLK_TRAILCNT	TCLK_TRAIL Counter

	0x0220	THS_HEADERCNT	THS_ZERO and THS_PREPARE Counter
	0x0224	TWAKEUP	TWAKEUP Counter
	0x0228	TCLK_POSTCNT	TCLK_POST Counter
	0x022C	THS_TRAILCNT	THS_TRAIL Counter
	0x0230	HSTXVREGCNT	TX Voltage Regulator setup Wait Counter
	0x0234	HSTXVREGEN	Voltage regulator enable for HSTX Data Lanes
	0x0238	TXOPTIONCNTRL	TX Option Control
TX CTRL (32-bit addressable)	0x040C	CSI_CONTROL	CSI2TX Control Register
	0x0410	CSI_STATUS	CSI2TX Status Register
	0x0414	CSI_INT	CSI2TX – Presents interrupts currently being held
	0x0418	CSI_INT_ENA	CSI2TX – Enables CSI_INT interrupt source
	0x044C	CSI_ERR	CSI2TX – transfer general errors
	0x0450	CSI_ERR_INTENA	CSI2TX – interrupt enable bits of the CSI_ERR register
	0x0454	CSI_ERR_HALT	CSI2TX – stop on error bit set in the CSI_ERR register
	0x0500	CSI_CONFW	CSI TX Configure Write Register
	0x0504	CSI_RESET	CSI2TX – reset he module and the Receive FIFO content
	0x050C	CSI_INT_CLR	CSI2TX – Clears particular bits of the CSI_INT register
	0x0518	CSI_START	CSI2-TX – Starts CSI-2-TX operation
CEC (32-bit addressable)	0x0600	CECEN	CEC Enable Register
	0x0604	CECADD	CEC Logical Address Register
	0x0608	CECRESET	CEC Reset Register
	0x060C	CECREN	CEC Receive Enable Register
	0x0610	--	Reserved
	0x0614	CECRCR1	CEC Receive Control Register 1
	0x0618	CECRCR2	CEC Receive Control Register 2
	0x061C	CECRCR3	CEC Receive Control Register 3
	0x0620	CECTEN	CEC Transmit Enable Register
	0x0628	CECTCR	CEC Transmit Control Register
	0x062C	CECRSTAT	Receive Interrupt Status Register
	0x0630	CECTSTAT	Transmit Interrupt Status Register
	0x0634	CECRBUF01	CEC Receive Buffer Register 1
	…	…	CEC Receive Buffer Register …
	0x0670	CECRBUF16	CEC Receive Buffer Register 16
	0x0674	CECTBUF01	CEC Transmit Buffer Register 1
	…	…	CEC Transmit Buffer Register …
	0x06B0	CECTBUF16	CEC Transmit Buffer Register 16
	0x06B4	CECRCTR	CEC Receive Byte Counter
	0x06B8	CECTESTR	CEC Test Purpose Register
	0x06C0	CECIMSC	CEC interrupt mask control register
	0x06CC	CECICR	CEC interrupt clear control register
	0x06D0 – 0x06FF	---	Reserved
IR (16-bit addressable)	0x07082	IR_CONTROL	IR Input Polarity Control
-	0x0700 – 0x84FF	Reserved	-
HDMIRX (8-bit addressable)	0x8500	HDMI_INT0	HDMI Interrupt 0
	0x8501	HDMI_INT1	HDMI Interrupt 1
	0x8502	SYS_INT	System Interrupt
	0x8503	CLK_INT	Clock Interrupt
	0x8504	PACKET_INT	Packet Interrupt
	0x8505	CBIT_INT	CBIT Interrupt
	0x8506	AUDIO_INT	AUDIO Interrupt
	0x8507	ERR_INT	ERROR Interrupt
	0x8508	HDCP_INT	HDCP Interrupt
	0x8509	GBD_INT	GBD Interrupt
	0x850b	MISC_INT	MISCELLANEOUS Interrupt

	0x850f	KEY_INT	KEY Interrupt
	0x8512	SYS_INTM	SYSTEM Interrupt Mask
	0x8513	CLK_INTM	CLOCK Interrupt Mask
	0x8514	PACKET_INTM	PACKET Interrupt Mask
	0x8515	CBIT_INTM	CBit Interrupt Mask
	0x8516	AUDIO_INTM	Audio Interrupt Mask
	0x8517	ERR_INTM	ERROR Interrupt Mask
	0x8518	HDCP_INTM	HDCP Interrupt Mask
	0x8519	GBD_INTM	GBD Interrupt Mask
	0x851b	MISC_INTM	MISCELLANEOUS Interrupt Mask
	0x851f	KEY_INTM	KEY Interrupt Mask
	0x8520	SYS_STATUS	SYS Status
	0x8521	VI_STATUS0	Input Video Signal Status 0
	0x8522	VI_STATUS1	Input Video Signal Status 1
	0x8523	AU_STATUS0	AUDIO Status 0
	0x8524	AU_STATUS1	AUDIO Status 1
	0x8525	VI_STATUS2	Input Video Signal Status 2
	0x8526	CLK_STATUS	CLOCK Status
	0x8527	PHYERR_STATUS	PHY ERROR Status
	0x8528	VI_STATUS3	Input Video Signal Status 3
	0x8531	PHY_CTL0	PHY Control 0
	0x8534	PHY_EN	PHY Enable
	0x8535	PHY_RST	PHY Reset
	0x8538	PHY_PLL	PHY PLL
	0x853a	PHY_CDR	PHY CDR
	0x8540	SYS_FREQ0	SYS FREQ0 Register
	0x8541	SYS_FREQ1	SYS FREQ1 Register
	0x8543	DDC_CTL	DDC Control
	0x8544	HPD_CTL	HPD Control
	0x8545	ANA_CTL	ANA Control
	0x8546	AVM_CTL	AVMUTE Control
	0x8547	SOFT_RST	Software Reset
	0x854A	INIT_END	INIT END
	0x8550	HDMI_DVI	HDMI ←→ DVI transition Detection Control
	0x8560	HDCP_MODE	HDCP Operation Mode
	0x8561	HDCP_CMD	HDCP Command
	0x8570	VI_MODE	VI MODE Register
	0x8573	VOUT_SET2	VOUT_SET2
	0x8574	VOUT_SET3	VOUT_SET3
	0x8576	VI_REP	VOUT Color Setting
	0x8577	DC_MODE	DC MODE Register
	0x85C7	EDID_MODE	EDID_MODE
	0x85C8	EDID_SLV	EDID_SLV
	0x85C9	EDID_OFF	EDID_OFF
	0x85CA	EDID_LEN1	EDID_LEN1
	0x85CB	EDID_LEN2	EDID_LEN2
	0x85CC	EDID_CMD	EDID_CMD
	-		
	0x8600	FORCE_MUTE	FORCE MUTE
	0x8601	CMD_AUD	CMD AUD
	0x8602	AUTO_CMD0	Audio Auto Mute
	0x8603	AUTO_CMD1	Audio Auto Mute
	0x8604	AUTO_CMD2	Audio Auto Play
	0x8606	BUFINIT_START	Audio Buffer Init. Start time
	0x8607	FS_MUTE	Audio Sample MUTE
	0x8608	MUTE_MODE	Audio Mute Mode
	0x8620	FS_IMODE	Audio Sample Frequency Input Mode
	0x8621	FS_SET	Audio Sample Frequency Mode
	0x8622	CBIT_BYTE0	Channel Status bits [7:0]
	0x8623	CBIT_BYTE1	Channel Status bits [15:8]

	0x8624	CBIT_BYTE2	Channel Status bits [23:16]
	0x8625	CBIT_BYTE3	Channel Status bits [31:24]
	0x8626	CBIT_BYTE4	Channel Status bits [39:32]
	0x8627	CBIT_BYTE5	Channel Status bits [47:40]
	0x8630	LOCKDET_REF0	RefClk Cycle numbers [7:0] for 10 ms
	0x8631	LOCKDET_REF1	RefClk Cycle numbers [15:8] for 10 ms
	0x8632	LOCKDET_REF2	RefClk Cycle numbers [19:16] for 10 ms
	0x8640	ACR_MODE	CTS Adjustment Mode
	0x8641	ACR_MDF0	CTS Adjustment Amount0
	0x8642	ACR_MDF1	CTS Adjustment Amount1
	0x8651	SDO_MODE0	SDO_MODE0
	0x8652	SDO_MODE1	SDO_MODE1
	0x8670	NCO_F0_MOD	Audio PLL Setting Register
	0x8690	APIN_ENO	Audio Output Module Terminal Control
	-		
	0x8701	TYP_VS_SET	VS_info Packet Type code setting
	0x8702	TYP_AVI_SET	AVI_info Packet Type code setting
	0x8703	TYP_SPD_SET	SPD_info Packet Type code setting
	0x8704	TYP_AUD_SET	AUD_info Packet Type code setting
	0x8705	TYP_MS_SET	MS_info Packet Type code setting
	0x8706	TYP_ACP_SET	ACP Packet Type code setting
	0x8707	TYP_ISRC1_SET	ISRC1 Packet Type code setting
	0x8708	TYP_ISRC2_SET	ISRC2 Packet Type code setting
	0x8709	PK_INT_MODE	Packet Interrupt Mode
	0x870a	PK_AUTO_CLR	Packet Auto Clear
	0x870b	NO_PK_LIMIT	No Packet Limit
	0x870c	NO_PK_CLR	No Packet Clear
	0x870d	ERR_PK_LIMIT	Error Packet Limit
	0x870e	NO_PK_LIMIT2	No Packet Limit 2
	0x870f	VS_IEEE_SEL	VS IEEE Select
	0x8710	PK_AVI_0HEAD	861B AVI_info packet Header byte 0
	0x8711	PK_AVI_1HEAD	861B AVI_info packet Header byte 1
	0x8712	PK_AVI_2HEAD	861B AVI_info packet Header byte 2
	0x8713	PK_AVI_0BYTE	861B AVI_info packet Data byte 0
	0x8714	PK_AVI_1BYTE	861B AVI_info packet Data byte 1
	0x8715	PK_AVI_2BYTE	861B AVI_info packet Data byte 2
	0x8716	PK_AVI_3BYTE	861B AVI_info packet Data byte 3
	0x8717	PK_AVI_4BYTE	861B AVI_info packet Data byte 4
	0x8718	PK_AVI_5BYTE	861B AVI_info packet Data byte 5
	0x8719	PK_AVI_6BYTE	861B AVI_info packet Data byte 6
	0x871a	PK_AVI_7BYTE	861B AVI_info packet Data byte 7
	0x871b	PK_AVI_8BYTE	861B AVI_info packet Data byte 8
	0x871c	PK_AVI_9BYTE	861B AVI_info packet Data byte 9
	0x871d	PK_AVI_10BYTE	861B AVI_info packet Data byte 10
	0x871e	PK_AVI_11BYTE	861B AVI_info packet Data byte 11
	0x871f	PK_AVI_12BYTE	861B AVI_info packet Data byte 12
	0x8720	PK_AVI_13BYTE	861B AVI_info packet Data byte 13
	0x8721	PK_AVI_14BYTE	861B AVI_info packet Data byte 14
	0x8722	PK_AVI_15BYTE	861B AVI_info packet Data byte 15
	0x8723	PK_AVI_16BYTE	861B AVI_info packet Data byte 16
	0x8730	PK_AUD_0HEAD	861B AUD_info packet Header byte 0
	0x8731	PK_AUD_1HEAD	861B AUD_info packet Header byte 1
	0x8732	PK_AUD_2HEAD	861B AUD_info packet Header byte 2
	0x8733	PK_AUD_0BYTE	861B AUD_info packet Data byte 0
	0x8734	PK_AUD_1BYTE	861B AUD_info packet Data byte 1
	0x8735	PK_AUD_2BYTE	861B AUD_info packet Data byte 2
	0x8736	PK_AUD_3BYTE	861B AUD_info packet Data byte 3
	0x8737	PK_AUD_4BYTE	861B AUD_info packet Data byte 4
	0x8738	PK_AUD_5BYTE	861B AUD_info packet Data byte 5
	0x8739	PK_AUD_6BYTE	861B AUD_info packet Data byte 6

	0x873a	PK_AUD_7BYTE	861B AUD_info packet Data byte 7
	0x873b	PK_AUD_8BYTE	861B AUD_info packet Data byte 8
	0x873c	PK_AUD_9BYTE	861B AUD_info packet Data byte 9
	0x873d	PK_AUD_10BYTE	861B AUD_info packet Data byte 10
	0x8740	PK_MS_0HEAD	861B MS_info packet Header byte 0
	0x8741	PK_MS_1HEAD	861B MS_info packet Header byte 1
	0x8742	PK_MS_2HEAD	861B MS_info packet Header byte 2
	0x8743	PK_MS_0BYTE	861B MS_info packet Data byte 0
	0x8744	PK_MS_1BYTE	861B MS_info packet Data byte 1
	0x8745	PK_MS_2BYTE	861B MS_info packet Data byte 2
	0x8746	PK_MS_3BYTE	861B MS_info packet Data byte 3
	0x8747	PK_MS_4BYTE	861B MS_info packet Data byte 4
	0x8748	PK_MS_5BYTE	861B MS_info packet Data byte 5
	0x8749	PK_MS_6BYTE	861B MS_info packet Data byte 6
	0x874a	PK_MS_7BYTE	861B MS_info packet Data byte 7
	0x874b	PK_MS_8BYTE	861B MS_info packet Data byte 8
	0x874c	PK_MS_9BYTE	861B MS_info packet Data byte 9
	0x874d	PK_MS_10BYTE	861B MS_info packet Data byte 10
	0x8750	PK_SPD_0HEAD	861B SPD_info packet Header byte 0
	0x8751	PK_SPD_1HEAD	861B SPD_info packet Header byte 1
	0x8752	PK_SPD_2HEAD	861B SPD_info packet Header byte 2
	0x8753	PK_SPD_0BYTE	861B SPD_info packet Data byte 0
	0x8754	PK_SPD_1BYTE	861B SPD_info packet Data byte 1
	0x8755	PK_SPD_2BYTE	861B SPD_info packet Data byte 2
	0x8756	PK_SPD_3BYTE	861B SPD_info packet Data byte 3
	0x8757	PK_SPD_4BYTE	861B SPD_info packet Data byte 4
	0x8758	PK_SPD_5BYTE	861B SPD_info packet Data byte 5
	0x8759	PK_SPD_6BYTE	861B SPD_info packet Data byte 6
	0x875a	PK_SPD_7BYTE	861B SPD_info packet Data byte 7
	0x875b	PK_SPD_8BYTE	861B SPD_info packet Data byte 8
	0x875c	PK_SPD_9BYTE	861B SPD_info packet Data byte 9
	0x875d	PK_SPD_10BYTE	861B SPD_info packet Data byte 10
	0x875e	PK_SPD_11BYTE	861B SPD_info packet Data byte 11
	0x875f	PK_SPD_12BYTE	861B SPD_info packet Data byte 12
	0x8760	PK_SPD_13BYTE	861B SPD_info packet Data byte 13
	0x8761	PK_SPD_14BYTE	861B SPD_info packet Data byte 14
	0x8762	PK_SPD_15BYTE	861B SPD_info packet Data byte 15
	0x8763	PK_SPD_16BYTE	861B SPD_info packet Data byte 16
	0x8764	PK_SPD_17BYTE	861B SPD_info packet Data byte 17
	0x8765	PK_SPD_18BYTE	861B SPD_info packet Data byte 18
	0x8766	PK_SPD_19BYTE	861B SPD_info packet Data byte 19
	0x8767	PK_SPD_20BYTE	861B SPD_info packet Data byte 20
	0x8768	PK_SPD_21BYTE	861B SPD_info packet Data byte 21
	0x8769	PK_SPD_22BYTE	861B SPD_info packet Data byte 22
	0x876a	PK_SPD_23BYTE	861B SPD_info packet Data byte 23
	0x876b	PK_SPD_24BYTE	861B SPD_info packet Data byte 24
	0x876c	PK_SPD_25BYTE	861B SPD_info packet Data byte 25
	0x876d	PK_SPD_26BYTE	861B SPD_info packet Data byte 26
	0x876e	PK_SPD_27BYTE	861B SPD_info packet Data byte 27
	0x8770	PK_VS_0HEAD	861B VS_info packet Header byte 0
	0x8771	PK_VS_1HEAD	861B VS_info packet Header byte 1
	0x8772	PK_VS_2HEAD	861B VS_info packet Header byte 2
	0x8773	PK_VS_0BYTE	861B VS_info packet Data byte 0
	0x8774	PK_VS_1BYTE	861B VS_info packet Data byte 1
	0x8775	PK_VS_2BYTE	861B VS_info packet Data byte 2
	0x8776	PK_VS_3BYTE	861B VS_info packet Data byte 3
	0x8777	PK_VS_4BYTE	861B VS_info packet Data byte 4
	0x8778	PK_VS_5BYTE	861B VS_info packet Data byte 5
	0x8779	PK_VS_6BYTE	861B VS_info packet Data byte 6
	0x877a	PK_VS_7BYTE	861B VS_info packet Data byte 7

	0x877b	PK_VS_8BYTE	861B VS_info packet Data byte 8
	0x877c	PK_VS_9BYTE	861B VS_info packet Data byte 9
	0x877d	PK_VS_10BYTE	861B VS_info packet Data byte 10
	0x877e	PK_VS_11BYTE	861B VS_info packet Data byte 11
	0x877f	PK_VS_12BYTE	861B VS_info packet Data byte 12
	0x8780	PK_VS_13BYTE	861B VS_info packet Data byte 13
	0x8781	PK_VS_14BYTE	861B VS_info packet Data byte 14
	0x8782	PK_VS_15BYTE	861B VS_info packet Data byte 15
	0x8783	PK_VS_16BYTE	861B VS_info packet Data byte 16
	0x8784	PK_VS_17BYTE	861B VS_info packet Data byte 17
	0x8785	PK_VS_18BYTE	861B VS_info packet Data byte 18
	0x8786	PK_VS_19BYTE	861B VS_info packet Data byte 19
	0x8787	PK_VS_20BYTE	861B VS_info packet Data byte 20
	0x8788	PK_VS_21BYTE	861B VS_info packet Data byte 21
	0x8789	PK_VS_22BYTE	861B VS_info packet Data byte 22
	0x878a	PK_VS_23BYTE	861B VS_info packet Data byte 23
	0x878b	PK_VS_24BYTE	861B VS_info packet Data byte 24
	0x878c	PK_VS_25BYTE	861B VS_info packet Data byte 25
	0x878d	PK_VS_26BYTE	861B VS_info packet Data byte 26
	0x878e	PK_VS_27BYTE	861B VS_info packet Data byte 27
	0x8790	PK_ACP_0HEAD	861B ACP_info packet Header byte 0
	0x8791	PK_ACP_1HEAD	861B ACP_info packet Header byte 1
	0x8792	PK_ACP_2HEAD	861B ACP_info packet Header byte 2
	0x8793	PK_ACP_0BYTE	861B ACP_info packet Data byte 0
	0x8794	PK_ACP_1BYTE	861B ACP_info packet Data byte 1
	0x8795	PK_ACP_2BYTE	861B ACP_info packet Data byte 2
	0x8796	PK_ACP_3BYTE	861B ACP_info packet Data byte 3
	0x8797	PK_ACP_4BYTE	861B ACP_info packet Data byte 4
	0x8798	PK_ACP_5BYTE	861B ACP_info packet Data byte 5
	0x8799	PK_ACP_6BYTE	861B ACP_info packet Data byte 6
	0x879a	PK_ACP_7BYTE	861B ACP_info packet Data byte 7
	0x879b	PK_ACP_8BYTE	861B ACP_info packet Data byte 8
	0x879c	PK_ACP_9BYTE	861B ACP_info packet Data byte 9
	0x879d	PK_ACP_10BYTE	861B ACP_info packet Data byte 10
	0x879e	PK_ACP_11BYTE	861B ACP_info packet Data byte 11
	0x879f	PK_ACP_12BYTE	861B ACP_info packet Data byte 12
	0x87a0	PK_ACP_13BYTE	861B ACP_info packet Data byte 13
	0x87a1	PK_ACP_14BYTE	861B ACP_info packet Data byte 14
	0x87a2	PK_ACP_15BYTE	861B ACP_info packet Data byte 15
	0x87a3	PK_ACP_16BYTE	861B ACP_info packet Data byte 16
	0x87a4	PK_ACP_17BYTE	861B ACP_info packet Data byte 17
	0x87a5	PK_ACP_18BYTE	861B ACP_info packet Data byte 18
	0x87a6	PK_ACP_19BYTE	861B ACP_info packet Data byte 19
	0x87a7	PK_ACP_20BYTE	861B ACP_info packet Data byte 20
	0x87a8	PK_ACP_21BYTE	861B ACP_info packet Data byte 21
	0x87a9	PK_ACP_22BYTE	861B ACP_info packet Data byte 22
	0x87aa	PK_ACP_23BYTE	861B ACP_info packet Data byte 23
	0x87ab	PK_ACP_24BYTE	861B ACP_info packet Data byte 24
	0x87ac	PK_ACP_25BYTE	861B ACP_info packet Data byte 25
	0x87ad	PK_ACP_26BYTE	861B ACP_info packet Data byte 26
	0x87ae	PK_ACP_27BYTE	861B ACP_info packet Data byte 27
	0x87b0	PK_ISRC1_0HEAD	861B ISRC1_info packet Header byte 0
	0x87b1	PK_ISRC1_1HEAD	861B ISRC1_info packet Header byte 1
	0x87b2	PK_ISRC1_2HEAD	861B ISRC1_info packet Header byte 2
	0x87b3	PK_ISRC1_0BYTE	861B ISRC1_info packet Data byte 0
	0x87b4	PK_ISRC1_1BYTE	861B ISRC1_info packet Data byte 1
	0x87b5	PK_ISRC1_2BYTE	861B ISRC1_info packet Data byte 2
	0x87b6	PK_ISRC1_3BYTE	861B ISRC1_info packet Data byte 3
	0x87b7	PK_ISRC1_4BYTE	861B ISRC1_info packet Data byte 4
	0x87b8	PK_ISRC1_5BYTE	861B ISRC1_info packet Data byte 5

	0x87b9	PK_ISRC1_6BYTE	861B ISRC1_info packet Data byte 6
	0x87ba	PK_ISRC1_7BYTE	861B ISRC1_info packet Data byte 7
	0x87bb	PK_ISRC1_8BYTE	861B ISRC1_info packet Data byte 8
	0x87bc	PK_ISRC1_9BYTE	861B ISRC1_info packet Data byte 9
	0x87bd	PK_ISRC1_10BYTE	861B ISRC1_info packet Data byte 10
	0x87be	PK_ISRC1_11BYTE	861B ISRC1_info packet Data byte 11
	0x87bf	PK_ISRC1_12BYTE	861B ISRC1_info packet Data byte 12
	0x87c0	PK_ISRC1_13BYTE	861B ISRC1_info packet Data byte 13
	0x87c1	PK_ISRC1_14BYTE	861B ISRC1_info packet Data byte 14
	0x87c2	PK_ISRC1_15BYTE	861B ISRC1_info packet Data byte 15
	0x87d0	PK_ISRC2_0HEAD	861B ISRC2_info packet Header byte 0
	0x87d1	PK_ISRC2_1HEAD	861B ISRC2_info packet Header byte 1
	0x87d2	PK_ISRC2_2HEAD	861B ISRC2_info packet Header byte 2
	0x87d3	PK_ISRC2_0BYTE	861B ISRC2_info packet Data byte 0
	0x87d4	PK_ISRC2_1BYTE	861B ISRC2_info packet Data byte 1
	0x87d5	PK_ISRC2_2BYTE	861B ISRC2_info packet Data byte 2
	0x87d6	PK_ISRC2_3BYTE	861B ISRC2_info packet Data byte 3
	0x87d7	PK_ISRC2_4BYTE	861B ISRC2_info packet Data byte 4
	0x87d8	PK_ISRC2_5BYTE	861B ISRC2_info packet Data byte 5
	0x87d9	PK_ISRC2_6BYTE	861B ISRC2_info packet Data byte 6
	0x87da	PK_ISRC2_7BYTE	861B ISRC2_info packet Data byte 7
	0x87db	PK_ISRC2_8BYTE	861B ISRC2_info packet Data byte 8
	0x87dc	PK_ISRC2_9BYTE	861B ISRC2_info packet Data byte 9
	0x87dd	PK_ISRC2_10BYTE	861B ISRC2_info packet Data byte 10
	0x87de	PK_ISRC2_11BYTE	861B ISRC2_info packet Data byte 11
	0x87df	PK_ISRC2_12BYTE	861B ISRC2_info packet Data byte 12
	0x87e0	PK_ISRC2_13BYTE	861B ISRC2_info packet Data byte 13
	0x87e1	PK_ISRC2_14BYTE	861B ISRC2_info packet Data byte 14
	0x87e2	PK_ISRC2_15BYTE	861B ISRC2_info packet Data byte 15
	0x87e3	PK_ISRC2_16BYTE	861B ISRC2_info packet Data byte 16
	0x87e4	PK_ISRC2_17BYTE	861B ISRC2_info packet Data byte 17
	0x87e5	PK_ISRC2_18BYTE	861B ISRC2_info packet Data byte 18
	0x87e6	PK_ISRC2_19BYTE	861B ISRC2_info packet Data byte 19
	0x87e7	PK_ISRC2_20BYTE	861B ISRC2_info packet Data byte 20
	0x87e8	PK_ISRC2_21BYTE	861B ISRC2_info packet Data byte 21
	0x87e9	PK_ISRC2_22BYTE	861B ISRC2_info packet Data byte 22
	0x87ea	PK_ISRC2_23BYTE	861B ISRC2_info packet Data byte 23
	0x87eb	PK_ISRC2_24BYTE	861B ISRC2_info packet Data byte 24
	0x87ec	PK_ISRC2_25BYTE	861B ISRC2_info packet Data byte 25
	0x87ed	PK_ISRC2_26BYTE	861B ISRC2_info packet Data byte 26
	0x87ee	PK_ISRC2_27BYTE	861B ISRC2_info packet Data byte 27
	0x8840	BCaps	HDCP Rx BCap Registers
	0x8841	BStatus0	HDCP Rx BStatu0
	0x8842	BStatus1	HDCP Rx BStatu0
	0x8843	KSVFIFO	HDCP Rx KSVFIFO Register

Note:

1) HDMI registers are 8-bit register.
2) CEC registers are 32-bit register. Host must write two consecutive 16-bit register write to form 32-bit access.

The following sections provide a detailed description of the registers.

6.2. Global

6.2.1. Chip and Revision ID (ChipID: 0x0000)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	ChipID							
Type	RO							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	RevID							
Type	RO							
Default	0x0							

Register Field	Bit	Description
ChipID	[15:8]	**Chip ID** Chip ID assigned for this device by Toshiba.
RevID	[7:0]	**Revision ID** Revision ID for this device assigned by Toshiba.

6.2.2. System Control Register (SysCtl: 0x0002)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				IRRst	CecRst	CTxRst	HdmiRst
Type	RO				R/W	R/W	R/W	R/W
Default	0x0				0x0	0x0	0x0	0x0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							SLEEP
Type	RO							R/W
Default	0x0							0x1

Register Field	Bit	Description
Reserved	[15:12]	-
IRRst	[11]	**IR Software Reset (Active high)** This bit is set to force IR logic to reset state only, the configuration registers are not affected 0: Normal operation 1: Reset operation Software needs to clear IRReset when set.
CecRst	[10]	**CEC Software Reset (Active high)** This bit is set to force CEC logic and its configuration registers to reset 0: Normal operation 1: Reset operation Software needs to clear CECReset when set.
CTxRst	[9]	**CSI-2-TX Software Reset (Active high)** This bit is set to force CEC logic and its configuration registers to reset. 0: Normal operation 1: Reset operation Software needs to clear CReset when set.
HdmiRst	[8]	**HDMI-RX Software Reset (Active high)** This bit is set to force CEC logic and its configuration registers to reset. 0: Normal operation 1: Reset operation Software needs to clear HdmiRst when set.
Reserved	[7:1]	-
SLEEP	[0]	**SLEEP** control 0: Normal operation 1: Sleep mode

6.2.3. Configuration Control Register (ConfCtl: 0x0004)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	PWRISO	Reserved		AClkOpt	AudChNum		AudChSel	I2SDlyOpt
Type	R/W	RO		R/W	R/W		R/W	R/W
Default	0x0	0x0		0x0	0x0		0x0	0x0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	YCbCrFmt		InFrmEn	AudOutSel		AutoIndex	ABufEn	VBufEn
Type	R/W		R/W	R/W		R/W	R/W	R/W
Default	0x0		0x0	0x0		0x0	0x0	0x0

Register Field	Bit	Description
PWRISO	[15]	**Power Island Enable** 1'b0: Normal 1'b1: Power Island Enable To be work with SysCtl.SLEEP, please refer to section 5.3
Reserved	[14:13]	-
AClkOpt	[12]	**Audio Bit Clock Option** 1'b0: I2S/TDM clock are free running 1'b1: I2S/TDM clock stops when Mute active
AudChNum	[11:10]	**Audio Channel Output Channels** 2'b00: Enable 8 Audio channels 2'b01: Enable 6 Audio channels 2'b10: Enable 4 Audio channels 2'b11: Enable 2 Audio channels Note: valid only AudChSel = 1
AudChSel	[9]	**Audio Channel Number Selection Mode** 1'b0: Auto detect by HW 1'b1: Select by AudChNum register bits Note: valid only when AudOutSel[4] = 0
I2SDlyOpt	[8]	**I2S/TDM Data Delay Option** 1'b0: No delay 1'b1: Delay by 1 clock
YCbCrFmt	[7:6]	**YCbCr Video Output Format select** 2'b00: Select YCbCr444 data format, Data Type 0x24 is used 2'b01: Select YCbCr422 24bpp data format, Data Type is specified in register PacketID3[VPID2] 2'b10: Internal Generated output pattern, e.g. ColorBar, Data Type is programmed in register field PacketID3[VPID2], independent of data format 2'b11: Select YCbCr422 16bpp (HDMI YCbCr422 24bpp data format, discard last 4 data bits), Data Type = 0x1E as specified in CSI-2 specification Note: RGB data, this field has to be set to 2'b00
InFrmEn	[5]	**InfoFrame Data enable** 1'b0: Do not send InfoFrame data out to CSI-2 1'b1: Send InfoFrame data out to CSI-2
AudOutSel	[4:3]	**Audio Output option** 2'b00: Audio output to CSI-2-TX i/f 2'b01: Reserved 2'b10: Audio output to I2S i/f (valid for 2 channel only) 2'b11: Audio output to TDM i/f Note: When HDMI source output more than 2 Audio channels, automatic select TDM i/f if AudOutSel[4] = 1.
AutoIndex	[2]	**I2C slave index increment**

Register Field	Bit	Description
		1'b0: I2C address index does not increment on every data byte transfer 1'b1: I2C address index increments on every data byte transfer
ABufEn	[1]	**Audio TX Buffer Enable** 1'b0: disable 1'b1: enable Note: enable only after HDMIRX and CSITX register have been setup.
VBufEn	[0]	**Video TX Buffer Enable** 1'b0: disable 1'b1: enable Note: enable only after HDMIRX and CSITX register have been setup.

6.2.4. FIFO Control Register (FIFOCtl: 0x0006)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							FIFOLevel[8]
Type	RO							R/W
Default	0x0							0x0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	FIFOLevel[7:0]							
Type	R/W							
Default	0x10							

Register Field	Bit	Description
Reserved	[15:9]	Reserved
FIFOLevel	[8:0]	**FIFOLevel** This field determines video delay from FiFo level, when reaches to this level FiFo controller asserts FiFoRdy for CSI-2-TX controller to start output

6.2.5. Audio Word Count Register (AWCnt: 0x0008)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved	AWcnt2[6:0]						
Type	RO	R/W						
Default	0x0	0x5F						
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved	AWcnt1[6:0]						
Type	RO	R/W						
Default	0x0	0x5F						

Register Field	Bit	Description
Reserved	[15]	Reserved
AWCnt2	[14:8]	**Audio Word Count 2 (used for 6 Audio channels)** 6'h0: Reserved 6'h1-127: Audio Byte count (2-128)to be send over CSI Note: Recommend setting is multiple of 24 byte. Best setting is either 24, 48, 72, 96 or 120 count Note: Value must be multiple of 4 bytes
Reserved	[7]	-

Register Field	Bit	Description
AWCnt1	[6:0]	**Audio Word Count 1 (used for 2, 4, 8 Audio channels)** 6'h0: Reserved 6'h1-127: Audio Byte count (2-128)to be send over CSI Note: Recommend setting is multiple of 32 byte. Best setting is either 32, 64, 96 or 128 count Note: Value must be multiple of 4 bytes

6.2.6. Video Data Word Count Register (VWCnt: 0x000A)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	VWordCnt[15:8]							
Type	R/W							
Default	0x01							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	VWordCnt[7:0]							
Type	R/W							
Default	0x00							

Register Field	Bit	Description
VWordCnt	[15:0]	**Video Data Word Count** Defined total number of byte for each line. **For testing only**

6.2.7. Packet ID Register 1 (PacketID1: 0x000C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	VPID1							
Type	R/W							
Default	0x34							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	VPID0							
Type	R/W							
Default	0x35							

Register Field	Bit	Description
VPID1	[15:8]	CSI Video Packet ID 1 Note: For interlace mode only, this ID is for Bottom video field.
VPID0	[7:0]	CSI Video Packet ID 0 Note: For interlace mode only, this ID is for Top video field

6.2.8. Packet ID Register 2 (PacketID2: 0x000E)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	IFPID							
Type	R/W							
Default	0x36							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	APID							
Type	R/W							
Default	0x37							

Register Field	Bit	Description
IFPID	[15:8]	CSI InfoFrame Packet ID
APID	[7:0]	CSI Audio Packet ID

6.2.9. Packet ID Register 3 (PacketID3: 0x0010)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VPID2							
Type	R/W							
Default	0x24							

Register Field	Bit	Description
Reserved	[15:8]	-
VPID2	[7:0]	CSI Video Packet ID Note: Use when YCbCrFmt[1:0] = 2'b01 or YCbCrFmt[1:0] = 2'b10

6.2.10. Frame Count Control Register (FCCtl: 0x0012)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	FrCnt							
Type	R/W							
Default	0x00							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	FrCnt							
Type	R/W							
Default	0x00							

Register Field	Bit	Description
FrCnt	[15:0]	Frame Count Control Register 16'h0000: Disable Frame Count 16'h0001: Count 1,1,1,1,1, 16'h0002: Count 1,2,1,2,1,2,1,2,…. 16'h0003: Count 1,2,3,1,2,3,….. 16'h0004: Count 1,2,3,4,1,2,3,4,1,2,3,4,…. Note: Increment on every HDMI Vsync. "Frame Start" and "Frame End" packet have the same FrameCount number.

6.2.11. Interrupt Status Register (IntStatus: 0x0014)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved					AMUTE_INT	HDMI_INT	CSI_INT
Type	RO					W1C/R	W1C/R	W1C/R
Default	0x0					0x0	0x0	0x0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved		SYS_INT	CEC_EINT	CEC_TINT	CEC_RINT	IR_EINT	IR_DINT
Type	RO		W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R
Default	0x0		0x0	0x0	0x0	0x0	0x0	0x0

Register Field	Bit	Description
Reserved	[15:11]	-
AMUTE_INT	[10]	Audio Mute Interrupt Status 1'b0: Normal 1'b1: Audio change from Normal to Mute
HDMI_INT	[9]	HDMI-RX Interrupt Status Note: all HDMI interrupt flags defined in HDMI register space
CSI_INT	[8]	CSI-2-TX Interrupt Status
Reserved	[7:6]	-
SYS_INT	[5]	TC9590XBG System Interrupt Status 1'b0: Normal 1'b1: Video/Audio Overflow/Underflow/WakeUp occurs
CEC_EINT	[4]	CEC Error Interrupt Status 1'b0: Normal 1'b1: CEC Errors occurs
CEC_TINT	[3]	CEC Transmit Interrupt Status 1'b0: Idle 1'b1: Transmit completed/done
CEC_RINT	[2]	CEC Receive Interrupt Status 1'b0: Idle 1'b1: Data Received
IR_EINT	[1]	IR Error Interrupt Status 1'b0: No Error 1'b1: Error occurs (overflow error)
IR_DINT	[0]	IR Data Interrupt Status 1'b0: Idle 1'b1: Interrupt occurs (IR Data available)

Note: Write "1" to clear Interrupt. Interrupt is only active when INT_MASK = 1'b0.

6.2.12. Interrupt Mask Register (IntMask: 0x0016)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved					AMUTE_MSK	HDMI_MSK	CSI_MSK
Type	RO					R/W	R/W	R/W
Default	0x0					0x1	0x0	0x0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved		SYS_MSK	CEC_EMSK	CEC_TMSK	CEC_RMSK	IR_EMSK	IR_DMSK
Type	RO		R/W	R/W	R/W	R/W	R/W	R/W
Default	0x0		0x0	0x0	0x0	0x0	0x0	0x0

Register Field	Bit	Description
Reserved	[15:11]	-
AMUTE_MSK	[10]	Audio Mute Interrupt Mask
HDMI_MSK	[9]	HDMI-RX Interrupt Mask
CSI_MSK	[8]	CSI-2-TX Interrupt Mask
Reserved	[7:6]	-
SYS_MSK	[5]	SYS Interrupt Mask
CEC_EMSK	[4]	CEC Error Interrupt Mask
CEC_TMSK	[3]	CEC Transmit Interrupt Mask
CEC_RMSK	[2]	CEC Receive Interrupt Mask
IR_EMSK	[1]	IR Error Interrupt Mask
IR_DMSK	[0]	IR Data Interrupt Mask 1'b0: Enable Interrupt 1'b1: Mask Interrupt

Note: if *MSK = 1'b1 then *INT is never asserted.

6.2.13. Interrupt Flag Register (IntFlag: 0x0018)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved					AMUTE_FLG	HDMI_FLG	CSI_FLG
Type	RO					RO	RO	RO
Default	0x0					0x0	0x0	0x0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved		SYS_FLG	CEC_EFLG	CEC_TFLG	CEC_RFLG	IR_EFLG	IR_DFLG
Type	RO		RO	RO	RO	RO	RO	RO
Default	0x0		0x0	0x0	0x0	0x0	0x0	0x0

Register Field	Bit	Description
Reserved	[15:11]	-
AMUTE_FLG	[10]	Audio Mute Interrupt Flag
HDMI_FLG	[9]	HDMI-RX Interrupt Flag
CSI_FLG	[8]	CSI-2-TX Interrupt Flag
Reserved	[7:6]	-
SYS_FLG	[5]	SYS Interrupt Flag
CEC_EFLG	[4]	CEC Error Interrupt Flag
CEC_TFLG	[3]	CEC Transmit Interrupt Flag
CEC_RFLG	[2]	CEC Receive Interrupt Flag
IR_EFLG	[1]	IR Error Interrupt Flag
IR_DFLG	[0]	IR Data Interrupt Flag 1'b0: Idle 1'b1: Interrupt occurs (Data available)

Note: *MASK does not affect these flag status.

6.2.14. SYS Interrupt Status Register (IntSYSStatus: 0x001A)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved			HPI_chg	DDC_act	Ab_ofl	Vb_ufl	Vb_ofl
Type	RO			RO	RO	RO	RO	RO
Default	0x0			0x0	0x0	0x0	0x0	0x0

Register Field	Bit	Description
Reserved	[15:5]	-
HPI_chg	[4]	HPDI status 0: Normal 1: change Note: only valid during sleep mode with Power Island Enable (Deep Sleep mode), use to wake up the host when HDPI is changing.
DDC_act	[3]	DDC interface status 0: idle 1: DDC active Note: (1) only valid during sleep mode with Power Island Enable (Deep Sleep mode), use to wake up the host when DDC interface is active. (2) Host should clear this status only if it finished re-program all the TC9590XBG HDMI/CSITX registers.
Ab_ofl	[2]	Audio Buffer Overflow status 0: Normal 1: Overflow Note: For CSITX audio path only
Vb_ufl	[1]	Video Buffer Underflow status 0: Normal 1: Underflow
Vb_ofl	[0]	Video Buffer Overflow status 0: Normal 1: Overflow

Note: These status will be clear when write “1” to SYS_INT register bit in IntStatus register.

6.2.15. PLL Control Register 0 (PLLCtl0: 0x0020)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	PLL_PRD				Reserved			PLL_FBD[8]
Type	R/W				RO			R/W
Default	0x4				0x00			0x0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	PLL_FBD[7:0]							
Type	R/W							
Default	0x63							

Register Field	Bit	Description
PLL_PRD	[15:12]	Input divider setting Division ratio = (PRD3...0) + 1
Reserved	[11:9]	-
PLL_FBD	[8:0]	Feedback divider setting Division ratio = (FBD8…0) + 1

6.2.16. PLL Control Register 1 (PLLCtl1: 0x0022)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				PLL_FRS		PLL_LBWS	
Type	RO				R/W		R/W	
Default	0x0				0x1		0x2	
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved	LFBREN	BYPCKEN	CKEN	Reserved		RESETB	PLL_EN
Type	RO	R/W	R/W	R/W	RO		R/W	R/W
Default	0x0	0x0	0x0	0x0	0x0		0x0	0x0

Register Field	Bit	Description
Reserved	[15:12]	-
PLL_FRS	[11:10]	Frequency range setting (post divider) for HSCK frequency 2'b00: 500 MHz – 1 GHz HSCK frequency 2'b01: 250 MHz – 500 MHz HSCK frequency 2'b10: 125 MHz – 250 MHz HSCK frequency 2'b11: 62.5 MHz – 125 MHz HSCK frequency
PLL_LBWS	[9:8]	Loop bandwidth setting 2'b00: 25% of maximum loop bandwidth 2'b01: 33% of maximum loop bandwidth 2'b10: 50% of maximum loop bandwidth (default) 2'b11: maximum loop bandwidth
Reserved	[7]	-
PLL_LFBREN	[6]	Lower Frequency Bound Removal Enable 1'b0: REFCLK toggling –> normal operation, REFCLK stops -> no oscillation 1'b1: REFCLK toggling -> normal operation, REFLCK stops -> free running PLL
PLL_BYPCKEN	[5]	Bypass clock enable 1'b0: Normal operation 1'b1: bypass mode, REFCLK is used instead of PLL_VCO output
PLL_CKEN	[4]	Clock enable 1'b0: clocks switched off (output LOW) 1'b1: clocks switched on
Reserved	[3:2]	-
PLL_RESETB	[1]	PLL Reset 1'b0: Reset 1'b1: Normal operation
PLL_EN	[0]	PLL Enable 1'b0: PLL off 1'b1: PLL on

6.2.17. CEC Clock High Time Register 0 (CecHclk: 0x0028)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved					cechclk		
Type	RO					R/W		
Default	0x0					0x2		
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	cechclk							
Type	R/W							
Default	0x90							

Register Field	Bit	Description
Reserved	[15:11]	-
cechclk	[10:0]	CEC Clock High Time 0: Disable 1: 1 RefClk 2: 2 RefClk ….

6.2.18. CEC Clock Low Time Register 0 (CecLclk: 0x002A)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved					ceclclk		
Type	RO					R/W		
Default	0x0					0x2		
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ceclclk							
Type	R/W							
Default	0x90							

Register Field	Bit	Description
Reserved	[15:11]	-
ceclclk	[10:0]	CEC Clock Low Time 0: Disable 1: 1 RefClk 2: 2 RefClk ….

6.2.19. IR Clock High Time Register 0 (IrHclk: 0x002C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved					irhclk		
Type	RO					R/W		
Default	0x0					0x2		
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	irhclk							
Type	R/W							
Default	0x29							

Register Field	Bit	Description
Reserved	[15:11]	-
irhclk	[10:0]	IR Clock High Time 0: Disable 1: 1 RefClk 2: 2 RefClk ….

6.2.20. IR Clock Low Time Register 0 (IrLclk: 0x002E)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved					irlclk		
Type	RO					R/W		
Default	0x0					0x2		
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	irlclk							
Type	R/W							
Default	0x29							

Register Field	Bit	Description
Reserved	[15:11]	-
irlclk	[10:0]	IR Clock Low Time 0: Disable 1: 1 RefClk 2: 2 RefClk ….

6.2.21. IR Lead Code HMin Register (LCHmin: 0x0034)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				lchmin			
Type	RO				R/W			
Default	0x0				0x1			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	lchmin							
Type	R/W							
Default	0x50							

Register Field	Bit	Description
Reserved	[15:12]	-
lchmin	[11:0]	IR Lead Code H Minimum Count 0: Not valid 1: 1 count 2: 2 count ….

6.2.22. IR Lead Code HMax Register (LCHmax: 0x0036)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				lchmax			
Type	RO				R/W			
Default	0x0				0x1			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	lchmax							
Type	R/W							
Default	0x64							

Register Field	Bit	Description
Reserved	[15:12]	-
lchmax	[11:0]	IR Lead Code H Maximum Count 0: Not valid 1: 1 count 2: 2 count ….

6.2.23. IR Lead Code LMin Register (LCLmin: 0x0038)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				lclmin			
Type	RO				R/W			
Default	0x0				0x0			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	lclmin							
Type	R/W							
Default	0xA3							

Register Field	Bit	Description
Reserved	[15:12]	-
lclmin	[11:0]	IR Lead Code L Minimum Count 0: Not valid 1: 1 count 2: 2 count ….

6.2.24. IR Lead Code LMax Register (LCLmax: 0x003A)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				lclmax			
Type	RO				R/W			
Default	0x0				0x0			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	lclmax							
Type	R/W							
Default	0xB7							

Register Field	Bit	Description
Reserved	[15:12]	-
lclmax	[11:0]	IR Lead Code L Maximum Count 0: Not valid 1: 1 count 2: 2 count ….

6.2.25. IR Bit “H” HMin Register (BHHmin: 0x003C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				bhhmin			
Type	RO				R/W			
Default	0x0				0x0			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	bhhmin							
Type	R/W							
Default	0x0C							

Register Field	Bit	Description
Reserved	[15:12]	-
bhhmin	[11:0]	IR Bit H H Minimum Count 0: Not valid 1: 1 count 2: 2 count ….

6.2.26. IR Bit “H” H Max Register (BHHmax: 0x003E)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				bhhmax			
Type	RO				R/W			
Default	0x0				0x0			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	bhhmax							
Type	R/W							
Default	0x20							

Register Field	Bit	Description
Reserved	[15:12]	-
bhhmax	[11:0]	IR Bit H H Maximum Count 0: Not valid 1: 1 count 2: 2 count ….

6.2.27. IR Bit “H” LMin Register (BHLmin: 0x0040)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				bhlmin			
Type	RO				R/W			
Default	0x0				0x0			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	bhlmin							
Type	R/W							
Default	0x0C							

Register Field	Bit	Description
Reserved	[15:12]	-
bhlmin	[11:0]	IR Bit H L Minimum Count 0: Not valid 1: 1 count 2: 2 count ….

6.2.28. IR Bit "H" LMax Register (BHLmax: 0x0042)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				bhlmax			
Type	RO				R/W			
Default	0x0				0x0			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	bhlmax							
Type	R/W							
Default	0x20							

Register Field	Bit	Description
Reserved	[15:12]	-
bhlmax	[11:0]	IR Bit H L Maximum Count 0: Not valid 1: 1 count 2: 2 count ….

6.2.29. IR Bit "L" HMin Register (BLHmin: 0x0044)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				blhmin			
Type	RO				R/W			
Default	0x0				0x0			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	blhmin							
Type	R/W							
Default	0x37							

Register Field	Bit	Description
Reserved	[15:12]	-
blhmin	[11:0]	IR Bit L H Minimum Count 0: Not valid 1: 1 count 2: 2 count ….

6.2.30. IR Bit “L” HMax Register (BLHmax: 0x0046)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				blhmax			
Type	RO				R/W			
Default	0x0				0x0			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	blhmax							
Type	R/W							
Default	0x4B							

Register Field	Bit	Description
Reserved	[15:12]	-
blhmax	[11:0]	IR Bit L H Maximum Count 0: Not valid 1: 1 count 2: 2 count ….

6.2.31. IR Bit “L” LMin Register (BLLmin: 0x0048)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				bllmin			
Type	RO				R/W			
Default	0x0				0x0			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	bllmin							
Type	R/W							
Default	0x0C							

Register Field	Bit	Description
Reserved	[15:12]	-
bllmin	[11:0]	IR Bit L L Minimum Count 0: Not valid 1: 1 count 2: 2 count ….

6.2.32. IR Bit “L” LMax Register (BLLmax: 0x004A)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				bllmax			
Type	RO				R/W			
Default	0x0				0x0			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	bllmax							
Type	R/W							
Default	0x20							

Register Field	Bit	Description
Reserved	[15:12]	-
bllmax	[11:0]	IR Bit L L Maximum Count 0: Not valid 1: 1 count 2: 2 count ….

6.2.33. IR "END" HMin Register (EndHmin: 0x004C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				endhmin			
Type	RO				R/W			
Default	0x0				0x0			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	endhmin							
Type	R/W							
Default	0x0C							

Register Field	Bit	Description
Reserved	[15:12]	-
endhmin	[11:0]	IR "END" H Minimum Count 0: Not valid 1: 1 count 2: 2 count ….

6.2.34. IR "END" HMax Register (EndHmax: 0x004E)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				endhmax			
Type	RO				R/W			
Default	0x0				0x0			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	endhmax							
Type	R/W							
Default	0x20							

Register Field	Bit	Description
Reserved	[15:12]	-
endhmax	[11:0]	IR "END" H Maximum Count 0: Not valid 1: 1 count 2: 2 count ….

6.2.35. IR Repeat Code LMin Register (RCLmin: 0x0050)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				rclmin			
Type	RO				R/W			
Default	0x0				0x0			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	rclmin							
Type	R/W							
Default	0x4C							

Register Field	Bit	Description
Reserved	[15:12]	-
rclmin	[11:0]	IR Repeat Code L Minimum Count 0: Not valid 1: 1 count 2: 2 count ….

6.2.36. IR Repeat Code LMax Register (RCLmax: 0x0052)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				rclmax			
Type	RO				R/W			
Default	0x0				0x0			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	rclmax							
Type	R/W							
Default	0x60							

Register Field	Bit	Description
Reserved	[15:12]	-
rclmax	[11:0]	IR Repeat Code L Maximum Count 0: Not valid 1: 1 count 2: 2 count ….

6.2.37. IR Control Register (IRCtl: 0x0058)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	ir_ccode							
Type	R/W							
Default	0x00							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved						ir_ccodem	Reserved
Type	RO						R/W	RO
Default	0x0						0x0	0x0

Register Field	Bit	Description
ir_ccode	[15:8]	IR Custom code TC9590XBG collects ir data only if the receive “custom code” match this ir_ccode (ir_ccodem = 1’b0)
Reserved	[7:2]	-
ir_ccodem	[1]	IR Custom Code Mask 0: Match 1: No Match (mask)
Reserved	[0]	-

6.2.38. IR Data Register (IRData: 0x005A)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	ir_rccode							
Type	RO							
Default	0x0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	ir_rdata							
Type	RO							
Default	0x0							

Register Field	Bit	Description
ir_rccode	[15:8]	IR Receive custom code data
ir_rdata	[7:0]	IR Receive data

6.3. CSI-2 Tx PHY/PPI

6.3.1. Clock Lane D-PHY TX Control register (CLW_DPHYCONTTX: 0x0100)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						CLW_CAP1	CLW_CAP0
Type	RO	RO	RO	RO	RO	RO	R/W	R/W
Default	0	0	0	0	0	0	1	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	DLYCNTRL3	DLYCNTRL2	DLYCNTRL1	DLYCNTRL0	Reserved		CLW_LPTXCURR1EN	CLW_LPTXCURR0EN
Type	R/W	R/W	R/W	R/W	RO	RO	R/W	R/W
Default	0	0	0	0	0	0	1	0

Table 6-3 Clock Lane D-PHY TX Control register

Register Field	Bit	Description
Reserved	[31:10]	-
CLW_CAP1	[9]	Selection bit 1 of different HSTX output capacitors for Clock Lane
CLW_CAP0	[8]	Selection bit 0 of different HSTX output capacitors for Clock Lane (CAP1,CAP0): = (00): 0 [pF] (CAP1,CAP0): = (01): 2.8 [pF] (CAP1,CAP0): = (10): 3.2 [pF] (CAP1,CAP0): = (11): 3.6 [pF]
DLYCNTRL[3:0]	[7:4]	Tuning of transmit window position. The High Speed Clock output can be delayed according to the setting. The recommended value is determined by evaluating the LSI in which this module is implemented. Typical delay for rising/falling edge is about DLYCNTRL x 24ps/27ps. Rising edge: DLYCNTRL x 24ps, Falling edge: DLYCNTRL x 27ps.
Reserved	[3:2]	-
CLW_LPTXCURR1EN	[1]	Selection bit-1 for LPTX output current (TRLP/TFLP tuning) for clock Lane
CLW_LPTXCURR0EN	[0]	Selection bit-0 for LPTX output current (TRLP/TFLP tuning) for clock Lane 00: no additional output current 01: 25% additional output current 10: 25% additional output current 11: 50% additional output current The default value is “10”. However, if “00” is set, the rise/fall time will become later and if “11” is set, the rise/fall time will become earlier.

6.3.2. Data Lane 0 D-PHY TX Control register (D0W_DPHYCONTTX:0x0104)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						D0W_CAP1	D0W_CAP0
Type	RO	RO	RO	RO	RO	RO	R/W	R/W
Default	0	0	0	0	0	0	1	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	DLYCNTRL3	DLYCNTRL2	DLYCNTRL1	DLYCNTRL0	Reserved	Reserved	D0W_LPTXCURR1EN	D0W_LPTXCURR0EN
Type	R/W	R/W	R/W	R/W	RO	RO	R/W	R/W
Default	0	0	0	0	0	0	1	0

Table 6-4 Data Lane 0 D-PHY TX Control register

Register Field	Bit	Description
Reserved	[31:10]	-
D0W_CAP1	[9]	Selection bit 1 of different HSTX output capacitors for Data Lane 0.
D0W_CAP0	[8]	Selection bit 0 of different HSTX output capacitors for Data Lane 0. (CAP1,CAP0): = (00): 0 [pF] (CAP1,CAP0): = (01): 2.8 [pF] (CAP1,CAP0): = (10): 3.2 [pF] (CAP1,CAP0): = (11): 3.6 [pF]
DLYCNTRL[3:0]	[7:4]	Tuning of transmit window position. The High Speed Data output can be delayed according to the setting. The recommended value is determined by evaluating the LSI in which this module is implemented. Typical delay for rising/falling edge is about DLYCNTRL x 24ps/27ps. Rising edge: DLYCNTRL x 24ps, Falling edge: DLYCNTRL x 27ps.
Reserved	[3:2]	-
D0W_LPTXCURR1EN	[1]	Selection bit-1 for LPTX output current (TRLP/TFLP tuning) for Data Lane 0.
D0W_LPTXCURR0EN	[0]	Selection bit-0 for LPTX output current (TRLP/TFLP tuning) for Data Lane 0. 00: no additional output current 01: 25% additional output current 10: 25% additional output current 11: 50% additional output current The default value is “10”. However, if “00” is set, the rise/fall time will become later and if “11” is set, the rise/fall time will become earlier.

6.3.3. Data Lane 1 D-PHY TX Control Register (D1W_DPHYCONTTX: 0x0108)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						D1W_CAP1	D1W_CAP0
Type	RO	RO	RO	RO	RO	RO	R/W	R/W
Default	0	0	0	0	0	0	1	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	DLYCNTRL3	DLYCNTRL2	DLYCNTRL1	DLYCNTRL0	Reserved		D1W_LPTXCURR1EN	D1W_LPTXCURR0EN
Type	R/W	R/W	R/W	R/W	RO	RO	R/W	R/W
Default	0	0	0	0	0	0	1	0

Table 6-5 Data Lane 1 D-PHY TX Control Register

Register Field	Bit	Description
Reserved	[31:10]	-
D1W_CAP1	[9]	Selection bit 1 of different HSTX output capacitors for Data Lane 1.
D1W_CAP0	[8]	Selection bit 0 of different HSTX output capacitors for Data Lane 1. (CAP1,CAP0): = (00): 0 [pF] (CAP1,CAP0): = (01): 2.8 [pF] (CAP1,CAP0): = (10): 3.2 [pF] (CAP1,CAP0): = (11): 3.6 [pF]
DLYCNTRL[3:0]	[7:4]	Tuning of transmit window position. The High Speed Clock output can be delayed according to the setting. The recommended value is determined by evaluating the LSI in which this module is implemented. Typical delay for rising/falling edge is about DLYCNTRL x 24ps/27ps. Rising edge: DLYCNTRL x 24ps, Falling edge: DLYCNTRL x 7ps.
Reserved	[3:2]	-
D1W_LPTXCURR1EN	[1]	Selection bit-1 for LPTX output current (TRLP/TFLP tuning) for Data Lane 1
D1W_LPTXCURR0EN	[0]	Selection bit-0 for LPTX output current (TRLP/TFLP tuning) for Data Lane 1 00: no additional output current 01: 25% additional output current 10: 25% additional output current 11: 50% additional output current The default value is “10”. However, if “00” is set, the rise/fall time will become later and if “11” is set, the rise/fall time will become earlier.

6.3.4. Data Lane 2 D-PHY TX Control Register (D2W_DPHYCONTTX: 0x010C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						D2W_CAP1	D2W_CAP0
Type	RO	RO	RO	RO	RO	RO	RO	R/W
Default	0	0	0	0	0	0	1	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	DLYCNTRL3	DLYCNTRL2	DLYCNTRL1	DLYCNTRL0	Reserved		D2W_LPTXCURR1EN	D2W_LPTXCURR0EN
Type	R/W	R/W	R/W	R/W	RO	RO	R/W	R/W
Default	0	0	0	0	0	0	1	0

Table 6-6 Data Lane 2 D-PHY TX Control Register

Register Field	Bit	Description
Reserved	[31:10]	-
D2W_CAP1	[9]	Selection bit 1 of different HSTX output capacitors for Data Lane 2.
D2W_CAP0	[8]	Selection bit 0 of different HSTX output capacitors for Data Lane 2. (CAP1,CAP0): = (00): 0 [pF] (CAP1,CAP0): = (01): 2.8 [pF] (CAP1,CAP0): = (10): 3.2 [pF] (CAP1,CAP0): = (11): 3.6 [pF]
DLYCNTRL[3:0]	[7:4]	Tuning of transmit window position. The High Speed Clock output can be delayed according to the setting. The recommended value is determined by evaluating the LSI in which this module is implemented. Typical delay for rising/falling edge is about DLYCNTRL x 24ps/27ps. Rising edge: DLYCNTRL x 24ps, Falling edge: DLYCNTRL x 27ps.
Reserved	[3:2]	-
D2W_LPTXCURR1EN	[1]	Selection bit-1 for LPTX output current (TRLP/TFLP tuning) for Data Lane 2.
D2W_LPTXCURR0EN	[0]	Selection bit-0 for LPTX output current (TRLP/TFLP tuning) for Data Lane 2 0: no additional output current 1: 25% additional output current 10: 25% additional output current 11: 50% additional output current The default value is “10”. However, if “00” is set, the rise/fall time will become later and if “11” is set, the rise/fall time will become earlier.

6.3.5. Data Lane 3 D-PHY TX Control Register (D3W_DPHYCONTTX: 0x0110)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						D3W_CAP1	D3W_CAP0
Type	RO	RO	RO	RO	RO	RO	RO	R/W
Default	0	0	0	0	0	0	1	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	DLYCNTRL3	DLYCNTRL2	DLYCNTRL1	DLYCNTRL0	Reserved		D3W_LPTXCURR1EN	D3W_LPTXCURR0EN
Type	R/W	R/W	R/W	R/W	RO	RO	R/W	R/W
Default	0	0	0	0	0	0	1	0

Table 6-7 Data Lane 3 D-PHY TX Control Register

Register Field	Bit	Description
Reserved	[31:10]	-
D3W_CAP1	[9]	Selection bit 1 of different HSTX output capacitors for Data Lane 3.
D3W_CAP0	[8]	Selection bit 0 of different HSTX output capacitors for Data Lane 3. (CAP1,CAP0): = (00): 0 [pF] (CAP1,CAP0): = (01): 2.8 [pF] (CAP1,CAP0): = (10): 3.2 [pF] (CAP1,CAP0): = (11): 3.6 [pF]
DLYCNTRL[3:0]	[7:4]	Tuning of transmit window position. The High Speed Clock output can be delayed according to the setting. The recommended value is determined by evaluating the LSI in which this module is implemented. Typical delay for rising/falling edge is about DLYCNTRL x 24ps/27ps. Rising edge : DLYCNTRL x 24ps, Falling edge : DLYCNTRL x 27ps.
Reserved	[3:2]	-
D3W_LPTXCURR1EN	[1]	Selection bit-1 for LPTX output current (TRLP/TFLP tuning) for Data Lane 3
D3W_LPTXCURR0EN	[0]	Selection bit-0 for LPTX output current (TRLP/TFLP tuning) for Data Lane 3 00: no additional output current 01: 25% additional output current 10: 25% additional output current 11: 50% additional output current The default value is “10”. However, if “00” is set, the rise/fall time will become later and if “11” is set, the rise/fall time will become earlier.

6.3.6. Clock Lane D-PHY Control Register (CLW_CNTRL: 0x0140)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x00							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							CLW_LaneDisable
Type	RO							R/W
Default	0x00							0

Table 6-8 Clock Lane D-PHY Control Register

Register Field	Bit	Default	Description
Reserved	[15:1]	0x0	-
CLW_LaneDisable	[0]	0x0	Force Lane Disable for Clock Lane. 1'b1: Force Lane Disable 1'b0: Bypass Lane Enable from PPI Layer enable.

6.3.7. Data Lane 0 D-PHY Control Register (D0W_CNTRL: 0x0144)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x00							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							CLW_LaneDisable
Type	RO							R/W
Default	0x00							0

Table 6-9 Data Lane 0 D-PHY Control Register

Register Field	Bit	Default	Description
Reserved	[15:1]	0x0	-
D0W_LaneDisable	[0]	0x0	Force Lane Disable for Data Lane 0. 1'b1: Force Lane Disable 1'b0: Bypass Lane Enable from PPI Layer enable.

6.3.8. Data Lane 1 D-PHY Control Register (D1W_CNTRL: 0x0148)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x00							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							D1W_LaneDisable
Type	RO							R/W
Default	0x00							0

Table 6-10 Data Lane 1 D-PHY Control Register

Register Field	Bit	Default	Description
Reserved	[15:1]	0x0	-
D1W_LaneDisable	[0]	0x0	Force Lane Disable for Data Lane 0. 1'b1: Force Lane Disable 1'b0: Bypass Lane Enable from PPI Layer enable.

6.3.9. Data Lane 2 D-PHY Control Register (D2W_CNTRL: 0x014C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x00							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							D2W_LaneDisable
Type	RO							R/W
Default	0x00							0

Table 6-11 Data Lane 2 D-PHY Control Register

Register Field	Bit	Default	Description
Reserved	[15:1]	0x0	-
D2W_LaneDisable	[0]	0x0	Force Lane Disable for Data Lane 2. 1'b1: Force Lane Disable 1'b0: Bypass Lane Enable from PPI Layer enable.

6.3.10. Data Lane 3 D-PHY Control Register (D3W_CNTRL: 0x0150)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x00							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							D3W_LaneDisable
Type	RO							R/W
Default	0x00							0

Table 6-12 Data Lane 3 D-PHY Control Register

Register Field	Bit	Default	Description
Reserved	[15:1]	0x0	-
D3W_LaneDisable	[0]	0x0	Force Lane Disable for Data Lane 3. 1'b1: Force Lane Disable 1'b0: Bypass Lane Enable from PPI Layer enable.

6.3.11. PPI STARTCNTRL (STARTCNTRL: 0x0204)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							START
Type	RO	RO	RO	RO	RO	RO	RO	W1O
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
Reserved	[31:1]	–
START	[0]	START control bit of PPI-TX function. By writing 1 to this bit, PPI starts function. 0: Stop function. (default). Writing 0 is invalid and the bit can be set to zero by system hardware reset or software only. 1: Start function. The following registers are set to appropriate value before starting any transmission by START bit in STARTCTRL register. Once START bit is set to high, the change of the register bits does not affect to function. In order to change the values, toggle SysCtr[CTxRst] is necessary.

6.3.12. PPI STATUS (PPISTATUS: 0x0208)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							BUSY
Type	RO	RO	RO	RO	RO	RO	RO	W1O
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
Reserved	[31:1]	-
BUSY	[0]	After writing 1 to the START bit in the STARTCNTRL register, this bit is set until SysCtr[CTxRst] is asserted. 0: Not Busy. (default) 1: Busy.

6.3.13. LINEINITCNT (LINEINITCNT: 0x0210)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	LINEINITCNT[15:8]							
Type	R/W							
Default	0x20							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	LINEINITCNT[7:0]							
Type	R/W							
Default	0x8E							

Register Field	Bit	Description
Reserved	[31:16]	-
LINEINITCNT	[15:0]	Line Initialization Wait Counter This counter is used for line initialization. **Set this register before setting [STARTCNTRL].START = 1.** MIPI specification requires that the slave device needs to observe LP-11 for 100 µs and ignore the received data before the period at initialization time. The count value depends on HFCLK and the value needs to be set to achieve more than 100 µs. The counter starts after the START bit of the STARTCNTRL register is set. The Master device needs to output LP-11 for 100 µs in order for the slave device to observe LP-11 for the period. For example, in order to set 100 µs when the period of HFCLK is 12 ns, the counter value should be more than 8333.3 = 0x208D (100 µs / 12 ns). Default is 0x208E.

6.3.14. LPTXTIMECNT (LPTXTIMECNT: 0x0214)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved					LPTXTIMECNT[10:8]		
Type	RO					R/W		
Default	0x00					0x0		
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	LPTXTIMECNT[7:0]							
Type	R/W							
Default	0x01							

Register Field	Bit	Description
Reserved	[15:11]	-
LPTXTIMECNT	[10:0]	SYSLPTX Timing Generation Counter The counter generates a timing signal for the period of LPTX. This counter is counted using the HSByteClk (the Main Bus clock), and the value of (setting + 1) * HSByteClk Period becomes the period LPTX. Be sure to set the counter to a value greater than 50 ns.

Set this register before setting [STARTCNTRL].START = 1.

6.3.15. TCLK_HEADERCNT (TCLK_HEADERCNT: 0x0218)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	TCLK_ZEROCNT[7:0]							
Type	R/W							
Default	0x01							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved	TCLK_PREPARECNT[6:0]						
Type	RO	R/W						
Default	0	0x01						

Register Field	Bit	Description
TCLK_ZEROCNT	[15:8]	**TCLK_ZERO Counter** This counter is used for Clock Lane control in the Master mode. In order to satisfy the timing parameter TCLK-PRE + TCLK-ZERO for Clock Lane, this counter is used. This counter is counted by HSBYTECLk. Set this register in order to set the minimum time (TCLK-PRE + TCLK-ZERO) to a value greater than 300 ns. The actual value is ((1 to 2) + (TCLK_ZEROCNT + 1)) x HSByteClkCycle + (PHY output delay). The PHY output delay is about (0 to 1) x HSByteClkCycle in the ByteClk conversion performed during RTL simulation, and is about (2 to 3) x MIPIBitClk cycle in the BitClk conversion.
Reserved	[7]	–

Register Field	Bit	Description
TCLK_PREPARECNT	[6:0]	**TCLK_PREPARE Counter** This counter is used for Clock Lane control in the Master mode. In order to satisfy the timing parameter TCLK-PREPARE for Clock Lane, this counter is used. This counter is counted by HSBYTECLK. Set TCLK-PREPARE period that is greater than 38 ns but less than 95 ns. Calculating formula (TCLK_PREPARECNT + 1) x HSByteClkCycle

Set this register before setting [STARTCNTRL].START = 1.

6.3.16. TCLK_TRAILCNT (TCLK_TRAILCNT: 0x021C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x00							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	TCLKTRAILCNT[7:0]							
Type	R/W							
Default	0x01							

Register Field	Bit	Description
Reserved	[15:8]	–
TCLK_TRAILCNT	[7:0]	**TCLK_TRAIL Counter** This counter is used for Clock Lane control in Master mode. In order to satisfy the timing parameter about TCLK-TRAIL and TEOT for Clock Lane, this counter is used. This counter is counted by HSBYTECLK. Set this register in order to set TCLK-TRAIL to a value greater than 60 ns and TEOT to a value less than 105 ns + 12 x UI The actual value is (TCLK_TRAILCNT + (1 to 2)) x HSByteClkCycle + (2 + (1 to 2)) * HSBYTECLKCycle - (PHY output delay). The PHY output delay is about (0 to 1) x HSByteClkCycle in the ByteClk conversion performed during RTL simulation, and is about (2 to 3) x MIPIBitClk cycle in the BitClk conversion.

Set this register before setting [STARTCNTRL].START = 1.

6.3.17. THS_HEADERCNT (THS_HEADERCNT: 0x0220)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved	THS_ZEROCNT[6:0]						
Type	RO	R/W						
Default	0	0x01						
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved	THS_PREPARECNT[6:0]						
Type	RO	R/W						
Default	0	0x01						

Register Field	Bit	Description
Reserved	[15]	-
THS_ZEROCNT	[14:8]	**THS_ZERO Counter** This counter is used for Data Lane control in Master mode. In order to satisfy the timing parameter about THS-PREPARE + THS-ZERO for Data Lane, this counter is used. This counter is counted by HSBYTECLK. Set this register to set the (THS-PREPARE + THS-ZERO) period, which should be greater than (145 ns + 10 x UI) results. The actual value is ((1 to 2) + 1 + (TCLK_ZEROCNT + 1) + (3 to 4)) x ByteClk cycle + HSByteClk x (2 + (1 to 2)) + (PHY delay). The PHY output delay is about (1 to 2) x HSByteClkCycle in the ByteClk conversion performed during RTL simulation, and is about (8 + (5 to 6)) x MIPIBitClk cycle in BitClk conversion.
Reserved	[7]	-
THS_PREPARECNT	[6:0]	**THS_PREPARE Counter** This counter is used for Data Lane control in Master mode. In order to satisfy the timing parameter about THS-PREPARE for Data Lane, this counter is used. This counter is counted by HSBYTECLK. Set this register in order to set the THS-PREPARE period, which should be greater than (40 ns + 4xUI) and less than (85 ns + 6xUI) results. Calculating Formula: (THS_PREPARECNT + 1) x HSByteClkCycle

Set this register before setting [STARTCNTRL].START = 1.

6.3.18. TWAKEUP (TWAKEUP: 0x0224)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	TWAKEUPCNT[15:8]							
Type	R/W							
Default	0x4E							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	TWAKEUPCNT[7:0]							
Type	R/W							
Default	0x20							

Register Field	Bit	Description
Reserved	[31:16]	-
TWAKEUPCNT	[15:0]	**TWAKEUP Counter** This counter is used to exit ULPS state. Ultra-Low Power State is exited by means of a Mark-1 state with a length TWAKEUP followed by a Stop state. This counter is counted by the unit of LPTXTIMECNT.

Set this register before setting [STARTCNTRL].START = 1.

6.3.19. TCLK_POSTCNT (TCLK_POSTCNT: 0x0228)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved					TCLK_POSTCNT[10:8]		
Type	RO					R/W		
Default	0x00					0x2		
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	TCLK_POSTCNT[7:0]							
Type	R/W							
Default	0x00							

Register Field	Bit	Description
Reserved	[15:11]	–
TCLK_POSTCNT	[10:0]	**TCLK_POST Counter** This counter is used for Clock Lane control in Master mode. This counter is counted by the HSByteClk. Set a value greater than (60 ns + 52 x UI) results. The actual value is ((1 to 2) + (TCLK_POSTCNT + 1)) x HSByteClk cycle + (1) x HSBYTECLK cycle.

Set this register before setting [STARTCNTRL].START = 1.

6.3.20. THS_TRAILCNT (THS_TRAILCNT: 0x022C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x00							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved				THS_TRAILCNT[3:0]			
Type	RO				R/W			
Default	0x0				0x2			

Register Field	Bit	Description
Reserved	[15:4]	–
THS_TAILCNT	[3:0]	**THS_TRAIL Counter** This counter is used for Data Lane control in Master mode. This counter is counted by HSBYTECLK. Set a value greater 8 x UI or (60 ns + 4 x UI) and less than TEOT which is 105 ns + 12 x UI results. The actual value is (1 + THS_TRAILCNT) x ByteClk cycle + ((1 to 2) + 2) x HSBYTECLK cycle - (PHY output delay). The PHY output delay is about (1 to 2) x HSByteClkCycle in ByteClk conversion performed during RTL simulation and is about (8 + (5 to 6)) x MIPIBitClk cycle in BitClk conversion.

Set this register before setting [STARTCNTRL].START = 1.

6.3.21. HSTXVREGCNT (HSTXVREGCNT: 0x0230)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	HSTXVREGCNT[15:8]							
Type	R/W							
Default	0x00							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	HSTXVREGCNT[7:0]							
Type	R/W							
Default	0x20							

Register Field	Bit	Description
HSTXVREGCNT	[15:0]	TX Voltage Regulator setup Wait Counter This counter is used for all lanes of HSTXVREG commonly. Counter value is counted by HFCLK. The counter starts when START bit is set. After the counter is counted up, PPI-TX can change the line from LP mode to HS mode. If the counter value is set to zero, there is no wait by the counter. Recommended counter value will be decided by evaluation. It was determined that a value of 200 ns max in the ELDEC TEG skew evaluation results (5/21/2009) is sufficient. LINEINCNT is 100 µs, so any value less than that will not affect the value of this counter. The value 1 µs is used in the example setting.

Set this register before setting [STARTCNTRL].START = 1.

6.3.22. HSTXVREGEN (HSTXVREGEN: 0x0234)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved			D3M_HSTXVREGEN	D2M_HSTXVREGEN	D1M_HSTXVREGEN	D0M_HSTXVREGEN	CLM_HSTXVREGEN
Type	RO	RO	RO	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
Reserved	[15:5]	-
D3M_HSTXVREGEN	[4]	Voltage regulator enable for HSTX Data Lane 3. In order to reduce power consumption, set to be “disable” when PPI-TX is not used. 0: Disable (Default) 1: Enable
D2M_HSTXVREGEN	[3]	Voltage regulator enable for HSTX Data Lane 2. In order to reduce power consumption, set to be “disable” when PPI-TX is not used. 0: Disable (Default) 1: Enable
D1M_HSTXVREGEN	[2]	Voltage regulator enable for HSTX Data Lane 1. In order to reduce power consumption, set to be “disable” when PPI-TX is not used. 0: Disable (Default) 1: Enable
D0M_HSTXVREGEN	[1]	Voltage regulator enable for HSTX Data Lane 0. In order to reduce power consumption, set to be “disable” when PPI-TX is not used. 0: Disable (Default) 1: Enable
CLM_HSTXVREGEN	[0]	Voltage regulator enable for HSTX Clock Lane. In order to reduce power consumption, set to be “disable” when PPI-TX is not used. 0: Disable (Default) 1: Enable

Set this register before setting [STARTCNTRL].START = 1.

6.3.23. TXOPTIONCNTRL (TXOPTIONCNTRL: 0x0238)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							CONTCLKMODE
Type	RO	RO	RO	RO	RO	RO	RO	R/W
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
Reserved	[15:1]	-
CONTCLKMODE	[0]	**Set Continuous Clock Mode** Writing “1” to this bit will set the Clock Lane to the Continuous Clock mode 0: Non-continuous clock mode. Transitions into the LP11 state in coordination with the Data Lane operation. 1: Continuous clock mode. Maintains the Clock Lane output regardless of the Data Lane operation.

6.4. Tx Control Register

6.4.1. CSI Configuration Read Register (CSI_CONTROL: 0x040C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Csi_mode	Reserved				HtxToEn	Reserved	
Type	RO	RO				RO	RO	
Default	1	0	1	1	1	1	0	
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	TxHSMd	Reserved				NOL[1:0]		EoTDis
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
CSI_mode	[15]	**CSI Mode Selection** 0: Reserved 1: CSI MOde
Reserved	[14:11]	-
HtxToEn	[10]	**HSTX_TO_EN** 0: Disables the HTX_TO timer. 1: Enables the HTX_TO timer.
Reserved	[9:8]	-
TxHSMd	[7]	**TX HS MODE** 0: Low power transfer is performed to Tx. 1: High-Speed data transfer is performed to Tx.
Reserved	[6:3]	-
NOL	[2:1]	**NOL** This field specifies the number of HS lanes. This setting can only be made during initial setup or during reset. 00: 1 Data Lane 01: 2 Data Lanes 10: 3 Data Lanes 11: 4 Data Lanes
EoTDis	[0]	**DISABLE EOT Packet Transmission** 0: The EOT packet is automatically granted at the end of HS transfer then is transmitted. 1: The EOT packet is not automatically granted at the end of HS transfer and is not transmitted.

Write to register 0x500, CSI_CONFW Register, to change this value.

6.4.2. CSI STATUS Register (CSI_STATUS: 0x0410)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved					WSync	TxAct	Reserved
Type	RO					RO	RO	RO
Default	0xX					0	0	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							Hlt
Type	RO							RO
Default	0x0X							0

Register Field	Bit	Default	Description
Reserved	[15:11]	X	-
WSync	[10]	0	**Wait Sync Signal** This bit indicates that the CSI-TX module is waiting for a particular Sync signal
TxAct	[9]	0	**Transmitter Active** This bit indicates that the CSI-TX module is in the Transmit mode.
Reserved	[8:1]	X	-
Hlt	[0]	0	**Halted** The CSI-TX module is stopped by either an error or a pause request.

6.4.3. CSI_INT Register (CSI_INT: 0x0414)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO							
Default	0x00							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved							
Type	RO							
Default	0x00							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x00							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved				IntHlt	IntEr	Reserved	
Type	RO				RO	RO	RO	
Default	0x00				0	0	0	

Register Field	Bit	Default	Description
Reserved	[31:4]	0x0	–
IntHlt	[3]	0x0	**INT_HALTED** The CSI-TX module was stopped by an error or a pause request.
IntEr	[2]	0x0	**INT_CSI_ERR** An interrupt was requested by a CSI_ERR register error.
Reserved	[1:0]	0x0	–

Each bit can indirectly clear a register value either when “1” is written to the bit of each corresponding CSI_INT_CLR register.

6.4.4. CSI_INT_ENA Register (CSI_INT_ENA: 0x0418)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO							
Default	0x00							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved							
Type	RO							
Default	0x00							
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved							
Type	RO							
Default	0x00							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved				IEnHlt	IEnEr	Reserved	
Type	RO				RO	RO	RO	
Default	0x0				0	0	0x0	

Register Field	Bit	Default	Description
Reserved	[31:4]	0x0	-
IEnHlt	[3]	0x0	**INTENA_HALTED** This bit enables interrupt notification by INT_HALTED sources.
IEnEr	[2]	0x0	**INTENA_CSI_ERR** This bit enables interrupt notification by INT_CSI_ERR sources.
Reserved	[1:0]	0x0	-

Only indirect writing, i.e. write to CSI_CONFW with [Addr] = 0x06.

6.4.5. CSI_ERR Register (CSI_ERR: 0x044C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						InEr	WCEr
Type	RO						RO	RO
Default	0x00						0	0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved			QUnk	Reserved		HTxBrk	Reserved
Type	RO			RO	RO		RO	RO
Default	0			0	0		0	0

Register Field	Bit	Default	Description
Reserved	[31:10]	0x0	-
InEr	[9]	0x0	**INTERNAL_ERROR** This bit indicates that another internal error occurred.
WCEr	[8]	0x0	**WC_ERROR** This bit indicates that more bytes than expected were received from the PDIF. Because distinguishing the current data from the next payload data of continuous transfers is difficult when the last payload data is 4-byte aligned, this error is not detected.
Reserved	[7:5]	0x0	-
QUnk	[4]	0x0	**CQ_UNKNOWN** This bit indicates that an unknown command or incorrect parameter was detected by the command queue.
Reserved	[3:2]	0x0	-
HTxBrk	[1]	0x0	**HSTX_BROKEN** This bit indicates that the byte stream was disrupted during High-Speed transfer.
Reserved	[0]	0x0	-

The content of the CSI_ERR register is cleared by reading it out.

6.4.6. CSI_ERR_INTENA (CSI_ERR_INTENA: 0x0450)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						CSI_ERR_INTENA[9:8]	
Type	RO						RO	
Default	0x00						0	
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	CSI_ERR_INTENA[7:0]							
Type	RO							
Default	0xbf							

Register Field	Bit	Default	Description
Reserved	[31:10]	0x0	-
CSI_ERR_INTENA	[9:0]	0xbf	**CSI_ERR_INTENA** This field controls interrupt generation for when an error has been reported to the CSI_ERR register. Generation of the CSI_ERR_INT interrupt which corresponds to the CSI_ERR register error is enabled.

Only indirect writing, i.e. write to CSI_CONFW with [Addr] = 0x14.

6.4.7. CSI_ERR_HALT Register (CSI_ERR_HALT: 0x0454)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						CSI_ERR_HALT[9:8]	
Type	RO						RO	
Default	0x00						0	
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	CSI_ERR_HALT[7:0]							
Type	RO							
Default	0xbf							

Register Field	Bit	Default	Description
Reserved	[31:10]	0x0	-
CSI_ERR_HALT	[9:0]	0xbf	**CSI_ERR_HALT** This field controls CSI-TX operation for when an error is reported to the CSI_ERR register. The CSI-TX module stops command processing when it receives an error corresponding to the set bits in the CSI_ERR_INTENA and CSI_ERR_HALT registers.

Only indirect writing, i.e. write to CSI_CONFW with [Addr] = 0x15.

6.4.8. CSI Configuration Register (CSI_CONFW: 0x0500)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	MODE			Address				
Type	WO	WO	WO	WO	WO	WO	WO	WO
Default	0	0	0	0	0	0	0	0
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved[23:16]							
Type	WO	WO	WO	WO	WO	WO	WO	WO
Default	0	0	0	0	0	0	0	0
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	DATA[15:8]							
Type	WO	WO	WO	WO	WO	WO	WO	WO
Default	0	0	0	0	0	0	0	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	DATA[7:0]							
Type	WO	WO	WO	WO	WO	WO	WO	WO
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
MODE	[31:29]	**Set or Clear AddrReg (register specified in Address field) Bits** 3'b101: Set Register Bits in AddReg as indicated in DATA field 3'b110: Clear Register Bits in AddReg as indicated in DATA field Others: Reserved
Address	[28:24]	**Address Field** 0x03: CSI_Control Register, please refer to 6.4.1, register 0x040C 0x06: CSI_INT_ENA Register 0x14: CSI_ERR_INTENA Register 0x15: CSI_ERR_ HALT Register Others: Reserved
Reserved	[23:16]	-
DATA	[15:0]	**DATA Field** When location DATA[n] is set to '1', the corresponding bit at AddrReg[n] will be cleared or set depending on MODE bits described above. Multiples bits can be set simultaneously

Note: Write to CSI_CONFW Register results to changes in corresponding bit changed in AddrReg Register.

6.4.9. CSI_RESET Register (CSI_RESET: 0x0504)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved						RstCnf	RstMdl
Type	RO						WO	WO
Default	0x00						0	0

Register Field	Bit	Default	Description
Reserved	[31:2]	0x0	–
RstCnf	[1]	0x0	**RST_CONF** 0: Operation is not affected. 1: Reset Configuration registers Only
RstMdl	[0]	0x0	**RST_MODULE** 0: Operation is not affected. 1: Reset Logic Only

6.4.10. CSI_INT_CLR Register (CSI_INT_CLR: 0x050C)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO							
Default	0							
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved							
Type	RO							
Default	0							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved				ICrHlt	ICrEr	Reserved	
Type	RO				WO	WO	RO	
Default	0				0	0	0	

Register Field	Bit	Default	Description
Reserved	[31:4]	0x0	-
ICrHlt	[3]	0x0	**INTCLR_HALTED** 0: Operation is not affected. 1: The INT_HALTED interrupt is cleared.
ICrEr	[2]	0x0	**INTCLR_CSI_ERR** 0: Operation is not affected. 1: The INT_CSI_ERR interrupt is cleared.
Reserved	[1:0]	0x0	-

6.4.11. CSI_START (CSI_START: 0x0518)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved[7:1]							Strt
Type	RO	RO	RO	RO	RO	RO	RO	WO
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
Reserved	[31:1]	-

6.5. CEC Control Register

6.5.1. CEC Enable Register (CECEN: 0x0600)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved							CECEN
Type	RO							R/W
Default	0x0							0x1

Table 6-13 CEC Enable Register

Register Field	Bit	Description
Reserved	[15:1]	-
CECEN	0	**CEC operation** 0: Disable 1: Enable

6.5.2. CEC Logical Address Register (CECADD: 0x0604)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	CECADD[15:8]							
Type	R/W							
Default	0x0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	CECADD[7:0]							
Type	R/W							
Default	0x0							

Table 6-14 CEC Logical Address Register

Register Field	Bit	Description
CECADD[15:0]	[15:0]	**Specify logical address assigned to CEC** Each bit corresponds to individual address, therefore multiple addresses can be assigned to CEC logic

6.5.3. CEC Reset Register (CECRST: 0x0608)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved							CECRST
Type	RO							R/W
Default	0x0							0x0

Table 6-15 CEC Reset Register

Register Field	Bit	Description
Reserved	[15:1]	Reserved
CECRST	[0]	**CEC soft reset** 0: Normal Operation 1: Reset Asserted All the logic got reset: - Reception: Stops immediately. The received data is discarded. - Transmission (including the CEC line): Stops immediately. - Registers: The following registers are also reset. (CECADD, CECREN, CECRCR1, CECRCR2, CECRCR3,CECTEN, CECTCR, CECRSTAT, CECTSTAT, CECRBUF01-16, CECTBUF01-16, CECRCTR)

6.5.4. CEC Receive Enable (CECREN: 0x060C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved							CECREN
Type	RO							R/W
Default	0x0							0x1

Table 6-16 CEC Receive Enable Register

Register Field	Bit	Description
Reserved	[15:1]	Reserved
CECREN	[0]	**CEC reception enable** 0: Disable 1: Enable

6.5.5. CEC Receive Control Register 1 (CECRCTL1: 0x0614)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							CECACKDIS
Type	RO							R/W
Default	0x0							0x0
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved		CECHNC[1:0]		Reserved	CECLNC[2:0]		
Type	RO		R/W		RO	R/W		
Default	0x0		0x0		0x0	0x0		
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved	CECMIN[2:0]			Reserved	CECMAX[2:0]		
Type	RO	R/W			R	R/W		
Default	0x0	0x0			0x0	0x0		
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B6**
Name	Reserved	CECDAT[2:0]			CECTOUT[1:0]		CECRIHLD	CECOTH
Type	RO	R/W			R/W		R/W	R/W
Default	0x0	0x0			0x0		0x0	0x0

Table 6-17 CEC Receive Control Register 1

Register Field	Bit	Description
Reserved	[31:25]	Reserved
CECACKDIS	[24]	Enable ACK transmission 1: Disable 0: Enable
Reserved	[23:22]	Reserved
CECHNC	[21:20]	Number of consecutive cycles sampling logical '1' for noise cancellation 00: 1 cycle 01: 2 cycles 10: 3 cycles 11: 4 cycles
Reserved	[19]	Reserved
CECLNC	[18:16]	Number of consecutive cycles sampling logical '0' for noise cancellation 000: 1 cycle 001: 2 cycles 100: 3 cycles 100: 4 cycles ⋮ 111: 8 cycles
Reserved	[15]	Reserved
CECMIN	[14:12]	The minimum time to detect valid bit value. Error is detected when signal changes earlier than the minimum value 000: 2.05ms 001: 2.05ms+1cycle 010: 2.05ms+2cycles 011: 2.05ms+3cycles 100: 2.05ms-1cycle 101: 2.05ms-2cycles 110: 2.05ms-3cycles 111: 2.05ms-4cycles
Reserved	[11]	Reserved
CECMAX	[10:8]	The maximum time to detect valid bit value. Error is detected when signal does not change within the maximum time 000: 2.75ms 001: 2.75ms+1cycle 010: 2.75ms+2cycles 011: 2.75ms+3cycles 100: 2.75ms-1cycle 101: 2.75ms-2cycles 110: 2.75ms-3cycles 111: 2.75ms-4cycles
Reserved	[7]	Reserved
CECDAT	[6:4]	Time to detect CEC signal as valid (0 or 1) 000: 1.05ms 001: 1.05ms+2cycles 010: 1.05ms+4cycles 011: 1.05ms+6cycles 100: 1.05ms-2cycles 101: 1.05ms-4cycles 110: 1.05ms-6cycles 111: Reserved
CECTOUT	[3:2]	Number of cycles to determine timeout 00: 1 bit cycle 01: 2 bit cycles

Register Field	Bit	Description
		10: 3 bit cycles 11: Reserved
CECRIHLD	[1]	Suspend CEC receive error interrupt 0: Disable 1: Enable
CECOTH	[0]	For Testing only. Enable the CEC reception when address does not match 0: Disable 1: Enable

6.5.6. CEC Receive Control Register 2 (CECRCTL2: 0x0618)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved	CECSWAV3[2:0]			Reserved	CECSWAV2[2:0]		
Type	RO	R/W			RO	R/W		
Default	0x0	0x0			0x0	0x0		
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved	CECSWAV1[2:0]			Reserved	CECSWAV0[2:0]		
Type	RO	R/W			RO	R/W		
Default	0x0	0x0			0x0	0x0		

Table 6-18 CEC Receive Control Register 2

Register Field	Bit	Description
Reserved	[15]	Reserved
CECSWAV3	[14:12]	Maximum time to detect start bit 000: 4.7ms 001: 4.7ms +1cycle 010: 4.7ms +2cycles 011: 4.7ms +3cycles 100: 4.7ms +4cycles 101: 4.7ms +5cycles 110: 4.7ms +6cycles 111: 4.7ms +7cycles
Reserved	[11]	Reserved
CECSWAV2	[10:8]	Minimum time to detect start bit 000: 4.3ms 001: 4.3ms -1cycle 010: 4.3ms -2cycles 011: 4.3ms -3cycles 100: 4.3ms -4cycles 101: 4.3ms -5cycles 110: 4.3ms -6cycles 111: 4.3ms -7cycles
Reserved	[7]	Reserved
CECSWAV1	[6:4]	Maximum time to detect start bit rising 000: 3.9ms 001: 3.9ms +1cycle 010: 3.9ms +2cycles 011: 3.9ms +3cycles 100: 3.9ms +4cycles 101: 3.9ms +5cycles 110: 3.9ms +6cycles 111: 3.9ms +7cycles
Reserved	[3]	Reserved

Register Field	Bit	Description
CECSWAV0	[2:0]	Minimum time to detect start bit rising 000: 3.5ms 001: 3.5ms -1cycle 010: 3.5ms -2cycles 011: 3.5ms -3cycles 100: 3.5ms -4cycles 101: 3.5ms -5cycles 110: 3.5ms -6cycles 111: 3.5ms -7cycles

6.5.7. CEC Receive Control Register 3 (CECRCTL3: 0x061C)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO							
Default	0x0							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved	CECWAV3[2:0]			Reserved	CECWAV2[2:0]		
Type	RO	R/W			RO	R/W		
Default	0x0	0x0			0x0	0x0		
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved	CECWAV1[2:0]			Reserved	CECWAV0[2:0]		
Type	RO	R/W			R	R/W		
Default	0x0	0x0			0x0	0x0		
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B6**
Name	Reserved			CECACKEI	CECMINEI	CECMAXEI	CECRSTEI	CECWAVEI
Type	RO			R/W	R/W	R/W	R/W	R/W
Default	0x0			0x0	0x0	0x0	0x0	0x0

Table 6-19 CEC Receive Control Register 3

Register Field	Bit	Description
Reserved	[31:23]	Reserved
CECWAV3	[22:20]	The latest rising timing of logical 0 000: 1.7ms 001: 1.7ms +1cycle 010: 1.7ms +2cycles 011: 1.7ms +3cycles 100: 1.7ms +4cycles 101: 1.7ms +5cycles 110: 1.7ms +6cycles 111: 1.7ms +7cycles
Reserved	[19]	Reserved
CECWAV2	[18:16]	The fastest rising timing of a logical 0 000: 1.3ms 001: 1.3ms -1cycle 010: 1.3ms -2cycles 011: 1.3ms -3cycles 100: 1.3ms -4cycles 101: 1.3ms -5cycles 110: 1.3ms -6cycles 111: 1.3ms -7cycles
Reserved	[15]	Reserved
CECWAV1	[14:12]	The latest rising timing of logical 1 000: 0.8ms 001: 0.8ms +1cycle 010: 0.8ms +2cycles

Register Field	Bit	Description
		011: 0.8ms +3cycles 100: 0.8ms +4cycles 101: 0.8ms +5cycles 110: 0.8ms +6cycles 111: 0.8ms +7cycles
Reserved	[11]	Reserved
CECWAV0	[10:8]	The fastest rising of a logical 1 000: 0.4ms 001: 0.4ms -1cycle 010: 0.4ms -2cycles 111: 0.4ms -3cycles 100: 0.4ms -4cycles 101: 0.4ms -5cycles 110: 0.4ms -6cycles 111: 0.4ms -7cycles
Reserved	[7:5]	Reserved
CECACKEI	[4]	ACK collision error interrupt enable 0: Disable 1: Enable
CECMINEI	[3]	Minimum timing error detection interrupt enable 0: Disable 1: Enable
CECMAXEI	[2]	Maximum timing error detection interrupt enable 0: Disable 1: Enable
CECRSTEI	[1]	Start bit interrupt enable 0: Disable 1: Enable
CECWAVEI	[0]	Waveform error interrupt enable 0: Disable 1: Enable

6.5.8. CEC Transmit Enable Register (CECTEN: 0x0620)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved						CECTBusy	CECTEN
Type	RO						RO	R/W
Default	0x0						0x0	0x0

Table 6-20 Audio Data Double Word Count Register 2

Register Field	Bit	Description
Reserved	[15:2]	Reserved
CECTBusy	[1]	CEC transmit state (read only) 0: idle 1: active
CECTEN	[0]	CEC transmission control 0: Disable 1: Enable

6.5.9. CEC Transmit Control Register (CECTCTL: 0x0628)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO							
Default	0x0							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved	CECSTRS[2:0]			Reserved	CECSPRD[2:0]		
Type	RO	R/W			RO	R/W		
Default	0x0	0x0			0x0	0x0		
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved	CECDTRS[2:0]			CECDPRD[3:0]			
Type	RO	R/W			R/W			
Default	0x0	0x0			0x0			
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved			CECBRD	CECFREE[3:0]			
Type	RO			R/W	R/W			
Default	0x0			0x0	0x0			

Table 6-21 CEC Transmit Control Register

Register Field	Bit	Description
Reserved	[31:23]	Reserved
CECSTRS	[22:20]	Rising cycle time of the start bit – between the default values and 0-7 cycles 000: default value (~ 3.7ms) 001: default value – 1 cycle 010: default value – 2 cycles 011: default value – 3 cycles 100: default value – 4 cycles 101: default value – 5 cycles 110: default value – 6 cycles 111: default value – 7 cycles
Reserved	[19]	Reserved
CECSPRD	[18:16]	Start bit cycle time 000: RV 001: RV –1cycle 010: RV –2cycle 011: RV –3cycle 100: RV –4cycle 101: RV –5cycle 110: RV –6cycle 111: RV –7cycle
Reserved	[15]	Reserved
CECDTRS	[14:12]	Rising cycle time of data bit 000: RV 001: RV –1cycle 010: RV –2cycle 011: RV –3cycle 100: RV –4cycle 101: RV –5cycle 110: RV –6cycle 111: RV –7cycle
CECDPRD	[11:8]	Data bit cycle time 0000: RV 0001: RV – 1 cycle 0010: RV – 2 cycles 0011: RV – 3 cycles 0100: RV – 4 cycles 1000: RV – 8 cycles 1001: RV – 9 cycles 1010: RV – 10 cycles 1011: RV – 11 cycles 1100: RV – 12 cycles

		0101: RV – 5 cycles 1101: RV – 13 cycles 0110: RV – 6 cycles 1110: RV – 14 cycles 0111: RV – 7 cycles 1111: RV – 15 cycles
Reserved	[7:5]	Reserved
CECBRD	[4]	Broadcast transmit enable 1'b0: disable 1'b1: enable
CECFREE	[3:0]	Number of cycles for checking the line to be inactive before the start of transmission 0000: 1-bit cycle 1000: 9 bit cycle 0001: 2 bit cycle 1001: 10 bit cycle 0010: 3 bit cycle 1010: 11 bit cycle 0011: 4 bit cycle 1011: 12 bit cycle 0100: 5 bit cycle 1100: 13 bit cycle 0101: 6 bit cycle 1101: 14 bit cycle 0110: 7 bit cycle 1110: 15 bit cycle 0111: 8 bit cycle 1111: 16 bit cycle

6.5.10. CEC Receive Interrupt Status Register (CECRSTAT: 0x062C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved	CECRIWA	CECRIOR	CECRIACK	CECRIMIN	CECRIMAX	CECRISTA	CECRIEND
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0x0	0x0	0x0	0x0	0x0	0x2	0x0	0x0

Table 6-22 CEC Receive Interrupt Status Register

Register Field	Bit	Description
Reserved	[15:7]	Reserved
CECRIWA	[6]	CEC Waveform error interrupt flag
CECRIOR	[5]	Receive buffer full flag
CECRIACK	[4]	ACK collision detection flag
CECRIMIN	[3]	Bit cycle time is less than minimum time flag
CECRIMAX	[2]	Bit cycle time is greater than maximum time flag
CECRISTA	[1]	Start bit detection flag
CECRIEND	[0]	Reception of CEC message with EOM

6.5.11. CEC Transmit Interrupt Status Register (CECTSTAT: 0x0630)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved			CECTIUR	CECTIACK	CECTIAL	CECTIEND	Reserved
Type	RO			RO	RO	RO	RO	RO
Default	0x0			0x0	0x0	0x0	0x0	0x0

Table 6-23 Interrupt Flag Register

Register Field	Bit	Description
Reserved	[15:5]	Reserved
CECTIUR	[4]	Transmission is completed and the transmit buffer is empty
CECTIACK	[3]	ACK error detection flag
CECTIAL	[2]	Arbitration loss flag (“0” is detected while transmit “1”)
CECTIEND	[1]	Data block transmission completion flag
Reserved	[0]	Reserved

6.5.12. CEC Receive Buffer Registers (01-16) (CECRBUF01-16: 0x0634-0x0670)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						CECRACK	CECEOM
Type	RO						RO	RO
Default	0x0						0x0	0x0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	CECRBYTE[7:0]							
Type	RO							
Default	0x0							

Table 6-24 CEC Receive Buffer Registers (01-16)

Register Field	Bit	Description
Reserved	[15:10]	Reserved
CECRACK	[9]	ACK bit received
CECEOM	[8]	EOM bit received
CECRBYTE	[7:0]	CEC byte received

6.5.13. CEC Transmit Buffer Registers (01-16) (CECTBUF01-16: 0x0674-0x06B0)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							CECTEOM
Type	RO							R/W
Default	0x0							0x0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	CECTBYTE[7:0]							
Type	R/W							
Default	0x0							

Table 6-25 CEC Transmit Buffer Registers (01-16)

Register Field	Bit	Description
Reserved	[15:9]	Reserved
CECTEOM	[8]	EOM bit value to be transmitted
CECTBYTE	[7:0]	Byte data to be transmitted

6.5.14. CEC Receive Byte Counter Register (CECRCTR: 0x06B4)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved			CECRCTR[4:0]				
Type	RO			RO				
Default	0x0			0x0				

Table 6-26 Interrupt Flag Register

Register Field	Bit	Description
Reserved	[15:5]	Reserved
CECRCTR	[4:0]	Numbers of bytes received

6.5.15. CEC Interrupt Enable Register (CECIMSK: 0x06C0)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved						CECTIM	CECRIM
Type	RO						R/W	R/W
Default	0x0						0x0	0x0

Table 6-27 CEC Interrupt Enable Register

Register Field	Bit	Description
Reserved	[15:2]	Reserved
CECTIM	[1]	CEC Transmit status interrupt enable 1'b0: disable 1'b1: enable
CECRIM	[0]	CEC Receive status interrupt enable 1'b0: disable 1'b1: enable

6.5.16. CEC Interrupt Clear Register (CECICLR: 0x06CC)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved						CECTClr	CECRClr
Type	RO						WO	WO
Default	0x0						0x0	0x0

Table 6-28 CEC Interrupt Enable Register

Register Field	Bit	Description
Reserved	[15:2]	Reserved
CECTIM	[1]	Host writes "1" to this bit to clear CEC Transmit status interrupt
CECRIM	[0]	Host writes "1" to this bit to clear CEC Receive status interrupt

6.5.17. IR CONTROL REGISTER (IR_CONTROL: 0x7082)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved						IRInv	Reserved
Type	RO						R/W	RO
Default	0x00						0	0

Register Field	Bit	Default	Description
Reserved	[7:2]	0x0	-
IRInv	[1]	0x0	**IRInv** 1: Invert IR Polarity
Reserved	[0]	0x0	Reserved

6.6. HDMI Rx System Control

6.6.1. INTERRUPT0 REGISTER (HDMI_INT0) (0x8500)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	I_KEY	Reserved					I_MISC	I_PHYERR
Type	RO	RO					RO	RO
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
I_KEY	[7]	0	KEY-EDID (address 0x85_0F) interrupt 0: No interrupt 1: Interrupt generated
Reserved	[6:2]	0	Reserved
I_MISC	[1]	0	MISC (address 0x85_0B) interrupt 0: No interrupt 1: Interrupt generated
I_PHYERR	[0]	0	PHY-ERR (address 0x85_0A) interrupt 0: No interrupt 1: Interrupt generated

6.6.2. INTERRUPT1 REGISTER (HDMI_INT1) (0x8501)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	I_GBD	I_HDCP	I_ERR	I_AUD	I_CBIT	I_PACKET	I_CLK	I_SYS
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
I_GBD	[7]	0	GBD (address 0x85_09) interrupt 0: No interrupt, 1: Interrupt generated
I_HDCP	[6]	0	HDCP (address 0x85_08) interrupt 0: No interrupt, 1: Interrupt generated
I_ERR	[5]	0	ERR (address 0x85_07) interrupt 0: No interrupt, 1: Interrupt generated
I_AUD	[4]	0	Audio Buffer (address 0x85_06) interrupt 0: No interrupt, 1: Interrupt generated
I_CBIT	[3]	0	Audio CBIT (address 0x85_05) interrupt 0: No interrupt, 1: Interrupt generated
I_PACKET	[2]	0	Info Packet (address 0x85_04) interrupt 0: No interrupt, 1: Interrupt generated
I_CLK	[1]	0	Pixel CLK (address 0x85_03) interrupt 0: No interrupt, 1: Interrupt generated
I_SYS	[0]	0	SYSTEM (address 0x85_02) interrupt 0: No interrupt, 1: Interrupt generated

6.6.3. SYSTEM INTERRUPT (SYS_INT) (0x8502)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	I_ACR_CTS	I_ACRN	I_DVI	I_HDMI	I_NOPMBDET	I_DPMBDET	I_TMDS	I_DDC
Type	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
I_ACR_CTS	[7]	0	Receive CTS update interrupt 0: No interrupt 1: Interrupt generated
I_ACRN	[6]	0	Receive N update interrupt 0: No interrupt 1: Interrupt generated
I_DVI	[5]	0	HDMI → DVI change detection interrupt 0: No interrupt 1: Interrupt generated
I_HDMI	[4]	0	DVI → HDMI change detection interrupt 0: No interrupt 1: Interrupt generated
I_NOPMBDET	[3]	0	No DataIsland Preamble detection interrupt 0: No interrupt 1: Interrupt generated
I_DPMBDET	[2]	0	With DataIsland Preamble detection interrupt 0: No interrupt 1: Interrupt generated
I_TMDS	[1]	0	TMDS amplitude change interrupt 0: No interrupt 1: Presence change detected (PHY squelch ON/OFF change detected)
I_DDC	[0]	0	DDC power change detection interrupt 0: No interrupt 1: 0V ⇔ 5V change detected

6.6.4. CLOCK INTERRUPT (CLK_INT) (0x8503)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved	I_OUT_H_CHG	I_IN_DE_CHG	I_IN_HV_CHG	I_DC_CHG	I_PXCLK_CHG	I_PHYCLK_CHG	I_TMDSCLK_CHG
Type	R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R
Default	x	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
Reserved	[7]	0	-
I_OUT_H_CHG	[6]	0	(Output side) H counter change detection interrupt 0: No interrupt 1: Interrupt generated
I_IN_DE_CHG	[5]	0	(Input side) DE size and position change detection interrupt 0: No interrupt 1: Interrupt generated

I_IN_HV_CHG	[4]	0	(Input side) HV counter change detection interrupt 0: No interrupt 1: Interrupt generated
I_DC_CHG	[3]	0	Deep Color mode change detection interrupt 0: No interrupt 1: Interrupt generated
I_PXCLK_CHG	[2]	0	Pixel CLK change detection interrupt 0: No interrupt 1: Interrupt generated
I_PHYCLK_CHG	[1]	0	PHY PLL CLK change detection interrupt 0: No interrupt 1: Interrupt generated
I_TMDSCLK_CHG	[0]	0	TMDS CLK change detection interrupt 0: No interrupt 1: Interrupt generated

6.6.5. PACKET INTERRUPT (PACKET_INT) (0x8504)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	I_PK_ISRC2	I_PK_ISRC	I_PK_ACP	I_PK_VS	I_PK_SPD	I_PK_MS	I_PK_AUD	I_PK_AVI
Type	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
I_PK_ISRC2	[7]	0	ISRC2 packet update interrupt 0: No interrupt 1: Interrupt generated
I_PK_ISRC	[6]	0	ISRC1 packet update interrupt 0: No interrupt 1: Interrupt generated
I_PK_ACP	[5]	0	ACP packet update interrupt 0: No interrupt 1: Interrupt generated
I_PK_VS	[4]	0	861B VS_info packet update interrupt 0: No interrupt 1: Interrupt generated
I_PK_SPD	[3]	0	861B SPD_info packet update interrupt 0: No interrupt 1: Interrupt generated
I_PK_MS	[2]	0	861B MS_info packet update interrupt 0: No interrupt 1: Interrupt generated
I_PK_AUD	[1]	0	861B AUD_info packet update interrupt 0: No interrupt 1: Interrupt generated
I_PK_AVI	[0]	0	861B AVI_info packet update interrupt 0: No interrupt 1: Interrupt generated

Note: Interrupt is generated only when receive content has changed.
If the same data is repeatedly received, interrupt is not generated.

6.6.6. CBIT INTERRUPT (CBIT_INT) (0x8505)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	I_AF_LOCK	I_AF_UNLOCK	I_AU_DST	I_AU_DSD	I_AU_HBR	I_CBIT_NLPCM	I_CBIT_FS	I_CBIT
Type	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
I_AF_LOCK	[7]	0	Audio clock frequency lock detection interrupt 0: No interrupt 1: Interrupt generated
I_AF_UNLOCK	[6]	0	Audio clock frequency unlock detection interrupt 0: No interrupt 1: Interrupt generated
I_AU_DST	[5]	0	DST packet detection interrupt 0: No interrupt 1: Interrupt generated
I_AU_DSD	[4]	0	DSD packet detection interrupt 0: No interrupt 1: Interrupt generated
I_AU_HBR	[3]	0	HBR packet detection interrupt 0: No interrupt 1: Interrupt generated
I_CBIT_NLPCM	[2]	0	Normal Audio LPCM ⇔ NLPCM change detection interrupt 0: No interrupt 1: Interrupt generated
I_CBIT_FS	[1]	0	Receive data FS update interrupt 0: No interrupt 1: Interrupt generated
I_CBIT	[0]	0	Receive C_bit data [47:0] update interrupt 0: No interrupt 1: Interrupt generated

6.6.7. AUDIO INTERRUPT (AUDIO_INT) (0x8506)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	I_BUF_OVER	I_BUF_NO2	I_BUF_NO1	I_BUF_CENTER	I_BUF_NU1	I_BUF_NU2	I_BUF_UNDER	I_BUFINIT_END
Type	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
I_BUF_OVER	[7]	0	Buffer Over flow detection interrupt 0: No interrupt 1: Interrupt generated
I_BUF_NO2	[6]	0	Buffer Nearly Over (threshold 2) detection interrupt 0: No interrupt 1: Interrupt generated
I_BUF_NO1	[5]	0	Buffer Nearly Over (threshold 1) detection interrupt 0: No interrupt 1: Interrupt generated
I_BUF_CENTER	[4]	0	Buffer CENTER detection interrupt 0: No interrupt 1: Interrupt generated
I_BUF_NU1	[3]	0	Buffer Nearly Under (threshold 1) detection interrupt 0: No interrupt 1: Interrupt generated
I_BUF_NU2	[2]	0	Buffer Nearly Under (threshold 2) detection interrupt 0: No interrupt 1: Interrupt generated
I_BUF_UNDER	[1]	0	Buffer Under flow detection interrupt 0: No interrupt 1: Interrupt generated
I_BUFINIT_END	[0]	0	Buffer initial operation completed interrupt 0: No interrupt 1: Interrupt generated

6.6.8. ERROR INTERRUPT (ERR_INT) (0x8507)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	I_EESS_ERR	I_AU_FRAME	I_NO_ACP	I_NO_AVI	I_DC_NOCD	I_DC_DEERR	I_DC_BUFERR	I_DC_PPERR
Type	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
I_EESS_ERR	[7]	0	EESS error generation detection interrupt Note1 [6] W1C/R 1'b0 0: No interrupt 1: Interrupt generate
I_AU_FRAME	[6]	0	60958Frame discontinuous change detection interrupt 0: No interrupt 1: Interrupt generated
I_NO_ACP	[5]	0	ACP Packet receive cutoff detection interrupt 0: No interrupt 1: Interrupt generated
I_NO_AVI	[4]	0	AVI Packet receive cut detection interrupt 0: No interrupt 1: Interrupt generated
I_DC_NOCD	[3]	0	Deep Color CD = 0 (or not defined) generates 24bit mode auto move 0: No interrupt 1: Interrupt generated
I_DC_DEERR	[2]	0	In Deep Color Packing Group, DE position abnormal generation 0: No interrupt 1: Interrupt generated
I_DC_BUFERR	[1]	0	Deep Color FIFO flow generation 0: No interrupt 1: Interrupt generated
I_DC_PPERR	[0]	0	Deep Color UnPack phase dis-unified generation 0: No interrupt 1: Interrupt generated

Note1: During HDMI (= EESS) mode, detects state where Enc_Disable、Enc_Enable can no longer be detected during HDCP decoding operation.
Used for detecting the abnormal state where HDCP goes OFF without te send side sending Enc_Disable.

6.6.9. HDCP INTERRUPT (HDCP_INT) (0x8508)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	I_AVM_SET	I_AVM_CLR	I_LINKERR	I_SHA_END	I_R0_END	I_KM_END	I_AKSV_END	I_AN_END
Type	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R	W1C/R
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
I_AVM_SET	[7]	0	SET AVMUTE receive interrupt 0: No receive 1: With receive
I_AVM_CLR	[6]	0	CLRAE AVMUTE receive interrupt 0: No receive 1: With receive
I_LINKERR	[5]	0	Link error detection interrupt Note1 0: No link error 1: Link error generated
I_SHA_END	[4]	0	V´value operation ended interrupt 0: During idle or operation 1: Operation ended
I_R0_END	[3]	0	Ks´, M0´, R0´ operation ended interrupt 0: During idle or operation 1: Operation ended
I_KM_END	[2]	0	Km´ operation ended interrupt 0: During idle or operation 1: Operation ended
I_AKSV_END	[1]	0	AKSV write completed interrupt 0: During idle or write 1: Write completed notification
I_AN_END	[0]	0	AN write completed interrupt 0: During idle or write 1: Write completed notification

Note1: This interrupt is generated when other device termination of HDCP encoding is detected.
(Detects IDLE State after HDCP certification No.3 part)
However, it may be set up even during HDMI SET_AVMUTE.

6.6.10. GBD INTERRUPT (GBD_INT) (0x8509)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	I_GBD_PKERR	I_GBD_ACLR	I_P1GBD_CHG	I_P0GBD_CHG	Reserved	I_P1GBD_DET	I_GBD_OFF	I_GBD_ON
Type	W1C/R	W1C/R	W1C/R	W1C/R	RO	W1C/R	W1C/R	W1C/R
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
I_GBD_PKERR	[7]	0	GBD packet receive ERR generation interrupt 0: No interrupt 1: Interrupt generated
I_GBD_ACLR	[6]	0	GBD packet receive cutoff detection interrupt 0: No interrupt 1: Interrupt generated (cutoff generated)
I_P1GBD_CHG	[5]	0	Valid P1 GBD update interrupt 0: No interrupt 1: Interrupt generated (GBD-RAM update generated)

I_P0GBD_CHG	[4]	0	Valid P0 GBD update interrupt 0: No interrupt 1: Interrupt generated (GBD-RAM update generated)
Reserved	[3]	0	Reserved
I_P1GBD_DET	[2]	0	P1 GBD data receive generation interrupt 0: No interrupt 1: Interrupt generated Note: Not related to change in packet content, generated each time packet is received.
I_GBD_OFF	[1]	0	Valid GBD yes → no change generation interrupt 0: No interrupt 1: Interrupt generated
I_GBD_ON	[0]	0	Valid GBD no → yes change generation interrupt 0: No interrupt 1: Interrupt generated

6.6.11. MISC INTERRUPT (MISC_INT) (0x850b)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved			I_AS_LAYOUT	I_NO_SPD	I_NO_VS	I_SYNC_CHG	I_AUDIO_MUTE
Type	RO			W1C/R	W1C/R	W1C/R	W1C/R	W1C/R
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
Reserved	[7:5]	0	Reserved
I_AS_LAYOUT	[4]	0	audio Layout Bit change detection interrupt 0: No interrupt 1: Interrupt generated
I_NO_SPD	[3]	0	SPD_Info packet receive cutoff detection interrupt 0: No interrupt 1: Interrupt generated
I_NO_VS	[2]	0	VS_Info packet receive cutoff detection interrupt 0: No interrupt 1: Interrupt generated
I_SYNC_CHG	[1]	0	Video sync signal state change detection interrupt 0: No interrupt 1: Interrupt generated
I_AUDIO_MUTE	[0]	0	Audio MUTE generation interrupt 0: No interrupt 1: Interrupt generated

6.6.12. KEY INTERRUPT (KEY_INT) (0x850f)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved	I_ED_RDEND	I_ED_RSTEND	I_ED_ERR	I_BKSV_ERR	I_KD_RDEND	I_KD_RSTEND	I_KD_ERR
Type	RO	W1C/R	W1C/R	W1C/R	RO	W1C/R	W1C/R	W1C/R
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
Reserved	[7]	0	Reserved
I_ED_RDEND	[6]	0	EDID RAM forward command completed interrupt 0: During idle or forwarding 1: EDID forward completed
I_ED_RSTEND	[5]	0	EDID-EEPROM reset command completed interrupt 0: During reset operation or command not issued 1: Reset completed
I_ED_ERR	[4]	0	EDID-EEPROM ACK error interrupt 0: No error 1: Error generation notification (No slave address ACK from EEPROM)
I_BKSV_ERR	[3]	0	BKSV data check error interrupt (1/0 number) 0: No error 1: Error generation notification
I_KD_RDEND	[2]	0	Device key forward completed interrupt 0: During idle or forwarding 1: Forward completed notification
I_KD_RSTEND	[1]	0	KEY-EEPROM reset operation completed interrupt 0: During idle or reset operation 1: Reset completed notification
I_KD_ERR	[0]	0	KEY-EEPROM ACK error interrupt 0: No error 1: Error generation notification (No slave address ACK from Key EEPROM)

6.6.13. SYS INTERRUPT MASK (SYS_INTM) (0x8512)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	M_ACR_CTS	M_ACR_N	M_DVI_DET	M_HDMI_DET	M_NOPMBDET	M_BPMBDET	M_TMDS	M_DDC
Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	1	1	1	1	1	1	1	1

Register Field	Bit	Default	Description
M_ACR_CTS	[7]	1	Receive CTS update interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_ACR_N	[6]	1	Receive N value update interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_DVI_DET	[5]	1	HDMI → DVI change detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_HDMI_DET	[4]	1	DVI → HDMI change detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_NOPMBDET	[3]	1	No DataIsland Preamble detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_BPMBDET	[2]	1	With DataIsland Preamble detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_TMDS	[1]	1	TMDS amplitude change detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_DDC	[0]	1	DDC power change detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)

6.6.14. CLK INTERRUPT MASK (CLK_INTM) (0x8513)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved	M_OUT_H_CHG	M_IN_DE_CHG	M_IN_HV_CHG	M_DC_CHG	M_PXCLK_CHG	M_PHYCLK_CHG	M_TMDS_CHG
Type	R	RW	RW	RW	RW	RW	RW	RW
Default	1	1	1	1	1	1	1	1

Register Field	Bit	Default	Description
Reserved	[7]	1	-
M_OUT_H_CHG	[6]	1	(Output side) H counter change detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_IN_DE_CHG	[5]	1	(Input side) DE size and position change detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_IN_HV_CHG	[4]	1	(Input side) HV counter change detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)

M_DC_CHG	[3]	1	Deep Color change detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_PXCLK_CHG	[2]	1	Pixel CLK change detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_PHYCLK_CHG	[1]	1	PHY PLL CLK change detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_TMDS_CHG	[0]	1	TMDS CLK change detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)

6.6.15. PACKET INTERRUPT MASK (PACKET_INTM) (0x8514)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	M_PK_ISRC2	M_PK_ISRC	M_PK_ACP	M_PK_VS	M_PK_SPD	M_PK_MS	M_PK_AUD	M_PK_AVI
Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	1	1	1	1	1	1	1	1

Register Field	Bit	Default	Description
M_PK_ISRC2	[7]	1	ISRC2 packet receive interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_PK_ISRC	[6]	1	ISRC1 packet receive interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_PK_ACP	[5]	1	ACP packet receive interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_PK_VS	[4]	1	861B VS_info packet update interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_PK_SPD	[3]	1	861B SPD_info packet update interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_PK_MS	[2]	1	861B MS_info packet update interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_PK_AUD	[1]	1	861B AUD_info packet update interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_PK_AVI	[0]	1	861B AVI_info packet update interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)

6.6.16. CBIT INTERRUPT MASK (CBIT_INTM) (0x8515)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	M_AF_LOCK	M_AF_UNLOCK	M_AU_DST	M_AU_DSD	M_AU_HBR	M_CBIT_NLPCM	M_CBIT_FS	M_CBIT
Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	1	1	1	1	1	1	1	1

Register Field	Bit	Default	Description
M_AF_LOCK	[7]	1	Audio clock frequency lock detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_AF_UNLOCK	[6]	1	Audio clock frequency unlock detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_AU_DST	[5]	1	DST Audio packet receive detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_AU_DSD	[4]	1	DSD Audio packet receive detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_AU_HBR	[3]	1	HBR Audio packet receive detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_CBIT_NLPCM	[2]	1	Receive data LPCM⇔NLPCM change detection interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_CBIT_FS	[1]	1	Receive data FS update interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)
M_CBIT	[0]	1	Receive C_bit data [39:0] update interrupt mask 0: Mask OFF, 1: Mask ON (Interrupt prohibited)

6.6.17. AUDIO INTERRUPT MASK (AUDIO_INTM) (0x8516)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	M_BUF_OVER	M_BUF_NO2	M_BUF_NO1	M_BUF_CENTER	M_BUF_NU1	M_BUF_NU2	M_BUF_UNDER	M_BUFINIT_END
Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	1	1	1	1	1	1	1	1

Register Field	Bit	Default	Description
M_BUF_OVER	[7]	1	Buffer Over flow detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_BUF_NO2	[6]	1	Buffer Nearly Over (Threshold 2) detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_BUF_NO1	[5]	1	Buffer Nearly Over (Threshold 1) detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)

M_BUF_CENTER	[4]	1	Buffer CENTER detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_BUF_NU1	[3]	1	Buffer Nearly Under (Threshold 1) detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_BUF_NU2	[2]	1	Buffer Nearly Under (Threshold 2) detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_BUF_UNDER	[1]	1	Buffer Under flow detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_BUFINIT_END	[0]	1	Buffer initialization operation completed interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)

6.6.18. ERR INTERRUPT MASK (ERR_INTM) (0x8517)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	M_EESS_ERR	M_AU_FRAME	M_NO_ACP	M_NO_AVI	M_DC_NOCD	M_DC_DEERR	M_DC_BUFERR	M_DC_PPERR
Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	1	1	1	1	1	1	1	1

Register Field	Bit	Default	Description
M_EESS_ERR	[7]	1	EESS error occurrence detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_AU_FRAME	[6]	1	Audio 60958Frame discontinuous detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_NO_ACP	[5]	1	ACP packet receive cutoff detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_NO_AVI	[4]	1	AVI packet receive cutoff detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_DC_NOCD	[3]	1	Deep color 24bit mode auto move occurrence interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_DC_DEERR	[2]	1	In Deep Color Packing Group, DE position abnormal occurrence interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_DC_BUFERR	[1]	1	Deep Color FIFO flow occurrence interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_DC_PPERR	[0]	1	Deep Color UnPack phase dis-unify occurrence 0: Mask OFF 1: Mask ON (Interrupt prohibited)

6.6.19. HDCP INTERRUPT MASK (HDCP_INTM) (0x8518)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	M_AVM_SET	M_AVM_CLR	M_LINKERR	M_SHA_END	M_R0_END	M_KM_END	M_AKSV_END	M_AN_END
Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	1	1	1	1	1	1	1	1

Register Field	Bit	Default	Description
M_AVM_SET	[7]	1	SET AVMUTE receive interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_AVM_CLR	[6]	1	CLRAE AVMUTE receive interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_LINKERR	[5]	1	Link error detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_SHA_END	[4]	1	V´ value operation completed interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_R0_END	[3]	1	Ks´, M0´, R0´ operation completed interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_KM_END	[2]	1	Km´ operation completed interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_AKSV_END	[1]	1	AKSV write completed interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_AN_END	[0]	1	AN write completed interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)

6.6.20. GBD INTERRUPT MASK (GBD_INTM) (0x8519)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	M_GBD_PKERR	M_GBD_ACLR	M_P1GBD_CHG	M_P0GBD_CHG	Reserved	M_P1GBD_DET	M_GBD_OFF	M_GBB_ON
Type	RW	RW	RW	RW	RO	RW	RW	RW
Default	1	1	1	1	1	1	1	1

Register Field	Bit	Default	Description
M_GBD_PKERR	[7]	1	GBD packet receive error occurrence interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_GBD_ACLR	[6]	1	GBD packet receive cutoff detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_P1GBD_CHG	[5]	1	P1 GBD update interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_P0GBD_CHG	[4]	1	P0 GBD update interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
Reserved	[3]	1	Reserved
M_P1GBD_DET	[2]	1	P1 GBD data receive detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_GBD_OFF	[1]	1	No Valid GBD detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_GBB_ON	[0]	1	With valid GBD detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)

6.6.21. MISC INTERRUPT MASK (MISC_INTM) (0x851b)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved			M_AS_LAYOUT	M_NO_SPD	M_NO_VS	M_SYNC_CHG	M_AUDIO MUTE
Type	RO			RW	RW	RW	RW	RW
Default	0	0	0	1	1	1	1	1

Register Field	Bit	Default	Description
Reserved	[7:5]	0	Reserved
M_AS_LAYOUT	[4]	1	audio Layout Bit change detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_NO_SPD	[3]	1	SPD_Info packet receive cutoff detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)

M_NO_VS	[2]	1	VS_Info packet receive cutoff detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_SYNC_CHG	[1]	1	Video sync signal state change detection interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_AUDIO_MUTE	[0]	1	Audio MUTE generation interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)

6.6.22. KEY INTERRUPT MASK (KEY_INTM) (0x851f)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved	M_ED_RDEND	M_ED_RSTEND	M_ED_ERR	M_BKSV_ERR	M_KD_RDEND	M_KD_RSTEND	M_KD_ERR
Type	RO	RW	RW	RW	RW	RW	RW	RW
Default	1	1	1	1	1	1	1	1

Register Field	Bit	Default	Description
Reserved	[7]	1	Reserved
M_ED_RDEND	[6]	1	EDID RAM forward command completed interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_ED_RSTEND	[5]	1	EDID-EEPROM reset command completed interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_ED_ERR	[4]	1	EDID-EEPROM ACK error interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_BKSV_ERR	[3]	1	BKSV data check error interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_KD_RDEND	[2]	1	Device key forward command completed interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_KD_RSTEND	[1]	1	KEY-EEPROM reset operation completed interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)
M_KD_ERR	[0]	1	KEY-EEPROM ACK error interrupt mask 0: Mask OFF 1: Mask ON (Interrupt prohibited)

6.6.23. SYS STATUS (SYS_STATUS) (0x8520)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	S_SYNC	S_AVMUTE	S_HDCP	S_HDMI	S_PHY_SCDT	S_PHY_PLL	S_TMDS	S_DDC5V
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
S_SYNC	[7]	0	Input Video sync signal status 0: No sync signal (unstable) 1: With sync signal (stable) Note: For the generation conditions for this status, follow the address 0x85A5 to 0x85AE settings.
S_AVMUTE	[6]	0	AVMUTE status 0: AVMUTE = OFF 1: AVMUTE = ON
S_HDCP	[5]	0	HDCP status 0: encrypted frame is currently received 1: encrypted frame is not received
S_HDMI	[4]	0	HDMI status 0: DVI 1: HDMI
S_PHY_SCDT	[3]	0	PHY DE detect status (PHY SCDT signal monitor) 0: No DE 1: With DE
S_PHY_PLL	[2]	0	PHY PLL status (PHY PLL_LOCK_IND signal monitor) 0: UnLock 1: Lock
S_TMDS	[1]	0	TMDS input amplitude status (PHY squelch signal monitor) 0: No input amplitude 1: With input amplitude
S_DDC5V	[0]	0	DDC_Power (DDC5V) input status 0: No input 1: With input

6.6.24. VIDEO INPUT STATUS (VI_STATUS) (0x8521)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	S_V_repeat				S_V_format			
Type	RO				RO			
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
S_V_repeat	[7:4]	0	Input Video signal status (Repetition) 0: No Repetition, 1: Repetition = 2, 2: Repetition = 3, 3: Repetition = 4, ・・・・, 9: Repetition = 10

S_V_format	[3:0]	0	Video format status detected from input DE size Note: Shows the status before implementation of correction using repetition. 4'd1 : VGA (Horizontal 631 to 649, Vertical 471 to 489) 4'd2 : 240p/480i (Horizontal 1401 to 1449, Vertical 231 to 249) 4'd3 : 288p/576i (Horizontal 1401 to 1449, Vertical 279 to 297) 4'd4 : W240p/480i (Horizontal 2801 to 2899, Vertical 231 to 249) 4'd5 : W288p/576i (Horizontal 2801 to 2899, Vertical 279 to 297) 4'd6 : 480p (Horizontal 701 to 729, Vertical 471 to 489) 4'd7 : 576p (Horizontal 701 to 729, Vertical 567 to 585) 4'd8 : W480p (Horizontal 1401 to 1449, Vertical 471 to 489) 4'd9 : W576p (Horizontal 1401 to 1449, Vertical 567 to 585) 4'd10 : WW480p (Horizontal 2801 to 2899, Vertical 471 to 489) 4'd11 : WW576p (Horizontal 2801 to 2899, Vertical 567 to 585) 4'd12 : 720p (Horizontal 1261 to 1289, Vertical 711 to 729) 4'd13 : 1035i (Horizontal 1911 to 1929, Vertical 507 to 527) 4'd14 : 1080i (Horizontal 1911 to 1929, Vertical 531 to 549) 4'd15 : 1080p (Horizontal 1911 to 1929, Vertical 1071 to 1089) 4'd0 : Other than above

6.6.25. VIDEO INPUT STATUS1 (VI_STATUS1) (0x8522)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	S_V_GBD	Reserved			S_DeepColor		S_V_422	S_V_interlace
Type	RO	RO			RO		RO	RO
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
S_V_GBD	[7]	0	Effective GBD data status Note1 0: No GBD 1: With GBD
Reserved	[6:4]	0	Reserved
S_DeepColor	[3:2]	0	Deep color status Note2 00: 24bit 01: 30bit 10: 36bit 11: 48bit
S_V_422	[1]	0	Input Video signal status (422 detection) Note3 0: 444 1: 422
S_V_interlace	[0]	0	Input Video signal status (Interlace detection) Note4 0: Progressive 1: Interlace

Note1: During DVI input, judged to be No GBD.
Note2: During DVI input, judged to be 24bit.
Note3: During DVI input, judged to be 444. During HDMI input, judged from the AVI-Info value.
Note4: Progressive/Interlace judgment method follows the address 0x858e[4] bit setting.

6.6.26. AUDIO STATUS0 (AU_STATUS0) (0x8523)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	S_A_MUTE	Reserved	Reserved	S_A_DST	S_A_DSD	S_A_HBR	S_A_NLPCM	S_A_sample
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
S_A_MUTE	[7]	0	AUDIO auto mute status 0: Mute OFF 1: Mute ON
Reserved	[6:5]	0	Reserved
S_A_DST	[4]	0	Compressed 1BIT Audio packet transmission status (1.5 msec update) 0: No DST transmission 1: With DST transmission
S_A_DSD	[3]	0	1BIT Audio packet transmission status (1.5 msec update) 0: No DSD transmission 1: With DSD transmission
S_A_HBR	[2]	0	HBR Audio packet transmission status (1.5 msec update) 0: No HBR transmission 1: With HBR transmission
S_A_NLPCM	[1]	0	Normal AUDIO/HBR AUDIO packet compression stream detection 0: LPCM 1: Compression stream (61937-1)
S_A_sample	[0]	0	Normal AUDIO packet transmission status (1.5 msec update) 0: No AUDIO transmission 1: With AUDIO transmission

6.6.27. AUDIO STATUS1 (AU_STATUS1) (0x8524)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	3D_STRUCURE				S_VS	S_SPD	S_PKERR	S_ACP
Type	RO				RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
3D_STRUCURE	[7:4]	0	3D transmission format information in VS info 0000: Frame packing 0001 Field alternative 0010: Line alternative 0011: Side-by-Side (Full) 0100: L + depth 0101: L + depth + graphics + graphics-depth 0110: Top-and-Bottom 0111: Reserved 1000: Side-by-Side (Half)

			1001-1110: Reserved 1111: Not used Note: Valid when S_VS_VIC_3D (0x8525[5]) is 1
S_VS	[3]	0	VS packet transmission status 0: No VS transmission 1: With VS transmission
S_SPD	[2]	0	SPD packet transmission status 0: No SPD transmission 1: With SPD transmission
S_PKERR	[1]	0	Packet receive error occurrence status 0: No Packet receive error 1: Packet receive error now occurring
S_ACP	[0]	0	ACP packet transmission status 0: No ACP transmission 1: With ACP transmission

6.6.28. VIDEO INPUT STATUS2 (VI_STATUS2) (0x8525)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	S_FP_IP		S_VS_VIC_3D	S_422out	Reserved			S_DC_NOCD
Type	RO		RO	RO	RO			RO
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
S_FP_IP	[7:6]	0	IP judgment result 0x8980[2] due to size (Vertical V size and vertical DE size) or VIC to select whether to use size or VIC to judge. Valid during Frame packing receive. 2'd0: Progressive 2'd1: Interlace 2'd2: VIC = 39
S_VS_VIC_3D	[5]	0	3D format judgment result due to VS info 0: Non-3D format 1: 3D format Note: Valid during HDMI input only. During DVI input, fixed at 0. When VS Info packet HDMI Video format (PB4 [7:5]) = 3'b010, set to 1.
S_422out	[4]	0	Current HDMI block Video output status 0: 444 output 1: 422 output
Reserved	[3:1]	0	Reserved
S_DC_NOCD	[0]	0	Status determining whether Color Depth used in current Deep Color unpack operation is in 24bit mode due to auto move 0: During normal operation (DVI mode or normal CD value) 1: CD = 0 or CD = reserved or Operations due to No GC Packet

6.6.29. CLK STATUS (CLK_STATUS) (0x8526)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	S_V_3D_format				Reserved	Reserved	S_CLK_U21M	S_CLK_DC
Type	RO				RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
S_V_3D_format	[7:4]	0	3D Video format status detected from input DE size Note1 4'd1 : 3D 1080i Frame Packing (Horizontal 1911 to 1929, Vertical 2219 to 2237) 4'd2 : 3D 1080p Frame Packing or L + depth (Horizontal 1911 to 1929, Vertical 2196 to 2214) 4'd3 : 3D 720p Frame Packing or L + depth (Horizontal 1271 to 1289, Vertical 1461 to 1479) 4'd4 : 3D 1080p Line alternative (Horizontal 1911 to 1929, Vertical 2151 to 2169) 4'd5 : 3D 720p Line alternative (Horizontal 1271 to 1289, Vertical 1431 to 1449) 4'd6 : 3D 1080i Side by Side(Full) (Horizontal 3831 to 3849, Vertical 531 to 549) 4'd7 : 3D 1080p Side by Side(Full) (Horizontal 3831 to 3849, Vertical 1071 to 1089) 4'd8 : 3D 720p Side by Side(Full) (Horizontal 2551 to 2569, Vertical 711 to 729) 4'd9 : 3D 1080p L + depth + G + G_depth (Horizontal 1911 to 1929, Vertical 4446 to 4464) 4'd10 : 3D 720p L + depth + G + G_depth (Horizontal 1271 to 1289, Vertical 2961 to 2979) 4'd0 : Other than above
Reserved	[3:2]	0	-
S_CLK_U21M	[1]	0	TMDS clock detection status at less than 21 MHz 0: 21 MHz or more 1: Less than 21 MHz
S_CLK_DC	[0]	0	TMDS clock DC condition detection status 0: Non DC condition 1: DC condition Note: In reality, DC to frequency of about 1 MHz or less is "1". Responds even when TMDS clock is not input (amplitude 0).

Note1: 3D 1080i Line alternative cannot identify 2D 1080p, 3D Side by Side (Half) cannot identify 2D format, 3D Top-and-Bottom cannot identify 2D format.
The above unidentifiable format is displayed as 4'd0.

6.6.30. PHYERR STATUS (PHYERR_STATUS) (0x8527)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	S_TMDS_TG	S_3YNC_ERR	S_PIT_ERR	S_AT_ERR	S_CDR2_ERR	S_CDR1_ERR	S_CDR0_ERR	S_PLL_ERR
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
S_TMDS_TG	[7]	0	TMDS clock toggle detection 1: With toggle
S_3YNC_ERR	[6]	0	3ch sync error (risk phase) detection 1: Abnormal detection
S_PIT_ERR	[5]	0	PIT abnormal operation detection 1: Abnormal detection
S_AT_ERR	[4]	0	AT abnormal operation detection 1: Abnormal detection
S_CDR2_ERR	[3]	0	CH2 CDR abnormal detection 1: Abnormal detection
S_CDR1_ERR	[2]	0	CH1 CDR abnormal detection 1: Abnormal detection
S_CDR0_ERR	[1]	0	CH0 CDR abnormal detection 1: Abnormal detection
S_PLL_ERR	[0]	0	PLL lock removal detection 1: Abnormal detection

6.6.31. VI STATUS3 (VI_STATUS3) (0x8528)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved			S_V_color				
Type	RO			RO				
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
Reserved	[7:5]	0	Reserved
S_V_color	[4:0]	0	Input Video signal color space judgment status Note1 5'b00 000 RGB (Full) 5'b00 001 RGB (Limited) 5'b00 010 YCbCr601 (Full) 5'b00 011 YCbCr601 (Limited) 5'b00 110 YCbCr709 (Full) 5'b00 111 YCbCr709 (Limited) 5'b00 100 Adobe_RGB (Full) 5'b00 101 Adobe_RGB (Limited) 5'b01 010 xvYCC601 (Full) 5'b01 011 xvYCC601 (Limited) 5'b01 110 xvYCC709 (Full) 5'b01 111 xvYCC709 (Limited)

			5'b10 010 sYCC601 (Full) 5'b10 011 sYCC601 (Limited) 5'b11 010 Adobe_YCC601 (Full) 5'b11 011 Adobe_YCC601 (Limited) Values other than above are not generated. Note: Each bit has the following meaning. [0] Full/Limited identification bit [1] RGB/YCbCr identification bit [2] During RGB input, category identification bit During YCbCr input, 601/709 identification bit [4: 3] During RGB input, 00 fixed During YCbCr input, category identification bit

Note1: During DVI input, judged as RGB. For range identification, follow the address 0x8570[3] bit setting. During HDMI input, judged from AVI-Info value. If at AVI-Info judged to be RGB, for the range identification follow the address 0x8570[2] bit.

6.6.32. PHY CONTROL0 (PHY_CTL0) (0x8531)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved						PHY_SYSCLK_IND	PHY_CTL
Type	RO						R/W	RW
Default	0	0	1	0	0	0	1	0

Register Field	Bit	Default	Description
Reserved	[7:2]	-	Reserved
PHY_SYSCLK_IND	[1]	1	PHY System clock frequency setting 0: 27 or 26 MHz 1: 42 MHz
PHY_CTL	[0]	0	PHY power ON/OFF control mode 0: HOST manual setting 1: DDC5V detection operation (reaction time depends on address 0x8543[1:0] setting)

6.6.33. PHY ENABLE (PHY_EN) (0x8534)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							ENABLE_PHY
Type	RO							RW
Default	0	0	1	1	1	1	1	1

Register Field	Bit	Default	Description
Reserved	[7:1]	-	Reserved
ENABLE_PHY	[0]	1	PHY general SUSPEND control Note1 Note2 0: Suspend 1: Normal Operation

Note1: When PHY power ON/OFF control mode is for “HOST manual setting” (address 0x85_31[0] == 0) only, Write is enabled in this register.

Note2: When PHY power ON/OFF control mode is “DDC5V detect link” (address 0x85_31[0] == 1), DDC5V input = H, and Suspend is automatically cleared.

6.6.34. PHY RESET (PHY_RST) (0x8535)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							RESET_CTRL
Type	RO							RW
Default	1	0	1	1	0	0	1	1

Register Field	Bit	Default	Description
Reserved	[7:1]	-	Reserved
RESET_CTRL	[0]	1	PHY general Reset control 0: Reset 1: Normal Operation

Note: There is no automatic clear function in this register.

6.6.35. PHY PLL (PHY_PLL) (0x8538)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	PLL_CONFIG				PLL_CLK_RANGE			
Type	RW				RW			
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
PLL_CONFIG	[7:4]	0	PHY PLL Band Width adjustment 0000: 4MHz 0001: 6MHz 0010: 8MHz 0011: 10MHz Other than above: prohibit
PLL_CLK_RANGE	[3:0]	0	PHY PLL oscillation clock range setting 0000: 0 to 36 MHz, 0001: 36 to 50 MHz, 0010: 50 to 70 MHz, 0011: 70 to 96 MHz, 0100: 96 to 140 MHz, 0101: 140 to 196 MHz, 0110: 196 to 246 MHz, 0111: 246 MHz or more Other than above: prohibit Note: When in automatic switching mode (address 0x8531[3] == 0), since HW is automatically set, write is impossible from the HOST.

6.6.36. PHY CDR (PHY_CDR) (0x853a)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved	CDR_SCALE			PI_CLK_RANGE			
Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	0	0	0	1	0	0	0	0

Register Field	Bit	Default	Description
Reserved	[7]	0	Reserved
CDR_SCALE	[6:4]	0x1	PHY Phase interpolator step size 001: default Other than above: prohibit
PI_CLK_RANGE	[3:0]	0	PHY Phase interpolator clock range setting 0000: 0 to 70 MHz, 0001: 70 to 170 MHz, 0010: 170 to 270 MHz, 0011: 270 MHz or more Other than above: prohibit Note: When in automatic switching mode (0x8531[4] == 0), Since HW is automatically set, write is impossible from the HOST.

6.6.37. SYS FREQ0 Register (SYS_FREQ0) (0x8540)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SYS_FREQ0							
Type	R/W							
Default	0x68							

Register Field	Bit	Default	Description
SYS_FREQ0	[7:0]	0x68	System clock frequency setting (lower bits) Set System clock frequency setting divide 10000 integer Ex. When system clock at 26 MHz, 2600 = 16'h0A28 When system clock at 27 MHz, 2700 = 16'h0A8C When system clock at 42 MHz, 4200 = 16'h1068

6.6.38. SYS FREQ1 Register (SYS_FREQ1) (0x8541)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SYS_FREQ1							
Type	R/W							
Default	0x10							

Register Field	Bit	Default	Description
SYS_FREQ1	[7:0]	0x10	System clock frequency setting (upper bits)

6.6.39. PClk Detection Threshold (PClk_Det) (0x8542)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved				CLK_DIFF		CLK_DIV	
Type	RW				RW		RW	
Default	0				0		0	

Register Field	Bit	Default	Description
Reserved	[7:4]	0	Reserved
CLK_DIFF	[3:2]	0	TMDS clock, PHY-PLL clock, pixel clock Change detection threshold for frequency change detection interrupt generation 00: 1/32 (3.1%) 01: 1/64 (1.6%) 10: 1/128 (0.8%) 11: 1/256 (0.4%) Note: Normally compares the system clock cycle number during the latest monitoring cycle with the system clock cycle number during the immediately previous monitoring cycle, and generates a change occurrence interrupt when the difference exceeds a set change tolerance range.
CLK_DIV	[1:0]	0	TMDS clock, PHY-PLL clock, pixel clock Monitoring cycle setting for Frequency change detection interrupt generation 00: Measurement clock 4096 division 01: Measurement clock 8192 division 10: Measurement clock 16384 division 11: Measurement clock 32768 division

6.6.40. DDC CONTROL (DDC_CTL) (0x8543)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved				DDC_ACK_POL	DDC_ACTION	DDC5V_MODE	
Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	0	0	1	1	0	0	0	0

Register Field	Bit	Default	Description
Reserved	[7:4]	-	Reserved
DDC_ACK_POL	[3]	0	DDC_ACK output terminal polarity selection 0: H active output 1: L active output
DDC_ACTION	[2]	0	Selection of response method for DDC access from send side 0: DDC is active only while HotPLUG is being output 1: DDC is active when initialization completion INIT_END, 0x854A[0], is asserted

DDC5V_MODE	[1:0]	0	DDC5V_active detect delay setting To prevent chattering in the DDC5V input rising detection area, DDC5V is judged as avtime after a specified time from the rise detect point in time. 00: 0 msec, 01: 50 msec, 10: 100 msec, 11: 200 msec, Note: With this setting, the DDC5V detection interrupt, HOTPLUG automatic output, and PHY automatic power ON timing are all delayed.

6.6.41. HPD Control Register (HPD_CTL) (0x8544)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved			HPD_CTL0	Reserved			HPD_OUT0
Type	RO			-	RO			-
Default	0x0			0x0	0x0			0x0

Register Field	Bit	Default	Description
Reserved	[7:5]	0x0	-
HPD_CTL0	[4]	0x0	HOTPLUG output ON/OFF control mode 0: Host manual setting 1: DDC5V detection interlock
Reserved	[3:1]	0x0	-
HPD_OUT0	[0]	0x0	HOTPLUT Output setting 0: HOTPLUG = “L” output 1: HOTPLUG = “H” output Note: When at DDC5V detection interlock setting, write is not valid. Become status monitor bit.

6.6.42. ANA CONTROL (ANA_CTL) (0x8545)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved		APLL_PCSX		Reserved			ANALOG_ON
Type	RO		RW		RO			RW
Default	0	0	0	1	0	0	0	0

Register Field	Bit	Default	Description
Reserved	[7]	0	Reserved
APLL_PCSX	[5:4]	0X1	PLL charge pump setting for Audio 00: Hi-Z 01: L-fix 10: H-fix 11: normal
Reserved	[3:1]	0	Reserved
ANALOG_ON	[0]	0	DAC/PLL power ON/OFF setting for Audio 0: Power OFF 1: Power ON

Note: When HDMI Not used, and the HDMI Audio clock is stopped, this address is set to 10h.
When using HDMI always set to 31h.

6.6.43. AVMUTE CONTROL (AVM_CTL) (0x8546)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AVM_CTL							
Type	RW							
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
AVM_CTL	[7:0]	0	AVMUTE automatic clear setting After moving to AVMUTEm status, if the SET_AVMUTE/CLEAR_AVMUTE is not received, the allowed time is set. When the set allowed time is reached, AVMUTE status is automatically cleared. Allowed time = Setting value * 100 msec If Setting value = 8'h00, automatic clear is not performed. Note: Valid for Video/Audio mute circuit only. HDCP state machine is re-identified and automatically cleared. If PHY-A/B switching, DDC5V = L, and DVI move has occurred. AVMUTE is cleared regardless of this register setting.

6.6.44. SOFTWARE RESET Register (SOFT_RST) (0x8547)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved		SRST_SH	SRST_HP	SRST_I2CK	SRST_I2CE	SRST_I2CD	SRST_PI
Type	RO		RW	RW	RW	RW	RW	RW
Default	0		0	0	0	0	0	0

Register Field	Bit	Default	Description
Reserved	[7:6]	0	–
SRST_SH	[5]	0	V' value calculation state machine reset 1: Reset (Auto clear)
SRST_HP	[4]	0	HDCP state machine reset 1: Reset (Auto clear)
SRST_I2CK	[3]	0	Key EEPROM I2C state machine reset 1: Reset (Auto clear)
SRST_I2CE	[2]	0	EDID EEPROM I2C state machine reset 1: Reset (Auto clear)
SRST_I2CD	[1]	0	DDC I2C state machine reset, 1: Reset (Auto clear)
SRST_PI	[0]	0	TMDS decoder reset 1: Reset (Auto clear)

6.6.45. INIT END REGISTER (INIT_END) (0x854A)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							INIT_END
Type	RO							RW
Default	0							0

Register Field	Bit	Default	Description
Reserved	[7:1]	0x0	–
INIT_END	[0]	0x0	Initialization completed flag After completion of all initialization settings, write "1" to this register. If 0x8544[4] = 1, HPDO is asserted only when INIT_END is asserted. If 0x8543[2] = 1, DDC is active only when INIT_END is asserted

6.6.46. HDMI_DVI Setting Register (HDMI_DVI) (0x8550)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	DC_DVI_SEL			Reserved			HDMI_DVI	DVI_HDMI
Type	R/W			RO			R/W	R/W
Default	3'b000			0			0	0

Register Field	Bit	Default	Description
DC_DVI_SEL	[7:5]	3'b000	If TMDS DC detection continues through the setting value * 800 msec time, setting automatically moves to DVI mode 000: Auto move OFF
Reserved	[4:2]	2'b00	-
HDMI_DVI	[1]	1'b0	HDMI → DVI move mode setting Note 0: Automatic (HW Write "0" to Bstatus1[4]) 1: Manual (HOST Write "0" to Bstatus1[4])
DVI_HDMI	[0]	1'b0	DVI → HDMI move mode setting Note 0: Automatic (HW Write "1" to Bstatus1[4]) 1: Manual (HOST Write "1" to Bstatus1[4])

Note: DVI/HDMI mode switching is set at the Bstatus1 [4] bit in the HDCP port register (address 0x8842 [4])

6.6.47. HDCP MODE Register (HDCP_MODE) (0x8560)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved		Mode_RST_TN	Line_Rekey	Reserved	AUTO_CLR	Reserved	
Type	RO		RW	RW	RO	RW	RO	
Default	0		1	0	0	1	0	

Register Field	Bit	Default	Description
Reserved	[7:6]	0	-
Mode_RST_TN	[5]	1	HDCP automatic reset when DVI ⇔ HDMI switched 0: Automatic reset OFF 1: Automatic reset ON
Line_Rekey	[4]	0	HDCP Line Rekey timing switch 0: 57clk mode (Data island delay ON) 1: 58clk mode (Data island delay OFF)
Reserved	[3]	0	-
AUTO_CLR	[2]	1	Bcaps[5] KSVINFO_READY (0x8840[5]) auto clear mode 0: No auto clear using AKSV write 1: Auto clear using AKSV write
Reserved	[1:0]	0	-

6.6.48. HDCP COMMAND Register (HDCP_CMD) (0x8561)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved				ShaS	Reserved		UnAuth
Type	RO				RW	RO		RW
Default	0x0				0	0x0		0

Register Field	Bit	Default	Description
Reserved	[7:4]	0	-
ShaS	[3]	0	V' value calculation start command (After calculation completed, automatically clears) 1: Command issued
Reserved	[2:1]	0	-
UnAuth	[0]	0	Unauthorized move command (automatic clear) 1: Command issued

6.6.49. VI MODE REGISTER (VI_MODE) (0x8570)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved			SG_ON	Reserved			
Type	R/W			RW	R/W			
Default	1	1	1	0	1	1	1	0

Register Field	Bit	Default	Description
Reserved	[7:5]	0x7	Do not change reserved value
SG_ON	[4]	0x0	Input HSYNC jitter absorption control 0: Jitter absorption OFF 1: Jitter absorption ON Note: Removes HSYNC jitter of +/- 1clk or less, and corrects HSYNC phase shift of +/- 4clk or less
Reserved	[3:0]	0xE	Do not change reserved value

6.6.50. VOUT SET2 REGISTER (VOUT_SET2) (0x8573)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Sel422	VOUT_422FIL			Reserved		VOutColorMode	
Type	RW	RW			R/W		R/W	
Default	1	0x0			0x0		0x0	

Register Field	Bit	Default	Description
Sel422	[7]	0x1	Video output 422/444 Selection 0: 444 fixed output 1: 422 fixed output Note: Valid only when 0x8574[3] = 1
VOUT_422FIL	[6:4]	0x0	Video Output 422 conversion mode selection 000: Normally 2 tap filter 001: Normally 3 tap filter 010: Normally simple decimation 011: During 444 input, 2tap filter; during 422 input, simple decimation 100: During 444 input, 3tap filter; during 422 input, simple decimation 101: When 444 input or matrix ON, 3tap filter; Other is simple decimation 11x: When 444 input or matrix ON, 3tap filter; Other is simple decimation Note: When 444 fixed output is selected, automatically becomes 422 conversion OFF
Reserved	[3:2]	0x0	-
VOutColorMode	[1:0]	0x0	RGB888 to YUV422 Conversion Mode Setting 00: Through mode (RGB888 Output) 01: Enable RGB888 to YUV422 Conversion (Fixed Color output) 10: Reserved 11: Enable RGB888 to YUV422 Conversion (Use Multiplication Coeff set in registers 0x85b0 to 0x85c1)

6.6.51. VOUT SET3 REGISTER (VOUT_SET3) (0x8574)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VOUT_ LIM	VOUT_ DIV_SEL	VOUT_BIT		VOUT_ EXTCNT	Reserved	VOUT_DIV	
Type	R/W	R/W	R/W		R/W	RO	R/W	
Default	0	0x0	2'b00		0	0	2'b00	

Register Field	Bit	Default	Description
VOUT_LIM	[7]	1'b0	VIDEO output limiter ON/OFF setting 0: Limiter OFF 1: Limiter ON (all "0" and all "1" prohibited) Note: Valid in all Y/G, Cb/B, Cr/R.
VOUT_DIV_SEL	[6]	1'b0	Simple decimation selection 0: Filtered decimation 1: Simple decimation Valid when 0x8574[1:0] = 01 or 1x
VOUT_BIT	[5:4]	2'b00	Output Bit rounding setting 00: 16bit 01: 12bit (Rounded up) 10: 10bit (Rounded up) 11: 8bit (Rounded up)
VOUT_EXTCNT	[3]	1'b0	444 output/422 output switching method selection 0: Follow register bit 0x0004[6] setting 1: Follow register bit 0x8573[7] setting
Reserved	[2]	0x0	-
VOUT_DIV	[1:0]	2'b0	Output horizontal pixel decimation setting 00: OFF (Through) 01: 1/2 decimation 1x: 1/4 decimation Note: If repetition is 5 or more, horizontal thinning process is OFF (Through) regardless of the setting in this register.

6.6.52. VI REAPEAT REGISTER (VI_REP) (0x8576)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VOUT_COLOR_SEL			IN_REP_HEN	IN_REP			
Type	R/W			R/W	R/W			
Default	3'b011			0	0x0			

Register Field	Bit	Default	Description
VOUT_COLOR_SEL	[7:5]	3'b011	Output Color setting 000: RGB Full 001: RGB Limited 010: 601YCbCr Full 011: 601 YCbCr Limited 100: 709 YCbCr Full 101: 709 YCbCr Limited 110: Range conversion（Full → Limited) 111: Range conversion（Limited → Full) Note: When 0x8573[1:0] = 00 (Through), this bit setting is invalid.
IN_REP_HEN	[4]	1'b0	Input Pixel Repetition judgment Automatic/HOST setting switch (Note) 0: Automatic setting 1: HOST setting
IN_REP	[3:0]	4'h0	Input Pixel Repetition HOST setting 0: No Repetition 1: Repetition = 2 2: Repetition = 3 3: Repetition = 4 …… 9: Repetition = 10 10-: Setting prohibited

Note: Valid only when address 0x8550 [0] bit = 0 (automatic input judgment mode).
When address 0x8550 [0] = 1 (HOST input judgment mode), IN_REP must be set by the HOST,

Note: Valid only when address 0x8550 [0] = 0 (automatic input judgment mode).
When address 8550 [0] = 1 (HOST input judgment mode), IN_REP must be set by the HOST.

6.6.53. DC MODE REGISTER (DC_MODE) (0x8577)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	DC_NOCD_NUN				Reserved			
Type	R/W				R/W			
Default	0x0				0x0			

Register Field	Bit	Default	Description
DC_NOCD_NUN	[7:4]	0x0	Threshold value for automatic move to 24bit mode when either GC packet input or GC Packet non-input have occurred in succession alongside DC_NOCD_SEL setting condition CD Sets above condition successive occurrence V number At 0000 setting, automatic move OFF (default) Note: In the standard, setting 4 (0100) is recommended
Reserved	[3:0]	0x7	Do not change reserved value

6.6.54. Video Mute Register (VI_MUTE) (0x857F)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AutoMute1	AutoMute0	Reserved	VI_Mute	Reserved			VI_Black
Type	RW	RW	RW	RW	RO			RW
Default	1	1	0	0	0			0

Register Field	Bit	Default	Description
AutoMute1	[7]	1	Auto mute of H/V/DE when No TMDS detected 0: No Mute 1: Mute
AutoMute0	[6]	1	Auto mute of H/V/DE when No DDC5V detected 0: No Mute 1: Mute
Reserved	[5]	0	Reserved
VI_Mute	[4]	0	H/V/DE output Mute setting 0: No Mute 1: Mute (H/V/DE fixed at “0”)
Reserved	[3:1]	0	Reserved
VI_Black	[0]	0	Black Screen Output Setting 0: Normal Operation 1: Black Screen Output

6.6.55. Horizontal Active Pixel Count REGISTER0 (HAct0) (0x8582)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	HAct[7:0]							
Type	R/W							
Default	0x0							

Register Field	Bit	Default	Description
HAct[7:0]	[7:0]	0x0	Input horizontal Active size measurement result lower 8bit

6.6.56. Horizontal Active Pixel Count REGISTER1 (HAct1) (0x8583)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved			HAct[12:8]				
Type	-			R/W				
Default	-			0x0				

Register Field	Bit	Default	Description
Reserved	[7:5]	0x0	Reserved
HAct[12:8]	[4:0]	0x0	Input horizontal Active size measurement result upper 5bit

6.6.57. Vertical Active Line Count REGISTER0 (VAct0) (0x8588)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VAct[7:0]							
Type	R/W							
Default	0x0							

Register Field	Bit	Default	Description
VAct[7:0]	[7:0]	0x0	Input Vertical line size measurement result lower 8bit

6.6.58. Vertical Active Line Count REGISTER1 (VAct1) (0x8589)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved			VAct[12:8]				
Type	-			R/W				
Default	-			0x0				

Register Field	Bit	Default	Description
Reserved	[7:5]	0x0	Reserved
VAct[12:8]	[4:0]	0x0	Input Vertical line size measurement result upper 5bit

6.6.59. Horizontal Total Pixel Count REGISTER0 (HTotal0) (0x858A)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	HTotal[7:0]							
Type	R/W							
Default	0x0							

Register Field	Bit	Default	Description
HTotal[7:0]	[7:0]	0x0	Input horizontal Total size measurement result lower 8bit

6.6.60. Horizontal Total Pixel Count REGISTER1 (HTotal1) (0x858B)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved			HTotal[12:8]				
Type	-			R/W				
Default	-			0x0				

Register Field	Bit	Default	Description
Reserved	[7:5]	0x0	Reserved
HTotal[12:8]	[4:0]	0x0	Input horizontal Total size measurement result upper 5bit

6.6.61. Vertical Total Line Count REGISTER0 (VTotal0) (0x858C)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VTotal[7:0]							
Type	R/W							
Default	0x0							

Register Field	Bit	Default	Description
VTotal[7:0]	[7:0]	0x0	Input Vertical Total line count measurement result lower 8bit (measured in 2 Vsync time period)

6.6.62. Vertical Total Line Count REGISTER1 (VTotal1) (0x858D)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved		VTotal[13:8]					
Type	-		R/W					
Default	0		0x0					

Register Field	Bit	Default	Description
Reserved	[7:6]	0x0	Reserved
VTotal[13:8]	[5:0]	0x0	Input Vertical line size measurement result upper 6bit (measured in 2 Vsync time period)

6.6.63. EDID MODE REGISTER (EDID_MODE) (0x85C7)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved	EDID_SPEED			Reserved		EDID_MODE	
Type	RO	R/W			RO		R/W	
Default	0x0	0x0			0x0		0x0	

Register Field	Bit	Default	Description
Reserved	[7]	0x0	-
EDID_SPEED	[6:4]	0x0	EDID dedicated terminal I^2C speed selection 000: 100 kHz 001: 400 kHz
Reserved	[3:2]	0x0	-
EDID_MODE	[1:0]	0x0	EDID access response mode selection 00: DDC line direct connection EEPROM mode (Absolutely no response to EDID access from DDC line) 01: Internal EDID-RAM & DDC2B mode (No response to 0x60slave => Returns NACK) 1x: Internal EDID-RAM & E-DDC mode

6.6.64. EDID Slave REGISTER (EDID_SLV) (0x85C8)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	EDID_SLV							
Type	R/W							
Default	0xA0							

Register Field	Bit	Default	Description
EDID_SLV	[7:0]	0xA0	EDID EEPROM SLAVE address setting Note: Fixed at bit0 = 0

6.6.65. EDID Offset REGISTER (EDID_OFF) (0x85C9)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	EDID_OFF							
Type	R/W							
Default	0x00							

Register Field	Bit	Default	Description
EDID_OFF	[7:0]	0x00	EDID EEPROM Read start offset address setting

6.6.66. EDID Length REGISTER 1 (EDID_LEN1) (0x85CA)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	EDID_LEN[7:0]							
Type	R/W							
Default	0x00							

Register Field	Bit	Default	Description
EDID_LEN[7:0]	[7:0]	0x00	EDID data size stored in RAM Note: Sets Data byte number Read from EEPROM Note: If EDID_LEN[10:0] = 0 is set, no read Note: if EDID_LEN[10:0] > 0x400 (1024 or more) is set, 1024 bytes only are Read Note: If EEPROM not used, and data is written directly to RAM from HOST, data size is set

6.6.67. EDID Length REGISTER 2 (EDID_LEN2) (0x85CB)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved					EDID_LEN[10:8]		
Type	RO					R/W		
Default	0x00					0x0		

Register Field	Bit	Default	Description
Reserved	[7:3]	0x00	Reserved
EDID_LEN[10:8]	[2:0]	0x0	EDID data size stored in RAM (upper address bits)

6.6.68. EDID Command REGISTER (EDID_CMD) (0x85CC)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved						ED_RST_CMD	ED_CMD
Type	RO						R/W	R/W
Default	0x00						0x0	0x0

Register Field	Bit	Default	Description
Reserved	[7:2]	0x00	Reserved
ED_RST_CMD	[1]	0x0	EDID EEPROM reset operation start command 1: Command issued Note: After reset action ended, automatically clears to “0”
ED_RD_CMD	[0]	0x0	Data forwarded to EDID-RAM from EEPROM start command 1: Command issues Note: After reset action ended, automatically clears to “0”

6.7. HDMI Rx Audio Control

6.7.1. FORCE MUTE (FORCE_MUTE) (0x8600)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved			FORCE_AMUTE	Reserved			FORCE_DMUTE
Type	RO			RW	RO			RW
Default	0	0	0	1	0	0	0	1

Register Field	Bit	Default	Description
Reserved	[7:5]	0	Reserved
FORCE_AMUTE	[4]	0x1	Forced AMUTEOUT terminal control 0: Mute OFF 1: Mute ON Note: Setting and clear is possible at HOST only Note: For Mute ON polarity, follow the 0x8608[5] setting
Reserved	[3:1]	0	Reserved
FORCE_DMUTE	[0]	0x1	Forced data MUTE control 0: Mute OFF 1: Mute ON Note: Setting and clear is possible at HOST only Note: For Mute signal, follow the 0x8608[2:0] setting

6.7.2. CMD AUD (CMD_AUD) (0x8601)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved					CMD_BUFINIT	CMD_LOCKDET	CMD_MUTE
Type	RO					RW	RW	RW
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
Reserved	[7:3]	0	Reserved
CMD_BUFINIT	[2]	0	Buffer initialization start command 1: Command issued Note: After buffer initialization completed, automatically clears Note: When in automatic command issue mode (address 0x8604[2:1] ≠ 2'b00), issue of commands from HOST is prohibited. Note: When issuing commands from HOST, always issue the MUTE start command first.
CMD_LOCKDET	[1]	0	Audio clock frequency lock detection start command 1：Command issued Note：The reproduced Audio clock frequency detects unification with FS information transmitted by Cannel Status bit, and issues interrupt. For observation cycle and detection precision, follow the address 0x8630 to 33 setting.

			Note：After frequency lock detection, automatically clears Use not recommended
CMD_MUTE	[0]	0	MUTE start command 1: Command issued Note: Automatic command issue mode exists. For automatic issue condition, follow the AUTO_CMD0, 1 (address 0x8602, 0x8603) setting. Note: When AUTO_PLAY3 setting ON, automatically clears to "0" when Buffer initialization completed. Note: For Mute signal, follow the 0x8608[2:0] setting Note: For AMUTE terminal output polarity, follow the 0x8608[5] setting

6.7.3. Auto Command REGISTER 0 (AUTO_CMD0) (0x8602)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Auto_ Mute7	Auto_ Mute6	Auto_ Mute5	Auto_ Mute4	Auto_ Mute3	Auto_ Mute2	Auto_ Mute1	Auto_ Mute0
Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
Auto_Mute7	[7]	In PHY-A/B switch, automatically set CMD_MUTE 0：Not set 1：Set
Auto_Mute6	[6]	In LPCM/NLPCM change detection, automatically set CMD_MUTE 0：Not set 1：Set Note: OR conditions for LPCM → NLPCM detect and NLPCM → LPCM detect
Auto_Mute5	[5]	In FS change detection, automatically set CMD_MUTE 0：Not set 1：Set
Auto_Mute4	[4]	In PHY output clock change detection, automatically set CMD_MUTE 0：Not set 1：Set
Auto_Mute3	[3]	In Non LPCM detection period, automatically set CMD_MUTE 0：Not set 1：Set
Auto_Mute2	[2]	In Audio clock frequency unlock detect period, automatically set CMD_MUTE 0：Not set 1：Set Note: **Use not recommended**
Auto_Mute1	[1]	In PHY no output clock detect period, automatically set CMD_MUTE 0：Not set 1：Set
Auto_Mute0	[0]	In DVI mode period, or in DDC5V = 0V period, automatically set CMD_MUTE 0：Not set 1：Set

6.7.4. Auto Command REGISTER 0 (AUTO_CMD1) (0x8603)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved					Auto_ Mute10	Auto_ Mute9	Auto_ Mute8
Type	RO					RW	RW	RW
Default	0x00					0	0	0

Register Field	Bit	Description
Reserved	[7:3]	-
Auto_Mute10	[2]	In 60958 frame discontinuous detect, automatically issue CMD_MUTE 0: Not issue 1: Issue
Auto_Mute9	[1]	In SET_AVMUTE receive period, automatically issue CMD_MUTE 0: Not issue 1: Issue
Auto_Mute8	[0]	In buffer flow detect, automatically issue CMD_MUTE 0: Not issue 1: Issue

6.7.5. Auto Command REGISTER 0 (AUTO_CMD2) (0x8604)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved				Auto_ Play3	Auto_ Play2	Reserved	
Type	RO				RW	RW	RO	
Default	0x0				0	0	0x0	

Register Field	Bit	Description
Reserved	[7:4]	-
Auto_Play3	[3]	In Buffer initialization end detect, automatically clears MUTE_CMD 0: Not clear 1: Clear
Auto_Play2	[2]	After generation of MUTE factor selected in AUTO_MUTE setting “after fixed time B” automatically issue CMD_BUFINIT 0: Not issue 1: Issue Note: Priority over frequency lock detect (= equivalent to lock detect time limit) Note: If MUTE factor continues for fixed period, issue command at end edge of factor. Note: If MUTE factor is generated during fixed time measurement, restart time measurement from beginning.
Reserved	[1:0]	-

6.7.6. Buffer Initialization Start Period (BUFINIT_START) (0x8606)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	BUFINIT_START							
Type	RW							
Default	0x0A							

Register Field	Bit	Description
BUFINIT_START	[7:0]	Wait time setting until Buffer initialization start in AUTO_PLAY2 → “fixed time B” 0.1 to 25.5 sec. (set in 0.1 sec. units) Note: Setting of 0 sec. (00h) is prohibited

6.7.7. FS MUTE REGISTER (FS_MUTE) (0x8607)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	FS_else_MUTE	FS22_MUTE	FS24_MUTE	FS88_MUTE	FS96_MUTE	FS176_MUTE	FS192_MUTE	FS_NO_MUTE
Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	1	1	1	1	1	1	1	1

Register Field	Bit	Default	Description
FS_else_MUTE	[7]	0x1	Other than FS = 22 k, 24 k, 32 k, 44 k, 48 k, 88 k, 96 k, 176 k, 192 k 0: Do not Mute 1: Mute
FS22_MUTE	[6]	0x1	When at FS = 22.05 kHz, routinely 0: Do not Mute 1: Mute
FS24_MUTE	[5]	0x1	When at FS = 24 kHz, routinely 0: Do not Mute 1: Mute
FS88_MUTE	[4]	0x1	When at FS = 88.2 kHz, routinely 0: Do not Mute 1: Mute
FS96_MUTE	[3]	0x1	When at FS = 96 kHz, routinely 0: Do not Mute 1: Mute
FS176_MUTE	[2]	0x1	When at FS = 176.4 kHz, routinely 0: Do not Mute 1: Mute
FS192_MUTE	[1]	0x1	When at FS = 192 kHz, routinely 0: Do not Mute 1: Mute
FS_NO_MUTE	[0]	0x1	When at FS = not indicated, routinely 0: Do not Mute 1: Mute

Write FS Bit corresponding to set specification to ”0”.
FS = 48 kHz, 44.1 kHz, 32 kHz are outside FS_MUTE applicability.
(In the standard, 48 kHz, 44.1 kHz, 32 kHz must be reproduced.)

6.7.8. AUDIO MUTE MODE REGISTER (MUTE_MODE) (0x8608)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AMUTE_DLY		AMUTE_POL	O_AMUTE_EN	I_AMUTE_OFF	MUTE_LRCK	MUTE_BCK	MUTE_SDO
Type	RW		RW	RW	RW	RW	RW	RW
Default	2'b01		1	1	1	0	0	1

Register Field	Bit	Default	Description
AMUTE_DLY	[7:6]	2'b01	When MUTE cleared, AMUTE output delay adjustment (Note2) 00: No delay 01: 100 msec delay 10: 200 msec delay 11: 300 msec delay
AMUTE_POL	[5]	1'b1	AMUTE polarity (Note1) 0: "0" output 1: "1" output
O_AMUTE_EN	[4]	1'b1	AMUTE signal ON/OFF when MUTE ON (Note1) 0: OFF ("0" output fixed) 1: ON
I_AMUTE_OFF	[3]	1'b0	AMUTE signal ON/OFF for ASP when MUTE ON (Note1) 0: ON 1: OFF ("0" output fixed)
MUTE_LRCK	[2]	1'b0	LRCK output when MUTE ON (Note1) 0: Do not Mute 1: Mute
MUTE_BCK	[1]	1'b0	BCK output when MUTE ON (Note1) 0: Do not Mute 1: Mute
MUTE_SDO	[0]	1'b1	SDO/DADO output when MUTE ON (Note1) 0: Do not Mute 1: Mute

Note1: Actually setting to MUTE ON occurs when any of the following (1) to (4) occur.
(1) When HOST sets FORCE_MUTE (address 0x8600)
(2) When HOST sets CMD_MUTE (address 0x8601[0])
(3) When factor selected in AUTO_MUTE (address 0x8602 to 0x8603) is generated
(4) When other than FS received in FS_MUTE (address 0x8607) is selected

Note2: If using AMUTEOUT to perform transistor mute at set output stage, this setting can also be used to delay the Mute clear timing.

6.7.9. AUDIO SAMPLE FREQUENCY INPUT MODE (FS_IMODE) (0x8620)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved	NLPCM_ HMODE	NLPCM_ SMODE	NLPCM_ IMODE	FS_ HMODE	FS_ AMODE	FS_ SMODE	FS_ IMODE
Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
Reserved	[7]	-
NLPCM_HMODE	[6]	LPCM/NLPCM identification information HOST setting mode 0: OFF (= automatic setting) 1: At HOST only, set identification information to 0x8621[4]
NLPCM_SMODE	[5]	LPCM/NLPCM identification information extraction mode setting 0: Information extracted from C_bit only 1: Information extracted at AUD_Info priority
NLPCM_IMODE	[4]	Action setting during CBIT- NLPCM bit error 0: When sub packet error includes the bit, update not performed 1: When sub packet error includes the bit, update performed
FS_HMODE	[3]	FS (sampling frequency) HOST setting mode 0: OFF (= automatic setting) 1: At HOST only, set FS information to 0x8621[3:0]
FS_AMODE	[2]	Sampling frequency due to ACR (N/CTS value) automatic calculation mode setting 0: OFF 1: Calculation result at highest priority Note: This mode can be used only when RefClk = 42 MHz
FS_SMODE	[1]	FS (sampling frequency) identification information extraction mode setting 0: Information extracted from C_bit only 1: Information extracted at AUD_Info priority
FS_IMODE	[0]	Action setting during CBIT-FS bit error 0: When sub packet error includes the bit, update not performed 1: When sub packet error includes the bit, update performed

6.7.10. AUDIO SAMPLE FREQUENCY MODE REGISTER (FS_SET) (0x8621)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	DST Double	Reserved		NLPCM	FS			
Type	RW	RW		RW	RW			
Default	0	0		0	0x2			

Register Field	Bit	Description
DST Double	[7]	DST double rate flag monitor (When other than DST selected, fixed at 0) 0: normal rate 1: double rate
Reserved	[6:5]	-
NLPCM	[4]	Normal Audio linear PCM/nonlinear PCM identification information extraction result 0: LPCM 1: Compression stream Note: When 0x8620[6] == 0, Follow the 0x8620[5:4] setting, and HW automatically set, write from Host is invalid. If 0x8620[6] == 1, HOST determines and sets. Note: LPCM/NLPCM change interrupt (address 0x8505[3:2]) is generated when this register has a change.
FS	[3:0]	AUDIO sampling frequency information extraction result 4'h0: 44.1kHz, 4'h2: 48kHz, 4'h3: 32kHz, 4'h4: 22.05kHz, 4'h6: 24kHz, 4'h8: 88.2kHz, 4'hA: 96kHz, 4'hC: 176.4kHz, 4'hE: 192kHz, **4'h9: 768kHz** **4'h5: 384kHz, 4'h7: 352.8kHz, 4'hB: 705.6kHz** Note: If 0x08620[3] == 0, Follow 0x8620[2:0] setting, HW is automatically set, write from Host is invalid. If 0x8620[3] == 1, Host determines and sets. Note: FS change interrupt (address 0x08505[1]) is generated when this register has a change.

6.7.11. CBIT Byte 0 (CBIT_BYTE0) (0x8622)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	CBIT_BYTE0							
Type	RW							
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
CBIT_BYTE0	[7:0]	Channel Status bit [7:0]

6.7.12. CBIT Byte 1 (CBIT_BYTE1) (0x8623)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	CBIT_BYTE1							
Type	RW							
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
CBIT_BYTE1	[7:0]	Channel Status bit [15:8]

6.7.13. CBIT Byte 2 (CBIT_BYTE2) (0x8624)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	CBIT_BYTE2							
Type	RW							
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
CBIT_BYTE2	[7:0]	Channel Status bit [23:16]

6.7.14. CBIT Byte 3 (CBIT_BYTE3) (0x8625)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	CBIT_BYTE3							
Type	RW							
Default	0	0	0	0	0	0	1	0

Register Field	Bit	Description
CBIT_BYTE3	[7:0]	Channel Status bit [31:24]

6.7.15. CBIT Byte 4 (CBIT_BYTE4) (0x8626)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	CBIT_BYTE4							
Type	RW							
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
CBIT_BYTE4	[7:0]	Channel Status bit [39:32]

6.7.16. CBIT Byte 5 (CBIT_BYTE5) (0x8627)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	CBIT_BYTE5							
Type	RW							
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Description
CBIT_BYTE5	[7:0]	Channel Status bit [47:40]

6.7.17. Audio FS Lock Detect Control REGISTER 0 (LKDet_REF0) (0x8630)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	LOCK_REF[7:0]							
Type	RW							
Default	0xA0							

Register Field	Bit	Description
LOCK_REF[7:0]	[7:0]	RefClk cycle number setting during 10 msec 20 bit Initial value 420000 = 668A0h (for 42 MHz) 270000 = 41EB0h (for 27 MHz) 260000 = 3F7A0h (for 26 MHz)

6.7.18. Audio FS Lock Detect Control REGISTER 1 (LKDet_REF1) (0x8631)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	LOCK_REF[15:8]							
Type	RW							
Default	0x68							

Register Field	Bit	Description
LOCK_REF[15:8]	[7:0]	RefClk cycle number setting during 10 msec 20 bit Initial value 420000 = 668A0h (for 42 MHz) 270000 = 41EB0h (for 27 MHz) 260000 = 3F7A0h (for 26 MHz)

6.7.19. Audio FS Lock Detect Control REGISTER 0 (LKDet_REF2) (0x8632)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved				LOCK_REF[19:16]			
Type	RO				RW			
Default	0x0				0x6			

Register Field	Bit	Description
Reserved	[7:4]	-
LOCK_REF[19:16]	[3:0]	RefClk cycle number setting during 10 msec 20 bit Initial value = 420000 = 668A0h (for 42 MHz) = 270000 = 41EB0h (for 27 MHz) = 260000 = 3F7A0h (for 26 MHz)

6.7.20. CTS Adjustment Mode REGISTER 1 (ACR_MODE) (0x8640)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved			ACR_LOAD	Reserved	N_MODE	CTS_MODE	
Type	RO			RW	RO	RW	RW	
Default	0x0			0	0	0	2'b0	

Register Field	Bit	Description
Reserved	[7:5]	–
ACR_LOAD	[4]	N/CTS value forced load command 0: Normal action 1: Command issued Note: Automatic clear
Reserved	[3]	Reserved
N_MODE	[2]	Audio PLL N value update action setting 0: Uses receive N value (normal action) 1: Uses HOST setting N value (for test)
CTS_MODE	[1:0]	Audio PLL CTS value update action setting 00: Uses receive CTS value (normal action) 01: Uses HW correction CTS value (HW automatic flow control) Note: In HW automatic flow control mode, the received CTS is corrected and PLL applied, in response to Audio Buffer balance state. When this function is used, even if illegitimate (violation of standard) CTS is received, undestroyed Audio replay is possible. The CTS correction amount is set at address 0x8641 to 0x8642.

6.7.21. CTS Adjustment REGISTER 0 (ACR_MDF0) (0x8641)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved	ACR_L2MDF			Reserved	ACR_L1MDF		
Type	RO	RW			RO	RW		
Default	0	3'b010			0	3'b001		

Register Field	Bit	Description
Reserved	[7]	-
ACR_L2MDF	[6:4]	CTS correction amount setting with Buffer linear Over/Under (Threshold 2) detection 000: ±0ppm (±0) 001: ±61ppm (±1/16384*CTS) 010: ±122ppm (±1/8192*CTS) 011: ±244ppm (±1/4096*CTS) 100: ±488ppm (±1/2048*CTS) 101: ±976ppm (±1/1024*CTS) 110: ±1976ppm (±1/512*CTS) 111: ±3906ppm (±1/256*CTS)
Reserved	[3]	Reserved
ACR_L1MDF	[2:0]	CTS correction amount setting with Buffer linear Over/Under (Threshold 1) detection 000: ±0ppm (±0) 001: ±61ppm (±1/16384*CTS) 010: ±122ppm (±1/8192*CTS) 011: ±244ppm (±1/4096*CTS) 100: ±488ppm (±1/2048*CTS) 101: ±976ppm (±1/1024*CTS) 110: ±1976ppm (±1/512*CTS) 111: ±3906ppm (±1/256*CTS)

6.7.22. CTS Adjustment REGISTER 0 (ACR_MDF1) (0x8642)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved					ACR_L3MDF		
Type	RO					RW		
Default	0x00					3'b011		

Register Field	Bit	Description
Reserved	[7:3]	Reserved
ACR_L3MDF	[2:0]	CTS correction amount setting with Buffer Over/Under detection Note: If Over/Under flow prevention control OFF, set to ±0ppm 000: ±0ppm (±0) 001: ±61ppm (±1/16384*CTS) 010: ±122ppm (±1/8192*CTS) 011: ±244ppm (±1/4096*CTS) 100: ±488ppm (±1/2048*CTS) 101: ±976ppm (±1/1024*CTS) 110: ±1976ppm (±1/512*CTS) 111: ±3906ppm (±1/256*CTS)

6.7.23. AUDIO OUTPUT MODE 0 Register (SDO_MODE0) (0x8651)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved					BCK_POL	BCK_FS	LR_POL
Type	RW							
Default	0	0	0	0	0	0	1	0

Register Field	Bit	Default	Description
Reserved	[7:3]	0	Reserved
BCK_POL	[2]	0	BCK polarity selection 0: Normal (ASDO data changed at down edge) 1: Inverted (ASDO data changed at up edge)
BCK_FS	[1]	1	BCK frequency selection 0: 32fs 1: 64fs
LR_POL	[0]	0	LRCK polarity selection 0: Normal (sample period: 1st half = L, 2nd half = H) 1: Inverted (sample period: 1st half = H, 2nd half = L)

6.7.24. AUDIO OUTPUT MODE 1 Register (SDO_MODE1) (0x8652)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved	SDO_BIT_LENG			Reserved		SDO_FMT	
Type	RO	R/W			RO		R/W	
Default	0	3'b110			2'b00		2'b00	

Register Field	Bit	Default	Description
Reserved	[7]	0	-
SDO_BIT_LENG	[6:4]	3'b110	ASDO output data Bit Length setting 000: 16bit (lower 8bit discarded) 001: 16bit (lower 8bit + 1 discarded) 010: 18bit (lower 6bit discarded) 011: 18bit (lower 6bit + 1 discarded) 100: 20bit (lower 4bit discarded) 101: 20bit (lower 4bit + 1 discarded) 110: 24bit no rounding 111: Output OFF (Mute)
Reserved	[3:2]	2'b00	–
SDO_FMT	[1:0]	2'b00	ASDO output format setting 00: Right justified 01: Left justified 1x: I2S

6.7.25. AUDIO PLL Setting Register (NCO_F0_MOD) (0x8670)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved						NCO_F0_MOD	
Type	RO						R/W	
Default	0x0						2'b00	

Register Field	Bit	Default	Description
Reserved	[7:2]	0x0	–
NCO_F0_MOD	[1:0]	0x0	NCO standard frequency setting for Audio PLL 00: For REFCLK = 42 MHz 01: For REFCLK = 27 MHz 1x: Register setting value uses 28 bit setting for 48 kHz series use, for 44.1 kHz series use. (address 0x8671 to 78) Note: 1. NCO standard frequency setting value calculation 48 kHz series: 6.144 MHz × 2^28 ÷ (RefClk frequency) 44.1 kHz series: 5.6448 MHz × 2^28 ÷ (RefClk clock frequency) 2. For 26MHz RefClk: • Set this field to 2'b10 f • 0x8671-74: NCO_48F0[27:0] = 0x3_C7_EA_93 • 0x8675-78: NCO_44F0[27:0] = 0x3_79_45_EA

6.7.26. AUDIO PLL Setting Register (NCO_48F0A) (0x8671)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	NCO_48F0[7:0]							
Type	RW							
Default	0x00							

Note: 6.144 MHz × 2^28 ÷ (System clock frequency)

6.7.27. AUDIO PLL Setting Register (NCO_48F0B) (0x8672)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	NCO_48F0[15:8]							
Type	RW							
Default	0x00							

6.7.28. AUDIO PLL Setting Register (NCO_48F0C) (0x8673)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	NCO_48F0[23:16]							
Type	RW							
Default	0x00							

6.7.29. AUDIO PLL Setting Register (NCO_48F0D) (0x8674)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved				NCO_48F0[27:24]			
Type	RO				RW			
Default	0x0				0x0			

Note: 6.144 MHz × 2^28 ÷ (System clock frequency)

6.7.30. AUDIO PLL Setting Register (NCO_44F0A) (0x8675)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	NCO_48F0[7:0]							
Type	RW							
Default	0x00							

Note: 5.6448 MHz × 2^28 ÷ (System clock frequency)

6.7.31. AUDIO PLL Setting Register (NCO_44F0B) (0x8676)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	NCO_48F0[15:8]							
Type	RW							
Default	0x00							

6.7.32. AUDIO PLL Setting Register (NCO_44F0C) (0x8677)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	NCO_48F0[23:16]							
Type	RW							
Default	0x00							

6.7.33. AUDIO PLL Setting Register (NCO_44F0D) (0x8678)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved				NCO_44F0[27:24]			
Type	RO				RW			
Default	0x0				0x0			

Note: 5.6448 MHz × 2^28 ÷ (System clock frequency)

6.7.34. AUDIO OUTPUT MODULE TERMINAL CONTROL (APIN_EN0) (0x8690)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AMTSEL		ALRSEL		ABCKSEL		AMCKSEL	
Type	RW		RW		RW		RW	
Default	1	1	1	1	1	1	1	1

Register Field	Bit	Default	Description
AMTSEL	[7:6]	0x3	AMUTE (module) terminal control 00: Normal 01: Low fixed 10: High fixed 11: Normal
ALRSEL	[5:4]	0x3	LRCK (module) terminal control 00: Normal 01: Low fixed 10: High fixed 11: Normal
ABCKSEL	[3:2]	0x3	BMCK (module) terminal control 00: Normal 01: Low fixed 10: High fixed 11: Normal
AMCKSEL	[1:0]	0x3	AMCK (module) terminal control 00: Normal 01: Low fixed 10: High fixed 11: Normal

6.8. HDMI Rx InfoFrame Data

6.8.1. VS INFO PACKET TYPE CODE SETTING (TYP_VS_SET) (0x8701)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	TYP_VS_SET							
Type	RW							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
TYP_VS_SET	[7:0]	X	VS_info Packet Type code setting

6.8.2. AVI INFO PACKET TYPE CODE SETTING (TYP_AVI_SET) (0x8702)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	TYP_AVI_SET							
Type	RW							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
TYP_AVI_SET	[7:0]	X	AVI_info Packet Type code setting

6.8.3. SPD INFO PACKET TYPE CODE SETTING (TYP_SPD_SET) (0x8703)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	TYP_SPD_SET							
Type	RW							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
TYP_SPD_SET	[7:0]	X	SPD_info Packet Type code setting

6.8.4. AUD INFO PACKET TYPE CODE SETTING (TYP_AUD_SET) (0x8704)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	TYP_AUD_SET							
Type	RW							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
TYP_AUD_SET	[7:0]	X	AUD_info Packet Type code setting

6.8.5. MS INFO PACKET TYPE CODE SETTING (TYP_MS_SET) (0x8705)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	TYP_MS_SET							
Type	RW							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
TYP_MS_SET	[7:0]	X	MS_info Packet Type code setting

6.8.6. ACP INFO PACKET TYPE CODE SETTING (TYP_ACP_SET) (0x8706)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	TYP_ACP_SET							
Type	RW							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
TYP_ACP_SET	[7:0]	X	ACP Packet Type code setting

6.8.7. ISRC1 INFO PACKET TYPE CODE SET. (TYP_ISRC1_SET) (0x8707)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	TYP_ISRC1_SET							
Type	RW							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
TYP_ISRC1_SET	[7:0]	X	ISRC1 Packet Type code setting

6.8.8. ISRC2 INFO PACKET TYPE CODE SETTING (TYP_ISRC2_SET) (0X8708)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	TYP_ISRC2_SET							
Type	RW							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
TYP_ISRC2_SET	[7:0]	X	ISRC2 Packet Type code setting

6.8.9. PACKET INTERRUPT MODE (PK_INT_MODE) (0x8709)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_INT_MODE	ISRC_INT_MODE	ACP_INT_MODE	VS_INT_MODE	SPD_INT_MODE	MS_INT_MODE	AUD_INT_MODE	AVI_INT_MODE
Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
ISRC2_INT_MODE	[7]	0	Action setting during ISRC2_info packet receive data error 0 : Error packet does not notify (update) HOST 1 : Error packet also notifies (updates) HOST
ISRC_INT_MODE	[6]	0	Action setting during ISRC 1 packet receive data error 0 : Error packet does not notify (update) HOST 1 : Error packet also notifies (updates) HOST
ACP_INT_MODE	[5]	0	Action setting during ACP packet receive data error 0 : Error packet does not notify (update) HOST 1 : Error packet also notifies (updates) HOST
VS_INT_MODE	[4]	0	Action setting during VS_info packet receive data error 0 : Error packet does not notify (update) HOST 1 : Error packet also notifies (updates) HOST
SPD_INT_MODE	[3]	0	Action setting during SPD_info packet receive data error 0 : Error packet does not notify (update) HOST 1 : Error packet also notifies (updates) HOST
MS_INT_MODE	[2]	0	Action setting during MS_info packet receive data error 0 : Error packet does not notify (update) HOST 1 : Error packet also notifies (updates) HOST
AUD_INT_MODE	[1]	0	Action setting during AUD_info packet receive data error 0 : Error packet does not notify (update) HOST 1 : Error packet also notifies (updates) HOST
AVI_INT_MODE	[0]	0	Action setting during AVI_info packet receive data error 0 : Error packet does not notify (update) HOST 1 : Error packet also notifies (updates) HOST

6.8.10. PACKET AUTO CLEAR (PK_AUTO_CLR) (0x870a)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	PK_AUTO_CLR7	PK_AUTO_CLR6	PK_AUTO_CLR5	PK_AUTO_CLR4	PK_AUTO_CLR3	PK_AUTO_CLR2	PK_AUTO_CLR1	PK_AUTO_CLR0
Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
PK_AUTO_CLR7	[7]	0	When DVI received, ISRC2_info packet data cleared 1: Clear 0: Do not clear
PK_AUTO_CLR6	[6]	0	When DVI received, ISRC packet data cleared 1: Clear 0: Do not clear
PK_AUTO_CLR5	[5]	0	When DVI received, ACP packet data cleared 1: Clear 0: Do not clear
PK_AUTO_CLR4	[4]	0	When DVI received, VS_info packet data cleared 1: Clear 0: Do not clear
PK_AUTO_CLR3	[3]	0	When DVI received, SPD_info packet data cleared 1: Clear 0: Do not clear
PK_AUTO_CLR2	[2]	0	When DVI received, MS_info packet data cleared 1: Clear 0: Do not clear
PK_AUTO_CLR1	[1]	0	When DVI received, AUD_info packet data cleared 1: Clear 0: Do not clear
PK_AUTO_CLR0	[0]	0	When DVI received, AVI_info packet data cleared 1: Clear 0: Do not clear

6.8.11. NO PACKET LIMIT (NO_PK_LIMIT) (0x870b)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	NO_ACP_LIMIT				NO_AVI_LIMIT			
Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
NO_ACP_LIMIT	[7:4]	0	After receiving ACP packet, when ACP packet not received during setting value*80msec period, ACP receive interrupt occurs. Note: At 4'b0000 setting, interrupt does not occur. Note: At 4'b0000 setting, ACP packet receive status action does not occur. Note: When DVI received, interrupt does not occur.

NO_AVI_LIMIT	[3:0]	0	When AVI packet not received during setting value*80msec period, AVI receive interrupt occurs. Note: At 4'b0000 setting, interrupt does not occur. Note: When DVI received, interrupt does not occur.

6.8.12. NO PACKET CLEAR (NO_PK _CLR) (0x870c)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved	NO_VS_CLR	NO_SPD_CLR	NO_ACP_CLR	Reserved		NO_AVI_CLR1	NO_AVI_CLR0
Type	RW	RW	RW	RW	RO		RW	RW
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
Reserved	[7]	0	Reserved
NO_VS_CLR	[6]	0	When VS receive interrupt is detected, VS storage register automatic clear setting 0: During receive interrupt, no automatic clear 1: During receive interrupt, automatic clear
NO_SPD_CLR	[5]	0	When SPD receive interrupt is detected, SPD storage register automatic clear setting 0: During receive interrupt, no automatic clear 1: During receive interrupt, automatic clear
NO_ACP_CLR	[4]	0	When ACP receive interrupt is detected, ACP storage register automatic clear 1: Clear 0: Do not clear
Reserved	[3:2]	0	Reserved
NO_AVI_CLR1	[1]	0	When AVI receive interrupt occurs, judge input video signal with RGB and no Repetition 1: Judge 0: No judge (preserve in status before interruption)
NO_AVI_CLR0	[0]	0	When AVI receive interrupt is detected, AVI storage register automatic clear 1: Clear 0: Do not clear

6.8.13. ERROR PACKET LIMIT (ERR_PK_LIMIT) (0x870d)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ERR_PK_MOD	ERR_PK_LIMIT						
Type	RW	RW						
Default	1	1	1	1	1	1	1	1

Register Field	Bit	Default	Description
ERR_PK_MOD	[7]	0x1	Packet continuing receive error detection start conditions 0: If error is included in either header/data 1: If correctable error was included in header
ERR_PK_LIMIT	[6:0]	0x7f	Packet continuing receive error occurrence detection threshold If error packet is continually received up to set Packet number value, Set Packet receive error status to “1”. If absolutely no error Packet is received, return Packet receive error status for both header/data to “0”. In 0 setting, detection OFF

6.8.14. NO PACKET LIMIT (NO_PK_LIMIT2) (0x870e)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	NO_VS_LIMIT				NO_SPD_LIMIT			
Type	RW				RW			
Default	0	0	0	0	0	0	0	0

Register Field	Bit	Default	Description
NO_VS_LIMIT	[7:4]	0	If no VS packet is received during setting value * 80 msec period judge receive interrupt has occurred. At 0000 setting, receive interrupt detect is OFF.
NO_SPD_LIMIT	[3:0]	0	If no SPD packet is received during setting value * 80 msec period judge receive interrupt has occurred. At 0000 setting, receive interrupt detect is OFF.

6.8.15. VS IEEE SELECT (VS_IEEE_SEL) (0x870f)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							VS_IEEE_SEL
Type	RO							RW
Default	0	0	0	0	0	0	0	1

Register Field	Bit	Default	Description
Reserved	[7:1]	0	Reserved
VS_IEEE_SEL	[0]	0x1	Extraction operation selection for VS Info packet stored at HDMI_VSInfo receive register (address 0x8770 to 8e). 1: Store only when IEEE Registration Identifier is 0x000C03 VS_Infopacket only. 0: Freely store VS_Info packet regardless of IEEE Registration Identifier. Note: This register setting is valid only at address 0x8701[7:0] = 81h. When address 0x8701[7:0] ≠ 81h, this register setting is ignored, and the specified Type Packet is stored at address 0x8770 to 8e each time it is received.

6.8.16. AVI INFO PACKET HEADER BYTE 0 (PK_AVI_0HEAD) (0x8710)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AVI_0HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AVI_0HEAD	[7:0]	X	861B AVI_info packet Header byte 0 (= type)

6.8.17. AVI INFO PACKET HEADER BYTE 1 (PK_AVI_1HEAD) (0x8711)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AVI_1HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AVI_1HEAD	[7:0]	X	861B AVI_info packet Header byte 1 (= version)

6.8.18. AVI INFO PACKET HEADER BYTE 2 (PK_AVI_2HEAD) (0x8712)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AVI_2HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AVI_2HEAD	[7:0]	X	861B AVI_info packet Header byte 2 (= data length)

6.8.19. AVI INFO PACKET DATA BYTE 0 (PK_AVI_0BYTE) (0x8713)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AVI_0BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AVI_0BYTE	[7:0]	X	861B AVI_info packet Data byte 0 (= checksum)

6.8.20. AVI INFO PACKET DATA BYTE 1 (PK_AVI_1BYTE) (0x8714)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AVI_1BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AVI_1BYTE	[7:0]	X	861B AVI_info packet Data byte 1

6.8.21. AVI INFO PACKET DATA BYTE 2 (PK_AVI_2BYTE) (0x8715)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AVI_2BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AVI_2BYTE	[7:0]	X	861B AVI_info packet Data byte 2

6.8.22. AVI INFO PACKET DATA BYTE 3 (PK_AVI_3BYTE) (0x8716)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AVI_3BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AVI_3BYTE	[7:0]	X	861B AVI_info packet Data byte 3

6.8.23. AVI INFO PACKET DATA BYTE 4 (PK_AVI_4BYTE) (0x8717)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AVI_4BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AVI_4BYTE	[7:0]	X	861B AVI_info packet Data byte 4

6.8.24. AVI INFO PACKET DATA BYTE 5 (PK_AVI_5BYTE) (0x8718)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AVI_5BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AVI_5BYTE	[7:0]	X	861B AVI_info packet Data byte 5

6.8.25. AVI INFO PACKET DATA BYTE 6 (PK_AVI_6BYTE) (0x8719)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AVI_6BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AVI_6BYTE	[7:0]	X	861B AVI_info packet Data byte 6

6.8.26. AVI INFO PACKET DATA BYTE 7 (PK_AVI_7BYTE) (0x871a)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AVI_7BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AVI_7BYTE	[7:0]	X	861B AVI_info packet Data byte 7

6.8.27. AVI INFO PACKET DATA BYTE 8 (PK_AVI_8BYTE) (0x871b)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AVI_8BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AVI_8BYTE	[7:0]	X	861B AVI_info packet Data byte 8

6.8.28. AVI INFO PACKET DATA BYTE 9 (PK_AVI_9BYTE) (0x871c)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AVI_9BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AVI_9BYTE	[7:0]	X	861B AVI_info packet Data byte 9

6.8.29. AVI INFO PACKET DATA BYTE 10 (PK_AVI_10BYTE) (0x871d)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AVI_10BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AVI_10BYTE	[7:0]	X	861B AVI_info packet Data byte 10

6.8.30. AVI INFO PACKET DATA BYTE 11 (PK_AVI_11BYTE) (0x871e)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AVI_11BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AVI_11BYTE	[7:0]	X	861B AVI_info packet Data byte 11

6.8.31. AVI INFO PACKET DATA BYTE 12 (PK_AVI_12BYTE) (0x871f)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AVI_12BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AVI_12BYTE	[7:0]	X	861B AVI_info packet Data byte 12

6.8.32. AVI INFO PACKET DATA BYTE 13 (PK_AVI_13BYTE) (0x8720)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AVI_13BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AVI_13BYTE	[7:0]	X	861B AVI_info packet Data byte 13

6.8.33. AVI INFO PACKET DATA BYTE 14 (PK_AVI_14BYTE) (0x8721)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AVI_14BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AVI_14BYTE	[7:0]	X	861B AVI_info packet Data byte 14 (Reserved for standards extension)

6.8.34. AVI INFO PACKET DATA BYTE 15 (PK_AVI_15BYTE) (0x8722)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AVI_15BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AVI_15BYTE	[7:0]	X	861B AVI_info packet Data byte 15 (Reserved for standards extension)

6.8.35. AVI INFO PACKET DATA BYTE 16 (PK_AVI_16BYTE) (0x8723)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AVI_16BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AVI_16BYTE	[7:0]	X	861B AVI_info packet Data byte 16 (Reserved for standards extension)

6.8.36. AUD INFO PACKET HEADER BYTE 0 (PK_AUD_0HEAD) (0x8730)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AUD_0HEAD							
Type	RW							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AUD_0HEAD	[7:0]	X	861B AUD_info packet Header byte 0 (= type)

6.8.37. AUD INFO PACKET HEADER BYTE 1 (PK_AUD_1HEAD) (0x8731)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AUD_1HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AUD_1HEAD	[7:0]	X	861B AUD_info packet Header byte 1 (= version)

6.8.38. AUD INFO PACKET HEADER BYTE 2 (PK_AUD_2HEAD) (0x8732)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AUD_2HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AUD_2HEAD	[7:0]	X	861B AUD_info packet Header byte 2 (= data length)

6.8.39. AUD INFO PACKET DATA BYTE 0 (PK_AUD_0BYTE) (0x8733)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AUD_0BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AUD_0BYTE	[7:0]	X	861B AUD_info packet Data byte 0 (= checksum)

6.8.40. AUD INFO PACKET DATA BYTE 1 (PK_AUD_1BYTE) (0x8734)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AUD_1BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AUD_1BYTE	[7:0]	X	861B AUD_info packet Data byte 1

6.8.41. AUD INFO PACKET DATA BYTE 2 (PK_AUD_2BYTE) (0x8735)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AUD_2BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AUD_2BYTE	[7:0]	X	861B AUD_info packet Data byte 2

6.8.42. AUD INFO PACKET DATA BYTE 3 (PK_AUD_3BYTE) (0x8736)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AUD_3BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AUD_3BYTE	[7:0]	X	861B AUD_info packet Data byte 3

6.8.43. AUD INFO PACKET DATA BYTE 4 (PK_AUD_4BYTE) (0x8737)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AUD_4BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AUD_4BYTE	[7:0]	X	861B AUD_info packet Data byte 4

6.8.44. AUD INFO PACKET DATA BYTE 5 (PK_AUD_5BYTE) (0x8738)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AUD_5BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AUD_5BYTE	[7:0]	X	861B AUD_info packet Data byte 5

6.8.45. AUD INFO PACKET DATA BYTE 6 (PK_AUD_6BYTE) (0x8739)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AUD_6BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AUD_6BYTE	[7:0]	X	861B AUD_info packet Data byte 6 (Reserved for standards extension)

6.8.46. AUD INFO PACKET DATA BYTE 7 (PK_AUD_7BYTE) (0x873a)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AUD_7BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AUD_7BYTE	[7:0]	X	861B AUD_info packet Data byte 7 (Reserved for standards extension)

6.8.47. AUD INFO PACKET DATA BYTE 8 (PK_AUD_8BYTE) (0x873b)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AUD_8BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AUD_8BYTE	[7:0]	X	861B AUD_info packet Data byte 8 (Reserved for standards extension)

6.8.48. AUD INFO PACKET DATA BYTE 9 (PK_AUD_9BYTE) (0x873c)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AUD_9BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AUD_9BYTE	[7:0]	X	861B AUD_info packet Data byte 9 (Reserved for standards extension)

6.8.49. AUD INFO PACKET DATA BYTE 10 (PK_AUD_10BYTE) (0x873d)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	AUD_10BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
AUD_10BYTE	[7:0]	X	861B AUD_info packet Data byte 10 (Reserved for standards extension)

6.8.50. MS INFO PACKET HEADER BYTE 0 (PK_MS_0HEAD) (0x8740)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	MS_0HEAD							
Type	RW							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
MS_0HEAD	[7:0]	X	861B MS_info packet Header byte 0 (= type)

6.8.51. MS INFO PACKET HEADER BYTE 1 (PK_MS_1HEAD) (0x8741)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	MS_1HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
MS_1HEAD	[7:0]	X	861B MS_info packet Header byte 1 (= version)

6.8.52. MS INFO PACKET HEADER BYTE 2 (PK_MS_2HEAD) (0x8742)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	MS_2HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
MS_2HEAD	[7:0]	X	861B MS_info packet Header byte 2 (= data length)

6.8.53. MS INFO PACKET DATA BYTE 0 (PK_MS_0BYTE) (0x8743)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	MS_0BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
MS_0BYTE	[7:0]	X	861B MS_info packet Data byte 0 (= checksum)

6.8.54. MS INFO PACKET DATA BYTE 1 (PK_MS_1BYTE) (0x8744)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	MS_1BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
MS_1BYTE	[7:0]	X	861B MS_info packet Data byte 1

6.8.55. MS INFO PACKET DATA BYTE 2 (PK_MS_2BYTE) (0x8745)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	MS_2BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
MS_2BYTE	[7:0]	X	861B MS_info packet Data byte 2

6.8.56. MS INFO PACKET DATA BYTE 3 (PK_MS_3BYTE) (0x8746)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	MS_3BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
MS_3BYTE	[7:0]	X	861B MS_info packet Data byte 3

6.8.57. MS INFO PACKET DATA BYTE 4 (PK_MS_4BYTE) (0x8747)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	MS_4BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
MS_4BYTE	[7:0]	X	861B MS_info packet Data byte 4

6.8.58. MS INFO PACKET DATA BYTE 5 (PK_MS_5BYTE) (0x8748)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	MS_5BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
MS_5BYTE	[7:0]	X	861B MS_info packet Data byte 5

6.8.59. MS INFO PACKET DATA BYTE 6 (PK_MS_6BYTE) (0x8749)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	MS_6BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
MS_6BYTE	[7:0]	X	861B MS_info packet Data byte 6 (Reserved for standards extension)

6.8.60. MS INFO PACKET DATA BYTE 7 (PK_MS_7BYTE) (0x874a)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	MS_7BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
MS_7BYTE	[7:0]	X	861B MS_info packet Data byte 7 (Reserved for standards extension)

6.8.61. MS INFO PACKET DATA BYTE 8 (PK_MS_8BYTE) (0x874b)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	MS_8BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
MS_8BYTE	[7:0]	X	861B MS_info packet Data byte 8 (Reserved for standards extension)

6.8.62. MS INFO PACKET DATA BYTE 9 (PK_MS_9BYTE) (0x874c)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	MS_9BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
MS_9BYTE	[7:0]	X	861B MS_info packet Data byte 9 (Reserved for standards extension)

6.8.63. MS INFO PACKET DATA BYTE 10 (PK_MS_10BYTE) (0x874d)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	MS_10BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
MS_10BYTE	[7:0]	X	861B MS_info packet Data byte 10 (Reserved for standards extension)

6.8.64. SPD INFO PACKET HEADER BYTE 0 (PK_SPD_0HEAD) (0x8750)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_0HEAD							
Type	RW							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_0HEAD	[7:0]	X	861B SPD_info packet Header byte 0 (= type)

6.8.65. SPD INFO PACKET HEADER BYTE 1 (PK_SPD_1HEAD) (0x8751)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_1HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_1HEAD	[7:0]	X	861B SPD_info packet Header byte 1 (= version)

6.8.66. SPD INFO PACKET HEADER BYTE 2 (PK_SPD_2HEAD) (0x8752)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_2HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_2HEAD	[7:0]	X	861B SPD_info packet Header byte 2 (= data length)

6.8.67. SPD INFO PACKET DATA BYTE 0 (PK_SPD_0BYTE) (0x8753)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_0BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_0BYTE	[7:0]	X	861B SPD_info packet Data byte 0 (= checksum)

6.8.68. SPD INFO PACKET DATA BYTE 1 (PK_SPD_1BYTE) (0x8754)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_1BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_1BYTE	[7:0]	X	861B SPD_info packet Data byte 1

6.8.69. SPD INFO PACKET DATA BYTE 2 (PK_SPD_2BYTE) (0x8755)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_2BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_2BYTE	[7:0]	X	861B SPD_info packet Data byte 2

6.8.70. SPD INFO PACKET DATA BYTE 3 (PK_SPD_3BYTE) (0x8756)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_3BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_3BYTE	[7:0]	X	861B SPD_info packet Data byte 3

6.8.71. SPD INFO PACKET DATA BYTE 4 (PK_SPD_4BYTE) (0x8757)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_4BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_4BYTE	[7:0]	X	861B SPD_info packet Data byte 4

6.8.72. SPD INFO PACKET DATA BYTE 5 (PK_SPD_5BYTE) (0x8758)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_5BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_5BYTE	[7:0]	X	861B SPD_info packet Data byte 5

6.8.73. SPD INFO PACKET DATA BYTE 6 (PK_SPD_6BYTE) (0x8759)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_6BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_6BYTE	[7:0]	X	861B SPD_info packet Data byte 6

6.8.74. SPD INFO PACKET DATA BYTE 7 (PK_SPD_7BYTE) (0x875a)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_7BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_7BYTE	[7:0]	X	861B SPD_info packet Data byte 7

6.8.75. SPD INFO PACKET DATA BYTE 8 (PK_SPD_8BYTE) (0x875b)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_8BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_8BYTE	[7:0]	X	861B SPD_info packet Data byte 8

6.8.76. SPD INFO PACKET DATA BYTE 9 (PK_SPD_9BYTE) (0x875c)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_9BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_9BYTE	[7:0]	X	861B SPD_info packet Data byte 9

6.8.77. SPD INFO PACKET DATA BYTE 10 (PK_SPD_10BYTE) (0x875d)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_10BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_10BYTE	[7:0]	X	861B SPD_info packet Data byte 10

6.8.78. SPD INFO PACKET DATA BYTE 11 (PK_SPD_11BYTE) (0x875e)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_11BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_11BYTE	[7:0]	X	861B SPD_info packet Data byte 11

6.8.79. SPD INFO PACKET DATA BYTE 12 (PK_SPD_12BYTE) (0x875f)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_12BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_12BYTE	[7:0]	X	861B SPD_info packet Data byte 12

6.8.80. SPD INFO PACKET DATA BYTE 13 (PK_SPD_13BYTE) (0x8760)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_13BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_13BYTE	[7:0]	X	861B SPD_info packet Data byte 13

6.8.81. SPD INFO PACKET DATA BYTE 14 (PK_SPD_14BYTE) (0x8761)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_14BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_14BYTE	[7:0]	X	861B SPD_info packet Data byte 14

6.8.82. SPD INFO PACKET DATA BYTE 15 (PK_SPD_15BYTE) (0x8762)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_15BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_15BYTE	[7:0]	X	861B SPD_info packet Data byte 15

6.8.83. SPD INFO PACKET DATA BYTE 16 (PK_SPD_16BYTE) (0x8763)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_16BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_16BYTE	[7:0]	X	861B SPD_info packet Data byte 16

6.8.84. SPD INFO PACKET DATA BYTE 17 (PK_SPD_17BYTE) (0x8764)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_17BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_17BYTE	[7:0]	X	861B SPD_info packet Data byte 17

6.8.85. SPD INFO PACKET DATA BYTE 18 (PK_SPD_18BYTE) (0x8765)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_18BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_18BYTE	[7:0]	X	861B SPD_info packet Data byte 18

6.8.86. SPD INFO PACKET DATA BYTE 19 (PK_SPD_19BYTE) (0x8766)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_19BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_19BYTE	[7:0]	X	861B SPD_info packet Data byte 19

6.8.87. SPD INFO PACKET DATA BYTE 20 (PK_SPD_20BYTE) (0x8767)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_20BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_20BYTE	[7:0]	X	861B SPD_info packet Data byte 20

6.8.88. SPD INFO PACKET DATA BYTE 21 (PK_SPD_21BYTE) (0x8768)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_21BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_21BYTE	[7:0]	X	861B SPD_info packet Data byte 21

6.8.89. SPD INFO PACKET DATA BYTE 22 (PK_SPD_22BYTE) (0x8769)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_22BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_22BYTE	[7:0]	X	861B SPD_info packet Data byte 22

6.8.90. SPD INFO PACKET DATA BYTE 23 (PK_SPD_23BYTE) (0x876a)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_23BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_23BYTE	[7:0]	X	861B SPD_info packet Data byte 23

6.8.91. SPD INFO PACKET DATA BYTE 24 (PK_SPD_24BYTE) (0x876b)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_24BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_24BYTE	[7:0]	X	861B SPD_info packet Data byte 24

6.8.92. SPD INFO PACKET DATA BYTE 25 (PK_SPD_25BYTE) (0x876c)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_25BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_25BYTE	[7:0]	X	861B SPD_info packet Data byte 25

6.8.93. SPD INFO PACKET DATA BYTE 26 (PK_SPD_26BYTE) (0x876d)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_26BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_26BYTE	[7:0]	X	861B SPD_info packet Data byte 26 (Reserved for standards extension)

6.8.94. SPD INFO PACKET DATA BYTE 27 (PK_SPD_27BYTE) (0x876e)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	SPD_27BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
SPD_27BYTE	[7:0]	X	861B SPD_info packet Data byte 27 (Reserved for standards extension)

6.8.95. VS INFO PACKET HEADER BYTE 0 (PK_VS_0HEAD) (0x8770)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_0HEAD							
Type	RW							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_0HEAD	[7:0]	X	861B VS_info packet Header byte 0 (= type)

6.8.96. VS INFO PACKET HEADER BYTE 1 (PK_VS_1HEAD) (0x8771)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_1HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_1HEAD	[7:0]	X	861B VS_info packet Header byte 1 (= version)

6.8.97. VS INFO PACKET HEADER BYTE 2 (PK_VS_2HEAD) (0x8772)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_2HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_2HEAD	[7:0]	X	861B VS_info packet Header byte 2 (= data length)

6.8.98. VS INFO PACKET DATA BYTE 0 (PK_VS_0BYTE) (0x8773)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_0BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_0BYTE	[7:0]	X	861B VS_info packet Data byte 0 (= checksum)

6.8.99. VS INFO PACKET DATA BYTE 1 (PK_VS_1BYTE) (0x8774)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_1BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_1BYTE	[7:0]	X	861B VS_info packet Data byte 1

6.8.100. VS INFO PACKET DATA BYTE 2 (PK_VS_2BYTE) (0x8775)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_2BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_2BYTE	[7:0]	X	861B VS_info packet Data byte 2

6.8.101. VS INFO PACKET DATA BYTE 3 (PK_VS_3BYTE) (0x8776)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_3BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_3BYTE	[7:0]	X	861B VS_info packet Data byte 3

6.8.102. VS INFO PACKET DATA BYTE 4 (PK_VS_4BYTE) (0x8777)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_4BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_4BYTE	[7:0]	X	861B VS_info packet Data byte 4

6.8.103. VS INFO PACKET DATA BYTE 5 (PK_VS_5BYTE) (0x8778)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_5BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_5BYTE	[7:0]	X	861B VS_info packet Data byte 5

6.8.104. VS INFO PACKET DATA BYTE 6 (PK_VS_6BYTE) (0x8779)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_6BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_6BYTE	[7:0]	X	861B VS_info packet Data byte 6

6.8.105. VS INFO PACKET DATA BYTE 7 (PK_VS_7BYTE) (0x877a)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_7BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_7BYTE	[7:0]	X	861B VS_info packet Data byte 7

6.8.106. VS INFO PACKET DATA BYTE 8 (PK_VS_8BYTE) (0x877b)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_8BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_8BYTE	[7:0]	X	861B VS_info packet Data byte 8

6.8.107. VS INFO PACKET DATA BYTE 9 (PK_VS_9BYTE) (0x877c)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_9BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_9BYTE	[7:0]	X	861B VS_info packet Data byte 9

6.8.108. VS INFO PACKET DATA BYTE 10 (PK_VS_10BYTE) (0x877d)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_10BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_10BYTE	[7:0]	X	861B VS_info packet Data byte 10

6.8.109. VS INFO PACKET DATA BYTE 11 (PK_VS_11BYTE) (0x877e)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_11BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_11BYTE	[7:0]	X	861B VS_info packet Data byte 11

6.8.110. VS INFO PACKET DATA BYTE 12 (PK_VS_12BYTE) (0x877f)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_12BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_12BYTE	[7:0]	X	861B VS_info packet Data byte 12

6.8.111. VS INFO PACKET DATA BYTE 13 (PK_VS_13BYTE) (0x8780)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_13BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_13BYTE	[7:0]	X	861B VS_info packet Data byte 13

6.8.112. VS INFO PACKET DATA BYTE 14 (PK_VS_14BYTE) (0x8781)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_14BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_14BYTE	[7:0]	X	861B VS_info packet Data byte 14

6.8.113. VS INFO PACKET DATA BYTE 15 (PK_VS_15BYTE) (0x8782)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_15BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_15BYTE	[7:0]	X	861B VS_info packet Data byte 15

6.8.114. VS INFO PACKET DATA BYTE 16 (PK_VS_16BYTE) (0x8783)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_16BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_16BYTE	[7:0]	X	861B VS_info packet Data byte 16

6.8.115. VS INFO PACKET DATA BYTE 17 (PK_VS_17BYTE) (0x8784)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_17BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_17BYTE	[7:0]	X	861B VS_info packet Data byte 17

6.8.116. VS INFO PACKET DATA BYTE 18 (PK_VS_18BYTE) (0x8785)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_18BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_18BYTE	[7:0]	X	861B VS_info packet Data byte 18

6.8.117. VS INFO PACKET DATA BYTE 19 (PK_VS_19BYTE) (0x8786)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_19BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_19BYTE	[7:0]	X	861B VS_info packet Data byte 19

6.8.118. VS INFO PACKET DATA BYTE 20 (PK_VS_20BYTE) (0x8787)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_20BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_20BYTE	[7:0]	X	861B VS_info packet Data byte 20

6.8.119. VS INFO PACKET DATA BYTE 21 (PK_VS_21BYTE) (0x8788)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_21BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_21BYTE	[7:0]	X	861B VS_info packet Data byte 21

6.8.120. VS INFO PACKET DATA BYTE 22 (PK_VS_22BYTE) (0x8789)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_22BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_22BYTE	[7:0]	X	861B VS_info packet Data byte 22

6.8.121. VS INFO PACKET DATA BYTE 23 (PK_VS_23BYTE) (0x878a)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_23BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_23BYTE	[7:0]	X	861B VS_info packet Data byte 23

6.8.122. VS INFO PACKET DATA BYTE 24 (PK_VS_24BYTE) (0x878b)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_24BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_24BYTE	[7:0]	X	861B VS_info packet Data byte 24

6.8.123. VS INFO PACKET DATA BYTE 25 (PK_VS_25BYTE) (0x878c)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_25BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_25BYTE	[7:0]	X	861B VS_info packet Data byte 25

6.8.124. VS INFO PACKET DATA BYTE 26 (PK_VS_26BYTE) (0x878d)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_26BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_26BYTE	[7:0]	X	861B VS_info packet Data byte 26

6.8.125. VS INFO PACKET DATA BYTE 27 (PK_VS_27BYTE) (0x878e)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	VS_27BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
VS_27BYTE	[7:0]	X	861B VS_info packet Data byte 27

6.8.126. ACP INFO PACKET HEADER BYTE 0 (PK_ACP_0HEAD) (0x8790)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_0HEAD							
Type	RW							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_0HEAD	[7:0]	X	861B ACP_info packet Header byte 0 (= type)

6.8.127. ACP INFO PACKET HEADER BYTE 1 (PK_ACP_1HEAD) (0x8791)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_1HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_1HEAD	[7:0]	X	861B ACP_info packet Header byte 1 (= version)

6.8.128. ACP INFO PACKET HEADER BYTE 2 (PK_ACP_2HEAD) (0x8792)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_2HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_2HEAD	[7:0]	X	861B ACP_info packet Header byte 2 (= data length)

6.8.129. ACP INFO PACKET DATA BYTE 0 (PK_ACP_0BYTE) (0x8793)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_0BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_0BYTE	[7:0]	X	861B ACP_info packet Data byte 0 (= checksum)

6.8.130. ACP INFO PACKET DATA BYTE 1 (PK_ACP_1BYTE) (0x8794)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_1BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_1BYTE	[7:0]	X	861B ACP_info packet Data byte 1

6.8.131. ACP INFO PACKET DATA BYTE 2 (PK_ACP_2BYTE) (0x8795)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_2BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_2BYTE	[7:0]	X	861B ACP_info packet Data byte 2

6.8.132. ACP INFO PACKET DATA BYTE 3 (PK_ACP_3BYTE) (0x8796)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_3BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_3BYTE	[7:0]	X	861B ACP_info packet Data byte 3

6.8.133. ACP INFO PACKET DATA BYTE 4 (PK_ACP_4BYTE) (0x8797)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_4BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_4BYTE	[7:0]	X	861B ACP_info packet Data byte 4

6.8.134. ACP INFO PACKET DATA BYTE 5 (PK_ACP_5BYTE) (0x8798)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_5BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_5BYTE	[7:0]	X	861B ACP_info packet Data byte 5

6.8.135. ACP INFO PACKET DATA BYTE 6 (PK_ACP_6BYTE) (0x8799)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_6BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_6BYTE	[7:0]	X	861B ACP_info packet Data byte 6

6.8.136. ACP INFO PACKET DATA BYTE 7 (PK_ACP_7BYTE) (0x879a)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_7BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_7BYTE	[7:0]	X	861B ACP_info packet Data byte 7

6.8.137. ACP INFO PACKET DATA BYTE 8 (PK_ACP_8BYTE) (0x879b)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_8BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_8BYTE	[7:0]	X	861B ACP_info packet Data byte 8

6.8.138. ACP INFO PACKET DATA BYTE 9 (PK_ACP_9BYTE) (0x879c)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_9BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_9BYTE	[7:0]	X	861B ACP_info packet Data byte 9

6.8.139. ACP INFO PACKET DATA BYTE 10 (PK_ACP_10BYTE) (0x879d)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_10BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_10BYTE	[7:0]	X	861B ACP_info packet Data byte 10

6.8.140. ACP INFO PACKET DATA BYTE 11 (PK_ACP_11BYTE) (0x879e)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_11BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_11BYTE	[7:0]	X	861B ACP_info packet Data byte 11

6.8.141. ACP INFO PACKET DATA BYTE 12 (PK_ACP_12BYTE) (0x879f)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_12BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_12BYTE	[7:0]	X	861B ACP_info packet Data byte 12

6.8.142. ACP INFO PACKET DATA BYTE 13 (PK_ACP_13BYTE) (0x87a0)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_13BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_13BYTE	[7:0]	X	861B ACP_info packet Data byte 13

6.8.143. ACP INFO PACKET DATA BYTE 14 (PK_ACP_14BYTE) (0x87a1)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_14BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_14BYTE	[7:0]	X	861B ACP_info packet Data byte 14

6.8.144. ACP INFO PACKET DATA BYTE 15 (PK_ACP_15BYTE) (0x87a2)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_15BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_15BYTE	[7:0]	X	861B ACP_info packet Data byte 15

6.8.145. ACP INFO PACKET DATA BYTE 16 (PK_ACP_16BYTE) (0x87a3)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_16BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_16BYTE	[7:0]	X	861B ACP_info packet Data byte 16

6.8.146. ACP INFO PACKET DATA BYTE 17 (PK_ACP_17BYTE) (0x87a4)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_17BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_17BYTE	[7:0]	X	861B ACP_info packet Data byte 17

6.8.147. ACP INFO PACKET DATA BYTE 18 (PK_ACP_18BYTE) (0x87a5)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_18BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_18BYTE	[7:0]	X	861B ACP_info packet Data byte 18

6.8.148. ACP INFO PACKET DATA BYTE 19 (PK_ACP_19BYTE) (0x87a6)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_19BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_19BYTE	[7:0]	X	861B ACP_info packet Data byte 19

6.8.149. ACP INFO PACKET DATA BYTE 20 (PK_ACP_20BYTE) (0x87a7)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_20BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_20BYTE	[7:0]	X	861B ACP_info packet Data byte 20

6.8.150. ACP INFO PACKET DATA BYTE 21 (PK_ACP_21BYTE) (0x87a8)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_21BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_21BYTE	[7:0]	X	861B ACP_info packet Data byte 21

6.8.151. ACP INFO PACKET DATA BYTE 22 (PK_ACP_22BYTE) (0x87a9)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_22BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_22BYTE	[7:0]	X	861B ACP_info packet Data byte 22

6.8.152. ACP INFO PACKET DATA BYTE 23 (PK_ACP_23BYTE) (0x87aa)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_23BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_23BYTE	[7:0]	X	861B ACP_info packet Data byte 23

6.8.153. ACP INFO PACKET DATA BYTE 24 (PK_ACP_24BYTE) (0x87ab)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_24BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_24BYTE	[7:0]	X	861B ACP_info packet Data byte 24

6.8.154. ACP INFO PACKET DATA BYTE 25 (PK_ACP_25BYTE) (0x87ac)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_25BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_25BYTE	[7:0]	X	861B ACP_info packet Data byte 25

6.8.155. ACP INFO PACKET DATA BYTE 26 (PK_ACP_26BYTE) (0x87ad)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_26BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_26BYTE	[7:0]	X	861B ACP_info packet Data byte 26

6.8.156. ACP INFO PACKET DATA BYTE 27 (PK_ACP_27BYTE) (0x87ae)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ACP_27BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ACP_27BYTE	[7:0]	X	861B ACP_info packet Data byte 27

6.8.157. ISRC1 INFO PACKET HEADER BYTE 0 (PK_ISRC1_0HEAD) (0x87b0)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC1_0HEAD							
Type	RW							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC1_0HEAD	[7:0]	X	861B ISRC1_info packet Header byte 0 (= type)

6.8.158. ISRC1 INFO PACKET HEADER BYTE 1 (PK_ISRC1_1HEAD) (0x87b1)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC1_1HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC1_1HEAD	[7:0]	X	861B ISRC1_info packet Header byte 1 (= version)

6.8.159. ISRC1 INFO PACKET HEADER BYTE 2 (PK_ISRC1_2HEAD) (0x87b2)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC1_2HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC1_2HEAD	[7:0]	X	861B ISRC1_info packet Header byte 2 (= data length)

6.8.160. ISRC1 INFO PACKET DATA BYTE 0 (PK_ISRC1_0BYTE) (0x87b3)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC1_0BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC1_0BYTE	[7:0]	X	861B ISRC1_info packet Data byte 0 (= checksum)

6.8.161. ISRC1 INFO PACKET DATA BYTE 1 (PK_ISRC1_1BYTE) (0x87b4)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC1_1BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC1_1BYTE	[7:0]	X	861B ISRC1_info packet Data byte 1

6.8.162. ISRC1 INFO PACKET DATA BYTE 2 (PK_ISRC1_2BYTE) (0x87b5)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC1_2BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC1_2BYTE	[7:0]	X	861B ISRC1_info packet Data byte 2

6.8.163. ISRC1 INFO PACKET DATA BYTE 3 (PK_ISRC1_3BYTE) (0x87b6)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC1_3BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC1_3BYTE	[7:0]	X	861B ISRC1_info packet Data byte 3

6.8.164. ISRC1 INFO PACKET DATA BYTE 4 (PK_ISRC1_4BYTE) (0x87b7)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC1_4BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC1_4BYTE	[7:0]	X	861B ISRC1_info packet Data byte 4

6.8.165. ISRC1 INFO PACKET DATA BYTE 5 (PK_ISRC1_5BYTE) (0x87b8)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC1_5BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC1_5BYTE	[7:0]	X	861B ISRC1_info packet Data byte 5

6.8.166. ISRC1 INFO PACKET DATA BYTE 6 (PK_ISRC1_6BYTE) (0x87b9)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC1_6BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC1_6BYTE	[7:0]	X	861B ISRC1_info packet Data byte 6

6.8.167. ISRC1 INFO PACKET DATA BYTE 7 (PK_ISRC1_7BYTE) (0x87ba)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC1_7BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC1_7BYTE	[7:0]	X	861B ISRC1_info packet Data byte 7

6.8.168. ISRC1 INFO PACKET DATA BYTE 8 (PK_ISRC1_8BYTE) (0x87bb)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC1_8BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC1_8BYTE	[7:0]	X	861B ISRC1_info packet Data byte 8

6.8.169. ISRC1 INFO PACKET DATA BYTE 9 (PK_ISRC1_9BYTE) (0x87bc)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC1_9BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC1_9BYTE	[7:0]	X	861B ISRC1_info packet Data byte 9

6.8.170. ISRC1 INFO PACKET DATA BYTE 10 (PK_ISRC1_10BYTE) (0x87bd)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC1_10BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC1_10BYTE	[7:0]	X	861B ISRC1_info packet Data byte 10

6.8.171. ISRC1 INFO PACKET DATA BYTE 11 (PK_ISRC1_11BYTE) (0x87be)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC1_11BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC1_11BYTE	[7:0]	X	861B ISRC1_info packet Data byte 11

6.8.172. ISRC1 INFO PACKET DATA BYTE 12 (PK_ISRC1_12BYTE) (0x87bf)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC1_12BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC1_12BYTE	[7:0]	X	861B ISRC1_info packet Data byte 12

6.8.173. ISRC1 INFO PACKET DATA BYTE 13 (PK_ISRC1_13BYTE) (0x87c0)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC1_13BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC1_13BYTE	[7:0]	X	861B ISRC1_info packet Data byte 13

6.8.174. ISRC1 INFO PACKET DATA BYTE 14 (PK_ISRC1_14BYTE) (0x87c1)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC1_14BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC1_14BYTE	[7:0]	X	861B ISRC1_info packet Data byte 14

6.8.175. ISRC1 INFO PACKET DATA BYTE 15 (PK_ISRC1_15BYTE) (0x87c2)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC1_15BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC1_15BYTE	[7:0]	X	861B ISRC1_info packet Data byte 15

6.8.176. ISRC2 INFO PACKET HEADER BYTE 0 (PK_ISRC2_0HEAD) (0x87d0)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_0HEAD							
Type	RW							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_0HEAD	[7:0]	X	861B ISRC2_info packet Header byte 0 (= type)

6.8.177. ISRC2 INFO PACKET HEADER BYTE 1 (PK_ISRC2_1HEAD) (0x87d1)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_1HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_1HEAD	[7:0]	X	861B ISRC2_info packet Header byte 1 (= version)

6.8.178. ISRC2 INFO PACKET HEADER BYTE 2 (PK_ISRC2_2HEAD) (0x87d2)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_2HEAD							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_2HEAD	[7:0]	X	861B ISRC2_info packet Header byte 2 (= data length)

6.8.179. ISRC2 INFO PACKET DATA BYTE 0 (PK_ISRC2_0BYTE) (0x87d3)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_0BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_0BYTE	[7:0]	X	861B ISRC2_info packet Data byte 0 (= checksum)

6.8.180. ISRC2 INFO PACKET DATA BYTE 1 (PK_ISRC2_1BYTE) (0x87d4)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_1BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_1BYTE	[7:0]	X	861B ISRC2_info packet Data byte 1

6.8.181. ISRC2 INFO PACKET DATA BYTE 2 (PK_ISRC2_2BYTE) (0x87d5)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_2BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_2BYTE	[7:0]	X	861B ISRC2_info packet Data byte 2

6.8.182. ISRC2 INFO PACKET DATA BYTE 3 (PK_ISRC2_3BYTE) (0x87d6)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_3BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_3BYTE	[7:0]	X	861B ISRC2_info packet Data byte 3

6.8.183. ISRC2 INFO PACKET DATA BYTE 4 (PK_ISRC2_4BYTE) (0x87d7)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_4BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_4BYTE	[7:0]	X	861B ISRC2_info packet Data byte 4

6.8.184. ISRC2 INFO PACKET DATA BYTE 5 (PK_ISRC2_5BYTE) (0x87d8)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_5BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_5BYTE	[7:0]	X	861B ISRC2_info packet Data byte 5

6.8.185. ISRC2 INFO PACKET DATA BYTE 6 (PK_ISRC2_6BYTE) (0x87d9)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_6BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_6BYTE	[7:0]	X	861B ISRC2_info packet Data byte 6

6.8.186. ISRC2 INFO PACKET DATA BYTE 7 (PK_ISRC2_7BYTE) (0x87da)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_7BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_7BYTE	[7:0]	X	861B ISRC2_info packet Data byte 7

6.8.187. ISRC2 INFO PACKET DATA BYTE 8 (PK_ISRC2_8BYTE) (0x87db)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_8BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_8BYTE	[7:0]	X	861B ISRC2_info packet Data byte 8

6.8.188. ISRC2 INFO PACKET DATA BYTE 9 (PK_ISRC2_9BYTE) (0x87dc)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_9BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_9BYTE	[7:0]	X	861B ISRC2_info packet Data byte 9

6.8.189. ISRC2 INFO PACKET DATA BYTE 10 (PK_ISRC2_10BYTE) (0x87dd)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_10BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_10BYTE	[7:0]	X	861B ISRC2_info packet Data byte 10

6.8.190. ISRC2 INFO PACKET DATA BYTE 11 (PK_ISRC2_11BYTE) (0x87de)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_11BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_11BYTE	[7:0]	X	861B ISRC2_info packet Data byte 11

6.8.191. ISRC2 INFO PACKET DATA BYTE 12 (PK_ISRC2_12BYTE) (0x87df)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_12BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_12BYTE	[7:0]	X	861B ISRC2_info packet Data byte 12

6.8.192. ISRC2 INFO PACKET DATA BYTE 13 (PK_ISRC2_13BYTE) (0x87e0)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_13BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_13BYTE	[7:0]	X	861B ISRC2_info packet Data byte 13

6.8.193. ISRC2 INFO PACKET DATA BYTE 14 (PK_ISRC2_14BYTE) (0x87e1)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_14BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_14BYTE	[7:0]	X	861B ISRC2_info packet Data byte 14

6.8.194. ISRC2 INFO PACKET DATA BYTE 15 (PK_ISRC2_15BYTE) (0x87e2)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_15BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_15BYTE	[7:0]	X	861B ISRC2_info packet Data byte 15

6.8.195. ISRC2 INFO PACKET DATA BYTE 16 (PK_ISRC2_16BYTE) (0x87e3)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_16BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_16BYTE	[7:0]	X	861B ISRC2_info packet Data byte 16

6.8.196. ISRC2 INFO PACKET DATA BYTE 17 (PK_ISRC2_17BYTE) (0x87e4)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_17BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_17BYTE	[7:0]	X	861B ISRC2_info packet Data byte 17

6.8.197. ISRC2 INFO PACKET DATA BYTE 18 (PK_ISRC2_18BYTE) (0x87e5)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_18BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_18BYTE	[7:0]	X	861B ISRC2_info packet Data byte 18

6.8.198. ISRC2 INFO PACKET DATA BYTE 19 (PK_ISRC2_19BYTE) (0x87e6)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_19BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_19BYTE	[7:0]	X	861B ISRC2_info packet Data byte 19

6.8.199. ISRC2 INFO PACKET DATA BYTE 20 (PK_ISRC2_20BYTE) (0x87e7)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_20BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_20BYTE	[7:0]	X	861B ISRC2_info packet Data byte 20

6.8.200. ISRC2 INFO PACKET DATA BYTE 21 (PK_ISRC2_21BYTE) (0x87e8)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_21BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_21BYTE	[7:0]	X	861B ISRC2_info packet Data byte 21

6.8.201. ISRC2 INFO PACKET DATA BYTE 22 (PK_ISRC2_22BYTE) (0x87e9)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_22BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_22BYTE	[7:0]	X	861B ISRC2_info packet Data byte 22

6.8.202. ISRC2 INFO PACKET DATA BYTE 23 (PK_ISRC2_23BYTE) (0x87ea)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_23BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_23BYTE	[7:0]	X	861B ISRC2_info packet Data byte 23

6.8.203. ISRC2 INFO PACKET DATA BYTE 24 (PK_ISRC2_24BYTE) (0x87eb)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_24BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_24BYTE	[7:0]	X	861B ISRC2_info packet Data byte 24

6.8.204. ISRC2 INFO PACKET DATA BYTE 25 (PK_ISRC2_25BYTE) (0x87ec)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_25BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_25BYTE	[7:0]	X	861B ISRC2_info packet Data byte 25

6.8.205. ISRC2 INFO PACKET DATA BYTE 26 (PK_ISRC2_26BYTE) (0x87ed)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_26BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_26BYTE	[7:0]	X	861B ISRC2_info packet Data byte 26

6.8.206. ISRC2 INFO PACKET DATA BYTE 27 (PK_ISRC2_27BYTE) (0x87ee)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	ISRC2_27BYTE							
Type	RO							
Default	X	X	X	X	X	X	X	X

Register Field	Bit	Default	Description
ISRC2_27BYTE	[7:0]	X	861B ISRC2_info packet Data byte 27

6.9. HDMI Rx HDCP Registers

Only a few a listed here. The others can be referred to HDCP specification. For register 0x88_XX, please refer to HDCP register 0xXX. For example: For register 0x88_08 ➔ HDCP Ri'0 Data.

6.9.1. HDCP BCAPS Register (BCAPS) (0x8840)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	HDMI_RSVD	Repeater	Ready	FastI2C	Reserved		1.1Fea	Fast_ReAu
Type	RW	RW	RW	RW	RO		RW	RW
Default	1	0	0	0	0		0	0

Register Field	Bit	Default	Description
HDMI_RESERVED	[7]	1	0: automatic move to HDMI mode is not performed.
REPETER	[6]	0	1: HDCP Repeater
READY	[5]	0	KSVFiFo is Ready for 2nd Authentication
FAST (DDC I2C speed)	[4]	0	1: 400 kHz Supported
Reserved	[3:2]	0	-
1.1_FEATURES	[1]	0	Fixed at '0'
FAST_REAUTH	[0]	0	Fast re-authentication

6.9.2. HDCP Rx BSTAUS0 Register (BSTATUS0) (0x8841)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	MAX_DEVS_EXCEEDED	DEVICE_COUNT						
Type	RW	RW						
Default	0	0x00						

Register Field	Bit	Description
MAX_DEVS_EXCEEDED	[7]	If later stage connection devices number is 17 or more, set to "1".
DEVICE_COUNT	[6:0]	Later stage connection device number (not including self)

6.9.3. HDCP Rx BSTAUS1 Register (BSTATUS1) (0x8842)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved		HDMI_RSVD	HDMI_MODE	MAX_EXCED	DEPTH		
Type	RO		RW	RW	RW	RW		
Default	0		0	0	0	0		

Register Field	Bit	Default	Description
Reserved	[7:6]	0	–
HDMI_RSVD	[5]	0	V' value calculation state machine reset 1: Reset (Auto clear)
HDMI_MODE	[4]	0	HDMI mode setting 0: DVI mode 1: HDMI mode
MAX_EXCED	[3]	0	Topology error indicator. When set to one, more than seven levels of the repeater have been cascaded together.
DEPTH	[2:0]	0	Three-bit repeater cascade depth. This value gives the number of attached levels through the connection topology.

6.9.4. KSVFIFO Register (KSVFIFO) (0x8843)

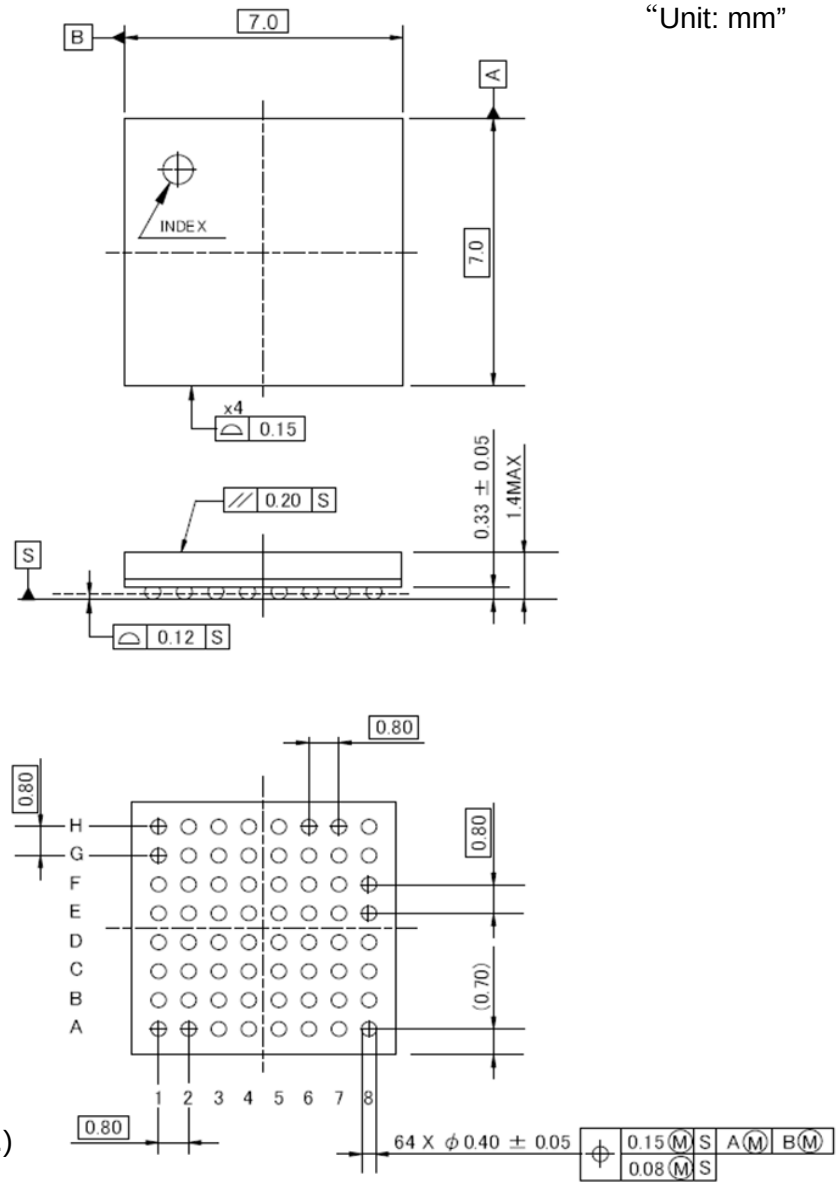
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	KSVFIFO							
Type	RW							
Default	0							

Register Field	Bit	Default	Description
KSVFIFO	[7:0]	0x00	Total 80Byte for 16Devices, DDC Address: 0x74, Offset 0x43

7. Package

The packages for TC9590XBG are described in the figures below.

"Unit: mm"



Weight: 98 mg (Typ.)

Figure 7.1 TC9590XBG package (64 pins)

Table 7-1 Mechanical Dimension

Dimension	Min	Typ.	Max
Solder ball pitch	---	0.80 mm	---
Package dimension	---	7.0 x 7.0 mm^2	---
Package height	---	---	1.4 mm

8. Electrical Characteristics

8.1. Absolute Maximum Ratings

VSS = 0V reference

Parameter	Symbol	Rating	Unit
Supply voltage (1.8V - Digital IO)	VDDIO	-0.3 to +3.9	V
Supply voltage (1.2V – Digital Core)	VDDC	-0.3 to +1.8	V
Supply voltage (1.2V – MIPI CSI PHY)	VDD_MIPI	-0.3 to +1.8	V
Supply voltage (3.3V – HDMIRX Phy)	AVDD33	-0.3 to +3.9	V
Supply voltage (1.2V – HDMIRX Phy)	AVDD12	-0.3 to +1.8	V
Supply voltage (2.5V – APLL)	AVDD25	-0.3 to +2.75	V
Input voltage (CSI IO)	V_{IN_CSI}	-0.3 to VDD_MIPI+0.3	V
Output voltage (CSI IO)	V_{OUT_CSI}	-0.3 to VDD_MIPI+0.3	V
Input voltage (Digital IO)	V_{IN_IO}	-0.3 to VDDIO+0.3	V
Output voltage (Digital IO)	V_{OUT_IO}	-0.3 to VDDIO+0.3	V
Output voltage (APLL)	V_{OUT_APLL}	-0.3 to AVDD25+0.3	V
Junction temperature	Tj	125	°C
Storage temperature	Tstg	-40 to +125	°C

8.2. Operating Condition

VSS = 0V reference

Parameter	Symbol	Min	Typ.	Max	Unit
Supply voltage (1.8/3.3V – Digital IO)	VDDIO2	1.65	1.8	3.6	V
Supply voltage (3.3V – HDMI Digital IO)	VDDIO1	3.0	3.3	3.6	V
Supply voltage (1.2V – Digital Core)	VDDC	1.1	1.2	1.3	V
Supply voltage (1.2V – MIPI CSI PHY)	VDD_MIPI	1.1	1.2	1.3	V
Supply voltage (2.5V – APLL)	AVDD25	2.25	2.5	2.75	V
Operating temperature (ambient temperature with voltage applied)	Ta	-40	25	85	^{o}C
Supply Noise Voltage	VSN	-	-	0.1	Vpp
Supply voltage (3.3V – HDMIRX PHY)	AVDD33	3.135	3.3	3.465	V
Supply Noise Voltage for AVDD33	VSN33	-	-	0.08	Vpp
Supply voltage (1.2V – HDMIRX PHY)	AVDD12	1.15	1.2	1.25	V
Supply Noise Voltage for AVDD12	VSN12	-	-	0.04	Vpp

8.3. DC Electrical Specification

Parameter	Symbol	Min	Typ.	Max	Unit
Input voltage, High level input Note1	V_{IH}	0.7 VDDIO	-	VDDIO	V
Input voltage, Low level input Note1	V_{IL}	0	-	0.3 VDDIO	V
Input voltage High level CMOS Schmitt Trigger Note1, 2	V_{IHS}	0.7 VDDIO	-	VDDIO	V
Input voltage Low level CMOS Schmitt Trigger Note1, 2	V_{ILS}	0	-	0.3 VDDIO	V
Output voltage High level Note1, Note2	V_{OH}	0.8 VDDIO	-	VDDIO	V
Output voltage Low level Note1, Note2	V_{OL}	0	-	0.2 VDDIO	V
Input leak current, High level (Condition: V_{IN} = +VDDIO, VDDIO = 3.6V)	I_{ILH1} (Note3)	-10	-	10	µA
Input leak current, Low level (Condition: V_{IN} = 0V, VDDIO = 3.6V)	I_{ILL1} (Note4)	-10	-	10	µA

Note1: Each power source is operating within recommended operation condition.

Note2: Current output value is specified to each IO buffer individually. Output voltage changes with output current value.

Note3: Normal pin or Pull-up IO pin applied VDDIO supply voltage to Vin (input voltage)

Note4: Normal pin applied VSS (0V) to Vin (input voltage)

9. Timing Definitions

9.1. RefClk Input Requirement

Parameter	Min	Typ.	Max	Unit
Frequency	26/27 or 42			MHz
Duty Cycle	40	50	60	%
Jitter	-100	0	100	ppm

9.2. MIPI CSI-2 Timings

Timing specification below has been ported from MIPI Alliance specification for D-PHY version 01-00-00. Timing defined in MIPI Alliance specification for D-PHY version 01-00-00 has precedence over timing described in the sections below.

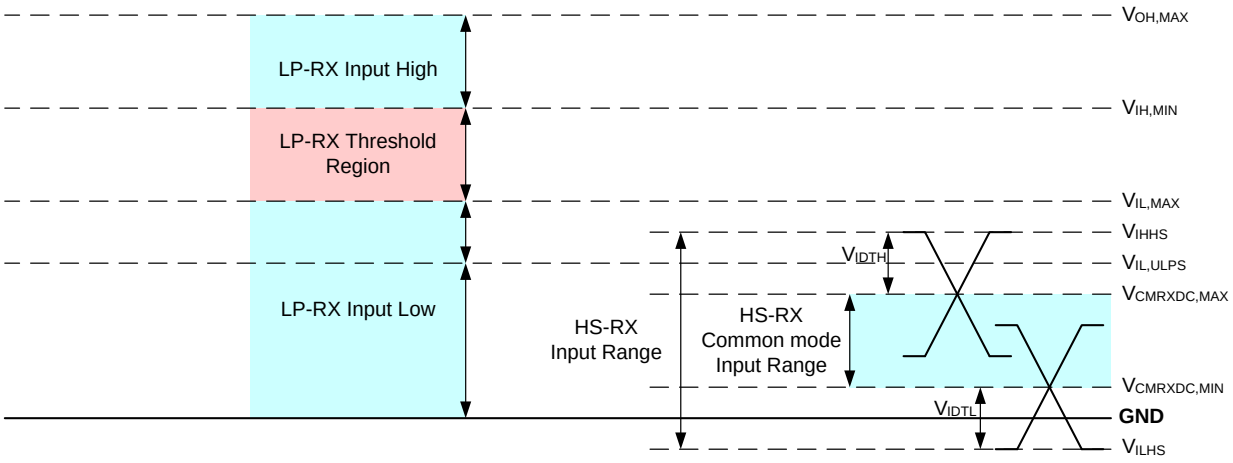


Figure 9.1 Signaling and voltage levels

Table 9-1 MIPI Tx DC specifications

Parameter	Description	Min	Typ.	Max	Unit	Note
HS mode						
VCMTX	HS transmit static common mode voltage	150	200	250	mV	1
|ΔVCMTX(1,0)|	VCMTX mismatch when output is Differential-1 or Differential-0	-	-	5	mV	2
|VOD|	HS transmit differential voltage	140	200	270	mV	1
|ΔVOD|	VOD mismatch when output is Differential-1 or Differential-0	-	-	10	mV	2
VOHHS	HS output high voltage	-	-	360	mV	-
ZOS	Single ended output impedance	40	50	62.5	Ω	-
ΔZOS	Single ended output impedance mismatch	-	-	10	%	-
LP Mode						
VOH	Thevenin output high level	1.1	1.2	1.3	V	-
VOL	Thevenin output low level	-50	-	50	mV	-
ZOLP	Output impedance of LP transmitter	110	-	-	Ω	3

Note:
1. Value when driving into load impedance anywhere in the ZID range.
2. It is recommended the implementer minimize ΔVOD and ΔVCMTX(1,0) in order to minimize radiation and optimize signal integrity.
3. Though no maximum value for ZOLP is specified, the LP transmitter output impedance shall ensure the TRLP/TFLP specification is met.

Table 9-2 MIPI High Speed Tx AC specifications

Parameter	Description	Min	Typ.	Max	Unit	Note
ΔVCMTX(HF)	Common-level variations above 450 MHz	-	-	15	mVRMS	-
ΔVCMTX(LF)	Common-level variation between 50 MHz– 450 MHz	-	-	25	mVPEAK	-
tR and tF	20% - 80% rise time and fall time	-	-	0.3	UI	1
		150	-	-	ps	-

Note:
1. UI is equal to 1/(2*fh). See section 7.3 for the definition of fh.

Table 9-3 MIPI Low Power Tx AC characteristics

Parameter	Description		Min	Typ.	Max	Unit	Note
TRLP/TFLP	15% - 85% rise time and fall time		-	-	25	ns	1
TREOT	30% - 85% rise time and fall time		-	-	35	ns	1, 5, 6
-	Pulse width of the LP exclusive-OR clock	First LP exclusive-OR clock pulse after Stop state or last pulse before Stop state	40	-	-	ns	4
		All other pulses	20	-	-	ns	4
TLP-PER-TX	Period of the LP exclusive-OR clock		90	-	-	ns	-
δV/δtSR	Slew rate @ CLOAD = 0 pF		30	-	500	mV/ns	1, 2, 3, 7
	Slew rate @ CLOAD = 5 pF		30	-	200	mV/ns	1, 2, 3, 7
	Slew rate @ CLOAD = 20 pF		30	-	150	mV/ns	1, 2, 3, 7
	Slew rate @ CLOAD = 70 pF		30	-	100	mV/ns	1, 2, 3, 7
CLOAD	Load capacitance		0	-	70	pF	1

Note:

1. CLOAD includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be < 10 pF. The distributed line capacitance can be up to 50 pF for a transmission line with 2ns delay.
2. When the output voltage is between 15% and below 85% of the fully settled LP signal levels.
3. Measured as average across any 50 mV segment of the output signal transition.
4. This parameter value can be lower than TLPX due to differences in rise vs. fall signal slopes and trip levels and mismatches between Dp and Dn LP transmitters. Any LP exclusive-OR pulse observed during HS EoT (transition from HS level to LP-11) is glitch behavior.
5. The rise-time of TREOT starts from the HS common-level at the moment the differential amplitude drops below 70 mV, due to stopping the differential drive.
6. With an additional load capacitance CCM between 0 - 60 pF on the termination center tap at RX side of the Lane.
7. This value represents a corner point in a piecewise linear curve.

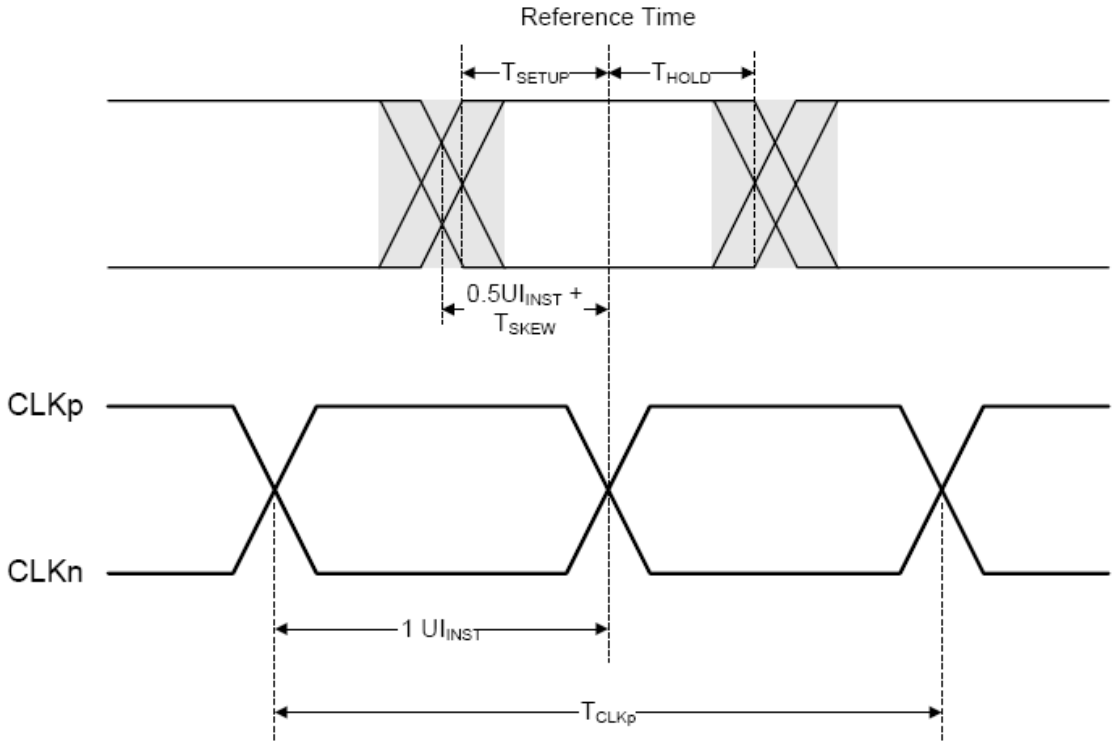


Figure 9.2 Data to clock timing reference

Table 9-4 Data-Clock timing specification

Parameter	Description	Min	Typ.	Max	Unit	Note
T_{SKEW}	Data to clock skew measured at the transmitter	-0.15	-	0.15	UI_{INST}	-
T_{SETUP}	Data to clock setup time at receiver	0.15	-	-	UI_{INST}	-
T_{HOLD}	clock to data hold time at receiver	0.15	-	-	UI_{INST}	-
UI_{INST}	1 Data bit time (instantaneous)	-	-	12.5	ns	-
T_{CLKp}	Period of dual data rate clock	2	2	2	UI_{INST}	-

9.3. I²C/DDC/EDIDI2C Timings

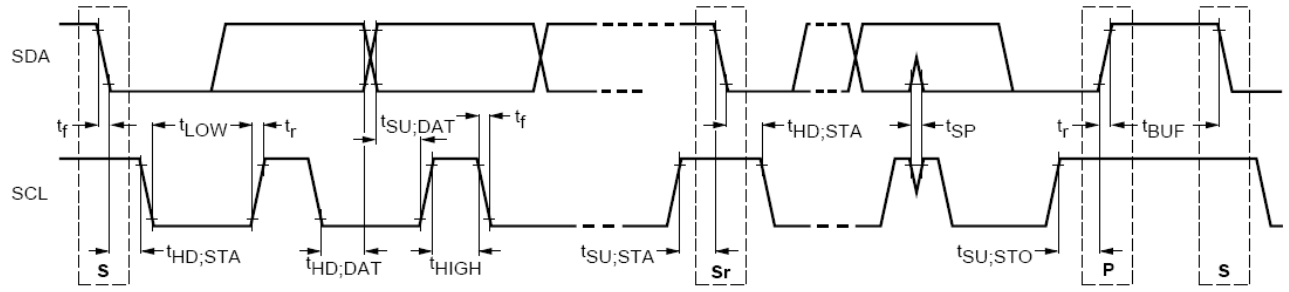


Figure 9.3 I²C/DDC/EDIDI2C Timing Diagram

Table 9-5 I²C/DDC/EDIDI2C Timing Specification

Item	Symbol	Min	Max	Unit
SCL clock frequency	f_{SCL}	0	400 Note1	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	0.6	-	µs
LOW period of the SCL clock	t_{LOW}	1.3	-	µs
HIGH period of the SCL clock	t_{HIGH}	0.6	-	µs
Set-up time for a repeated START condition	$t_{SU;STA}$	0.6	-	µs
Data hold time: for I²C-bus devices	$t_{HD;DAT}$	0	0.9	µs
Data set-up time	$t_{SU;DAT}$	100	-	ns
Rise time of both SDA and SCL signals	t_r	20+0.1Cb Note2	300	ns
Fall time of both SDA and SCL signals	t_f	20+0.1Cb Note2	300	ns
Set-up time for STOP condition	$t_{SU;STO}$	0.6	-	µs
Bus free time between a STOP and START condition	t_{BUF}	1.3	-	µs

Note:

1. DDC Bus is limited to max at 100 kHz.
2. Cb = Capacitive load for each bus line (400 pF max).

9.4. HDMI-RX Input

(Ta = 25℃, AVDD12VADC = 1.25V, DVDD12HDMI = 1.20V, AVDD33VADC = 3.3V, AVDD33VADC = 3.3V, DVDD33HDMI = 3.3V)

Parameter	Symbol	Min	Typ.	Max	Unit	Comment
HDMI Clock Frequency	FIN	25	---	165	MHz	300 mVp-p
HDMI minimum Amplitude	VMIN	150	---	---	mVp-p	165 MHz at TP2 Compliance test (TestID 8-5)

9.5. I2S/TDM Timings

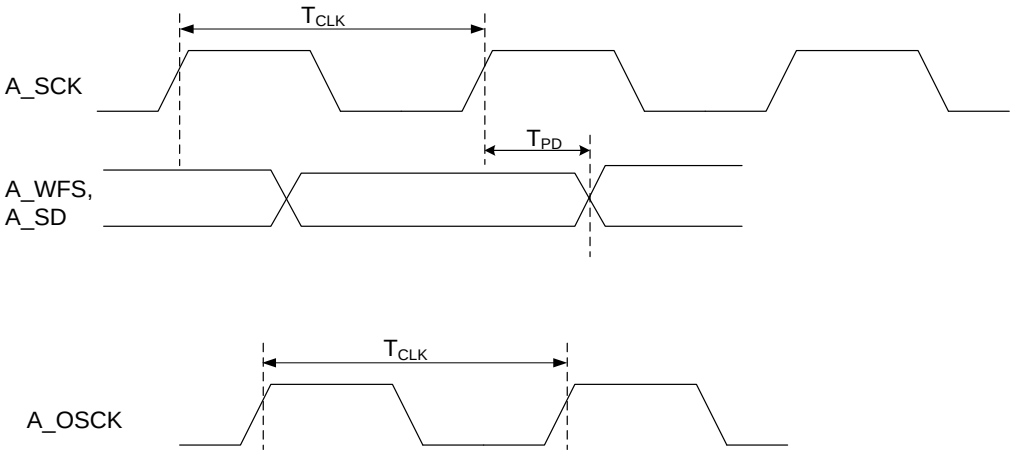


Figure 9.4 I2S/TDM Timing Diagram

Table 9-6 I2S/TDM timing specification

Item	Symbol	Min	Typ.	Max	Unit
Propagation Output Delay	T_{PD}	2	--	9	ns
Clock Period	T_{CLK}	20	--	--	ns

Note: Above timings are for 15 pF load on all I2S/TDM signals.

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