1.1.1. LPDDR4-3200 design recommendations

The following list details some generic guidelines that should be adhered to when implementing an i.MX 8M Nano design using LPDDR4.

1. It is expected that the layout engineer and design team already have experience and training with DDR designs at speeds of 1.6 GHz / 3200 MT/s.
2. All high-speed signal traces must reference a solid GND plane. Referencing only to the VDD power plane is not supported.
3. Keep edge to edge spacing of high speed signal traces no less than 2 times the trace width to minimize trace crosstalk. Increase spacing when available in the system.
4. At a speed of 3200 MT/s, signal vias can be a significant source of crosstalk. If not properly designed, they can introduce crosstalk larger than that from the trace. To minimize via crosstalk, make sure the total number of vias to be two or less on each point-to-point single-ended/differential trace. Place at least one ground stitching via within 50 mils of signal via when switching reference planes to provide continuous return path and reduce crosstalk. If it is not possible to place enough ground stitching vias due to space limitation, try to make the length that the signal actually travels on the via as short as possible, as illustrated in **Figure 1**.

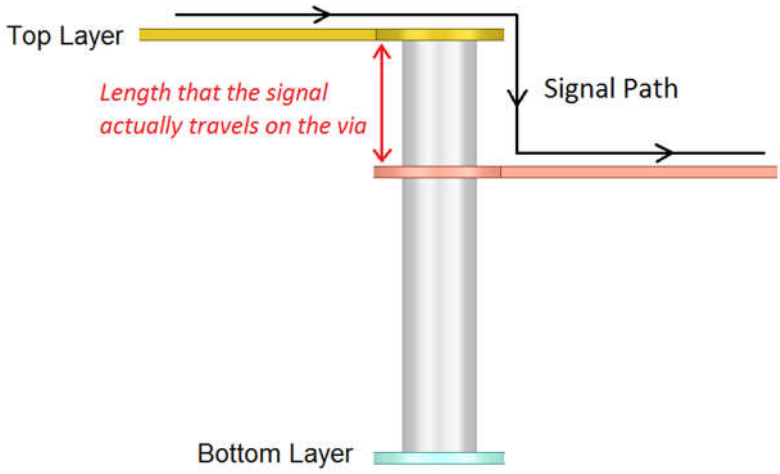

Figure 1. Length that the signal actually travels on the Via

5. CLK and DQS signals can be routed on different layer with DQ/CA signals to ease routing. When doing this, keep no less than 5 times trace width spacing from other signals.
6. Use time delay instead of length when performing the delay matching. The delay matching includes the PCB trace delay and the IC package delay. Incorporate the package pin delay into the CAD tool's constraint manager.
7. Include the delay of vias when performing delay matching. This can be realized in

Allegro tool by enabling the **Z Axis Delay** in “Setup -> Constraints -> Modes”.

8. Data Byte swapping within each 16-bit channel is OK. Bit swapping within each slice/byte lane is OK.
9. Bit swapping of Command/Address (CA[5:0], CKE[1:0], CS[1:0]) signals is **NOT** allowed.
10. i.MX 8M Nano does not drive ODT_CA signal. The ODT_CA balls on the LPDDR4 devices should be connected directly to the VDD2 supply.
11. In general, the 200-ball LPDDR4 package should be placed 200 mils from the i.MX 8M Nano.
12. Enable the DBI (data bus inversion) feature. It can help reduce both power consumption and power noise.
13. The LPDDR4 routing delay rules allow for reduction of most DATA bus serpentine requirements resulting in easier routing on i.MX 8M Nano. Command Bus Training is required for LPDDR4. Please ensure SW enables and configures the Command Bus Training.
14. The LPDDR4 routing delay rules allow for limited reduction Command/Address bus serpentine requirements on i.MX 8M Nano. Address/Command Bus is sectioned into 3 group that still require tight timing control. Command Bus Training is required for LPDDR4. Please ensure SW enables and configures the Command Bus Training.

1.1.1.1. i.MX 8M Nano LPDDR4-3200 routing recommendations

LPDDR4-3200 needs to be routed with signal fly times matched shown in **Table 1**. The delay of the via transitions needs to be included in the overall calculation. This can be realized in Allegro tool by enabling the **Z Axis Delay** in “Setup - Constraints - Modes”.

An example of the delay match calculation has been shown for the i.MX 8M Nano EVK board design in **Table 2** and **Table 3**. This analysis was done for the LPDDR4-3200 implementation using the i.MX 8M Nano. In **Table 2** and **Table 3**, the **PCB Delay** column was obtained directly from the Allegro PCB file, and the **Pkg Delay** column is the package delay obtained from Error! Reference source not found..

NXP recommends that users simulate their LPDDR4 implementation before fabricating PCBs.

Table 1. i.MX 8M Nano LPDDR4-3200 routing recommendations

LPDDR4-3200				
LPDDR4 signal (each 16-bit channel)	**Group**	**PCB + package prop delay**		
		Min	**Max**	**Considerations**
CK_t/CK_c	Clock	Short as possible	200 ps	Match the true/complement signals within 1 ps.
CA5, CA4	Address/ Command/ Control	CK_t - 50 ps	CK_t + 50 ps	Match CA5, CA4 within 2.0ps
CA3, CA2, CA1, CA0				Match CA3, CA2, CA1, CA0 within 2.0ps
CKE1, CKE0, CS1, CS0				Match CKE1, CKE0, CS1, CS0 within 2.0ps
DQS0_t/DQS0_c	Byte 0 - DQS	CK_t - 75 ps	CK_t + 75 ps	Match the true/complement signals of each DQS within 1 ps.
DM0	Byte 0 - Data	DQS0_t -50 ps	DQS0_t +50 ps	
DQ[7:0]				
DQS1_t/DQS1_c	Byte 1 - DQS	CK_t - 75 ps	CK_t + 75 ps	
DM1	Byte 1 - Data	DQS1_t -50 ps	DQS1_t +50 ps	
DQ[15:8]				

Table 2. LPDDR4 delay matching example (CA/CTL signals)

Net name	PCB delay (ps)	Pkg delay (ps)	Comments
DRAM_CK_T_A	99	41.1	Vias are L1-> L6->L1
	140.1		Total Net Delay
DRAM_CK_C_A	98.5	41.2	Vias are L1-> L6->L1
	139.7		Total Net Delay
DRAM_CA0_A	134.2	39.6	Vias are L1-> L3->L1
	173.8		Total Net Delay
DRAM_CA1_A	144.9	29.1	Vias are L1-> L3->L1
	174		Total Net Delay
DRAM_CA2_A	119.6	54.8	Vias are L1-> L6->L1
	174.4		Total Net Delay
DRAM_CA3_A	114	59.7	Vias are L1-> L6->L1
	173.7		Total Net Delay
DRAM_CA4_A	75.5	33.8	Vias are L1-> L3->L1
	109.3		Total Net Delay
DRAM_CA5_A	78.2	32.0	Vias are L1-> L3->L1
	110.2		Total Net Delay

Table 2. LPDDR4 delay matching example (CA/CTL signals)

Net name	PCB delay (ps)	Pkg delay (ps)	Comments
DRAM_nCS0_A	142.8	35.9	Vias are L1-> L3->L1
	178.7		Total Net Delay
DRAM_nCS1_A	134	44.2	Vias are L1-> L3->L1
	178.2		Total Net Delay
DRAM_CKE0_A	127	51.2	Vias are L1-> L3->L1
	178.2		Total Net Delay
DRAM_CKE1_A	138.9	39.9	Vias are L1-> L3->L1
	178.8		Total Net Delay

Table 3. LPDDR4 length matching example (Byte0/Byte1 signals)

Net name	PCB delay (ps)	Pkg delay (ps)	Comments
DRAM_SDQS0_T	122.6	59.0	Routed on bottom layer, no via
	181.6		Total Net Delay
DRAM_SDQS0_C	123.2	58.9	Routed on bottom layer, no via
	182.1		Total Net Delay
DRAM_DMI0	135.9	57.2	Vias are L1-> L3->L1
	193.1		Total Net Delay
DRAM_DQ00	142.2	47.2	Vias are L1-> L3->L1
	189.4		Total Net Delay
DRAM_DQ01	143.8	43.0	Vias are L1-> L3->L1
	186.8		Total Net Delay
DRAM_DQ02	126.8	54.6	Vias are L1-> L3->L1
	181.4		Total Net Delay
DRAM_DQ03	118.7	51.7	Vias are L1-> L3->L1
	170.4		Total Net Delay
DRAM_DQ04	112.7	59.9	Vias are L1-> L3->L1
	172.6		Total Net Delay
DRAM_DQ05	114.8	58.1	Vias are L1-> L3->L1
	172.9		Total Net Delay
DRAM_DQ06	114	64.6	Vias are L1-> L3->L1
	178.6		Total Net Delay
DRAM_DQ07	126.6	51.4	Vias are L1-> L3->L1
	178		Total Net Delay
DRAM_SDQS1_T	83.5	48.6	Routed on bottom layer, no via
	132.1		Total Net Delay
DRAM_SDQS1_C	84.2	47.2	Routed on bottom layer, no via
	131.4		Total Net Delay
DRAM_DMI1	56.8	58.6	Routed on top layer, no via
	115.4		Total Net Delay

Table 3. LPDDR4 length matching example (Byte0/Byte1 signals)

Net name	PCB delay (ps)	Pkg delay (ps)	Comments
DRAM_DQ008	56.1	45.0	Routed on top layer, no via
	101.1		Total Net Delay
DRAM_DQ09	53.5	50.1	Routed on top layer, no via
	103.6		Total Net Delay
DRAM_DQ10	55.8	46.2	Routed on top layer, no via
	103		Total Net Delay
DRAM_DQ11	52.3	47.2	Routed on top layer, no via
	99.5		Total Net Delay
DRAM_DQ12	50	40.3	Routed on top layer, no via
	90.3		Total Net Delay
DRAM_DQ13	71.5	48.8	Routed on top layer, no via
	120.3		Total Net Delay
DRAM_DQ14	67.3	58.4	Routed on top layer, no via
	125.7		Total Net Delay
DRAM_DQ15	78.2	52.4	Routed on top layer, no via
	130.6		Total Net Delay

1.1.1.2. LPDDR4-3200 routing example (i.MX 8M Nano)

Figure 2 to **Figure 2** show the placement and routing of the LPDDR4 signals on the i.MX 8M Nano EVK board. The CLK and DQS signals are routed on bottom layer to save routing space on top layer and layer 3. Data byte lane 1 signals are routed on top layer, and data byte lane 0 and CA/CTL signals are routed on layer 3. This is to make the signal actually travels on the via as short as possible to minimize via crosstalk.

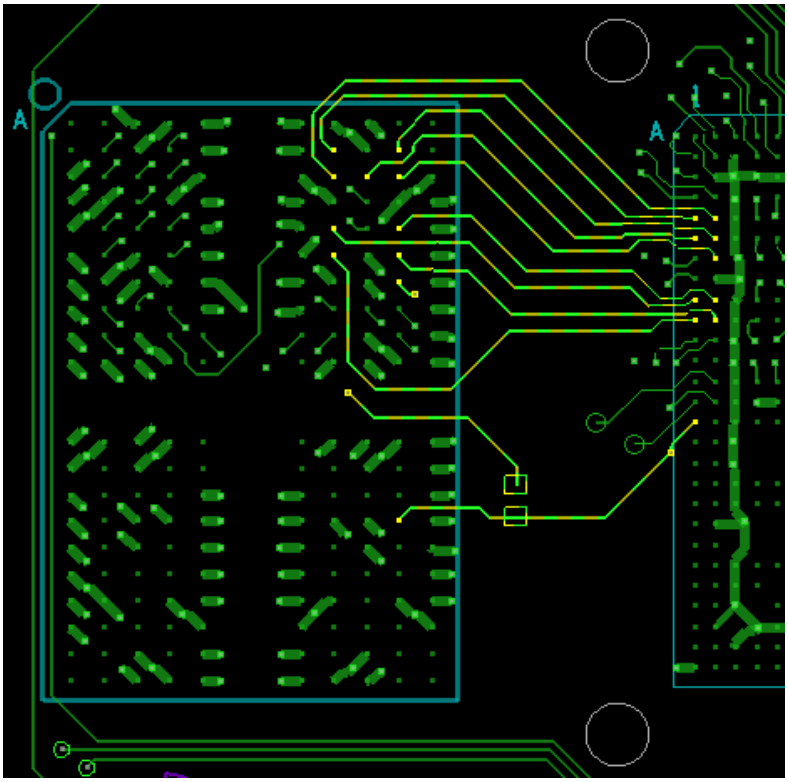

Figure 2. i.MX 8M Mini EVK board LPDDR4 routing (Top Layer)

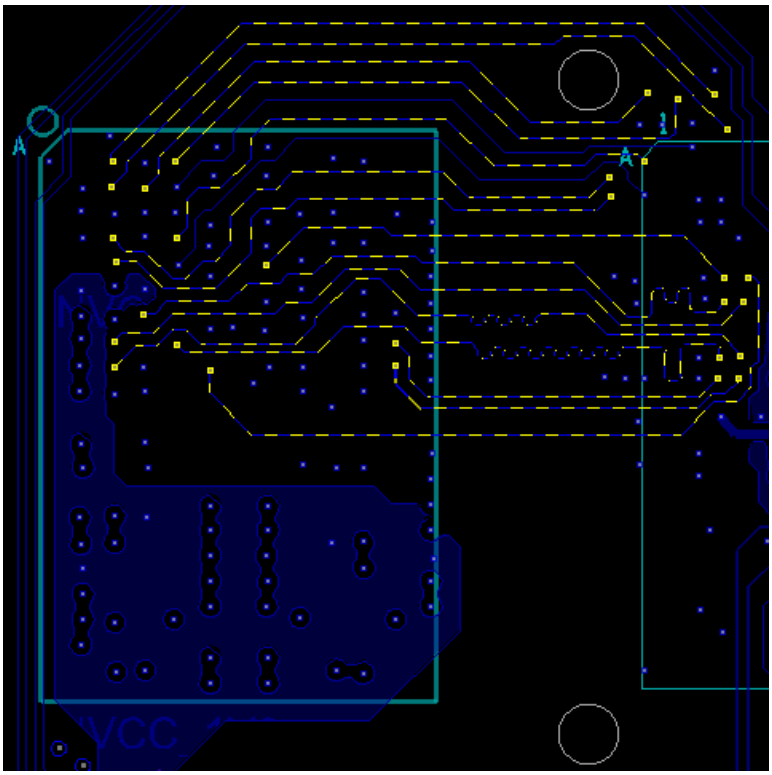

Figure 3. i.MX 8M Mini EVK board LPDDR4 routing (Layer 3)

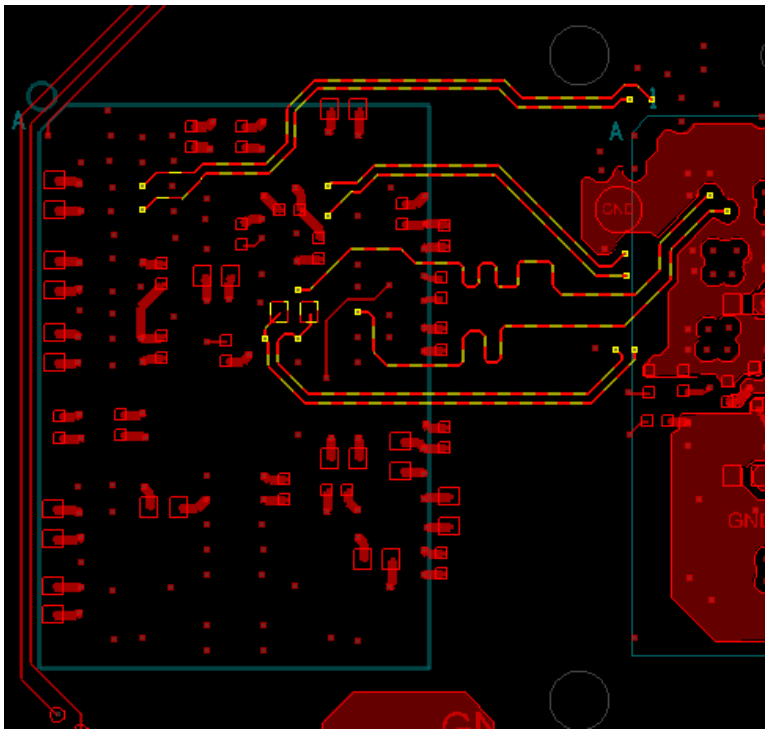

Figure 4. i.MX 8M Mini EVK board LPDDR4 routing (Bottom Layer)