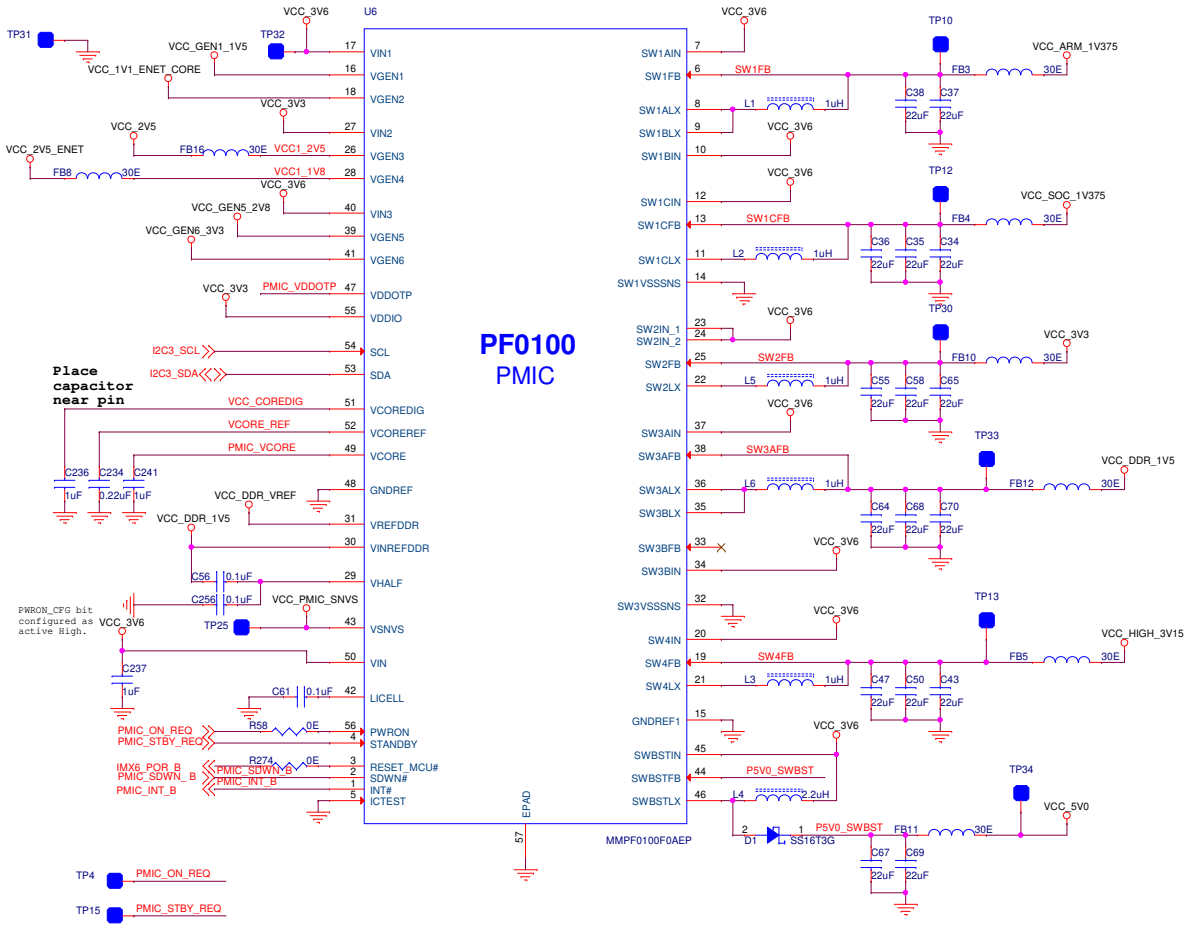
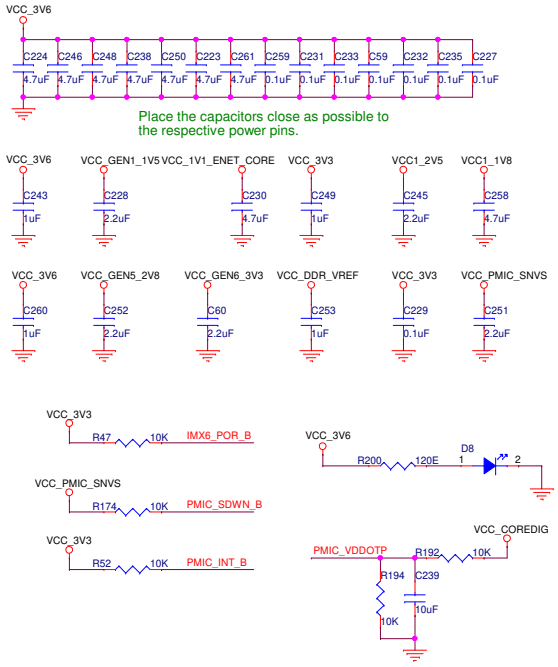
PMIC Section





Layout Guidelines

1). SW1VSSSNS (pin 14), GNDREF1 (pin 15), SW3VSSSNS (pin 32), and GNDREF (pin 48) are signal ground. These should not be connected to exposed pad . Connect these through seprate via to gnd plane.

2) Exposed pad is ground return for all the switching and should be connected to the GND planes through multiple via

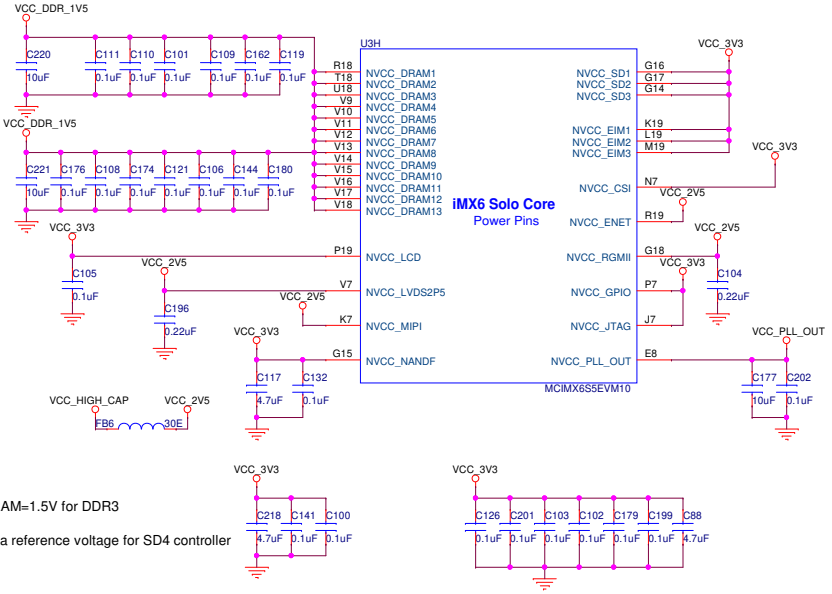
3) Use minimum 16 via under EP. Use via without thermal releif

4) Use array of opening in stencil

5) Refer to AN4622

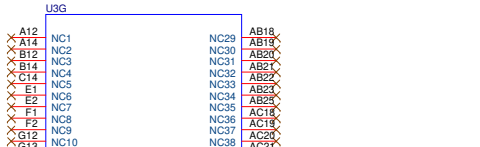
6) Refer to assembly guidelines Application notes

POWER CORE 1

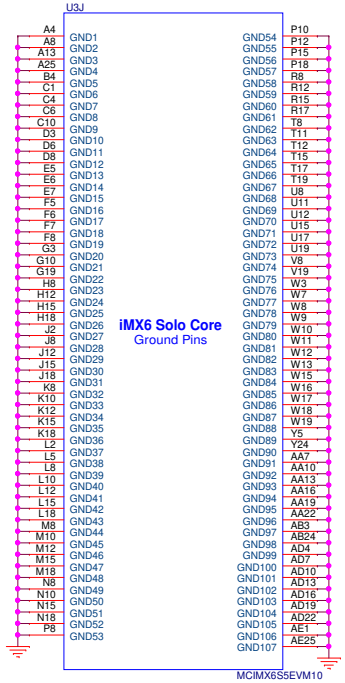


NOTE: NVCC_DRAM=1.5V for DDR3

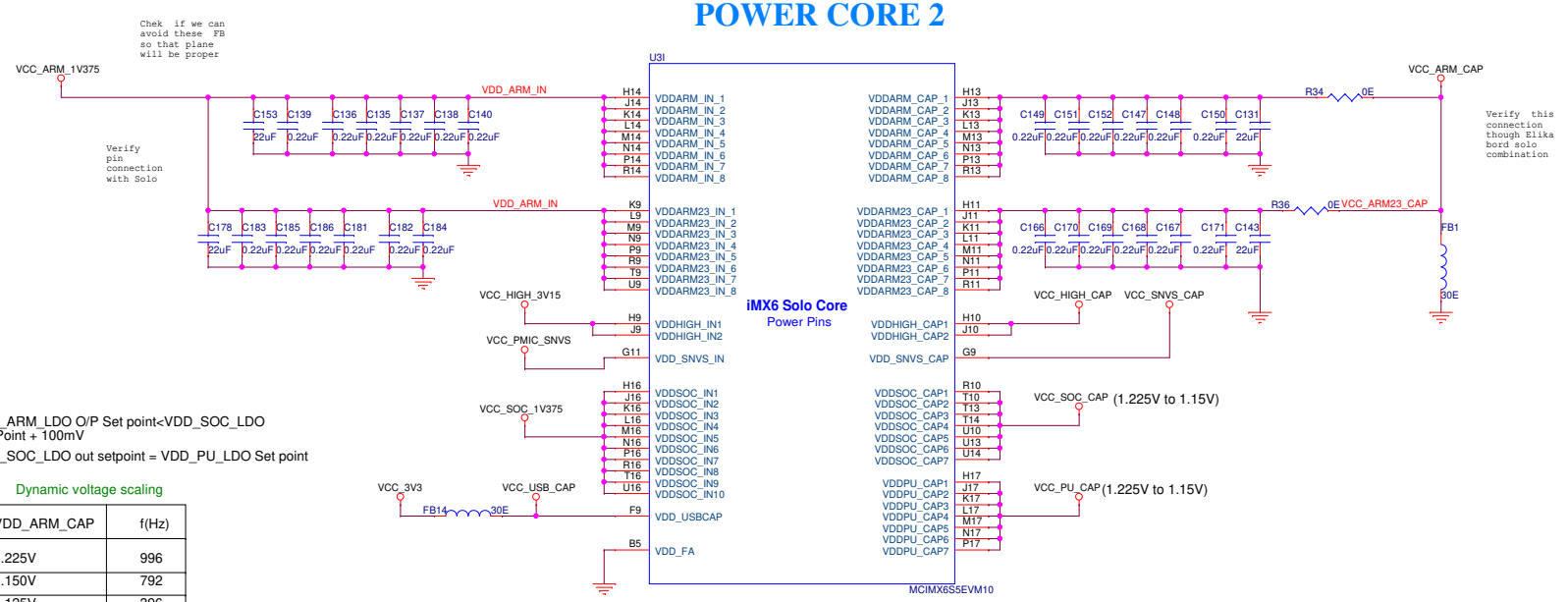
NVCC_NANDF is a reference voltage for SD4 controller



iMAX NC Section



POWER CORE 2



NOTE:

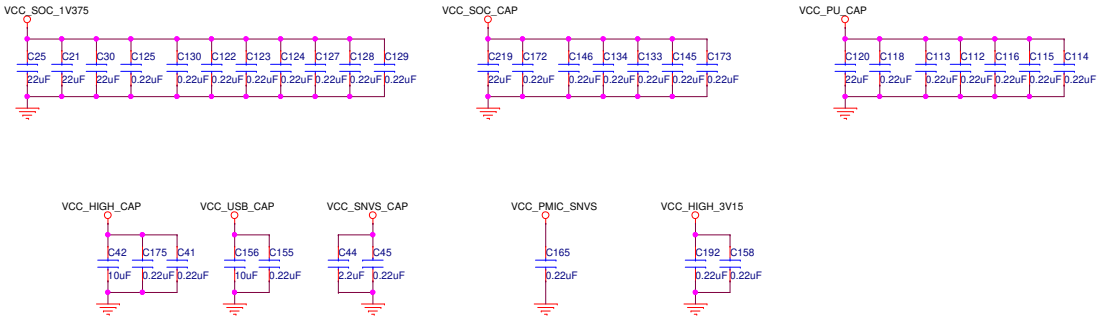
VDD_ARM_LDO O/P Set point<VDD_SOC_LDO Set Point + 100mV

VDD_SOC_LDO out setpoint = VDD_PU_LDO Set point

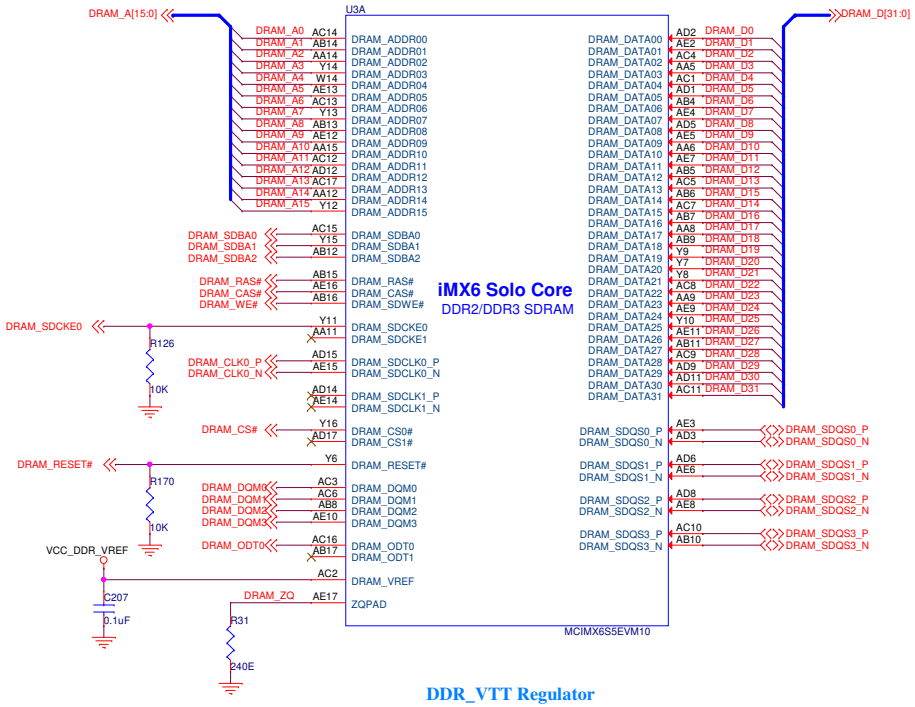
Dynamic voltage scaling

VDD_ARM_CAP	f(Hz)
1.225V	996
1.150V	792
1.125V	396

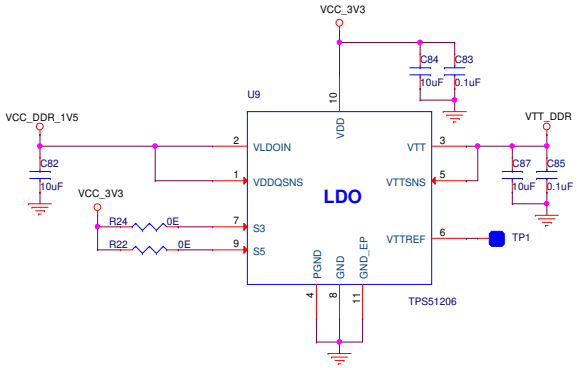
Decoupling Capacitor



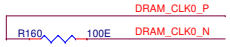
I.MX6 DDR CONTROLLER



DDR_VTT Regulator

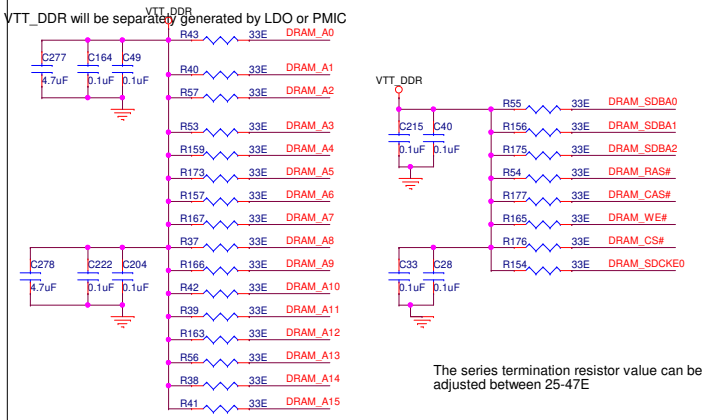


DDR CLK TERMINATION



ADDRESS AND CONTROL LINES TERMINATION

VTT_DDR will be separately generated by LDO or PMIC

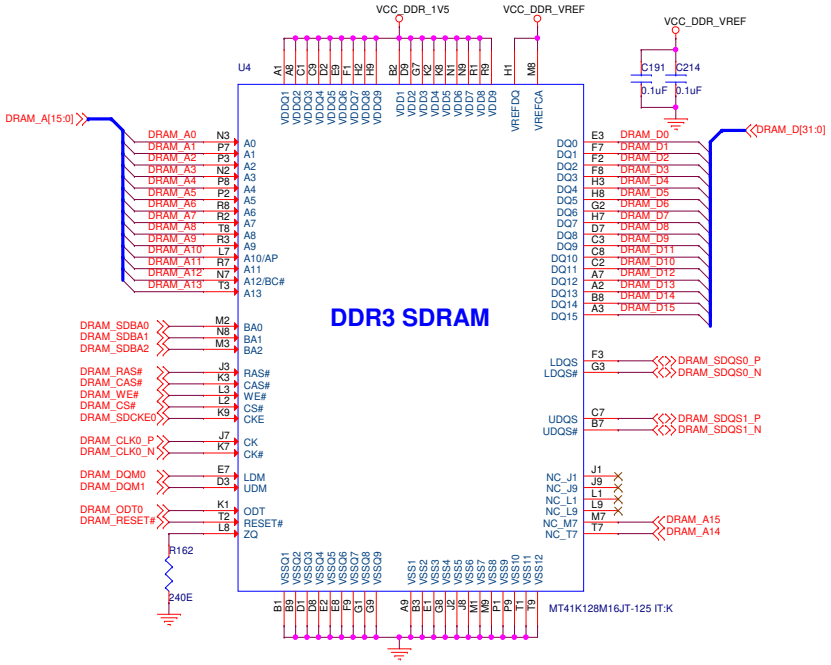


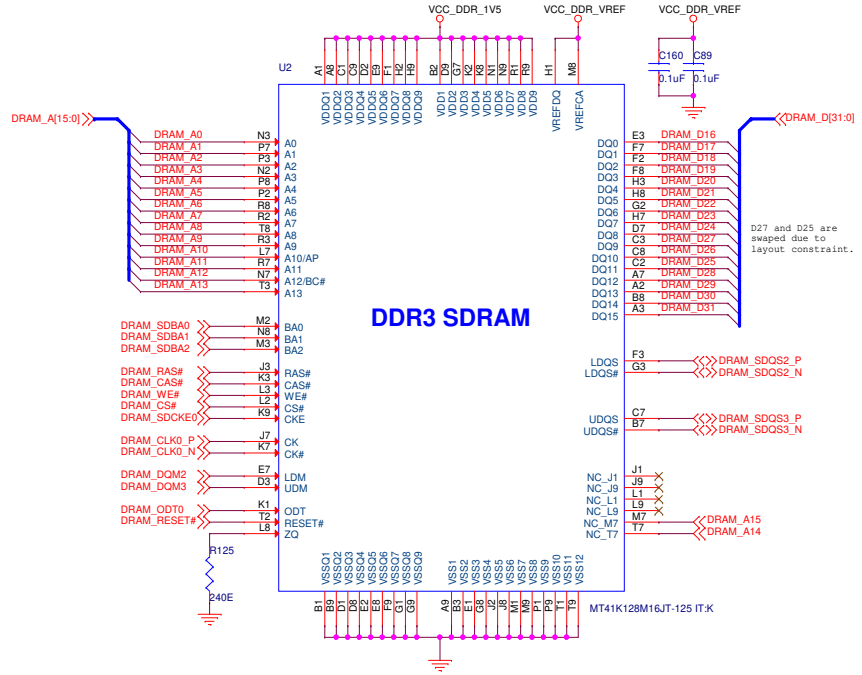
The series termination resistor value can be adjusted between 25-47E

Layout Guidelines

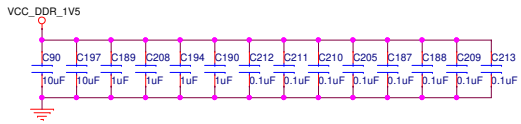
1. Place the DDR decoupling cap near to IC power pin.
2. Place the VTT generator as close to termination resistors as possible to minimize impedance.
3. For DDR data lane swapping Lowest order bit within byte lane ie D0, D8, D16, D24 must not be swapped. Other datalines are free to swap.
4. The max. trace length for DDR Clock signal should be within 3 inches
5. Match the trace length of other DDR signals w.r.t. Clock within +/- 25 mils

DDR3 SDRAM 1-2

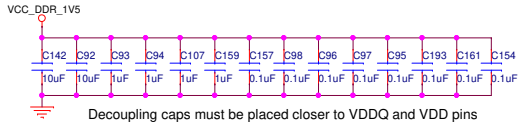




Decoupling Caps



Decoupling caps must be placed closer to VDDQ and VDD pins



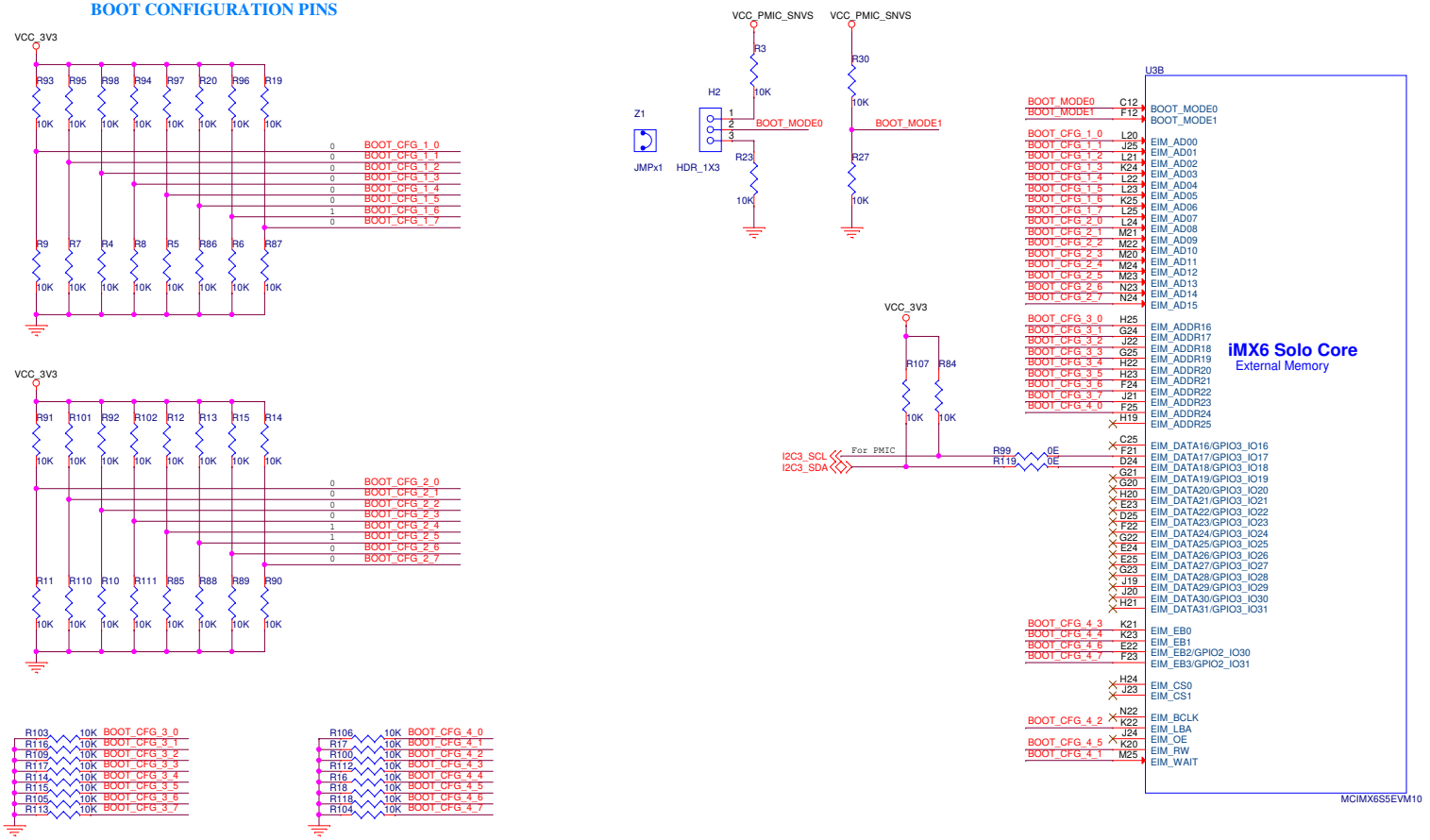
Decoupling caps must be placed closer to VDDQ and VDD pins

Layout Guidelines

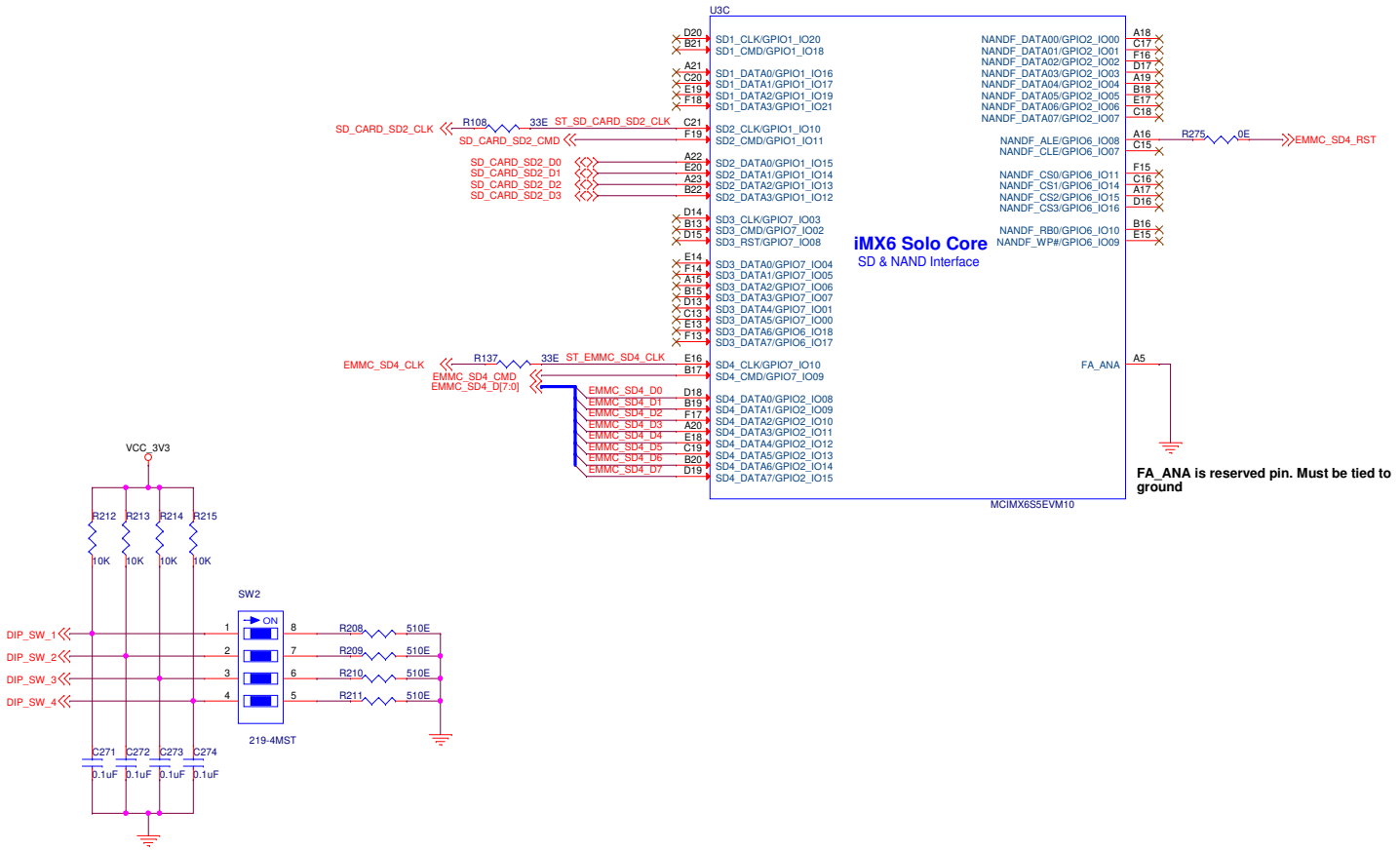
1)Make sure VTT is not connected to Vref
2) Make different plane of VTT and Vref
3)Try to put Vref and VTT on different plane , or try to isolate two by 40 /60 mil

I.MX6 BOOT CONFIGURATION

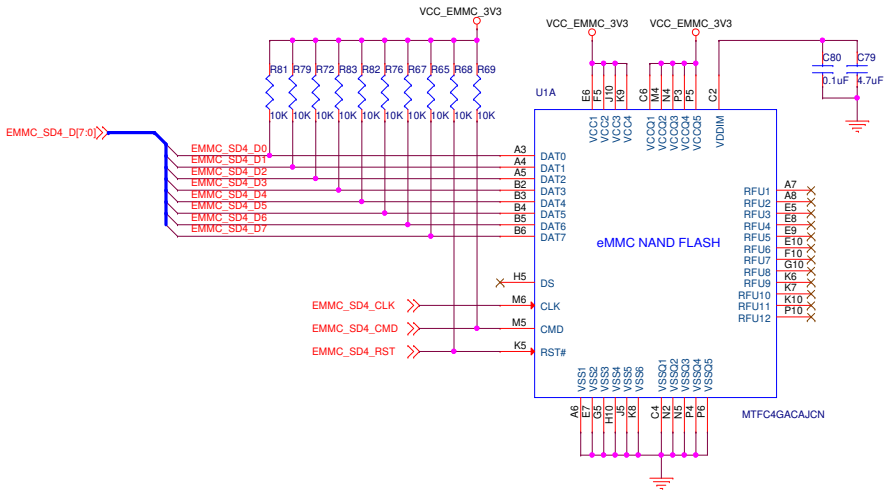
BOOT CONFIGURATION PINS

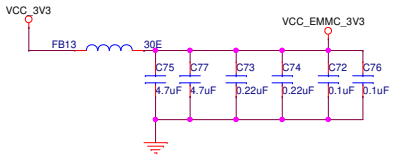


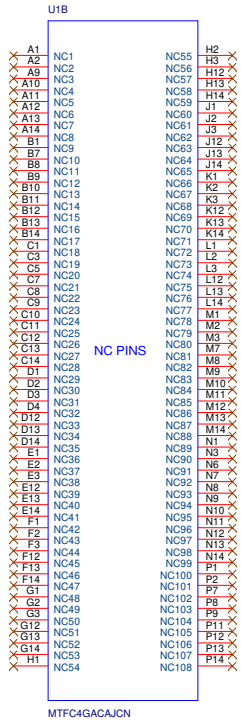
I.MX6 SDCARD AND EMMC



eMMC INTERFACE







Layout Guidelines

1. eMMC 5.0 spec compatibility
2. Coupling capacitor must be connected to VDD and VSS as close as possible.

I.MX6 USB AND JTAG