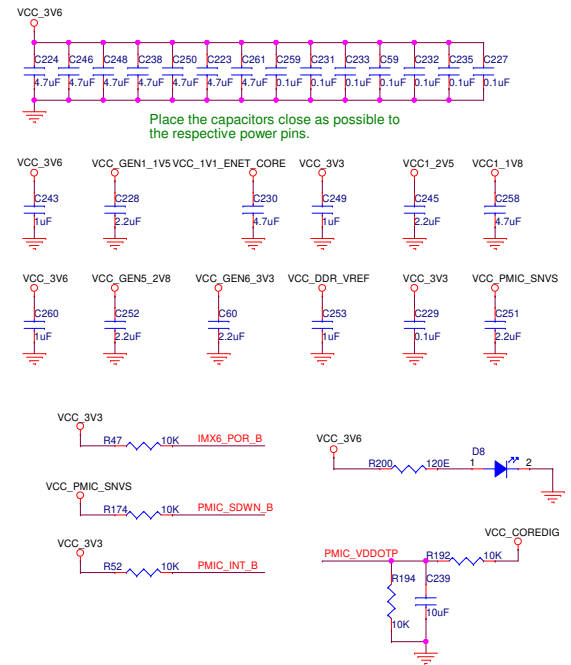
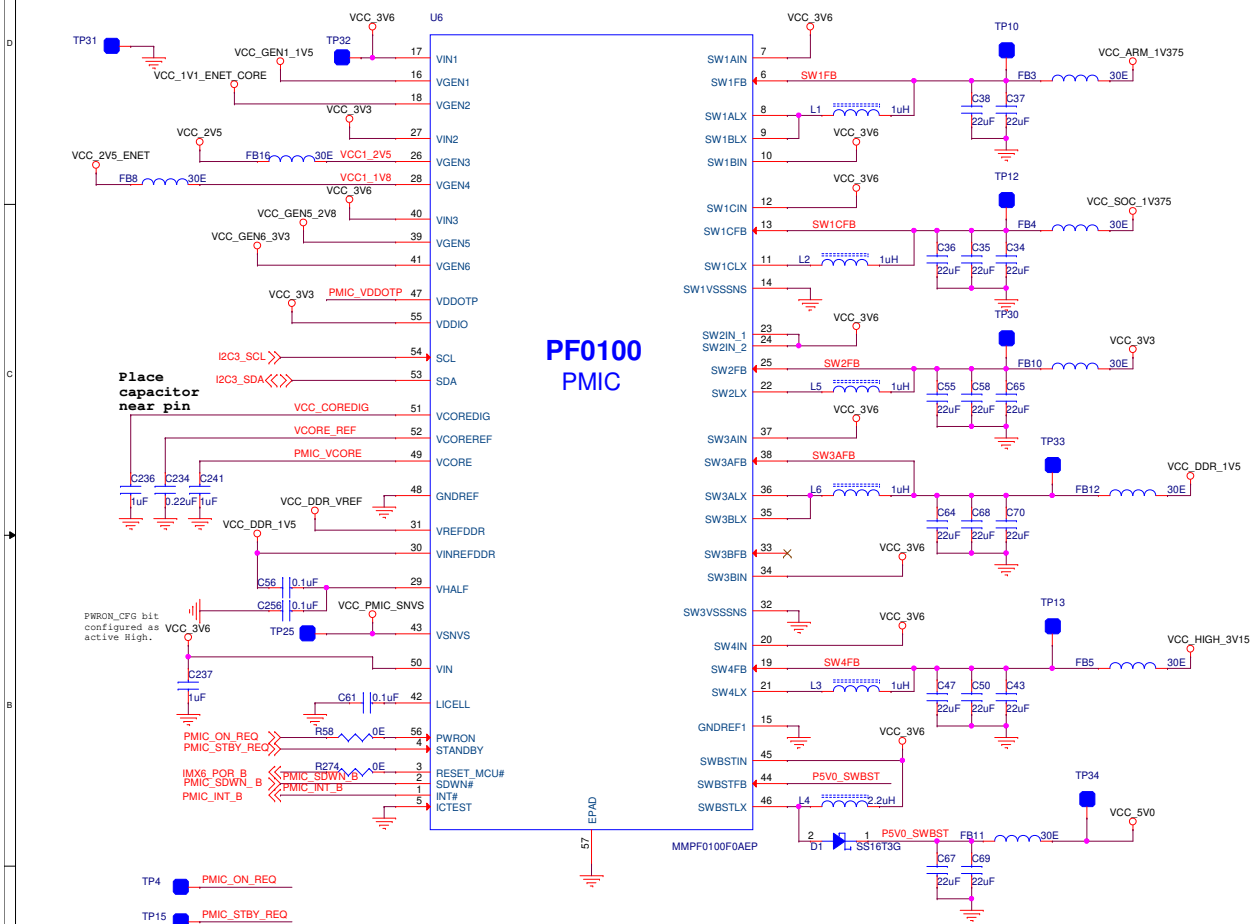


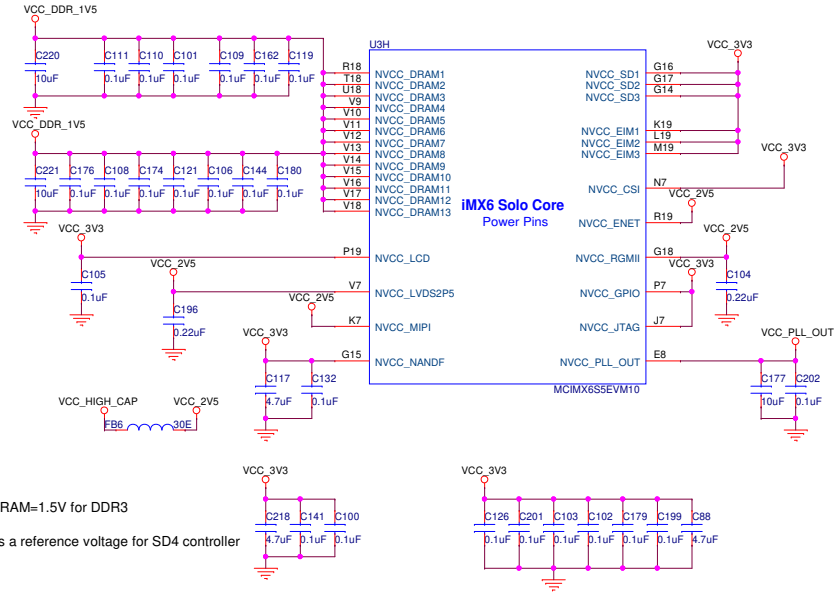
PMIC Section



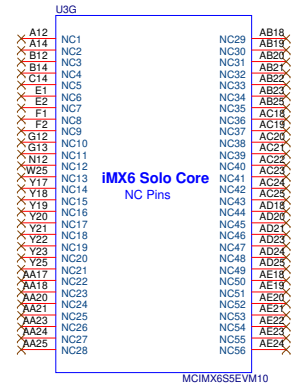
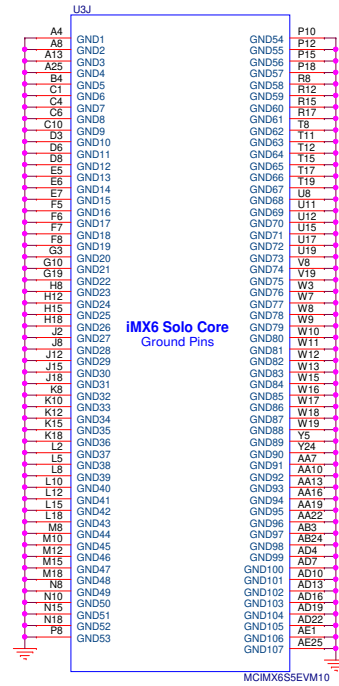
Layout Guidelines

- 1). SW1VSSNS (pin 14), GNDREF1 (pin 15), SW3VSSNS (pin 32), and GNDREF (pin 48) are signal ground. These should not be connected to exposed pad. Connect these through separate via to gnd plane.
- 2) Exposed pad is ground return for all the switching and should be connected to the GND planes through multiple via
- 3) Use minimum 16 via under EP. Use via without thermal relief
- 4) Use array of opening in stencil
- 5) Refer to AN4622
- 6) Refer to assembly guidelines Application notes

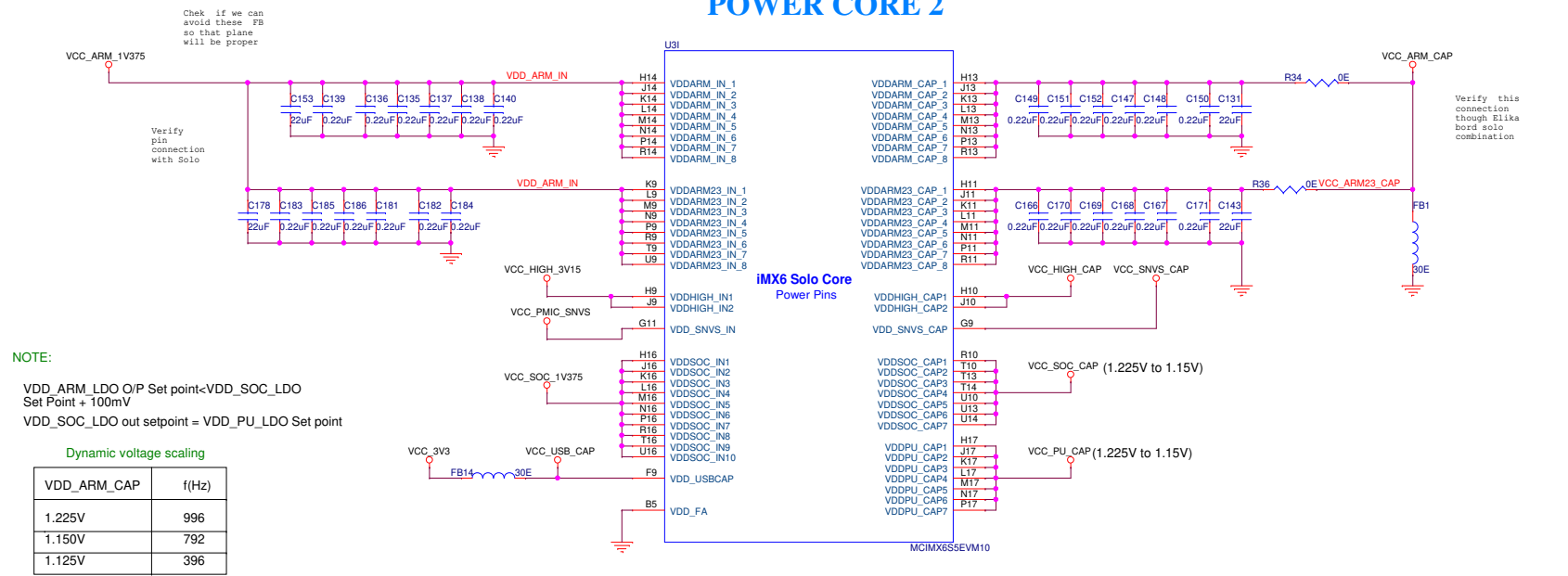
POWER CORE 1



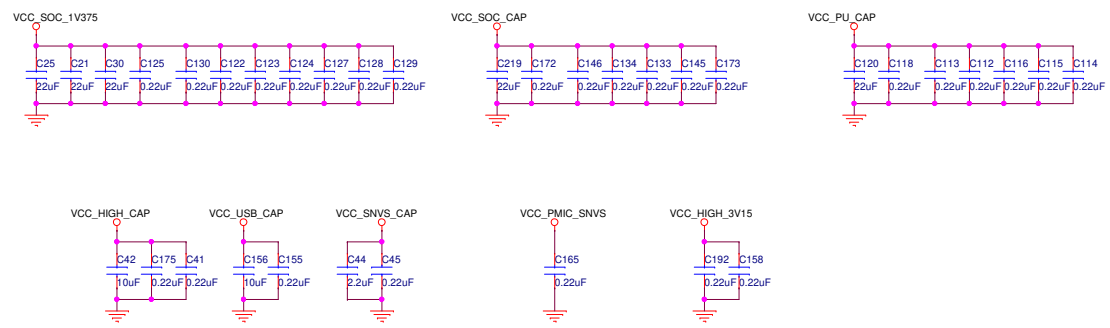
iMx6 NC Section



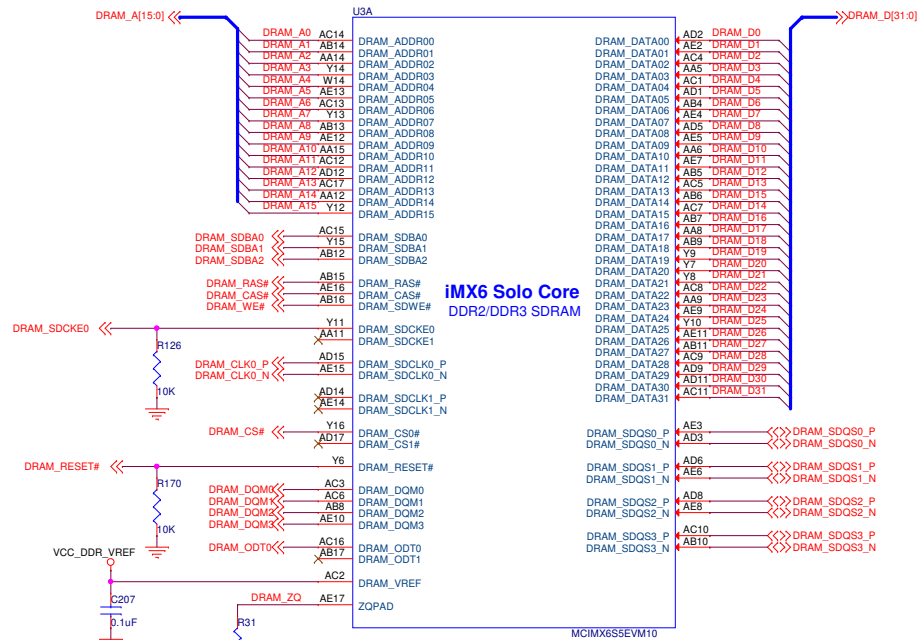
POWER CORE 2



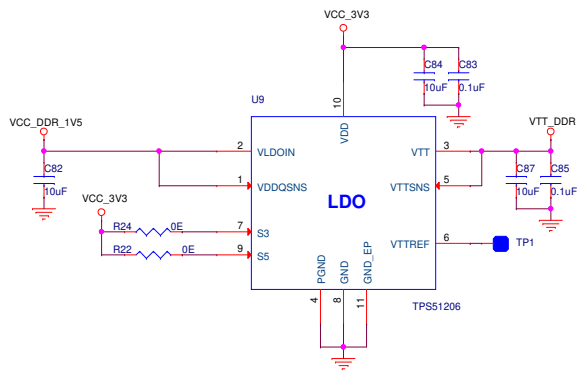
Decoupling Capacitor



IMX6 DDR CONTROLLER



DDR_VTT Regulator

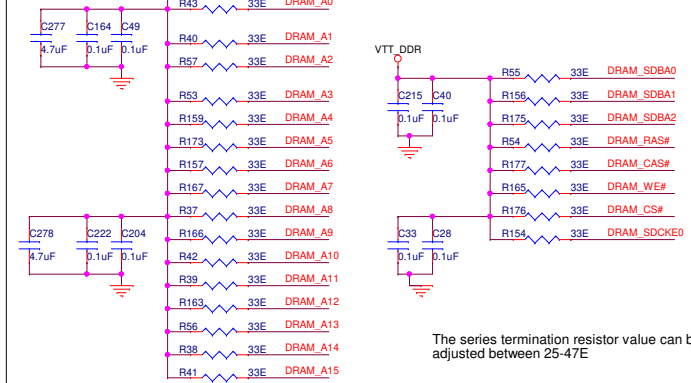


DDR CLK TERMINATION



ADDRESS AND CONTROL LINES TERMINATION

VTT_DDR will be separately generated by LDO or PMIC

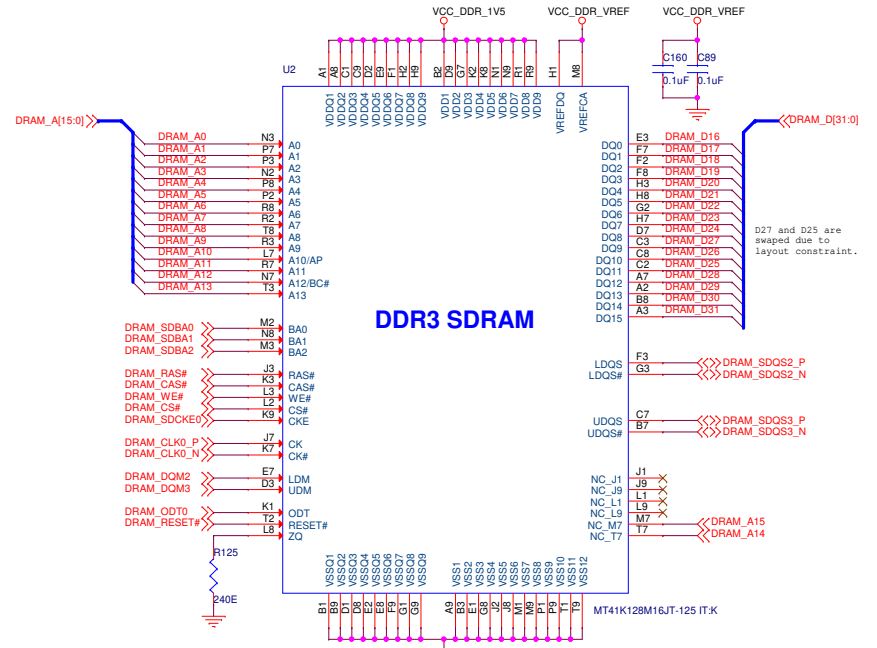
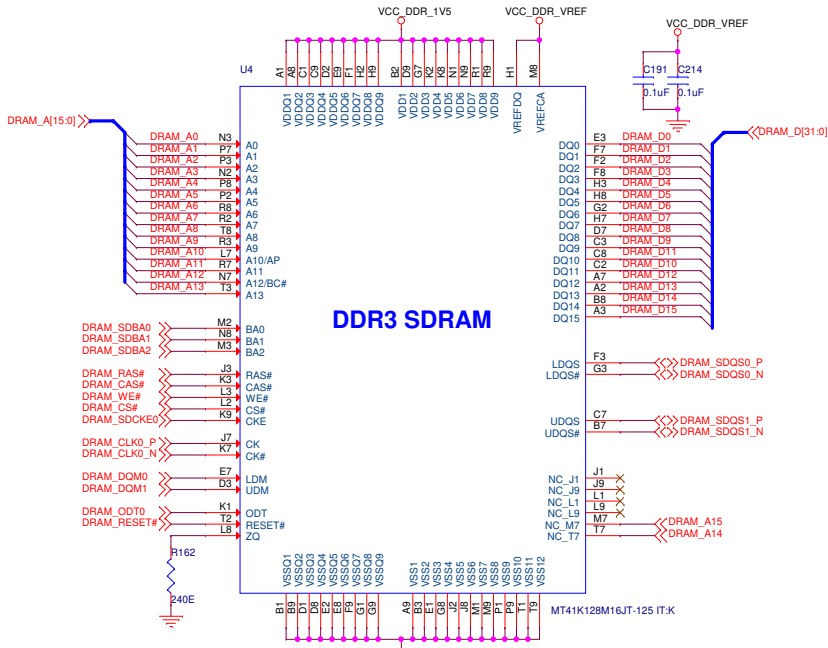


The series termination resistor value can be adjusted between 25-47E

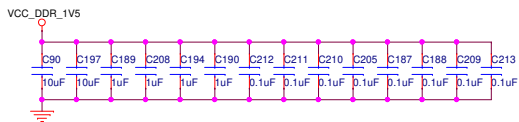
Layout Guidelines

1. Place the DDR decoupling cap near to IC power pin.
2. Place the VTT generator as close to termination resistors as possible to minimize impedance.
3. For DDR data lane swapping Lowest order bit within byte lane ie D0, D8, D16, D24 must not be swapped. Other datalines are free to swap.
4. The max. trace length for DDR Clock signal should be within 3 inches
5. Match the trace length of other DDR signals w.r.t. Clock within +/- 25 mils

DDR3 SDRAM 1-2



Decoupling Caps



Decoupling caps must be placed closer to VDDQ and VDD pins



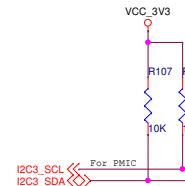
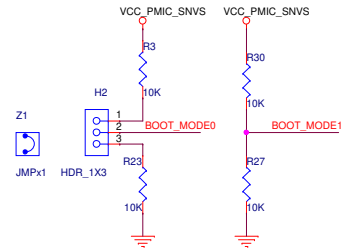
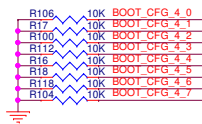
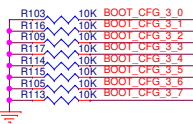
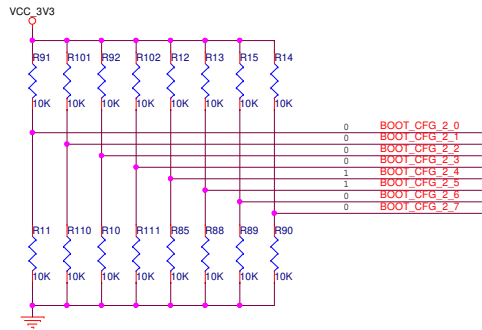
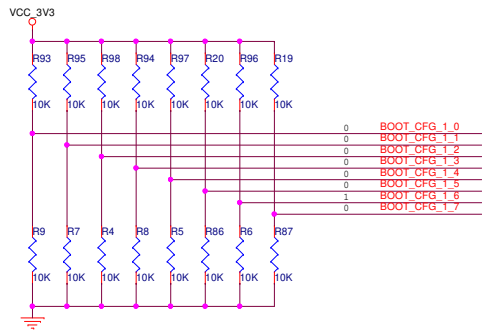
Decoupling caps must be placed closer to VDDQ and VDD pins

Layout Guidelines

- 1) Make sure VTT is not connected to Vref
- 2) Make different plane of VTT and Vref
- 3) Try to put Vref and VTT on different plane, or try to isolate two by 40 / 60 mil

I.MX6 BOOT CONFIGURATION

BOOT CONFIGURATION PINS

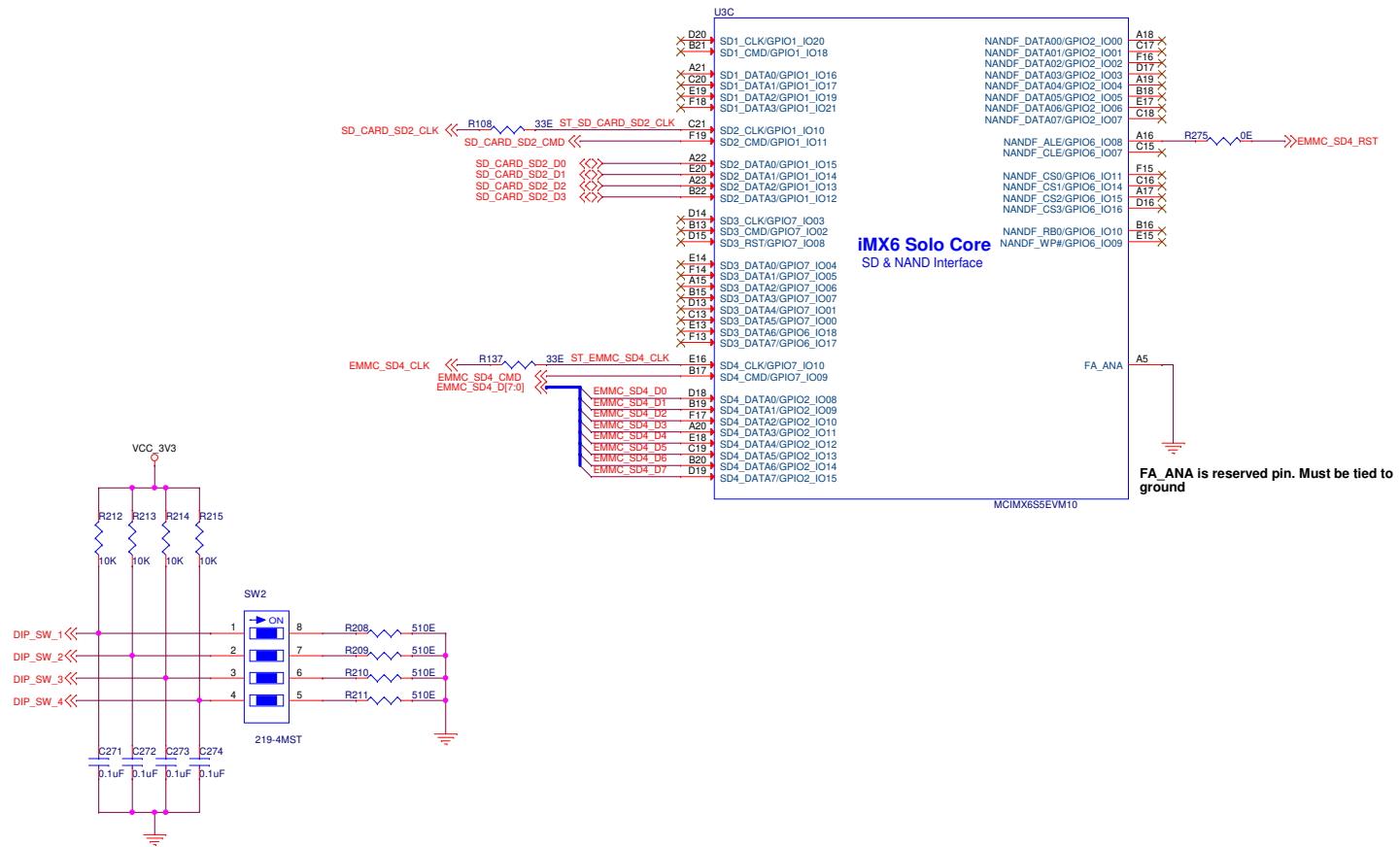


BOOT_MODE0	C12	BOOT_MODE0
BOOT_MODE1	F12	BOOT_MODE1
BOOT_CFG 1.0	L20	EIM_AD00
BOOT_CFG 1.1	J25	EIM_AD01
BOOT_CFG 1.2	L21	EIM_AD02
BOOT_CFG 1.3	K24	EIM_AD03
BOOT_CFG 1.4	L22	EIM_AD04
BOOT_CFG 1.5	L23	EIM_AD05
BOOT_CFG 1.6	K25	EIM_AD06
BOOT_CFG 1.7	L23	EIM_AD07
BOOT_CFG 2.0	L24	EIM_AD08
BOOT_CFG 2.1	M21	EIM_AD09
BOOT_CFG 2.2	M22	EIM_AD10
BOOT_CFG 2.3	M20	EIM_AD11
BOOT_CFG 2.4	M24	EIM_AD12
BOOT_CFG 2.5	M23	EIM_AD13
BOOT_CFG 2.6	N23	EIM_AD14
BOOT_CFG 2.7	N24	EIM_AD15
BOOT_CFG 3.0	H25	EIM_ADDR16
BOOT_CFG 3.1	G24	EIM_ADDR17
BOOT_CFG 3.2	J22	EIM_ADDR18
BOOT_CFG 3.3	G25	EIM_ADDR19
BOOT_CFG 3.4	H22	EIM_ADDR20
BOOT_CFG 3.5	H25	EIM_ADDR21
BOOT_CFG 3.6	F24	EIM_ADDR22
BOOT_CFG 3.7	J21	EIM_ADDR23
BOOT_CFG 4.0	F25	EIM_ADDR24
	H19	EIM_ADDR25
	C25	EIM_DATA16/GPIO3_IO16
	F21	EIM_DATA17/GPIO3_IO17
	D24	EIM_DATA18/GPIO3_IO18
	G21	EIM_DATA19/GPIO3_IO19
	G20	EIM_DATA20/GPIO3_IO20
	H20	EIM_DATA21/GPIO3_IO21
	E23	EIM_DATA22/GPIO3_IO22
	D25	EIM_DATA23/GPIO3_IO23
	F22	EIM_DATA24/GPIO3_IO24
	G22	EIM_DATA25/GPIO3_IO25
	E24	EIM_DATA26/GPIO3_IO26
	E25	EIM_DATA27/GPIO3_IO27
	G23	EIM_DATA28/GPIO3_IO28
	J18	EIM_DATA29/GPIO3_IO29
	J20	EIM_DATA30/GPIO3_IO30
	H21	EIM_DATA31/GPIO3_IO31
BOOT_CFG 4.3	K21	EIM_EB0
BOOT_CFG 4.4	K23	EIM_EB1
BOOT_CFG 4.6	E22	EIM_EB2/GPIO2_IO30
BOOT_CFG 4.7	F23	EIM_EB3/GPIO2_IO31
	H24	EIM_CS0
	J23	EIM_CS1
	N22	EIM_BCLK
BOOT_CFG 4.2	K22	EIM_LBA
	J24	EIM_LBA
BOOT_CFG 4.5	K20	EIM_RW
BOOT_CFG 4.1	M25	EIM_WAIT

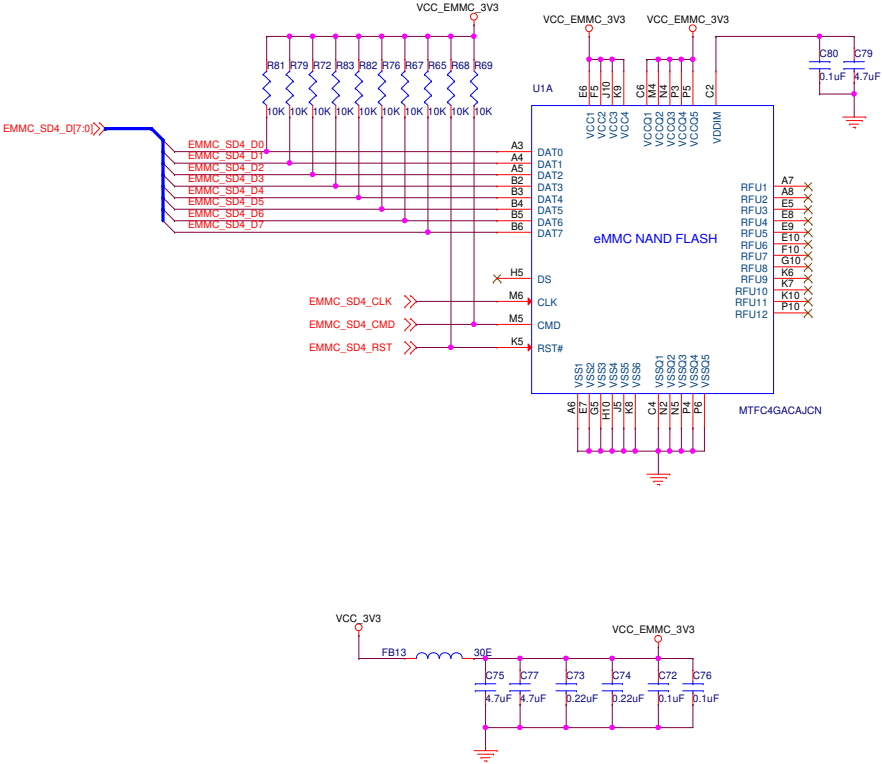
IMX6 Solo Core
External Memory

MCIMX6SSEVM10

I.MX6 SDCARD AND EMMC



eMMC INTERFACE



U1B

A1	NC1	NC55	H2
A2	NC2	NC56	H3
A3	NC3	NC57	H13
A10	NC4	NC58	H14
A11	NC5	NC59	J1
A12	NC6	NC60	J2
A13	NC7	NC61	J3
A14	NC8	NC62	J15
B1	NC9	NC63	J12
B7	NC10	NC64	J14
B8	NC11	NC65	K1
B9	NC12	NC66	K2
B10	NC13	NC67	K3
B11	NC14	NC68	K12
B12	NC15	NC69	K14
B13	NC16	NC70	K13
B14	NC17	NC71	L1
C1	NC18	NC72	L2
C3	NC19	NC73	L3
C5	NC20	NC74	L13
C8	NC21	NC75	L15
C9	NC22	NC76	L14
C10	NC23	NC77	M1
C11	NC24	NC78	M2
C12	NC25	NC79	M3
C13	NC26	NC80	M7
C14	NC27	NC81	M8
D1	NC28	NC82	M5
D2	NC29	NC83	M10
D3	NC30	NC84	M11
D4	NC31	NC85	M12
D12	NC32	NC86	M13
D13	NC33	NC87	M1
D14	NC34	NC88	M14
E1	NC35	NC89	N3
E2	NC36	NC90	N6
E3	NC37	NC91	N7
E12	NC38	NC92	N8
E13	NC39	NC93	N9
E14	NC40	NC94	N10
F1	NC41	NC95	N11
F2	NC42	NC96	N12
F3	NC43	NC97	N13
F12	NC44	NC98	N14
F13	NC45	NC99	P1
F14	NC46	NC100	P2
G1	NC47	NC101	P7
G2	NC48	NC102	P6
G3	NC49	NC103	P9
G12	NC50	NC104	P11
G13	NC51	NC105	P12
G14	NC52	NC106	P13
H1	NC53	NC107	P14
NC54	NC108		

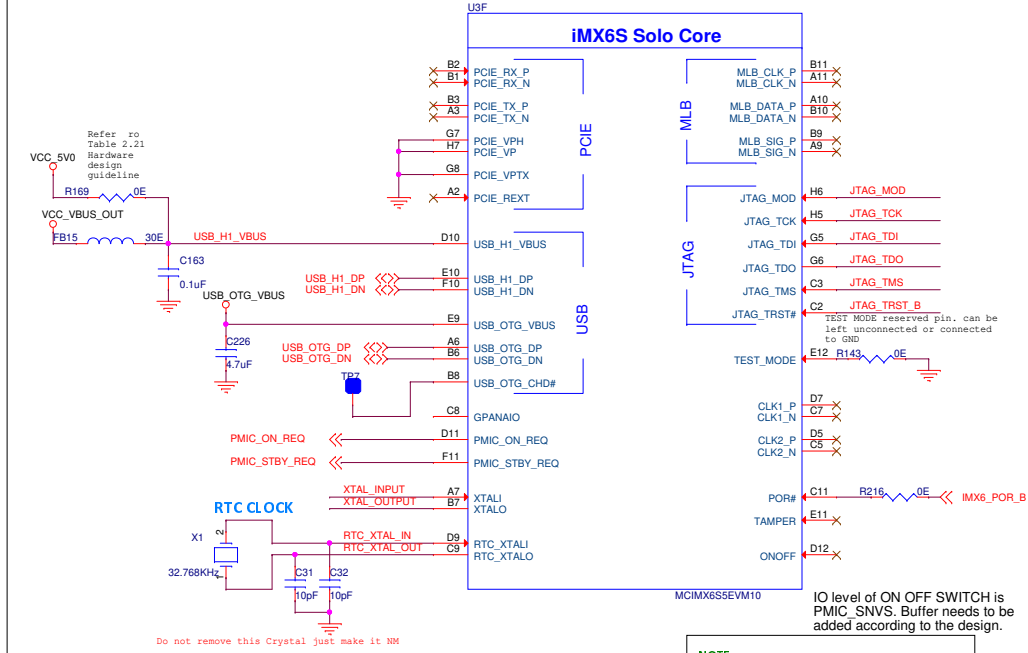
NC PINS

MTFC4GACAJCN

Layout Guidelines

1. eMMC 5.0 spec compatibility
2. Coupling capacitor must be connected to VDD and VSS as close as possible.

I.MX6 USB AND JTAG



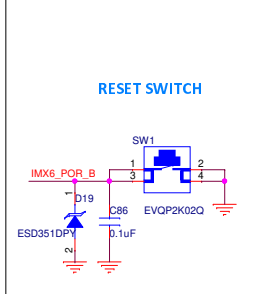
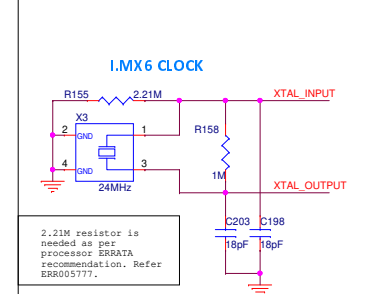
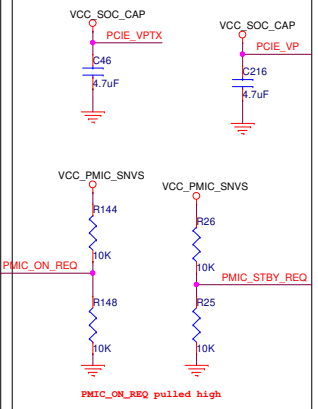
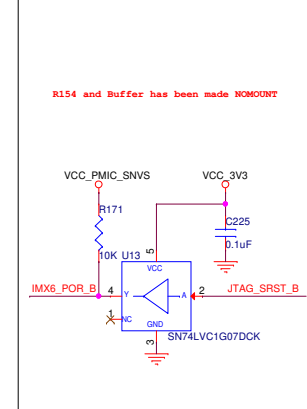
The Logic level of clock signal on XTALI pin should be as follows

- Low Logic == 0.0 -0.2V
- High Logic == 0.8V* NVCC_PLL_OUT- NVCC_PLL_OUT

Typical NVCC_PLL_OUT=1.1V

If RTC_XTALI is tied to GND and RTC_XTALO is left unconnected, the on-chip oscillator is automatically engaged

NOTE:
POR duration will be controlled by PMIC



Need to check How XTALI has to be biased to GND

