



LPDDR4 SDRAM

MT53B384M32D2, MT53B768M32D4

Features

- Ultra-low-voltage core and I/O power supplies
 - $V_{DD1} = 1.70\text{--}1.95\text{V}$; 1.8V nominal
 - $V_{DD2}/V_{DDQ} = 1.06\text{--}1.17\text{V}$; 1.1V nominal
- Frequency range
 - 1866–10 MHz (data rate range: 3733–20 Mb/s/pin)
- 16n prefetch DDR architecture
- 1-channel partitioned architecture for low RD/WR energy and low average latency
- 8 internal banks per channel for concurrent operation
- Single-data-rate CMD/ADR entry
- Bidirectional/differential data strobe per byte lane
- Programmable READ and WRITE latencies (RL/WL)
- Programmable and on-the-fly burst lengths (BL = 16, 32)
- Directed per-bank refresh for concurrent bank operation and ease of command scheduling
- Up to 7.5 GB/s per die
- On-chip temperature sensor to control self refresh rate
- Partial-array self refresh (PASR)
- Selectable output drive strength (DS)
- Clock-stop capability
- RoHS-compliant, “green” packaging
- Programmable V_{SS} (ODT) termination

Options

- V_{DD1}/V_{DD2} : 1.8V/1.1V
- Array configuration
 - 384 Meg x 32 (2 channels x16 I/O) 384M32
 - 768 Meg x 32 (4 channels x16 I/O) 768M32
- Device configuration
 - 384M16 x 2 die in package D2
 - 384M16 x 4 die in package D4
- FBGA “green” package
 - 200-ball WFBGA (10mm x 14.5mm x 0.8mm, Ø0.28 SMD) NP
 - 200-ball VFBGA (10mm x 14.5mm x 0.95mm, Ø0.28 SMD) NQ
 - 200-ball WFBGA (10mm x 14.5mm x 0.8mm, Ø0.35 SMD) DS¹
 - 200-ball VFBGA (10mm x 14.5mm x 0.95mm, Ø0.35 SMD) DT¹
- Speed grade, cycle time
 - 625ps @ RL = 28/32 -062
 - 535ps @ RL = 32/36 -053
- Operating temperature range
 - -30°C to $+85^{\circ}\text{C}$ WT
 - -30°C to $+105^{\circ}\text{C}$ XT
- Revision :B

Note: 1. Preliminary status: Products and specifications discussed herein are for evaluation and reference purposes only and are subject to change by Micron without notice. Products are only warranted by Micron to meet Micron’s production data sheet specifications.

Table 1: Key Timing Parameters

| Speed Grade | Clock Rate (MHz) | Data Rate (Mb/s/pin) | WRITE Latency Set A | WRITE Latency Set B | READ Latency (DBI Disabled) | READ Latency (DBI Enabled) | Note |
|-------------|------------------|----------------------|---------------------|---------------------|-----------------------------|----------------------------|------|
| -053 | 1866 | 3733 | 16 | 30 | 32 | 36 | 1 |
| -062 | 1600 | 3200 | 14 | 26 | 28 | 32 | |

Note: 1. Contact factory



SDRAM Addressing

The table below shows the addressing for the 6Gb die density. All bank, row, and column addresses are shown per-die.

Table 2: Device Addressing

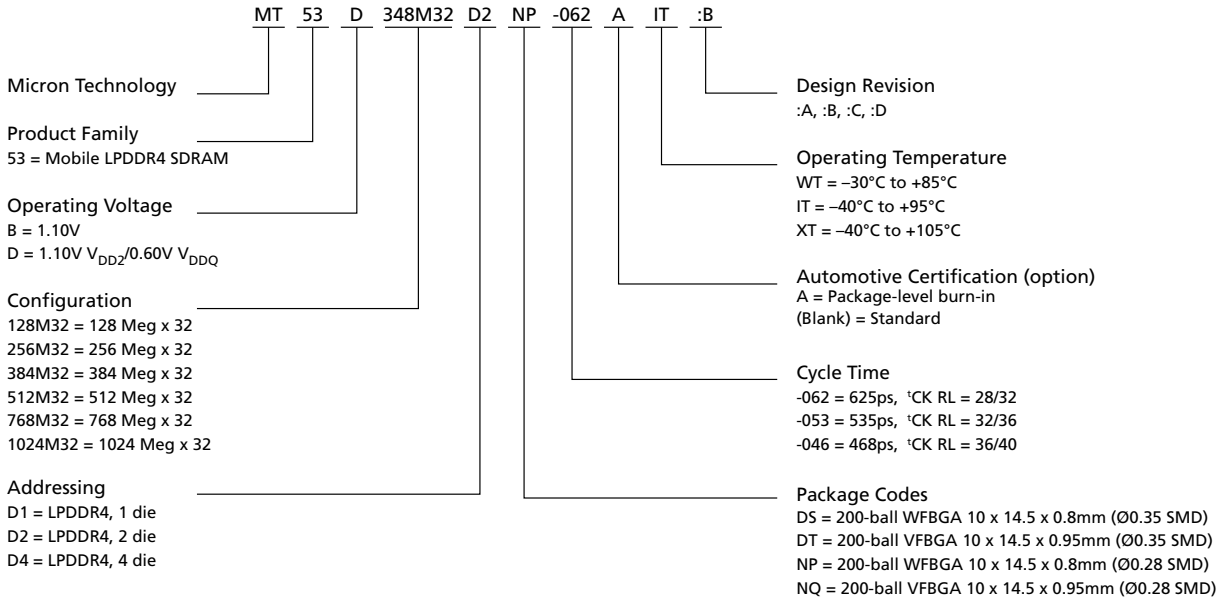
| Configuration | | 384M32 (12Gb) | 768M32 (24Gb) |
|--------------------------------------|------------------|--|--|
| Die per package | | 2 | 4 |
| Device density (per die) | | 6Gb | 6Gb |
| Device density (per channel) | | 6Gb | 6Gb |
| Configuration | | 48Mb × 16 DQ × 8 banks x 2 channels | 96Mb × 16 DQ × 8 banks x 2 channels |
| Number of channels (per die) | | 1 | 1 |
| Number of ranks per channel | | 1 | 2 |
| Number of banks (per channel) | | 8 | 8 |
| Array prefetch (bits) (per channel) | | 256 | 256 |
| Number of rows (per bank) | | 49,152 | 49,152 |
| Number of columns (fetch boundaries) | | 64 | 64 |
| Page size (bytes) | | 2048 | 2048 |
| Channel density (bits per channel) | | 6,442,450,944 | 6,442,450,944 |
| Total density (bits per die) | | 6,442,450,944 | 6,442,450,944 |
| Bank address | | BA[2:0] | BA[2:0] |
| ×16 | Row addresses | R[15:0] | R[15:0] |
| | Column addresses | C[9:0] | C[9:0] |
| Burst starting address boundary | | 64-bit | 64-bit |

- Notes:
1. The lower two column addresses (C0–C1) are assumed to be zero and are not transmitted on the CA bus.
 2. Row and column address values on the CA bus that are not used for a particular density are "Don't Care."
 3. For non-binary memory densities, only a quarter of the row address space is invalid. When the MSB address bit is HIGH, then the MSB - 1 address bit must be LOW.



Part Number Ordering Information

Figure 1: Part Number Chart



Note: 1. Not all options listed can be combined to define an offered product. Use the part catalog search on www.micron.com for available offerings.

FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. Micron's FBGA part marking decoder is available at www.micron.com/decoder.



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**200b: x32 LPDDR4 SDRAM
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Important Notes and Warnings

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General Description

The 6Gb Mobile Low-Power DDR4 SDRAM (LPDDR4) is a high-speed CMOS, dynamic random-access memory. The device is internally configured with x16 I/O, 8-banks.

Each of the x16's 805,306,368-bit banks is organized as 49,152 rows by 1024 columns by 16 bits.



General Notes

Throughout the data sheet, figures and text refer to DQs as “DQ.” DQ should be interpreted as any or all DQ collectively, unless specifically stated otherwise.

“DQS” and “CK” should be interpreted as DQS_t, DQS_c and CK_t, CK_c respectively, unless specifically stated otherwise. “CA” includes all CA pins used for a given density.

In timing diagrams, “CMD” is used as an indicator only. Actual signals occur on CA[5:0]. V_{REF} indicates $V_{REF(CA)}$ and $V_{REF(DQ)}$.

Complete functionality may be described throughout the entire document. Any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.

Any specific requirement takes precedence over a general statement.

Any functionality not specifically stated herein is considered undefined, illegal, is not supported, and will result in unknown operation.



Package Block Diagrams

Figure 2: Dual-Die, Dual-Channel, Single-Rank Package Block Diagram

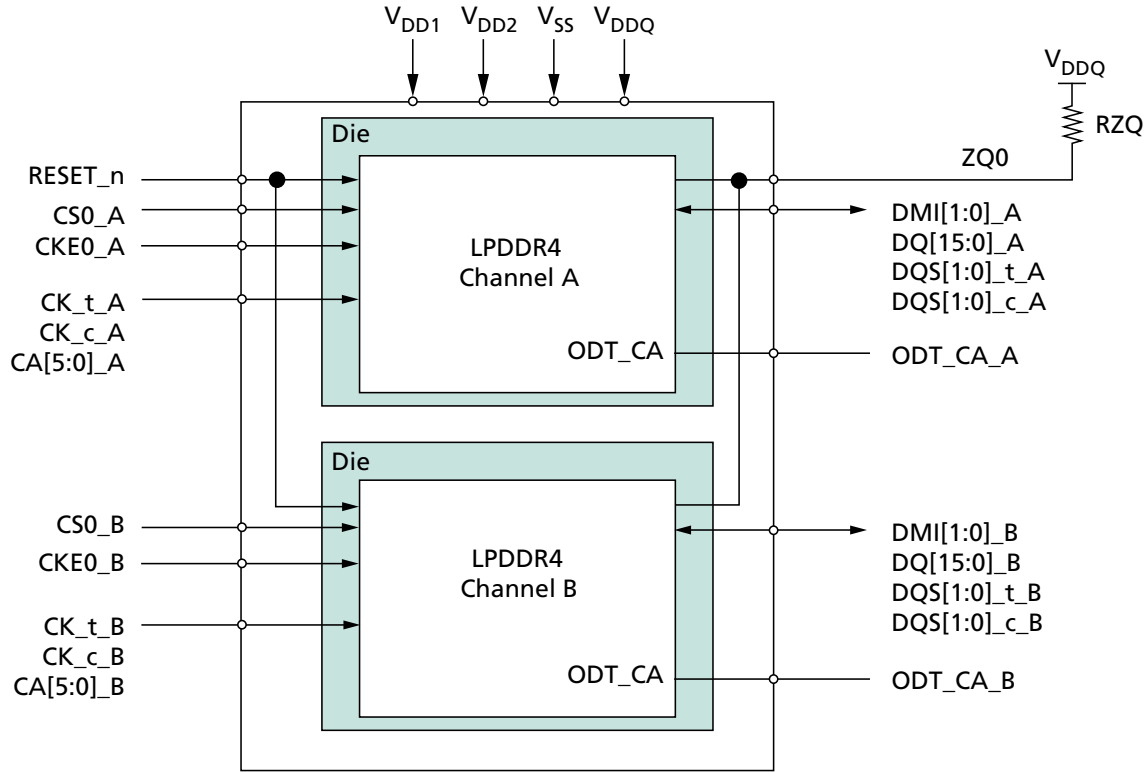
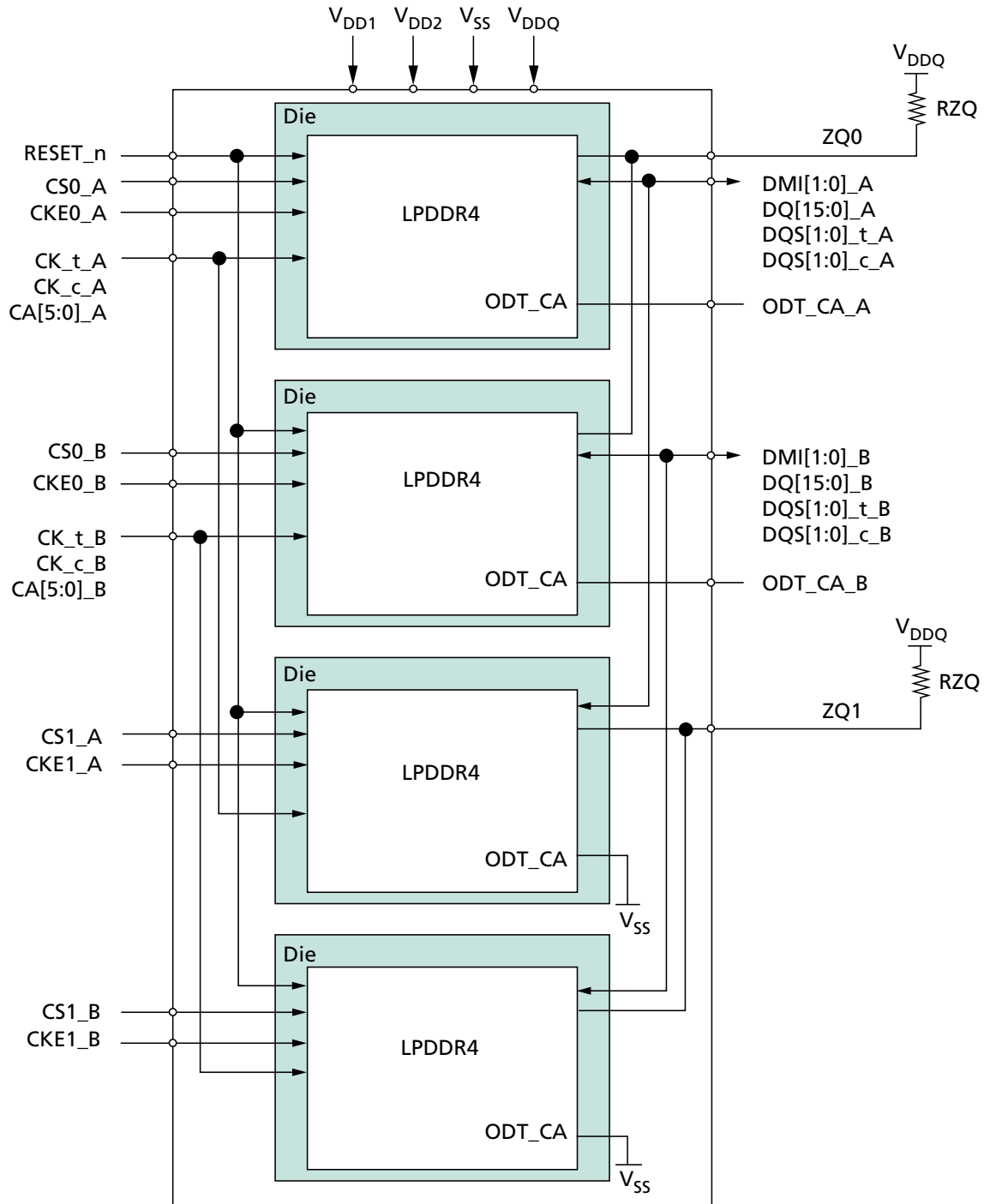




Figure 3: Quad-Die, Dual-Channel, Dual-Rank Package Block Diagram



Note: 1. ODT(ca) for rank 0 of each channel is wired to the respective ODT ball. ODT(ca) for rank 1 of each channel is wired to V_{SS} in the package.



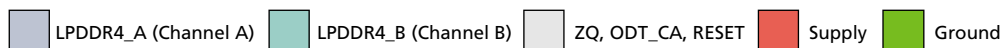
**200b: x32 LPDDR4 SDRAM
Ball Assignments and Descriptions**

Ball Assignments and Descriptions

Figure 4: 200-Ball Dual-Channel, Single-Rank Discrete FBGA

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
|----|------------------|-----------------|------------------|------------------|------------------|---|---|------------------|------------------|------------------|-----------------|------------------|
| A | DNU | DNU | V _{SS} | V _{DD2} | ZQ0 | | | NC | V _{DD2} | V _{SS} | DNU | DNU |
| B | DNU | DQ0_A | V _{DDQ} | DQ7_A | V _{DDQ} | | | V _{DDQ} | DQ15_A | V _{DDQ} | DQ8_A | DNU |
| C | V _{SS} | DQ1_A | DMI0_A | DQ6_A | V _{SS} | | | V _{SS} | DQ14_A | DMI1_A | DQ9_A | V _{SS} |
| D | V _{DDQ} | V _{SS} | DQS0_t_A | V _{SS} | V _{DDQ} | | | V _{DDQ} | V _{SS} | DQS1_t_A | V _{SS} | V _{DDQ} |
| E | V _{SS} | DQ2_A | DQS0_c_A | DQ5_A | V _{SS} | | | V _{SS} | DQ13_A | DQS1_c_A | DQ10_A | V _{SS} |
| F | V _{DD1} | DQ3_A | V _{DDQ} | DQ4_A | V _{DD2} | | | V _{DD2} | DQ12_A | V _{DDQ} | DQ11_A | V _{DD1} |
| G | V _{SS} | ODT_CA_A | V _{SS} | V _{DD1} | V _{SS} | | | V _{SS} | V _{DD1} | V _{SS} | NC | V _{SS} |
| H | V _{DD2} | CA0_A | NC | CS0_A | V _{DD2} | | | V _{DD2} | CA2_A | CA3_A | CA4_A | V _{DD2} |
| J | V _{SS} | CA1_A | V _{SS} | CKE0_A | NC | | | CK_t_A | CK_c_A | V _{SS} | CA5_A | V _{SS} |
| K | V _{DD2} | V _{SS} | V _{DD2} | V _{SS} | NC | | | NC | V _{SS} | V _{DD2} | V _{SS} | V _{DD2} |
| L | | | | | | | | | | | | |
| M | | | | | | | | | | | | |
| N | V _{DD2} | V _{SS} | V _{DD2} | V _{SS} | NC | | | NC | V _{SS} | V _{DD2} | V _{SS} | V _{DD2} |
| P | V _{SS} | CA1_B | V _{SS} | CKE0_B | NC | | | CK_t_B | CK_c_B | V _{SS} | CA5_B | V _{SS} |
| R | V _{DD2} | CA0_B | NC | CS0_B | V _{DD2} | | | V _{DD2} | CA2_B | CA3_B | CA4_B | V _{DD2} |
| T | V _{SS} | ODT_CA_B | V _{SS} | V _{DD1} | V _{SS} | | | V _{SS} | V _{DD1} | V _{SS} | RESET_n | V _{SS} |
| U | V _{DD1} | DQ3_B | V _{DDQ} | DQ4_B | V _{DD2} | | | V _{DD2} | DQ12_B | V _{DDQ} | DQ11_B | V _{DD1} |
| V | V _{SS} | DQ2_B | DQS0_c_B | DQ5_B | V _{SS} | | | V _{SS} | DQ13_B | DQS1_c_B | DQ10_B | V _{SS} |
| W | V _{DDQ} | V _{SS} | DQS0_t_B | V _{SS} | V _{DDQ} | | | V _{DDQ} | V _{SS} | DQS1_t_B | V _{SS} | V _{DDQ} |
| Y | V _{SS} | DQ1_B | DMI0_B | DQ6_B | V _{SS} | | | V _{SS} | DQ14_B | DMI1_B | DQ9_B | V _{SS} |
| AA | DNU | DQ0_B | V _{DDQ} | DQ7_B | V _{DDQ} | | | V _{DDQ} | DQ15_B | V _{DDQ} | DQ8_B | DNU |
| AB | DNU | DNU | V _{SS} | V _{DD2} | V _{SS} | | | V _{SS} | V _{DD2} | V _{SS} | DNU | DNU |

Top View (ball down)





200b: x32 LPDDR4 SDRAM Ball Assignments and Descriptions

Figure 5: 200-Ball Dual-Channel, Dual-Rank Discrete FBGA

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
|----|------------------|-----------------|------------------|------------------|------------------|---|---|------------------|------------------|------------------|-----------------|------------------|
| A | DNU | DNU | V _{SS} | V _{DD2} | ZQ0 | | | ZQ1 | V _{DD2} | V _{SS} | DNU | DNU |
| B | DNU | DQ0_A | V _{DDQ} | DQ7_A | V _{DDQ} | | | V _{DDQ} | DQ15_A | V _{DDQ} | DQ8_A | DNU |
| C | V _{SS} | DQ1_A | DMI0_A | DQ6_A | V _{SS} | | | V _{SS} | DQ14_A | DMI1_A | DQ9_A | V _{SS} |
| D | V _{DDQ} | V _{SS} | DQS0_t_A | V _{SS} | V _{DDQ} | | | V _{DDQ} | V _{SS} | DQS1_t_A | V _{SS} | V _{DDQ} |
| E | V _{SS} | DQ2_A | DQS0_c_A | DQ5_A | V _{SS} | | | V _{SS} | DQ13_A | DQS1_c_A | DQ10_A | V _{SS} |
| F | V _{DD1} | DQ3_A | V _{DDQ} | DQ4_A | V _{DD2} | | | V _{DD2} | DQ12_A | V _{DDQ} | DQ11_A | V _{DD1} |
| G | V _{SS} | ODT_CA_A | V _{SS} | V _{DD1} | V _{SS} | | | V _{SS} | V _{DD1} | V _{SS} | NC | V _{SS} |
| H | V _{DD2} | CA0_A | CS1_A | CS0_A | V _{DD2} | | | V _{DD2} | CA2_A | CA3_A | CA4_A | V _{DD2} |
| J | V _{SS} | CA1_A | V _{SS} | CKE0_A | CKE1_A | | | CK_t_A | CK_c_A | V _{SS} | CA5_A | V _{SS} |
| K | V _{DD2} | V _{SS} | V _{DD2} | V _{SS} | NC | | | NC | V _{SS} | V _{DD2} | V _{SS} | V _{DD2} |
| L | | | | | | | | | | | | |
| M | | | | | | | | | | | | |
| N | V _{DD2} | V _{SS} | V _{DD2} | V _{SS} | NC | | | NC | V _{SS} | V _{DD2} | V _{SS} | V _{DD2} |
| P | V _{SS} | CA1_B | V _{SS} | CKE0_B | CKE1_B | | | CK_t_B | CK_c_B | V _{SS} | CA5_B | V _{SS} |
| R | V _{DD2} | CA0_B | CS1_B | CS0_B | V _{DD2} | | | V _{DD2} | CA2_B | CA3_B | CA4_B | V _{DD2} |
| T | V _{SS} | ODT_CA_B | V _{SS} | V _{DD1} | V _{SS} | | | V _{SS} | V _{DD1} | V _{SS} | RESET_n | V _{SS} |
| U | V _{DD1} | DQ3_B | V _{DDQ} | DQ4_B | V _{DD2} | | | V _{DD2} | DQ12_B | V _{DDQ} | DQ11_B | V _{DD1} |
| V | V _{SS} | DQ2_B | DQS0_c_B | DQ5_B | V _{SS} | | | V _{SS} | DQ13_B | DQS1_c_B | DQ10_B | V _{SS} |
| W | V _{DDQ} | V _{SS} | DQS0_t_B | V _{SS} | V _{DDQ} | | | V _{DDQ} | V _{SS} | DQS1_t_B | V _{SS} | V _{DDQ} |
| Y | V _{SS} | DQ1_B | DMI0_B | DQ6_B | V _{SS} | | | V _{SS} | DQ14_B | DMI1_B | DQ9_B | V _{SS} |
| AA | DNU | DQ0_B | V _{DDQ} | DQ7_B | V _{DDQ} | | | V _{DDQ} | DQ15_B | V _{DDQ} | DQ8_B | DNU |
| AB | DNU | DNU | V _{SS} | V _{DD2} | V _{SS} | | | V _{SS} | V _{DD2} | V _{SS} | DNU | DNU |

Top View (ball down)

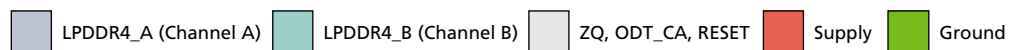


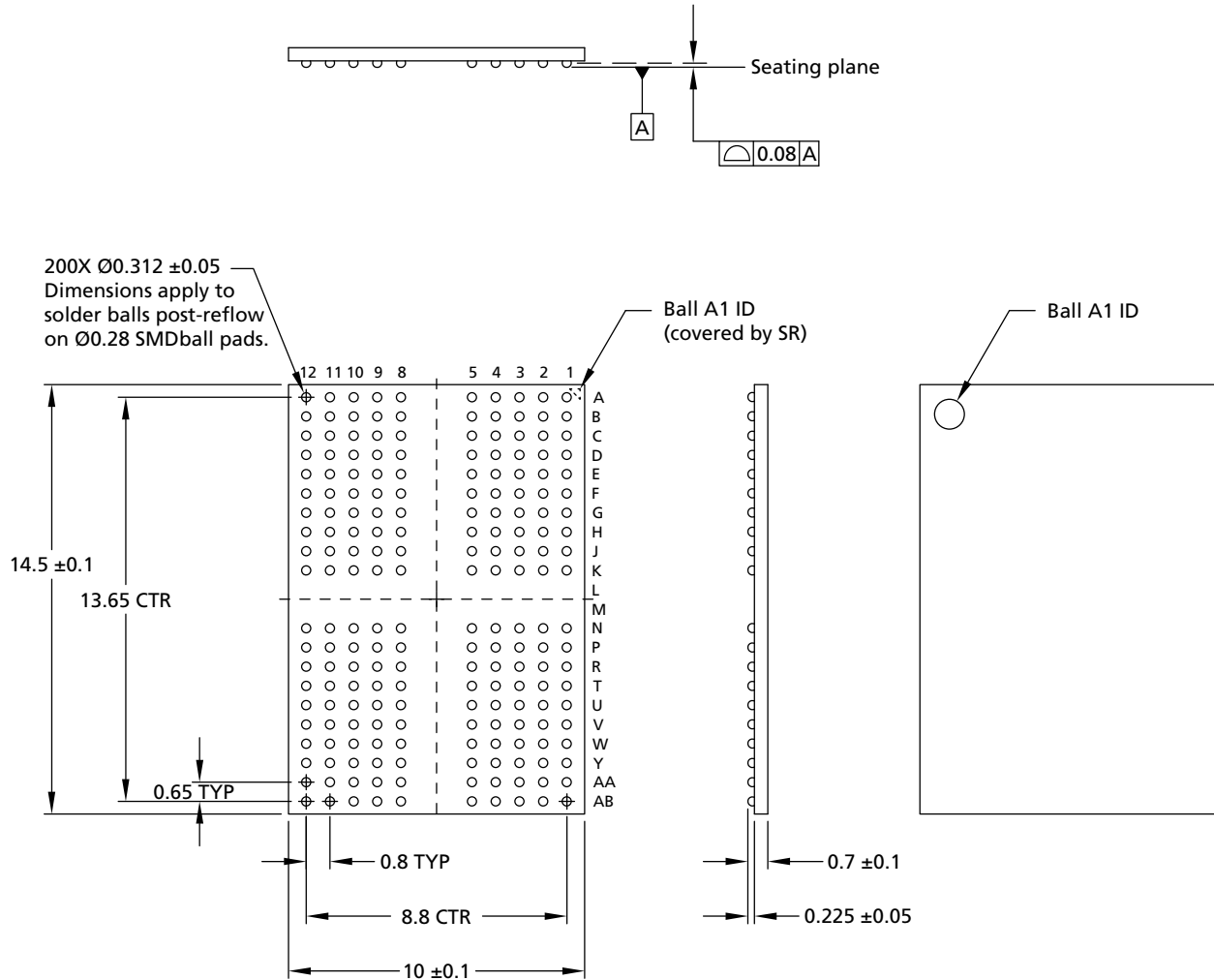

Table 3: Ball/Pad Descriptions

| Symbol | Type | Description |
|---|-----------|--|
| CK_t_A, CK_c_A, CK_t_B, CK_c_B | Input | Clock: CK_t and CK_c are differential clock inputs. All address, command and control input signals are sampled on positive edge of CK_t and the negative edge of CK_c. AC timings for CA parameters are referenced to clock. Each channel (A, B) has its own clock pair. |
| CKE0_A, CKE1_A, CKE0_B, CKE1_B | Input | Clock enable: CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is sampled at the rising edge of CK. |
| CS0_A, CS1_A, CS0_B, CS1_B | Input | Chip select: Each channel (A, B) has its own CS signals. |
| CA[5:0]_A, CA[5:0]_B | Input | Command/address inputs: Provide the command and address inputs according to the command truth table. Each channel (A, B) has its own CA signals. |
| ODT_CA_A, ODT_CA_B | Input | CA ODT Control: The ODT_CA pin is used in conjunction with the mode register to turn on/off the on-die termination for CA pins. It is bonded to V _{DD2} within the package, or at the package ball, for the terminating rank, and the non-terminating ranks are bonded to V _{SS} (or left floating with a weak pull-down on the DRAM die). The terminating rank is the DRAM that terminates the CA bus for all die on the same channel. |
| DQ[15:0]_A, DQ[15:0]_B | I/O | Data input/output: Bidirectional data bus. |
| DQS[1:0]_t_A, DQS[1:0]_c_A, DQS[1:0]_t_B, DQS[1:0]_c_B | I/O | Data strobe: DQS_t and DQS_c are bi-directional differential output clock signals used to strobe data during a READ or WRITE. The data strobe is generated by the DRAM for a READ and is edge-aligned with data. The data strobe is generated by the SoC memory controller for a WRITE and is trained to precede data. Each byte of data has a data strobe signal pair. Each channel (A, B) has its own DQS_t and DQS_c strobes. |
| DMI[1:0]_A, DMI[1:0]_B | I/O | Data Mask/Data Bus Inversion: DMI is a dual use bi-directional signal used to indicate data to be masked, and data which is inverted on the bus. For data bus inversion (DBI), the DMI signal is driven HIGH when the data on the data bus is inverted, or driven LOW when the data is in its normal state. DBI can be disabled via a mode register setting. For data mask, the DMI signal is used in combination with the data lines to indicate data to be masked in a MASK WRITE command (see the Data Mask (DM) and Data Bus Inversion (DBI) sections for details). The data mask function can be disabled via a mode register setting. Each byte of data has a DMI signal. Each channel has its own DMI signals. |
| ZQ0, ZQ1 | Reference | ZQ Calibration Reference: Used to calibrate the output drive strength and the termination resistance. The ZQ pin shall be connected to V _{DDQ} through a 240Ω ±1% resistor. |
| V _{DDQ} , V _{DD1} , V _{DD2} | Supply | Power supplies: Isolated on the die for improved noise immunity. |
| V _{SS} | Supply | Ground Reference: Power supply ground reference. |
| RESET_n | Input | RESET: When asserted LOW, the RESET pin resets all channels of the die. |
| DNU | – | Do not use: Must be grounded or left floating. |
| NC | – | No connect: Not internally connected. |



Package Dimensions

Figure 6: 200-Ball WFBGA – 10mm × 14.5mm (Package Code: NP)

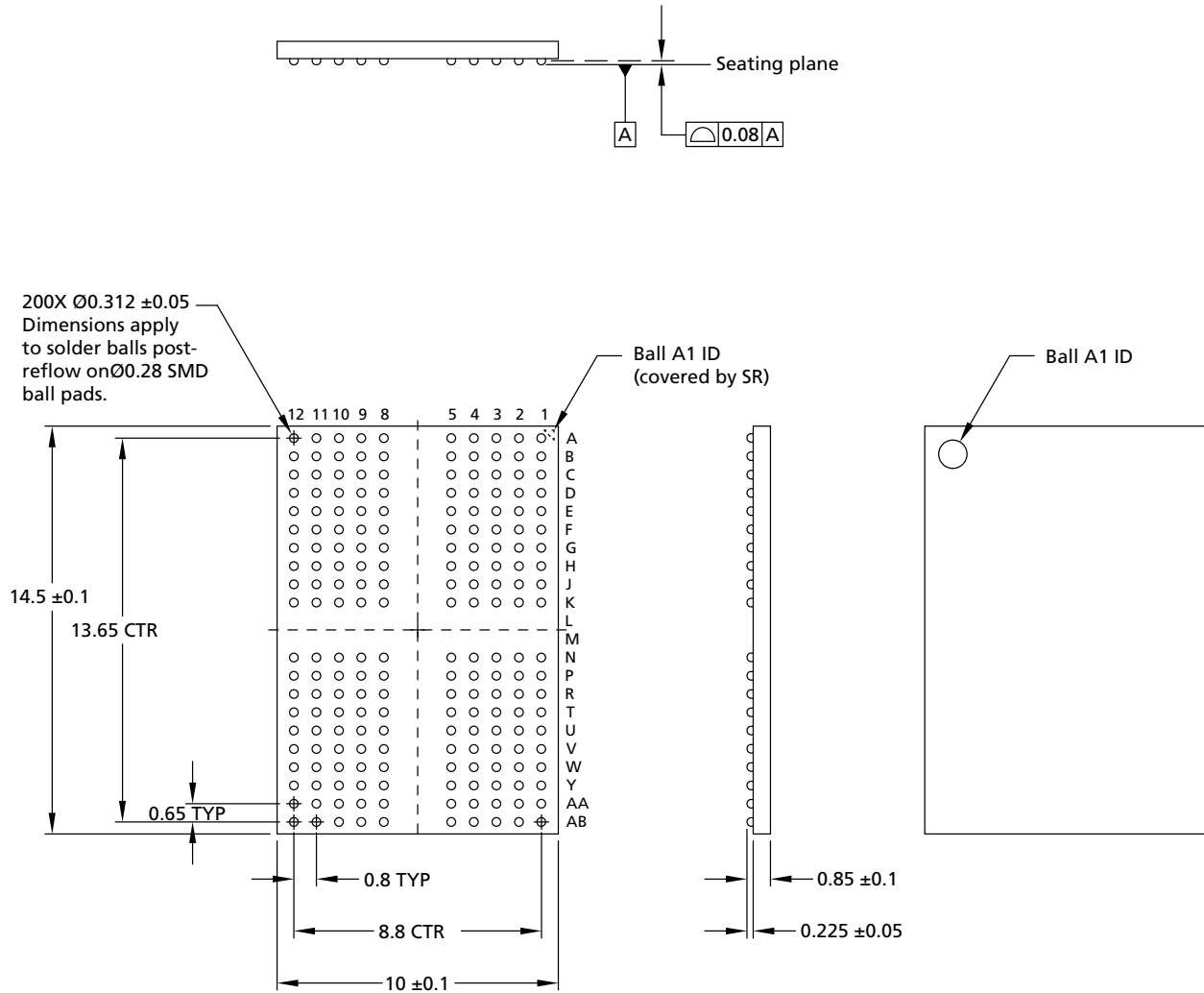


- Notes:
1. All dimensions are in millimeters.
 2. Solder ball composition: SAC302 with NiAu pads (96.8% Sn, 3Ag, 0.2% Cu).
 3. The package height does not include room temperature warpage.



**200b: x32 LPDDR4 SDRAM
Package Dimensions**

Figure 7: 200-Ball VFBGA – 10mm × 14.5mm (Package Code: NQ)

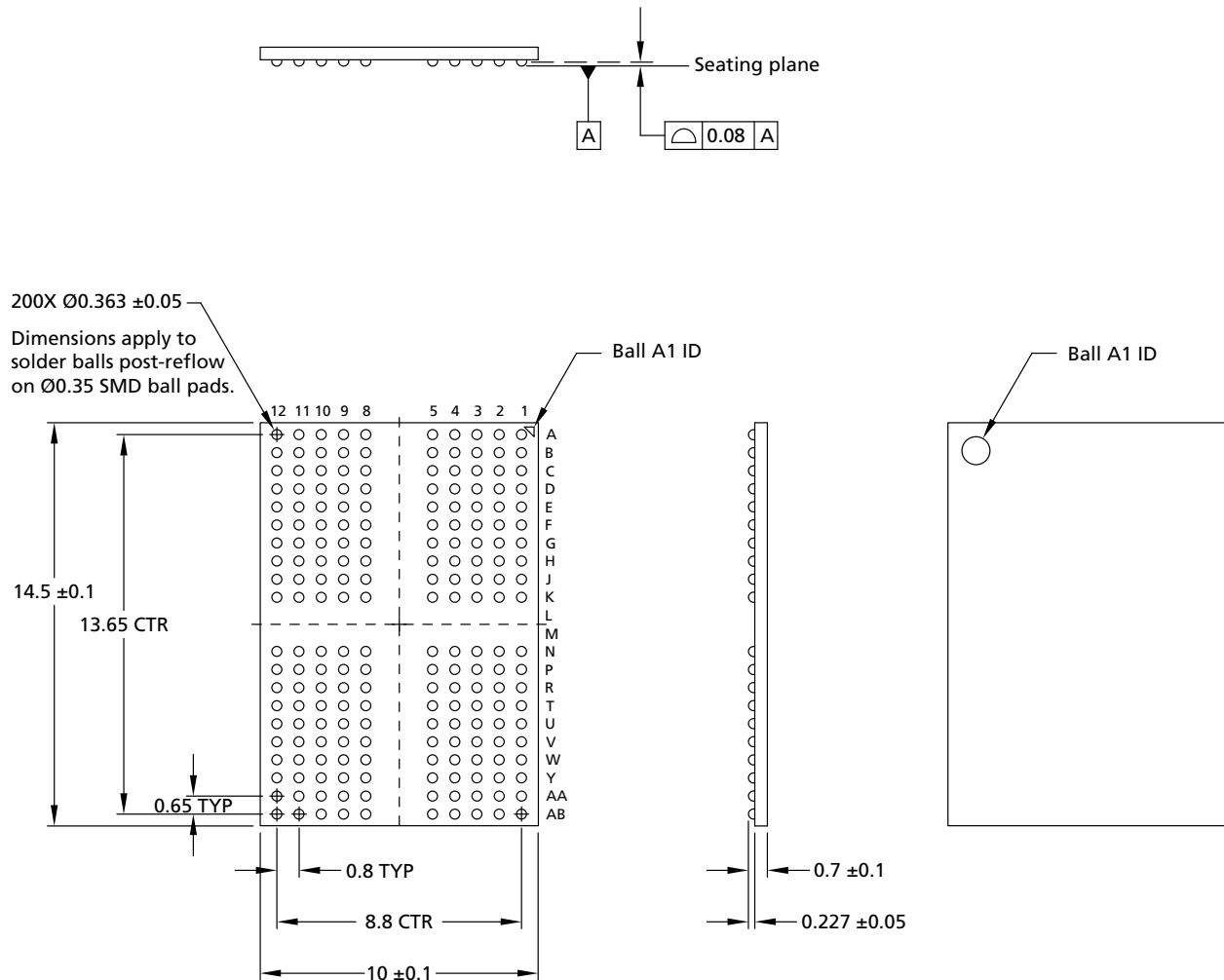


- Notes:
1. All dimensions are in millimeters.
 2. Solder ball composition: SAC302 with NiAu pads (96.8% Sn, 3Ag, 0.2% Cu).
 3. The package height does not include room temperature warpage.



**200b: x32 LPDDR4 SDRAM
Package Dimensions**

Figure 8: 200-Ball WFBGA – 10mm × 14.5mm (Package Code: DS)

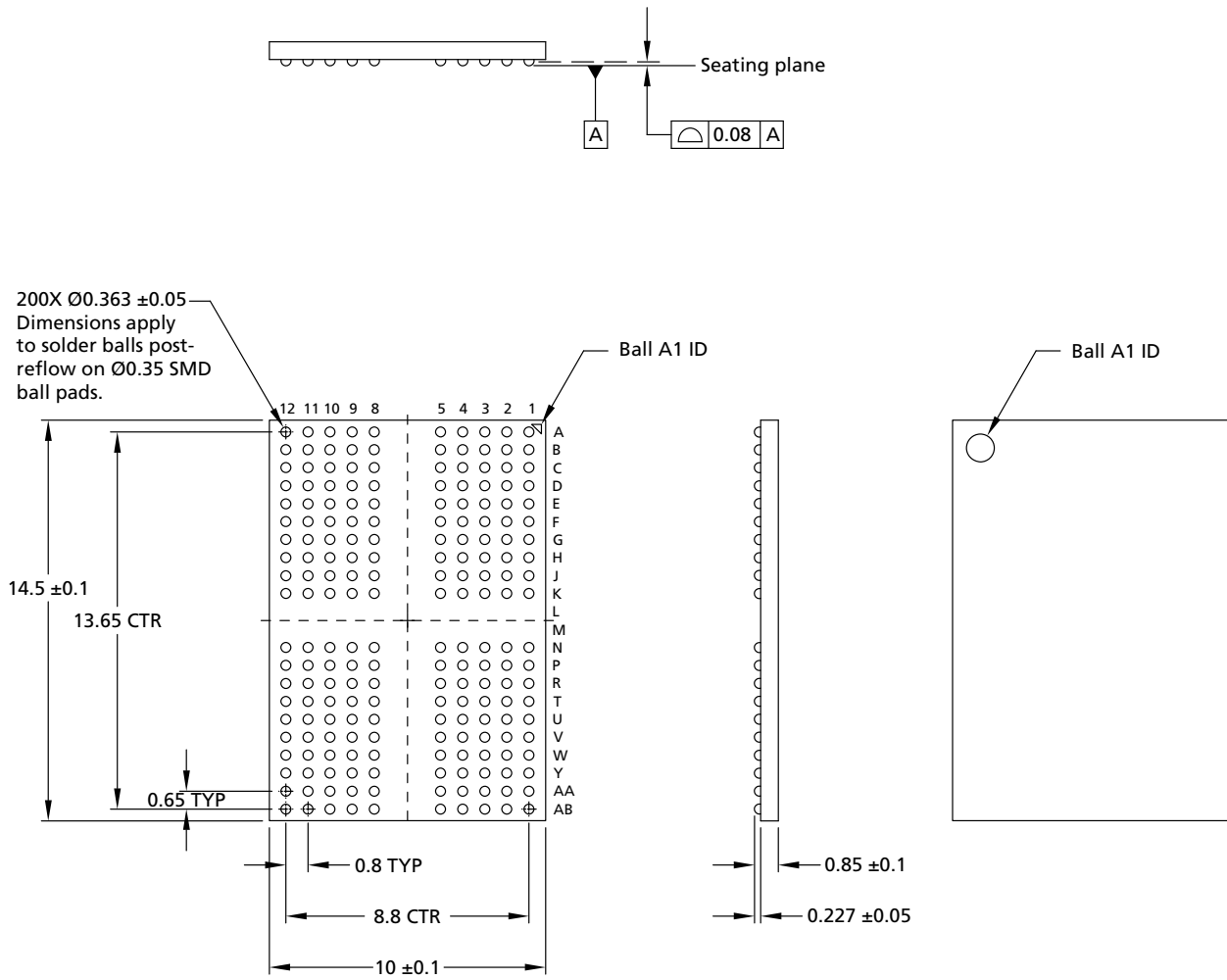


- Notes:
1. All dimensions are in millimeters.
 2. Solder ball composition: SAC302 with NiAu pads (96.8% Sn, 3Ag, 0.2% Cu).
 3. The package height does not include room temperature warpage.



**200b: x32 LPDDR4 SDRAM
Package Dimensions**

Figure 9: 200-Ball WFBGA – 10mm × 14.5mm (Package Code: DT)



- Notes:
1. All dimensions are in millimeters.
 2. Solder ball composition: SAC302 with NiAu pads (96.8% Sn, 3Ag, 0.2% Cu).
 3. The package height does not include room temperature warpage.



MR0, MR[6:5], MR8, MR13, MR24 Definition

Table 4: Mode Register Contents

| Mode Register | OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---------------|--|-----|-----|-----|--------------------------|------------------|------------|------------|
| MR0 | | | | | | | | REF |
| | OP[0] = 0b: Both legacy and modified refresh mode supported | | | | | | | |
| MR5 | Manufacturer ID | | | | | | | |
| | 1111 1111b : Micron | | | | | | | |
| MR6 | Revision ID1 | | | | | | | |
| | 0000 0001b | | | | | | | |
| MR8 | Density | | | | | | | |
| | OP[5:2] = 0011b: 6Gb single channel die | | | | | | | |
| MR13 | | | | | | | VRO | |
| | 0b: Normal operation (default) 1b: Output the $V_{REF(CA)}$ value on DQ7 and $V_{REF(DQ)}$ value on DQ6 | | | | | | | |
| MR24 | TRR | | | | Unlimited MAC | MAC value | | |
| | OP[3:0] = 1000b: Unlimited MAC OP[7] = 0b: Disable (default) 1b: Reserved | | | | | | | |

- Notes:
1. The contents of MR0, MR[6:5], MR8, MR13, and MR24 will reflect information specific to each in these packages.
 2. Other bits not defined above and other mode registers are referred to in Mode Register Assignments and Definitions section.



I_{DD} Parameters

Refer to I_{DD} Specification Parameters and Test Conditions section for detailed conditions.

Table 5: I_{DD} Parameters – Single-Die

V_{DD2}, V_{DDQ} = 1.06–1.17V; V_{DD1} = 1.70–1.95V; T_C = –30°C to +85°C

| Parameter | Supply | Speed Grade | | Unit | Note |
|---------------------|------------------|-------------|-----------|------|------|
| | | 3200 Mbps | 3733 Mbps | | |
| I _{DD01} | V _{DD1} | 3.5 | 3.5 | mA | |
| I _{DD02} | V _{DD2} | 45 | 45 | | |
| I _{DD0Q} | V _{DDQ} | 0.75 | 0.75 | | |
| I _{DD2P1} | V _{DD1} | 1.2 | 1.2 | mA | |
| I _{DD2P2} | V _{DD2} | 3 | 3 | | |
| I _{DD2PQ} | V _{DDQ} | 0.75 | 0.75 | | |
| I _{DD2PS1} | V _{DD1} | 1.2 | 1.2 | mA | |
| I _{DD2PS2} | V _{DD2} | 3 | 3 | | |
| I _{DD2PSQ} | V _{DDQ} | 0.75 | 0.75 | | |
| I _{DD2N1} | V _{DD1} | 2 | 2 | mA | |
| I _{DD2N2} | V _{DD2} | 27 | 27 | | |
| I _{DD2NQ} | V _{DDQ} | 0.75 | 0.75 | | |
| I _{DD2NS1} | V _{DD1} | 2 | 2 | mA | |
| I _{DD2NS2} | V _{DD2} | 23 | 23 | | |
| I _{DD2NSQ} | V _{DDQ} | 0.75 | 0.75 | | |
| I _{DD3P1} | V _{DD1} | 1.2 | 1.2 | mA | |
| I _{DD3P2} | V _{DD2} | 9 | 9 | | |
| I _{DD3PQ} | V _{DDQ} | 0.75 | 0.75 | | |
| I _{DD3PS1} | V _{DD1} | 1.2 | 1.2 | mA | |
| I _{DD3PS2} | V _{DD2} | 9 | 9 | | |
| I _{DD3PSQ} | V _{DDQ} | 0.75 | 0.75 | | |
| I _{DD3N1} | V _{DD1} | 2.25 | 2.25 | mA | |
| I _{DD3N2} | V _{DD2} | 30 | 30 | | |
| I _{DD3NQ} | V _{DDQ} | 0.75 | 0.75 | | |
| I _{DD3NS1} | V _{DD1} | 2.25 | 2.25 | mA | |
| I _{DD3NS2} | V _{DD2} | 26 | 26 | | |
| I _{DD3NSQ} | V _{DDQ} | 0.75 | 0.75 | | |
| I _{DD4R1} | V _{DD1} | 2.25 | 2.25 | mA | 3 |
| I _{DD4R2} | V _{DD2} | 275 | 315 | | |
| I _{DD4RQ} | V _{DDQ} | 150 | 160 | | |
| I _{DD4W1} | V _{DD1} | 2.25 | 2.25 | mA | |
| I _{DD4W2} | V _{DD2} | 210 | 240 | | |
| I _{DD4WQ} | V _{DDQ} | 55 | 65 | | |



Table 5: I_{DD} Parameters – Single-Die (Continued)

V_{DD2}, V_{DDQ} = 1.06–1.17V; V_{DD1} = 1.70–1.95V; T_C = –30°C to +85°C

| Parameter | Supply | Speed Grade | | Unit | Note |
|---------------------|------------------|-------------|-----------|------|------|
| | | 3200 Mbps | 3733 Mbps | | |
| I _{DD51} | V _{DD1} | 10 | 10 | mA | |
| I _{DD52} | V _{DD2} | 90 | 90 | | |
| I _{DD5Q} | V _{DDQ} | 0.75 | 0.75 | | |
| I _{DD5AB1} | V _{DD1} | 2.5 | 2.5 | mA | |
| I _{DD5AB2} | V _{DD2} | 30 | 30 | | |
| I _{DD5ABQ} | V _{DDQ} | 0.75 | 0.75 | | |
| I _{DD5PB1} | V _{DD1} | 2.5 | 2.5 | mA | |
| I _{DD5PB2} | V _{DD2} | 30 | 30 | | |
| I _{DD5PBQ} | V _{DDQ} | 0.75 | 0.75 | | |

- Notes: 1. Published I_{DD} values except I_{DD4RQ} are the maximum of the distribution of the arithmetic mean. Refer to the following note for I_{DD4RQ}; refer to I_{DD6} Full-Array Self Refresh Current table for I_{DD6}.
2. I_{DD4RQ} value is reference only. Typical value. DBI disabled, V_{OH} = V_{DDQ}/3, T_C = 25°C.

Table 6: I_{DD6} Full-Array Self Refresh Current

V_{DD2}, V_{DDQ} = 1.06–1.17V; V_{DD1} = 1.70–1.95V

| Temperature | Supply | Full-Array Self Refresh Current | Unit |
|-------------|------------------|---------------------------------|------|
| 25°C | V _{DD1} | 0.3 | mA |
| | V _{DD2} | 0.5 | |
| | V _{DDQ} | 0.1 | |
| 85°C | V _{DD1} | 2.0 | |
| | V _{DD2} | 5.0 | |
| | V _{DDQ} | 0.75 | |

- Note: 1. I_{DD6} 25°C is the typical, and I_{DD6} 85°C is the maximum of the distribution of the arithmetic mean.

Table 7: I_{DD} Parameters – Single-Die

V_{DD2}, V_{DDQ} = 1.06–1.17V; V_{DD1} = 1.70–1.95V; T_C = –30°C to +105°C

| Parameter | Supply | Speed Grade | | Unit | Note |
|--------------------|------------------|-------------|-----------|------|------|
| | | 3200 Mbps | 3733 Mbps | | |
| I _{DD01} | V _{DD1} | 3.5 | 3.5 | mA | |
| I _{DD02} | V _{DD2} | 45 | 45 | | |
| I _{DD0Q} | V _{DDQ} | 0.75 | 0.75 | | |
| I _{DD2P1} | V _{DD1} | 1.2 | 1.2 | mA | |
| I _{DD2P2} | V _{DD2} | 3 | 3 | | |
| I _{DD2PQ} | V _{DDQ} | 0.75 | 0.75 | | |


Table 7: I_{DD} Parameters – Single-Die (Continued)
 $V_{DD2}, V_{DDQ} = 1.06\text{--}1.17\text{V}; V_{DD1} = 1.70\text{--}1.95\text{V}; T_C = -30^\circ\text{C to } +105^\circ\text{C}$

| Parameter | Supply | Speed Grade | | Unit | Note |
|---------------------|------------------|-------------|-----------|------|------|
| | | 3200 Mbps | 3733 Mbps | | |
| I _{DD2PS1} | V _{DD1} | 1.2 | 1.2 | mA | |
| I _{DD2PS2} | V _{DD2} | 3 | 3 | | |
| I _{DD2PSQ} | V _{DDQ} | 0.75 | 0.75 | | |
| I _{DD2N1} | V _{DD1} | 2 | 2 | mA | |
| I _{DD2N2} | V _{DD2} | 30 | 30 | | |
| I _{DD2NQ} | V _{DDQ} | 0.75 | 0.75 | | |
| I _{DD2NS1} | V _{DD1} | 2 | 2 | mA | |
| I _{DD2NS2} | V _{DD2} | 23 | 23 | | |
| I _{DD2NSQ} | V _{DDQ} | 0.75 | 0.75 | | |
| I _{DD3P1} | V _{DD1} | 1.2 | 1.2 | mA | |
| I _{DD3P2} | V _{DD2} | 9 | 9 | | |
| I _{DD3PQ} | V _{DDQ} | 0.75 | 0.75 | | |
| I _{DD3PS1} | V _{DD1} | 1.2 | 1.2 | mA | |
| I _{DD3PS2} | V _{DD2} | 9 | 9 | | |
| I _{DD3PSQ} | V _{DDQ} | 0.75 | 0.75 | | |
| I _{DD3N1} | V _{DD1} | 2.25 | 2.25 | mA | |
| I _{DD3N2} | V _{DD2} | 36 | 36 | | |
| I _{DD3NQ} | V _{DDQ} | 0.75 | 0.75 | | |
| I _{DD3NS1} | V _{DD1} | 2.25 | 2.25 | mA | |
| I _{DD3NS2} | V _{DD2} | 30 | 30 | | |
| I _{DD3NSQ} | V _{DDQ} | 0.75 | 0.75 | | |
| I _{DD4R1} | V _{DD1} | 2.25 | 2.25 | mA | 3 |
| I _{DD4R2} | V _{DD2} | 310 | 350 | | |
| I _{DD4RQ} | V _{DDQ} | 165 | 170 | | |
| I _{DD4W1} | V _{DD1} | 2.25 | 2.25 | mA | |
| I _{DD4W2} | V _{DD2} | 235 | 265 | | |
| I _{DD4WQ} | V _{DDQ} | 60 | 70 | | |
| I _{DD51} | V _{DD1} | 10 | 10 | mA | |
| I _{DD52} | V _{DD2} | 90 | 90 | | |
| I _{DD5Q} | V _{DDQ} | 0.75 | 0.75 | | |
| I _{DD5AB1} | V _{DD1} | 2.5 | 2.5 | mA | |
| I _{DD5AB2} | V _{DD2} | 30 | 30 | | |
| I _{DD5ABQ} | V _{DDQ} | 0.75 | 0.75 | | |



Table 7: I_{DD} Parameters – Single-Die (Continued)

V_{DD2}, V_{DDQ} = 1.06–1.17V; V_{DD1} = 1.70–1.95V; T_C = –30°C to +105°C

| Parameter | Supply | Speed Grade | | Unit | Note |
|---------------------|------------------|-------------|-----------|------|------|
| | | 3200 Mbps | 3733 Mbps | | |
| I _{DD5PB1} | V _{DD1} | 2.5 | 2.5 | mA | |
| I _{DD5PB2} | V _{DD2} | 30 | 30 | | |
| I _{DD5PBQ} | V _{DDQ} | 0.75 | 0.75 | | |

- Notes: 1. Published I_{DD} values except I_{DD4RQ} are the maximum of the distribution of the arithmetic mean. Refer to another note for I_{DD4RQ}. And refer to another table for I_{DD6}.
2. I_{DD4RQ} value is reference only. Typical value. DBI disabled, V_{OH} = V_{DDQ}/3, T_C = 25°C

Table 8: I_{DD6} Full-Array Self Refresh Current

V_{DD2}, V_{DDQ} = 1.06–1.17V; V_{DD1} = 1.70–1.95V

| Temperature | Supply | Full-Array Self Refresh Current | Unit |
|-------------|------------------|---------------------------------|------|
| 105°C | V _{DD1} | 2 | mA |
| | V _{DD2} | 8 | |
| | V _{DDQ} | 1 | |

- Note: 1. I_{DD6} 105°C is the maximum of the distribution of the arithmetic mean.



Functional Description

The Mobile Low-Power DDR4 SDRAM (LPDDR4) is a high-speed CMOS, dynamic random-access memory internally configured with either 1 or 2 channels. Each channel is comprised of 16 DQs and 8 banks.

LPDDR4 uses a 2-tick, single-data-rate (SDR) protocol on the CA bus to reduce the number of input signals in the system. The term "2-tick" means that the command/address is decoded across two transactions, such that half of the command/address is captured with each of two consecutive rising edges of CK. The 6-bit CA bus contains command, address, and bank information. Some commands such as READ, WRITE, MASKED WRITE, and ACTIVATE require two consecutive 2-tick SDR commands to complete the instruction.

LPDDR4 uses a double-data-rate (DDR) protocol on the DQ bus to achieve high-speed operation. The DDR interface transfers two data bits to each DQ lane in one clock cycle and is matched to a $16n$ -prefetch DRAM architecture. A write/read access consists of a single $16n$ -bit-wide data transfer to/from the DRAM core and 16 corresponding n -bit-wide data transfers at the I/O pins.

Read and write accesses to the device are burst-oriented. Accesses start at a selected column address and continue for a programmed number of columns in a programmed sequence.

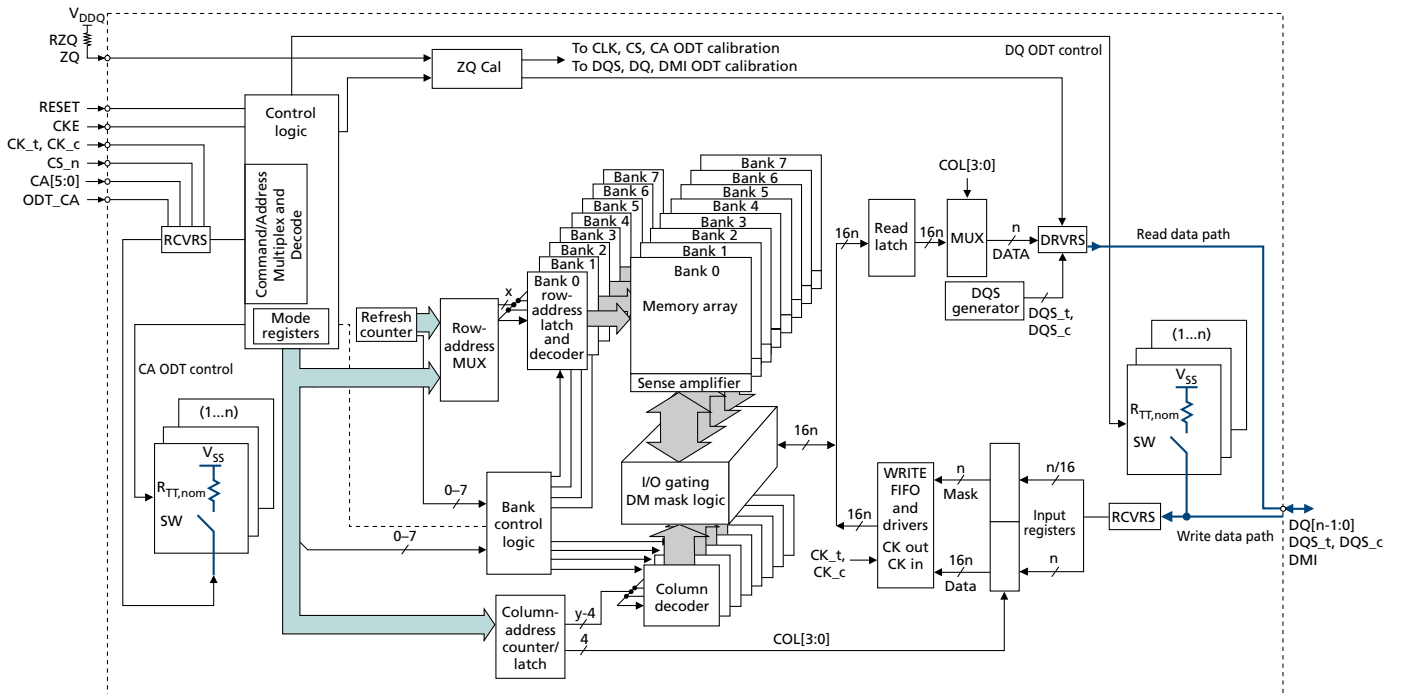
Accesses begin with the registration of an ACTIVATE command to open a row in the memory core, followed by a WRITE or READ command to access column data within the open row. The address and bank address (BA) bits registered by the ACTIVATE command are used to select the bank and row to be opened. The address and BA bits registered with the WRITE or READ command are used to select the bank and the starting column address for the burst access.

Prior to normal operation, the LPDDR4 SDRAM must be initialized. Following sections provide detailed information about device initialization, register definition, command descriptions and device operations.



200b: x32 LPDDR4 SDRAM Monolithic Device Addressing

Figure 10: Functional Block Diagram



Monolithic Device Addressing

The table below includes all monolithic device addressing options defined by JEDEC. Under the SDRAM Addressing heading near the beginning of this data sheet are addressing details for this product data sheet.



Table 9: Monolithic Device Addressing – Dual-Channel Die

| Memory Density (Per Die) | 4Gb | 6Gb | 8Gb | 12Gb | 16Gb | 24Gb | 32Gb | |
|--------------------------------------|--|--|--|--|--|--|---|---------|
| Memory density (per channel) | 2Gb | 3Gb | 4Gb | 6Gb | 8Gb | 12Gb | 16Gb | |
| Configuration | 16Mb × 16DQ × 8 banks × 2 channels | 24Mb × 16DQ × 8 banks × 2 channels | 32Mb × 16DQ × 8 banks × 2 channels | 48Mb × 16DQ × 8 banks × 2 channels | 64Mb × 16DQ × 8 banks × 2 channels | 96Mb × 16DQ × 8 banks × 2 channels | 128Mb × 16DQ × 8 banks × 2 channels | |
| Number of channels (per die) | 2 | 2 | 2 | 2 | 2 | 2 | 2 | |
| Number of banks (per channel) | 8 | 8 | 8 | 8 | 8 | 8 | 8 | |
| Array prefetch (bits, per channel) | 256 | 256 | 256 | 256 | 256 | 256 | 256 | |
| Number of rows (per channel) | 16,384 | 24,576 | 32,768 | 49,152 | 65,536 | 98,304 | 131,072 | |
| Number of columns (fetch boundaries) | 64 | 64 | 64 | 64 | 64 | 64 | 64 | |
| Page size (bytes) | 2048 | 2048 | 2048 | 2048 | 2048 | 2048 | 2048 | |
| Channel density (bits per channel) | 2,147,483,648 | 3,221,225,472 | 4,294,967,296 | 6,442,450,944 | 8,589,934,592 | 12,884,901,888 | 17,179,869,184 | |
| Total density (bits per die) | 4,294,967,296 | 6,442,450,944 | 8,589,934,592 | 12,884,901,888 | 17,179,869,184 | 25,769,803,776 | 34,359,738,368 | |
| Bank address | BA[2:0] | BA[2:0] | BA[2:0] | BA[2:0] | BA[2:0] | BA[2:0] | BA[2:0] | |
| ×16 | Row add | R[13:0] | R[14:0] (R13 = 0 when R14 = 1) | R[14:0] | R[15:0] (R14 = 0 when R15 = 1) | R[15:0] | R[16:0] (R15 = 0 when R16 = 1) | R[16:0] |
| | Col. add | C[9:0] | C[9:0] | C[9:0] | C[9:0] | C[9:0] | C[9:0] | C[9:0] |
| Burst starting address boundary | 64 bit | 64 bit | 64 bit | 64 bit | 64 bit | 64 bit | 64 bit | |

Table 10: Monolithic Device Addressing – Single-Channel Die

| Memory Density (Per Die) | 2Gb | 3Gb | 4Gb | 6Gb | 8Gb | 12Gb | 16Gb |
|--------------------------------------|------------------------|------------------------|--------------------------------------|------------------------|--------------------------------------|------------------------|--------------------------------------|
| Memory density (per channel) | 2Gb | 3Gb | 4Gb | 6Gb | 8Gb | 12Gb | 16Gb |
| Configuration | 16Mb × 16 DQ × 8 banks | 24Mb × 16 DQ × 8 banks | 32Mb × 16 DQ × 8 banks | 48Mb × 16 DQ × 8 banks | 64Mb × 16 DQ × 8 banks | 96Mb × 16 DQ × 8 banks | 128Mb × 16 DQ × 8 banks |
| Number of channels (per die) | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Number of banks (per channel) | 8 | 8 | 8 | 8 | 8 | 8 | 8 |
| Array prefetch (bits, per channel) | 256 | 256 | 256 | 256 | 256 | 256 | 256 |
| Number of rows (per channel) | 16,384 | 24,576 | 32,768 | 49,152 | 65,536 | 98,304 | 131,072 |
| Number of columns (fetch boundaries) | 64 | 64 | 64 | 64 | 64 | 64 | 64 |
| Page size (bytes) | 2048 | 2048 | 2048 | 2048 | 2048 | 2048 | 2048 |
| Channel density (bits per channel) | 2,147,483,648 | 3,221,225,472 | 4,294,967,296 | 6,442,450,944 | 8,589,934,592 | 12,884,901,888 | 17,179,869,184 |
| Total density (bits per die) | 2,147,483,648 | 3,221,225,472 | 4,294,967,296 | 6,442,450,944 | 8,589,934,592 | 12,884,901,888 | 17,179,869,184 |
| Bank address | BA[2:0] | BA[2:0] | BA[2:0] | BA[2:0] | BA[2:0] | BA[2:0] | BA[2:0] |
| ×16 | Row add | R[13:0] | R[14:0] (R13 = 0 when R14 = 1) | R[14:0] | R[15:0] (R14 = 0 when R15 = 1) | R[15:0] | R[16:0] (R15 = 0 when R16 = 1) |
| | Col. add | C[9:0] | C[9:0] | C[9:0] | C[9:0] | C[9:0] | C[9:0] |
| Burst starting address boundary | 64 bit | 64 bit | 64 bit | 64 bit | 64 bit | 64 bit | 64 bit |

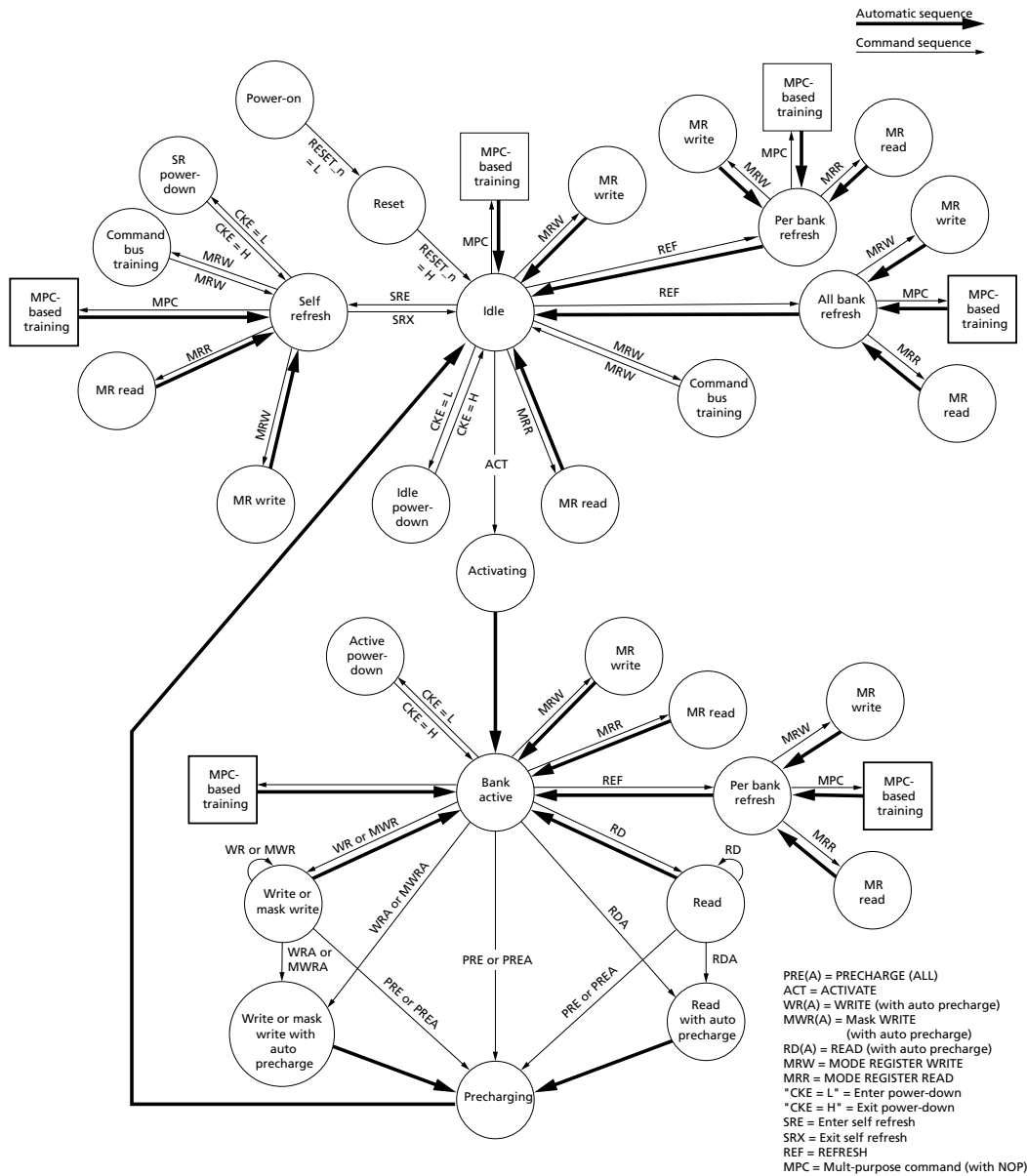
- Notes:
1. The lower two column addresses (C[1:0]) are assumed to be zero and are not transmitted on the CA bus.
 2. Row and column address values on the CA bus that are not used for a particular density should be at valid logic levels.
 3. For non-binary memory densities, only a quarter of the row address space is invalid. When the MSB address bit is HIGH, then the MSB - 1 address bit must be LOW.



Simplified Bus Interface State Diagram

The state diagram provides a simplified illustration of the bus interface, supported state transitions, and the commands that control them. For a complete description of device behavior, use the information provided in the state diagram with the truth tables and timing specifications. The truth tables describe device behavior and applicable restrictions when considering the actual state of all banks. For command descriptions, see the Commands and Timing section.

Figure 11: Simplified State Diagram

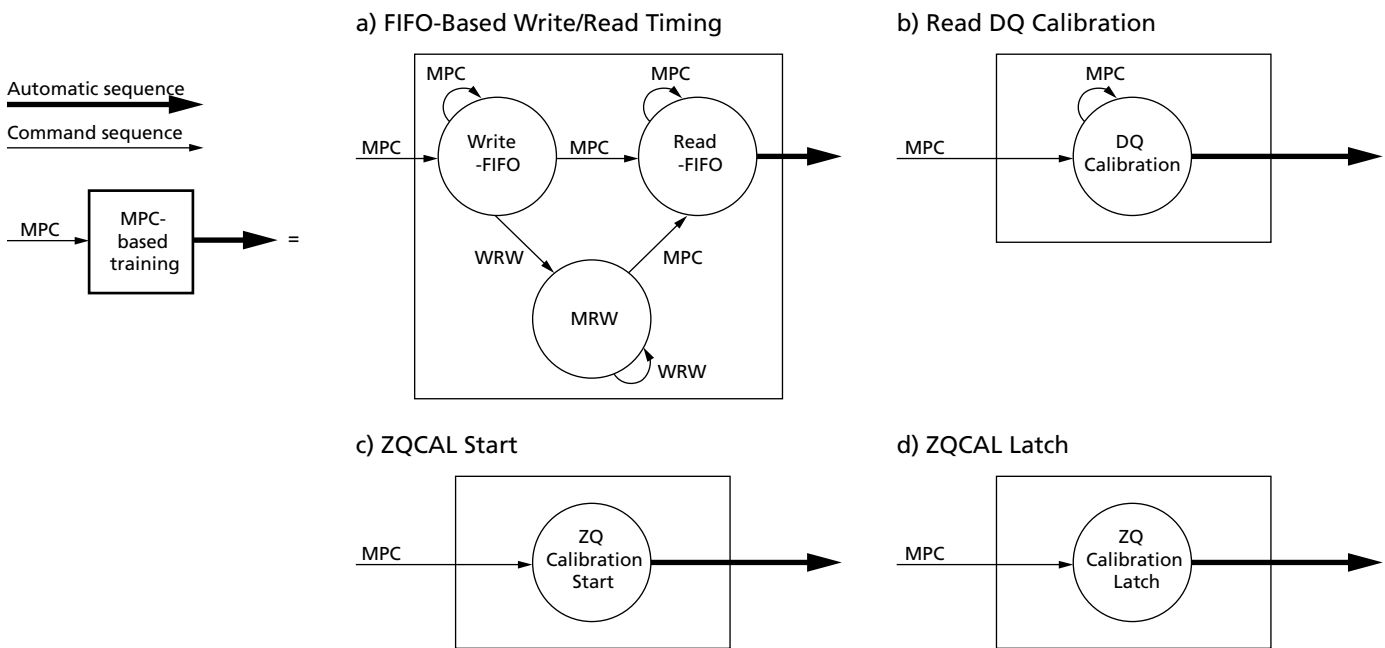


Notes: 1. From the self refresh state, the device can enter power-down, MRR, MRW, or any of the training modes initiated with the MPC command. See the Self Refresh section.



2. All banks are precharged in the idle state.
3. In the case of using an MRW command to enter a training mode, the state machine will not automatically return to the idle state at the conclusion of training. See the applicable training section for more information.
4. In the case of an MPC command to enter a training mode, the state machine may not automatically return to the idle state at the conclusion of training. See the applicable training section for more information.
5. This diagram is intended to provide an overview of the possible state transitions and commands to control them; however, it does not contain the details necessary to operate the device. In particular, situations involving more than one bank are not captured in complete detail.
6. States that have an "automatic return" and can be accessed from more than one prior state (that is, MRW from either idle or active states) will return to the state where they were initiated (that is, MRW from idle will return to idle).
7. The RESET pin can be asserted from any state and will cause the device to enter the reset state. The diagram shows RESET applied from the power-on and idle states as an example, but this should not be construed as a restriction on RESET.
8. MRW commands from the active state cannot change operating parameters of the device that affect timing. Mode register fields which may be changed via MRW from the active state include: MR1-OP[3:0], MR1-OP[7], MR3-OP[7:6], MR10-OP[7:0], MR11-OP[7:0], MR13-OP[5], MR15-OP[7:0], MR16-OP[7:0], MR17-OP[7:0], MR20-OP[7:0], and MR22-OP[4:0].

Figure 12: Simplified State Diagram



Power-Up and Initialization

To ensure proper functionality for power-up and reset initialization, default values for the MR settings are provided in the table below.


Table 11: Mode Register Default Settings

| Item | Mode Register Setting | Default Setting | Description |
|-----------------------|-----------------------|-----------------|-----------------------------------|
| FSP-OP/WR | MR13 OP[7:6] | 00b | FSP-OP/WR[0] are enabled |
| WLS | MR2 OP[6] | 0b | WRITE latency set A is selected |
| WL | MR2 OP[5:3] | 000b | WL = 4 |
| RL | MR2 OP[2:0] | 000b | RL = 6, $nRTP = 8$ |
| nWR | MR1 OP[6:4] | 000b | $nWR = 6$ |
| DBI-WR/RD | MR3 OP[7:6] | 00b | Write and read DBI are disabled |
| CA ODT | MR11 OP[6:4] | 000b | CA ODT is disabled |
| DQ ODT | MR11 OP[2:0] | 000b | DQ ODT is disabled |
| $V_{REF(CA)}$ setting | MR12 OP[6] | 1b | $V_{REF(CA)}$ range[1] is enabled |
| $V_{REF(CA)}$ value | MR12 OP[5:0] | 001101b | Range1: 27.2% of V_{DD2} |
| $V_{REF(DQ)}$ setting | MR14 OP[6] | 1b | $V_{REF(DQ)}$ range[1] enabled |
| $V_{REF(DQ)}$ value | MR14 OP[5:0] | 001101b | Range1: 27.2% of V_{DDQ} |

The following sequence must be used to power up the device. Unless specified otherwise, this procedure is mandatory. The power-up sequence of all channels must proceed simultaneously.

Voltage Ramp

1. While applying power (after T_a), RESET_n should be held LOW ($\leq 0.2 \times V_{DD2}$), and all other inputs must be between $V_{IL,min}$ and $V_{IH,max}$. The device outputs remain at High-Z while RESET_n is held LOW. Power supply voltage ramp requirements are provided in the table below. V_{DD1} must ramp at the same time or earlier than V_{DD2} . V_{DD2} must ramp at the same time or earlier than V_{DDQ} .

Table 12: Voltage Ramp Conditions

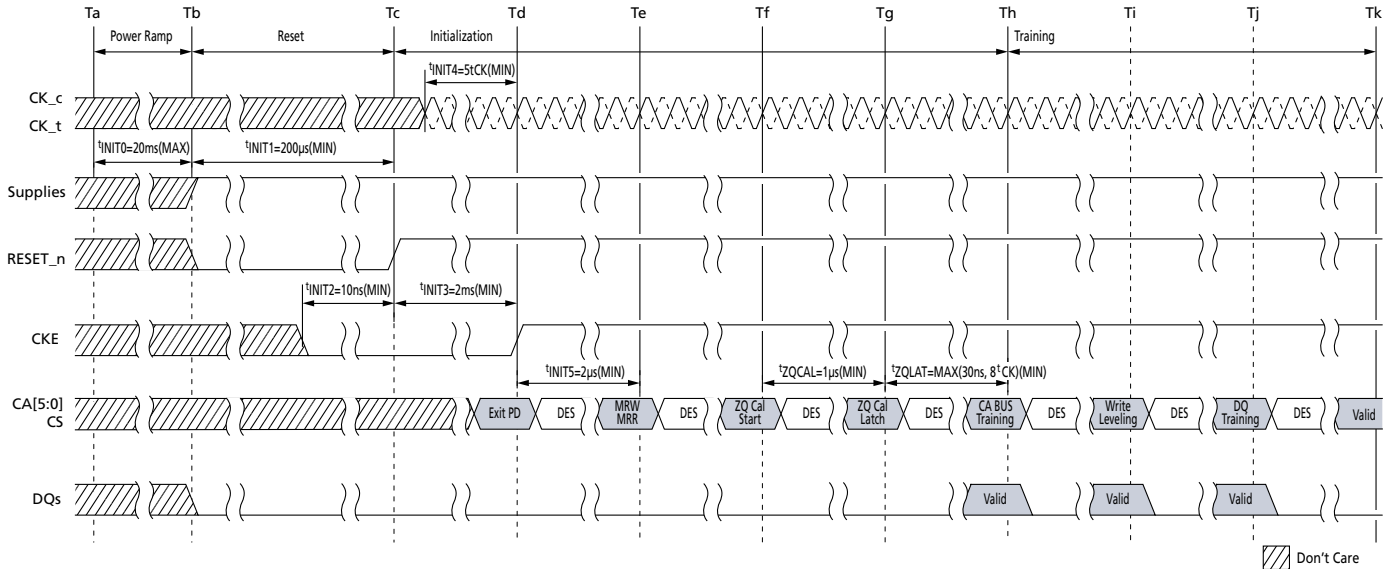
| After... | Applicable Conditions |
|---------------|--|
| Ta is reached | V_{DD1} must be greater than V_{DD2} |
| | V_{DD2} must be greater than $V_{DDQ} - 200mV$ |

- Notes:
1. T_a is the point when any power supply first reaches 300mV.
 2. Voltage ramp conditions in above table apply between T_a and power-off (controlled or uncontrolled).
 3. T_b is the point at which all supply and reference voltages are within their defined operating ranges.
 4. Power ramp duration t_{INIT0} ($T_b - T_a$) must not exceed 20ms.
 5. The voltage difference between any V_{SS} and V_{SSQ} must not exceed 100mV.
2. Following completion of the of the voltage ramp (T_b), RESET_n must be held LOW for t_{INIT1} . DQ, DMI, DQS_t, and DQS_c voltage levels must be between V_{SSQ} and V_{DDQ} during voltage ramp to avoid latch-up. CK_t and CK_c, CS, and CA input levels must be between V_{SS} and V_{DD2} during voltage ramp to avoid latch-up. Voltage ramp power supply requirements are provided in the table below.



3. Beginning at T_b , RESET_n must remain LOW for at least $t_{INIT1}(T_c)$, after which RESET_n can be de-asserted to HIGH(T_c). At least 10ns before CKE de-assertion, CKE is required to be set LOW. All other input signals are "Don't Care."

Figure 13: Voltage Ramp and Initialization Sequence



Note: 1. Training is optional and may be done at the system designer's discretion. The order of training may be different than what is shown here.

4. After RESET_n is de-asserted(T_c), wait at least t_{INIT3} before activating CKE. CK_t, CK_c must be started and stabilized for t_{INIT4} before CKE goes active(T_d). CS must remain LOW when the controller activates CKE.

5. After CKE is set to HIGH, wait a minimum of t_{INIT5} to issue any MRR or MRW commands(T_e). For MRR and MRW commands, the clock frequency must be within the range defined for t_{CKb} . Some AC parameters (for example, t_{DQSCk}) could have relaxed timings (such as t_{DQSCkb}) before the system is appropriately configured.

6. After completing all MRW commands to set the pull-up, pull-down, and Rx termination values, the controller can issue the ZQCAL START command to the memory(T_f). This command is used to calibrate the V_{OH} level and the output impedance over process, voltage, and temperature. In systems where more than one device share one external ZQ resistor, the controller must not overlap the ZQ calibration sequence of each device. The ZQ calibration sequence is completed after t_{ZQCAL} (T_g). The ZQCAL LATCH command must be issued to update the DQ drivers and DQ + CA ODT to the calibrated values.

7. After t_{ZQLAT} is satisfied (T_h), the command bus (internal $V_{REF(CA)}$, CS, and CA) should be trained for high-speed operation by issuing an MRW command (command bus training mode). This command is used to calibrate the device's internal V_{REF} and align CS/CA with CK for high-speed operation. The device will power-up with receivers configured for low-speed operations and with $V_{REF(CA)}$ set to a default factory setting. Normal device operation at clock speeds higher than t_{CKb} may not be possible until command bus training is complete. The command bus training MRW command uses the CA bus as inputs for the calibration data stream, and it outputs the results asynchro-



nously on the DQ bus. See command bus training in the MRW section for information on how to enter/exit the training mode.

8. After command bus training, the controller must perform write leveling. Write leveling mode is enabled when MR2 OP[7] is HIGH(Ti). See the Write Leveling section for a detailed description of the write leveling entry and exit sequence. In write leveling mode, the controller adjusts write DQS timing to the point where the device recognizes the start of write DQ data burst with desired WRITE latency.

9. After write leveling, the DQ bus (internal $V_{REF(DQ)}$, DQS, and DQ) should be trained for high-speed operation using the MPC TRAINING commands and by issuing MRW commands to adjust $V_{REF(DQ)}$. The device will power-up with receivers configured for low-speed operations and with $V_{REF(DQ)}$ set to a default factory setting. Normal device operation at clock speeds higher than t_{CKb} should not be attempted until DQ bus training is complete. The MPC[READ DQ CALIBRATION] command is used together with MPC[READ-FIFO] or MPC[WRITE-FIFO] commands to train the DQ bus without disturbing the memory array contents. See the DQ Bus Training section for more information on the DQ bus training sequence.

10. At T_k , the device is ready for normal operation and is ready to accept any valid command. Any mode registers that have not previously been configured for normal operation should be written at this time.

Table 13: Initialization Timing Parameters

| Parameter | Min | Max | Unit | Comment |
|-------------|-----------|-----------|----------|---|
| t_{INIT0} | – | 20 | ms | Maximum voltage ramp time |
| t_{INIT1} | 200 | – | μ s | Minimum RESET_n LOW time after completion of voltage ramp |
| t_{INIT2} | 10 | – | ns | Minimum CKE LOW time before RESET_n goes HIGH |
| t_{INIT3} | 2 | – | ms | Minimum CKE LOW time after RESET_n goes HIGH |
| t_{INIT4} | 5 | – | t_{CK} | Minimum stable clock before first CKE HIGH |
| t_{INIT5} | 2 | – | μ s | Minimum idle time before first MRW/MRR command |
| t_{CKb} | Note 1, 2 | Note 1, 2 | ns | Clock cycle time during boot |

- Notes:
1. Minimum t_{CKb} guaranteed by DRAM test is 18ns.
 2. The system may boot at a higher frequency than dictated by minimum t_{CKb} . The higher boot frequency is system dependent.

Reset Initialization with Stable Power

The following sequence is required for RESET at no power interruption initialization.

1. Assert RESET_n below $0.2 \times V_{DD2}$ anytime when reset is needed. RESET_n needs to be maintained for minimum t_{PW_RESET} . CKE must be pulled LOW at least 10ns before de-asserting RESET_n.
2. Repeat steps 4–10 in Voltage Ramp section.


Table 14: Reset Timing Parameter

| Parameter | Value | | Unit | Comment |
|-----------------------|-------|-----|------|---|
| | Min | Max | | |
| ^t PW_RESET | 100 | – | ns | Minimum RESET_n LOW time for reset initialization with stable power |

Power-Off Sequence

Controlled Power-Off

While powering off, CKE must be held LOW ($\leq 0.2 \times V_{DD2}$); all other inputs must be between $V_{IL,min}$ and $V_{IH,max}$. The device outputs remain at High-Z while CKE is held LOW.

DQ, DMI, DQS_t, and DQS_c voltage levels must be between V_{SSQ} and V_{DDQ} during the power-off sequence to avoid latch-up. CK_t, CK_c, CS, and CA input levels must be between V_{SS} and V_{DD2} during the power-off sequence to avoid latch-up.

Tx is the point where any power supply drops below the minimum value specified in the minimum DC Operating Condition.

Tz is the point where all power supplies are below 300mV. After Tz, the device is powered off.

Table 15: Power Supply Conditions

The voltage difference between V_{SS} and V_{SSQ} must not exceed 100mV

| Between... | Applicable Conditions |
|------------|--|
| Tx and Tz | V_{DD1} must be greater than V_{DD2} |
| | V_{DD2} must be greater than $V_{DDQ} - 200mV$ |

Uncontrolled Power-Off

When an uncontrolled power-off occurs, the following conditions must be met.

- At Tx, when the power supply drops below the minimum values specified in the Recommended DC Operating Conditions table, all power supplies must be turned off and all power supply current capacity must be at zero, except for any static charge remaining in the system.
- After Tz (the point at which all power supplies first reach 300mV), the device must power off. During this period, the relative voltage between power supplies is uncontrolled. V_{DD1} and V_{DD2} must decrease with a slope lower than $0.5 V/\mu s$ between Tx and Tz.

An uncontrolled power-off sequence can occur a maximum of 400 times over the life of the device.


Table 16: Power-Off Timing

| Parameter | Symbol | Min | Max | Unit |
|---------------------|------------|-----|-----|------|
| Power-off ramp time | t_{POFF} | – | 2 | sec |

Mode Registers

Mode Register Assignments and Definitions

Mode register definitions are provided in the Mode Register Assignments table. In the access column of the table, R indicates read-only; W indicates write-only; R/W indicates read- or write-capable or enabled. The MRR command is used to read from a register. The MRW command is used to write to a register.

Table 17: Mode Register Assignments

Notes 1–5 apply to entire table

| MR# | MA[5:0] | Function | Access | OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 | Link |
|-----|---------|----------------------|--------|---|----------------|---------------|----------|--------------|--------|--------|-----------|------------|
| 0 | 00h | Device info | R | CATR | RFU | RFU | RZQI | | RFU | REF | | Go to MR0 |
| 1 | 01h | Device feature 1 | W | RD-PST | nWR (for AP) | | | RD-PRE | WR-PRE | BL | | Go to MR1 |
| 2 | 02h | Device feature 2 | W | WR Lev | WLS | WL | | RL | | | Go to MR2 | |
| 3 | 03h | I/O config-1 | W | DBI-WR | DBI-RD | PDDS | | | PPRP | WR-PST | PU-CAL | Go to MR3 |
| 4 | 04h | Refresh and training | R/W | TUF | Thermal offset | PPRE | SR abort | Refresh rate | | | Go to MR4 | |
| 5 | 05h | Basic config-1 | R | Manufacturer ID | | | | | | | | Go to MR5 |
| 6 | 06h | Basic config-2 | R | Revision ID1 | | | | | | | | Go to MR6 |
| 7 | 07h | Basic config-3 | R | Revision ID2 | | | | | | | | Go to MR7 |
| 8 | 08h | Basic config-4 | R | I/O width | Density | | | Type | | | Go to MR8 | |
| 9 | 09h | Test mode | W | Vendor-specific test mode | | | | | | | | Go to MR9 |
| 10 | 0Ah | I/O calibration | W | RFU | | | | | | | ZQ RST | Go to MR10 |
| 11 | 0Bh | ODT | W | RFU | CA ODT | | | RFU | DQ ODT | | | Go to MR11 |
| 12 | 0Ch | $V_{REF(CA)}$ | R/W | RFU | VR_{CA} | $V_{REF(CA)}$ | | | | | | Go to MR12 |
| 13 | 0Dh | Register control | W | FSP-OP | FSP-WR | DMD | RRO | VRCG | VRO | RPT | CBT | Go to MR13 |
| 14 | 0Eh | $V_{REF(DQ)}$ | R/W | RFU | VR_{DQ} | $V_{REF(DQ)}$ | | | | | | Go to MR14 |
| 15 | 0Fh | DQI-LB | W | Lower-byte invert register for DQ calibration | | | | | | | | Go to MR15 |
| 16 | 10h | PASR_Bank | W | PASR bank mask | | | | | | | | Go to MR16 |
| 17 | 11h | PASR_Seg | W | PASR segment mask | | | | | | | | Go to MR17 |
| 18 | 12h | IT-LSB | R | DQS oscillator count – LSB | | | | | | | | Go to MR18 |
| 19 | 13h | IT-MSB | R | DQS oscillator count – MSB | | | | | | | | Go to MR19 |
| 20 | 14h | DQI-UB | W | Upper-byte invert register for DQ calibration | | | | | | | | Go to MR20 |
| 21 | 15h | Vendor use | W | RFU | | | | | | | | Go to MR21 |


Table 17: Mode Register Assignments (Continued)

Notes 1–5 apply to entire table

| MR# | MA[5:0] | Function | Access | OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 | Link |
|-------|---------|--------------------------|--------|---------------------------------|--------------|---------|---------|-----------|-----------|-----|-----|------------|
| 22 | 16h | ODT feature 2 | W | RFU | | ODTD-CA | ODTE-CS | ODTE-CK | SoC ODT | | | Go to MR22 |
| 23 | 17h | DQS oscillator stop | W | DQS oscillator run-time setting | | | | | | | | Go to MR23 |
| 24 | 18h | TRR control | R/W | TRR mode | TRR mode BAn | | | Unltd MAC | MAC value | | | Go to MR24 |
| 25 | 19h | PPR resources | R | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | Go to MR25 |
| 26–31 | 1Ah~1Fh | – | – | Reserved for future use | | | | | | | | |
| 32 | 20h | DQ calibration pattern A | W | See DQ calibration section | | | | | | | | Go to MR32 |
| 33–39 | 21h~27h | Do not use | – | Do not use | | | | | | | | |
| 40 | 28h | DQ calibration pattern B | W | See DQ calibration section | | | | | | | | Go to MR40 |
| 41–47 | 29h~2Fh | Do not use | – | Do not use | | | | | | | | |
| 48–63 | 30h~3Fh | Reserved | – | Reserved for future use | | | | | | | | |

- Notes:
1. RFU bits must be set to 0 during MRW commands.
 2. RFU bits are read as 0 during MRR commands.
 3. All mode registers that are specified as RFU or write-only shall return undefined data when read via an MRR command.
 4. RFU mode registers must not be written.
 5. Writes to read-only registers will not affect the functionality of the device.

Table 18: MR0 Device Feature 0 (MA[5:0] = 00h)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|------|-----|-----|------|-----|-----|-----|-----|
| CATR | RFU | | RZQI | | RFU | | REF |

Table 19: MR0 Op-Code Bit Definitions

| Register Information | Tag | Type | OP | Definition | Notes |
|--|------|-----------|---------|---|-------|
| Refresh mode | REF | Read only | OP[0] | 0b: Both legacy and modified refresh mode supported 1b: Only modified refresh mode supported | |
| Built-in self-test for RZQ information | RZQI | Read only | OP[4:3] | 00b: RZQ self-test not supported 01b: ZQ may connect to V _{SSQ} or float 10b: ZQ may short to V _{DDQ} 11b: ZQ pin self-test completed, no error condition detected (ZQ may not connect to V _{SSQ} , float, or short to V _{DDQ}) | 1–4 |


Table 19: MR0 Op-Code Bit Definitions (Continued)

| Register Information | Tag | Type | OP | Definition | Notes |
|----------------------|------|-----------|-------|--|-------|
| CA terminating rank | CATR | Read only | OP[7] | 0b: CA for this rank is not terminated 1b: CA for this rank is terminated | |

- Notes:
1. RZQI, if supported, will be set upon completion of MPC[ZQCAL START] command. (^tZQCAL after MPC[ZQCAL START] command.) RZQI value will be lost after reset.
 2. If ZQ is connected to V_{SSQ} to set default calibration, OP[4:3] must be set to 01b. If ZQ is not connected to V_{SSQ}, either OP[4:3] = 01b or OP[4:3] = 10b might indicate a ZQ pin assembly error. It is recommended that the assembly error be corrected.
 3. In the case of possible assembly error, the device will default to factory trim settings for R_{ON}, and will ignore ZQ CALIBRATION commands. In either case, the device may not function as intended.
 4. If the ZQ pin self-test returns OP[4:3] = 11b, the device has detected a resistor connected to the ZQ pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor meets the specified limits (that is, 240Ω ±1%).

Table 20: MR1 Device Feature 1 (MA[5:0] = 01h)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|--------|--------------|-----|-----|--------|--------|-----|-----|
| RD-PST | nWR (for AP) | | | RD-PRE | WR-PRE | BL | |

Table 21: MR1 Op-Code Bit Definitions

| Feature | Type | OP | Definition | Notes |
|--|------------|---------|---|---------|
| BL Burst length | Write only | OP[1:0] | 00b: BL = 16 sequential (default) 01b: BL = 32 sequential 10b: BL = 16 or 32 sequential (on-the-fly) 11b: Reserved | 1, 5, 6 |
| WR-PRE Write preamble length | Write only | OP[2] | 0b: Reserved 1b: WR preamble = 2 × ^t CK | 5, 6 |
| RD-PRE Read preamble type | Write only | OP[3] | 0b: RD preamble = Static (default) 1b: RD preamble = Toggle | 3, 5, 6 |
| nWR Write-recovery for auto-precharge command | Write only | OP[6:4] | 000b: nWR = 6 (default) 001b: nWR = 10 010b: nWR = 16 011b: nWR = 20 100b: nWR = 24 101b: nWR = 30 110b: nWR = 34 111b: nWR = 40 | 2, 5, 6 |


Table 21: MR1 Op-Code Bit Definitions (Continued)

| Feature | Type | OP | Definition | Notes |
|---------------------------------|---------------|-------|--|---------|
| RD-PST Read postamble length | Write only | OP[7] | 0b: RD postamble = $0.5 \times t_{CK}$ (default) 1b: RD postamble = $1.5 \times t_{CK}$ | 4, 5, 6 |

- Notes:
1. Burst length on-the-fly can be set to either BL = 16 or BL = 32 by setting the BL bit in the command operands. See the Command Truth Table.
 2. The programmed value of nWR is the number of clock cycles the device uses to determine the starting point of an internal precharge after a write burst with auto precharge (AP) enabled. See Frequency Ranges for RL, WL, and nWR Settings table.
 3. For READ operations, this bit must be set to select between a toggling preamble and a non-toggling preamble. (See the Preamble section.)
 4. OP[7] provides an optional READ postamble with an additional rising and falling edge of DQS_t. The optional postamble cycle is provided for the benefit of certain memory controllers.
 5. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address.
 6. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, that is, the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.

Table 22: Burst Sequence for Read

| C4 | C3 | C2 | C1 | C0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | | | |
|------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--|--|--|
| 16-Bit READ Operation | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | 0 | 0 | 0 | 0 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F | | | | | | | | | | | | | | | | | | | |
| V | 0 | 1 | 0 | 0 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F | 0 | 1 | 2 | 3 | | | | | | | | | | | | | | | | | | | |
| V | 1 | 0 | 0 | 0 | 8 | 9 | A | B | C | D | E | F | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | | | | | | | | | | | | | | | | | | | |
| V | 1 | 1 | 0 | 0 | C | D | E | F | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | | | | | | | | | | | | | | | | | | | |
| 32-Bit READ Operation | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F | | | |
| 0 | 0 | 1 | 0 | 0 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F | 0 | 1 | 2 | 3 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F | 10 | 11 | 12 | 13 | | | |
| 0 | 1 | 0 | 0 | 0 | 8 | 9 | A | B | C | D | E | F | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | | | |
| 0 | 1 | 1 | 0 | 0 | C | D | E | F | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | 1C | 1D | 1E | 1F | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | | | |
| 1 | 0 | 0 | 0 | 0 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F | | | |
| 1 | 0 | 1 | 0 | 0 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F | 10 | 11 | 12 | 13 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F | 0 | 1 | 2 | 3 | | | |
| 1 | 1 | 0 | 0 | 0 | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 8 | 9 | A | B | C | D | E | F | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | | | |
| 1 | 1 | 1 | 0 | 0 | 1C | 1D | 1E | 1F | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | C | D | E | F | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | | | |

- Notes:
1. C[1:0] are not present on the CA bus; they are implied to be zero.
 2. The starting burst address is on 64-bit (4n) boundaries.

Table 23: Burst Sequence for Write

| C4 | C3 | C2 | C1 | C0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | | | |
|-------------------------------|----|----|----|----|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|--|--|--|
| 16-Bit WRITE Operation | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V | 0 | 0 | 0 | 0 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F | | | | | | | | | | | | | | | | | | | |
| 32-Bit WRITE Operation | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F | | | |

- Notes:
1. C[1:0] are not present on the CA bus; they are implied to be zero.
 2. The starting burst address is on 256-bit (16n) boundaries for burst length 16.
 3. The starting burst address is on 512-bit (32n) boundaries for burst length 32.
 4. C[3:2] must be set to 0 for all WRITE operations.



Table 24: MR2 Device Feature 2 (MA[5:0] = 02h)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|--------|-----|-----|-----|-----|-----|-----|-----|
| WR Lev | WLS | WL | | | RL | | |

Table 25: MR2 Op-Code Bit Definitions

| Feature | Type | OP | Definition | Notes |
|--------------------|----------------|---------|---|---------|
| RL READ latency | Write- only | OP[2:0] | RL and <i>n</i> RTP for DBI-RD disabled (MR3 OP[6] = 0b) 000b: RL = 6, <i>n</i> RTP = 8 (default) 001b: RL = 10, <i>n</i> RTP = 8 010b: RL = 14, <i>n</i> RTP = 8 011b: RL = 20, <i>n</i> RTP = 8 100b: RL = 24, <i>n</i> RTP = 10 101b: RL = 28, <i>n</i> RTP = 12 110b: RL = 32, <i>n</i> RTP = 14 111b: RL = 36, <i>n</i> RTP = 16 | 1, 3, 4 |
| | | | RL and <i>n</i> RTP for DBI-RD enabled (MR3 OP[6] = 1b) 000b: RL = 6, <i>n</i> RTP = 8 001b: RL = 12, <i>n</i> RTP = 8 010b: RL = 16, <i>n</i> RTP = 8 011b: RL = 22, <i>n</i> RTP = 8 100b: RL = 28, <i>n</i> RTP = 10 101b: RL = 32, <i>n</i> RTP = 12 110b: RL = 36, <i>n</i> RTP = 14 111b: RL = 40, <i>n</i> RTP = 16 | |


Table 25: MR2 Op-Code Bit Definitions (Continued)

| Feature | Type | OP | Definition | Notes |
|-----------------------------|----------------|---------|---|---------|
| WL WRITE latency | Write- only | OP[5:3] | WL set A (MR2 OP[6] = 0b) 000b: WL = 4 (default) 001b: WL = 6 010b: WL = 8 011b: WL = 10 100b: WL = 12 101b: WL = 14 110b: WL = 16 111b: WL = 18 <hr/> WL set B (MR2 OP[6] = 1b) 000b: WL = 4 001b: WL = 8 010b: WL = 12 011b: WL = 18 100b: WL = 22 101b: WL = 26 110b: WL = 30 111b: WL = 34 | 1, 3, 4 |
| WLS WRITE latency set | Write- only | OP[6] | 0b: Use WL set A (default) 1b: Use WL set B | 1, 3, 4 |
| WR Lev Write leveling | Write- only | OP[7] | 0b: Disable write leveling (default) 1b: Enable write leveling | 2 |

- Notes:
1. See Latency Code Frequency Table for allowable frequency ranges for RL/WL/nWR.
 2. After an MRW command to set the write leveling enable bit (OP[7] = 1b), the device remains in the MRW state until another MRW command clears the bit (OP[7] = 0b). No other commands are allowed until the write leveling enable bit is cleared.
 3. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command this MR address, or read from with an MRR command to this address.
 4. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, that is, the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.
 5. nRTP is valid for BL16 only. For BL32, the SDRAM will add 8 clocks to the nRTP value before starting a precharge.


Table 26: Frequency Ranges for RL, WL, *n*WR, and *n*RTP Settings

| READ Latency | | WRITE Latency | | <i>n</i> WR | <i>n</i> RTP | Lower Frequency Limit (>) | Upper Frequency Limit (≤) | Units | Notes |
|--------------|-------|---------------|-------|-------------|--------------|---------------------------|---------------------------|-------|-------|
| No DBI | w/DBI | Set A | Set B | | | | | | |
| 6 | 6 | 4 | 4 | 6 | 8 | 10 | 266 | MHz | 1–6 |
| 10 | 12 | 6 | 8 | 10 | 8 | 266 | 533 | | |
| 14 | 16 | 8 | 12 | 16 | 8 | 533 | 800 | | |
| 20 | 22 | 10 | 18 | 20 | 8 | 800 | 1066 | | |
| 24 | 28 | 12 | 22 | 24 | 10 | 1066 | 1333 | | |
| 28 | 32 | 14 | 26 | 30 | 12 | 1333 | 1600 | | |
| 32 | 36 | 16 | 30 | 34 | 14 | 1600 | 1866 | | |
| 36 | 40 | 18 | 34 | 40 | 16 | 1866 | 2133 | | |

- Notes:
1. The device should not be operated at a frequency above the upper frequency limit or below the lower frequency limit shown for each RL, WL, or *n*WR value.
 2. DBI for READ operations is enabled in MR3 OP[6]. When MR3 OP[6] = 0, then the "No DBI" column should be used for READ latency. When MR3 OP[6] = 1, then the "w/DBI" column should be used for READ latency.
 3. WRITE latency set A and set B are determined by MR2 OP[6]. When MR2 OP[6] = 0, then WRITE latency set A should be used. When MR2 OP[6] = 1, then WRITE latency set B should be used.
 4. The programmed value for *n*RTP is the number of clock cycles the device uses to determine the starting point of an internal PRECHARGE operation after a READ burst with AP (auto precharge) enabled. It is determined by $RU^{(tRTP/tCK)}$.
 5. The programmed value of *n*WR is the number of clock cycles the device uses to determine the starting point of an internal PRECHARGE operation after a WRITE burst with AP (auto precharge) enabled. It is determined by $RU^{(tWR/tCK)}$.
 6. *n*RTP shown in this table is valid for BL16 only. For BL32, the device will add 8 clocks to the *n*RTP value before starting a precharge.

Table 27: MR3 I/O Configuration 1 (MA[5:0] = 03h)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|--------|--------|------|-----|-----|------|--------|--------|
| DBI-WR | DBI-RD | PDDS | | | PPRP | WR-PST | PU-CAL |


Table 28: MR3 Op-Code Bit Definitions

| Feature | Type | OP | Definition | Notes |
|---------------------------------------|------------|---------|---|---------|
| PU-CAL (Pull-up calibration point) | Write-only | OP[0] | 0b: $V_{DDQ}/2.5$ 1b: $V_{DDQ}/3$ (default) | 1–4 |
| WR-PST (WR postamble length) | | OP[1] | 0b: WR postamble = $0.5 \times t_{CK}$ (default) 1b: WR postamble = $1.5 \times t_{CK}$ | 2, 3, 5 |
| PPRP (Post-package repair protection) | | OP[2] | 0b: PPR protection disabled (default) 1b: PPR protection enabled | 6 |
| PDDS (Pull-down drive strength) | | OP[5:3] | 000b: RFU 001b: $R_{ZQ}/1$ 010b: $R_{ZQ}/2$ 011b: $R_{ZQ}/3$ 100b: $R_{ZQ}/4$ 101b: $R_{ZQ}/5$ 110b: $R_{ZQ}/6$ (default) 111b: Reserved | 1, 2, 3 |
| DBI-RD (DBI-read enable) | | OP[6] | 0b: Disabled (default) 1b: Enabled | 2, 3 |
| DBI-WR (DBI-write enable) | | OP[7] | 0b: Disabled (default) 1b: Enabled | 2, 3 |

- Notes:
1. All values are typical. The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Recalibration may be required as voltage and temperature vary.
 2. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
 3. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.
 4. For dual-channel device, PU-CAL (MR3-OP[0]) must be set the same for both channels on a die. The SDRAM will read the value of only one register (Ch.A or Ch.B), the choice is vendor-specific, so both channels must be set the same.
 5. Refer to the supplier data sheet for vendor-specific function. $1.5 \times t_{CK}$ apply $> 1.6\text{GHz}$ clock.
 6. If MR3 OP[2] is set to 1b, PPR protection mode is enabled. The PPR protection bit is a sticky bit and can only be set to 0b by a power on reset. MR4 OP[4] controls entry to PPR mode. If PPR protection is enabled then the DRAM will not allow writing of 1b to MR4 OP[4].


Table 29: MR4 Device Temperature (MA[5:0] = 04h)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|-----|----------------|-----|------|----------|--------------|-----|-----|
| TUF | Thermal offset | | PPRE | SR abort | Refresh rate | | |

Table 30: MR4 Op-Code Bit Definitions

| Feature | Type | OP | Definition | Notes |
|---|-----------|---------|---|-------------|
| Refresh rate | Read-only | OP[2:0] | 000b: SDRAM low temperature operating limit exceeded 001b: 4x refresh 010b: 2x refresh 011b: 1x refresh (default) 100b: 0.5x refresh 101b: 0.25x refresh, no derating 110b: 0.25x refresh, with derating 111b: SDRAM high temperature operating limit exceeded | 1–4, 7–9 |
| SR abort (Self Refresh Abort) | Write | OP[3] | 0b: Disable (default) 1b: Device dependent | 9 |
| PPRE (Post-package repair entry/exit) | Write | OP[4] | 0b: Exit PPR mode (default) 1b: Enter PPR mode (Reference MR25 OP[7:0] for available PPR resources) | 5, 9 |
| Thermal Offset-Control-ler offset to TCSR | Write | OP[6:5] | 00b: No offset, 0~5°C gradient (default) 01b: 5°C offset, 5~10°C gradient 10b: 10°C offset, 10~15°C gradient 11b: Reserved | 9 |
| TUF (Temperature update flag) | Read-only | OP7 | 0b: OP[2:0] No change in OP[2:0] since last MR4 read (default) 1b: Change in OP[2:0] since last MR4 read | 6–8 |

- Notes:
1. The refresh rate for each MR4 OP[2:0] setting applies to t_{REFI} , t_{REFIpb} , and t_{REFW} . MR4 OP[2:0] = 011b corresponds to a device temperature of 85°C. Other values require either a longer (2x, 4x) refresh interval at lower temperatures or a shorter (0.5x, 0.25x) refresh interval at higher temperatures. If MR4 OP[2] = 1b, the device temperature is greater than 85°C.
 2. At higher temperatures (>85°C), AC timing derating may be required. If derating is required the device will set MR4 OP[2:0] = 110b. See derating timing requirements in the AC Timing section.
 3. DRAM vendors may or may not report all of the possible settings over the operating temperature range of the device. Each vendor guarantees that their device will work at any temperature within the range using the refresh interval requested by their device.
 4. The device may not operate properly when MR4 OP[2:0] = 000b or 111b.
 5. Post-package repair can be entered or exited by writing to MR4 OP[4].
 6. When MR4 OP[7] = 1b, the refresh rate reported in MR4 OP[2:0] has changed since the last MR4 read. A mode register read from MR4 will reset MR4 OP[7] to 0b.
 7. MR4 OP[7] = 0b at power-up. MR4 OP[2:0] bits are undefined at power-up.



8. See the Temperature Sensor section for information on the recommended frequency of reading MR4.
9. MR4 OP[6:3] can be written in this register. All other bits will be ignored by the device during an MRW command to this register.

Table 31: MR5 Basic Configuration 1 (MA[5:0] = 05h)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|-----------------|-----|-----|-----|-----|-----|-----|-----|
| Manufacturer ID | | | | | | | |

Table 32: MR5 Op-Code Bit Definitions

| Feature | Type | OP | Definition |
|-----------------|-----------|---------|---|
| Manufacturer ID | Read-only | OP[7:0] | 1111 1111b : Micron All others: Reserved |

Table 33: MR6 Basic Configuration 2 (MA[5:0] = 06h)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|--------------|-----|-----|-----|-----|-----|-----|-----|
| Revision ID1 | | | | | | | |

Note: 1. MR6 is vendor-specific.

Table 34: MR6 Op-Code Bit Definitions

| Feature | Type | OP | Definition |
|--------------|-----------|---------|--------------------------|
| Revision ID1 | Read-only | OP[7:0] | xxxx xxxxb: Revision ID1 |

Note: 1. MR6 is vendor-specific.

Table 35: MR7 Basic Configuration 3 (MA[5:0] = 07h)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|--------------|-----|-----|-----|-----|-----|-----|-----|
| Revision ID2 | | | | | | | |

Table 36: MR7 Op-Code Bit Definitions

| Feature | Type | OP | Definition |
|--------------|-----------|---------|--------------------------|
| Revision ID2 | Read-only | OP[7:0] | xxxx xxxxb: Revision ID2 |

Note: 1. MR7 is vendor-specific.


Table 37: MR8 Basic Configuration 4 (MA[5:0] = 08h)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|-----------|-----|---------|-----|-----|-----|------|-----|
| I/O width | | Density | | | | Type | |

Table 38: MR8 Op-Code Bit Definitions

| Feature | Type | OP | Definition |
|-----------|-----------|---------|---|
| Type | Read-only | OP[1:0] | 00b: S16 SDRAM (16n prefetch) All others: Reserved |
| Density | Read-only | OP[5:2] | 0000b: 4Gb per die (2Gb per channel) 0001b: 6Gb per die (3Gb per channel) 0010b: 8Gb per die (4Gb per channel) or 4Gb per die (4Gb per channel) 0011b: 12Gb per die (6Gb per channel) or 6Gb per die (6Gb per channel) 0100b: 16Gb per die (8Gb per channel) or 8Gb per die (8Gb per channel) 0101b: 24Gb per die (12Gb per channel) 0110b: 32Gb per die (16Gb per channel) All others: Reserved |
| I/O width | Read-only | OP[7:6] | 00b: x16/channel All others: Reserved |

Table 39: MR9 Test Mode (MA[5:0] = 09h)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---------------------------|-----|-----|-----|-----|-----|-----|-----|
| Vendor-specific test mode | | | | | | | |

Table 40: MR9 Op-Code Definitions

| Feature | Type | OP | Definition |
|-----------|------------|---------|--|
| Test mode | Write-only | OP[7:0] | 0000000b; Vendor-specific test mode disabled (default) |

Table 41: MR10 Calibration (MA[5:0] = 0Ah)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|-----|-----|-----|-----|-----|-----|-----|----------|
| RFU | | | | | | | ZQ RESET |



Table 42: MR10 Op-Code Bit Definitions

| Feature | Type | OP | Definition |
|----------|------------|-------|--|
| ZQ reset | Write-only | OP[0] | 0b: Normal operation (default) 1b: ZQ reset |

- Notes:
1. See AC Timing table for calibration latency and timing.
 2. If ZQ is connected to V_{DDQ} through R_{ZQ} , either the ZQ CALIBRATION function or default calibration (via ZQ reset) is supported. If ZQ is connected to V_{SS} , the device operates with default calibration and ZQ CALIBRATION commands are ignored. In both cases, the ZQ connection must not change after power is supplied to the device.

Table 43: MR11 ODT Control (MA[5:0] = 0Bh)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|-----|--------|-----|-----|-----|--------|-----|-----|
| RFU | CA ODT | | | RFU | DQ ODT | | |

Table 44: MR11 Op-Code Bit Definitions

Notes 1-3 apply to entire table

| Feature | Type | OP | Definition |
|--|------------|---------|--|
| DQ ODT DQ bus receiver on-die termination | Write-only | OP[2:0] | 000b: Disable (default) 001b: RZQ/1 010b: RZQ/2 011b: RZQ/3 100b: RZQ/4 101b: RZQ/5 110b: RZQ/6 111b: RFU |
| CA ODT CA bus receiver on-die termination | Write-only | OP[6:4] | 000b: Disable (default) 001b: RZQ/1 010b: RZQ/2 011b: RZQ/3 100b: RZQ/4 101b: RZQ/5 110b: RZQ/6 111b: RFU |

- Notes:
1. All values are typical. The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Re-calibration may be required as voltage and temperature vary.
 2. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.



- There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.

Table 45: MR12 Register Information (MA[5:0] = 0Ch)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|-----|------------------|----------------------|-----|-----|-----|-----|-----|
| RFU | VR _{CA} | V _{REF(CA)} | | | | | |

Table 46: MR12 Op-Code Bit Definitions

| Feature | Type | OP | Data | Notes |
|---|----------------|---------|--|------------------|
| V _{REF(CA)} V _{REF(CA)} settings | Read/ Write | OP[5:0] | 000000b–110010b: See V _{REF} Settings Table All others: Reserved | 1–3, 5, 6 |
| VR _{CA} V _{REF(CA)} range | Read/ Write | OP[6] | 0b: V _{REF(CA)} range[0] enabled 1b: V _{REF(CA)} range[1] enabled (default) | 1, 2, 4, 5, 6 |

- Notes:
- This register controls the V_{REF(CA)} levels for frequency set point[1:0]. Values from either VR(ca)[0] or VR(ca)[1] may be selected by setting MR12 OP[6] appropriately.
 - A read to MR12 places the contents of OP[7:0] on DQ[7:0]. Any RFU bits and unused DQ will be set to 0. See the MRR Operation section.
 - A write to MR12 OP[5:0] sets the internal V_{REF(CA)} level for FSP[0] when MR13 OP[6] = 0b or sets the internal V_{REF(CA)} level for FSP[1] when MR13 OP[6] = 1b. The time required for V_{REF(CA)} to reach the set level depends on the step size from the current level to the new level. See the V_{REF(CA)} training section.
 - A write to MR12 OP[6] switches the device between two internal V_{REF(CA)} ranges. The range (range[0] or range[1]) must be selected when setting the V_{REF(CA)} register. The value, once set, will be retained until overwritten or until the next power-on or reset event.
 - There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
 - There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

Table 47: MR13 Register Control (MA[5:0] = 0Dh)

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|--------|--------|-------|-------|-------|-------|-------|-------|
| FSP-OP | FSP-WR | DMD | RRO | VRCG | VRO | RPT | CBT |


Table 48: MR13 Op-Code Bit Definition

| Feature | Type | OP | Definition | Notes |
|--|------------|-------|--|-------|
| CBT Command bus training | Write-only | OP[0] | 0b: Normal operation (default) 1b: Command bus training mode enabled | 1 |
| RPT Read preamble training | | OP[1] | 0b: Disabled (default) 1b: Read preamble training mode enabled | |
| VRO V_{REF} output | | OP[2] | 0b: Normal operation (default) 1b: Output the $V_{REF(CA)}$ and $V_{REF(DQ)}$ values on DQ bits | 2 |
| VRCG V_{REF} current generator | | OP[3] | 0b: Normal operation (default) 1b: Fast response (high current) mode | 3 |
| RRO Refresh rate option | | OP[4] | 0b: Disable MR4 OP[2:0] (default) 1b: Enable MR4 OP[2:0] | 4, 5 |
| DMD Data mask disable | | OP[5] | 0b: DATA MASK operation enabled (default) 1b: DATA MASK operation disabled | 6 |
| FSP-WR Frequency set point write / read | | OP[6] | 0b: Frequency set point[0] (default) 1b: Frequency set point[1] | 7 |
| FSP-OP Frequency set point operation mode | | OP[7] | 0b: Frequency set point[0] (default) 1b: Frequency set point[1] | 8 |

- Notes:
1. A write to set OP[0] = 1 causes the LPDDR4-SDRAM to enter the Command Bus Training mode. When OP[0] = 1 and CKE goes LOW, commands are ignored and the contents of CA[5:0] are mapped to the DQ bus. CKE must be brought HIGH before doing a MRW to clear this bit (OP[0] = 0) and return to normal operation. See the Command Bus Training section for more information.
 2. When set, the device will output the $V_{REF(CA)}$ and $V_{REF(DQ)}$ voltage on DQ pins. Only the "active" frequency set point, as defined by MR13 OP[7], will be output on the DQ pins. This function allows an external test system to measure the internal V_{REF} levels. The DQ pins used for V_{REF} output are vendor-specific.
 3. When OP[3] = 1, the V_{REF} circuit uses a high current mode to improve V_{REF} settling time.
 4. MR13 OP[4] RRO bit is valid only when MR0 OP[0] = 1. For LPDDR4-SDRAM with MR0 OP[0] = 0, MR4 OP[2:0] bits are not dependent on MR13 OP[4].
 5. When OP[4] = 0, only 001b and 010b in MR4 OP[2:0] are disabled. LPDDR4-SDRAM must report 011b instead of 001b or 010b in this case. Controller should follow the refresh mode reported by MR4 OP[2:0], regardless of RRO setting. TCSR function does not depend on RRO setting.
 6. When enabled (OP[5] = 0b) data masking is enabled for the device. When disabled (OP[5] = 1b), the device will ignore any mask patterns issued during a MASKED WRITE command. See the Data Mask section for more information.
 7. FSP-WR determines which frequency set point registers are accessed with MRW and MRR commands for the following functions such as $V_{REF(CA)}$ setting, $V_{REF(CA)}$ range, $V_{REF(DQ)}$ setting, $V_{REF(DQ)}$ range. For more information, refer to Frequency Set Point section.
 8. FSP-OP determines which frequency set point register values are currently used to specify device operation for the following functions such as $V_{REF(CA)}$ setting, $V_{REF(CA)}$ range, $V_{REF(DQ)}$ setting, $V_{REF(DQ)}$ range. For more information, refer to Frequency Set Point section.


Table 49: Mode Register14 (MA[5:0] = 0Eh)

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|-------|------------------|----------------------|-------|-------|-------|-------|-------|
| RFU | VR _{DQ} | V _{REF(DQ)} | | | | | |

Table 50: MR14 Op-Code Bit Definition

| Feature | Type | OP | Definition | Notes |
|--|----------------|---------|--|-----------|
| V _{REF(DQ)} V _{REF(DQ)} setting | Read/ Write | OP[5:0] | 000000b–110010b: See V _{REF} Settings Table All others: Reserved | 1–3, 5, 6 |
| VR _{DQ} V _{REF(DQ)} range | | OP[6] | 0b: V _{REF(DQ)} range[0] enabled 1b: V _{REF(DQ)} range[1] enabled (default) | 1, 2, 4–6 |

- Notes:
1. This register controls the V_{REF(DQ)} levels for frequency set point[1:0]. Values from either VR_{DQ}[0] (vendor defined) or VR_{DQ}[1] (vendor defined) may be selected by setting OP[6] appropriately.
 2. A read (MRR) to this register places the contents of OP[7:0] on DQ[7:0]. Any RFU bits and unused DQ shall be set to 0. See the MRR Operation section.
 3. A write to OP[5:0] sets the internal V_{REF(DQ)} level for FSP[0] when MR13 OP[6] = 0b, or sets FSP[1] when MR13 OP[6] = 1b. The time required for V_{REF(DQ)} to reach the set level depends on the step size from the current level to the new level. See the V_{REF(DQ)} training section.
 4. A write to OP[6] switches the device between two internal V_{REF(DQ)} ranges. The range (range[0] or range[1]) must be selected when setting the V_{REF(DQ)} register. The value, once set, will be retained until overwritten, or until the next power-on or reset event.
 5. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
 6. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.



Table 51: V_{REF} Setting for Range[0] and Range[1]

Notes 1–3 apply to entire table.

| Function | OP | Range[0] Values | | Range[1] Values | |
|--|----------------------|---|----------------------|---|----------------|
| | | V _{REF(CA)} (% of V _{DD2}) | | V _{REF(CA)} (% of V _{DD2}) | |
| | | V _{REF(DQ)} (% of V _{DDQ}) | | V _{REF(DQ)} (% of V _{DDQ}) | |
| V _{REF} Setting for MR12 and MR14 | OP[5:0] | 000000b: 10.0% | 011010b: 20.4% | 000000b: 22.0% | 011010b: 32.4% |
| | | 000001b: 10.4% | 011011b: 20.8% | 000001b: 22.4% | 011011b: 32.8% |
| | | 000010b: 10.8% | 011100b: 21.2% | 000010b: 22.8% | 011100b: 33.2% |
| | | 000011b: 11.2% | 011101b: 21.6% | 000011b: 23.2% | 011101b: 33.6% |
| | | 000100b: 11.6% | 011110b: 22.0% | 000100b: 23.6% | 011110b: 34.0% |
| | | 000101b: 12.0% | 011111b: 22.4% | 000101b: 24.0% | 011111b: 34.4% |
| | | 000110b: 12.4% | 100000b: 22.8% | 000110b: 24.4% | 100000b: 34.8% |
| | | 000111b: 12.8% | 100001b: 23.2% | 000111b: 24.8% | 100001b: 35.2% |
| | | 001000b: 13.2% | 100010b: 23.6% | 001000b: 25.2% | 100010b: 35.6% |
| | | 001001b: 13.6% | 100011b: 24.0% | 001001b: 25.6% | 100011b: 36.0% |
| | | 001010b: 14.0% | 100100b: 24.4% | 001010b: 26.0% | 100100b: 36.4% |
| | | 001011b: 14.4% | 100101b: 24.8% | 001011b: 26.4% | 100101b: 36.8% |
| | | 001100b: 14.8% | 100110b: 25.2% | 001100b: 26.8% | 100110b: 37.2% |
| | | 001101b: 15.2% | 100111b: 25.6% | 001101b: 27.2% default | 100111b: 37.6% |
| | | 001110b: 15.6% | 101000b: 26.0% | 001110b: 27.6% | 101000b: 38.0% |
| | | 001111b: 16.0% | 101001b: 26.4% | 001111b: 28.0% | 101001b: 38.4% |
| | | 010000b: 16.4% | 101010b: 26.8% | 010000b: 28.4% | 101010b: 38.8% |
| | | 010001b: 16.8% | 101011b: 27.2% | 010001b: 28.8% | 101011b: 39.2% |
| | | 010010b: 17.2% | 101100b: 27.6% | 010010b: 29.2% | 101100b: 39.6% |
| | | 010011b: 17.6% | 101101b: 28.0% | 010011b: 29.6% | 101101b: 40.0% |
| 010100b: 18.0% | 101110b: 28.4% | 010100b: 30.0% | 101110b: 40.4% | | |
| 010101b: 18.4% | 101111b: 28.8% | 010101b: 30.4% | 101111b: 40.8% | | |
| 010110b: 18.8% | 110000b: 29.2% | 010110b: 30.8% | 110000b: 41.2% | | |
| 010111b: 19.2% | 110001b: 29.6% | 010111b: 31.2% | 110001b: 41.6% | | |
| 011000b: 19.6% | 110010b: 30.0% | 011000b: 31.6% | 110010b: 42.0% | | |
| 011001b: 20.0% | All Others: Reserved | 011001b: 32.0% | All Others: Reserved | | |

- Notes:
1. These values may be used for MR14 OP[5:0] and MR12 OP[5:0] to set the V_{REF(CA)} or V_{REF(DQ)} levels in the device.
 2. The range may be selected in each of the MR14 or MR12 registers by setting OP[6] appropriately.
 3. Each of the MR14 or MR12 registers represents either FSP[0] or FSP[1]. Two frequency set points each for CA and DQ are provided to allow for faster switching between terminated and un-terminated operation or between different high-frequency settings, which may use different terminations values.


Table 52: MR15 Register Information (MA[5:0] = 0Fh)

| OP[7] | OP[6] | OP[5] | OP[4] | OP[3] | OP[2] | OP[1] | OP[0] |
|---|-------|-------|-------|-------|-------|-------|-------|
| Lower-byte invert register for DQ calibration | | | | | | | |

Table 53: MR15 Op-code Bit Definition

| Feature | Type | OP | Definition | Notes |
|--------------------------------------|------------|---------|---|-------|
| Lower-byte invert for DQ calibration | Write-only | OP[7:0] | The following values may be written for any operand OP[7:0] and will be applied to the corresponding DQ locations DQ[7:0] within a byte lane 0b: Do not invert 1b: Invert the DQ calibration patterns in MR32 and MR40 Default value for OP[7:0] = 55h | 1–3 |

- Notes:
1. This register will invert the DQ Calibration pattern found in MR32 and MR40 for any single DQ or any combination of DQ. Example: If MR15 OP[7:0] = 00010101b, then the DQ calibration patterns transmitted on DQ[7, 6, 5, 3, 1] will not be inverted, but the DQ calibration patterns transmitted on DQ[4, 2, 0] will be inverted.
 2. DM[0] is not inverted and always transmits the "true" data contained in MR32 and MR40.
 3. No data bus inversion (DBI) function is enacted during DQ read calibration, even if DBI is enabled in MR3-OP[6].

Table 54: MR15 Invert Register Pin Mapping

| PIN | DQ0 | DQ1 | DQ2 | DQ3 | DMIO | DQ4 | DQ5 | DQ6 | DQ7 |
|------|-----|-----|-----|-----|-----------|-----|-----|-----|-----|
| MR15 | OP0 | OP1 | OP2 | OP3 | No invert | OP4 | OP5 | OP6 | OP7 |

Table 55: MR16 PASR Bank Mask (MA[5:0] = 010h)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|----------------|-----|-----|-----|-----|-----|-----|-----|
| PASR bank mask | | | | | | | |

Table 56: MR16 Op-Code Bit Definitions

| Feature | Type | OP | Definition |
|----------------|------------|---------|---|
| Bank[7:0] mask | Write-only | OP[7:0] | 0b: Bank refresh enabled (default) 1b: Bank refresh disabled |

| OP[n] | Bank Mask | 8-Bank SDRAM |
|-------|-----------|--------------|
| 0 | xxxxxxx1 | Bank 0 |
| 1 | xxxxxxx1x | Bank 1 |



**200b: x32 LPDDR4 SDRAM
Mode Registers**

| OP _[n] | Bank Mask | 8-Bank SDRAM |
|-------------------|-----------|--------------|
| 2 | xxxxx1xx | Bank 2 |
| 3 | xxxx1xxx | Bank 3 |
| 4 | xxx1xxxx | Bank 4 |
| 5 | xx1xxxxx | Bank 5 |
| 6 | x1xxxxxx | Bank 6 |
| 7 | 1xxxxxxx | Bank 7 |

- Notes:
1. When a mask bit is asserted (OP_[n] = 1), refresh to that bank is disabled.
 2. PASR bank masking is on a per-channel basis; the two channels on the die may have different bank masking.

Table 57: MR17 PASR Segment Mask (MA[5:0] = 11h)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|-------------------|-----|-----|-----|-----|-----|-----|-----|
| PASR segment mask | | | | | | | |

Table 58: MR17 PASR Segment Mask Definitions

| Feature | Type | OP | Definition |
|-------------------|------------|---------|---|
| Segment[7:0] mask | Write-only | OP[7:0] | 0b: Segment refresh enabled (default) 1b: Segment refresh disabled |

Table 59: MR17 PASR Segment Mask

| Segment | OP | Segment Mask | Density (per channel) | | | | | | |
|---------|----|--------------|-----------------------|-------------|----------|-------------|----------|-------------|------|
| | | | 2Gb | 3Gb | 4Gb | 6Gb | 8Gb | 12Gb | 16Gb |
| | | | R[13:11] | R[14:12] | R[14:12] | R[15:13] | R[15:13] | TBD | TBD |
| 0 | 0 | XXXXXXXX1 | 000b | | | | | | |
| 1 | 1 | XXXXXX1X | 001b | | | | | | |
| 2 | 2 | XXXXX1XX | 010b | | | | | | |
| 3 | 3 | XXXX1XXX | 011b | | | | | | |
| 4 | 4 | XXX1XXXX | 100b | | | | | | |
| 5 | 5 | XX1XXXXX | 101b | | | | | | |
| 6 | 6 | X1XXXXXX | 110b | Not allowed | 110b | Not allowed | 110b | Not allowed | 110b |
| 7 | 7 | 1XXXXXXX | 111b | | 111b | | 111b | | 111b |

- Notes:
1. This table indicates the range of row addresses in each masked segment. "X" is "Don't Care" for a particular segment.
 2. PASR segment-masking is on a per-channel basis. The two channels on the die may have different segment masking.
 3. For 3Gb, 6Gb, and 12Gb density per channel, OP[7:6] must always be LOW (= 00b).


Table 60: MR18 Register Information (MA[5:0]=12h)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|----------------------------|-----|-----|-----|-----|-----|-----|-----|
| DQS oscillator count - LSB | | | | | | | |

Table 61: MR18 LSB DQS Oscillator Count

Notes 1–3 apply to entire table

| Function | Type | OP | Definition |
|---|-----------|---------|--------------------------------------|
| DQS oscillator count (WR training DQS oscillator) | Read-only | OP[7:0] | 0h–FFh LSB DRAM DQS oscillator count |

- Notes:
1. MR18 reports the LSB bits of the DRAM DQS oscillator count. The DRAM DQS oscillator count value is used to train DQS to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQS relative to DQ.
 2. Both MR18 and MR19 must be read (MRR) and combined to get the value of the DQS oscillator count.
 3. The value in this register is reset each time an MPC command is issued to start in the DQS oscillator counter.

Table 62: MR19 Register Information (MA[5:0] = 13h)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|----------------------------|-----|-----|-----|-----|-----|-----|-----|
| DQS oscillator count – MSB | | | | | | | |

Table 63: MR19 DQS Oscillator Count

Notes 1–3 apply to the entire table

| Function | Type | OP | Definition |
|---|-----------|---------|--------------------------------------|
| DQS oscillator count – MSB (WR training DQS oscillator) | Read-only | OP[7:0] | 0h–FFh MSB DRAM DQS oscillator count |

- Notes:
1. MR19 reports the MSB bits of the DRAM DQS oscillator count. The DRAM DQS oscillator count value is used to train DQS to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQS relative to DQ.
 2. Both MR18 and MR19 must be read (MRR) and combined to get the value of the DQS oscillator count.
 3. A new MPC[START DQS OSCILLATOR] should be issued to reset the contents of MR18/ MR19.


Table 64: MR20 Register Information (MA[5:0] = 14h)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|-----|-----|-----|-----|-----|-----|-----|
| Upper-byte invert register for DQ calibration | | | | | | | |

Table 65: MR20 Register Information

Notes 1–3 apply to entire table

| Function | Type | OP | Definition |
|--------------------------------------|------------|---------|--|
| Upper-byte invert for DQ calibration | Write-only | OP[7:0] | The following values may be written for any operand OP[7:0] and will be applied to the corresponding DQ locations DQ[15:8] within a byte lane 0b: Do not invert 1b: Invert the DQ calibration patterns in MR32 and MR40 Default value for OP[7:0] = 55h |

- Notes:
1. This register will invert the DQ calibration pattern found in MR32 and MR40 for any single DQ or any combination of DQ. For example, if MR20 OP[7:0] = 00010101b, the DQ calibration patterns transmitted on DQ[15, 14, 13, 11, 9] will not be inverted, but the DQ calibration patterns transmitted on DQ[12, 10, 8] will be inverted.
 2. DM[1] is not inverted and always transmits the true data contained in MR32 and MR40.
 3. No data bus inversion (DBI) function is enacted during DQ read calibration, even if DBI is enabled in MR3 OP[6].

Table 66: MR20 Invert Register Pin Mapping

| Pin | DQ8 | DQ9 | DQ10 | DQ11 | DMI1 | DQ12 | DQ13 | DQ14 | DQ15 |
|------|-----|-----|------|------|-----------|------|------|------|------|
| MR20 | OP0 | OP1 | OP2 | OP3 | No invert | OP4 | OP5 | OP6 | OP7 |

Table 67: MR21 Register Information (MA[5:0] = 15h)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|-----|-----|-----|-----|-----|-----|-----|-----|
| RFU | | | | | | | |

Table 68: MR22 Register Information (MA[5:0] = 16h)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|-----|-----|---------|---------|---------|---------|-----|-----|
| RFU | | ODTD-CA | ODTE-CS | ODTE-CK | SOC ODT | | |


Table 69: MR22 Register Information

| Function | Type | OP | Data | Notes |
|---|------------|---------|--|---------------|
| SOC ODT (controller ODT value for V_{OH} calibration) | Write-only | OP[2:0] | 000b: Disable (default) 001b: $R_{ZQ}/1$ 010b: $R_{ZQ}/2$ 011b: $R_{ZQ}/3$ 100b: $R_{ZQ}/4$ 101b: $R_{ZQ}/5$ 110b: $R_{ZQ}/6$ 111b: RFU | 1, 2, 3 |
| ODTE-CK (CK ODT enabled for non-terminating rank) | Write-only | OP[3] | 0b: ODT-CK override disabled (default) 1b: ODT-CK override enabled | 2, 3, 4, 6, 8 |
| ODTE-CS (CS ODT enabled for non-terminating rank) | Write-only | OP[4] | 0b: ODT-CS override disabled (default) 1b: ODT-CS override enabled | 2, 3, 5, 6, 8 |
| ODTD-CA (CA ODT termination disable) | Write-only | OP[5] | 0b: CA ODT obeys ODT_CA bond pad (default) 1b: CA ODT disabled | 2, 3, 6, 7, 8 |

- Notes:
- All values are typical.
 - There are two physical registers assigned to each bit of this MR parameter: designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command or read from with an MRR command to this address.
 - There are two physical registers assigned to each bit of this MR parameter: designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.
 - When OP[3] = 1 the CK signals will be terminated to the value set by MR11 OP[6:4] regardless of the state of the ODT_CA bond pad. This overrides the ODT_CA bond pad for configurations where CA is shared by two or more devices but CK is not, enabling CK to terminate on all devices.
 - When OP[4] = 1 the CS signal will be terminated to the value set by MR11 OP[6:4] regardless of the state of the ODT_CA bond pad. This overrides the ODT_CA bond pad for configurations where CA is shared by two or more devices but CS is not, enabling CS to terminate on all devices.
 - For system configurations where the CK, CS, and CA signals are shared between packages, the package design should provide for the ODT_CA ball to be bonded on the system board outside of the memory package. This provides the necessary control of the ODT function for all die with shared command bus signals.
 - When OP[5] = 0, CA[5:0] will terminate when the ODT_CA bond pad is HIGH and MR11 OP[6:4] is valid and disable termination when ODT_CA is LOW or MR11 OP[6:4] is disabled. When OP[5] = 1, termination for CA[5:0] is disabled regardless of the state of the ODT_CA bond pad or MR11 OP[6:4].
 - To ensure proper operation in a multi-rank configuration, when CA, CK or CS ODT is enabled via MR11 OP[6:4] and also via MR22 or ODT_CA pad setting, the rank providing ODT will continue to terminate the command bus in all DRAM states including Active, Self-refresh, Self-refresh Power-down, Active Power-down and Precharge Power-down.



Table 70: MR23 Register Information (MA[5:0] = 17h)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|-------------------------------------|-----|-----|-----|-----|-----|-----|-----|
| DQS interval timer run-time setting | | | | | | | |

Table 71: MR23 Register Information

Notes 1–2 apply to entire table

| Function | Type | OP | Data |
|-----------------------------|------------|---------|---|
| DQS interval timer run-time | Write-only | OP[7:0] | 00000000b: Disabled (default) 00000001b: DQS timer stops automatically at the 16 th clock after timer start 00000010b: DQS timer stops automatically at the 32 nd clock after timer start 00000011b: DQS timer stops automatically at the 48 th clock after timer start 00000100b: DQS timer stops automatically at the 64 th clock after timer start ----- Through ----- 00111111b: DQS timer stops automatically at the (63 × 16) th clock after timer start 01XXXXXXb: DQS timer stops automatically at the 2048 th clock after timer start 10XXXXXXb: DQS timer stops automatically at the 4096 th clock after timer start 11XXXXXXb: DQS timer stops automatically at the 8192 nd clock after timer start |

- Notes: 1. MPC command with OP[6:0] = 1001101b (stop DQS Interval Oscillator) stops the DQS interval timer in the case of MR23 OP[7:0] = 00000000b.
 2. MPC command with OP[6:0] = 1001101b (stop DQS Interval Oscillator) is illegal with valid nonzero values in MR23 OP[7:0].

Table 72: MR24 Register Information (MA[5:0] = 18h)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|----------|--------------|-----|-----|---------------|-----------|-----|-----|
| TRR mode | TRR mode BAn | | | Unlimited MAC | MAC value | | |


Table 73: MR24 Register Information

| Function | Type | OP | Data | Notes |
|---------------|-------|---------|--|-------|
| MAC value | Read | OP[2:0] | 000b: Unknown (OP[3] = 0) or Unlimited (OP[3] = 1) 001b: 700K 010b: 600K 011b: 500K 100b: 400K 101b: 300K 110b: 200K 111b: Reserved | 1, 2 |
| Unlimited MAC | Read | OP[3] | 0b: OP[2:0] defines the MAC value 1b: Unlimited MAC value | 2, 3 |
| TRR mode BAn | Write | OP[6:4] | 000b: Bank 0 001b: Bank 1 010b: Bank 2 011b: Bank 3 100b: Bank 4 101b: Bank 5 110b: Bank 6 111b: Bank 7 | |
| TRR mode | Write | OP[7] | 0b: Disabled (default) 1b: Enabled | |

- Notes:
1. Unknown means that the device is not tested for ^tMAC and pass/fail values are unknown. Unlimited means that there is no restriction on the number of activates between refresh windows.
 2. There is no restriction to the number of activates.
 3. MR24 OP[2:0] set to 000b.

Table 74: MR25 Register Information (MA[5:0] = 19h)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|--------|--------|--------|--------|--------|--------|--------|--------|
| Bank 7 | Bank 6 | Bank 5 | Bank 4 | Bank 3 | Bank 2 | Bank 1 | Bank 0 |

Table 75: MR25 Register Information

| Function | Type | OP | Data |
|---------------|-----------|---------|--|
| PPR resources | Read-only | OP[7:0] | 0b: PPR resource is not available 1b: PPR resource is available |

- Note:
1. When OP[n] = 0, there is no PPR resource available for that bank. When OP[n] = 1, there is a PPR resource available for that bank, and PPR can be initiated by the controller.


Table 76: MR26:31 Register Information (MA[5:0] = 1Ah–1Fh)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|-------------------------|-----|-----|-----|-----|-----|-----|-----|
| Reserved for future use | | | | | | | |

Table 77: MR32 Register Information (MA[5:0] = 20h)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|--|-----|-----|-----|-----|-----|-----|-----|
| DQ calibration pattern A (default = 5Ah) | | | | | | | |

Table 78: MR32 Register Information

| Function | Type | OP | Data | Notes |
|---|------------|---------|--|---------|
| Return DQ calibration pattern MR32 + MR40 | Write-only | OP[7:0] | Xb: An MPC command issued with OP[6:0] = 1000011b causes the device to return the DQ calibration pattern contained in this register and (followed by) the contents of MR40. A default pattern 5Ah is loaded at power-up or reset, or the pattern may be overwritten with a MRW to this register. The contents of MR15 and MR20 will invert the MR32/MR40 data pattern for a given DQ (see MR15/MR20 for more information). | 1, 2, 3 |

- Notes:
1. The patterns contained in MR32 and MR40 are transmitted on DQ[15:0] and DMI[1:0] when DQ read calibration is initiated via an MPC command. The pattern is transmitted serially on each data lane and organized little endian such that the low-order bit in a byte is transmitted first. If the data pattern is 27H, the first bit transmitted is a 1 followed by 1, 1, 0, 0, 1, 0, and 0. The bit stream will be 00100111.
 2. MR15 and MR20 may be used to invert the MR32/MR40 data pattern on the DQ pins. See MR15 and MR20 for more information. Data is never inverted on the DMI[1:0] pins.
 3. The data pattern is not transmitted on the DMI[1:0] pins if DBI-RD is disabled via MR3 OP[6].
 4. No data bus inversion (DBI) function is enacted during DQ read calibration, even if DBI is enabled in MR3 OP[6].

Table 79: MR33:39 Register Information (MA[5:0] = 21h–27h)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|------------|-----|-----|-----|-----|-----|-----|-----|
| Do not use | | | | | | | |

Table 80: MR40 Register Information (MA[5:0] = 28h)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|--|-----|-----|-----|-----|-----|-----|-----|
| DQ calibration pattern B (default = 3Ch) | | | | | | | |


Table 81: MR40 Register Information

| Function | Type | OP | Data | Notes |
|--|------------|---------|---|---------|
| Return DQ calibration pattern MR32 + MR40 | Write-only | OP[7:0] | Xb: A default pattern 3Ch is loaded at power-up or reset, or the pattern may be overwritten with a MRW to this register. See MR32 for more information. | 1, 2, 3 |

- Notes:
1. The pattern contained in MR40 is concatenated to the end of MR32 and transmitted on DQ[15:0] and DMI[1:0] when DQ read calibration is initiated via an MPC command. The pattern is transmitted serially on each data lane and organized little endian such that the low-order bit in a byte is transmitted first. If the data pattern in MR40 is 27H, the first bit transmitted will be a 1, followed by 1, 1, 0, 0, 1, 0, and 0. The bit stream will be 00100111.
 2. MR15 and MR20 may be used to invert the MR32/MR40 data patterns on the DQ pins. See MR15 and MR20 for more information. Data is never inverted on the DMI[1:0] pins.
 3. The data pattern is not transmitted on the DMI[1:0] pins if DBI-RD is disabled via MR3 OP[6].
 4. No data bus inversion (DBI) function is enacted during DQ read calibration, even if DBI is enabled in MR3 OP[6].

Table 82: MR41:47 Register Information (MA[5:0] = 29h–2Fh)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|------------|-----|-----|-----|-----|-----|-----|-----|
| Do not use | | | | | | | |

Table 83: MR48:63 Register Information (MA[5:0] = 30h–3Fh)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|-------------------------|-----|-----|-----|-----|-----|-----|-----|
| Reserved for future use | | | | | | | |

Commands and Timing

Commands transmitted on the CA bus are encoded into two parts and are latched on two consecutive rising edges of the clock. This is called 2-tick CA capture because each command requires two clock edges to latch and decode the entire command.

Truth Tables

Truth tables provide complementary information to the state diagram. They also clarify device behavior and applicable restrictions when considering the actual state of the banks.

Unspecified operations and timings are illegal. To ensure proper operation after an illegal event, the device must be either reset by asserting the RESET_n command or powered down and then restarted using the specified initialization sequence before normal operation can continue.

CKE signal has to be held HIGH when the commands listed in the command truth table input.


Table 84: Command Truth Table

Commands are transmitted to the device across a six-lane interface and use CK, CKE, and CS to control the capture of transmitted data

| Command | CS | SDR CA Pins | | | | | | CK Edge | Notes |
|---|----|-------------|-----|-----|-----|-----|-----|---------|------------------------|
| | | CA0 | CA1 | CA2 | CA3 | CA4 | CA5 | | |
| MRW-1 | H | L | H | H | L | L | OP7 | | 1, 11 |
| | L | MA0 | MA1 | MA2 | MA3 | MA4 | MA5 | | |
| MRW-2 | H | L | H | H | L | H | OP6 | | 1, 11 |
| | L | OP0 | OP1 | OP2 | OP3 | OP4 | OP5 | | |
| MRR-1 | H | L | H | H | H | L | V | | 1, 2, 12 |
| | L | MA0 | MA1 | MA2 | MA3 | MA4 | MA5 | | |
| REFRESH (all/per bank) | H | L | L | L | H | L | AB | | 1, 2, 3, 4 |
| | L | BA0 | BA1 | BA2 | V | V | V | | |
| ENTER SELF RE- FRESH | H | L | L | L | H | H | V | | 1, 2 |
| | L | V | | | | | | | |
| ACTIVATE-1 | H | H | L | R12 | R13 | R14 | R15 | | 1, 2, 3, 11 |
| | L | BA0 | BA1 | BA2 | R16 | R10 | R11 | | |
| ACTIVATE-2 | H | H | H | R6 | R7 | R8 | R9 | | 1, 11 |
| | L | R0 | R1 | R2 | R3 | R4 | R5 | | |
| WRITE-1 | H | L | L | H | L | L | BL | | 1, 2, 3, 6, 7, 9 |
| | L | BA0 | BA1 | BA2 | V | C9 | AP | | |
| EXIT SELF RE- FRESH | H | L | L | H | L | H | V | | 1, 2 |
| | L | V | | | | | | | |
| MASK WRITE-1 | H | L | L | H | H | L | BL | | 1, 2, 3, 5, 6, 7, 9 |
| | L | BA0 | BA1 | BA2 | V | C9 | AP | | |
| RFU | H | L | L | H | H | H | V | | 1, 2 |
| | L | V | | | | | | | |
| RFU | H | L | H | L | H | L | V | | 1, 2 |
| | L | V | | | | | | | |
| RFU | H | L | H | L | H | H | V | | 1, 2 |
| | L | V | | | | | | | |
| READ-1 | H | L | H | L | L | L | BL | | 1, 2, 3, 6, 7, 9 |
| | L | BA0 | BA1 | BA2 | V | C9 | AP | | |
| CAS-2 (WRITE-2, MASKED WRITE-2, READ-2, MRR-2, MPC (except NOP) | H | L | H | L | L | H | C8 | | 1, 8, 9 |
| | L | C2 | C3 | C4 | C5 | C6 | C7 | | |


Table 84: Command Truth Table (Continued)

Commands are transmitted to the device across a six-lane interface and use CK, CKE, and CS to control the capture of transmitted data

| Command | CS | SDR CA Pins | | | | | | CK Edge | Notes |
|-----------------------------|----|-------------|-----|-----|-----|-----|-----|---------|------------|
| | | CA0 | CA1 | CA2 | CA3 | CA4 | CA5 | | |
| PRECHARGE (all/per bank) | H | L | L | L | L | H | AB | | 1, 2, 3, 4 |
| | L | BA0 | BA1 | BA2 | V | V | V | | |
| MPC (TRAIN, NOP) | H | L | L | L | L | L | OP6 | | 1, 2, 13 |
| | L | OP0 | OP1 | OP2 | OP3 | OP4 | OP5 | | |
| DESELECT | L | X | | | | | | | 1, 2 |

- Notes:
- All commands except for Deselect are two clock cycles and are defined by the current state of CS and CA[5:0] at the rising edge of the clock. Deselect command is one clock cycle and is not latched by the device.
 - V = H or L (a defined logic level); X = "Don't Care," in which case CS, CK_t, CK_c, and CA[5:0] can be floated.
 - Bank addresses BA[2:0] determine which bank is to be operated upon.
 - AB HIGH during PRECHARGE or REFRESH commands indicate the command must be applied to all banks, and the bank addresses are "Don't Care."
 - MASK WRITE-1 command only supports BL16. For MASK WRITE-1 commands, CA5 must be driven LOW on the first rising clock cycle (R1).
 - AP HIGH during a WRITE-1, MASK WRITE-1, or READ-1 command indicates that an auto precharge will occur to the bank the command is operating on. AP LOW indicates that no auto precharge will occur and the bank will remain open upon completion of the command.
 - When enabled in the mode register, BL HIGH during a WRITE-1, MASK-WRITE-1, or READ-1 command indicates the burst length should be set on-the-fly to BL = 32; BL LOW during one of these commands indicates the burst length should be set on-the-fly to BL = 16. If on-the-fly burst length is not enabled in the mode register, this bit should be driven to a valid level and is ignored by the device.
 - For CAS-2 commands (WRITE-2, MASK WRITE-2, READ-2, MRR-2, or MPC (only WRITE-FIFO, READ-FIFO, and READ DQ CALIBRATION)), C[1:0] are not transmitted on the CA [5:0] bus and are assumed to be zero. Note that for CAS-2 WRITE-2 or CAS-2 MASK WRITE-2 command, C[3:2] must be driven LOW.
 - WRITE-1, MASK-WRITE-1, READ-1, MODE REGISTER READ-1, or MPC (only WRITE-FIFO, READ-FIFO, and READ DQ CALIBRATION) command must be immediately followed by CAS-2 command consecutively without any other command in between. WRITE-1, MASK WRITE-1, READ-1, MRR-1, or MPC (only WRITE-FIFO, READ-FIFO, and READ DQ CALIBRATION) command must be issued first before issuing CAS-2 command. MPC (only START and STOP DQS OSCILLATOR, ZQCAL START and LATCH) commands do not require CAS-2 command; they require two additional DES or NOP commands consecutively before issuing any other commands.
 - The ACTIVATE-1 command must be followed by the ACTIVATE-2 command consecutively without any other command between them. The ACTIVATE-1 command must be issued prior to the ACTIVATE-2 command. When the ACTIVATE-1 command is issued, the ACTIVATE-2 command must be issued before issuing another ACTIVATE-1 command.
 - The MRW-1 command must be followed by the MRW-2 command consecutively without any other command between them. The MRW-1 command must be issued prior to the MRW-2 command.



12. The MRR-1 command must be followed by the CAS-2 command consecutively without any other commands between them. The MRR-1 command must be issued prior to the CAS-2 command.
13. The MPC command for READ or WRITE TRAINING operations must be followed by the CAS-2 command consecutively without any other commands between them. The MPC command must be issued prior to the CAS-2 command.

ACTIVATE Command

The ACTIVATE command must be executed before a READ or WRITE command can be issued. The ACTIVATE command is issued in two parts: The bank and upper-row addresses are entered with activate-1 and the lower-row addresses are entered with ACTIVATE-2. ACTIVATE-1 and ACTIVATE-2 are executed by strobing CS HIGH while setting CA[5:0] at valid levels (see Command table) at the rising edge of CK.

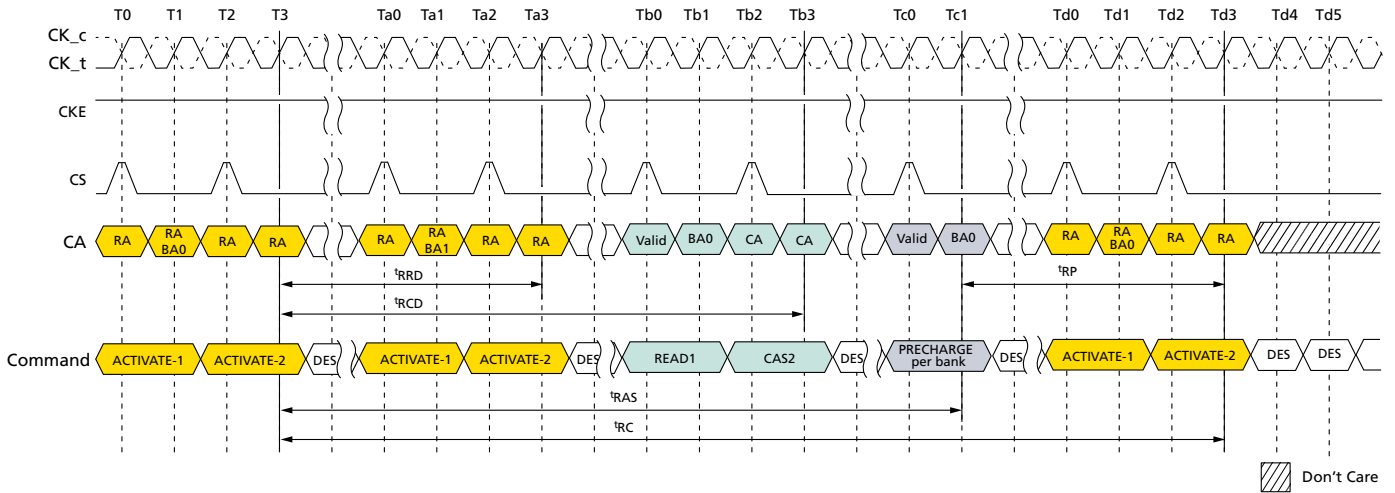
The bank addresses (BA[2:0]) are used to select the desired bank. The row addresses (R[15:0]) are used to determine which row to activate in the selected bank. The ACTIVATE-2 command must be applied before any READ or WRITE operation can be executed. The device can accept a READ or WRITE command at time t_{RCD} after the ACTIVATE-2 command is sent. After a bank has been activated, it must be precharged to close the active row before another ACTIVATE-2 command can be applied to the same bank. The bank active and precharge times are defined as t_{RAS} and t_{RP} , respectively. The minimum time interval between successive ACTIVATE-2 commands to the same bank is determined by the row cycle time of the device (t_{RC}). The minimum time interval between ACTIVATE-2 commands to different banks is t_{RRD} .

Certain restrictions must be observed for bank ACTIVATE and REFpb operations.

- Four-activate window (t_{FAW}): No more than 4 banks may be activated (or refreshed, in the case of REFpb) per channel in a rolling t_{FAW} window. Convert to clocks by dividing $t_{FAW}[ns]$ by $t_{CK}[ns]$ and rounding up to the next integer value. As an example of the rolling window, if $RU[(t_{FAW}/t_{CK})]$ is 64 clocks, and an ACTIVATE command is issued on clock N, no more than three additional ACTIVATE commands may be issued between clock N + 1 and N + 63. REFpb also counts as bank activation for the purposes of t_{FAW} .
- 8-bank per channel, precharge all banks (AB) allowance: t_{RP} for a PRECHARGE ALL BANKS command for an 8-bank device must equal t_{RPab} , which is greater than t_{RPpb} .

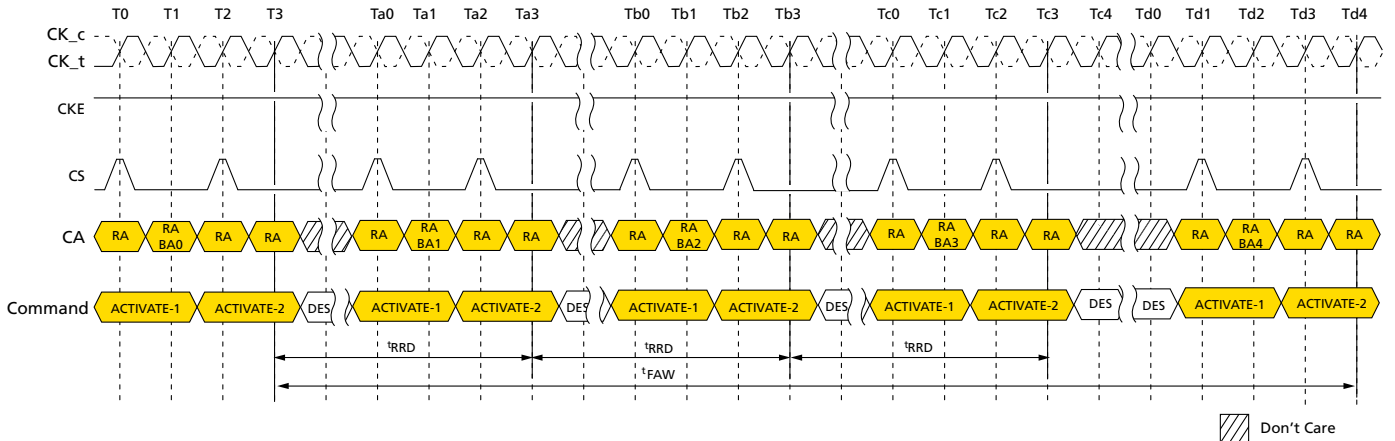


Figure 14: ACTIVATE Command



Note: 1. A PRECHARGE command uses tRP_{ab} timing for all-bank precharge and tRP_{pb} timing for single-bank precharge. In this figure, tRP is used to denote either all-bank precharge or a single-bank precharge. $tCCD = \text{MIN}, 1.5nCK$ postamble, $533 \text{ MHz} < \text{clock frequency} \leq 800 \text{ MHz}$, ODT worst timing case.

Figure 15: $tFAW$ Timing



Note: 1. REFpb may be substituted for one of the ACTIVATE commands for the purposes of $tFAW$.

Read and Write Access Modes

After a bank has been activated, a READ or WRITE command can be executed. This is accomplished by asserting CKE asynchronously, with CS and CA[5:0] set to the proper state (see Command Truth Table) on the rising edge of CK.

The device provides a fast column access operation. A single READ or WRITE command will initiate a burst READ or WRITE operation, where data is transferred to/from the device on successive clock cycles. Burst interrupts are not allowed; however, the optimal burst length may be set on-the-fly (see Command Truth Table).



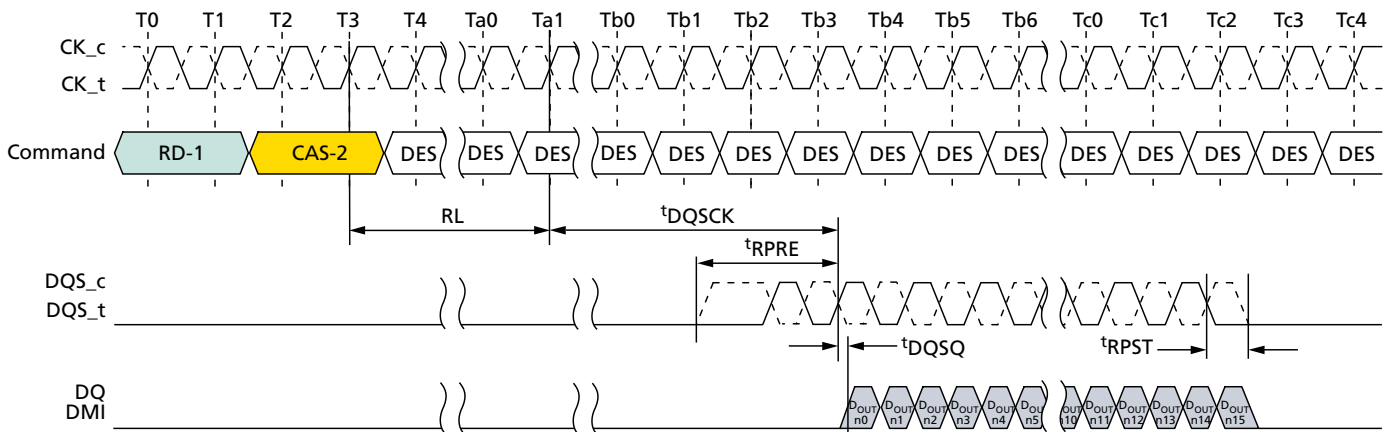
Preamble and Postamble

The DQS strobe for the device requires a preamble prior to the first latching edge (the rising edge of DQS_t with data valid), and it requires a postamble after the last latching edge. The preamble and postamble options are set via MODE REGISTER WRITE commands.

The read preamble is two ^tCK in length and is either static or has one clock toggle before the first latching edge. The read preamble option is enabled via MRW to MR1 OP[3] (0 = Static; 1 = Toggle).

The read postamble has a programmable option to extend the postamble by 1 *n*CK (^tRPSTE). The extended postamble option is enabled via MRW to MR1 OP[7] (0 = 0.5 *n*CK; 1 = 1.5 *n*CK).

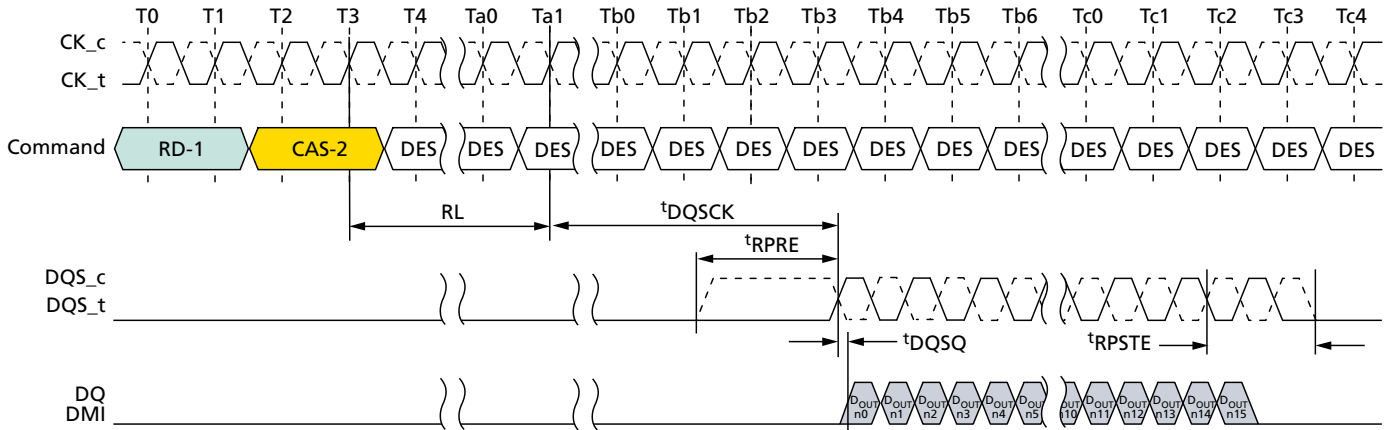
Figure 16: DQS Read Preamble and Postamble – Toggling Preamble and 0.5*n*CK Postamble



- Notes:
1. BL = 16, Preamble = Toggling, Postamble = 0.5 *n*CK.
 2. DQS and DQ terminated V_{SSQ}.
 3. DQS_t/DQS_c is "Don't Care" prior to the start of ^tRPRE. No transition of DQS is implied, as DQS_t/DQS_c can be HIGH, LOW, or High-Z prior to ^tRPRE.

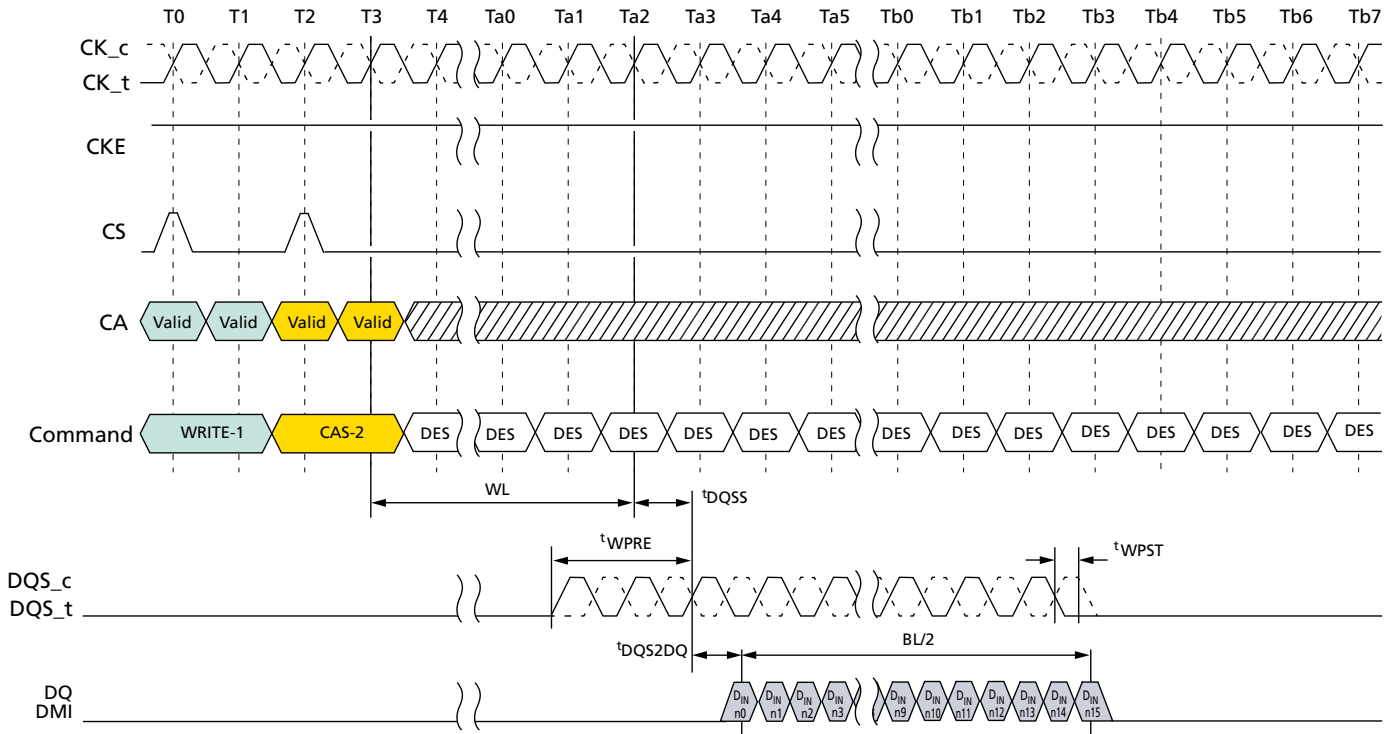


Figure 17: DQS Read Preamble and Postamble – Static Preamble and 1.5nCK Postamble



- Notes:
1. BL = 16, Preamble = Static, Postamble = 1.5nCK (extended).
 2. DQS and DQ terminated V_{SSQ} .
 3. DQS_t/DQS_c is "Don't Care" prior to the start of t_{RPRE} . No transition of DQS is implied, as DQS_t/DQS_c can be HIGH, LOW, or High-Z prior to t_{RPRE} .

Figure 18: DQS Write Preamble and Postamble – 0.5nCK Postamble



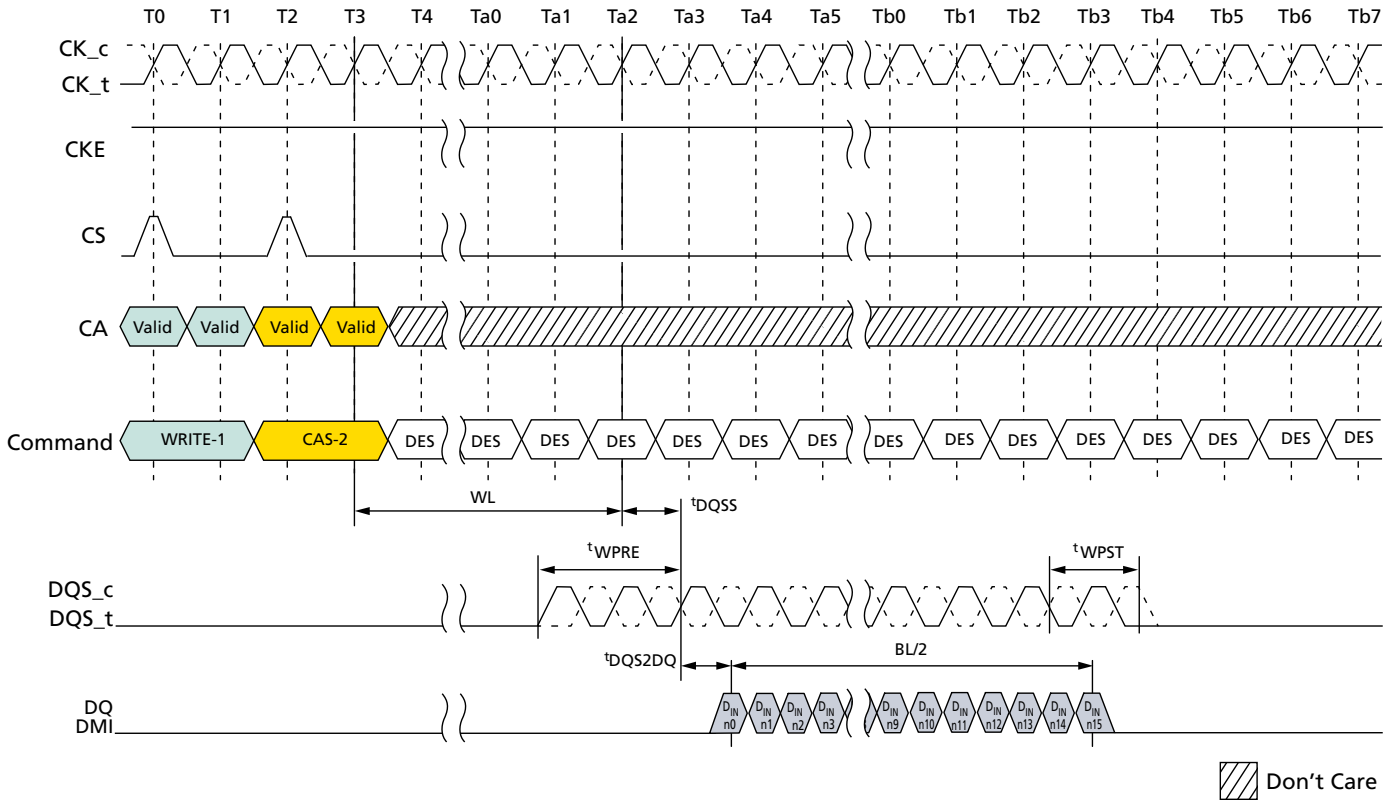
Don't Care

- Notes:
1. BL = 16, Postamble = 0.5nCK.
 2. DQS and DQ terminated V_{SSQ} .



3. DQS_t/DQS_c is "Don't Care" prior to the start of t_{WPRE} . No transition of DQS is implied, as DQS_t/DQS_c can be HIGH, LOW, or High-Z prior to t_{WPRE} .

Figure 19: DQS Write Preamble and Postamble – 1.5nCK Postamble



- Notes:
1. BL = 16, Postamble = 1.5nCK.
 2. DQS and DQ terminated V_{SSQ} .
 3. DQS_t/DQS_c is "Don't Care" prior to the start of t_{WPRE} . No transition of DQS is implied, as DQS_t/DQS_c can be HIGH, LOW, or High-Z prior to t_{WPRE} .



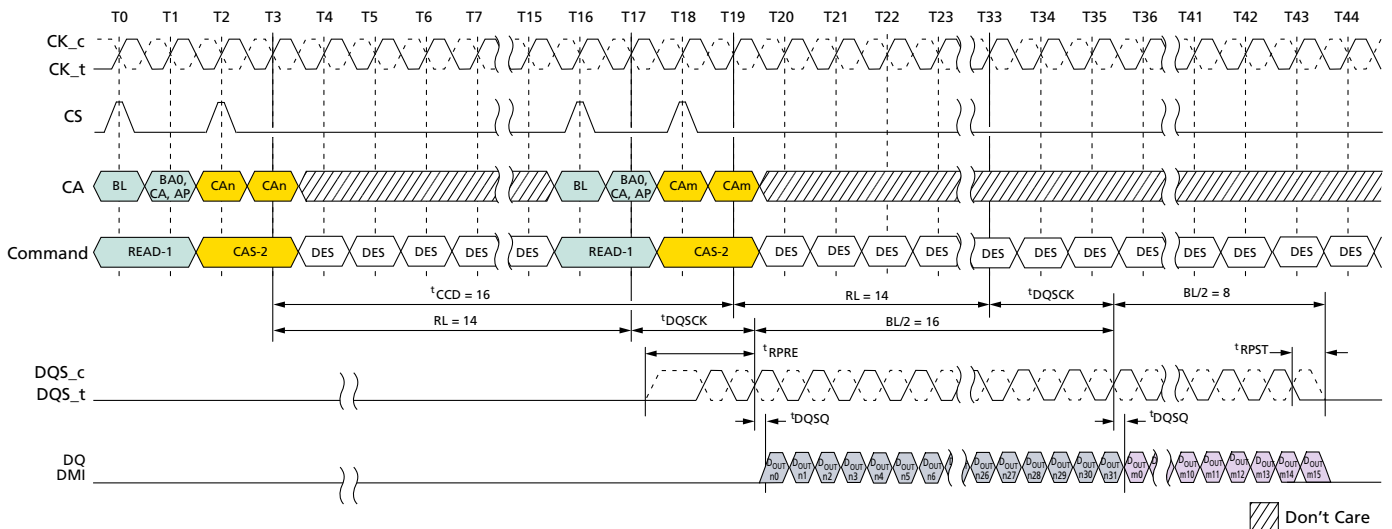
Burst READ Operation

A burst READ command is initiated with CKE, CS, and CA[5:0] asserted to the proper state on the rising edge of CK, as defined by the Command Truth Table. The command address bus inputs determine the starting column address for the burst. The two low-order address bits are not transmitted on the CA bus and are implied to be 0; therefore, the starting burst address is always a multiple of four (that is, 0x0, 0x4, 0x8, 0xC).

The READ latency (RL) is defined from the last rising edge of the clock that completes a READ command (for example, the second rising edge of the CAS-2 command) to the rising edge of the clock from which the t^{DQSCK} delay is measured. The first valid data is available $RL \times {}^t\text{CK} + {}^t\text{DQSCK} + {}^t\text{DQSQ}$ after the rising edge of clock that completes a READ command.

The data strobe output is driven t^{RPRE} before the first valid rising strobe edge. The first data bit of the burst is synchronized with the first valid (post-preamble) rising edge of the data strobe. Each subsequent data-out appears on each DQ pin, edge-aligned with the data strobe. At the end of a burst, the DQS signals are driven for another half cycle postamble, or for a 1.5-cycle postamble if the programmable postamble bit is set in the mode register. The RL is programmed in the mode registers. Pin timings for the data strobe are measured relative to the cross-point of DQS_t and DQS_c .

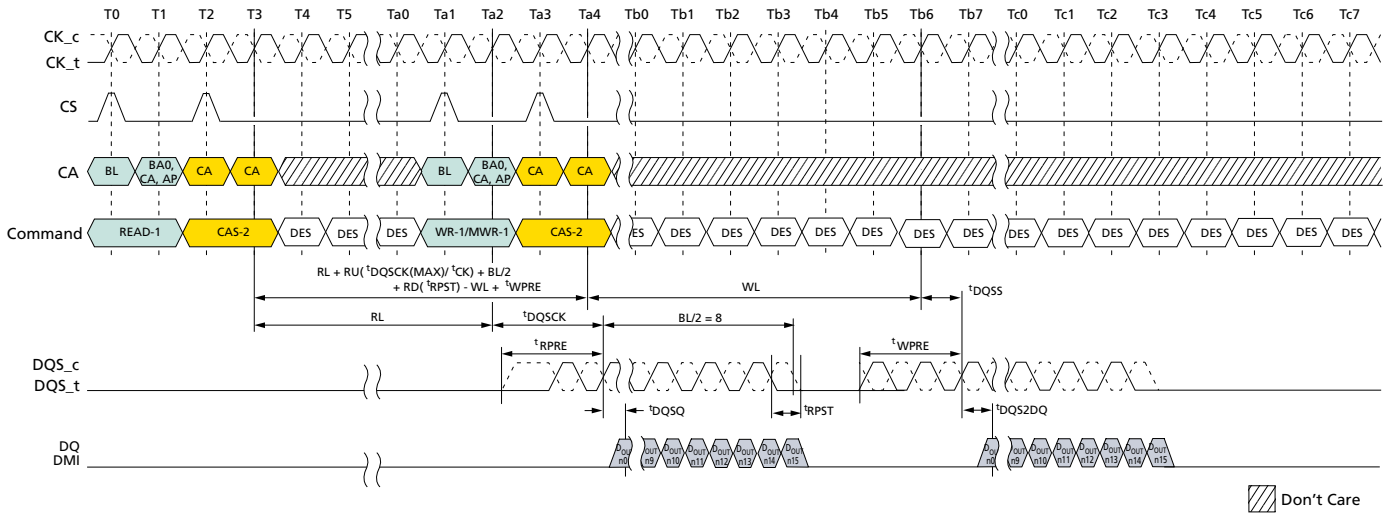
Figure 20: Burst Read Timing



- Notes:
1. BL = 32 for column n , BL = 16 for column m , RL = 14, Preamble = Toggle, Postamble = $0.5n\text{CK}$, DQ/DQS: V_{SSQ} termination.
 2. $\text{D}_{\text{OUT } n/m}$ = data-out from column n and column m .
 3. DES commands are shown for ease of illustration; other commands may be valid at these times.

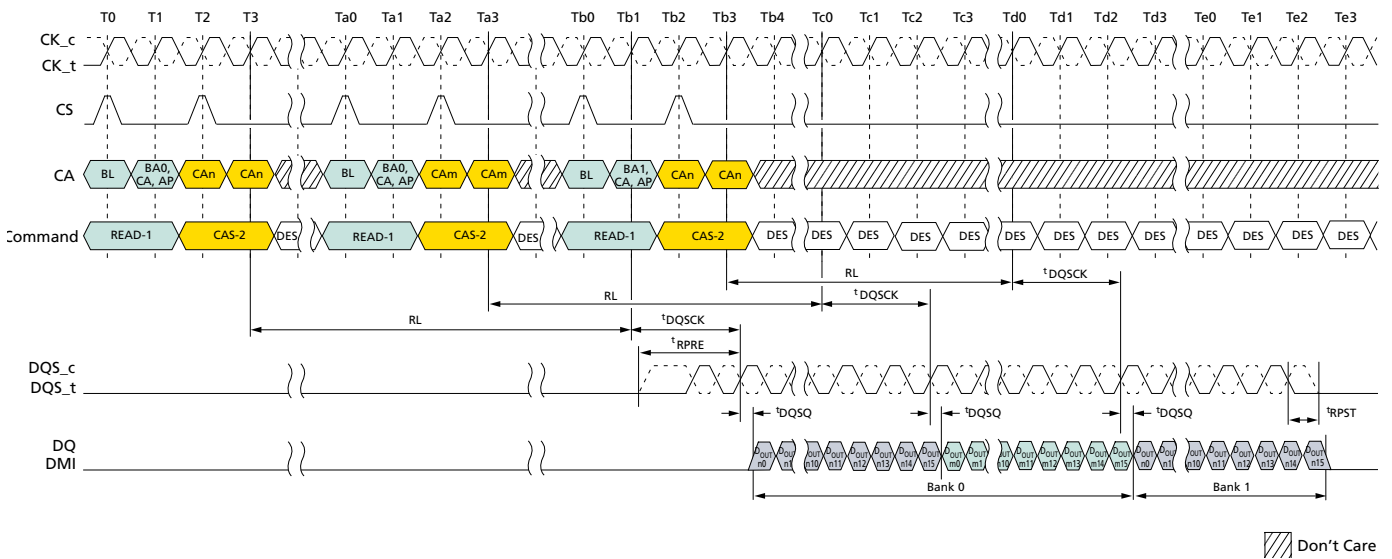


Figure 21: Burst Read Followed by Burst Write or Burst Mask Write



- Notes:
1. BL = 16, Read preamble = Toggle, Read postamble = 0.5nCK, Write preamble = 2nCK, Write postamble = 0.5nCK, DQ/DQS: V_{SSQ} termination.
 2. D_{OUT} n = data-out from column n and D_{IN} n = data-in to column n.
 3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 22: Seamless Burst Read

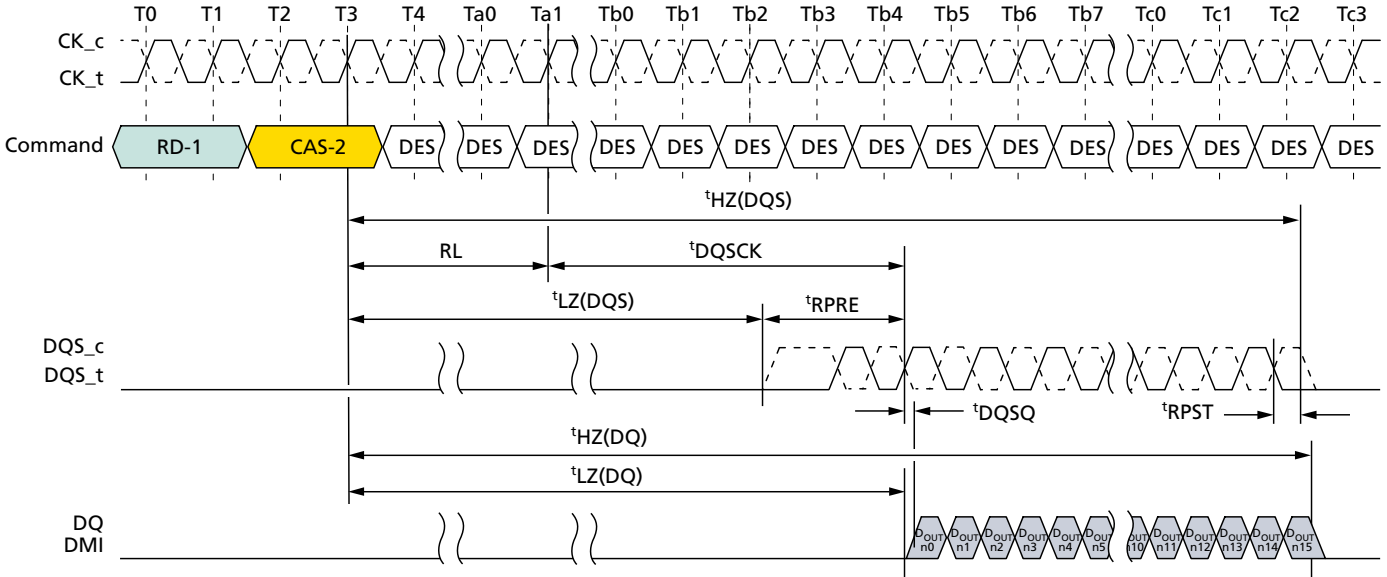


- Notes:
1. BL = 16, t_{CCD} = 8, Preamble = Toggle, Postamble = 0.5nCK, DQ/DQS: V_{SSQ} termination.
 2. D_{OUT} n/m = data-out from column n and column m.
 3. DES commands are shown for ease of illustration; other commands may be valid at these times.



Read Timing

Figure 23: Read Timing



- Notes:
1. BL = 16, Preamble = Toggling, Postamble = 0.5nCK.
 2. DQS, DQ, and DMI terminated V_{SSQ} .
 3. Output driver does not turn on before an endpoint of $tLZ(DQS)$ and $tLZ(DQ)$.
 4. Output driver does not turn off before an endpoint of $tHZ(DQS)$ and $tHZ(DQ)$.

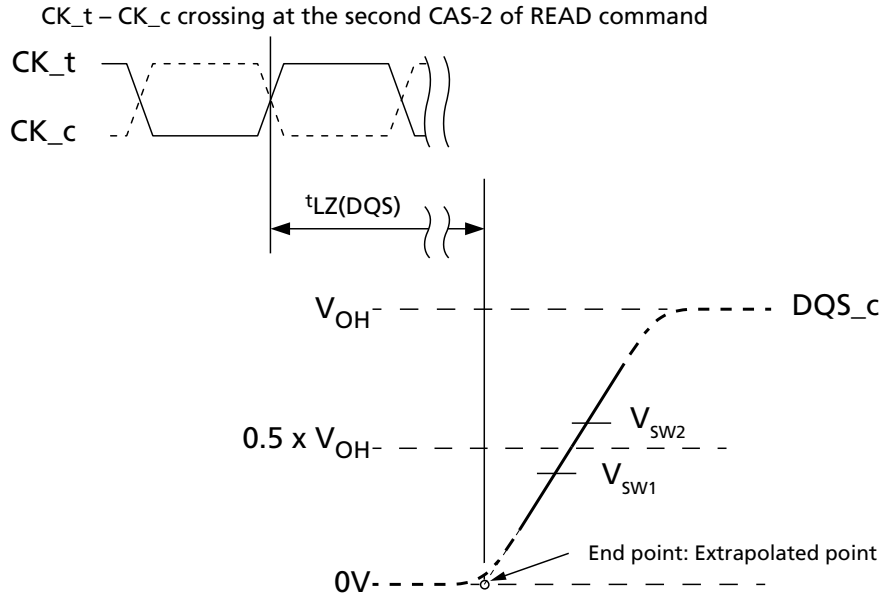
$tLZ(DQS)$, $tLZ(DQ)$, $tHZ(DQS)$, $tHZ(DQ)$ Calculation

tHZ and tLZ transitions occur in the same time window as valid data transitions. These parameters are referenced to a specific voltage level that specifies when the device output is no longer driving $tHZ(DQS)$ and $tHZ(DQ)$, or begins driving $tLZ(DQS)$ and $tLZ(DQ)$. This section shows a method to calculate the point when the device is no longer driving $tHZ(DQS)$ and $tHZ(DQ)$, or begins driving $tLZ(DQS)$ and $tLZ(DQ)$, by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. The parameters $tLZ(DQS)$, $tLZ(DQ)$, $tHZ(DQS)$, and $tHZ(DQ)$ are defined as single ended.



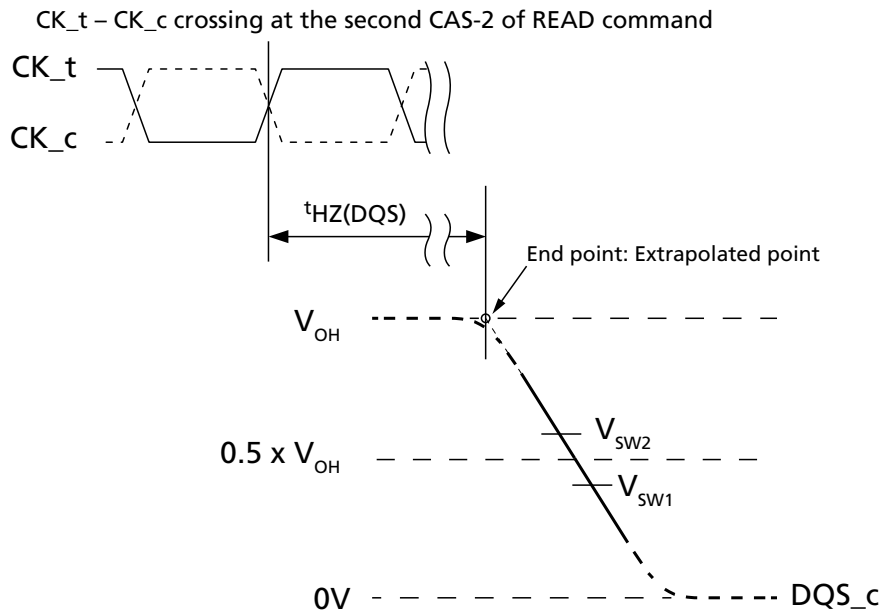
$t_{LZ}(DQS)$ and $t_{HZ}(DQS)$ Calculation for ATE (Automatic Test Equipment)

Figure 24: $t_{LZ}(DQS)$ Method for Calculating Transitions and Endpoint



- Notes:
1. Conditions for calibration: Pull down driver R_{ON} = 40 ohms, V_{OH} = V_{DDQ}/3.
 2. Termination condition for DQS_t and DQS_c = 50 ohms to V_{SSQ}.
 3. The V_{OH} level depends on MR22 OP[2:0] and MR3 OP[0] settings as well as device tolerances. Use the actual V_{OH} value for t_{HZ} and t_{LZ} measurements.

Figure 25: $t_{HZ}(DQS)$ Method for Calculating Transitions and Endpoint



- Notes:
1. Conditions for calibration: Pull down driver R_{ON} = 40 ohms, V_{OH} = V_{DDQ}/3.
 2. Termination condition for DQS_t and DQS_c = 50 ohms to V_{SSQ}.



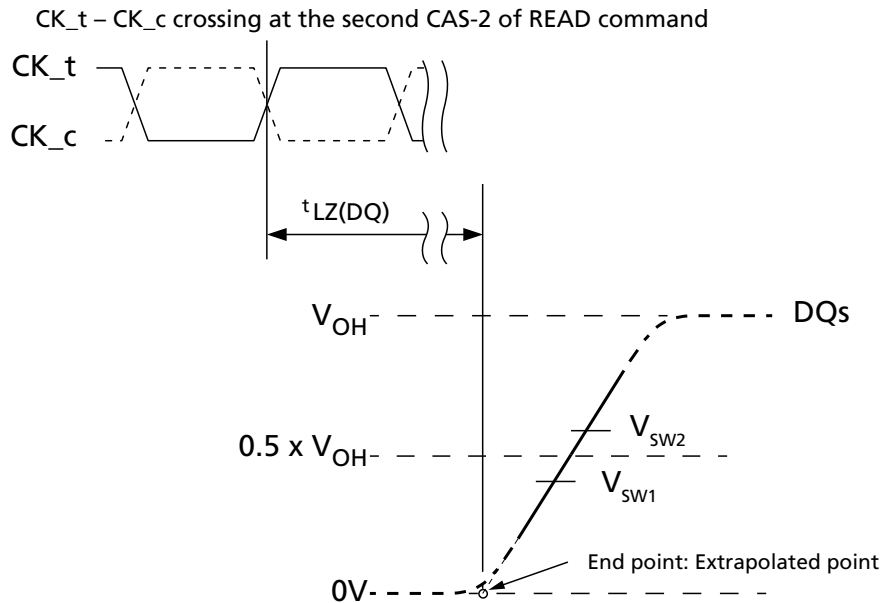
- The V_{OH} level depends on MR22 OP[2:0] and MR3 OP[0] settings as well as device tolerances. Use the actual V_{OH} value for t_{HZ} and t_{LZ} measurements.

Table 85: Reference Voltage for $t_{LZ}(DQS)$, $t_{HZ}(DQS)$ Timing Measurements

| Measured Parameter | Measured Parameter Symbol | Vsw1 | Vsw2 | Unit |
|-----------------------------------|---------------------------|---------------------|---------------------|------|
| DQS_c Low-Z time from CK_t, CK_c | $t_{LZ}(DQS)$ | $0.4 \times V_{OH}$ | $0.6 \times V_{OH}$ | V |
| DQS_c High-Z time from CK_t, CK_c | $t_{HZ}(DQS)$ | $0.4 \times V_{OH}$ | $0.6 \times V_{OH}$ | |

$t_{LZ}(DQ)$ and $t_{HZ}(DQ)$ Calculation for ATE (Automatic Test Equipment)

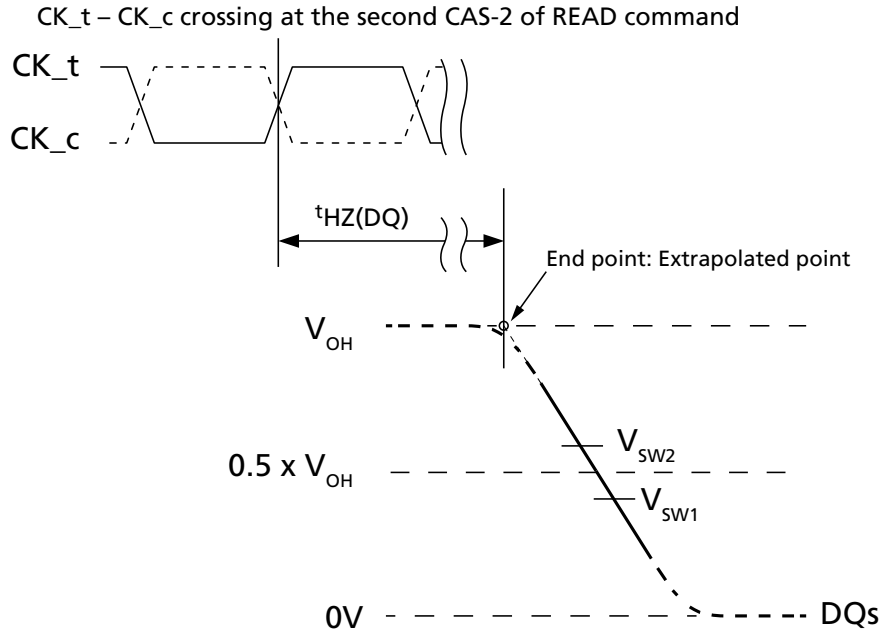
Figure 26: $t_{LZ}(DQ)$ Method for Calculating Transitions and Endpoint



- Notes:
- Conditions for calibration: Pull down driver $R_{ON} = 40$ ohms, $V_{OH} = V_{DDQ}/3$.
 - Termination condition for DQ and DMI = 50 ohms to V_{SSQ} .
 - The V_{OH} level depends on MR22 OP[2:0] and MR3 OP[0] settings as well as device tolerances. Use the actual V_{OH} value for t_{HZ} and t_{LZ} measurements.



Figure 27: ^tHZ(DQ) Method for Calculating Transitions and Endpoint



- Notes:
1. Conditions for calibration: Pull down driver $R_{ON} = 40$ ohms, $V_{OH} = V_{DDQ}/3$.
 2. Termination condition for DQ and DMI = 50 ohms to V_{SSQ} .
 3. The V_{OH} level depends on MR22 OP[2:0] and MR3 OP[0] settings as well as device tolerances. Use the actual V_{OH} value for ^tHZ and ^tLZ measurements.

Table 86: Reference Voltage for ^tLZ(DQ), ^tHZ(DQ) Timing Measurements

| Measured Parameter | Measured Parameter Symbol | Vsw1 | Vsw2 | Unit |
|---|---------------------------|---------------------|---------------------|------|
| DQ Low-Z time from CK _t , CK _c | ^t LZ(DQ) | $0.4 \times V_{OH}$ | $0.6 \times V_{OH}$ | V |
| DQ High-Z time from CK _t , CK _c | ^t HZ(DQ) | $0.4 \times V_{OH}$ | $0.6 \times V_{OH}$ | |



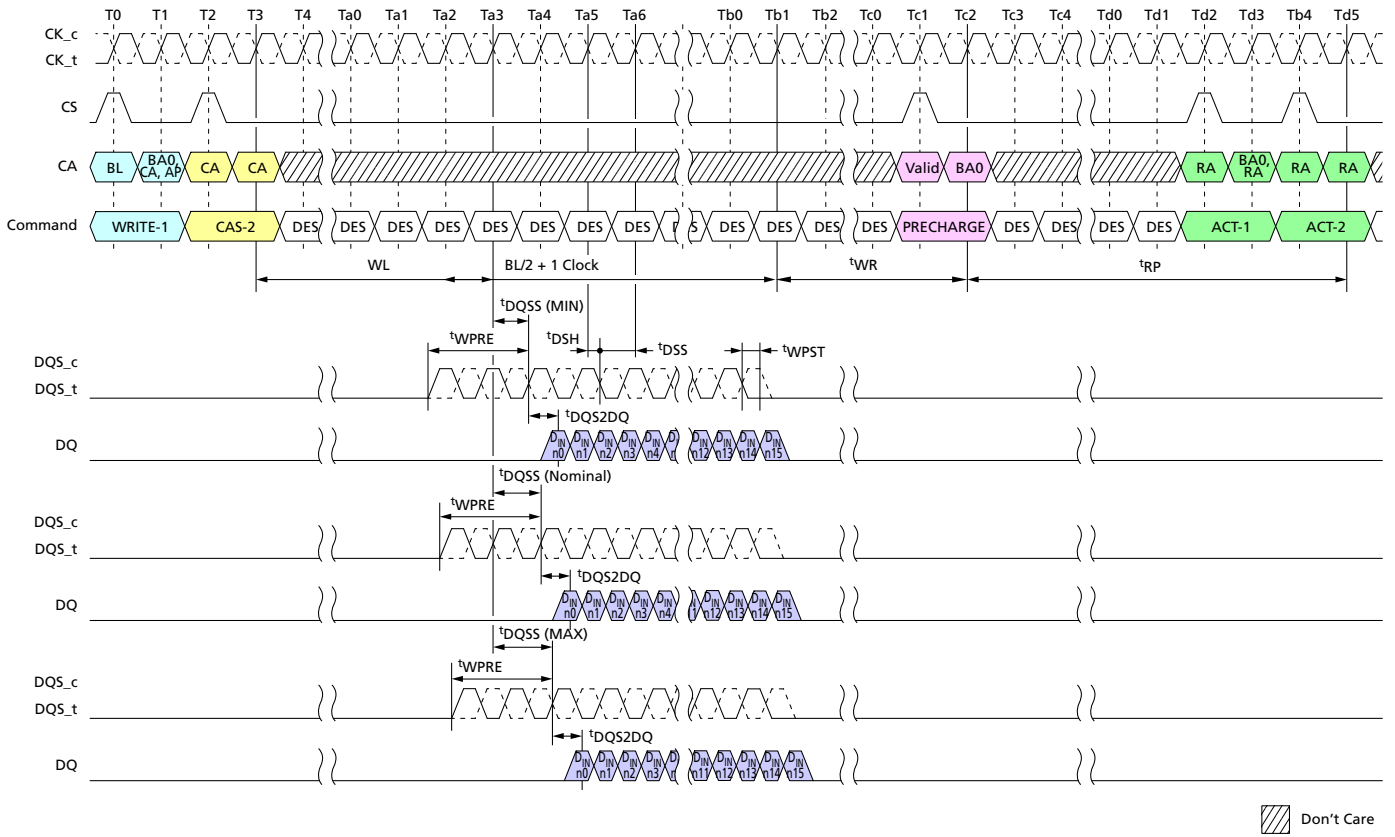
Burst WRITE Operation

A burst WRITE command is initiated with CKE, CS, and CA[5:0] asserted to the proper state at the rising edge of CK, as defined by the Command Truth Table. Column addresses C[3:2] should be driven LOW for burst WRITE commands, and column addresses C[1:0] are not transmitted on the CA bus and are assumed to be zero so that the starting column burst address is always aligned with a 32-byte boundary. The WRITE latency (WL) is defined from the last rising edge of the clock that completes a WRITE command (for example, the second rising edge of the CAS-2 command) to the rising edge of the clock from which t^{DQSS} is measured. The first valid latching edge of DQS must be driven $WL \times t^{\text{CK}} + t^{\text{DQSS}}$ after the rising edge of clock that completes a WRITE command.

The device uses an unmatched DQS DQ path for lower power, so the DQS strobe must arrive at the SDRAM ball prior to the DQ signal by t^{DQS2DQ} . The DQS strobe output must be driven t^{WPRE} before the first valid rising strobe edge. The t^{WPRE} preamble is required to be $2 \times t^{\text{CK}}$ at any speed ranges. The DQS strobe must be trained to arrive at the DQ pad latch center-aligned with the DQ data. The DQ data must be held for T_{diVW} , and the DQS must be periodically trained to stay roughly centered in the T_{diVW} . Burst data is captured by the SDRAM on successive edges of DQS until the 16- or 32-bit data burst is complete. The DQS strobe must remain active (toggling) for t^{WPST} (write postamble) after the completion of the burst WRITE. After a burst WRITE operation, t^{WR} must be satisfied before a PRECHARGE command to the same bank can be issued. Signal input timings are measured relative to the cross point of DQS_t and DQS_c.



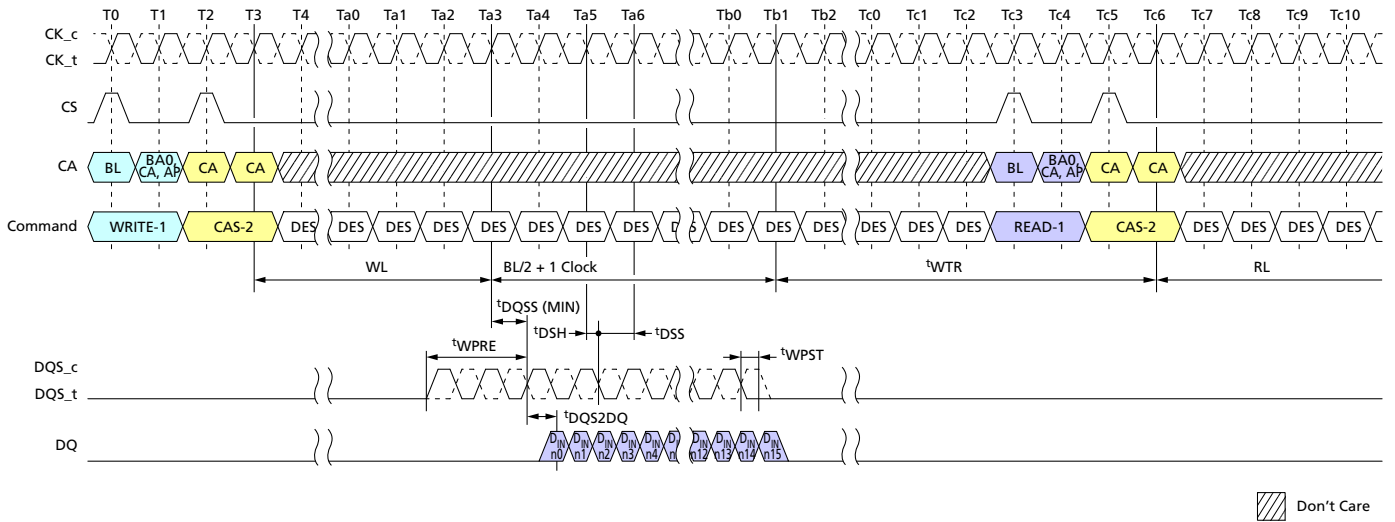
Figure 28: Burst WRITE Operation



- Notes:
1. BL = 16, Write postamble = 0.5nCK, DQ/DQS: V_{SSQ} termination.
 2. $D_{IN} n$ = data-in to column n .
 3. t_{WR} starts at the rising edge of CK after the last latching edge of DQS.
 4. DES commands are shown for ease of illustration; other commands may be valid at these times.



Figure 29: Burst Write Followed by Burst Read

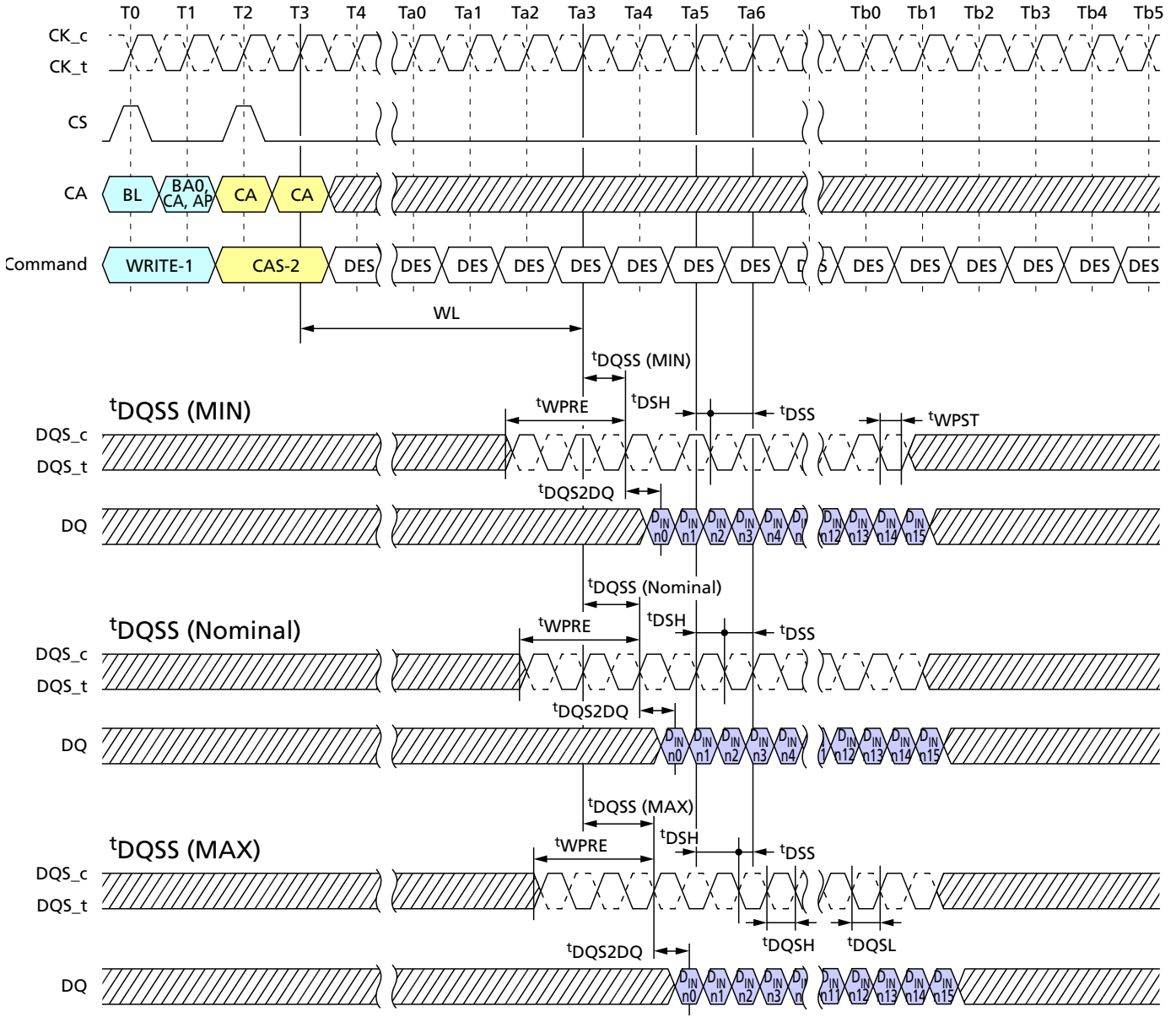


- Notes:
1. BL = 16, Write postamble = $0.5nCK$, DQ/DQS: V_{SSQ} termination.
 2. $D_{IN} n =$ data-in to column n .
 3. The minimum number of clock cycles from the burst WRITE command to the burst READ command for any bank is $[WL + 1 + BL/2 + RU(t_{WTR}/t_{CK})]$.
 4. t_{WTR} starts at the rising edge of CK after the last latching edge of DQS.
 5. DES commands are shown for ease of illustration; other commands may be valid at these times.



Write Timing

Figure 30: Write Timing



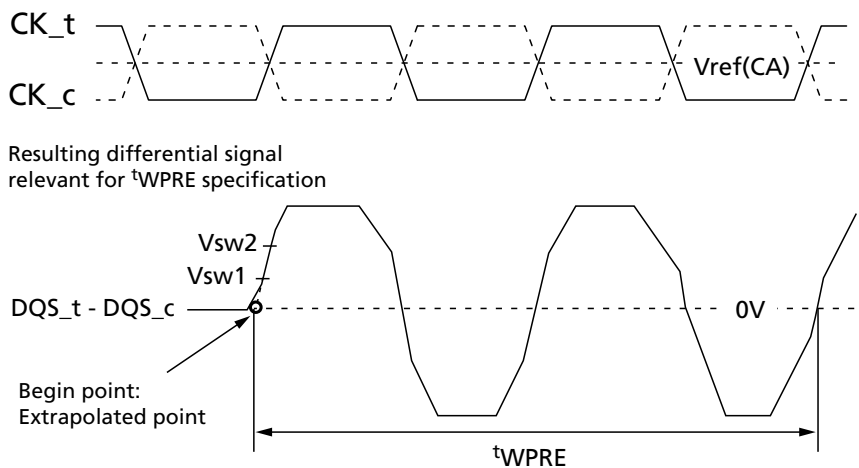
Don't Care

- Notes:
1. BL = 16, Write postamble = 0.5nCK.
 2. D_{IN} n = data-in to column n.
 3. DES commands are shown for ease of illustration; other commands may be valid at these times.



^tWPRE Calculation for ATE (Automatic Test Equipment)

Figure 31: Method for Calculating ^tWPRE Transitions and Endpoints



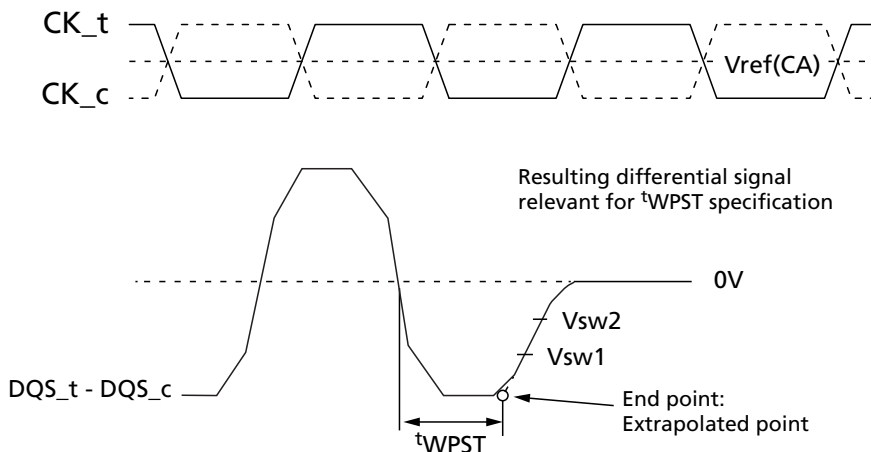
Note: 1. Termination condition for DQS_t, DQS_c, DQ, and DMI = 50 ohms to V_{SSQ}.

Table 87: Method for Calculating ^tWPRE Transitions and Endpoints

| Measured Parameter | Measured Parameter Symbol | Vsw1 | Vsw2 | Unit |
|--|---------------------------|---------------------------|---------------------------|------|
| DQS_t, DQS_c differential write preamble | ^t WPRE | V _{IHL_AC} × 0.3 | V _{IHL_AC} × 0.7 | V |

^tWPST Calculation for ATE (Automatic Test Equipment)

Figure 32: Method for Calculating ^tWPST Transitions and Endpoints



- Notes:
1. Termination condition for DQS_t, DQS_c, DQ, and DMI = 50 ohms to V_{SSQ}.
 2. Write postamble: 0.5^tCK
 3. The method for calculating differential pulse widths for 1.5^tCK postamble is same as 0.5^tCK postamble.



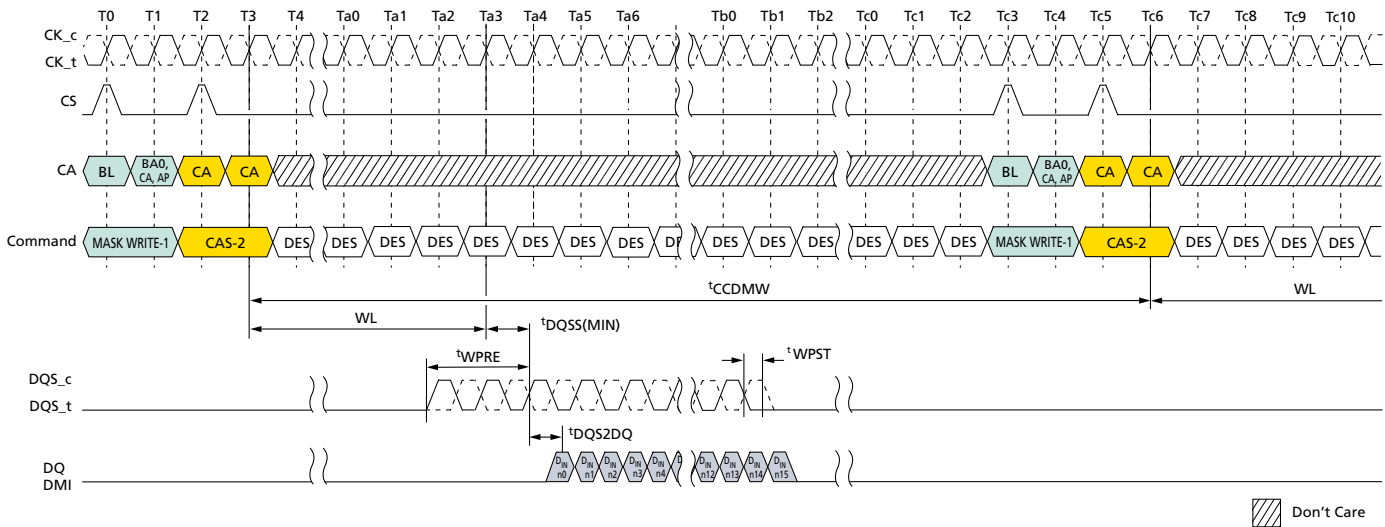
Table 88: Reference Voltage for t_{WPST} Timing Measurements

| Measured Parameter | Measured Parameter Symbol | Vsw1 | Vsw2 | Unit |
|---|---------------------------|-----------------------------|-----------------------------|------|
| DQS_t, DQS_c differential write postamble | t_{WPST} | $-(V_{IHL_AC} \times 0.7)$ | $-(V_{IHL_AC} \times 0.3)$ | V |

MASK WRITE Operation

The device requires that WRITE operations that include a byte mask anywhere in the burst sequence must use the MASK WRITE command. This allows the device to implement efficient data protection schemes based on larger data blocks. The MASK WRITE-1 command is used to begin the operation, followed by a CAS-2 command. A MASKED WRITE command to the same bank cannot be issued until t_{CCDMW} later, to allow the device to finish the internal READ-MODIFY-WRITE operation. One data-mask-invert (DMI) pin is provided per byte lane, and the data-mask-invert timings match data bit (DQ) timing. See Data Mask Invert for more information on the use of the DMI signal.

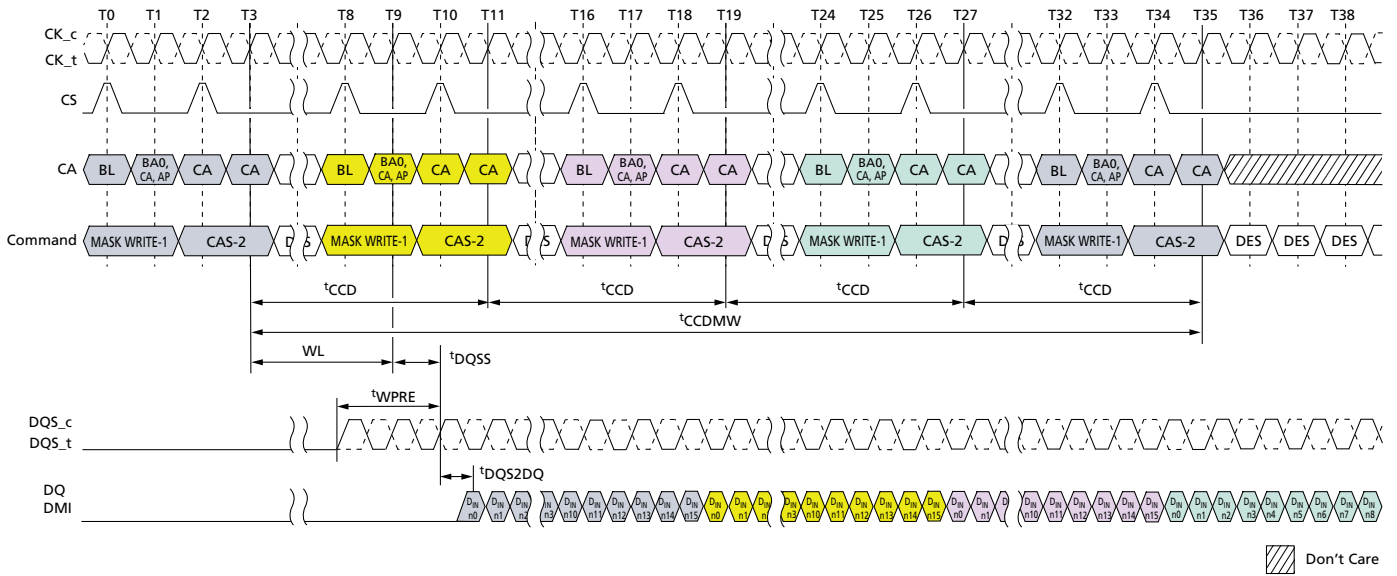
Figure 33: MASK WRITE Command – Same Bank



- Notes:
1. BL = 16, Write postamble = $0.5nCK$, DQ/DQS: V_{SSQ} termination.
 2. $D_{IN} n$ = data-in to column n .
 3. Mask-write supports only BL16 operations. For BL32 configuration, the system needs to insert only 16-bit wide data for MASKED WRITE operation.
 4. DES commands are shown for ease of illustration; other commands may be valid at these time.



Figure 34: MASK WRITE Command – Different Bank



- Notes:
1. BL = 16, DQ/DQS/DMI: V_{SSQ} termination.
 2. $D_{IN} n$ = data-in to column n .
 3. Mask-write supports only BL16 operations. For BL32 configuration, the system needs to insert only 16-bit wide data for MASKED WRITE operation.
 4. DES commands are shown for ease of illustration; other commands may be valid at these time.



Mask Write Timing Constraints for BL16

Table 89: Same Bank (ODT Disabled)

| Next CMD Current CMD | ACTIVE | READ (BL = 16 or 32) | WRITE (BL = 16 or 32) | MASK WRITE | PRECHARGE |
|-------------------------|--|--------------------------------------|---|---|--|
| ACTIVE | Illegal | $RU(t_{RCD}/t_{CK})$ | $RU(t_{RCD}/t_{CK})$ | $RU(t_{RCD}/t_{CK})$ | $RU(t_{RAS}/t_{CK})$ |
| READ (with BL = 16) | Illegal | 8^1 | $RL + RU(t_{DQSC}(MAX)/t_{CK}) + BL/2 - WL + t_{WPRE} + RD(t_{RPST})$ | $RL + RU(t_{DQSC}(MAX)/t_{CK}) + BL/2 - WL + t_{WPRE} + RD(t_{RPST})$ | $BL/2 + \text{MAX}\{(8, RU(t_{RTP}/t_{CK}))\} - 8$ |
| READ (with BL = 32) | Illegal | 16^2 | $RL + RU(t_{DQSC}(MAX)/t_{CK}) + BL/2 - WL + t_{WPRE} + RD(t_{RPST})$ | $RL + RU(t_{DQSC}(MAX)/t_{CK}) + BL/2 - WL + t_{WPRE} + RD(t_{RPST})$ | $BL/2 + \text{MAX}\{(8, RU(t_{RTP}/t_{CK}))\} - 8$ |
| WRITE (with BL = 16) | Illegal | $WL + 1 + BL/2 + RU(t_{WTR}/t_{CK})$ | 8^1 | t_{CCDMW}^3 | $WL + 1 + BL/2 + RU(t_{WR}/t_{CK})$ |
| WRITE (with BL = 32) | Illegal | $WL + 1 + BL/2 + RU(t_{WTR}/t_{CK})$ | 16^2 | $t_{CCDMW} + 8^4$ | $WL + 1 + BL/2 + RU(t_{WR}/t_{CK})$ |
| MASK WRITE | Illegal | $WL + 1 + BL/2 + RU(t_{WTR}/t_{CK})$ | t_{CCD} | t_{CCDMW}^3 | $WL + 1 + BL/2 + RU(t_{WR}/t_{CK})$ |
| PRECHARGE | $RU(t_{RP}/t_{CK}), RU(t_{RPab}/t_{CK})$ | Illegal | Illegal | Illegal | 4 |

- Notes:
1. In the case of BL = 16, t_{CCD} is $8 \times t_{CK}$.
 2. In the case of BL = 32, t_{CCD} is $16 \times t_{CK}$.
 3. $t_{CCDMW} = 32 \times t_{CK}$ ($4 \times t_{CCD}$ at BL = 16).
 4. WRITE with BL = 32 operation is $8 \times t_{CK}$ longer than BL = 16.

Table 90: Different Bank (ODT Disabled)

| Next CMD Current CMD | ACTIVE | READ (BL = 16 or 32) | WRITE (BL = 16 or 32) | MASK WRITE | PRECHARGE |
|-------------------------|----------------------|--------------------------------------|---|---|-----------|
| ACTIVE | $RU(t_{RRD}/t_{CK})$ | 4 | 4 | 4 | 2^2 |
| READ (with BL = 16) | 4 | 8^1 | $RL + RU(t_{DQSC}(MAX)/t_{CK}) + BL/2 - WL + t_{WPRE} + RD(t_{RPST})$ | $RL + RU(t_{DQSC}(MAX)/t_{CK}) + BL/2 - WL + t_{WPRE} + RD(t_{RPST})$ | 2^2 |
| READ (with BL = 32) | 4 | 16^2 | $RL + RU(t_{DQSC}(MAX)/t_{CK}) + BL/2 - WL + t_{WPRE} + RD(t_{RPST})$ | $RL + RU(t_{DQSC}(MAX)/t_{CK}) + BL/2 - WL + t_{WPRE} + RD(t_{RPST})$ | 2^2 |
| WRITE (with BL = 16) | 4 | $WL + 1 + BL/2 + RU(t_{WTR}/t_{CK})$ | 8^1 | 8^1 | 2^2 |
| WRITE (with BL = 32) | 4 | $WL + 1 + BL/2 + RU(t_{WTR}/t_{CK})$ | 16^2 | 16^2 | 2^2 |
| MASK WRITE | 4 | $WL + 1 + BL/2 + RU(t_{WTR}/t_{CK})$ | 8^1 | 8^1 | 2^2 |



Table 90: Different Bank (ODT Disabled) (Continued)

| Next CMD Current CMD | ACTIVE | READ (BL = 16 or 32) | WRITE (BL = 16 or 32) | MASK WRITE | PRECHARGE |
|-------------------------|--------|-------------------------|--------------------------|------------|-----------|
| PRECHARGE | 4 | 4 | 4 | 4 | 4 |

- Notes: 1. In the case of BL = 16, t_{CCD} is $8 \times t_{CK}$
2. In the case of BL = 32, t_{CCD} is $16 \times t_{CK}$

Table 91: Same Bank (ODT Enabled)

| Next CMD Current CMD | ACTIVE | READ (BL = 16 or 32) | WRITE (BL = 16 or 32) | MASK WRITE | PRECHARGE |
|-------------------------|--|--------------------------------------|---|---|---|
| ACTIVE | Illegal | $RU(t_{RCD}/t_{CK})$ | $RU(t_{RCD}/t_{CK})$ | $RU(t_{RCD}/t_{CK})$ | $RU(t_{RAS}/t_{CK})$ |
| READ (with BL = 16) | Illegal | 8^1 | $RL + RU(t_{DQSK}(\text{MAX})/t_{CK}) + BL/2 + RD(t_{RPST}) - ODT_{Lon} - RD(t_{ODTon}(\text{MIN})/t_{CK})$ | $RL + RU(t_{DQSK}(\text{MAX})/t_{CK}) + BL/2 + RD(t_{RPST}) - ODT_{Lon} - RD(t_{ODTon}(\text{MIN})/t_{CK})$ | $BL/2 + \text{MAX}\{(8, RU(t_{RTP}/t_{CK})\} - 8$ |
| READ (with BL = 32) | Illegal | 16^2 | $RL + RU(t_{DQSK}(\text{MAX})/t_{CK}) + BL/2 + RD(t_{RPST}) - ODT_{Lon} - RD(t_{ODTon}(\text{MIN})/t_{CK})$ | $RL + RU(t_{DQSK}(\text{MAX})/t_{CK}) + BL/2 + RD(t_{RPST}) - ODT_{Lon} - RD(t_{ODTon}(\text{MIN})/t_{CK})$ | $BL/2 + \text{MAX}\{(8, RU(t_{RTP}/t_{CK})\} - 8$ |
| WRITE (with BL = 16) | Illegal | $WL + 1 + BL/2 + RU(t_{WTR}/t_{CK})$ | 8^1 | t_{CCDMW}^3 | $WL + 1 + BL/2 + RU(t_{WTR}/t_{CK})$ |
| WRITE (with BL = 32) | Illegal | $WL + 1 + BL/2 + RU(t_{WTR}/t_{CK})$ | 16^2 | $t_{CCDMW} + 8^4$ | $WL + 1 + BL/2 + RU(t_{WTR}/t_{CK})$ |
| MASK WRITE | Illegal | $WL + 1 + BL/2 + RU(t_{WTR}/t_{CK})$ | t_{CCD} | t_{CCDMW}^3 | $WL + 1 + BL/2 + RU(t_{WTR}/t_{CK})$ |
| PRECHARGE | $RU(t_{RP}/t_{CK}), RU(t_{RPab}/t_{CK})$ | Illegal | Illegal | Illegal | 4 |

- Notes: 1. In the case of BL = 16, t_{CCD} is $8 \times t_{CK}$.
2. In the case of BL = 32, t_{CCD} is $16 \times t_{CK}$.
3. $t_{CCDMW} = 32 \times t_{CK}$ ($4 \times t_{CCD}$ at BL = 16).
4. WRITE with BL = 32 operation is $8 \times t_{CK}$ longer than BL = 16.

Table 92: Different Bank (ODT Enabled)

| Next CMD Current CMD | ACTIVE | READ (BL = 16 or 32) | WRITE (BL = 16 or 32) | MASK WRITE | PRECHARGE |
|-------------------------|----------------------|-------------------------|---|---|-----------|
| ACTIVE | $RU(t_{RRD}/t_{CK})$ | 4 | 4 | 4 | 2^2 |
| READ (with BL = 16) | 4 | 8^1 | $RL + RU(t_{DQSK}(\text{MAX})/t_{CK}) + BL/2 + RD(t_{RPST}) - ODT_{Lon} - RD(t_{ODTon}(\text{MIN})/t_{CK})$ | $RL + RU(t_{DQSK}(\text{MAX})/t_{CK}) + BL/2 + RD(t_{RPST}) - ODT_{Lon} - RD(t_{ODTon}(\text{MIN})/t_{CK})$ | 2^2 |



Table 92: Different Bank (ODT Enabled) (Continued)

| Next CMD Current CMD | ACTIVE | READ (BL = 16 or 32) | WRITE (BL = 16 or 32) | MASK WRITE | PRECHARGE |
|-------------------------|--------|---------------------------------|---|---|----------------|
| READ (with BL = 32) | 4 | 16 ² | RL + RU(tDQSK(MAX)/tCK + BL/2 + RD(tRPST) - ODTLon - RD(tODTon(MIN)/tCK) | RL + RU(tDQSK(MAX)/tCK + BL/2 + RD(tRPST) - ODTLon - RD(tODTon(MIN)/tCK) | 2 ² |
| WRITE (with BL = 16) | 4 | WL + 1+ BL/2 + RU(tWTR/tCK) | 8 ¹ | 8 ¹ | 2 ² |
| WRITE (with BL = 32) | 4 | WL + 1 + BL/2 + RU(tWTR/tCK) | 16 ² | 16 ² | 2 ² |
| MASK WRITE | 4 | WL + 1 + BL/2 + RU(tWTR/tCK) | 8 ¹ | 8 ¹ | 2 ² |
| PRECHARGE | 4 | 4 | 4 | 4 | 4 |

- Notes: 1. In the case of BL = 16, tCCD is 8 x tCK.
2. In the case of BL = 32, tCCD is 16 x tCK.

Data Mask and Data Bus Inversion (DBI [DC]) Function

Data mask (DM) is supported for WRITE operations and the data bus inversion DBI (DC) is supported for READ, WRITE, MASK WRITE, MRR, and MRW operations. DM and DBI (DC) functions are supported with byte granularity. DBI (DC) for READ operations (READ, MRR) can be enabled or disabled via MR3 OP[6]. DBI (DC) for WRITE operations (WRITE, MASK WRITE, MRW) can be enabled or disabled via MR3 OP[7]. DM for MASK WRITE operations can be enabled or disabled via MR13 OP[5]. The device has one data mask inversion (DMI) pin per byte and a total of two DMI pins per channel. The DMI signal is a bidirectional DDR signal, is sampled with the DQ signals, and is electrically identical to a DQ signal.

There are eight possible states for the device with the DM and DBI (DC) functions.

Table 93: Function Behavior of DMI Signal During WRITE, MASKED WRITE, and READ Operations

| DM Function | Write DBI (DC) | Read DBI (DC) | DMI Signal | | | | | |
|-------------|----------------|---------------|-------------------------|-------------------------|-----------------------|-------------------------|-----------------------|-------------------------|
| | | | During WRITE | During MASKED WRITE | During READ | During MPC[WRITE-FIFO] | During MPC[READ-FIFO] | During MPC[READ-DQ CAL] |
| Disabled | Disabled | Disabled | Don't Care ¹ | Illegal ^{1, 3} | High-Z ² | Don't Care ¹ | High-Z ² | High-Z ² |
| Disabled | Enabled | Disabled | DBI (DC) ⁴ | Illegal ³ | High-Z ² | Train ⁹ | Train ¹⁰ | Train ¹¹ |
| Disabled | Disabled | Enabled | Don't Care ¹ | Illegal ³ | DBI (DC) ⁵ | Train ⁹ | Train ¹⁰ | Train ¹¹ |
| Disabled | Enabled | Enabled | DBI (DC) ⁴ | Illegal ³ | DBI (DC) ⁵ | Train ⁹ | Train ¹⁰ | Train ¹¹ |
| Enabled | Disabled | Disabled | Don't Care ⁶ | DM ⁷ | High-Z ² | Train ⁹ | Train ¹⁰ | Train ¹¹ |
| Enabled | Enabled | Disabled | DBI (DC) ⁴ | DBI (DC) ⁸ | High-Z ² | Train ⁹ | Train ¹⁰ | Train ¹¹ |
| Enabled | Disabled | Enabled | Don't Care ⁶ | DM ⁷ | DBI (DC) ⁵ | Train ⁹ | Train ¹⁰ | Train ¹¹ |



200b: x32 LPDDR4 SDRAM Data Mask and Data Bus Inversion (DBI [DC]) Function

Table 93: Function Behavior of DMI Signal During WRITE, MASKED WRITE, and READ Operations (Continued)

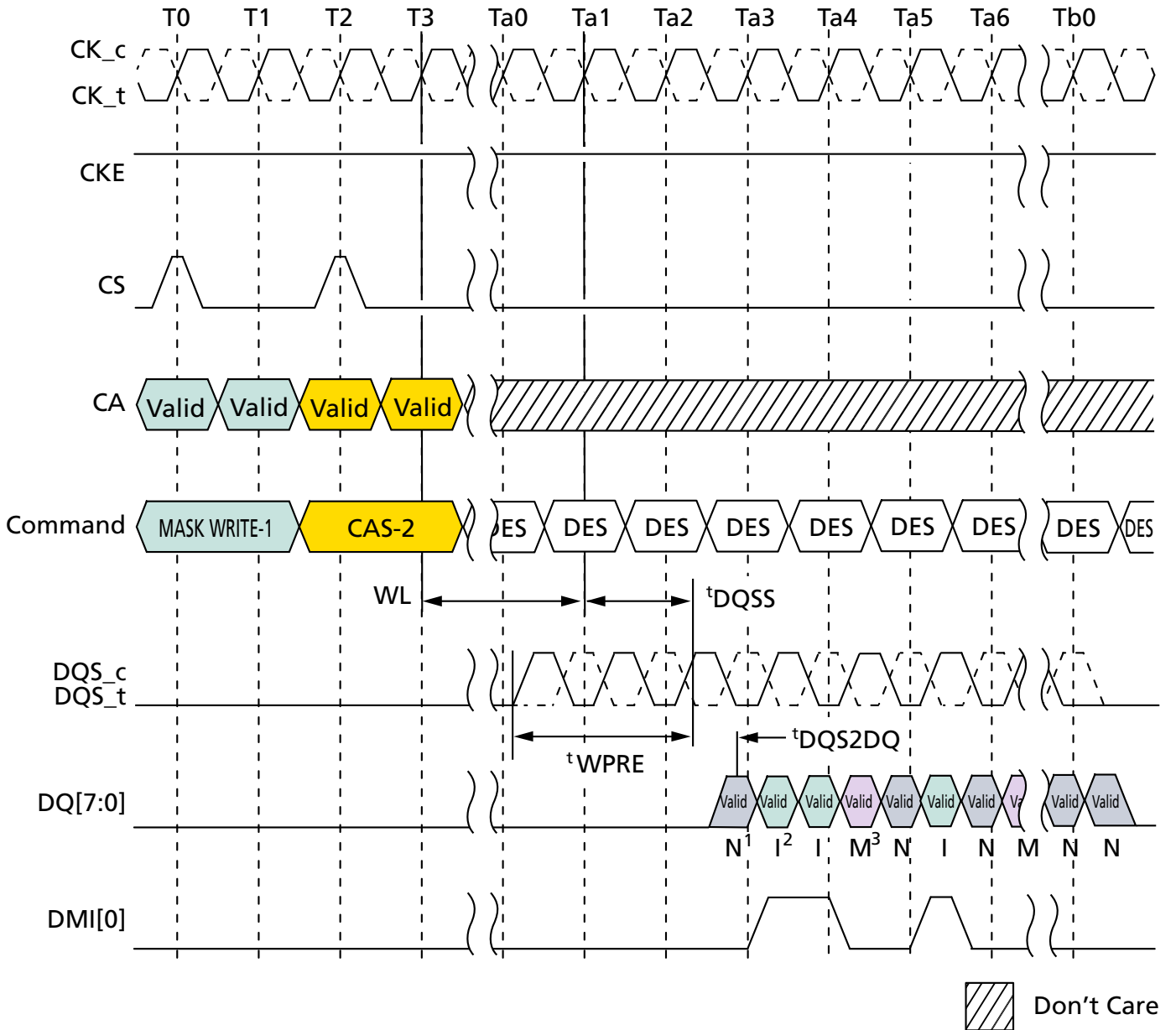
| DM Function | Write DBI (DC) | Read DBI (DC) | DMI Signal | | | | | |
|-------------|----------------|---------------|-----------------------|-----------------------|-----------------------|------------------------|-----------------------|-------------------------|
| | | | During WRITE | During MASKED WRITE | During READ | During MPC[WRITE-FIFO] | During MPC[READ-FIFO] | During MPC[READ DQ CAL] |
| Enabled | Enabled | Enabled | DBI (DC) ⁴ | DBI (DC) ⁸ | DBI (DC) ⁵ | Train ⁹ | Train ¹⁰ | Train ¹¹ |

- Notes:
1. The DMI input signal is "Don't Care." DMI input receivers are turned off.
 2. DMI output drivers are turned off.
 3. The MASK WRITE command is not allowed and is considered an illegal command when the DM function is disabled.
 4. The DMI signal is treated as DBI and indicates whether the device needs to invert the write data received on DQ within a byte. The device inverts write data received on the DQ inputs if DMI is sampled HIGH and leaves the write data non-inverted if DMI is sampled LOW.
 5. The device inverts read data on its DQ outputs associated within a byte and drives the DMI signal HIGH when more than four data bits = 1 within a given byte lane; otherwise, the device does not invert the read data and drives DMI signal LOW.
 6. The device does not perform a MASK operation when it receives a WRITE (or MRW) command. During the WRITE burst, the DMI signal must be driven LOW.
 7. The device requires an explicit MASKED WRITE command for all MASKED WRITE operations. The DMI signal is treated as a data mask (DM) and indicates which bytes within a burst will be masked. When the DMI signal is sampled HIGH, the device masks that beat of the burst for the given byte lane. All DQ input signals within a byte are "Don't Care" (either HIGH or LOW) when DMI is HIGH. When the DMI signal is sampled LOW, the device does not perform a MASK operation and data received on the DQ inputs is written to the array.
 8. The device requires an explicit MASKED WRITE command for all MASKED WRITE operations. The device masks the write data received on the DQ inputs if five or more data bits = 1 on DQ[2:7] or DQ[10:15] (for lower byte or upper byte respectively) and the DMI signal is LOW. Otherwise, the device does not perform the MASK operation and treats it as a legal DBI pattern. The DMI signal is treated as a DBI signal, and data received on the DQ input is written to the array.
 9. The DMI signal is treated as a training pattern. The device does not perform any MASK operation and does not invert write data received on the DQ inputs.
 10. The DMI signal is treated as a training pattern. The device returns the data pattern written to the WRITE-FIFO.
 11. The DMI signal is treated as a training pattern. For more information, see the Read DQ Calibration Training section.



200b: x32 LPDDR4 SDRAM
Data Mask and Data Bus Inversion (DBI [DC]) Function

Figure 35: MASKED WRITE Command with Write DBI Enabled; DM Enabled

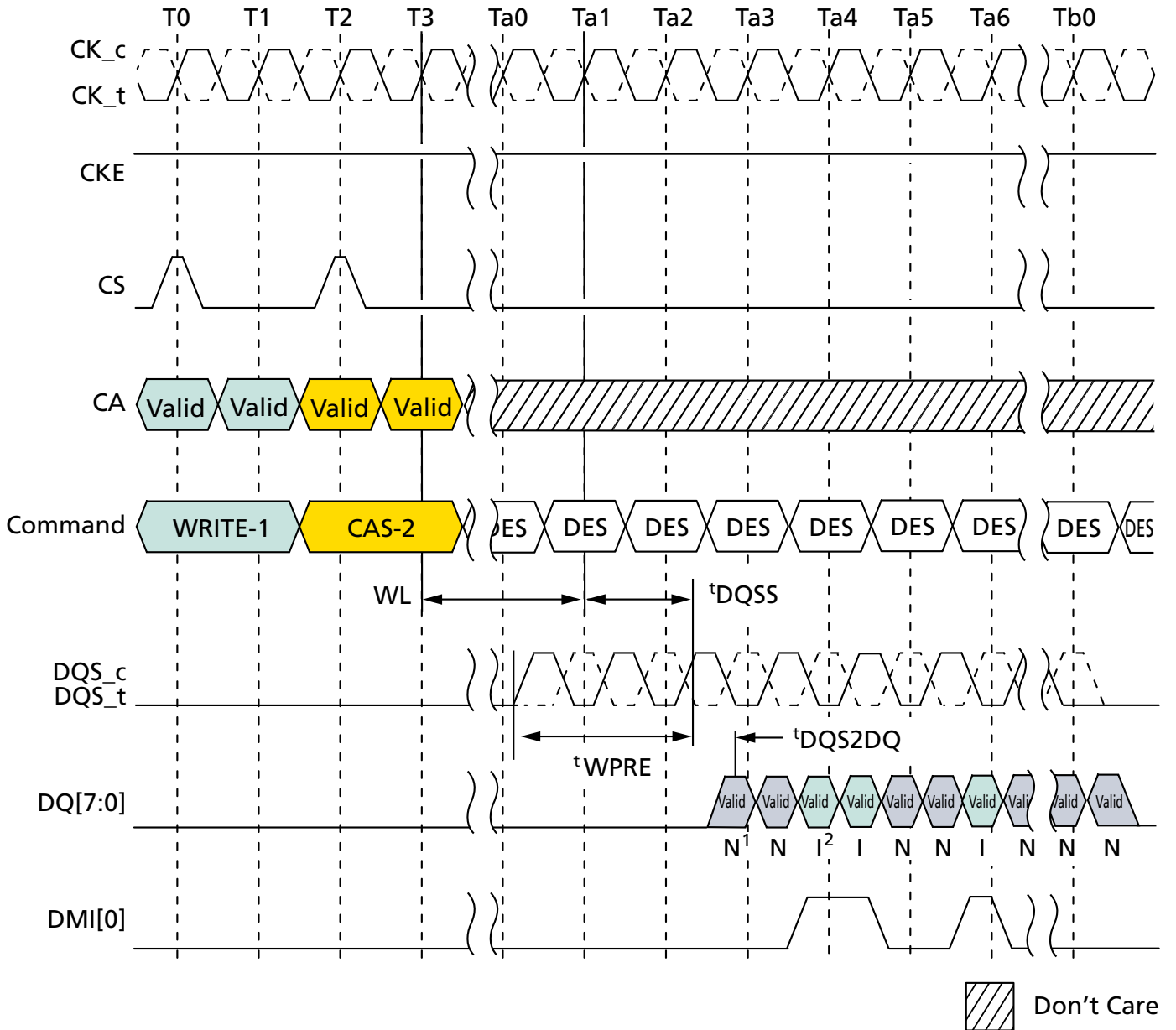


- Notes:
1. N: Input data is written to DRAM cell.
 2. I: Input data is inverted, then written to DRAM cell.
 3. M: Input data is masked. The total count of 1 data bits on DQ[7:2] is equal to or greater than five.
 4. Data mask (DM) is enable: MR13 OP [5] = 0, Data bus inversion (DBI) write is enable: MR3 OP[7] = 1.



**200b: x32 LPDDR4 SDRAM
Data Mask and Data Bus Inversion (DBI [DC]) Function**

Figure 36: WRITE Command with Write DBI Enabled; DM Disabled



- Notes:
1. N: Input data is written to DRAM cell.
 2. I: Input data is inverted, then written to DRAM cell.
 3. Data mask (DM) is disable: MR13 OP [5] = 1, Data bus inversion (DBI) write is enable: MR3 OP[7] = 1.



Preamble and Postamble Behavior

Preamble, Postamble Behavior in READ-to-READ Operations

The following illustrations show the behavior of the device's read DQS_t and DQS_c pins during cases where the preamble, postamble, and/or data clocking overlap.

DQS will be driven with the following priority

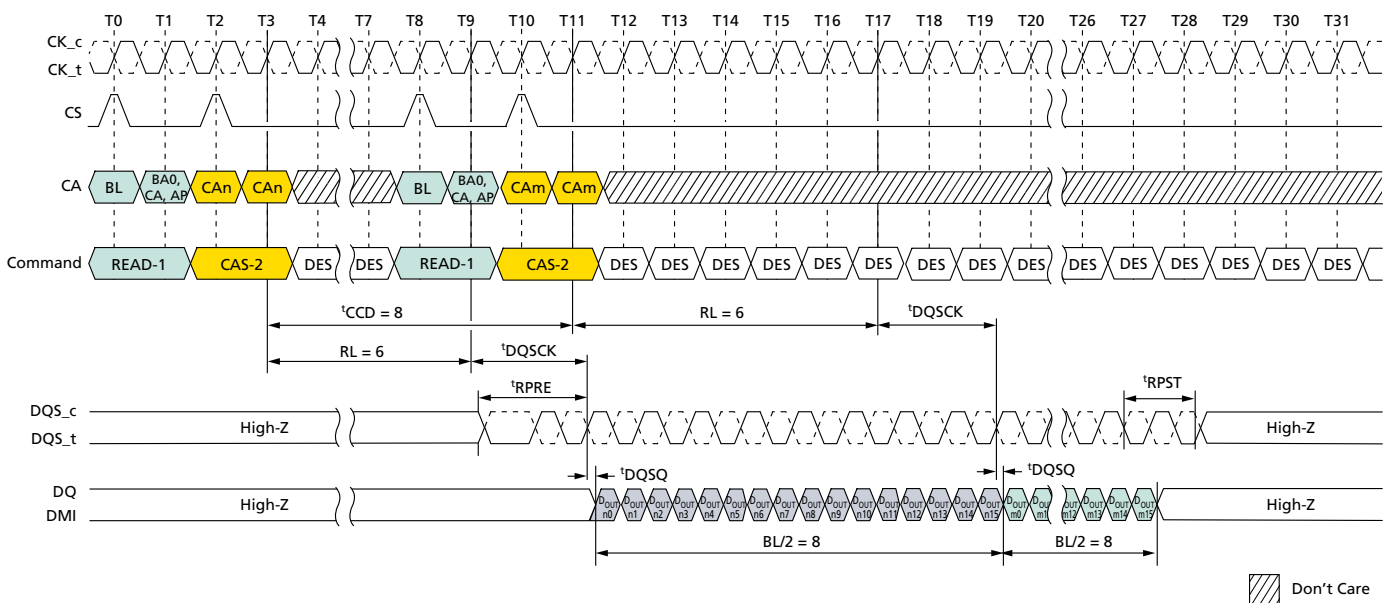
1. Data clocking edges will always be driven
2. Postamble
3. Preamble

Essentially the data clocking, preamble, and postamble will be ordered such that all edges will be driven.

Additional examples of seamless and borderline non-overlapping cases have been included for clarity.

READ-to-READ Operations – Seamless

Figure 37: READ Operations: $t_{CCD} = \text{MIN}$, Preamble = Toggle, 1.5nCK Postamble

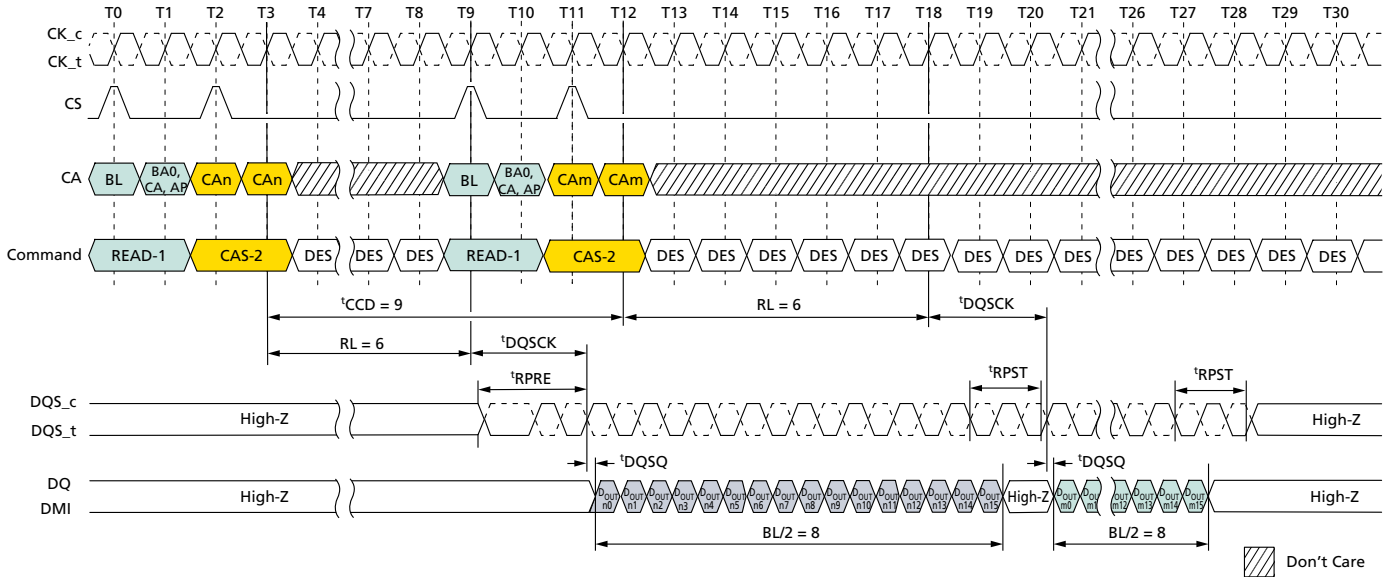


- Notes:
1. BL = 16 for column *n* and column *m*; RL = 6; Preamble = Toggle; Postamble = 1.5nCK.
 2. D_{OUT} *n/m* = data-out from column *n* and column *m*.
 3. DES commands are shown for ease of illustration; other commands may be valid at these times.



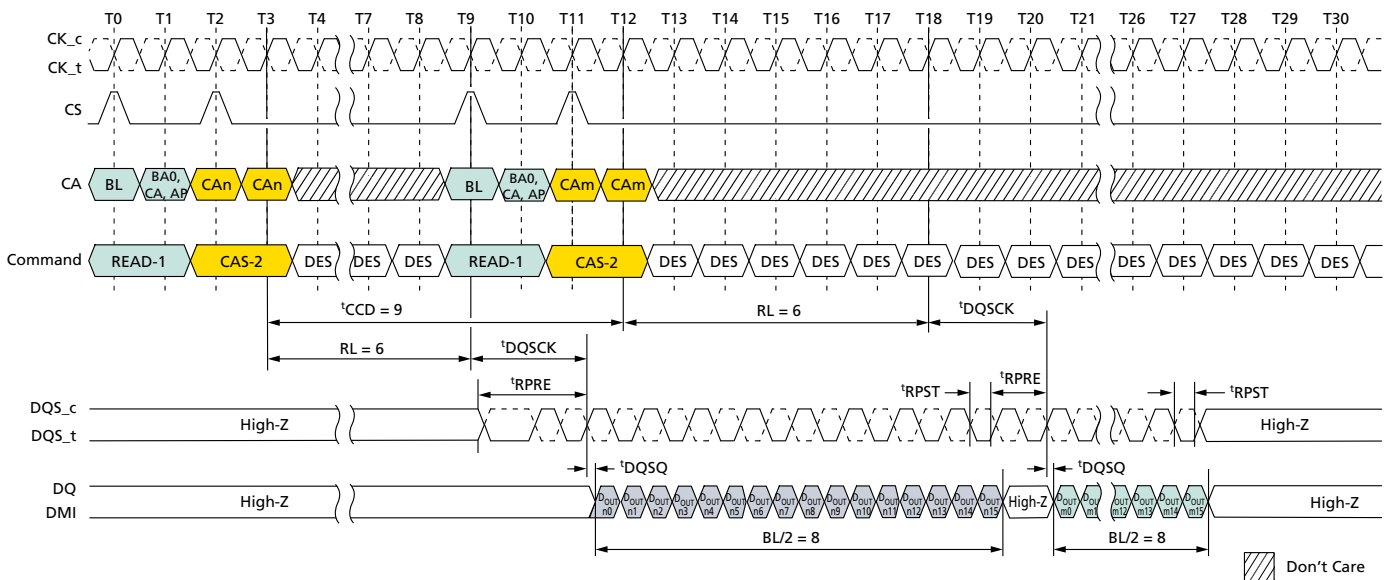
READ-to-READ Operations – Consecutive

Figure 38: Seamless READ: $t_{CCD} = MIN + 1$, Preamble = Toggle, 1.5nCK Postamble



- Notes: 1. BL = 16 for column n and column m ; RL = 6; Preamble = Toggle; Postamble = 1.5nCK.
2. $D_{OUT} n/m$ = data-out from column n and column m .
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 39: Consecutive READ: $t_{CCD} = MIN + 1$, Preamble = Toggle, 0.5nCK Postamble



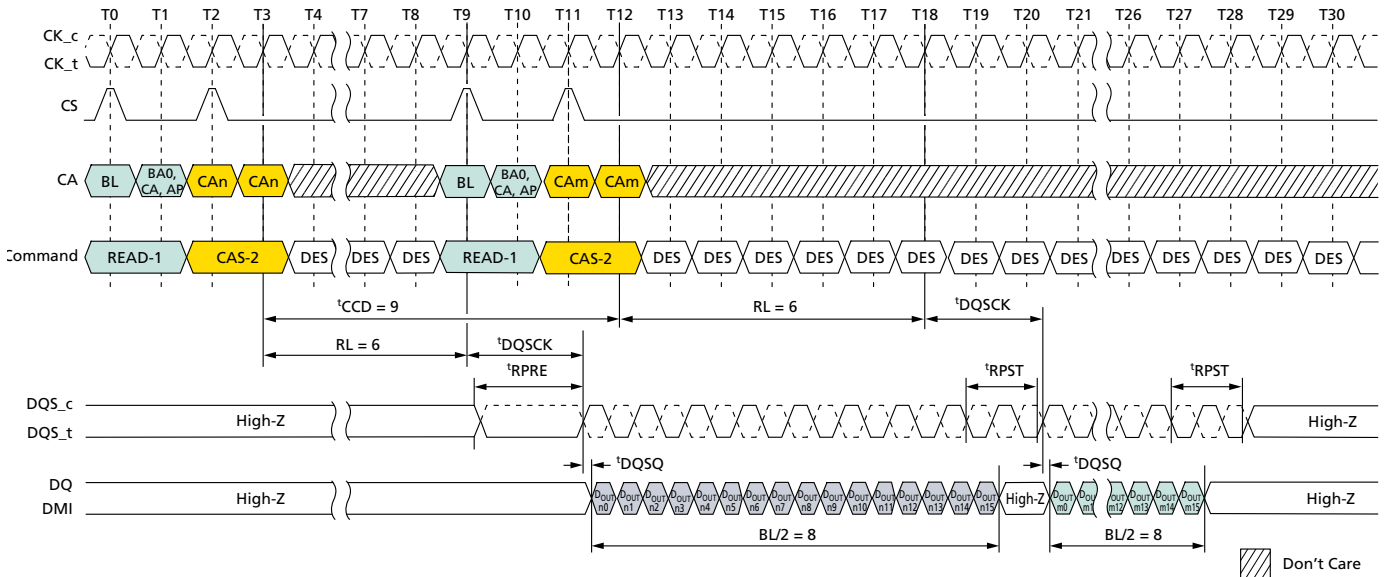
- Notes: 1. BL = 16 for column n and column m ; RL = 6; Preamble = Toggle; Postamble = 0.5nCK.
2. $D_{OUT} n/m$ = data-out from column n and column m .



**200b: x32 LPDDR4 SDRAM
Preamble and Postamble Behavior**

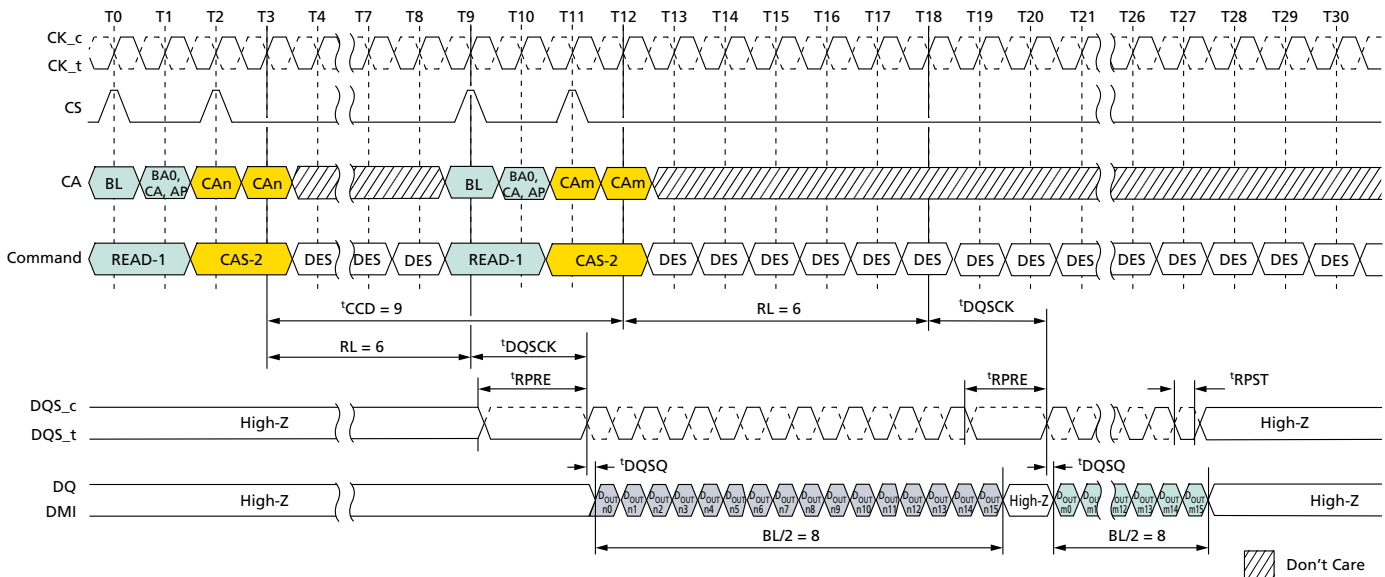
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 40: Consecutive READ: $t_{CCD} = MIN + 1$, Preamble = Static, $1.5nCK$ Postamble



- Notes:
1. BL = 16 for column n and column m ; $RL = 6$; Preamble = Static; Postamble = $1.5nCK$.
 2. $D_{OUT} n/m$ = data-out from column n and column m .
 3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 41: Consecutive READ: $t_{CCD} = MIN + 1$, Preamble = Static, $0.5nCK$ Postamble



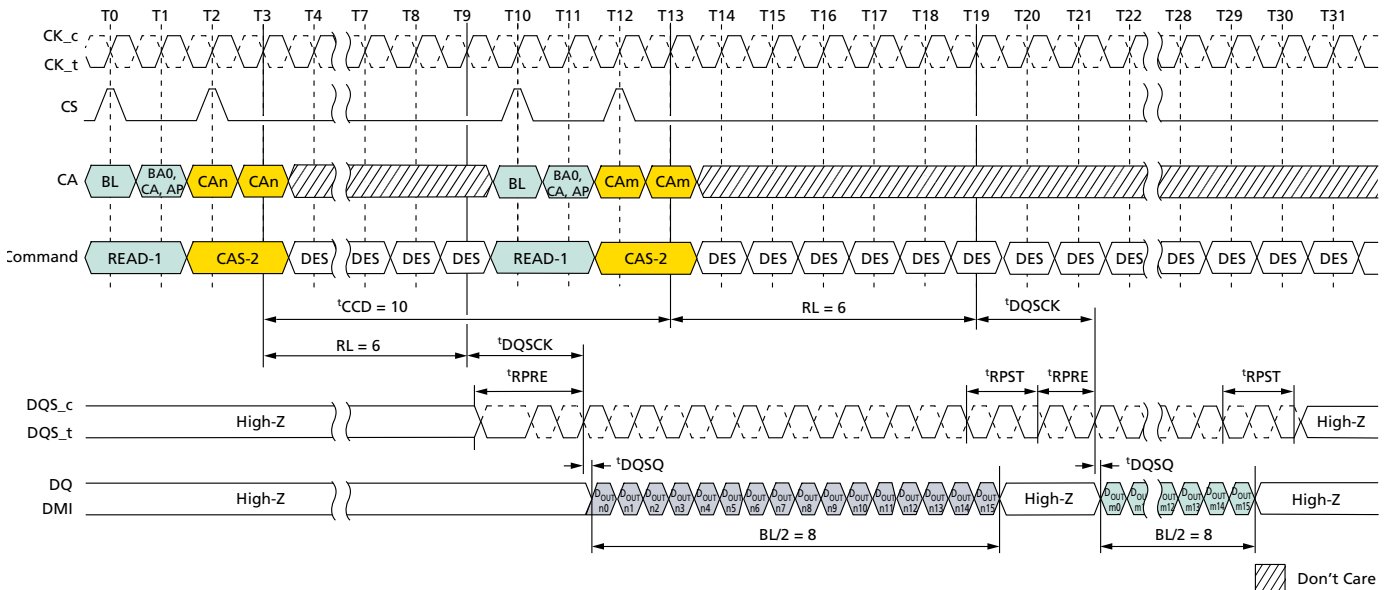
- Notes:
1. BL = 16 for column n and column m ; $RL = 6$; Preamble = Static; Postamble = $0.5nCK$.



**200b: x32 LPDDR4 SDRAM
Preamble and Postamble Behavior**

2. $D_{OUT\ n/m}$ = data-out from column n and column m .
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 42: Consecutive READ: $t_{CCD} = MIN + 2$, Preamble = Toggle, $1.5nCK$ Postamble

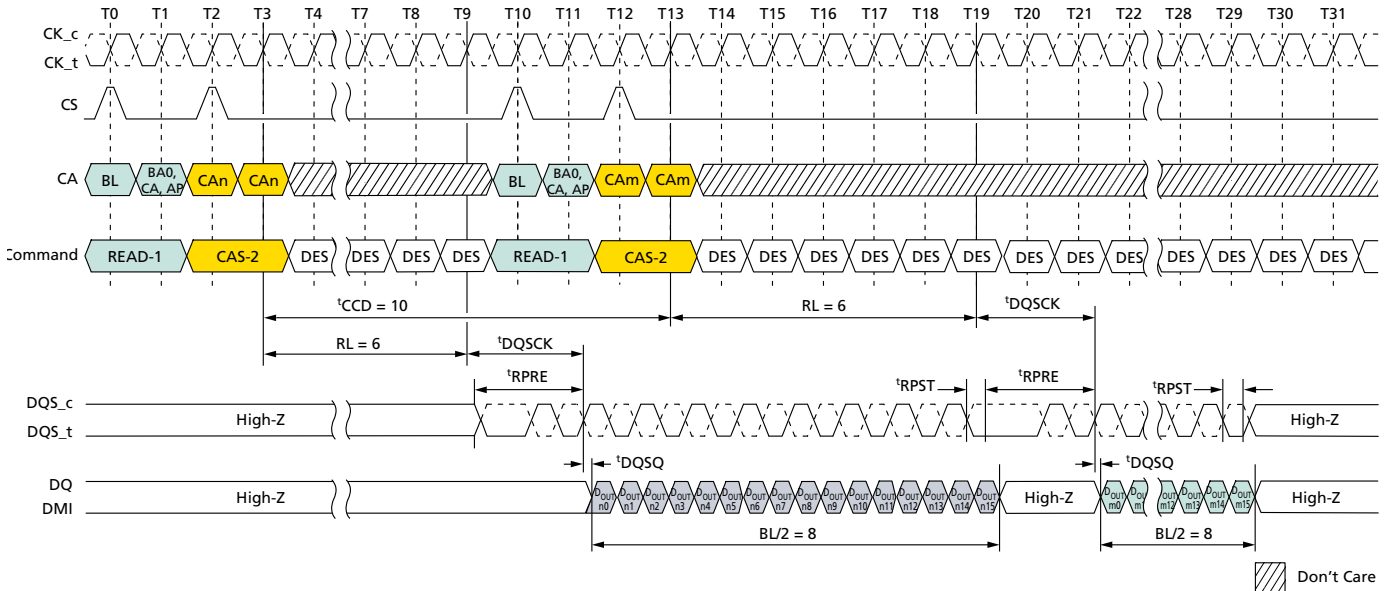


- Notes:
1. $BL = 16$ for column n and column m ; $RL = 6$; Preamble = Toggle; Postamble = $1.5nCK$.
 2. $D_{OUT\ n/m}$ = data-out from column n and column m .
 3. DES commands are shown for ease of illustration; other commands may be valid at these times.



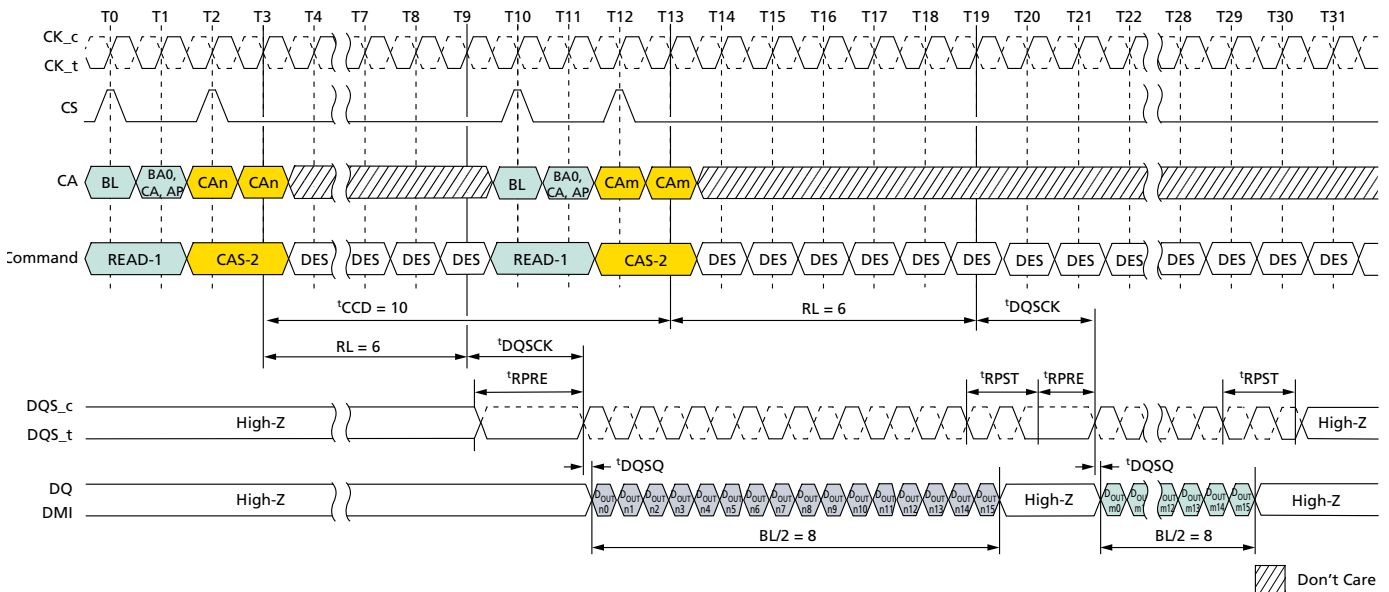
200b: x32 LPDDR4 SDRAM
Preamble and Postamble Behavior

Figure 43: Consecutive READ: $t_{CCD} = MIN + 2$, Preamble = Toggle, $0.5nCK$ Postamble



- Notes:
1. BL = 16 for column n and column m ; $RL = 6$; Preamble = Toggle; Postamble = $0.5nCK$.
 2. $D_{OUT\ n/m}$ = data-out from column n and column m .
 3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 44: Consecutive READ: $t_{CCD} = MIN + 2$, Preamble = Static, $1.5nCK$ Postamble



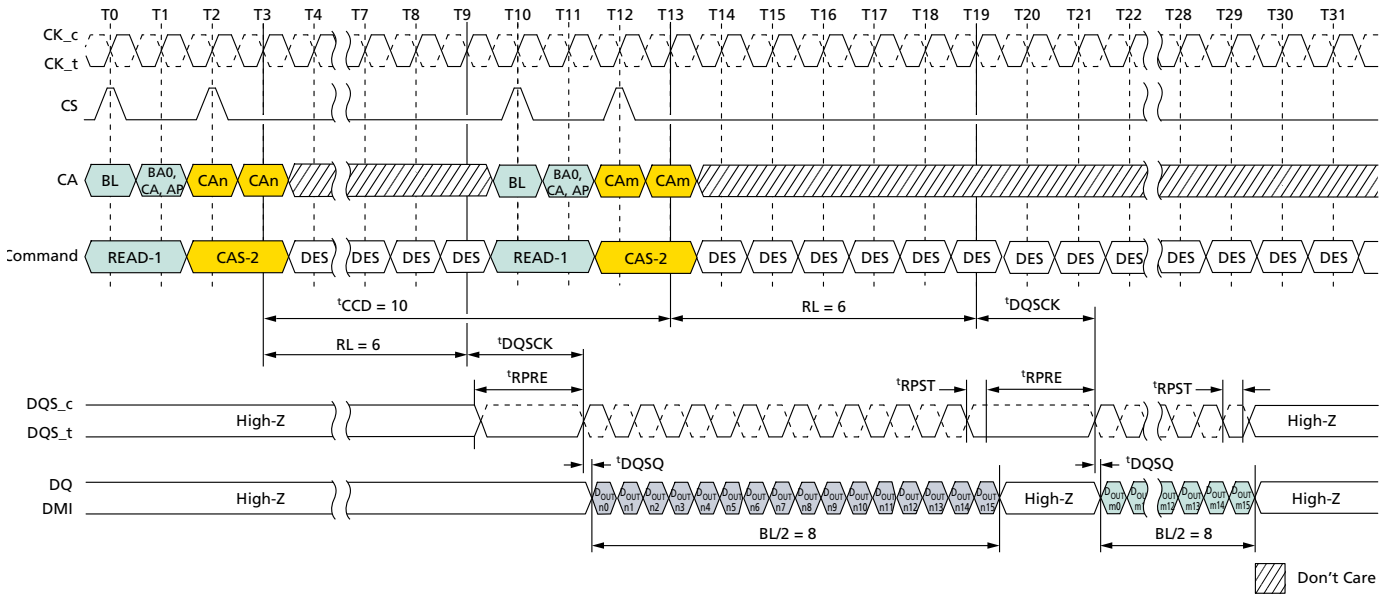
- Notes:
1. BL = 16 for column n and column m ; $RL = 6$; Preamble = Static; Postamble = $1.5nCK$.
 2. $D_{OUT\ n/m}$ = data-out from column n and column m .



**200b: x32 LPDDR4 SDRAM
Preamble and Postamble Behavior**

- DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 45: Consecutive READ: $t_{CCD} = \text{MIN} + 2$, Preamble = Static, $0.5n\text{CK}$ Postamble

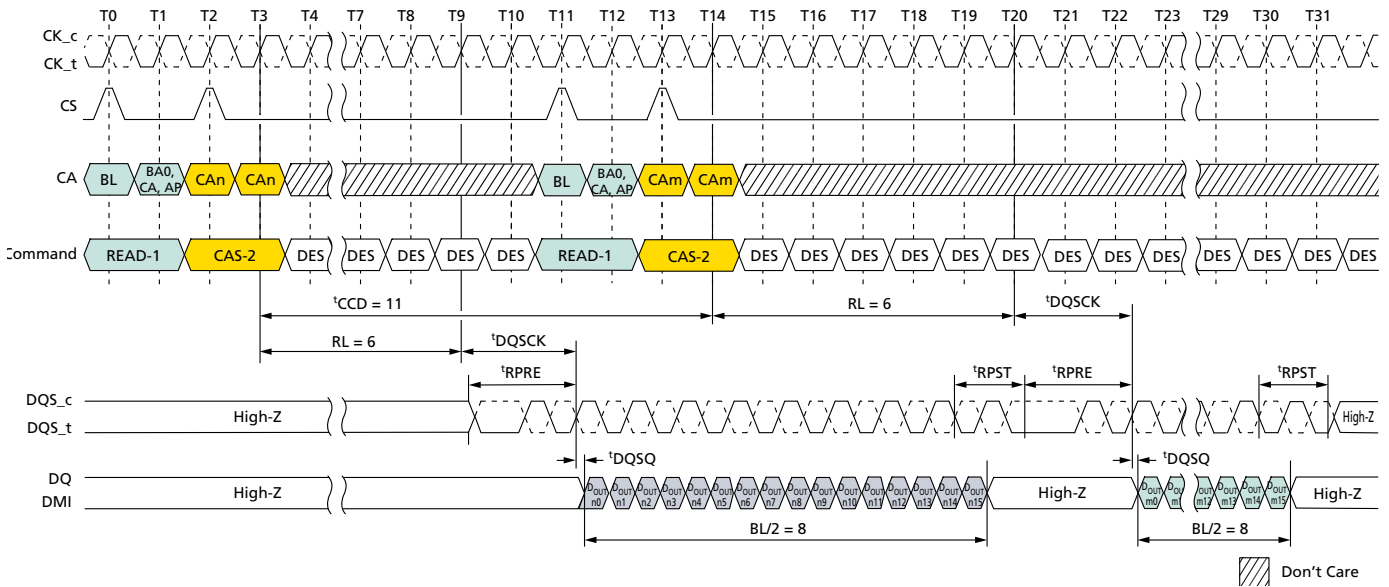


- Notes:
- BL = 16 for column n and column m ; RL = 6; Preamble = Static; Postamble = $0.5n\text{CK}$.
 - $D_{OUT} n/m$ = data-out from column n and column m .
 - DES commands are shown for ease of illustration; other commands may be valid at these times.



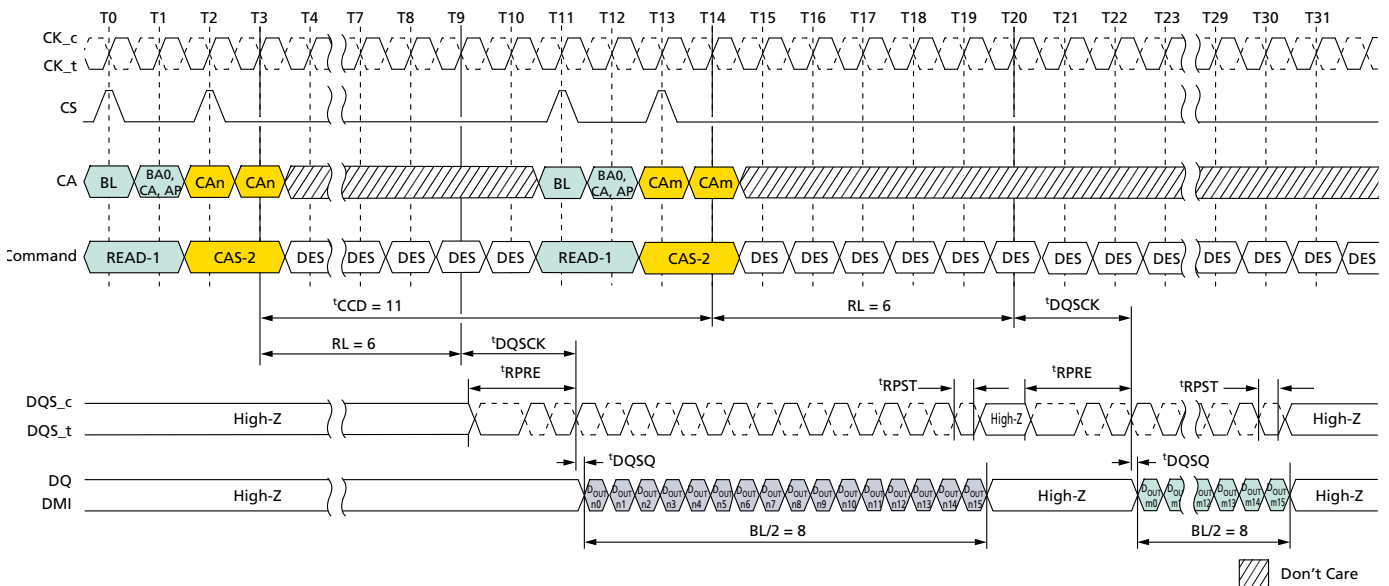
**200b: x32 LPDDR4 SDRAM
Preamble and Postamble Behavior**

Figure 46: Consecutive READ: $t_{CCD} = \text{MIN} + 3$, Preamble = Toggle, 1.5nCK Postamble



- Notes:
1. BL = 16 for column n and column m ; $RL = 6$; Preamble = Toggle; Postamble = 1.5nCK.
 2. $D_{OUT} n/m$ = data-out from column n and column m .
 3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 47: Consecutive READ: $t_{CCD} = \text{MIN} + 3$, Preamble = Toggle, 0.5nCK Postamble

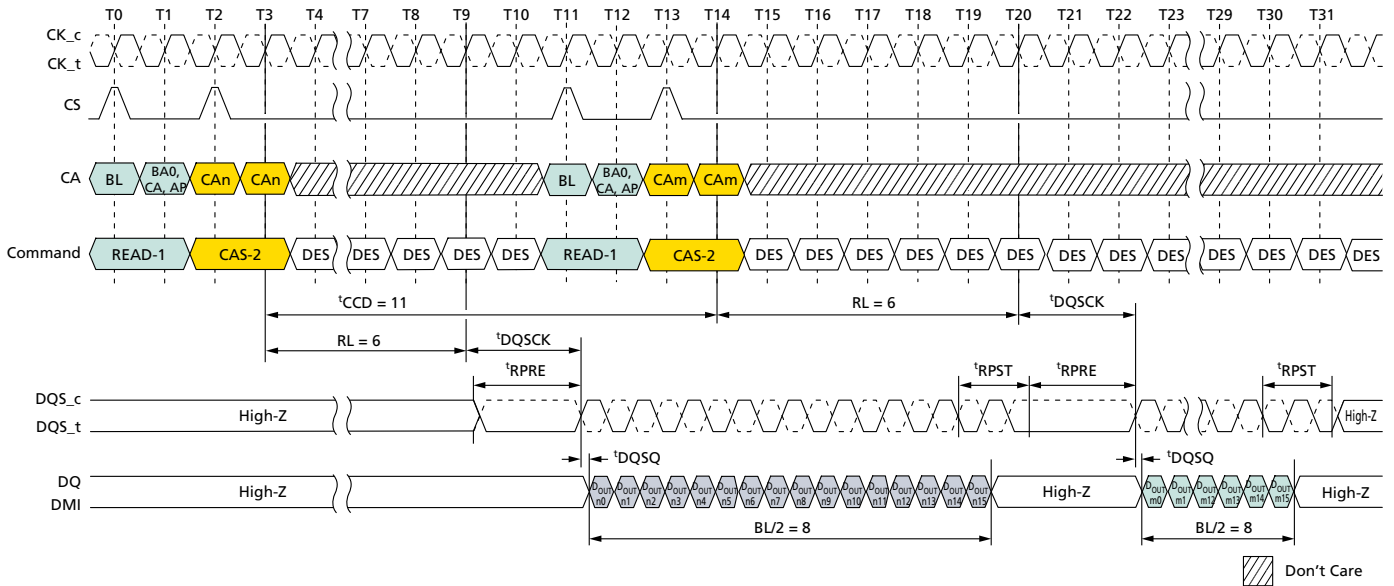


- Notes:
1. BL = 16 for column n and column m ; $RL = 6$; Preamble = Toggle; Postamble = 0.5nCK.
 2. $D_{OUT} n/m$ = data-out from column n and column m .
 3. DES commands are shown for ease of illustration; other commands may be valid at these times.



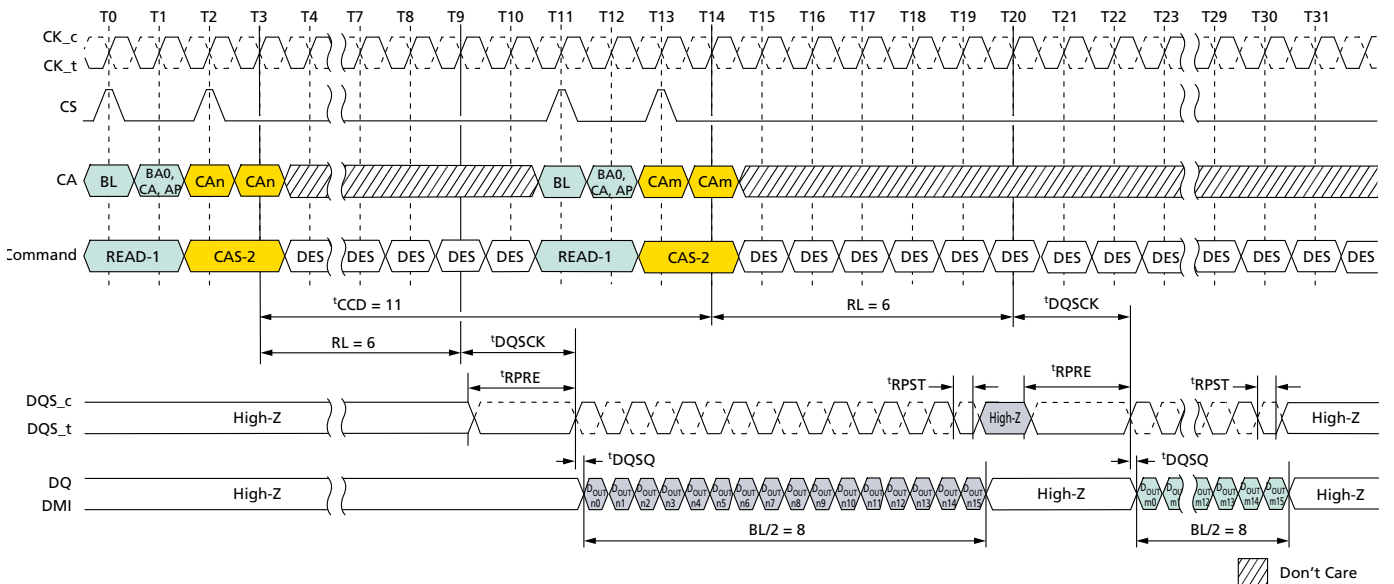
200b: x32 LPDDR4 SDRAM
Preamble and Postamble Behavior

Figure 48: Consecutive READ: $t_{CCD} = \text{MIN} + 3$, Preamble = Static, 1.5nCK Postamble



- Notes:
1. $BL = 16$ for column n and column m ; $RL = 6$; Preamble = Static; Postamble = $1.5nCK$.
 2. $D_{OUT\ n/m}$ = data-out from column n and column m .
 3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 49: Consecutive READ: $t_{CCD} = \text{MIN} + 3$, Preamble = Static, 0.5nCK Postamble

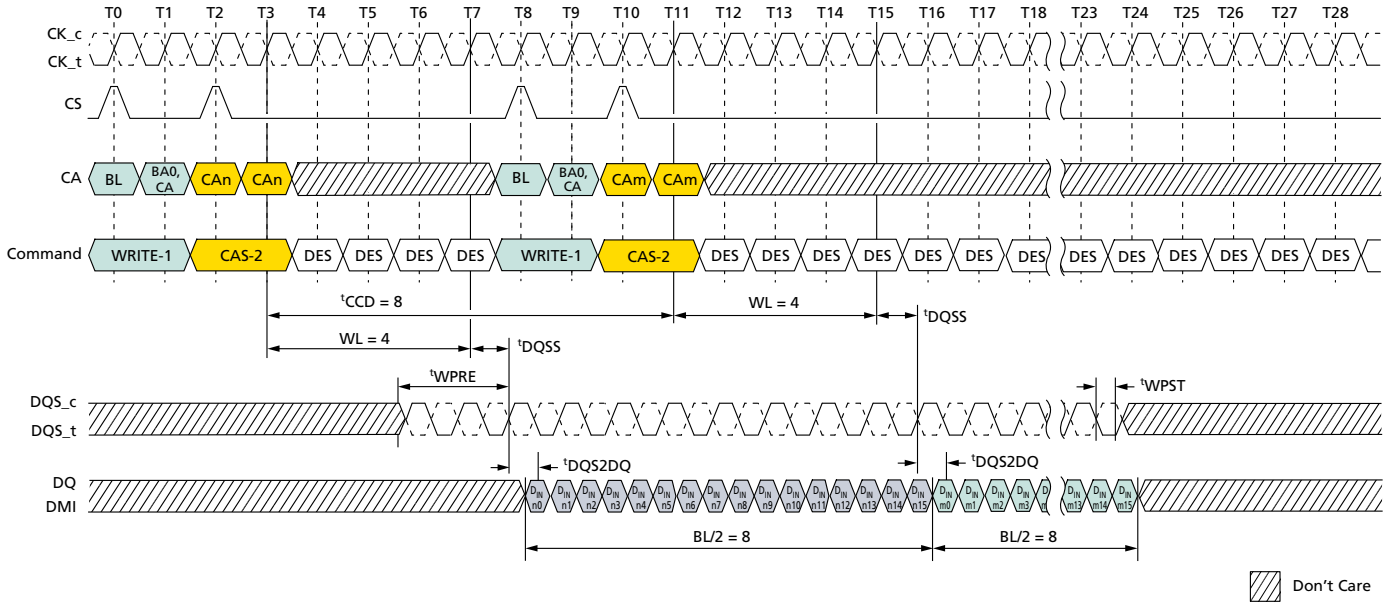


- Notes:
1. $BL = 16$ for column n and column m ; $RL = 6$, Preamble = Static; Postamble = $0.5nCK$
 2. $D_{OUT\ n/m}$ = data-out from column n and column m .
 3. DES commands are shown for ease of illustration; other commands may be valid at these times.



WRITE-to-WRITE Operations – Seamless

Figure 50: Seamless WRITE: $t_{CCD} = \text{MIN}, 0.5n\text{CK}$ Postamble

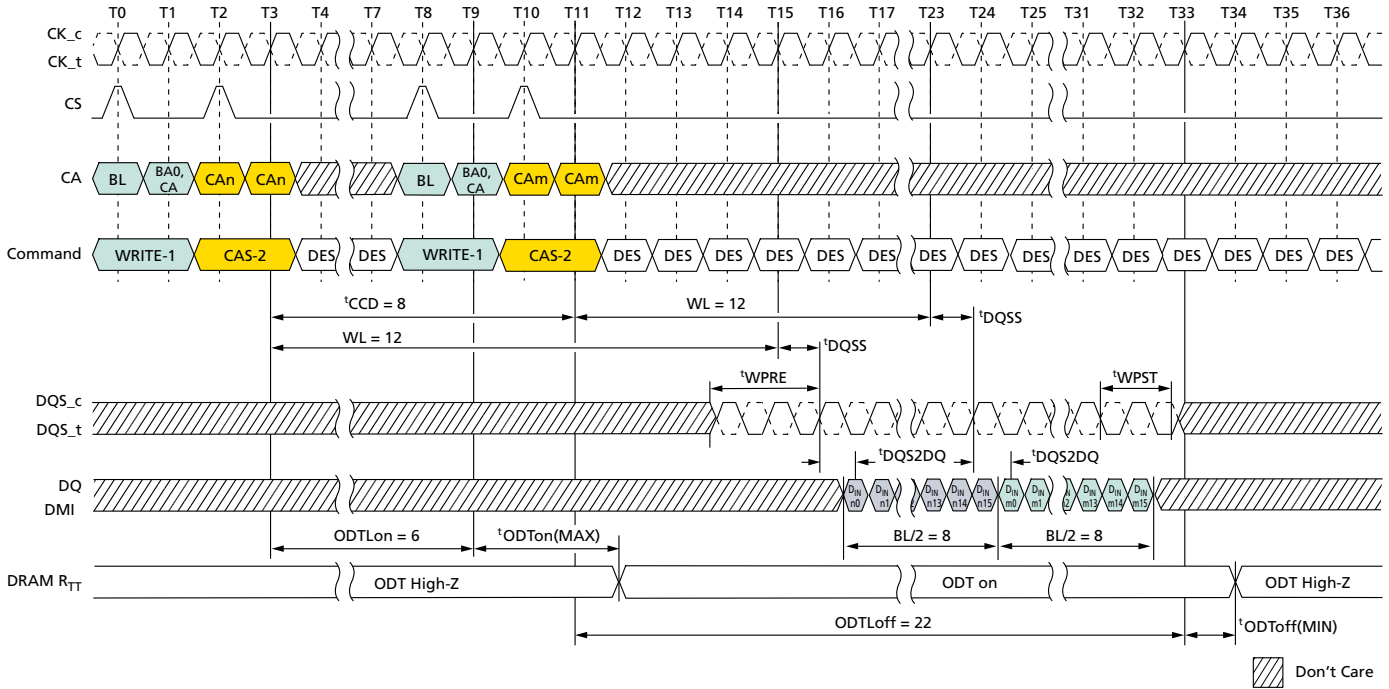


- Notes:
1. BL = 16, Write postamble = $0.5n\text{CK}$.
 2. $D_{IN\ n/m}$ = data-in from column n and column m .
 3. The minimum number of clock cycles from the burst WRITE command to the burst WRITE command for any bank is BL/2.
 4. DES commands are shown for ease of illustration; other commands may be valid at these times.



200b: x32 LPDDR4 SDRAM
Preamble and Postamble Behavior

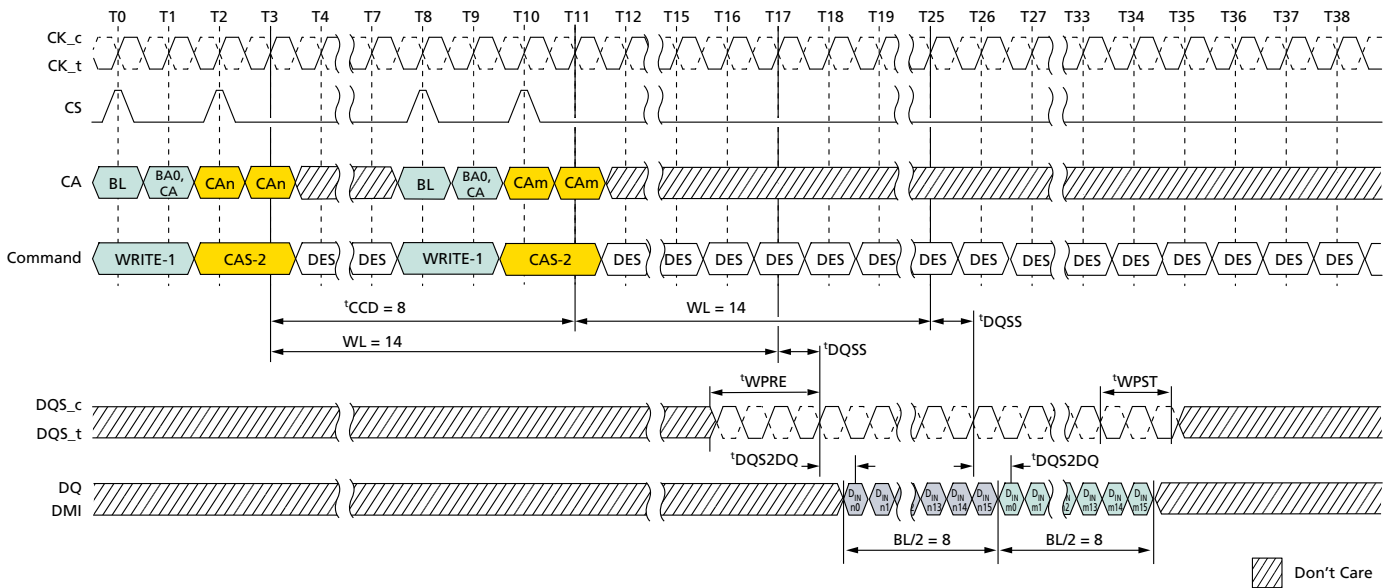
Figure 51: Seamless WRITE: $t_{CCD} = \text{MIN}$, $1.5n\text{CK}$ Postamble, $533 \text{ MHz} < \text{Clock Frequency} \leq 800 \text{ MHz}$, ODT Worst Timing Case



- Notes:
1. Clock frequency = 800 MHz, $t_{CK}(AVG) = 1.25\text{ns}$.
 2. $BL = 16$, Write postamble = $1.5n\text{CK}$.
 3. $D_{IN} n/m$ = data-in from column n and column m .
 4. The minimum number of clock cycles from the burst WRITE command to the burst WRITE command for any bank is $BL/2$.
 5. DES commands are shown for ease of illustration; other commands may be valid at these times.



Figure 52: Seamless WRITE: $t_{CCD} = \text{MIN}, 1.5n\text{CK}$ Postamble

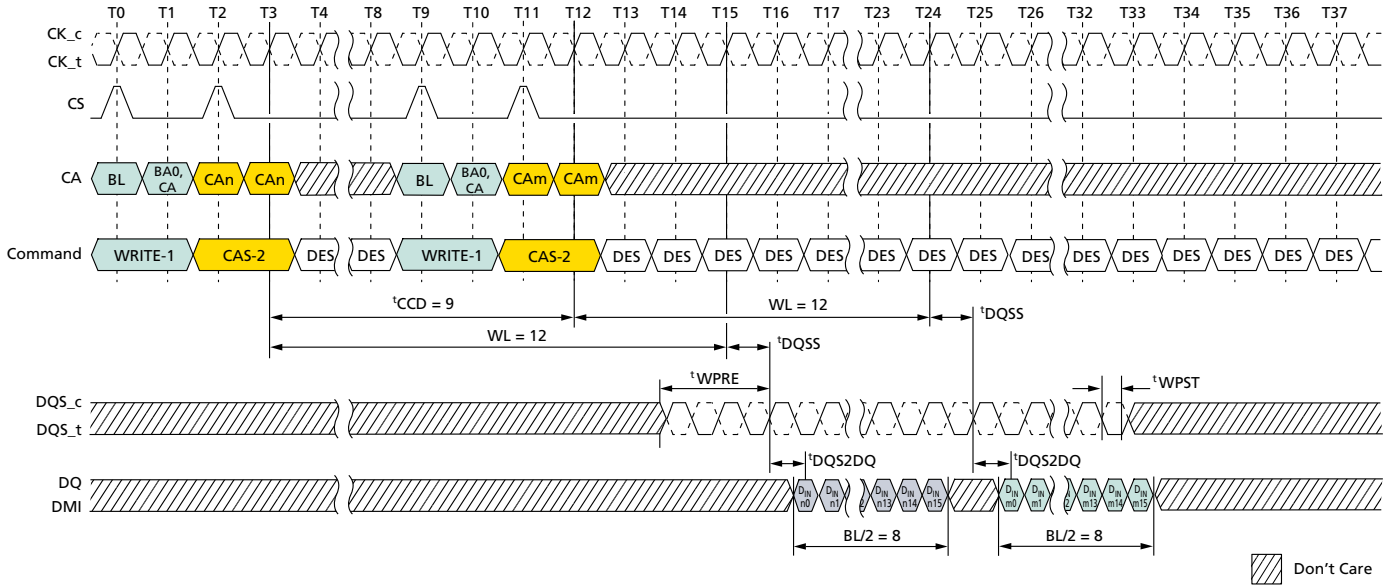


- Notes:
1. $BL = 16$, Write postamble = $1.5n\text{CK}$.
 2. $D_{IN} n/m$ = data-in from column n and column m .
 3. The minimum number of clock cycles from the burst WRITE command to the burst WRITE command for any bank is $BL/2$.
 4. DES commands are shown for ease of illustration; other commands may be valid at these times.



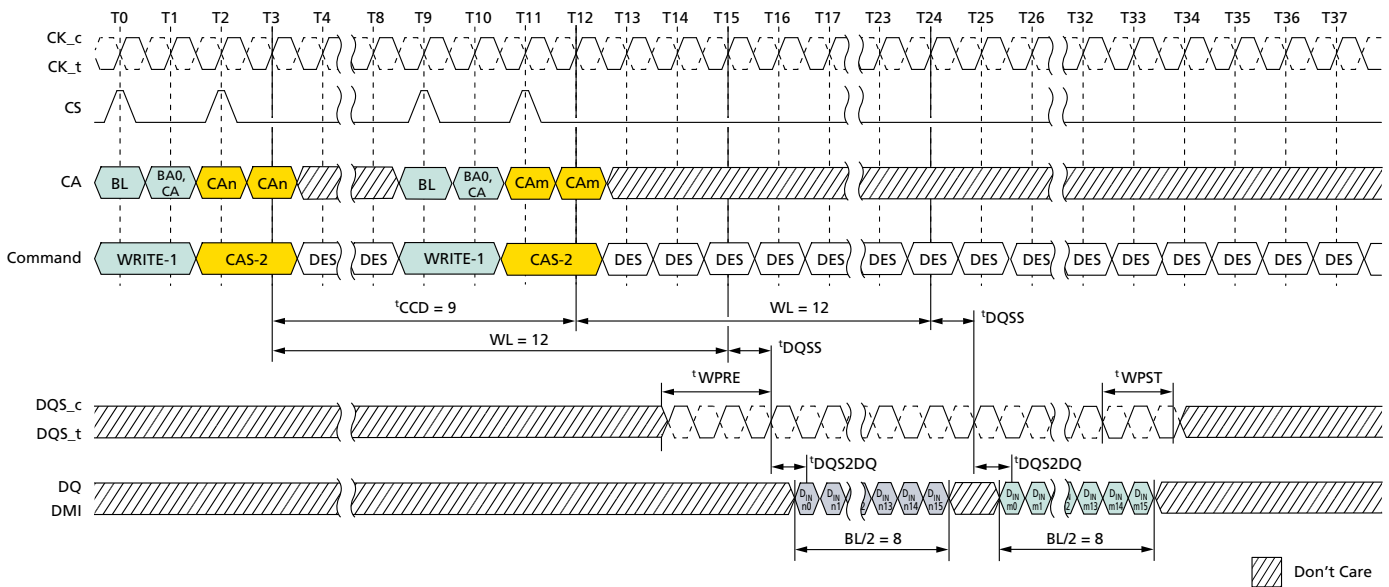
WRITE-to-WRITE Operations – Consecutive

Figure 53: Consecutive WRITE: $t_{CCD} = \text{MIN} + 1, 0.5n\text{CK}$ Postamble



- Notes:
1. BL = 16, Write postamble = $0.5n\text{CK}$.
 2. $D_{IN} n/m$ = data-in from column n and column m .
 3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 54: Consecutive WRITE: $t_{CCD} = \text{MIN} + 1, 1.5n\text{CK}$ Postamble



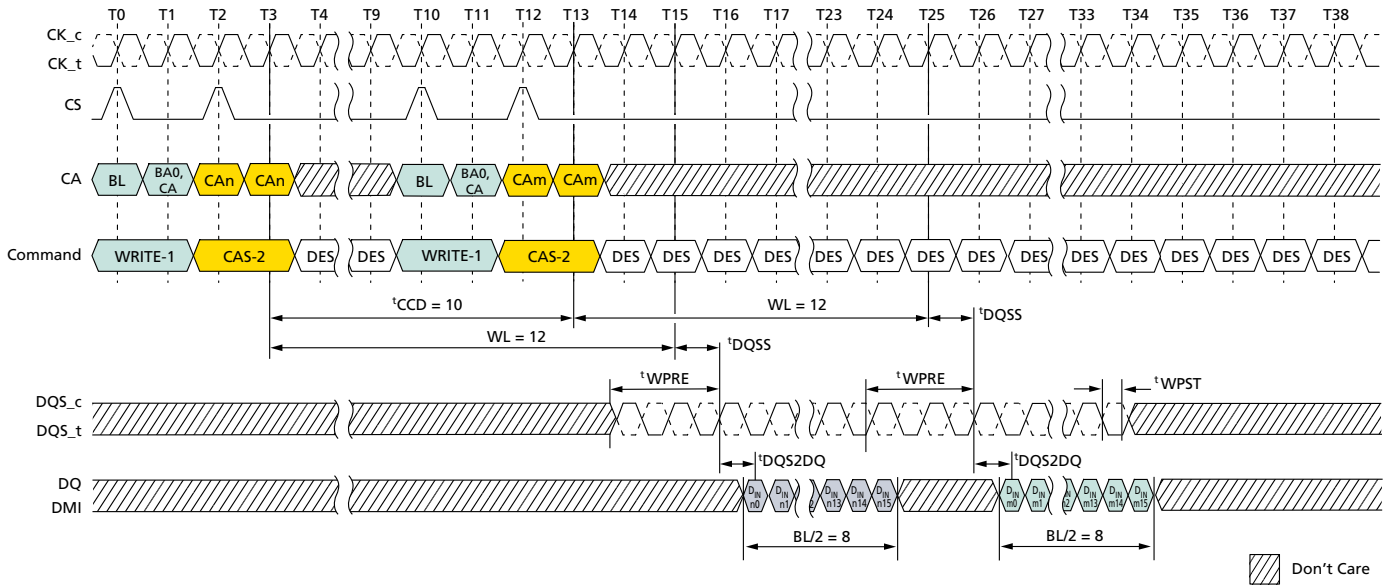
- Notes:
1. BL = 16, Write postamble = $1.5n\text{CK}$.
 2. $D_{IN} n/m$ = data-in from column n and column m .



**200b: x32 LPDDR4 SDRAM
Preamble and Postamble Behavior**

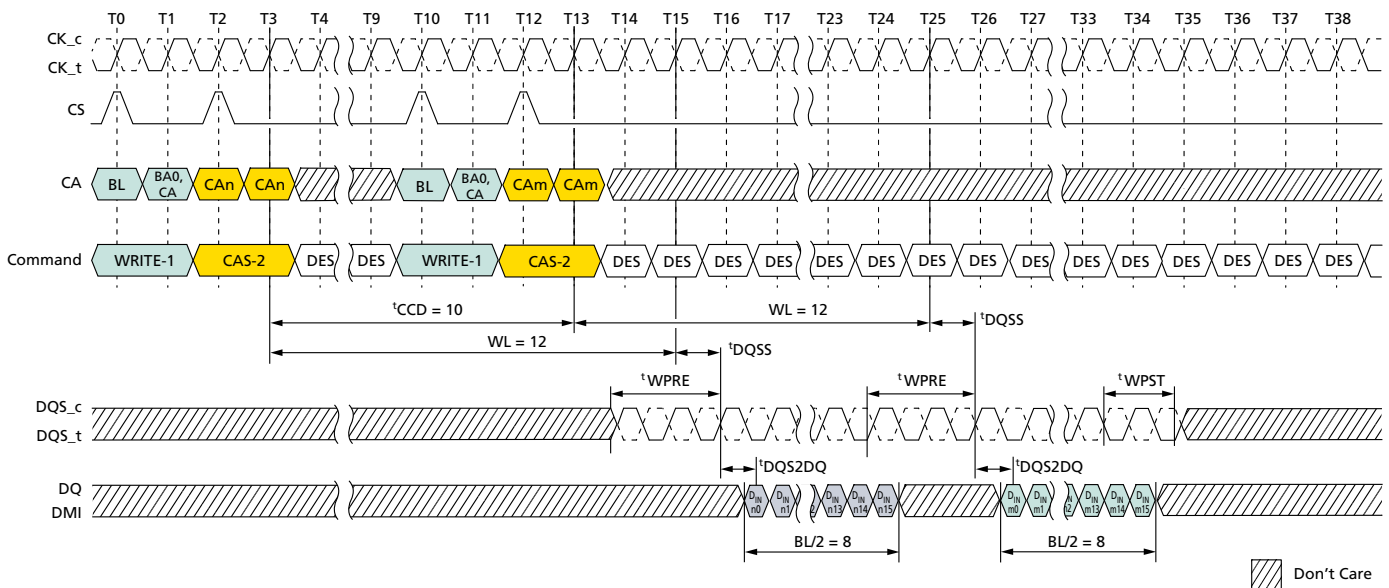
- DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 55: Consecutive WRITE: $t_{CCD} = MIN + 2, 0.5nCK$ Postamble



- Notes:
- BL = 16, Write postamble = $0.5nCK$.
 - $D_{IN} n/m$ = data-in from column n and column m .
 - DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 56: Consecutive WRITE: $t_{CCD} = MIN + 2, 1.5nCK$ Postamble



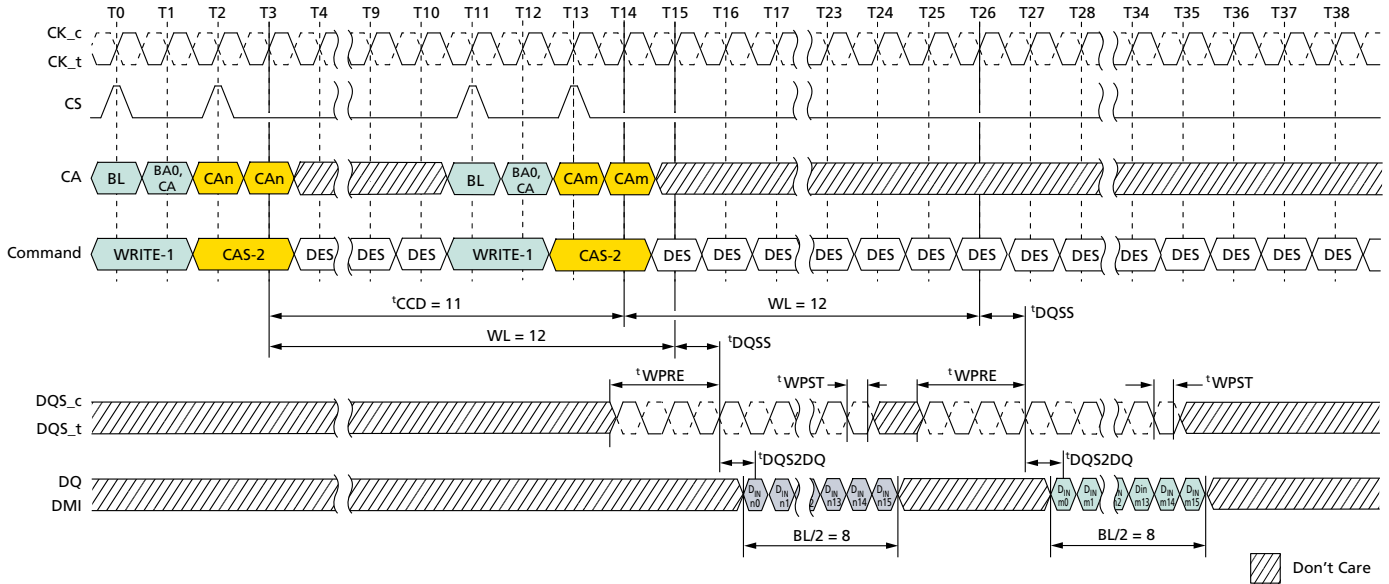
- Notes:
- BL = 16, Write postamble = $1.5nCK$.



**200b: x32 LPDDR4 SDRAM
Preamble and Postamble Behavior**

2. $D_{IN\ n/m}$ = data-in from column n and column m .
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 57: Consecutive WRITE: $t_{CCD} = MIN + 3, 0.5nCK$ Postamble

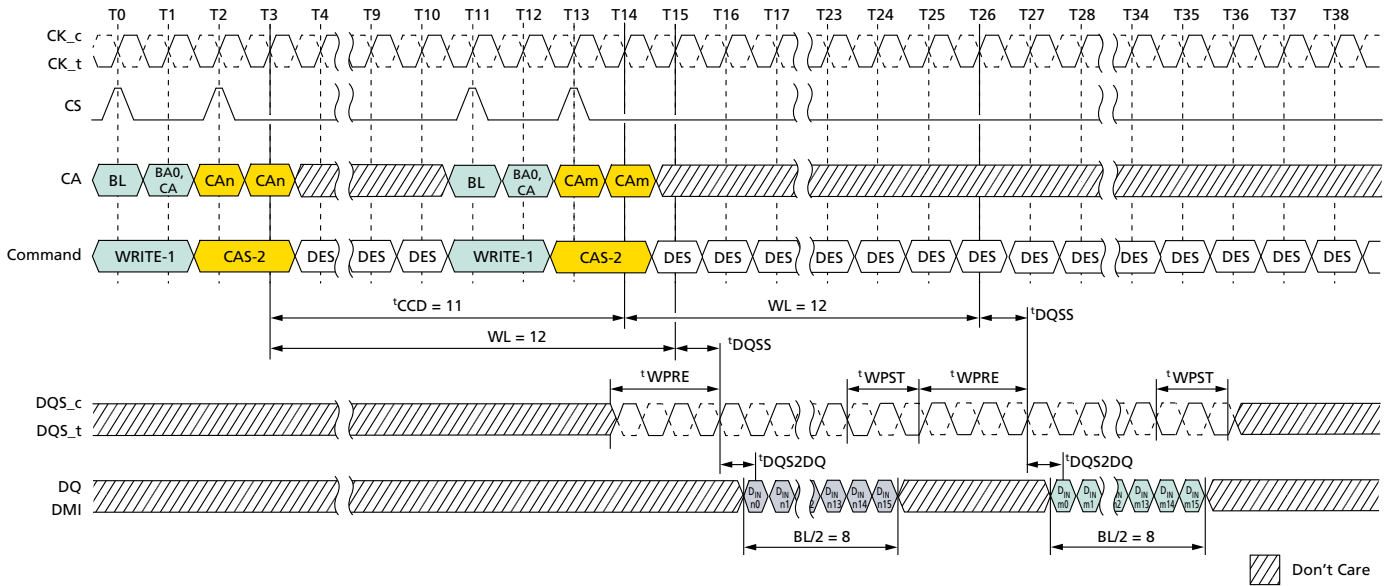


- Notes:
1. $BL = 16$, Write postamble = $0.5nCK$.
 2. $D_{IN\ n/m}$ = data-in from column n and column m .
 3. DES commands are shown for ease of illustration; other commands may be valid at these times.



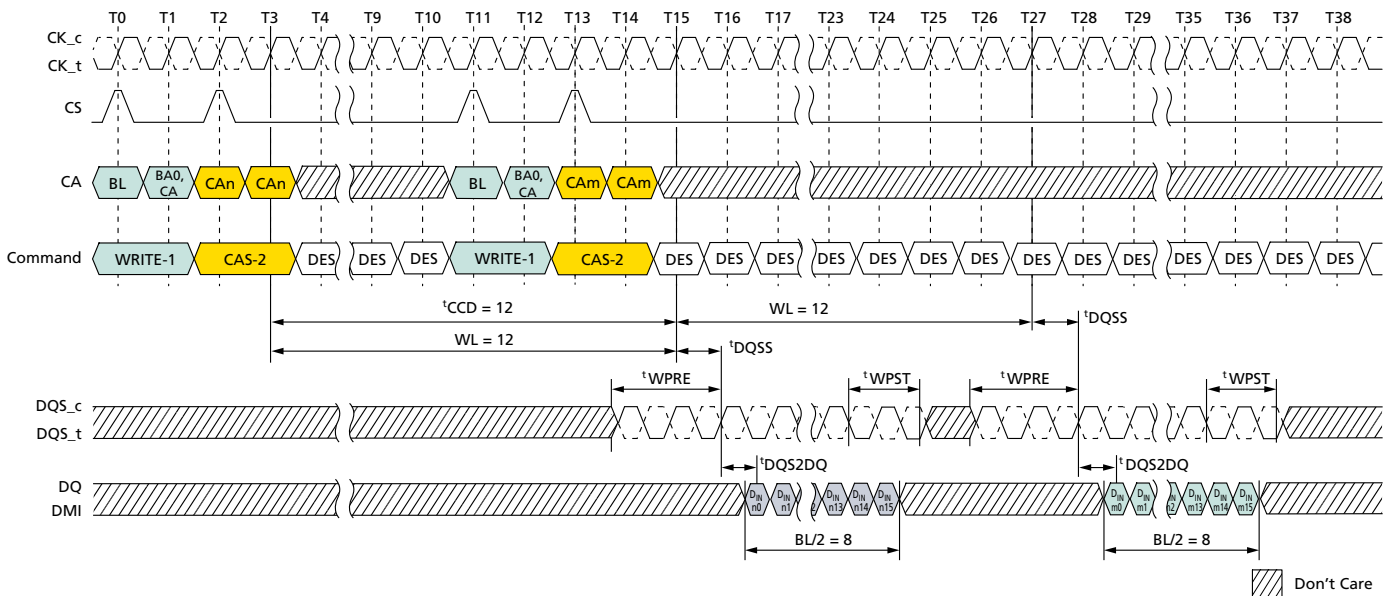
200b: x32 LPDDR4 SDRAM
Preamble and Postamble Behavior

Figure 58: Consecutive WRITE: $t_{CCD} = \text{MIN} + 3, 1.5n\text{CK}$ Postamble



- Notes:
1. BL = 16, Write postamble = $1.5n\text{CK}$.
 2. $D_{IN} n/m$ = data-in from column n and column m .
 3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 59: Consecutive WRITE: $t_{CCD} = \text{MIN} + 4, 1.5n\text{CK}$ Postamble



- Notes:
1. BL = 16, Write postamble = $1.5n\text{CK}$.
 2. $D_{IN} n/m$ = data-in from column n and column m .
 3. DES commands are shown for ease of illustration; other commands may be valid at these times.



PRECHARGE Operation

The PRECHARGE command is used to precharge or close a bank that has been activated. The PRECHARGE command is initiated with CKE, CS, and CA[5:0] in the proper state (see Command Truth Table). The PRECHARGE command can be used to precharge each bank independently or all banks simultaneously. The all banks (AB) flag and the bank address bit are used to determine which bank(s) to precharge. The precharged bank(s) will be available for subsequent row access t_{RPab} after an all-bank PRECHARGE command is issued, or t_{RPpb} after a single-bank PRECHARGE command is issued.

To ensure that the device can meet the instantaneous current demands, the row precharge time for an all-bank PRECHARGE (t_{RPab}) is longer than the per-bank precharge time (t_{RPpb}).

Table 94: Precharge Bank Selection

| AB (CA[5], R1) | BA2 (CA[2], R2) | BA1 (CA[1], R2) | BA0 (CA[0], R2) | Precharged Bank |
|----------------|-----------------|-----------------|-----------------|-----------------|
| 0 | 0 | 0 | 0 | Bank 0 only |
| 0 | 0 | 0 | 1 | Bank 1 only |
| 0 | 0 | 1 | 0 | Bank 2 only |
| 0 | 0 | 1 | 1 | Bank 3 only |
| 0 | 1 | 0 | 0 | Bank 4 only |
| 0 | 1 | 0 | 1 | Bank 5 only |
| 0 | 1 | 1 | 0 | Bank 6 only |
| 0 | 1 | 1 | 1 | Bank 7 only |
| 1 | Don't Care | Don't Care | Don't Care | All banks |

Burst READ Operation Followed by Precharge

The PRECHARGE command can be issued as early as BL/2 clock cycles after a READ command, but the PRECHARGE command cannot be issued until after t_{RAS} is satisfied. A new bank ACTIVATE command can be issued to the same bank after the row precharge time (t_{RP}) has elapsed. The minimum read-to-precharge time must also satisfy a minimum analog time from the second rising clock edge of the CAS-2 command. t_{RTP} begins BL/2 - 8 clock cycles after the READ command.



Figure 60: Burst READ Followed by Precharge – BL16, Toggling Preamble, 0.5nCK Postamble

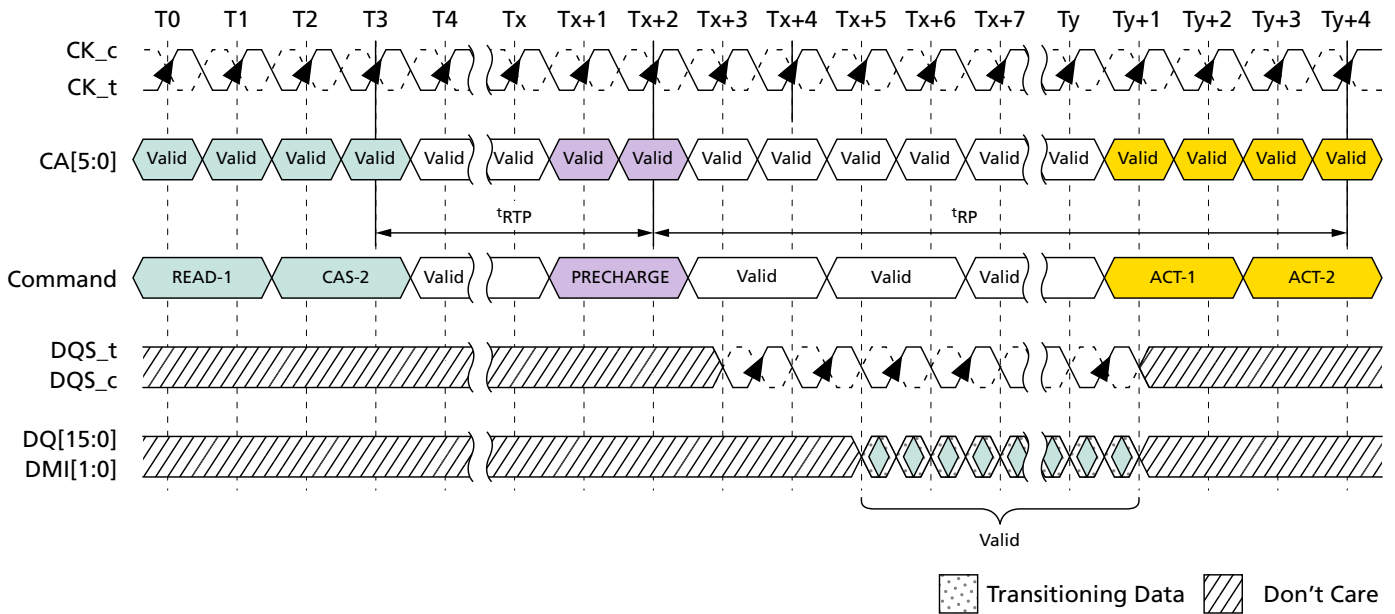
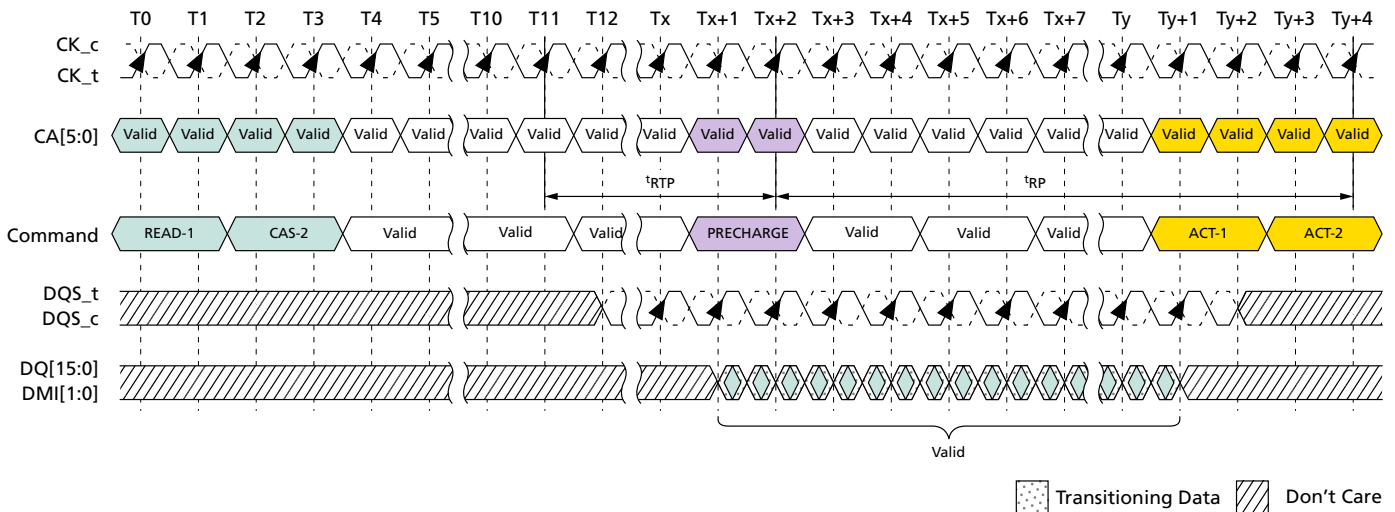


Figure 61: Burst READ Followed by Precharge – BL32, 2^tCK, 0.5nCK Postamble



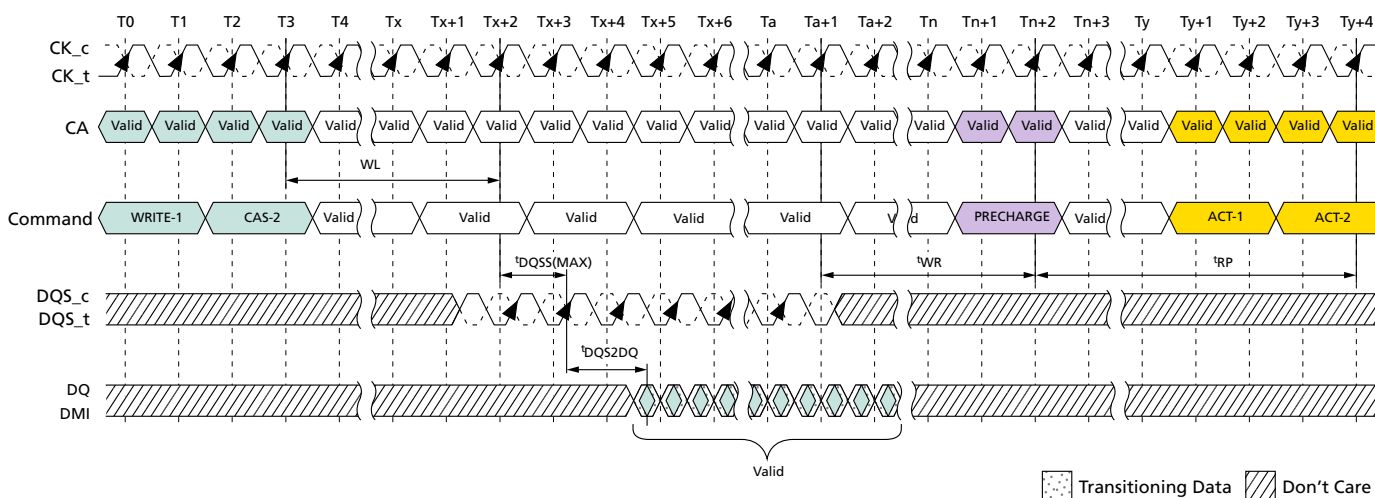
Burst WRITE Followed by Precharge

A write recovery time (t^w_{WR}) must be provided before a PRECHARGE command may be issued. This delay is referenced from the next rising edge of CK after the last valid DQS clock of the burst.

Devices write data to the memory array in prefetch multiples (prefetch = 16). An internal WRITE operation can only begin after a prefetch group has been clocked; therefore, t^w_{WR} starts at the prefetch boundaries. The minimum write-to-precharge time for commands to the same bank is $WL + BL/2 + 1 + RU(t^w_{WR} / ^tCK)$ clock cycles.



Figure 62: Burst WRITE Followed by PRECHARGE – BL16, 2nCK Preamble, 0.5nCK Postamble



Auto Precharge

Before a new row can be opened in an active bank, the active bank must be precharged using either the PRECHARGE command or the auto precharge (AP) function. When a READ or a WRITE command is issued to the device, the AP bit (CA5) can be set to enable the active bank to automatically begin precharge at the earliest possible moment during the burst READ or WRITE cycle.

If AP is LOW when the READ or WRITE command is issued, the normal READ or WRITE burst operation is executed, and the bank remains active at the completion of the burst.

If AP is HIGH when the READ or WRITE command is issued, the auto PRECHARGE function is engaged. This feature enables the PRECHARGE operation to be partially or completely hidden during burst READ cycles (dependent upon READ or WRITE latency), thus improving system performance for random data access.

Burst READ With Auto Precharge

If AP is HIGH when a READ command is issued, the READ with AUTO PRECHARGE function is engaged. The devices start an AUTO PRECHARGE operation on the rising edge of the clock at BL/2 after the second beat of the READ w/AP command, or BL/4 - 4 + RU(^tRTP/^tCK) clock cycles after the second beat of the READ w/AP command, whichever is greater. Following an AUTO PRECHARGE operation, an ACTIVATE command can be issued to the same bank if the following two conditions are both satisfied:

1. The RAS precharge time (^tRP) has been satisfied from the clock at which the auto precharge began, and
2. The RAS cycle time (^tRC) from the previous bank activation has been satisfied.



Figure 63: Burst READ With Auto Precharge – BL16, Non-Toggling Preamble, 0.5nCK Postamble

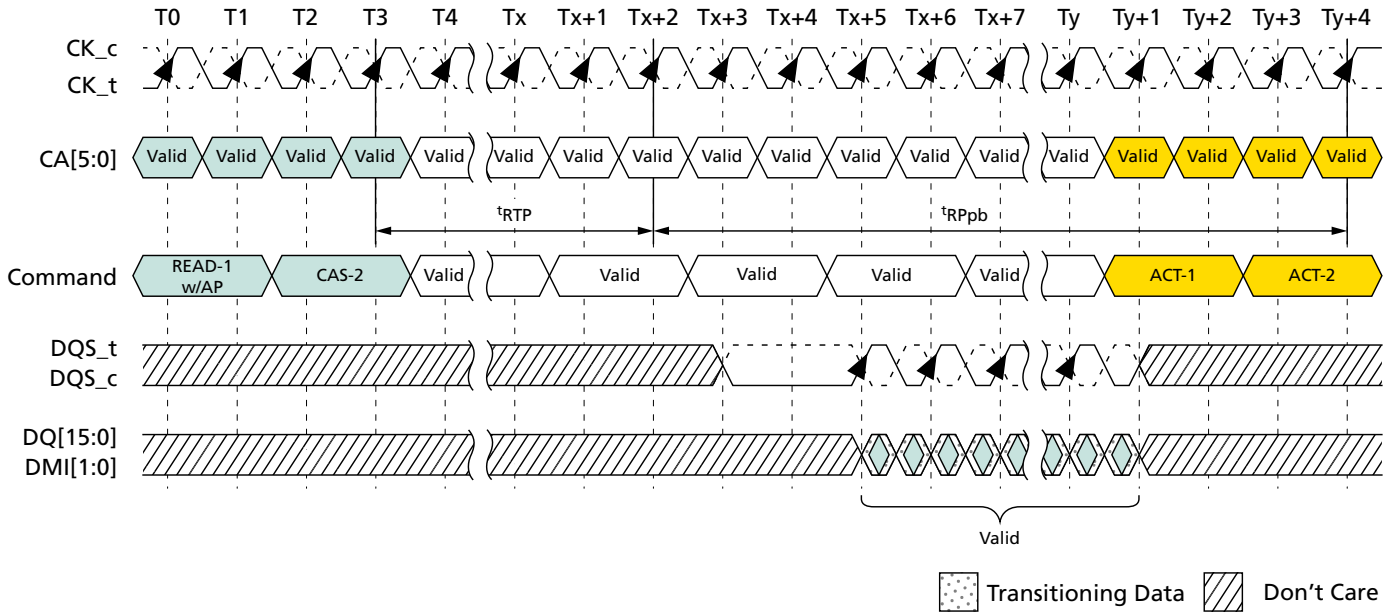
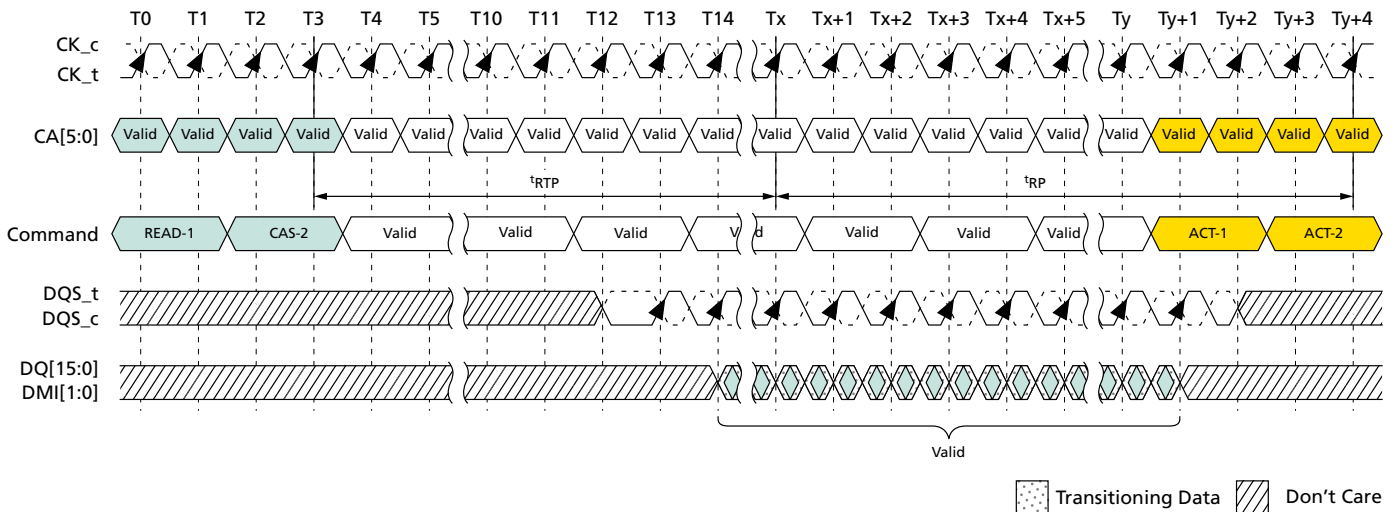


Figure 64: Burst READ With Auto Precharge – BL32, Toggling Preamble, 1.5nCK Postamble



Burst WRITE With Auto Precharge

If AP is HIGH when a WRITE command is issued, the WRITE with AUTO PRECHARGE function is engaged. The device starts an auto precharge on the rising edge t_{WR} cycles after the completion of the burst WRITE.

Following a WRITE with AUTO PRECHARGE, an ACTIVATE command can be issued to the same bank if the following conditions are met:

1. The RAS precharge time (t_{RP}) has been satisfied from the clock at which the auto precharge began, and



2. The RAS cycle time (t_{RC}) from the previous bank activation has been satisfied.

Figure 65: Burst WRITE With Auto Precharge – BL16, 2nCK Preamble, 0.5nCK Postamble

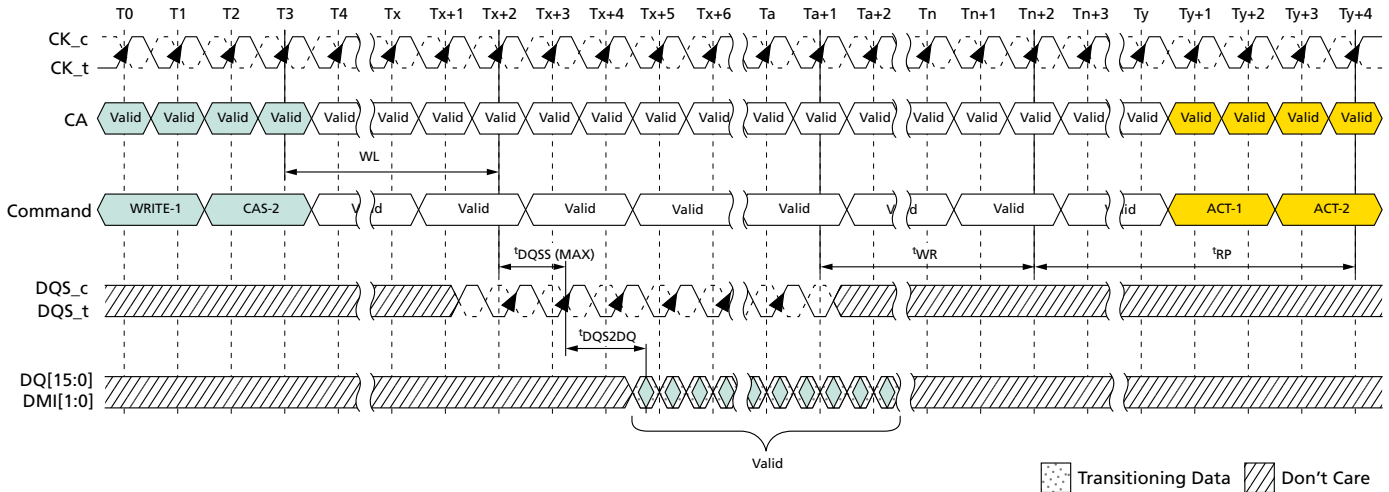


Table 95: Timing Between Commands (PRECHARGE and AUTO PRECHARGE): DQ ODT is Disable

| From Command | To Command | Minimum Delay Between "From Command" and "To Command" | Unit | Notes |
|----------------------|---|--|----------|----------|
| READ BL = 16 | PRECHARGE (to same bank as READ) | t_{RTP} | t_{CK} | 1, 6 |
| | PRECHARGE ALL | t_{RTP} | t_{CK} | 1, 6 |
| READ BL = 32 | PRECHARGE (to same bank as READ) | $8t_{CK} + t_{RTP}$ | t_{CK} | 1, 6 |
| | PRECHARGE ALL | $8t_{CK} + t_{RTP}$ | t_{CK} | 1, 6 |
| READ w/AP BL = 16 | PRECHARGE (to same bank as READ w/AP) | $nRTP$ | t_{CK} | 1, 10 |
| | PRECHARGE ALL | $nRTP$ | t_{CK} | 1, 10 |
| | ACTIVATE (to same bank as READ w/AP) | $nRTP + t_{RPpb}$ | t_{CK} | 1, 8, 10 |
| | WRITE or WRITE w/AP (same bank) | Illegal | - | |
| | MASK-WR or MASK-WR w/AP (same bank) | Illegal | - | |
| | WRITE or WRITE w/AP (different bank) | $RL + RU(t_{DQSCK(MAX)}/t_{CK}) + BL/2 + RD(t_{RPST}) - WL + t_{WPRE}$ | t_{CK} | 3, 4, 5 |
| | MASK-WR or MASK-WR w/AP (different bank) | $RL + RU(t_{DQSCK(MAX)}/t_{CK}) + BL/2 + RD(t_{RPST}) - WL + t_{WPRE}$ | t_{CK} | 3, 4, 5 |
| | READ or READ w/AP (same bank) | Illegal | - | |
| | READ or READ w/AP (different bank) | $BL/2$ | t_{CK} | 3 |


Table 95: Timing Between Commands (PRECHARGE and AUTO PRECHARGE): DQ ODT is Disable (Continued)

| From Command | To Command | Minimum Delay Between "From Command" and "To Command" | Unit | Notes |
|------------------------------|---|--|---------------|----------|
| READ w/AP BL = 32 | PRECHARGE (to same bank as READ w/AP) | $8^t\text{CK} + n\text{RTP}$ | ^tCK | 1, 10 |
| | PRECHARGE ALL | $8^t\text{CK} + n\text{RTP}$ | ^tCK | 1, 10 |
| | ACTIVATE (to same bank as READ w/AP) | $8^t\text{CK} + n\text{RTP} + ^t\text{RPpb}$ | ^tCK | 1, 8, 10 |
| | WRITE or WRITE w/AP (same bank) | Illegal | – | |
| | MASK-WR or MASK-WR w/AP (same bank) | Illegal | – | |
| | WRITE or WRITE w/AP (different bank) | $\text{RL} + \text{RU}(^t\text{DQSCk}(\text{MAX})/^t\text{CK}) + \text{BL}/2 + \text{RD}(^t\text{RPST}) - \text{WL} + ^t\text{WPRE}$ | ^tCK | 3, 4, 5 |
| | MASK-WR or MASK-WR w/AP (different bank) | $\text{RL} + \text{RU}(^t\text{DQSCk}(\text{MAX})/^t\text{CK}) + \text{BL}/2 + \text{RD}(^t\text{RPST}) - \text{WL} + ^t\text{WPRE}$ | ^tCK | 3, 4, 5 |
| | READ or READ w/AP (same bank) | Illegal | – | |
| | READ or READ w/AP (different bank) | BL/2 | ^tCK | 3 |
| WRITE BL = 16 and 32 | PRECHARGE (to same bank as WRITE) | $\text{WL} + \text{BL}/2 + ^t\text{WR} + 1$ | ^tCK | 1, 7 |
| | PRECHARGE ALL | $\text{WL} + \text{BL}/2 + ^t\text{WR} + 1$ | ^tCK | 1, 7 |
| MASK-WR BL = 16 | PRECHARGE (to same bank as MASK-WR) | $\text{WL} + \text{BL}/2 + ^t\text{WR} + 1$ | ^tCK | 1, 7 |
| | PRECHARGE ALL | $\text{WL} + \text{BL}/2 + ^t\text{WR} + 1$ | ^tCK | 1, 7 |
| WRITE w/AP BL = 16 and 32 | PRECHARGE (to same bank as WRITE w/AP) | $\text{WL} + \text{BL}/2 + n\text{WR} + 1$ | ^tCK | 1, 11 |
| | PRECHARGE ALL | $\text{WL} + \text{BL}/2 + n\text{WR} + 1$ | ^tCK | 1, 11 |
| | ACTIVATE (to same bank as WRITE w/AP) | $\text{WL} + \text{BL}/2 + n\text{WR} + 1 + ^t\text{RPpb}$ | ^tCK | 1, 8, 11 |
| | WRITE or WRITE w/AP (same bank) | Illegal | – | |
| | READ or READ w/AP (same bank) | Illegal | – | |
| | WRITE or WRITE w/AP (different bank) | BL/2 | ^tCK | 3 |
| | MASK-WR or MASK-WR w/AP (different bank) | BL/2 | ^tCK | 3 |
| | READ or READ w/AP (different bank) | $\text{WL} + \text{BL}/2 + ^t\text{WTR} + 1$ | ^tCK | 3, 9 |


Table 95: Timing Between Commands (PRECHARGE and AUTO PRECHARGE): DQ ODT is Disable (Continued)

| From Command | To Command | Minimum Delay Between "From Command" and "To Command" | Unit | Notes |
|-------------------------|---|---|----------|----------|
| MASK-WR w/AP BL = 16 | PRECHARGE (to same bank as MASK-WR w/AP) | $WL + BL/2 + nWR + 1$ | t_{CK} | 1, 11 |
| | PRECHARGE ALL | $WL + BL/2 + nWR + 1$ | t_{CK} | 1, 11 |
| | ACTIVATE (to same bank as MASK-WR w/AP) | $WL + BL/2 + nWR + 1 + t_{RPpb}$ | t_{CK} | 1, 8, 11 |
| | WRITE or WRITE w/AP (same bank) | Illegal | – | 3 |
| | MASK-WR or MASK-WR w/AP (same bank) | Illegal | – | 3 |
| | WRITE or WRITE w/AP (different bank) | BL/2 | t_{CK} | 3 |
| | MASK-WR or MASK-WR w/AP (different bank) | BL/2 | t_{CK} | 3 |
| | READ or READ w/AP (same bank) | Illegal | – | 3 |
| | READ or READ w/AP (different bank) | $WL + BL/2 + t_{WTR} + 1$ | t_{CK} | 3, 9 |
| PRECHARGE | PRECHARGE (to same bank as PRECHARGE) | 4 | t_{CK} | 1 |
| | PRECHARGE ALL | 4 | t_{CK} | 1 |
| PRECHARGE ALL | PRECHARGE | 4 | t_{CK} | 1 |
| | PRECHARGE ALL | 4 | t_{CK} | 1 |

- Notes:
- For a given bank, the precharge period should be counted from the latest PRECHARGE command, whether per-bank or all-bank, issued to that bank. The precharge period is satisfied t_{RP} after that latest PRECHARGE command.
 - Any command issued during the minimum delay time as specified in the table above is illegal.
 - After READ w/AP, seamless READ operations to different banks are supported. After WRITE w/AP or MASK-WR w/AP, seamless WRITE operations to different banks are supported. READ, WRITE, and MASK-WR operations may not be truncated or interrupted.
 - t_{RPST} values depend on MR1 OP[7] respectively.
 - t_{WPRE} values depend on MR1 OP[2] respectively.
 - Minimum delay between "from command" and "to command" in clock cycle is calculated by dividing t_{RTP} (in ns) by t_{CK} (in ns) and rounding up to the next integer: Minimum delay [cycles] = $\text{roundup}(t_{RTP} [\text{ns}] / t_{CK} [\text{ns}])$.
 - Minimum delay between "from command" and "to command" in clock cycle is calculated by dividing t_{WR} (in ns) by t_{CK} (in ns) and rounding up to the next integer: Minimum delay [cycles] = $\text{roundup}(t_{WR} [\text{ns}] / t_{CK} [\text{ns}])$.



8. Minimum delay between "from command" and "to command" in clock cycle is calculated by dividing t_{RPpb} (in ns) by t_{CK} (in ns) and rounding up to the next integer: Minimum delay [cycles] = $\text{roundup}(t_{RPpb} [\text{ns}] / t_{CK} [\text{ns}])$.
9. Minimum delay between "from command" and "to command" in clock cycle is calculated by dividing t_{WTR} (in ns) by t_{CK} (in ns) and rounding up to the next integer: Minimum delay [cycles] = $\text{roundup}(t_{WTR} [\text{ns}] / t_{CK} [\text{ns}])$.
10. For READ w/AP the value is $nRTP$, which is defined in mode register 2.
11. For WRITE w/AP the value is nWR , which is defined in mode register 1.

Table 96: Timing Between Commands (PRECHARGE and AUTO PRECHARGE): DQ ODT is Enable

| From Command | To Command | Minimum Delay Between "From Command" and "To Command" | Unit | Notes |
|----------------------|--|--|----------|-------|
| READ w/AP BL = 16 | WRITE or WRITE w/AP (different bank) | $RL + RU(t_{DQSCK}(\text{MAX})/t_{CK}) + BL/2 + RD(t_{RPST}) - ODT_{Lon} - RD(t_{ODTon}(\text{MIN})/t_{CK}) + 1$ | t_{CK} | 2, 3 |
| | MASK-WR or MASK-WR w/AP (different bank) | $RL + RU(t_{DQSCK}(\text{MAX})/t_{CK}) + BL/2 + RD(t_{RPST}) - ODT_{Lon} - RD(t_{ODTon}(\text{MIN})/t_{CK}) + 1$ | t_{CK} | 2, 3 |
| READ w/AP BL = 32 | WRITE or WRITE w/AP (different bank) | $RL + RU(t_{DQSCK}(\text{MAX})/t_{CK}) + BL/2 + RD(t_{RPST}) - ODT_{Lon} - RD(t_{ODTon}(\text{MIN})/t_{CK}) + 1$ | t_{CK} | 2, 3 |
| | MASK-WR or MASK-WR w/AP (different bank) | $RL + RU(t_{DQSCK}(\text{MAX})/t_{CK}) + BL/2 + RD(t_{RPST}) - ODT_{Lon} - RD(t_{ODTon}(\text{MIN})/t_{CK}) + 1$ | t_{CK} | 2, 3 |

- Notes:
1. The rest of the timing about PRECHARGE and AUTO PRECHARGE is same as DQ ODT is disable case.
 2. After READ w/AP, seamless read operations to different banks are supported. READ, WRITE, and MASK-WR operations may not be truncated or interrupted.
 3. t_{RPST} values depend on MR1 OP[7] respectively.

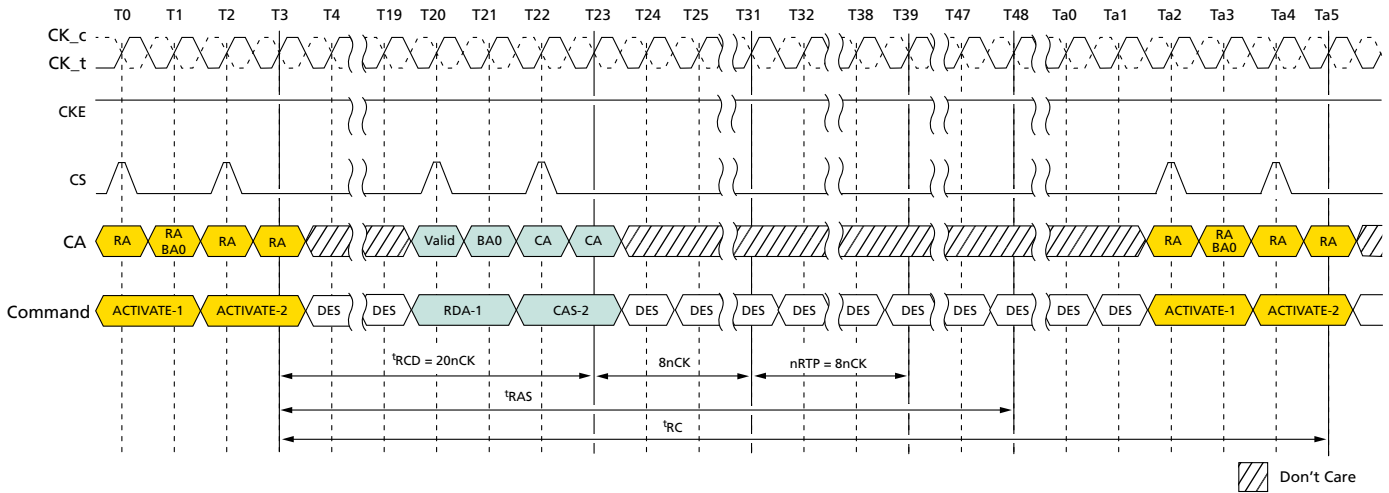
RAS Lock Function

READ with AUTO PRECHARGE or WRITE/MASK WRITE with AUTO PRECHARGE commands may be issued after t_{RCD} has been satisfied. The LPDDR4 SDRAM RAS lockout feature will schedule the internal precharge to assure that t_{RAS} is satisfied. t_{RC} needs to be satisfied prior to issuing subsequent ACTIVATE commands to the same bank.

The figure below shows example of RAS lock function.



Figure 66: Command Input Timing with RAS Lock

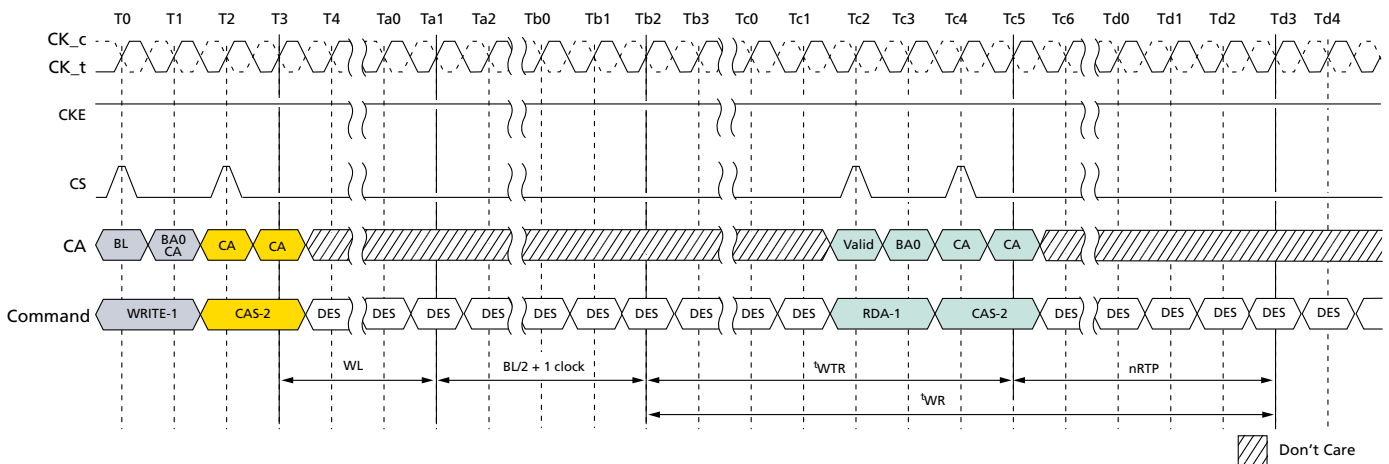


- Notes:
1. $t_{CK} (AVG) = 0.938ns$, Data rate = 2133 Mbps, $t_{RCD}(MIN) = MAX(18ns, 4nCK)$, $t_{RAS}(MIN) = MAX(42ns, 3nCK)$, $nRTP = 8nCK$, $BL = 32$.
 2. $t_{RCD} = 20nCK$ comes from $roundup(18ns/0.938ns)$.
 3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Delay Time From WRITE-to-READ with Auto Precharge

In the case of WRITE command followed by READ with AUTO PRECHARGE, controller must satisfy t_{WR} for the WRITE command before initiating the device internal auto-precharge. It means that $(t_{WTR} + nRTP)$ should be equal or longer than (t_{WR}) when BL setting is 16, as well as $(t_{WTR} + nRTP + 8nCK)$ should be equal or longer than (t_{WR}) when BL setting is 32. Refer to the following figure for details.

Figure 67: Delay Time From WRITE-to-READ with Auto Precharge



- Notes:
1. Burst length at read = 16.



2. DES commands are shown for ease of illustration; other commands may be valid at these times.

REFRESH Command

The REFRESH command is initiated with CS HIGH, CA0 LOW, CA1 LOW, CA2 LOW, CA3 HIGH and CA4 LOW at the first rising edge of clock. Per bank REFRESH is initiated with CA5 LOW at the first rising edge of the clock. The all-bank REFRESH is initiated with CA5 HIGH at the first rising edge of clock.

A per bank REFRESH command (REFpb) is performed to the bank address as transferred on CA0, CA1, and CA2 on the second rising edge of the clock. Bank address BA0 is transferred on CA0, bank address BA1 is transferred on CA1, and bank address BA2 is transferred on CA2. A per bank REFRESH command (REFpb) to the eight banks can be issued in any order. For example, REFpb commands may be issued in the following order: 1-3-0-2-4-7-5-6. After the eight banks have been refreshed using the per bank REFRESH command, the controller can send another set of per bank REFRESH commands in the same order or a different order. One possible order can be a sequential round robin: 0-1-2-3-4-5-6-7. It is illegal to send a per bank REFRESH command to the same bank unless all eight banks have been refreshed using the per bank REFRESH command. The count of eight REFpb commands starts with the first REFpb command after a synchronization event.

The bank count is synchronized between the controller and the device by resetting the bank count to zero. Synchronization can occur upon reset procedure or at every exit from self refresh. The REFab command also synchronizes the counter between the controller and the device to zero. The device can be placed in self refresh, or a REFab command can be issued at any time without cycling through all eight banks using per bank REFRESH command. After the bank count is synchronized to zero, the controller can issue per bank REFRESH commands in any order, as described above.

A REFab command issued when the bank counter is not zero will reset the bank counter to zero and the device will perform refreshes to all banks as indicated by the row counter. If another REFRESH command (REFab or REFpb) is issued after the REFab command then it uses an incremented value of the row counter.

The table below shows examples of both bank and refresh counter increment behavior.

Table 97: Bank and Refresh Counter Increment Behavior

| # | Command | BA2 | BA1 | BA0 | Refresh Bank # | Bank Counter # | Ref. Conter # (Row Address #) |
|---|----------------------|-----|-----|-----|----------------|----------------|-------------------------------|
| 0 | Reset, SRX, or REFab | | | | | To 0 | – |
| 1 | REFpb | 0 | 0 | 0 | 0 | 0 to 1 | n |
| 2 | REFpb | 0 | 0 | 1 | 1 | 1 to 2 | |
| 3 | REFpb | 0 | 1 | 0 | 2 | 2 to 3 | |
| 4 | REFpb | 0 | 1 | 1 | 3 | 3 to 4 | |
| 5 | REFpb | 1 | 0 | 0 | 4 | 4 to 5 | |
| 6 | REFpb | 1 | 0 | 1 | 5 | 5 to 6 | |
| 7 | REFpb | 1 | 1 | 0 | 6 | 6 to 7 | |
| 8 | REFpb | 1 | 1 | 1 | 7 | 7 to 0 | |


Table 97: Bank and Refresh Counter Increment Behavior (Continued)

| # | Command | BA2 | BA1 | BA0 | Refresh Bank # | Bank Counter # | Ref. Conter # (Row Address #) | |
|-----------|--------------|----------|----------|----------|----------------|----------------|-------------------------------|-------|
| 9 | REFpb | 1 | 1 | 0 | 6 | 0 to 1 | n + 1 | |
| 10 | REFpb | 1 | 1 | 1 | 7 | 1 to 2 | | |
| 11 | REFpb | 0 | 0 | 1 | 1 | 2 to 3 | | |
| 12 | REFpb | 0 | 1 | 1 | 3 | 3 to 4 | | |
| 13 | REFpb | 1 | 0 | 1 | 5 | 4 to 5 | | |
| 14 | REFpb | 0 | 1 | 0 | 2 | 5 to 6 | | |
| 15 | REFpb | 0 | 0 | 0 | 0 | 6 to 7 | | |
| 16 | REFpb | 1 | 0 | 0 | 4 | 7 to 0 | | |
| 17 | REFpb | 0 | 0 | 0 | 0 | 0 to 1 | | n + 2 |
| 18 | REFpb | 0 | 0 | 1 | 1 | 1 to 2 | | |
| 19 | REFpb | 0 | 1 | 0 | 2 | 2 to 3 | | |
| 20 | REFab | V | V | V | 0 to 7 | To 0 | n + 2 | |
| 21 | REFpb | 1 | 1 | 0 | 6 | 0 to 1 | n + 3 | |
| 22 | REFpb | 1 | 1 | 1 | 7 | 1 to 2 | | |
| Snip | | | | | | | | |

A bank must be idle before it can be refreshed. The controller must track the bank being refreshed by the per bank REFRESH command.

The REFpb command must not be issued to the device until the following conditions have been met:

- t_{RFCab} has been satisfied after the prior REFab command
- t_{RFCpb} has been satisfied after the prior REFpb command
- t_{RP} has been satisfied after the prior PRECHARGE command to that bank
- t_{RRD} has been satisfied after the prior ACTIVATE command (for example, after activating a row in a different bank than the one affected by the REFpb command)

The target bank is inaccessible during per bank REFRESH cycle time (t_{RFCpb}). However, other banks within the device are accessible and can be addressed during the cycle. During the REFpb operation, any of the banks other than the one being refreshed can be maintained in an active state or accessed by a READ or a WRITE command. When the per bank REFRESH cycle has completed, the affected bank will be in the idle state.

After issuing REFpb, the following conditions must be met:

- t_{RFCpb} must be satisfied before issuing a REFab command
- t_{RFCpb} must be satisfied before issuing an ACTIVATE command to the same bank
- t_{RRD} must be satisfied before issuing an ACTIVATE command to a different bank
- t_{RFCpb} must be satisfied before issuing another REFpb command

An all-bank REFRESH command (REFab) issues a REFRESH command to every bank in a channel. All banks must be idle when REFab is issued (for example, by issuing a PRECHARGE ALL command prior to issuing an all-bank REFRESH command). The REFab



command must not be issued to the device until the following conditions have been met:

- t_{RFCab} has been satisfied following the prior REFab command
- t_{RFCpb} has been satisfied following the prior REFpb command
- t_{RP} has been satisfied following the prior PRECHARGE command

When an all-bank REFRESH cycle has completed, all banks will be idle. After issuing REFab:

- RFCab latency must be satisfied before issuing an ACTIVATE command,
- RFCab latency must be satisfied before issuing a REFab or REFpb command

Table 98: REFRESH Command Timing Constraints

| Symbol | Minimum Delay From... | To | Notes |
|-------------|-----------------------|--|-------|
| t_{RFCab} | REFab | REFab | |
| | | ACTIVATE command to any bank | |
| | | REFpb | |
| t_{RFCpb} | REFpb | REFab | |
| | | ACTIVATE command to same bank as REFpb | |
| | | REFpb | |
| t_{RRD} | REFpb | ACTIVATE command to a different bank than REFpb | |
| | ACTIVATE | REFpb | 1 |
| | | ACTIVATE command to a different bank than the prior ACTIVATE command | |

Note: 1. A bank must be in the idle state before it is refreshed; therefore, REFab is prohibited following an ACTIVATE command. REFpb is supported only if it affects a bank that is in the idle state.

Figure 68: All-Bank REFRESH Operation

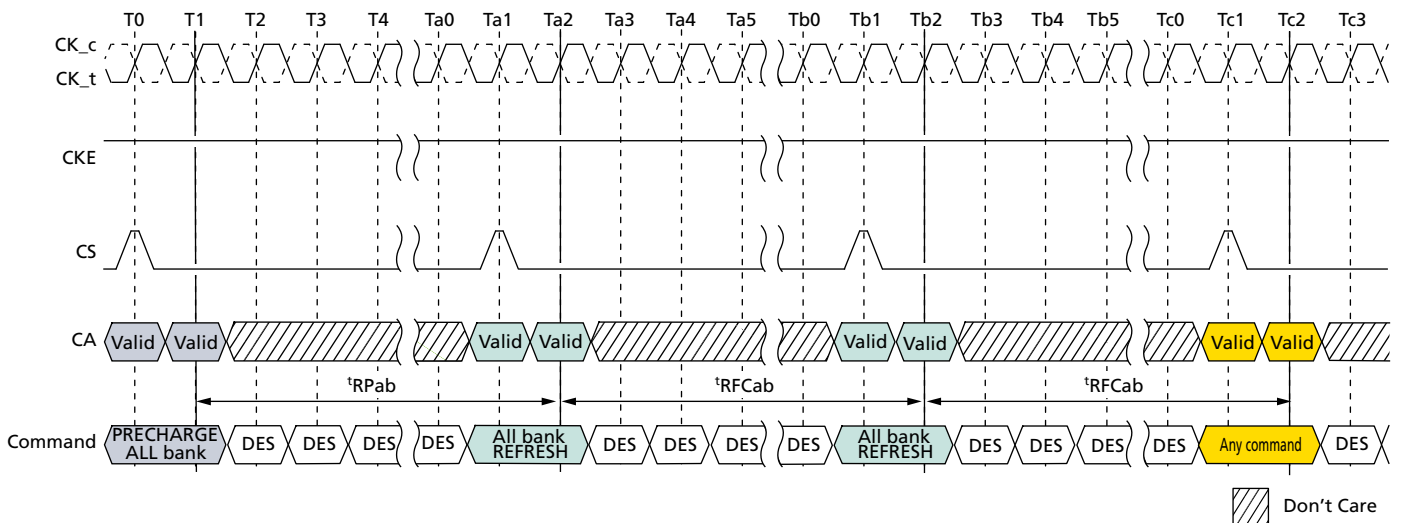
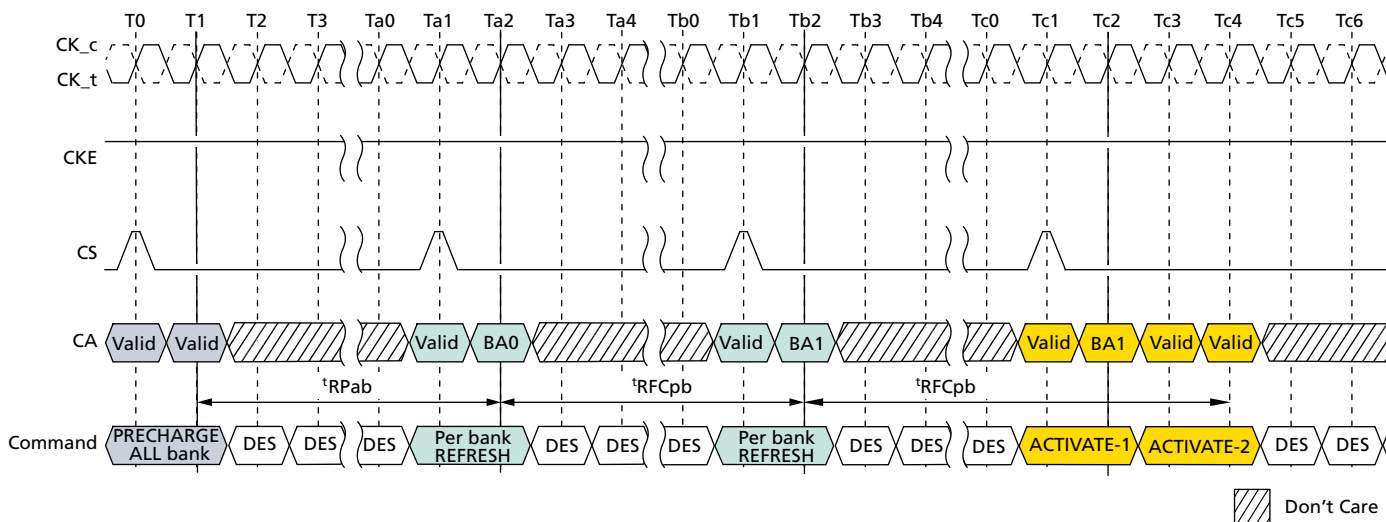




Figure 69: Per Bank REFRESH Operation



- Notes:
1. In the beginning of this example, the REFpb bank is pointing to bank 0.
 2. Operations to banks other than the bank being refreshed are supported during the t_{RFCpb} period.

In general, a REFRESH command needs to be issued to the device regularly every t_{REFI} interval. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight REFRESH commands can be postponed during operation of the device, but at no point in time are more than a total of eight REFRESH commands allowed to be postponed. And a maximum number of pulled-in or postponed REF command is dependent on refresh rate. It is described in the table below. In the case where eight REFRESH commands are postponed in a row, the resulting maximum interval between the surrounding REFRESH commands is limited to $9 \times t_{REFI}$. A maximum of eight additional REFRESH commands can be issued in advance (pulled in), with each one reducing the number of regular REFRESH commands required later by one. Note that pulling in more than eight REFRESH commands in advance does not reduce the number of regular REFRESH commands required later; therefore, the resulting maximum interval between two surrounding REFRESH commands is limited to $9 \times t_{REFI}$. At any given time, a maximum of 16 REFRESH commands can be issued within $2 \times t_{REFI}$.

Self refresh mode may be entered with a maximum of eight REFRESH commands being postponed. After exiting self refresh mode with one or more REFRESH commands postponed, additional REFRESH commands may be postponed to the extent that the total number of postponed REFRESH commands (before and after self refresh) will never exceed eight. During self refresh mode, the number of postponed or pulled-in REFRESH commands does not change.

And for per bank refresh, a maximum of 8 x 8 per bank REFRESH commands can be postponed or pulled in for scheduling efficiency. At any given time, a maximum of 2 x 8 x 8 per bank REFRESH commands can be issued within $2 \times t_{REFI}$.


Table 99: Legacy REFRESH Command Timing Constraints

| MR4 OP[2:0] | Refresh Rate | Max. No. of pulled-in or postponed REFab | Max. Interval between Two REFab | Max. No. of REFab ¹ | Per Bank Refresh |
|-------------|------------------------|--|---------------------------------|--------------------------------|------------------|
| 000b | Low Temp. Limit | N/A | N/A | N/A | N/A |
| 001b | $4 \times t_{REFI}$ | 8 | $9 \times 4 \times t_{REFI}$ | 16 | 1/8 of REFab |
| 010b | $2 \times t_{REFI}$ | 8 | $9 \times 2 \times t_{REFI}$ | 16 | 1/8 of REFab |
| 011b | $1 \times t_{REFI}$ | 8 | $9 \times t_{REFI}$ | 16 | 1/8 of REFab |
| 100b | $0.5 \times t_{REFI}$ | 8 | $9 \times 0.5 \times t_{REFI}$ | 16 | 1/8 of REFab |
| 101b | $0.25 \times t_{REFI}$ | 8 | $9 \times 0.25 \times t_{REFI}$ | 16 | 1/8 of REFab |
| 110b | $0.25 \times t_{REFI}$ | 8 | $9 \times 0.25 \times t_{REFI}$ | 16 | 1/8 of REFab |
| 111b | High Temp. Limit | N/A | N/A | N/A | N/A |

Note: 1. Maximum number of REFab within $\text{MAX}(2 \times t_{REFI} \times \text{refresh rate multiplier}, 16 \times t_{RFC})$.

Table 100: Modified REFRESH Command Timing Constraints

| MR4 OP[2:0] | Refresh Rate | Max. No. of pulled-in or postponed REFab | Max. Interval between Two REFab | Max. No. of REFab ¹ | Per Bank Refresh |
|-------------|------------------------|--|---------------------------------|--------------------------------|------------------|
| 000B | LOW Temp. Limit | N/A | N/A | N/A | N/A |
| 001B | $4 \times t_{REFI}$ | 2 | $3 \times 4 \times t_{REFI}$ | 4 | 1/8 of REFab |
| 010B | $2 \times t_{REFI}$ | 4 | $5 \times 2 \times t_{REFI}$ | 8 | 1/8 of REFab |
| 011B | $1 \times t_{REFI}$ | 8 | $9 \times t_{REFI}$ | 16 | 1/8 of REFab |
| 100B | $0.5 \times t_{REFI}$ | 8 | $9 \times 0.5 \times t_{REFI}$ | 16 | 1/8 of REFab |
| 101B | $0.25 \times t_{REFI}$ | 8 | $9 \times 0.25 \times t_{REFI}$ | 16 | 1/8 of REFab |
| 110B | $0.25 \times t_{REFI}$ | 8 | $9 \times 0.25 \times t_{REFI}$ | 16 | 1/8 of REFab |
| 111B | HIGH Temp. Limit | N/A | N/A | N/A | N/A |

- Notes:
- For any thermal transition phase where refresh mode is transitioned to either $2 \times t_{REFI}$ or $4 \times t_{REFI}$, LPDDR4 devices will support the previous postponed refresh requirement provided the number of postponed refreshes is monotonically reduced to meet the new requirement. However, the pulled-in REFRESH commands in previous thermal phase are not applied in new thermal phase. Entering new thermal phase the controller must count the number of pulled-in REFRESH commands as zero, regardless of remaining pulled-in REFRESH commands in previous thermal phase.
 - LPDDR4 devices are refreshed properly if memory controller issues REFRESH commands with same or shorter refresh period than reported by MR4 OP[2:0]. If shorter refresh period is applied, the corresponding requirements from Table apply. For example, when MR4 OP[2:0] = 001b, controller can be in any refresh rate from $4 \times t_{REFI}$ to $0.25 \times t_{REFI}$. When MR4 OP[2:0] = 010b, the only prohibited refresh rate is $4 \times t_{REFI}$.



Figure 70: Postponing REFRESH Commands (Example)

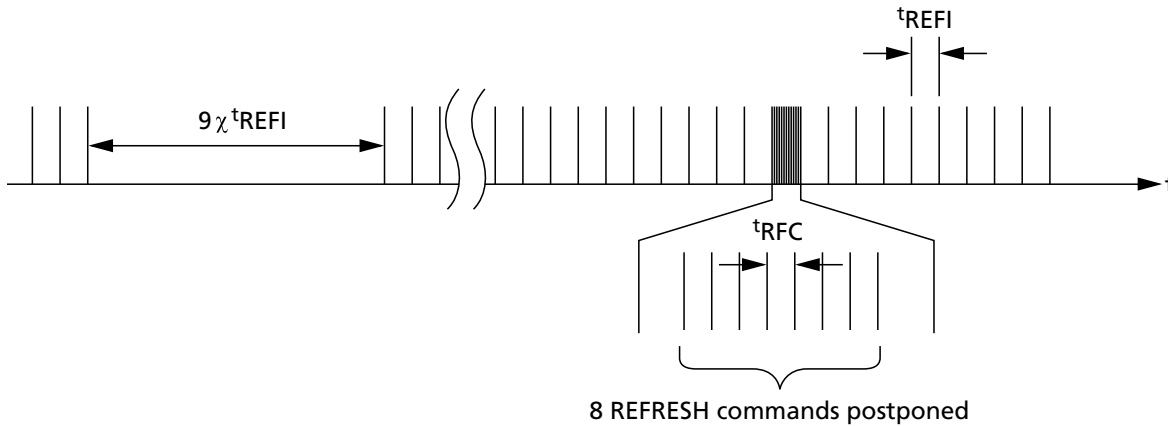
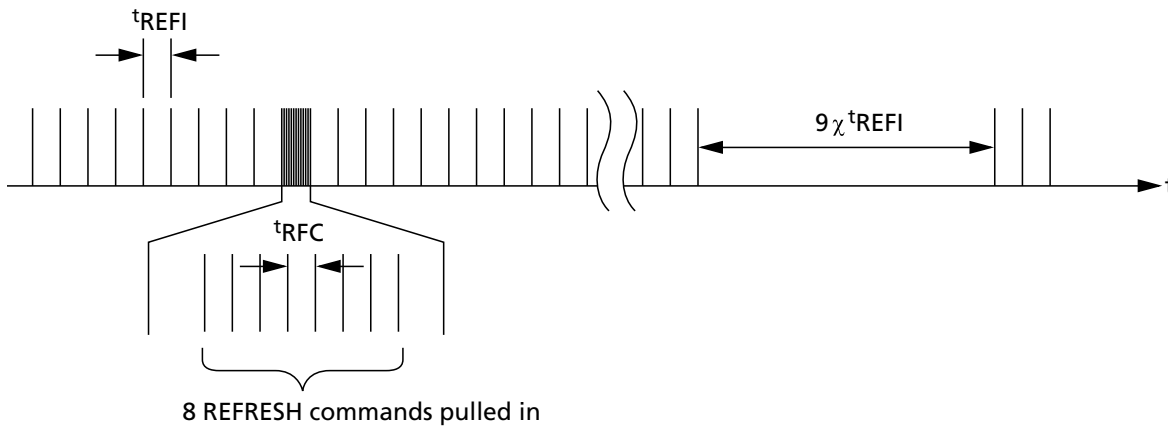


Figure 71: Pulling In REFRESH Commands (Example)



Refresh Requirement

Between the SRX command and SRE command, at least one extra REFRESH command is required. After the SELF REFRESH EXIT command, in addition to the normal REFRESH command at t_{REFI} interval, the device requires a minimum of one extra REFRESH command prior to the SELF REFRESH ENTRY command.

Table 101: Refresh Requirement Parameters

| Parameter | Symbol | Density (per channel) | | | | | | Unit |
|--|------------|-----------------------|-----|-----|-----|-----|------|------|
| | | 2Gb | 3Gb | 4Gb | 6Gb | 8Gb | 12Gb | |
| Number of banks per channel | – | 8 | | | | | | – |
| Refresh window (t_{REFW}): (1 × Refresh) ³ | t_{REFW} | 32 | | | | | | ms |
| Required number of REFRESH commands in t_{REFW} window | R | 8192 | | | | | | – |


Table 101: Refresh Requirement Parameters (Continued)

| Parameter | Symbol | Density (per channel) | | | | | | Unit |
|--|--------|-----------------------|-----|-----|-----|-----|------|------|
| | | 2Gb | 3Gb | 4Gb | 6Gb | 8Gb | 12Gb | |
| Average refresh interval (1 × Refresh) ³ | REFab | †REFI | | | | | | μs |
| | REFpb | †REFIpb | | | | | | ns |
| REFRESH cycle time (all banks) | †RFCab | 130 | 180 | 280 | 380 | 380 | ns | |
| REFRESH cycle time (per bank) | †RFCpb | 60 | 90 | 140 | 190 | 190 | ns | |

- Notes:
1. Refresh for each channel is independent of the other channel on the die, or other channels in a package. Power delivery in the user's system should be verified to make sure the DC operating conditions are maintained when multiple channels are refreshed simultaneously.
 2. Self refresh abort feature is available for higher density devices starting with 6Gb density per channel device and †XSR_abort(MIN) is defined as †RFCpb + 17.5ns.
 3. Refer to MR4 OP[2:0] for detailed refresh rate and its multipliers.

SELF REFRESH Operation

Self Refresh Entry and Exit

The SELF REFRESH command can be used to retain data in the device without external REFRESH commands. The device has a built-in timer to accommodate SELF REFRESH operation. Self refresh is entered by the SELF REFRESH ENTRY command defined by having CS HIGH, CA0 LOW, CA1 LOW, CA2 LOW, CA3 HIGH, CA4 HIGH, and CA5 valid (valid meaning that it is at a logic level HIGH or LOW) for the first rising edge, and CS LOW, CA0 valid, CA1 valid, CA2 valid, CA3 valid, CA4 valid, and CA5 valid at the second rising edge of clock. The SELF REFRESH command is only allowed when READ DATA burst is completed and the device is in the idle state.

During self refresh mode, external clock input is needed and all input pins of the device are activated. The device can accept the following commands: MRR-1, CAS-2, DES, SRX, MPC, MRW-1, and MRW-2, except PASR bank/segment mask setting and SR abort setting.

The device can operate in self refresh mode within the standard and elevated temperature ranges. It also manages self refresh power consumption when the operating temperature changes: lower at low temperatures and higher at high temperatures.

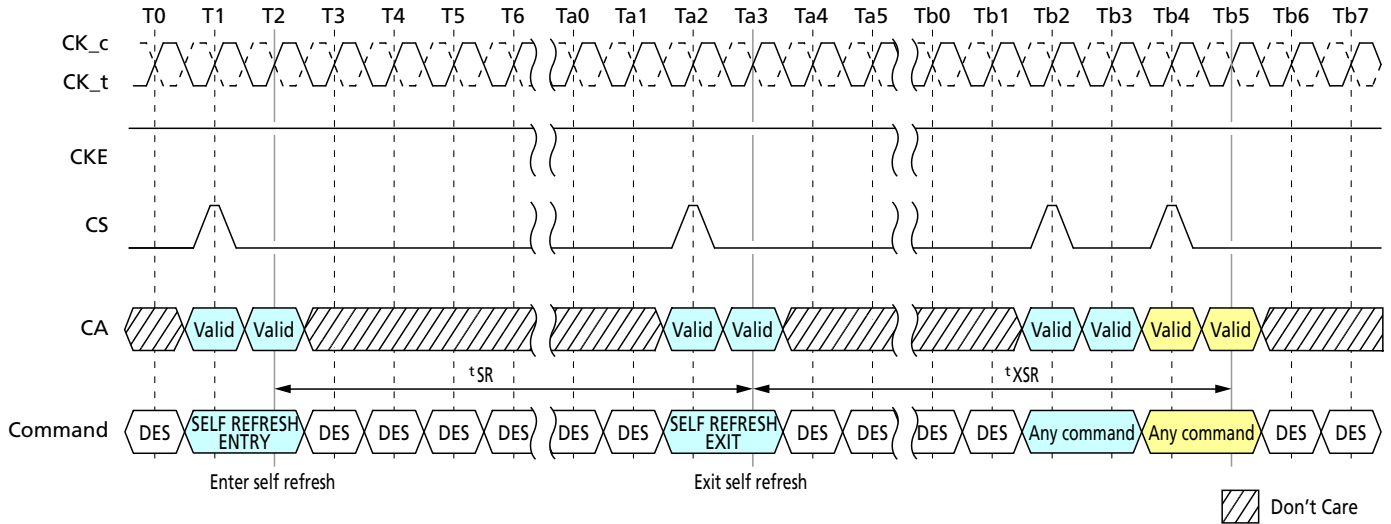
For proper SELF REFRESH operation, power supply pins (V_{DD1} , V_{DD2} , and V_{DDQ}) must be at valid levels. V_{DDQ} can be turned off during self refresh with power-down after †CKELCK is satisfied. (Refer to the Self Refresh Entry/Exit Timing with Power-Down Entry/Exit figure.) Prior to exiting self refresh with power-down, V_{DDQ} must be within specified limits. The minimum time that the device must remain in self refresh mode is †SR(MIN). After self refresh exit is registered, only MRR-1, CAS-2, DES, MPC, MRW-1, and MRW-2 except PASR bank/segment mask setting and SR abort setting are allowed until †XSR is satisfied.

The use of self refresh mode introduces the possibility that an internally timed refresh event can be missed when self refresh exit is registered. Upon exit from self refresh, it is required that at least one REFRESH command (8 per-bank or 1 all-bank) is issued before entry into a subsequent self refresh. This REFRESH command is not included in the



count of regular REFRESH commands required by the t_{REFI} interval, and does not modify the postponed or pulled-in refresh counts; the REFRESH command does count toward the maximum refreshes permitted within $2 \times t_{REFI}$.

Figure 72: Self Refresh Entry/Exit Timing



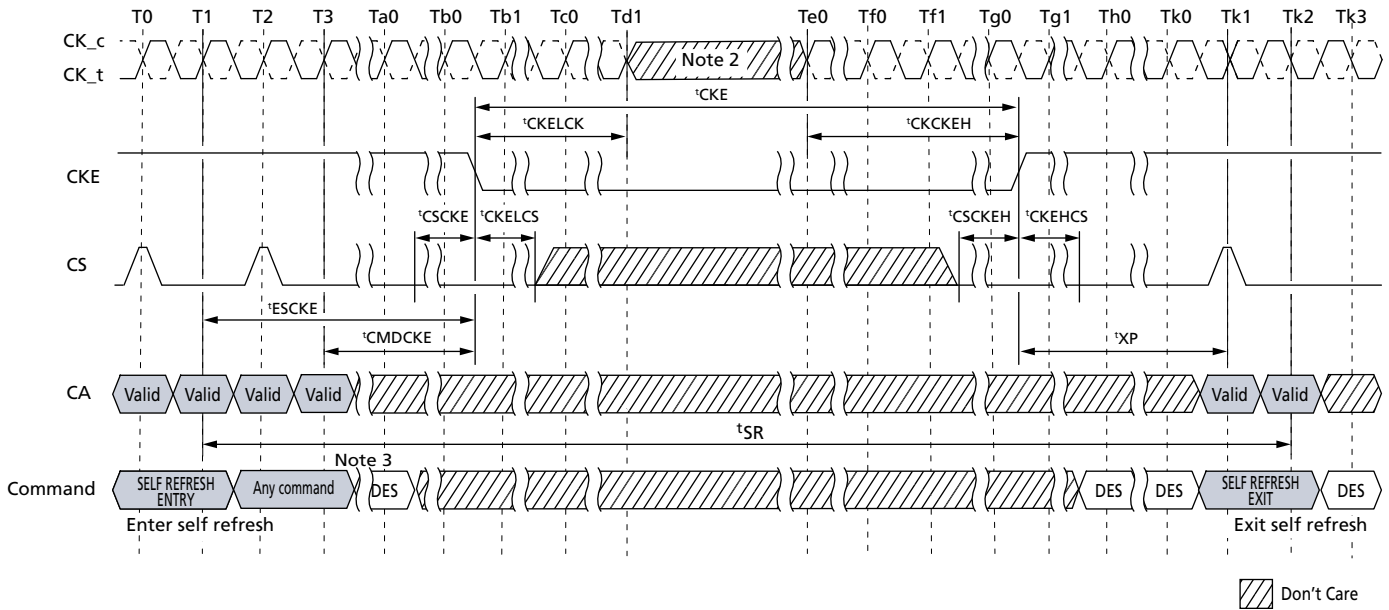
- Notes:
1. MRR-1, CAS-2, DES, SRX, MPC, MRW-1, and MRW-2 commands (except PASR bank/segment mask setting and SR abort setting) are allowed during self refresh.
 2. DES commands are shown for ease of illustration; other commands may be valid at these times.

Power-Down Entry and Exit During Self Refresh

Entering/exiting power-down mode is allowed during self refresh mode. The related timing parameters between self refresh entry/exit and power-down entry/exit are shown below.



Figure 73: Self Refresh Entry/Exit Timing with Power-Down Entry/Exit



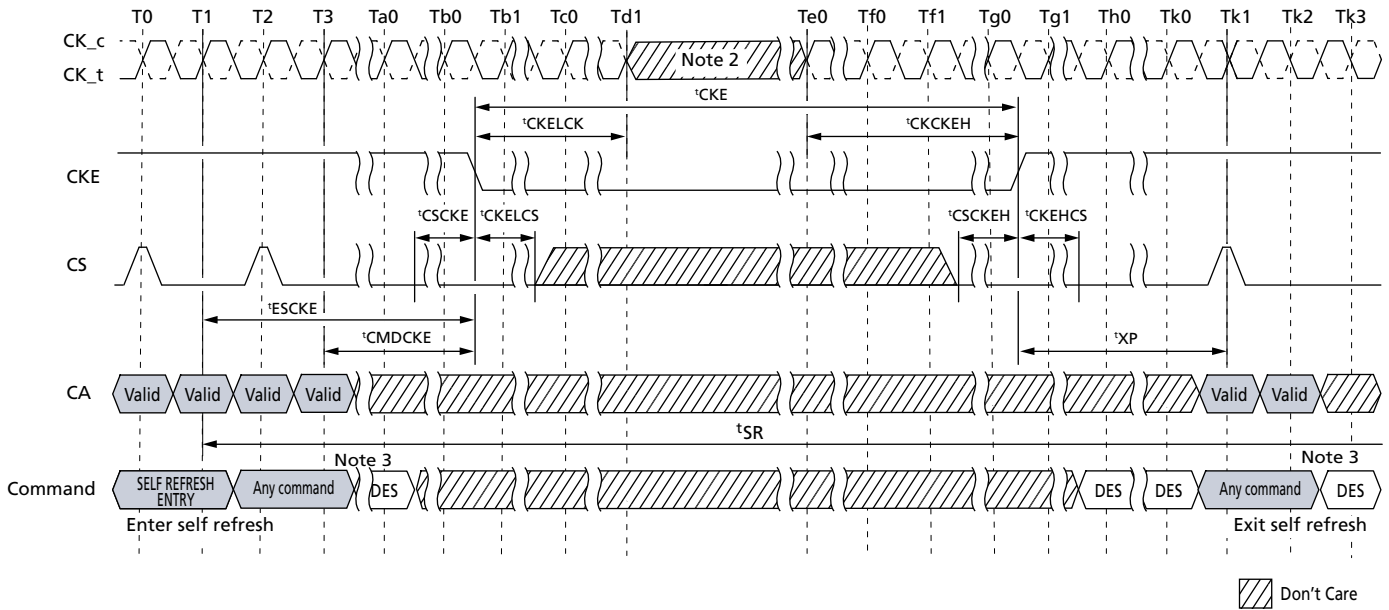
- Notes:
1. MRR-1, CAS-2, DES, SRX, MPC, MRW-1, and MRW-2 commands (except PASR bank/segment mask setting and SR abort setting) are allowed during self refresh.
 2. Input clock frequency can be changed, or the input clock can be stopped, or floated after t_{CKELCK} satisfied and during power-down, provided that upon exiting power-down, the clock is stable and within specified limits for a minimum of t_{CKCKEH} of stable clock prior to power-down exit and the clock frequency is between the minimum and maximum specified frequency for the speed grade in use.
 3. Two clock command for example.

Command Input Timing After Power-Down Exit

Command input timings after power-down exit during self refresh mode are shown below.



Figure 74: Command Input Timings after Power-Down Exit During Self Refresh



- Notes:
1. MRR-1, CAS-2, DES, SRX, MPC, MRW-1, and MRW-2 commands (except PASR bank/segment setting) are allowed during self refresh.
 2. Input clock frequency can be changed or the input clock can be stopped or floated after t_{CKELCK} satisfied and during power-down, provided that upon exiting power-down, the clock is stable and within specified limits for a minimum of t_{CKCKEH} of stable clock prior to power-down exit and the clock frequency is between the minimum and maximum specified frequency for the speed grade in use.
 3. Two clock command for example.

Self Refresh Abort

If MR4 OP[3] is enabled, the device aborts any ongoing refresh during self refresh exit and does not increment the internal refresh counter. The controller can issue a valid command after a delay of t_{XSR_abort} instead of t_{XSR} .

The value of $t_{XSR_abort(MIN)}$ is defined as $t_{RFCpb} + 17.5ns$.

Upon exit from self refresh mode, the device requires a minimum of one extra refresh (eight per bank or one for the entire bank) before entering a subsequent self refresh mode. This requirement remains the same irrespective of the setting of the MR bit for self refresh abort.

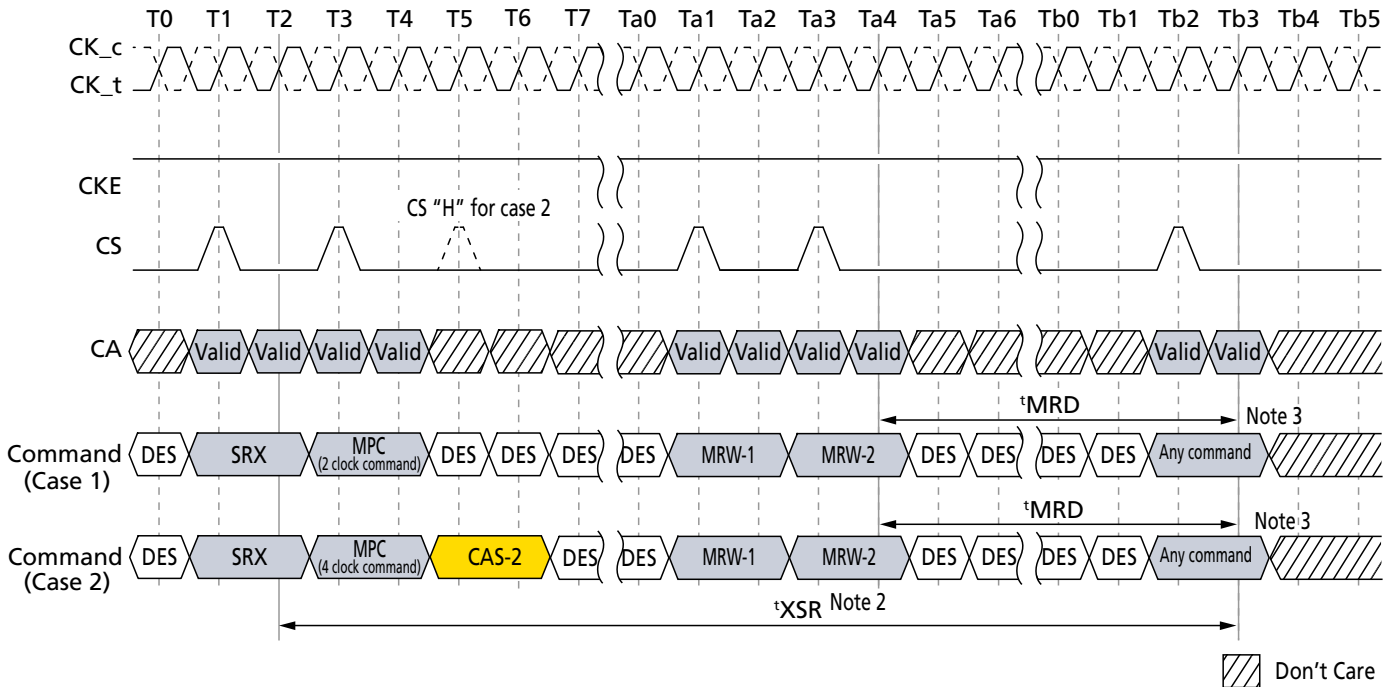
Self refresh abort feature is valid for 6Gb density per channel and larger densities only.

MRR, MRW, MPC Commands During t_{XSR} , t_{RFC}

MODE REGISTER READ (MRR), MULTI PURPOSE (MPC), and MODE REGISTER WRITE (MRW) command except PASR bank/segment mask setting and SR abort setting can be issued during t_{XSR} period.



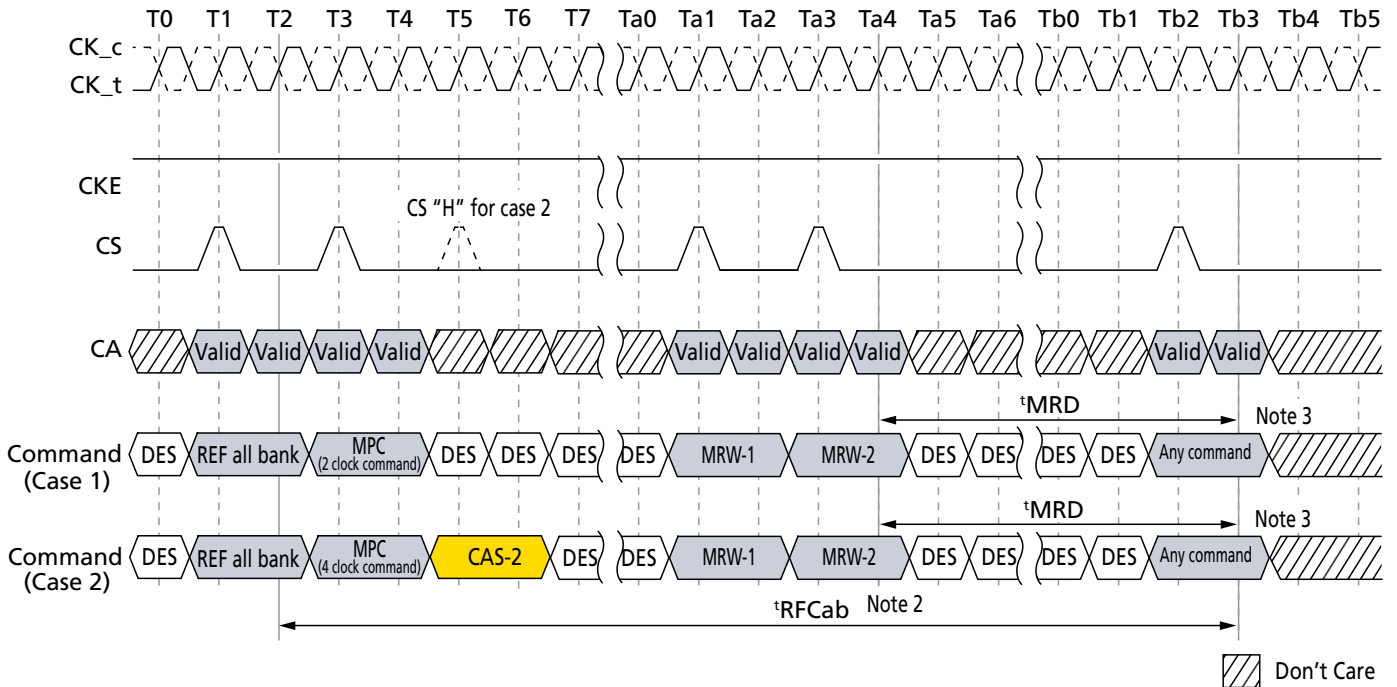
Figure 75: MRR, MRW, and MPC Commands Issuing Timing During t^{XSR}



- Notes:
1. MPC and MRW commands are shown. Any combination of MRR, MRW, and MPC is allowed during t^{XSR} period.
 2. "Any command" includes MRR, MRW, and all MPC commands.
- MRR, MRW, and MPC can be issued during t^{RFC} period.



Figure 76: MRR, MRW, and MPC Commands Issuing Timing During t_{RFC}



- Notes:
1. MPC and MRW commands are shown. Any combination of MRR, MRW, and MPC is allowed during t_{RFCab} or t_{RFCpb} period.
 2. REFRESH cycle time depends on REFRESH command. In the case of per bank REFRESH command issued, REFRESH cycle time will be t_{RFCpb} .
 3. "Any command" includes MRR, MRW, and all MPC commands.



Power-Down Mode

Power-Down Entry and Exit

Power-down is asynchronously entered when CKE is driven LOW. CKE must not go LOW while the following operations are in progress:

- Mode register read
- Mode register write
- Read
- Write
- $V_{REF(CA)}$ range and value setting via MRW
- $V_{REF(DQ)}$ range and value setting via MRW
- Command bus training mode entering/exiting via MRW
- VRCG HIGH current mode entering/exiting via MRW

CKE can go LOW while any other operations such as row activation, precharge, auto precharge, or refresh are in progress. The power-down I_{DD} specification will not be applied until such operations are complete. Power-down entry and exit are shown below.

Entering power-down deactivates the input and output buffers, excluding CKE and RESET_n. To ensure that there is enough time to account for internal delay on the CKE signal path, CS input is required stable LOW level and CA input level is "Don't Care" after CKE is driven LOW, this timing period is defined as t_{CKELCS} . Clock input is required after CKE is driven LOW, this timing period is defined as t_{CKELCK} . CKE LOW will result in deactivation of all input receivers except RESET_n after t_{CKELCK} has expired. In power-down mode, CKE must be held LOW; all other input signals except RESET_n are "Don't Care." CKE LOW must be maintained until $t_{CKE(MIN)}$ is satisfied.

V_{DDQ} can be turned off during power-down after t_{CKELCK} is satisfied. Prior to exiting power-down, V_{DDQ} must be within its minimum/maximum operating range. No REFRESH operations are performed in power-down mode except self refresh power-down. The maximum duration in non-self-refresh power-down mode is only limited by the refresh requirements outlined in the REFRESH command section.

The power-down state is asynchronously exited when CKE is driven HIGH. CKE HIGH must be maintained until $t_{CKE(MIN)}$ is satisfied. A valid, executable command can be applied with power-down exit latency t_{XP} after CKE goes HIGH. Power-down exit latency is defined in the AC timing parameter table.

Clock frequency change or clock stop is inhibited during t_{CMDCKE} , t_{CKELCK} , t_{CKCKEH} , t_{XP} , $t_{MRWCKEL}$, and t_{ZQCKE} periods.

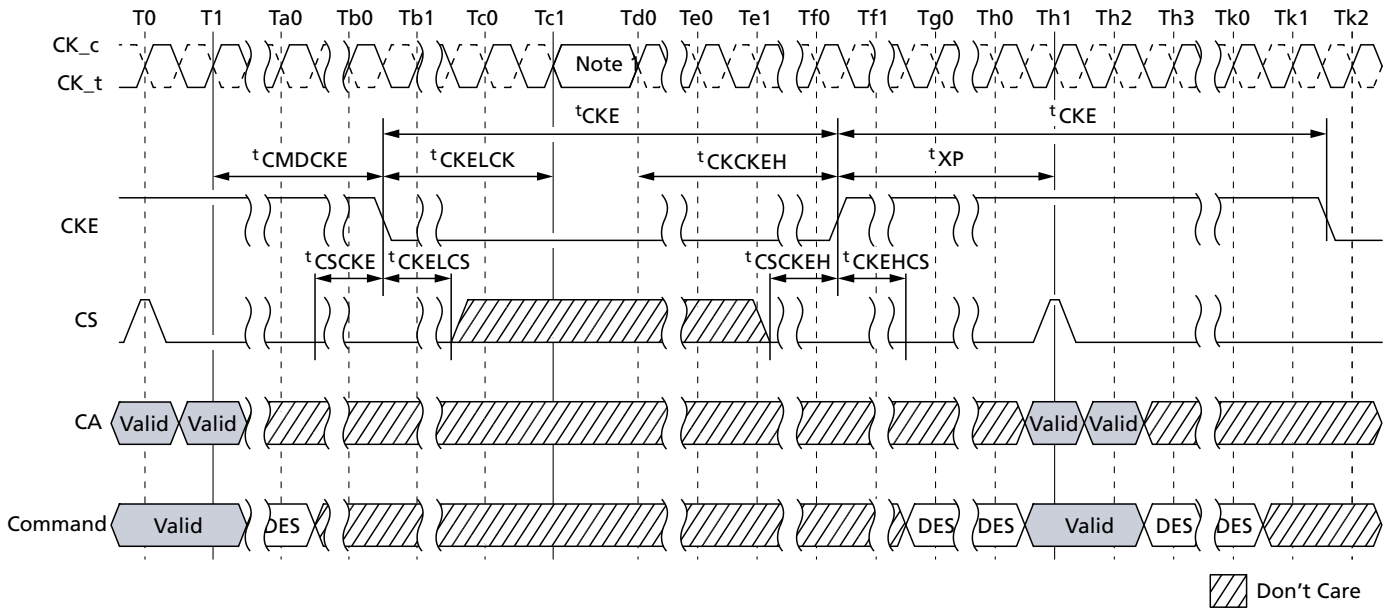
If power-down occurs when all banks are idle, this mode is referred to as idle power-down. If power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. And if power-down occurs when self refresh is in progress, this mode is referred to as self refresh power-down in which the internal refresh is continuing in the same way as self refresh mode.

When CA, CK, and/or CS ODT is enabled via MR11 OP[6:4] and also via MR22 or CA-ODT pad setting, the rank providing ODT will continue to terminate the command bus in all DRAM states including power-down when V_{DDQ} is stable and within its minimum/maximum operating range.



The LPDDR4 DRAM cannot be placed in power-down state during start DQS interval oscillator operation.

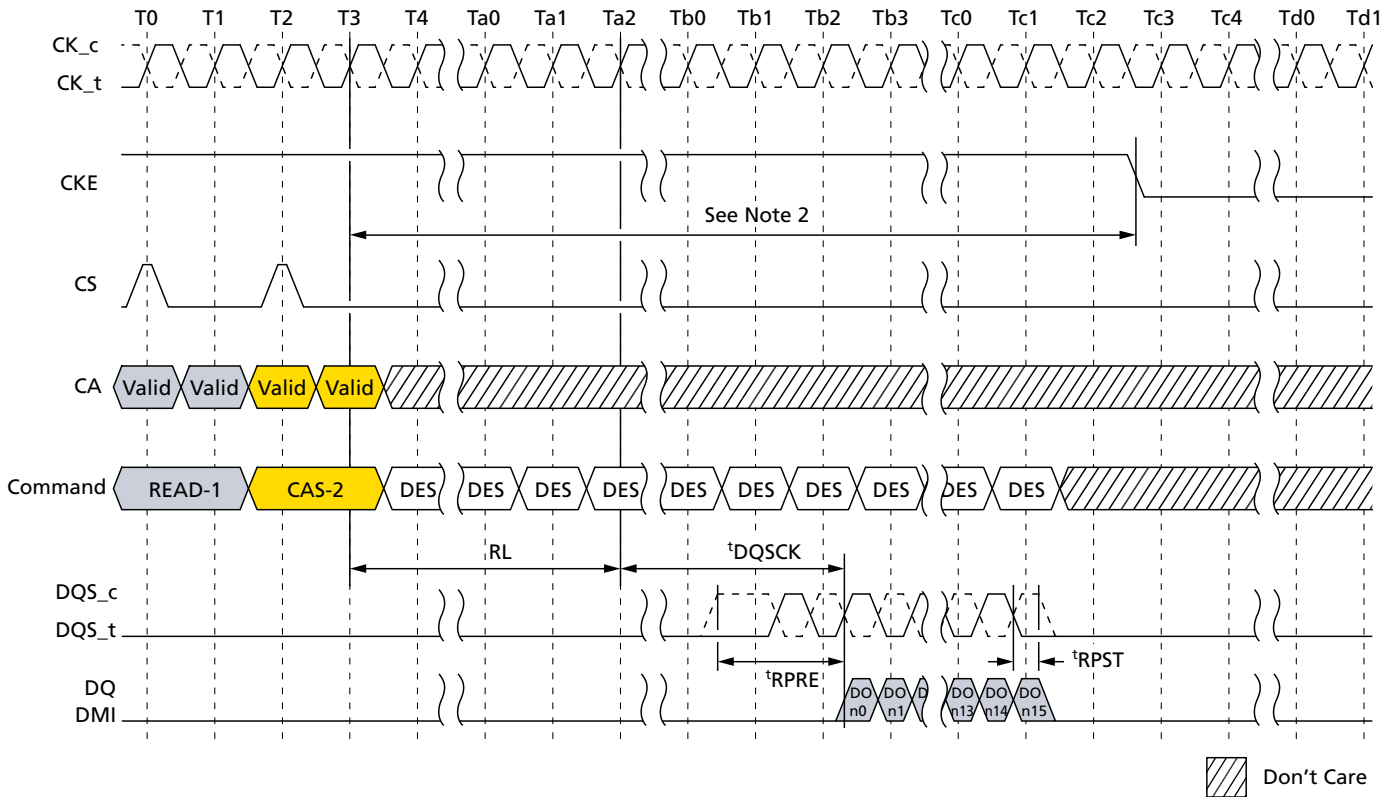
Figure 77: Basic Power-Down Entry and Exit Timing



Note: 1. Input clock frequency can be changed or the input clock can be stopped or floated during power-down, provided that upon exiting power-down, the clock is stable and within specified limits for a minimum of t_{CKCKEH} of stable clock prior to power-down exit and the clock frequency is between the minimum and maximum specified frequency for the speed grade in use.



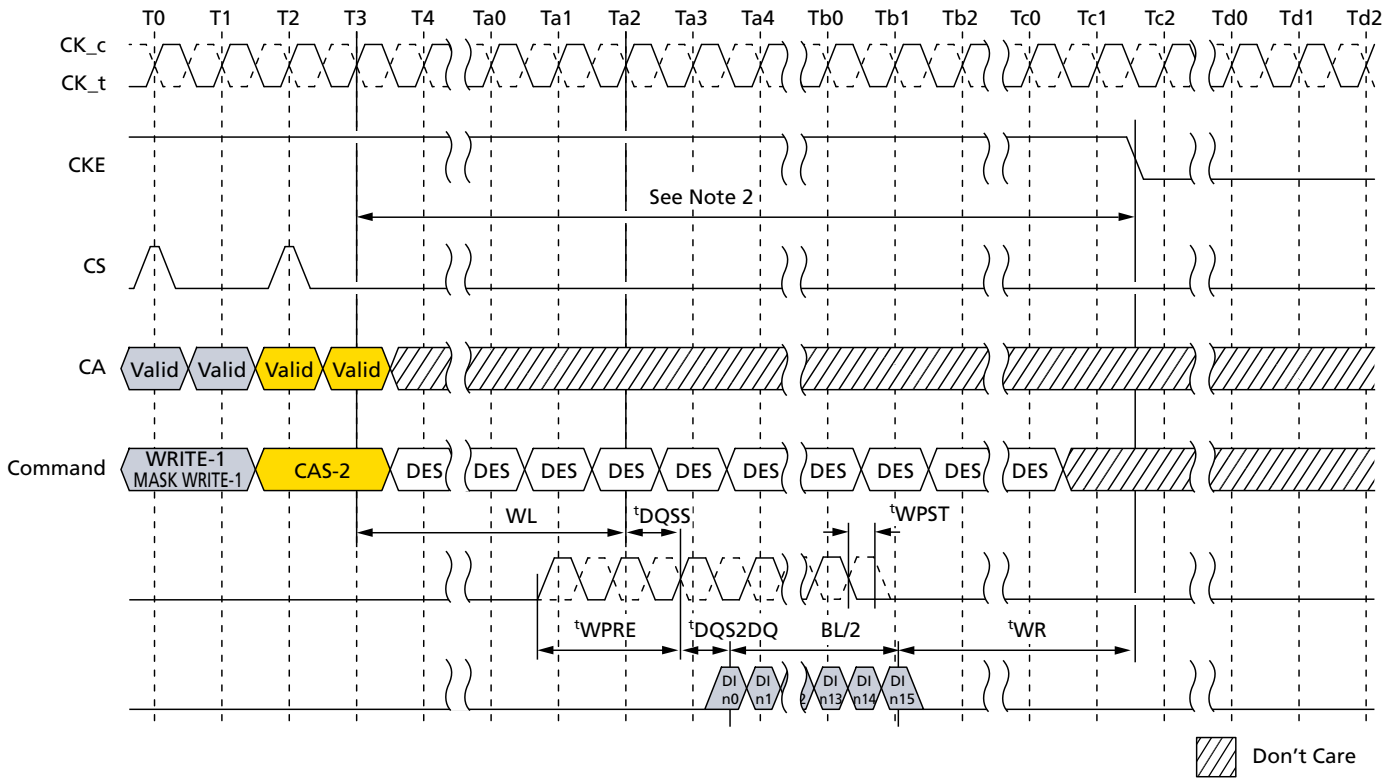
Figure 78: Read and Read with Auto Precharge to Power-Down Entry



- Notes:
1. CKE must be held HIGH until the end of the burst operation.
 2. Minimum delay time from READ command or READ with AUTO PRECHARGE command to falling edge of CKE signal is as follows:
 - When read postamble = $0.5nCK$ (MR1 OP[7] = [0]),
 $(RL \times tCK) + tDQSCK(MAX) + ((BL/2) \times tCK) + 1tCK$
 - When read postamble = $1.5nCK$ (MR1 OP[7] = [1]),
 $(RL \times tCK) + tDQSCK(MAX) + ((BL/2) \times tCK) + 2tCK$



Figure 79: Write and Mask Write to Power-Down Entry

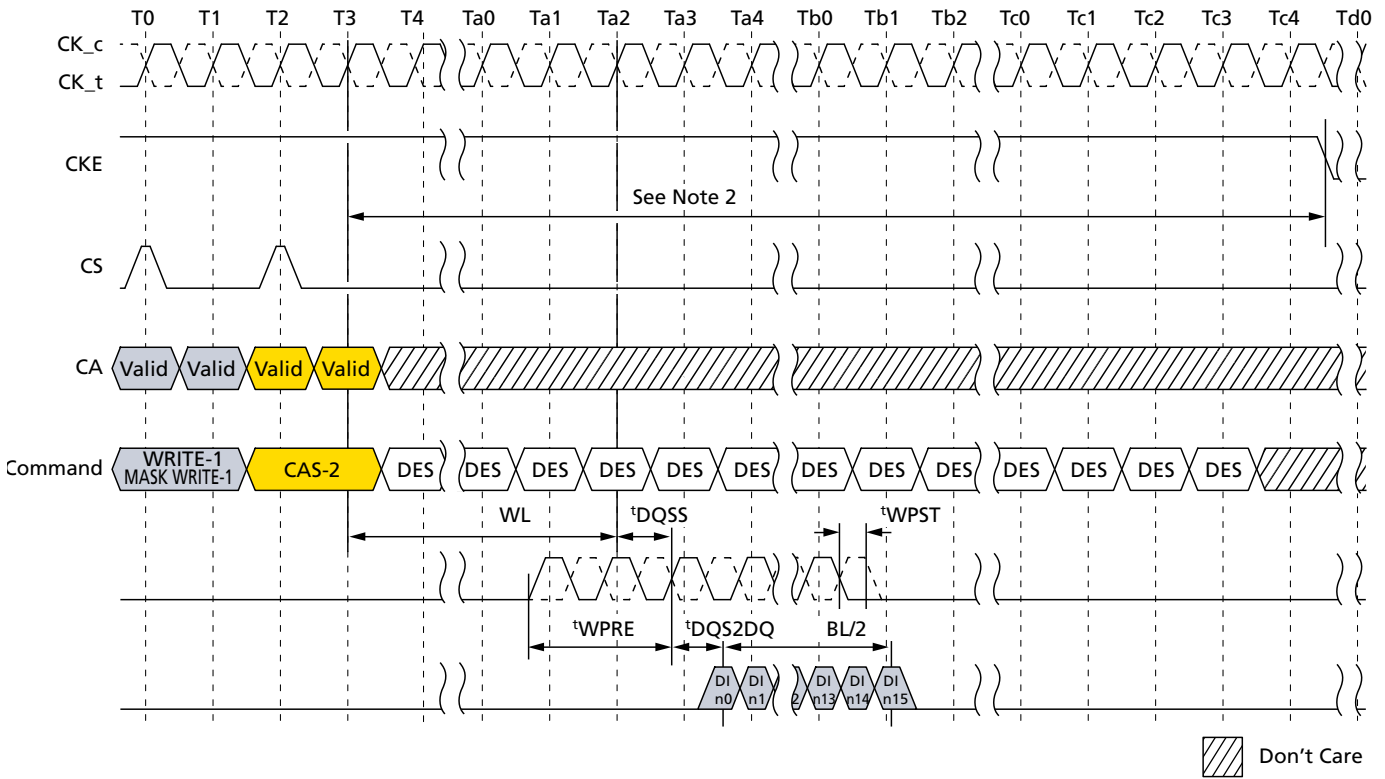


- Notes:
1. CKE must be held HIGH until the end of the burst operation.
 2. Minimum delay time from WRITE command or MASK WRITE command to falling edge of CKE signal is as follows:

$$(WL \times t_{CK}) + t_{DQSS(MAX)} + t_{DQS2DQ(MAX)} + ((BL/2) \times t_{CK}) + t_{WR}$$
 3. This timing is applied regardless of DQ ODT disable/enable setting: MR11 OP[2:0].
 4. This timing diagram only applies to the WRITE and MASK WRITE commands without auto precharge.



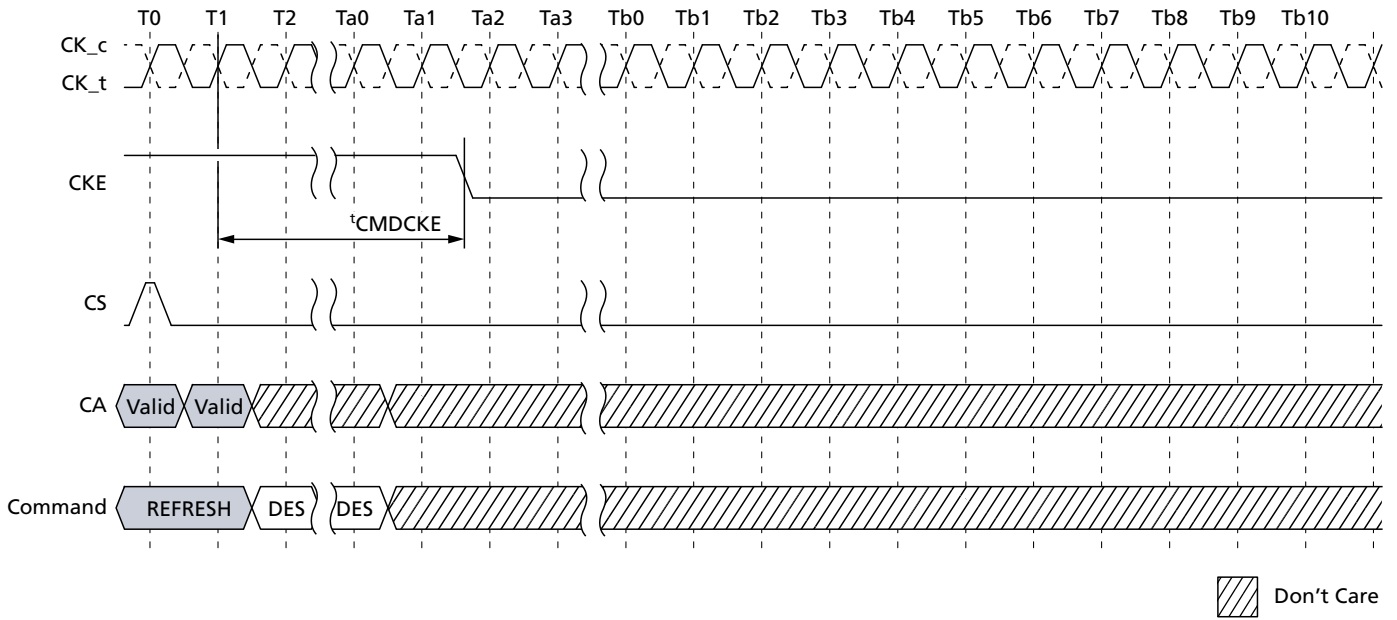
Figure 80: Write With Auto Precharge and Mask Write With Auto Precharge to Power-Down Entry



- Notes:
1. CKE must be held HIGH until the end of the burst operation.
 2. Delay time from WRITE with AUTO PRECHARGE command or MASK WRITE with AUTO PRECHARGE command to falling edge of CKE signal is more than $(WL \times t_{CK}) + t_{DQSS(MAX)} + t_{DQ52DQ(MAX)} + ((BL/2) \times t_{CK}) + (n_{WR} \times t_{CK}) + (2 \times t_{CK})$
 3. This timing is applied regardless of DQ ODT disable/enable setting: MR11 OP[2:0].

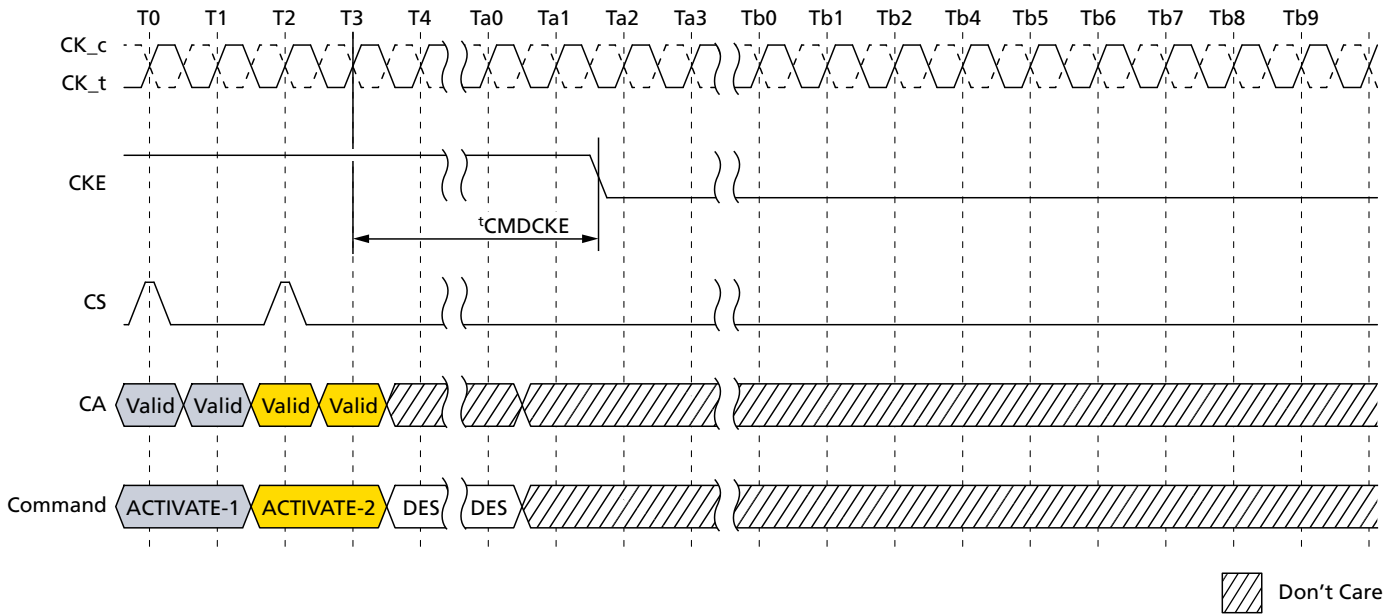


Figure 81: Refresh Entry to Power-Down Entry



Note: 1. CKE must be held HIGH until t_{CMDCKE} is satisfied.

Figure 82: ACTIVATE Command to Power-Down Entry



Note: 1. CKE must be held HIGH until t_{CMDCKE} is satisfied.



Figure 83: PRECHARGE Command to Power-Down Entry

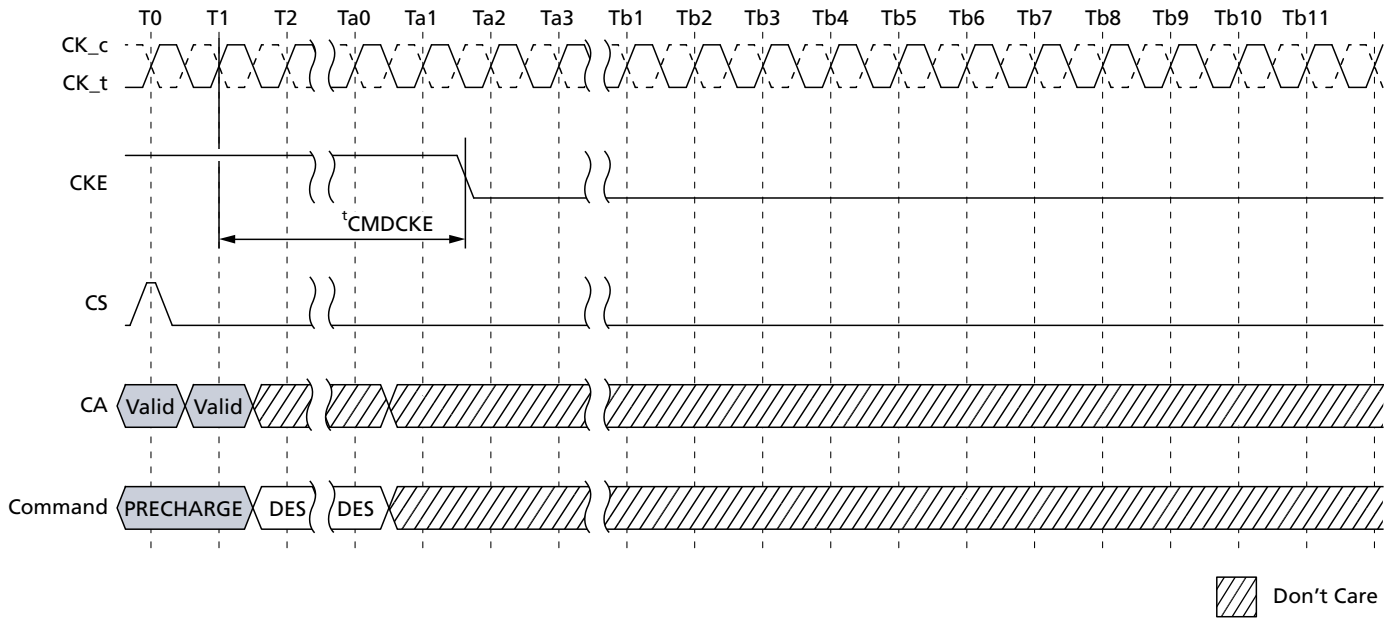
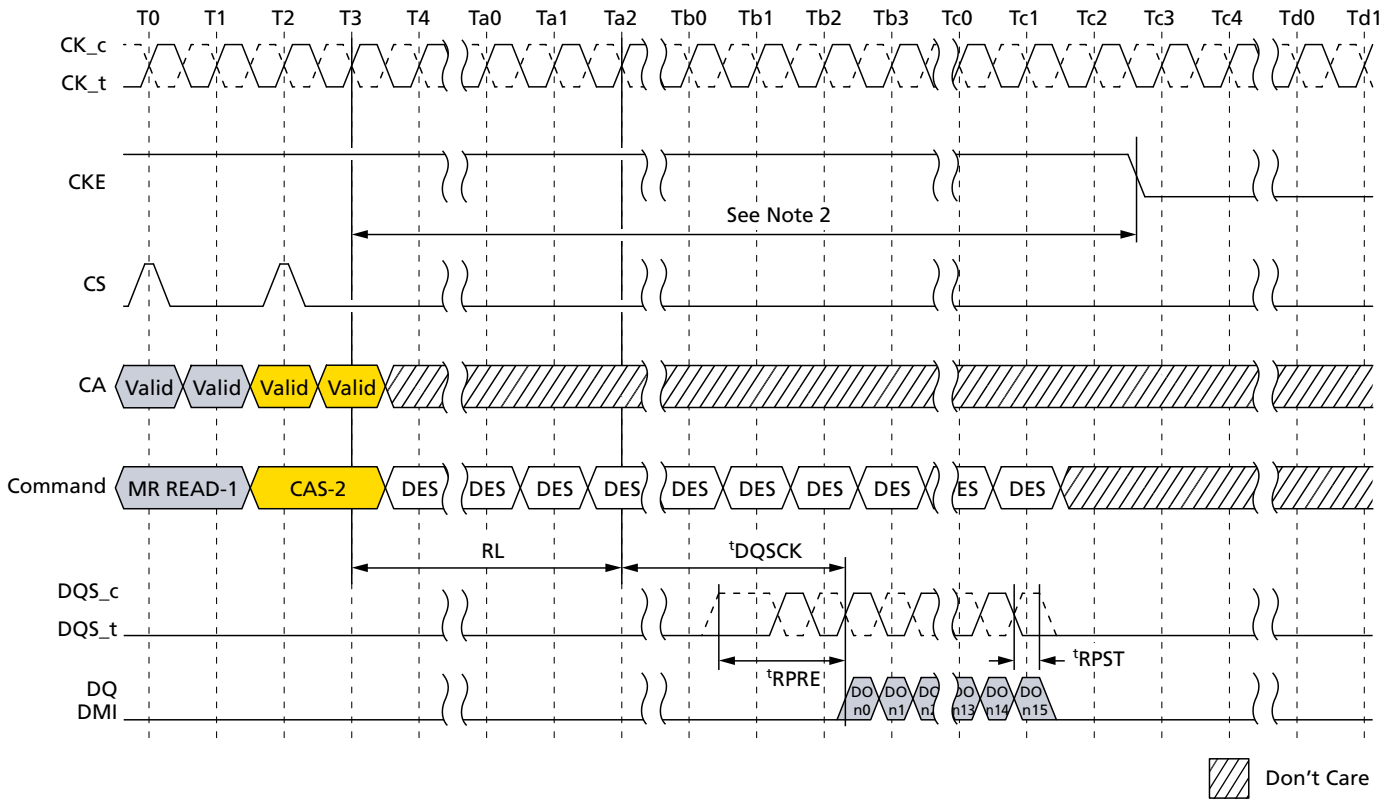




Figure 84: Mode Register Read to Power-Down Entry



- Notes: 1. CKE must be held HIGH until the end of the burst operation.
2. Minimum delay time from MODE REGISTER READ command to falling edge of CKE signal is as follows:

When read postamble = 0.5nCK (MR1 OP[7] = [0]),

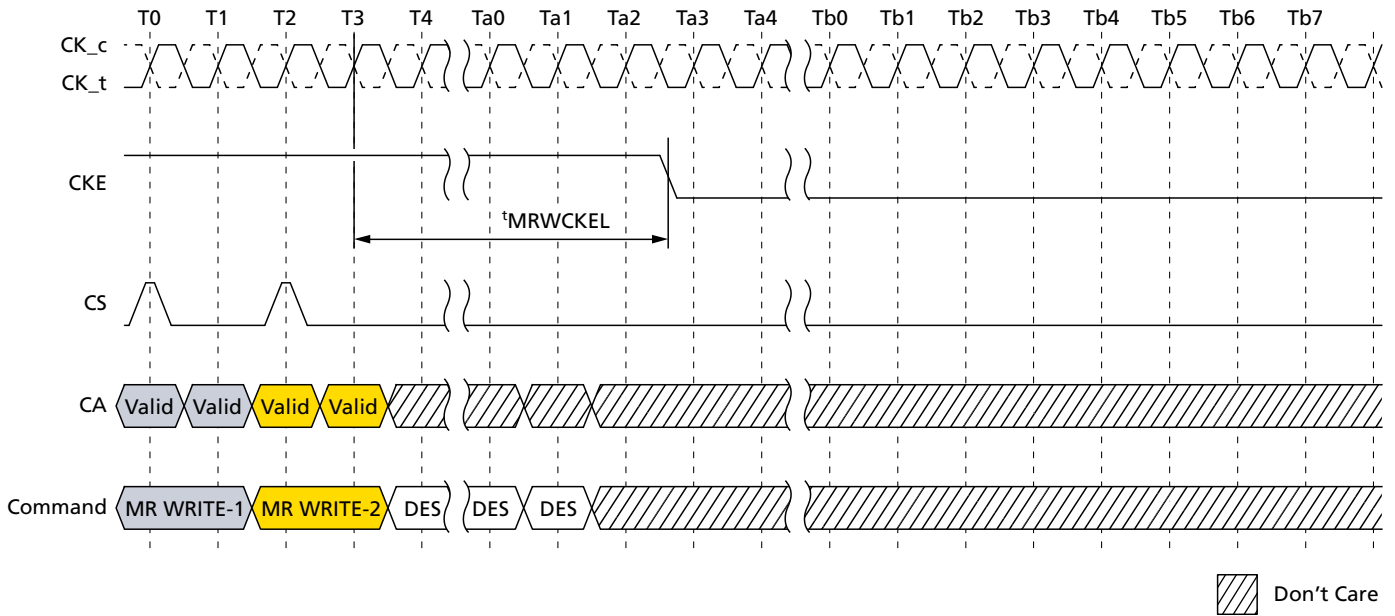
$$(RL \times tCK) + tDQSCK(MAX) + ((BL/2) \times tCK) + 1tCK$$

When read postamble = 1.5nCK (MR1 OP[7] = [1]),

$$(RL \times tCK) + tDQSCK(MAX) + ((BL/2) \times tCK) + 2tCK$$



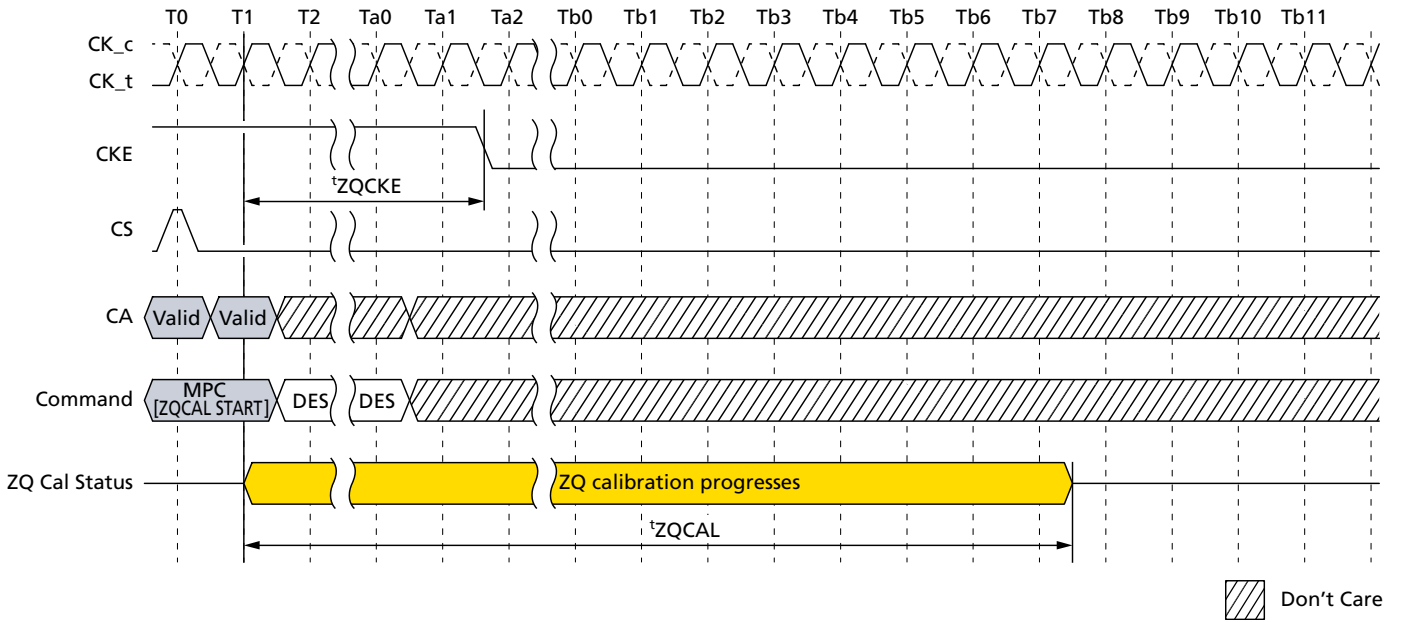
Figure 85: Mode Register Write to Power-Down Entry



- Notes:
1. CKE must be held HIGH until $t_{MRWCKEL}$ is satisfied.
 2. This timing is the general definition for power-down entry after MODE REGISTER WRITE command. When a MODE REGISTER WRITE command changes a parameter or starts an operation that requires special timing longer than $t_{MRWCKEL}$, that timing must be satisfied before CKE is driven LOW. Changing the $V_{REF(DQ)}$ value is one example, in this case the appropriate $t_{VREF-SHORT/MIDDLE/LONG}$ must be satisfied.



Figure 86: MULTI PURPOSE Command for ZQCAL Start to Power-Down Entry



Note: 1. ZQ calibration continues if CKE goes LOW after t_{ZQCKE} is satisfied.



Input Clock Stop and Frequency Change

Clock Frequency Change – CKE LOW

During CKE LOW, the device supports input clock frequency changes under the following conditions:

- $t_{CK(ABS)min}$ is met for each clock cycle
- Refresh requirements apply during clock frequency change
- During clock frequency change, only REFab or REFpb commands may be executing
- Any ACTIVATE or PRECHARGE commands have completed prior to changing the frequency
- Related timing conditions, t_{RCD} and t_{RP} , have been met prior to changing the frequency
- The initial clock frequency must be maintained for a minimum of t_{CKELCK} after CKE goes LOW
- The clock satisfies $t_{CH(ABS)}$ and $t_{CL(ABS)}$ for a minimum of t_{CKCKEH} prior to CKE going HIGH

After the input clock frequency changes and CKE is held HIGH, additional MRW commands may be required to set the WR, RL, and so forth. These settings may require adjustment to meet minimum timing requirements at the target clock frequency.

Clock Stop – CKE LOW

During CKE LOW, the device supports clock stop under the following conditions:

- CK_t and CK_c are don't care during clock stop
- Refresh requirements apply during clock stop
- During clock stop, only REFab or REFpb commands may be executing
- Any ACTIVATE or PRECHARGE commands have completed prior to stopping the clock
- Related timing conditions, t_{RCD} and t_{RP} , have been met prior to stopping the clock
- The initial clock frequency must be maintained for a minimum of t_{CKELCK} after CKE goes LOW
- The clock satisfies $t_{CH(ABS)}$ and $t_{CL(ABS)}$ for a minimum of t_{CKCKEH} prior to CKE going HIGH

Clock Frequency Change – CKE HIGH

During CKE HIGH, the device supports input clock frequency change under the following conditions:

- $t_{CK(ABS)min}$ is met for each clock cycle
- Refresh requirements apply during clock frequency change
- During clock frequency change, only REFab or REFpb commands may be executing
- Any ACTIVATE, READ, WRITE, PRECHARGE, MODE REGISTER WRITE, or MODE REGISTER READ commands (and any associated data bursts) have completed prior to changing the frequency
- Related timing conditions (t_{RCD} , t_{WR} , t_{RP} , t_{MRW} , and t_{MRR}) have been met prior to changing the frequency



- During clock frequency change, CS is held LOW
- The device is ready for normal operation after the clock satisfies $t_{CH}(abs)$ and $t_{CL}(abs)$ for a minimum of $2 \times t_{CK} + t_{XP}$

After the input clock frequency is changed, additional MRW commands may be required to set the WR, RL, and so forth. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

Clock Stop – CKE HIGH

During CKE HIGH, the device supports clock stop under the following conditions:

- CK_t is held LOW and CK_c is held HIGH during clock stop
- During clock stop, CS is held LOW
- Refresh requirements apply during clock stop
- During clock stop, only REF_{ab} or REF_{pb} commands may be executing
- Any ACTIVATE, READ, WRITE, MPC (WRITE-FIFO, READ-FIFO, READ DQ CALIBRATION), PRECHARGE, MODE REGISTER WRITE, or MODE REGISTER READ commands have completed, including any associated data bursts and extra 4 clock cycles must be provided prior to stopping the clock
- Related timing conditions (t_{RCD} , t_{WR} , t_{RP} , t_{MRW} , t_{MRR} , t_{ZQLAT} , and so forth) have been met prior to stopping the clock
- READ with AUTO PRECHARGE and WRITE with AUTO PRECHARGE commands need extra 4 clock cycles in addition to the related timing constraints, nWR and nRTP, to complete the operations
- REF_{ab}, REF_{pb}, SRE, SRX, and MPC[ZQCAL START] commands are required to have extra 4 clock cycles prior to stopping the clock
- The device is ready for normal operation after the clock is restarted and satisfies $t_{CH}(abs)$ and $t_{CL}(abs)$ for a minimum of $2 \times t_{CK} + t_{XP}$



MODE REGISTER READ Operation

The MODE REGISTER READ (MRR) command is used to read configuration and status data from the device registers. The MRR command is initiated with CS and CA[5:0] in the proper state as defined by the Command Truth Table. The mode register address operands (MA[5:0]) enable the user to select one of 64 registers. The mode register contents are available on the first four UI data bits of DQ[7:0] after $RL \times {}^tCK + {}^tDQSCK + {}^tDQSQ$ following the MRR command. Subsequent data bits contain valid but undefined content. DQS is toggled for the duration of the MODE REGISTER READ burst. The MRR has a command burst length of 16. MRR operation must not be interrupted.

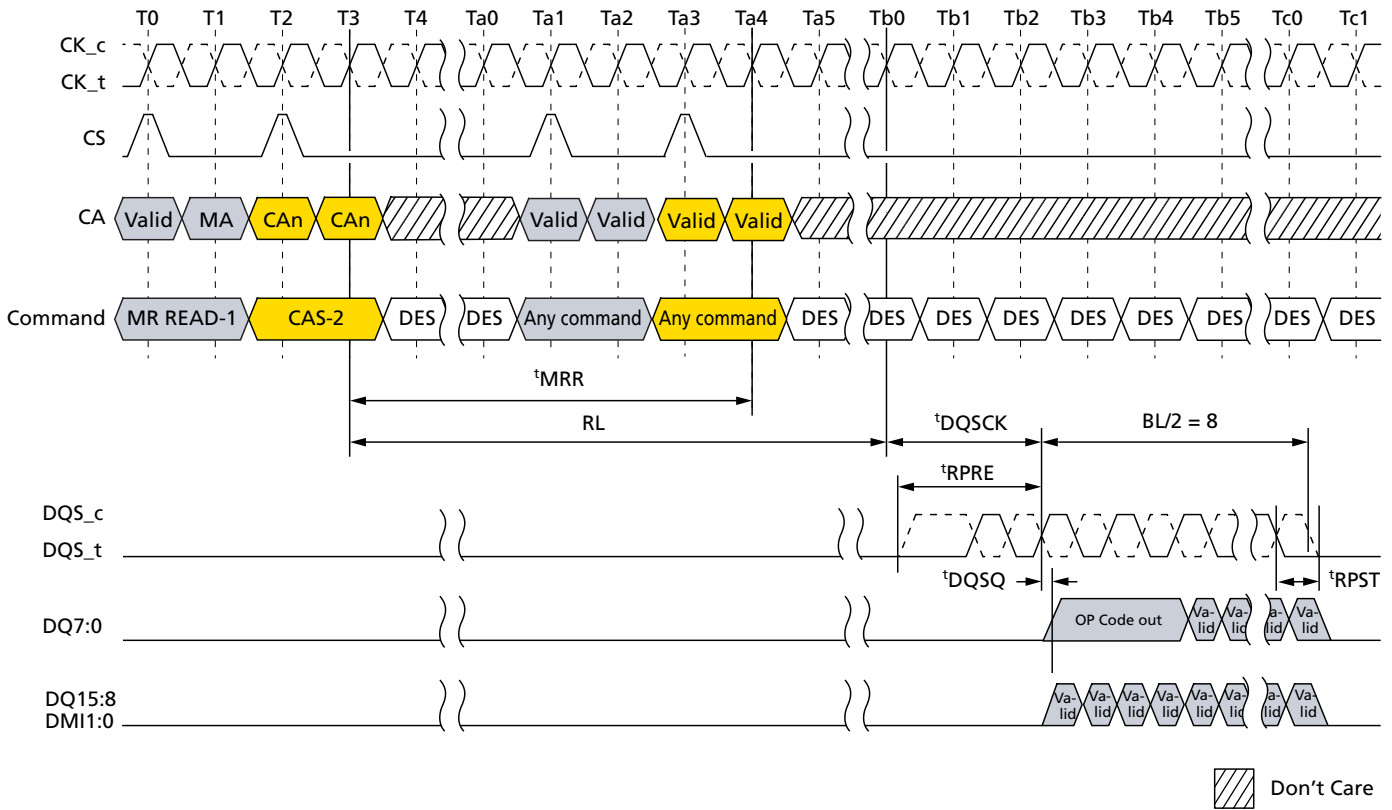
Table 102: MRR

| UI | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
|---------------|-----|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|
| DQ0 | OP0 | | | V | | | | | | | | | | | | |
| DQ1 | OP1 | | | V | | | | | | | | | | | | |
| DQ2 | OP2 | | | V | | | | | | | | | | | | |
| DQ3 | OP3 | | | V | | | | | | | | | | | | |
| DQ4 | OP4 | | | V | | | | | | | | | | | | |
| DQ5 | OP5 | | | V | | | | | | | | | | | | |
| DQ6 | OP6 | | | V | | | | | | | | | | | | |
| DQ7 | OP7 | | | V | | | | | | | | | | | | |
| DQ8– DQ15 | V | | | | | | | | | | | | | | | |
| DMI0– DMI1 | V | | | | | | | | | | | | | | | |

- Notes:
1. MRR data are extended to the first 4 UIs, allowing the LPDRAM controller to sample data easily.
 2. DBI during MRR depends on mode register setting MR3 OP[6].
 3. The read preamble and postamble of MRR are the same as for a normal read.



Figure 87: MODE REGISTER READ Operation



- Notes:
1. Only BL = 16 is supported.
 2. Only DESELECT is allowed during t_{MRR} period.
 3. There are some exceptions about issuing commands after t_{MRR} . Refer to MRR/MRW Timing Constraints Table for detail.
 4. DBI is disable mode.
 5. DES commands except t_{MRR} period are shown for ease of illustration; other commands may be valid at these times.
 6. DQ/DQS: V_{SSQ} termination

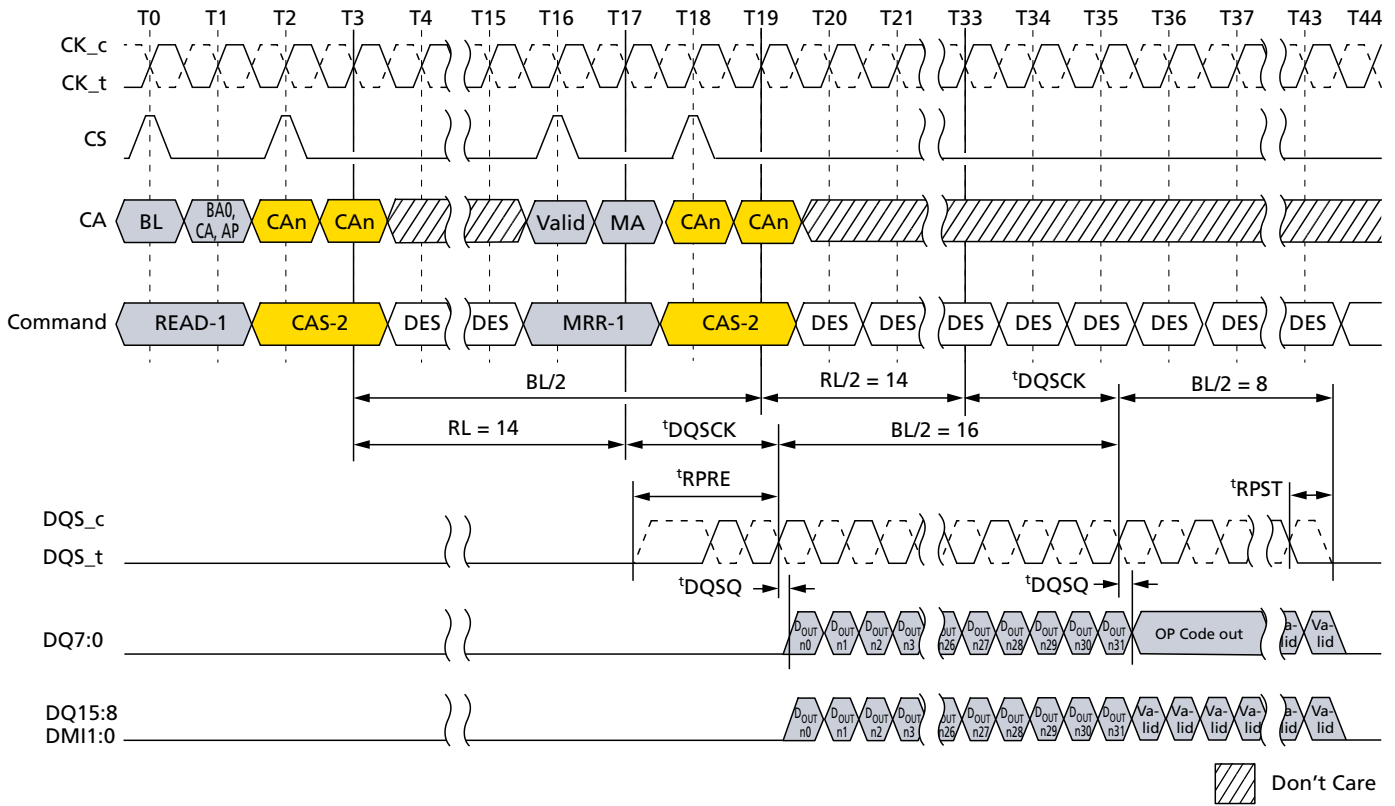
MRR After a READ and WRITE Command

After a prior READ command, the MRR command must not be issued earlier than $BL/2$ clock cycles, in a similar way $WL + BL/2 + 1 + RU(t_{WTR}/t_{CK})$ clock cycles after a PRIOR WRITE, WRITE with AP, MASK WRITE, MASK WRITE with AP, and MPC[WRITE-FIFO] command in order to avoid the collision of READ and WRITE burst data on device internal data bus.



**200b: x32 LPDDR4 SDRAM
MODE REGISTER READ Operation**

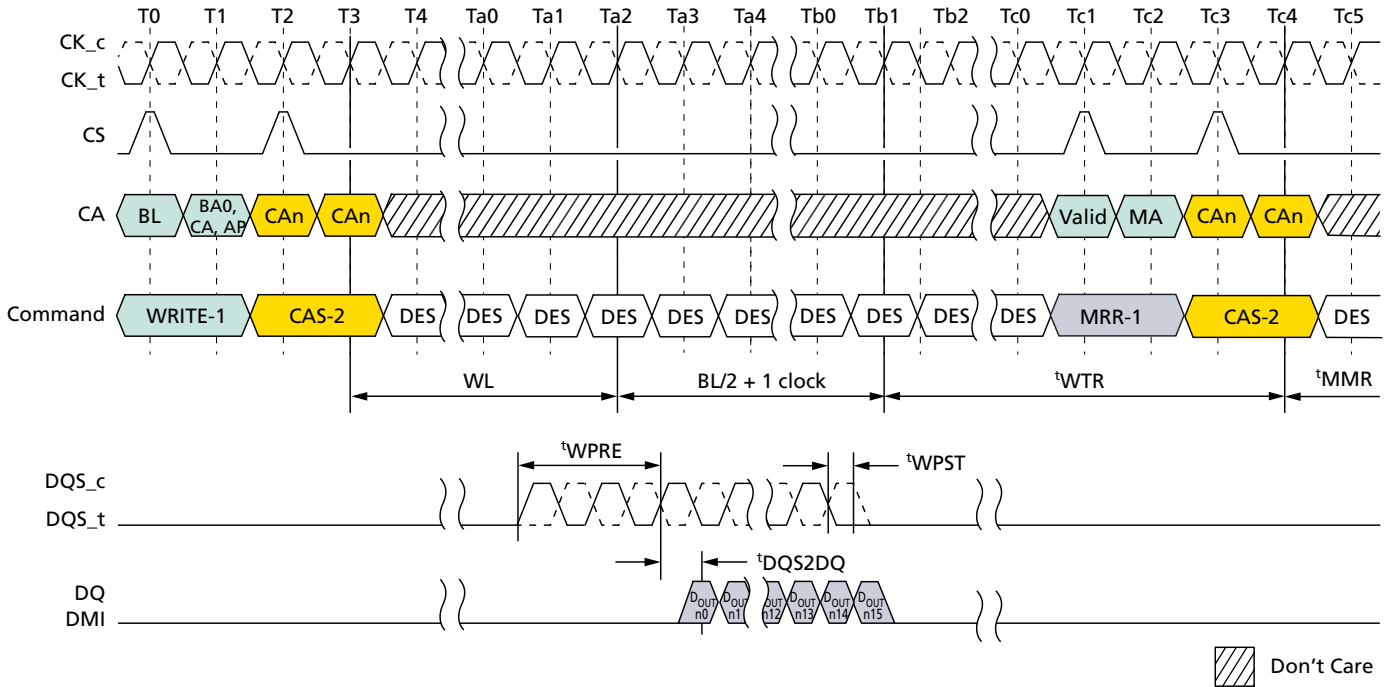
Figure 88: READ-to-MRR Timing



- Notes:
1. The minimum number of clock cycles from the burst READ command to the MRR command is BL/2.
 2. Read BL = 32, MRR BL = 16, RL = 14, Preamble = Toggle, Postamble = 0.5nCK, DBI = Disable, DQ/DQS: V_{SSQ} termination.
 3. D_{OUT} n = data-out to column n.
 4. DES commands except tMRR period are shown for ease of illustration; other commands may be valid at these times.



Figure 89: WRITE-to-MRR Timing



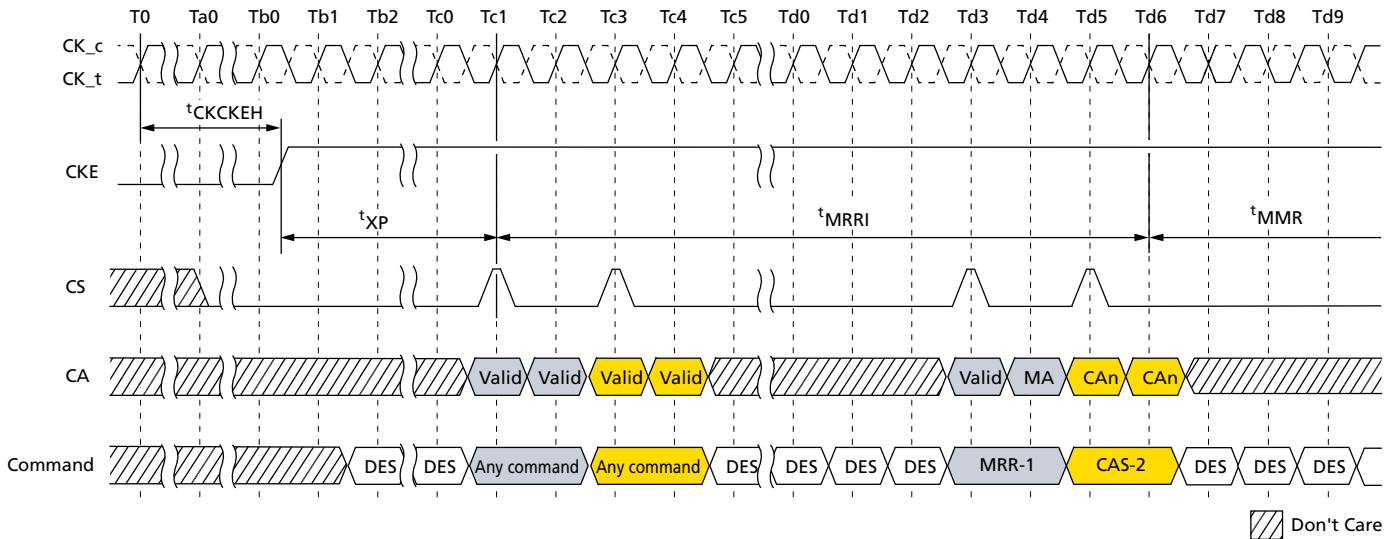
- Notes:
1. Write BL = 16, Write postamble = $0.5nCK$, DQ/DQS: V_{SSQ} termination.
 2. Only DES is allowed during t_{MMR} period.
 3. $D_{OUT} n$ = data-out to column n .
 4. The minimum number of clock cycles from the BURST WRITE command to MRR command is $WL + BL/2 + 1 + RU(t_{WTR}/t_{CK})$.
 5. t_{WTR} starts at the rising edge of CK after the last latching edge of DQS.
 6. DES commands except t_{MMR} period are shown for ease of illustration; other commands may be valid at these times.

MRR After Power-Down Exit

Following the power-down state, an additional time, t_{MRRI} , is required prior to issuing the MODE REGISTER READ (MRR) command. This additional time (equivalent to t_{RCD}) is required in order to maximize power-down current savings by allowing more power-up time for the MRR data path after exit from power-down mode.



Figure 90: MRR Following Power-Down

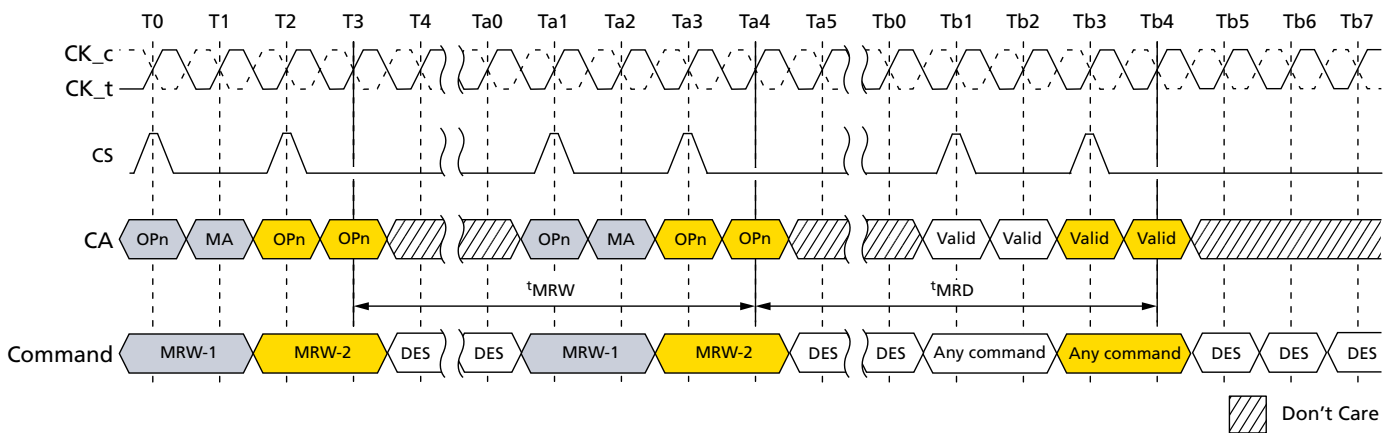


- Notes:
1. Only DES is allowed during t_{MRR} period.
 2. DES commands except t_{MRR} period are shown for ease of illustration; other commands may be valid at these times.

MODE REGISTER WRITE

The MODE REGISTER WRITE (MRW) writes configuration data to the mode registers. The MRW command is initiated with CKE, CS, and CA[5:0] to valid levels at the rising edge of the clock. The mode register address and the data written to it is contained in CA[5:0] according to the Command Truth Table. The MRW command period is defined by t_{MRW} . Mode register WRITES to read-only registers have no impact on the functionality of the device.

Figure 91: MODE REGISTER WRITE Timing





Mode Register Write States

MRW can be issued from either a bank-idle or a bank-active state. Certain restrictions may apply for MRW from an active state.

Table 103: Truth Table for MRR and MRW

| Current State | Command | Intermediate State | Next State |
|----------------|---------|---------------------------------------|----------------|
| All banks idle | MRR | Reading mode register, all banks idle | All banks idle |
| | MRW | Writing mode register, all banks idle | All banks idle |
| Bank(s) active | MRR | Reading mode register | Bank(s) active |
| | MRW | Writing mode register | Bank(s) active |

Table 104: MRR/MRW Timing Constraints: DQ ODT is Disable

| From Command | To Command | Minimum Delay Between "From Command" and "To Command" | Unit | Notes |
|--------------------------------|-----------------|---|--------------|-------|
| MRR | MRR | t^{MRR} | – | |
| | RD/RDA | t^{MRR} | – | |
| | WR/WRA/MWR/MWRA | $RL + RU(t^{\text{DQSC}}(\text{MAX})/t^{\text{CK}}) + BL/2 - WL + t^{\text{WPRE}} + RD(t^{\text{RPST}})$ | $n\text{CK}$ | |
| | MRW | $RL + RU(t^{\text{DQSC}}(\text{MAX})/t^{\text{CK}}) + BL/2 + 3$ | $n\text{CK}$ | |
| RD/RDA | MRR | $BL/2$ | $n\text{CK}$ | |
| WR/WRA/MWR/MWRA | | $WL + 1 + BL/2 + RU(t^{\text{WTR}}/t^{\text{CK}})$ | $n\text{CK}$ | |
| MRW | | t^{MRD} | – | |
| POWER-DOWN EXIT | | $t^{\text{XP}} + t^{\text{MRRI}}$ | – | |
| MRW | RD/RDA | t^{MRD} | – | |
| | WR/WRA/MWR/MWRA | t^{MRD} | – | |
| | MRW | t^{MRW} | – | |
| RD/ RD-FIFO/ READ DQ CAL | MRW | $RL + BL/2 + RU(t^{\text{DQSC}}(\text{MAX})/t^{\text{CK}}) + RD(t^{\text{RPST}}) + \text{MAX}(RU(7.5\text{ns}/t^{\text{CK}}), 8n\text{CK})$ | $n\text{CK}$ | |
| RD with AUTO PRECHARGE | | $RL + BL/2 + RU(t^{\text{DQSC}}(\text{MAX})/t^{\text{CK}}) + RD(t^{\text{RPST}}) + \text{MAX}(RU(7.5\text{ns}/t^{\text{CK}}), 8n\text{CK}) + n\text{RTP} - 8$ | $n\text{CK}$ | |
| WR/ MWR/ WR-FIFO | | $WL + 1 + BL/2 + \text{MAX}(RU(7.5\text{ns}/t^{\text{CK}}), 8n\text{CK})$ | $n\text{CK}$ | |
| WR/MWR with AUTO PRE-CHARGE | | $WL + 1 + BL/2 + \text{MAX}(RU(7.5\text{ns}/t^{\text{CK}}), 8n\text{CK}) + n\text{WR}$ | $n\text{CK}$ | |


Table 105: MRR/MRW Timing Constraints: DQ ODT is Enable

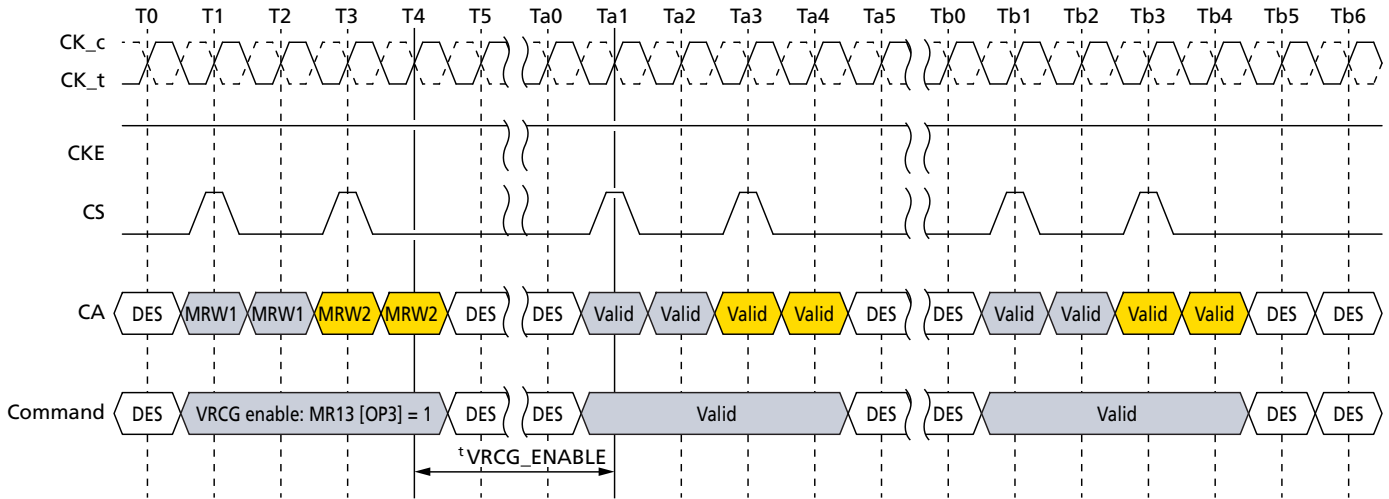
| From Command | To Command | Minimum Delay Between "From Command" and "To Command" | Unit | Notes |
|--------------------------------|-----------------|--|------|-------|
| MRR | MRR | t^{MRR} | – | |
| | RD/RDA | t^{MRR} | – | |
| | WR/WRA/MWR/MWRA | $RL + RU(t^{\text{DQ}}SCK(\text{MAX})/t^{\text{CK}}) + BL/2 - ODTL_{\text{on}} - RD(t^{\text{ODT}}_{\text{on}}(\text{MIN})/t^{\text{CK}}) + RD(t^{\text{RPST}}) + 1$ | nCK | |
| | MRW | $RL + RU(t^{\text{DQ}}SCK(\text{MAX})/t^{\text{CK}}) + BL/2 + 3$ | nCK | |
| RD/RDA | MRR | $BL/2$ | nCK | |
| WR/WRA/MWR/MWRA | | $WL + 1 + BL/2 + RU(t^{\text{WTR}}/t^{\text{CK}})$ | nCK | |
| MRW | | t^{MRD} | – | |
| POWER-DOWN EXIT | | $t^{\text{XP}} + t^{\text{MRR1}}$ | – | |
| MRW | RD/RDA | t^{MRD} | – | |
| | WR/WRA/MWR/MWRA | t^{MRD} | – | |
| | MRW | t^{MRW} | – | |
| RD/ RD-FIFO/ READ DQ CAL | MRW | $RL + BL/2 + RU(t^{\text{DQ}}SCK(\text{MAX})/t^{\text{CK}}) + RD(t^{\text{RPST}}) + \text{MAX}(RU(7.5\text{ns}/t^{\text{CK}}), 8n\text{CK})$ | nCK | |
| RD with AUTO PRECHARGE | | $RL + BL/2 + RU(t^{\text{DQ}}SCK(\text{MAX})/t^{\text{CK}}) + RD(t^{\text{RPST}}) + \text{MAX}(RU(7.5\text{ns}/t^{\text{CK}}), 8n\text{CK}) + n\text{RTP} - 8$ | nCK | |
| WR/ MWR/ WR-FIFO | | $WL + 1 + BL/2 + \text{MAX}(RU(7.5\text{ns}/t^{\text{CK}}), 8n\text{CK})$ | nCK | |
| WR/MWR with AUTO PRE-CHARGE | | $WL + 1 + BL/2 + \text{MAX}(RU(7.5\text{ns}/t^{\text{CK}}), 8n\text{CK}) + n\text{WR}$ | nCK | |

V_{REF} Current Generator (VRCG)

LPDDR4 SDRAM V_{REF} current generators (VRCG) incorporate a high current mode to reduce the settling time of the internal V_{REF(DQ)} and V_{REF(CA)} levels during training and when changing frequency set points during operation. The high current mode is enabled by setting MR13[OP3] = 1. Only DESELECT commands may be issued until $t^{\text{VRCG_ENABLE}}$ is satisfied. $t^{\text{VRCG_ENABLE}}$ timing is shown below.

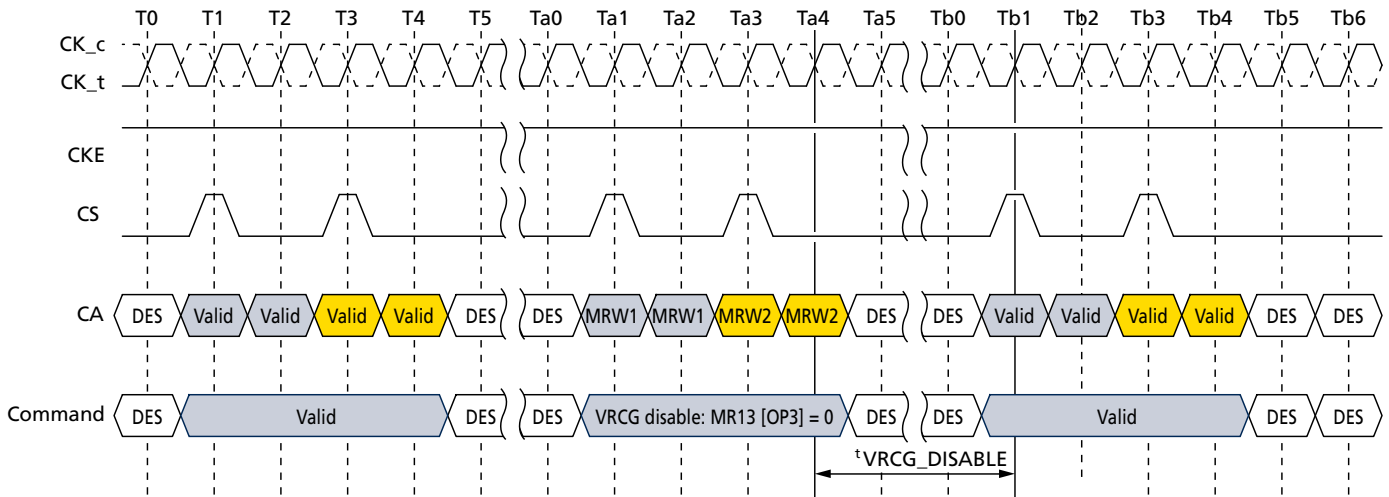


Figure 92: VRCG Enable Timing



VRCG high current mode is disabled by setting MR13[OP3] = 0. Only DESELECT commands may be issued until $t_{VRCG_DISABLE}$ is satisfied. $t_{VRCG_DISABLE}$ timing is shown below.

Figure 93: VRCG Disable Timing



Note that LPDDR4 SDRAM devices support $V_{FER(CA)}$ and $V_{REF(DQ)}$ range and value changes without enabling VRCG high current mode.

Table 106: VRCG Enable/Disable Timing

| Parameter | Symbol | Min | Max | Unit |
|---|---------------------|-----|-----|------|
| V _{REF} high current mode enable time | t_{VRCG_ENABLE} | – | 200 | ns |
| V _{REF} high current mode disable time | $t_{VRCG_DISABLE}$ | – | 100 | ns |



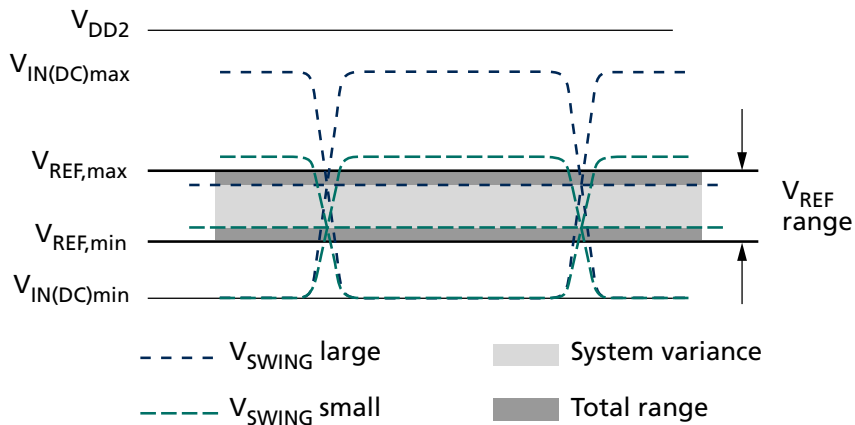
V_{REF} Training

V_{REF(CA)} Training

The device's internal V_{REF(CA)} specification parameters are operating voltage range, step size, V_{REF} step time, V_{REF} full-range step time, and V_{REF} valid level.

The voltage operating range specifies the minimum required V_{REF} setting range for LPDDR4 devices. The minimum range is defined by V_{REF,max} and V_{REF,min}.

Figure 94: V_{REF} Operating Range (V_{REF,max}, V_{REF,min})

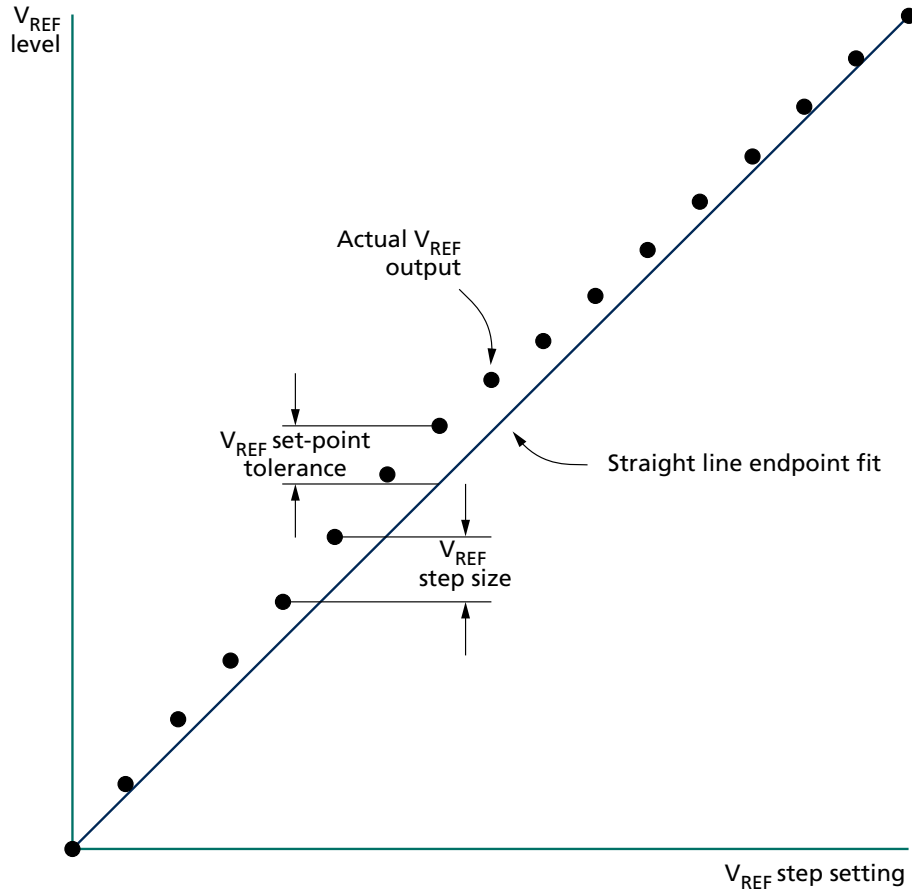


The V_{REF} step size is defined as the step size between adjacent steps. However, for a given design, the device has one value for V_{REF} step size that falls within the given range.

The V_{REF} set tolerance is the variation in the V_{REF} voltage from the ideal setting. This accounts for accumulated error over multiple steps. There are two ranges for V_{REF} set tolerance uncertainty. The range of V_{REF} set tolerance uncertainty is a function of the number of steps *n*.

The V_{REF} set tolerance is measured with respect to the ideal line that is based on the two endpoints, where the endpoints are at the minimum and maximum V_{REF} values for a specified range.

Figure 95: V_{REF} Set-Point Tolerance and Step Size



The V_{REF} increment/decrement step times are defined by ^tV_{REF}_TIME-SHORT, ^tV_{REF}_TIME-MIDDLE, and ^tV_{REF}_TIME-LONG. The parameters are defined from TS to TE as shown below, where TE is referenced to when the V_{REF} voltage is at the final DC level within the V_{REF} valid tolerance (V_{REF, val_tol}).

The V_{REF} valid level is defined by V_{REF, val_tol} to qualify the step time TE (see the following figures). This parameter is used to ensure an adequate RC time constant behavior of the voltage level change after any V_{REF} increment/decrement adjustment. This parameter is only applicable for LPDDR4 component level validation/characterization.

^tV_{REF}_TIME-SHORT is for a single step size increment/decrement change in the V_{REF} voltage.

^tV_{REF}_TIME-MIDDLE is at least two stepsizes increment/decrement change within the same V_{REF(CA)} range in V_{REF} voltage.

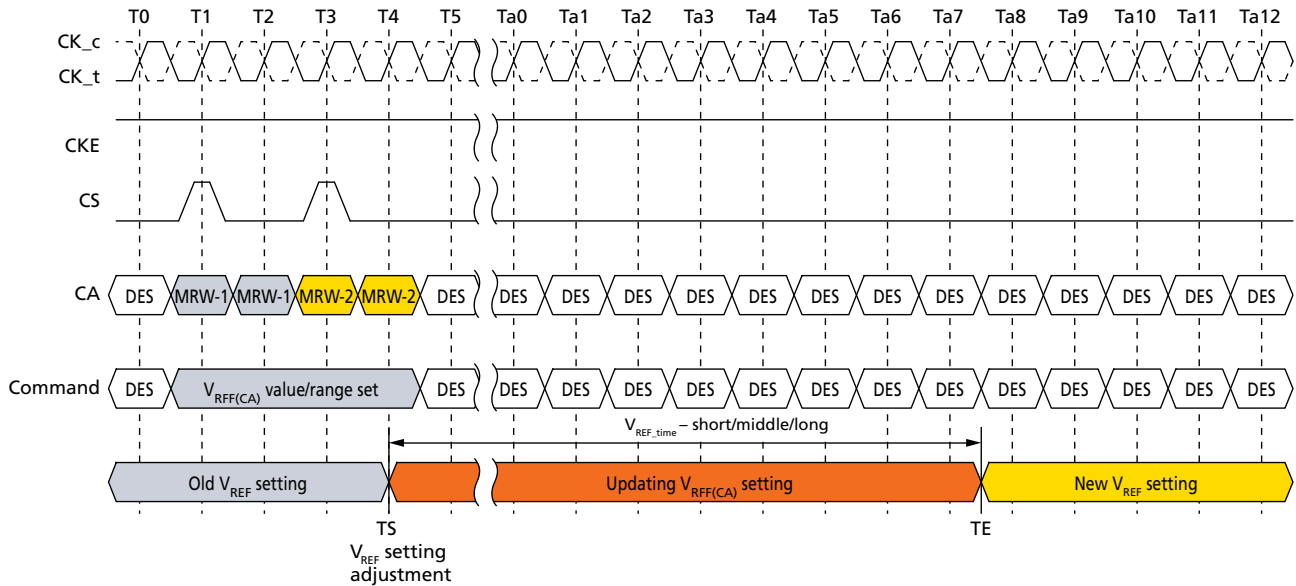
^tV_{REF}_TIME-LONG is the time including up to V_{REF, min} to V_{REF, max} or V_{REF, max} to V_{REF, min} change across the V_{REF(CA)} range in V_{REF} voltage.

TS is referenced to MRW command clock.

TE is referenced to V_{REF, val_tol}.



Figure 96: $t_{V_{ref}}$ for Short, Middle, and Long Timing Diagram



The MRW command to the mode register bits are as follows;

MR12 OP[5:0] : V_{REF(CA)} Setting

MR12 OP[6] : V_{REF(CA)} Range

The minimum time required between two V_{REF} MRW commands is $t_{V_{REF_TIME_SHORT}}$ for a single step and $t_{V_{REF_TIME_MIDDLE}}$ for a full voltage range step.

Figure 97: V_{REF(CA)} Single-Step Increment

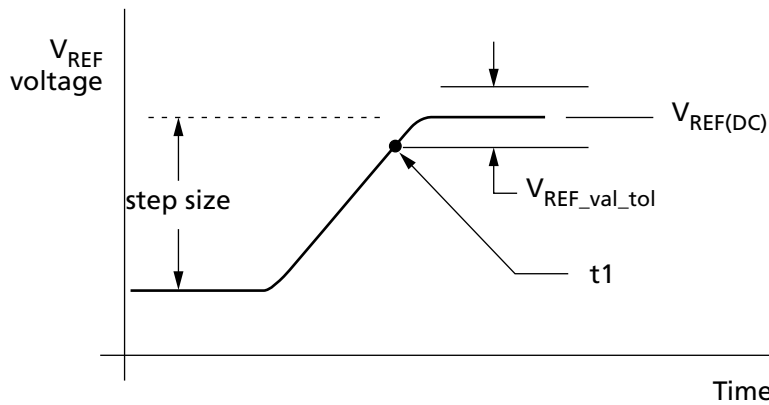




Figure 98: V_{REF(CA)} Single-Step Decrement

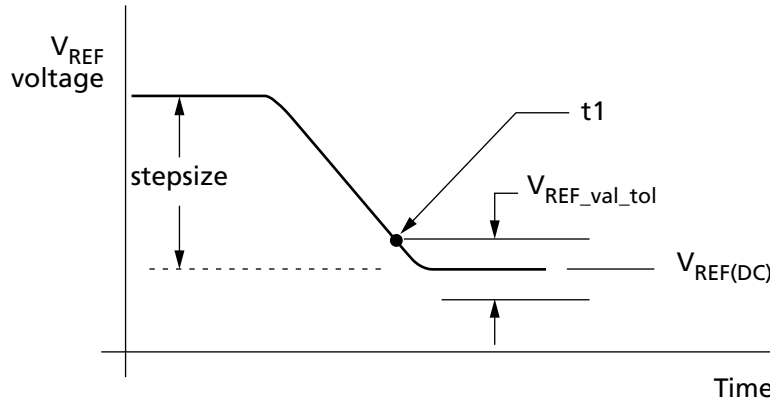


Figure 99: V_{REF(CA)} Full Step from V_{REF,min} to V_{REF,max}

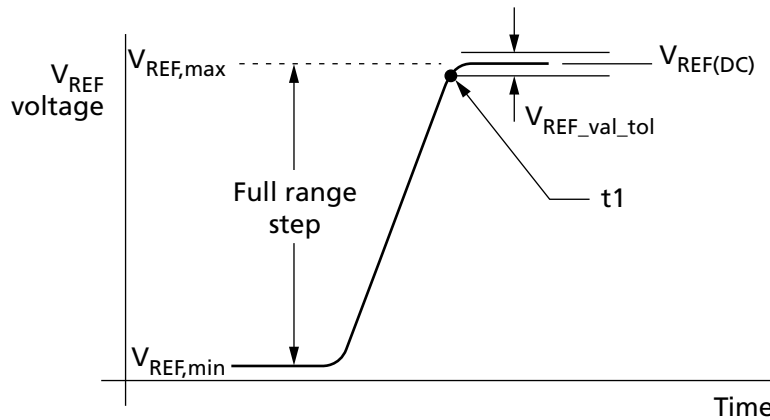
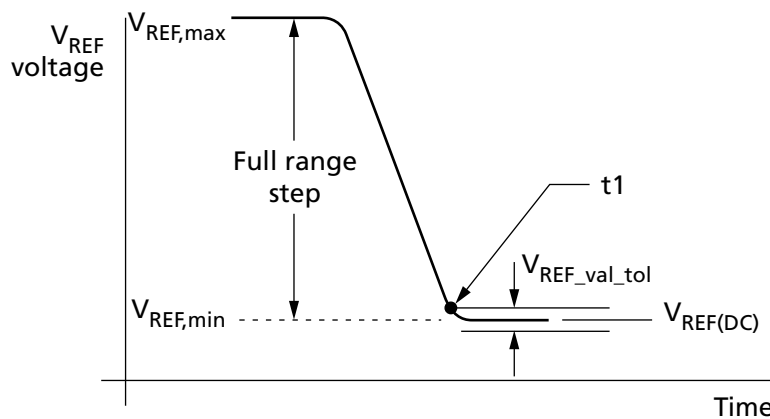


Figure 100: V_{REF(CA)} Full Step from V_{REF,max} to V_{REF,min}



The following table contains the CA internal V_{REF} specification that will be characterized at the component level for compliance.


Table 107: Internal V_{REF(CA)} Specifications

| Symbol | Parameter | Min | Typ | Max | Unit | Notes |
|-------------------------------|--|--------|-------|-------|------------------|---------|
| V _{REF(CA),max_r0} | V _{REF(CA)} range-0 MAX operating point | – | – | 30% | V _{DD2} | 1, 11 |
| V _{REF(CA),min_r0} | V _{REF(CA)} range-0 MIN operating point | 10% | – | – | V _{DD2} | 1, 11 |
| V _{REF(CA),max_r1} | V _{REF(CA)} range-1 MAX operating point | – | – | 42% | V _{DD2} | 1, 11 |
| V _{REF(CA),min_r1} | V _{REF(CA)} range-1 MIN operating point | 22% | – | – | V _{DD2} | 1, 11 |
| V _{REF(CA),step} | V _{REF(CA)} step size | 0.30% | 0.40% | 0.50% | V _{DD2} | 2 |
| V _{REF(CA),set_tol} | V _{REF(CA)} set tolerance | –1.00% | 0.00% | 1.00% | V _{DD2} | 3, 4, 6 |
| | | –0.10% | 0.00% | 0.10% | V _{DD2} | 3, 5, 7 |
| t _{VREF_TIME-SHORT} | V _{REF(CA)} step time | – | – | 100 | ns | 8 |
| t _{VREF_TIME-MIDDLE} | | – | – | 200 | ns | 12 |
| t _{VREF_TIME-LONG} | | – | – | 250 | ns | 9 |
| t _{VREF_time_weak} | | – | – | 1 | ms | 13, 14 |
| V _{REF(CA)_val_tol} | V _{REF(CA)} valid tolerance | –0.10% | 0.00% | 0.10% | V _{DD2} | 10 |

- Notes:
1. V_{REF(CA)} DC voltage referenced to V_{DD2(DC)}.
 2. V_{REF(CA)} step size increment/decrement range. V_{REF(CA)} at DC level.
 3. $V_{REF(CA),new} = V_{REF(CA),old} + n \times V_{REF(CA),step}$; n = number of steps; if increment, use "+"; if decrement, use "-".
 4. The minimum value of V_{REF(CA)} setting tolerance = $V_{REF(CA),new} - 1.0\% \times V_{DD2}$. The maximum value of V_{REF(CA)} setting tolerance = $V_{REF(CA),new} + 1.0\% \times V_{DD2}$. For n > 4.
 5. The minimum value of V_{REF(CA)} setting tolerance = $V_{REF(CA),new} - 0.10\% \times V_{DD2}$. The maximum value of V_{REF(CA)} setting tolerance = $V_{REF(CA),new} + 0.10\% \times V_{DD2}$. For n < 4.
 6. Measured by recording the minimum and maximum values of the V_{REF(CA)} output over the range, drawing a straight line between those points and comparing all other V_{REF(CA)} output settings to that line.
 7. Measured by recording the minimum and maximum values of the V_{REF(CA)} output across four consecutive steps (n = 4), drawing a straight line between those points and comparing all other V_{REF(CA)} output settings to that line.
 8. Time from MRW command to increment or decrement one step size for V_{REF(CA)}.
 9. Time from MRW command to increment or decrement V_{REF,min} to V_{REF,max} or V_{REF,max} to V_{REF,min} change across the V_{REF(CA)} range in V_{REF} voltage.
 10. Only applicable for DRAM component level test/characterization purposes. Not applicable for normal mode of operation. V_{REF} valid is to qualify the step times which will be characterized at the component level.
 11. DRAM range-0 or range-1 set by MR12 OP[6].
 12. Time from MRW command to increment or decrement more than one step size up to a full range of V_{REF} voltage within the same V_{REF(CA)} range.
 13. Applies when VRCG high current mode is not enabled, specified by MR13 [OP3] = 0b.
 14. t_{VREF_time_weak} covers all V_{REF(CA)} range and value change conditions are applied to t_{VREF_TIME-SHORT/MIDDLE/LONG}.

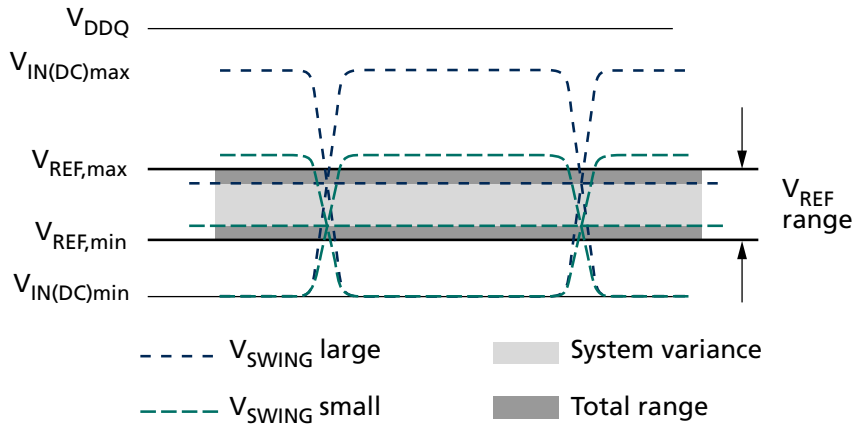


V_{REF(DQ)} Training

The device's internal V_{REF(DQ)} specification parameters are operating voltage range, step size, V_{REF} step tolerance, V_{REF} step time and V_{REF} valid level.

The voltage operating range specifies the minimum required V_{REF} setting range for LPDDR4 devices. The minimum range is defined by V_{REF,max} and V_{REF,min}.

Figure 101: V_{REF} Operating Range (V_{REF,max}, V_{REF,min})

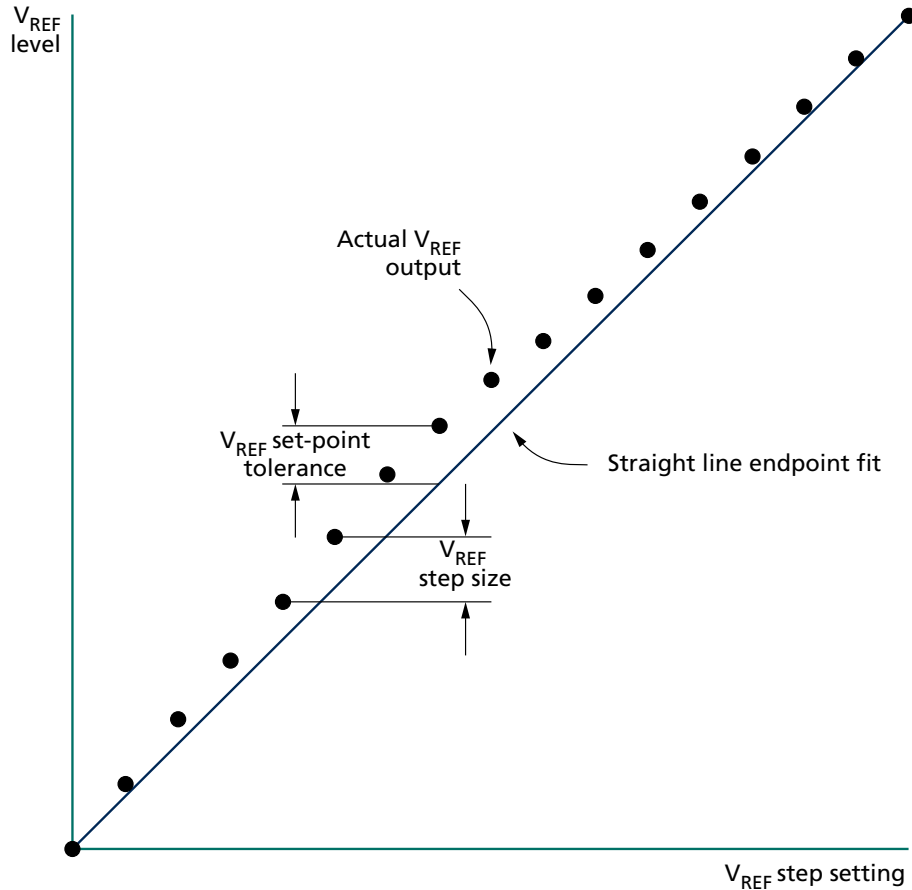


The V_{REF} step size is defined as the step size between adjacent steps. However, for a given design, the device has one value for V_{REF} step size that falls within the given range.

The V_{REF} set tolerance is the variation in the V_{REF} voltage from the ideal setting. This accounts for accumulated error over multiple steps. There are two ranges for V_{REF} set tolerance uncertainty. The range of V_{REF} set tolerance uncertainty is a function of the number of steps *n*.

The V_{REF} set tolerance is measured with respect to the ideal line that is based on the two endpoints, where the endpoints are at the minimum and maximum V_{REF} values for a specified range.

Figure 102: V_{REF} Set Tolerance and Step Size



The V_{REF} increment/decrement step times are defined by ^tV_{REF}_TIME-SHORT, ^tV_{REF}_TIME-MIDDLE and ^tV_{REF}_TIME-LONG. The ^tV_{REF}_TIME-SHORT, ^tV_{REF}_TIME-MIDDLE and ^tV_{REF}_TIME-LONG times are defined from TS to TE in the following figure where TE is referenced to when the V_{REF} voltage is at the final DC level within the V_{REF} valid tolerance (V_{REFVAL_TOL}).

The V_{REF} valid level is defined by V_{REFVAL_TOL} to qualify the step time TE (see the figure below). This parameter is used to ensure an adequate RC time constant behavior of the voltage level change after any V_{REF} increment/decrement adjustment. This parameter is only applicable for DRAM component level validation/characterization.

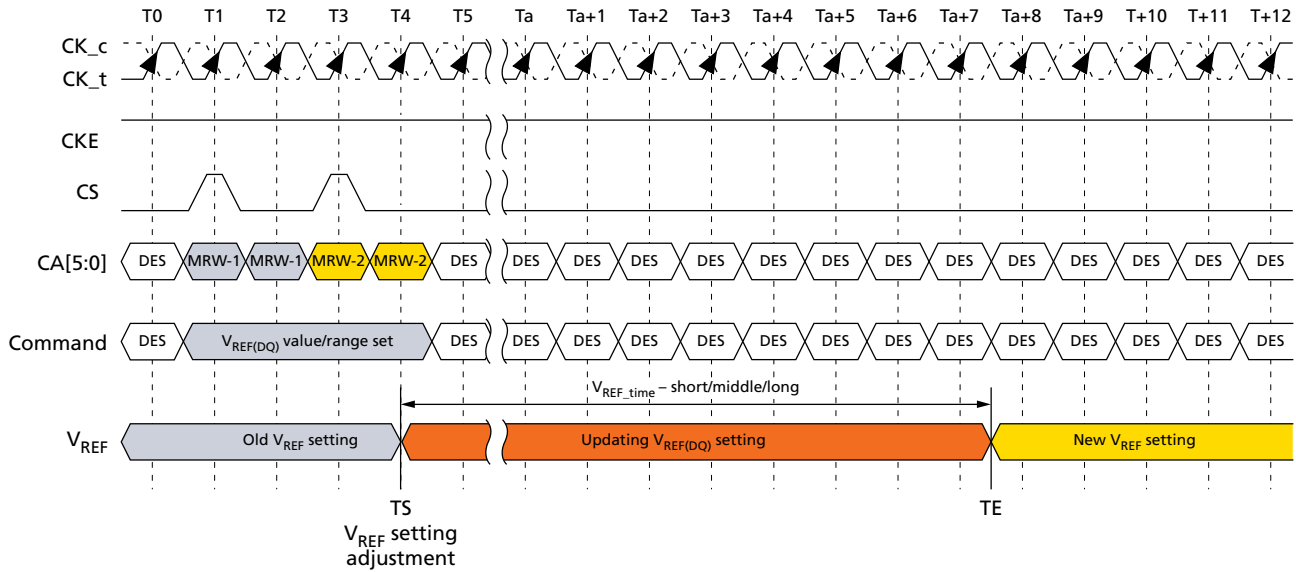
^tV_{REF}_TIME-SHORT is for a single step size increment/decrement change in the V_{REF} voltage.

^tV_{REF}_TIME-MIDDLE is at least two step sizes of increment/decrement change in the V_{REF(DQ)} range in the V_{REF} voltage.

^tV_{REF}_TIME-LONG is the time including and up to the full range of V_{REF} (MIN to MAX or MAX to MIN) across the V_{REF(DQ)} range in V_{REF} voltage.



Figure 103: V_{REF(DQ)} Transition Time for Short, Middle, or Long Changes



- Notes: 1. TS is referenced to MRW command clock.
2. TE is referenced to V_{REF,VAL_TOL}.

The MRW command to the mode register bits are defined as:

MR14 OP[5:0]: V_{REF(DQ)} setting

MR14 OP[6]: V_{REF(DQ)} range

The minimum time required between two V_{REF} MRW commands is ^tV_{REF_TIME-SHORT} for a single step and ^tV_{REF_TIME-MIDDLE} for a full voltage range step.

Figure 104: V_{REF(DQ)} Single-Step Size Increment

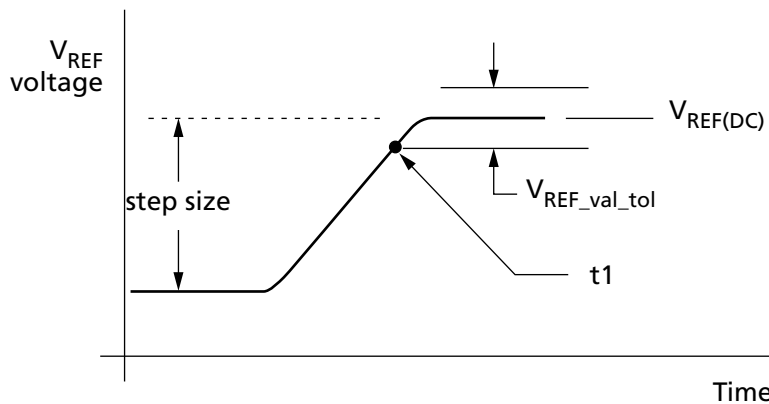




Figure 105: V_{REF(DQ)} Single-Step Size Decrement

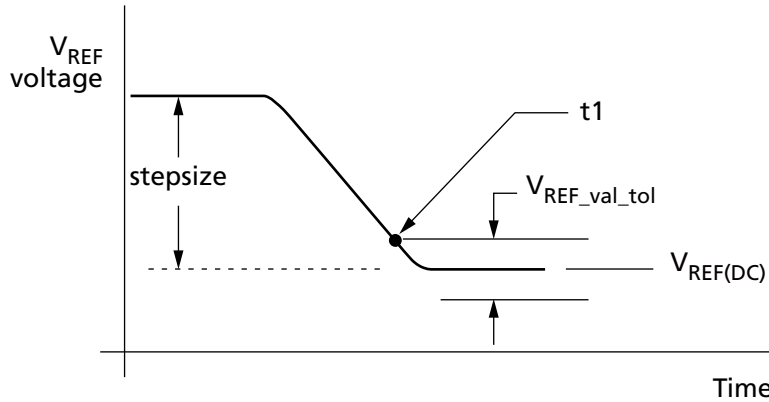


Figure 106: V_{REF(DQ)} Full Step from V_{REF,min} to V_{REF,max}

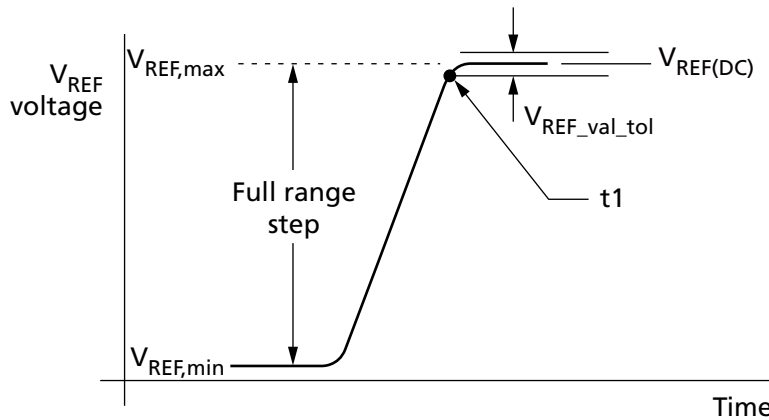
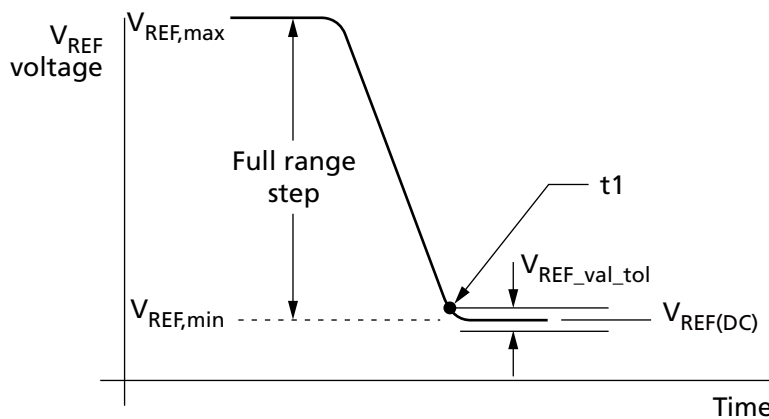


Figure 107: V_{REF(DQ)} Full Step from V_{REF,max} to V_{REF,min}



The following table contains the DQ internal V_{REF} specification that will be characterized at the component level for compliance.


Table 108: Internal V_{REF(DQ)} Specifications

| Symbol | Parameter | Min | Typ | Max | Unit | Notes |
|--|--|--------|-------|-------|------------------|---------|
| V _{REF(DQ),max_r0} | V _{REF} MAX operating point Range-0 | – | – | 30% | V _{DDQ} | 1, 11 |
| V _{REF(DQ),min_r0} | V _{REF} MIN operating point Range-0 | 10% | – | – | V _{DDQ} | 1, 11 |
| V _{REF(DQ),max_r1} | V _{REF} MAX operating point Range-1 | – | – | 42% | V _{DDQ} | 1, 11 |
| V _{REF(DQ),min_r1} | V _{REF} MIN operating point Range-1 | 22% | – | – | V _{DDQ} | 1, 11 |
| V _{REF(DQ),step} | V _{REF(DQ)} step size | 0.30% | 0.40% | 0.50% | V _{DDQ} | 2 |
| V _{REF(DQ),set_tol} | V _{REF(DQ)} set tolerance | –1.00% | 0.00% | 1.00% | V _{DDQ} | 3, 4, 6 |
| | | –0.10% | 0.00% | 0.10% | V _{DDQ} | 3, 5, 7 |
| t _{V_{REF}_TIME-SHORT} | V _{REF(DQ)} step time | – | – | 100 | ns | 8 |
| t _{V_{REF}_TIME-MIDDLE} | | – | – | 200 | ns | 12 |
| t _{V_{REF}_TIME-LONG} | | – | – | 250 | ns | 9 |
| t _{V_{REF}_time_weak} | | – | – | 1 | ms | 13, 14 |
| V _{REF(DQ),val_tol} | V _{REF(DQ)} valid tolerance | –0.10% | 0.00% | 0.10% | V _{DDQ} | 10 |

- Notes:
1. V_{REF(DQ)} DC voltage referenced to V_{DDQ(DC)}.
 2. V_{REF(DQ)} step size increment/decrement range. V_{REF(DQ)} at DC level.
 3. $V_{REF(DQ),new} = V_{REF(DQ),old} + n \times V_{REF(DQ),step}$; n = number of steps; if increment, use "+"; if decrement, use "-".
 4. The minimum value of V_{REF(DQ)} setting tolerance = $V_{REF(DQ),new} - 1.0\% \times V_{DDQ}$. The maximum value of V_{REF(DQ)} setting tolerance = $V_{REF(DQ),new} + 1.0\% \times V_{DDQ}$. For n > 4.
 5. The minimum value of V_{REF(DQ)} setting tolerance = $V_{REF(DQ),new} - 0.10\% \times V_{DDQ}$. The maximum value of V_{REF(DQ)} setting tolerance = $V_{REF(DQ),new} + 0.10\% \times V_{DDQ}$. For n < 4.
 6. Measured by recording the minimum and maximum values of the V_{REF(DQ)} output over the range, drawing a straight line between those points and comparing all other V_{REF(DQ)} output settings to that line.
 7. Measured by recording the minimum and maximum values of the V_{REF(DQ)} output across four consecutive steps (n = 4), drawing a straight line between those points and comparing all other V_{REF(DQ)} output settings to that line.
 8. Time from MRW command to increment or decrement one step size for V_{REF(DQ)}.
 9. Time from MRW command to increment or decrement V_{REF,min} to V_{REF,max} or V_{REF,max} to V_{REF,min} change across the V_{REF(DQ)} Range in V_{REF(DQ)} Voltage.
 10. Only applicable for DRAM component level test/characterization purposes. Not applicable for normal mode of operation. V_{REF} valid is to qualify the step times which will be characterized at the component level.
 11. DRAM range-0 or range-1 set by MR14 OP[6].
 12. Time from MRW command to increment or decrement more than one step size up to a full range of V_{REF} voltage within the same V_{REF(DQ)} range.
 13. Applies when VRCG high current mode is not enabled, specified by MR13 [OP3] = 0.
 14. t_{V_{REF}_time_weak} covers all V_{REF(DQ)} Range and Value change conditions are applied to t_{V_{REF}_TIME-SHOR/MIDDLE/LONG}.



Command Bus Training

Command Bus Training Mode

The command bus must be trained before enabling termination for high-frequency operation. The device provides an internal $V_{REF(CA)}$ that defaults to a level suitable for un-terminated, low-frequency operation, but the $V_{REF(CA)}$ must be trained to achieve suitable receiver voltage margin for terminated, high-frequency operation.

The training mode described here centers the internal $V_{REF(CA)}$ in the CA data eye and at the same time allows for timing adjustments of the CS and CA signals to meet setup/hold requirements. Because it can be difficult to capture commands prior to training the CA inputs, the training mode described here uses a minimum of external commands to enter, train, and exit the CA bus training mode.

The die has a bond-pad (ODT_CA) to control the command bus termination for multi-rank operation. Other mode register bits are provided to fine tune termination control in a variety of system configuration. See On-Die Termination for more information.

The device uses frequency set points to enable multiple operating settings for the die. The device defaults to FSP-OP[0] at power-up, which has the default settings to operate in un-terminated, low-frequency environments. Prior to training, the termination should be enabled for one die in each channel by setting MR13 OP[6] = 1b (FSP-WR[1]) and setting all other mode register bits for FSP-OP[1] to the desired settings for high-frequency operation. Upon training entry, the device will automatically switch to FSP-OP[1] and use the high-frequency settings during training (See the Command Bus Training Entry Timing figure for more information on FSP-OP register sets). Upon training exit, the device will automatically switch back to FSP-OP[0], returning to a "known-good" state for un-terminated, low-frequency operation.

To enter command bus training mode, issue a MRW-1 command followed by a MRW-2 command to set MR13 OP[0] = 1b (command bus training mode enabled).

After time t_{MRD} , CKE may be set LOW, causing the device to switch to FSP-OP[1], and completing the entry into command bus training mode.

A status DQS_t, DQS_c, DQ, and DMI are as noted below; the DQ ODT state will be followed by FREQUENCY SET POINT function except in the case of output pins.

- DQS_t[0], DQS_c[0] become input pins for capturing DQ[6:0] levels by toggling.
- DQ[5:0] become input pins for setting $V_{REF(CA)}$ level.
- DQ[6] becomes an input pin for setting $V_{REF(CA)}$ range.
- DQ[7] and DMI[0] become input pins, and their input level is valid or floating.
- DQ[13:8] become output pins to feedback, capturing value via the command bus using the CS signal.
- DQS_t[1], DQS_c[1], DMI[1], and DQ[15:14] become output pins or are disabled, meaning the device may be driven to a valid level or may be left floating.

At time t_{CAENT} later, the device may change its $V_{REF(CA)}$ range and value using input signals DQS_t[0], DQS_c[0], and DQ[6:0] from existing value that is set via MR12 OP[6:0]. The mapping between MR12 OP code and DQs is shown below. At least one $V_{REF(CA)}$ setting is required before proceeding to the next training step.


Table 109: Mapping MR12 Op Code and DQ Numbers

| | Mapping | | | | | | |
|--------------|---------|-----|-----|-----|-----|-----|-----|
| MR12 OP code | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
| DQ number | DQ6 | DQ5 | DQ4 | DQ3 | DQ2 | DQ1 | DQ0 |

The new $V_{REF(CA)}$ value must "settle" for time t_{VREFCA_Long} before attempting to latch CA information.

Note: If DQ ODT is enabled in MR11-OP[2:0], then the SDRAM will terminate the DQ lanes during command bus training when entering $V_{REF(CA)}$ range and values on DQ[6:0].

To verify that the receiver has the correct $V_{REF(CA)}$ setting, and to further train the CA eye relative to clock (CK), values latched at the receiver on the CA bus are asynchronously output to the DQ bus.

To exit command bus training mode, drive CKE HIGH, and after time t_{VREFCA_Long} , issue the MRW-1 command followed by the MRW-2 command to set MR13 OP[0] = 0b. After time t_{MRW} , the device is ready for normal operation. After training exit, the device will automatically switch back to the FSP-OP registers that were in use prior to training.

Command bus training (CBT) may be executed from the idle or self refresh state. When executing CBT within the self refresh state, the device must not be in a power-down state (for example, CKE must be HIGH prior to training entry). CBT entry and exit is the same, regardless of the state from which CBT is initiated.

Training Sequence for Single-Rank Systems

The sequence example shown here assumes an initial low-frequency, non-terminating operating point training a high-frequency, terminating operating point. The **bold text** shows high-frequency instructions. Any operating point may be trained from any known good operating point.

1. Set MR13 OP[6] = 1b to enable writing to frequency set point 1 (FSP-WR[1]) (or FSP-OP[0]).
2. Write FSP-WR[1] (or FSP-WR[0]) registers for all channels to set up high-frequency operating parameters.
3. Issue MRW-1 and MRW-2 commands to enter command bus training mode.
4. Drive CKE LOW, **and change CK frequency to the high-frequency operating point.**
5. **Perform command bus training ($V_{REF(CA)}$, CS, and CA).**
6. **Exit training by driving CKE HIGH**, change CK frequency to the low-frequency operating point, and issue MRW-1 and MRW-2 commands. When CKE is driven HIGH, the device will automatically switch back to the FSP-OP registers that were in use prior to training (trained values are not retained).
7. Write the trained values to FSP-WR[1] (or FSP-WR[0]) by issuing MRW-1 and MRW-2 commands to the SDRAM and setting all applicable mode register parameters.
8. Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[1] (or FSP-OP[0]), to turn on termination, **and change CK frequency to the high-frequency operating point. At this point the command bus is trained and you may proceed to other training or normal operation.**



Training Sequence for Multiple-Rank Systems

The sequence example shown here is assuming an initial low-frequency operating point, training a high-frequency operating point. The **bold text** shows high-frequency instructions. Any operating point may be trained from any known good operating point.

1. Set MR13 OP[6] = 1b to enable writing to frequency set point 1 (FSP-WR[1]) (or FSP-WR[0]).
2. Write FSP-WR[1] (or FSP-WR[0]) registers for all channels and ranks to set up high-frequency operating parameters.
3. Read MR0 OP[7] on all channels and ranks to determine which die are terminating, signified by MR0 OP[7] = 1b.
4. Issue MRW-1 and MRW-2 commands to enter command bus training mode on the terminating rank.
5. Drive CKE LOW on the terminating rank (or all ranks), **and change CK frequency to the high-frequency operating point.**
6. **Perform command bus training on the terminating rank ($V_{REF(CA)}$, CS, and CA).**
7. **Exit training by driving CKE HIGH**, change CK frequency to the low-frequency operating point, and issue MRW-1 and MRW-2 commands to write the trained values to FSP-WR[1] (or FSP-WR[0]). When CKE is driven HIGH, the SDRAM will automatically switch back to the FSP-OP registers that were in use prior to training (trained values are not retained by the device).
8. Issue MRW-1 and MRW-2 commands to enter training mode on the non-terminating rank (but keep CKE HIGH).
9. Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[1] (or FSP-OP[0]), to turn on termination, **and change CK frequency to the high-frequency operating point.**
10. **Drive CKE LOW on the non-terminating (or all) ranks. The non-terminating rank(s) will now be using FSP-OP[1] (or FSP-OP[0]).**
11. **Perform command bus training on the non-terminating rank ($V_{REF(CA)}$, CS, and CA).**
12. **Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[0] (or FSP-OP[1]) to turn off termination.**
13. **Exit training by driving CKE HIGH on the non-terminating rank**, change CK frequency to the low-frequency operating point, and issue MRW-1 and MRW-2 commands. When CKE is driven HIGH, the device will automatically switch back to the FSP-OP registers that were in use prior to training (that is, trained values are not retained by the device).
14. Write the trained values to FSP-WR[1] (or FSP-WR[0]) by issuing MRW-1 and MRW-2 commands and setting all applicable mode register parameters.
15. Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[1] (or FSP-OP[0]), to turn on termination, **and change CK frequency to the high-frequency operating point. At this point the command bus is trained for both ranks and the user may proceed to other training or normal operation.**

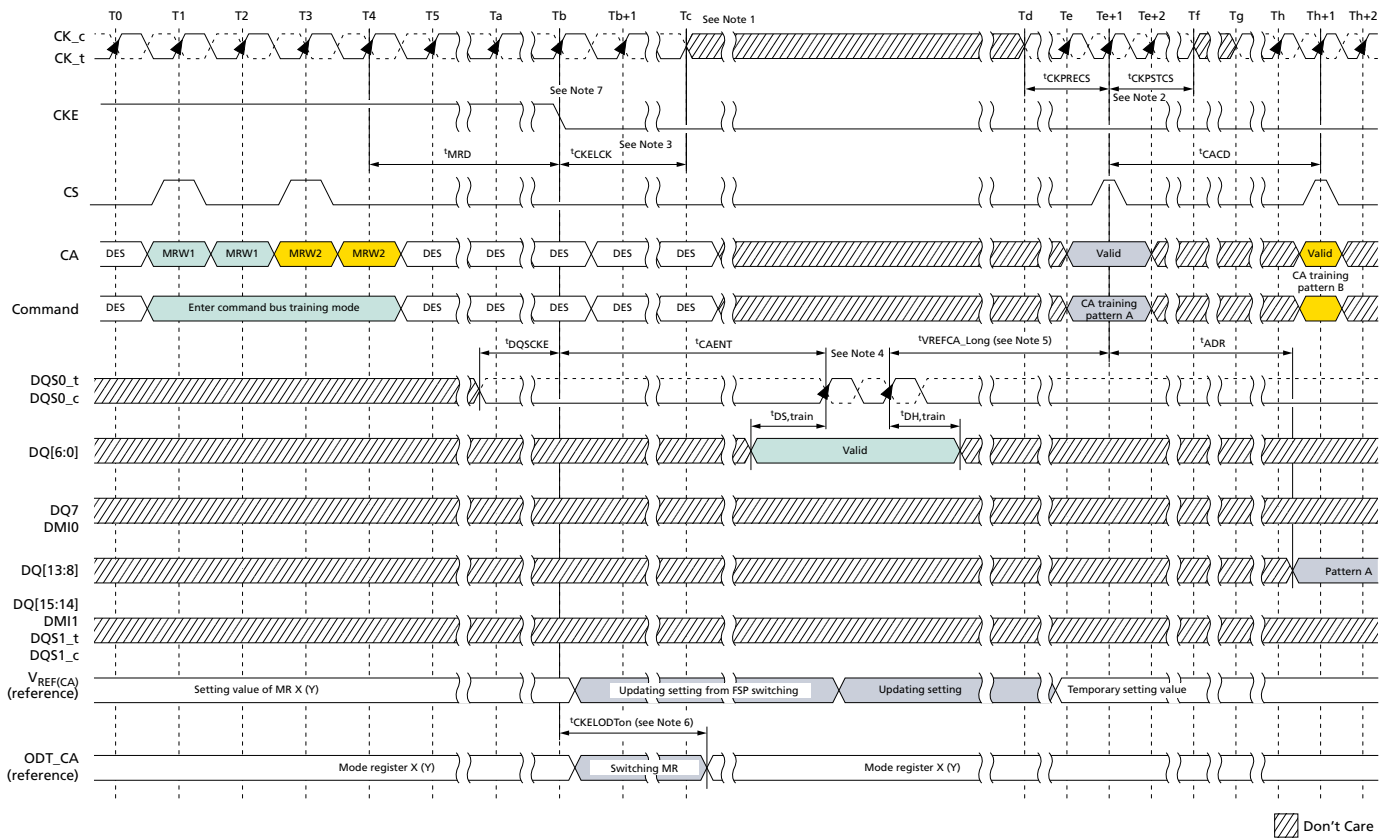


Relation Between CA Input Pin and DQ Output Pin

Table 110: Mapping of CA Input Pin and DQ Output Pin

| | Mapping | | | | | |
|-----------|---------|------|------|------|-----|-----|
| CA number | CA5 | CA4 | CA3 | CA2 | CA1 | CA0 |
| DQ number | DQ13 | DQ12 | DQ11 | DQ10 | DQ9 | DQ8 |

Figure 108: Command Bus Training Mode Entry – CA Training Pattern I/O with V_{REF(CA)} Value Update

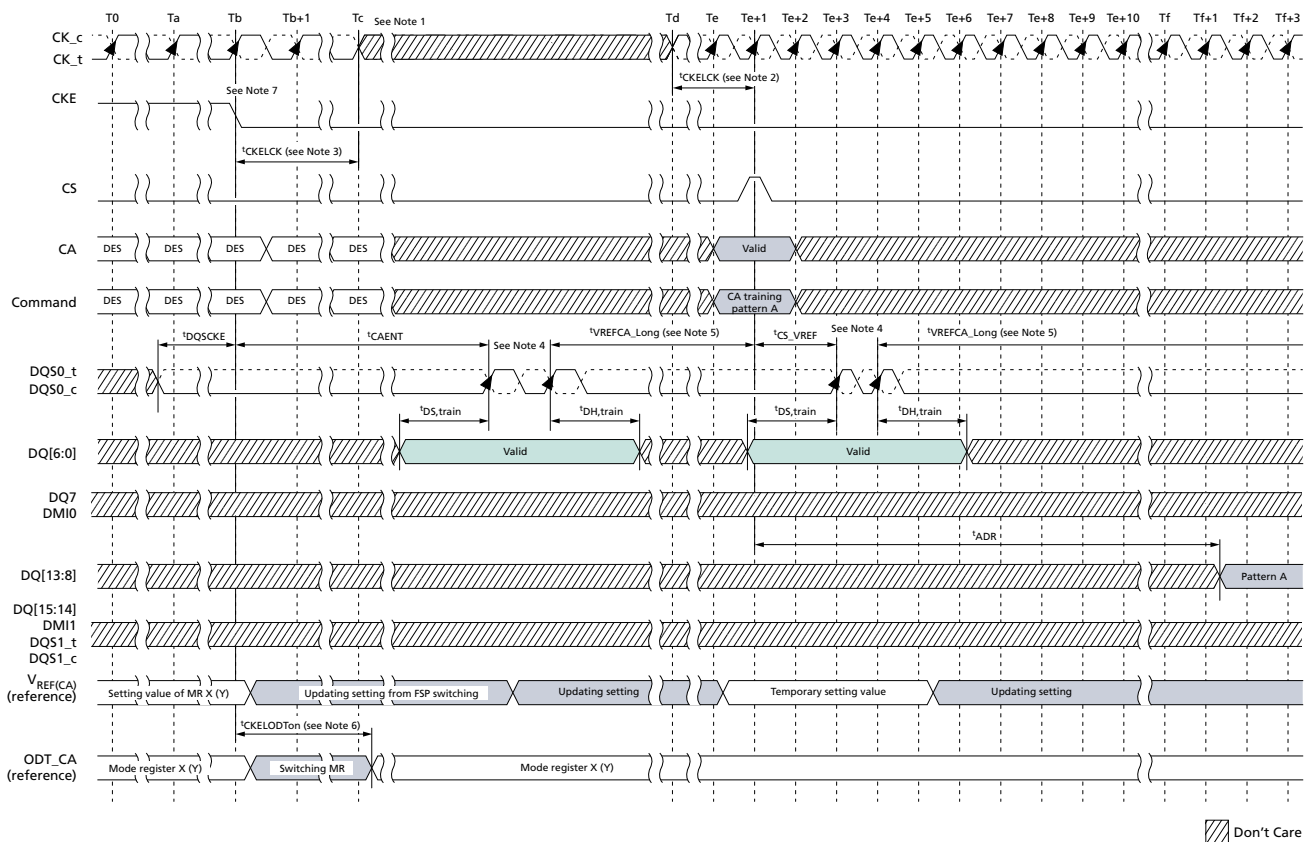


- Notes:
1. After ^tCKELCK, the clock can be stopped or the frequency changed any time.
 2. The input clock condition should be satisfied ^tCKPRECS and ^tCKPSTCS.
 3. Continue to drive CK, and hold CA and CS LOW, until ^tCKELCK after CKE is LOW (which disables command decoding).
 4. The device may or may not capture the first rising edge of DQS_t/DQS_c due to an unstable first rising edge. Therefore, at least two consecutive pulses of DQS signal input is required every for DQS input signal while capturing DQ[6:0] signals. The captured value of the DQ[6:0] signal level by each DQS edge may be overwritten at any time and the device will temporarily update the V_{REF(CA)} setting of MR12 after time ^tVREFCA_Long.
 5. ^tVREFCA_Long may be reduced to ^tVREFCA_Short if the following conditions are met: 1) The new V_{REF} setting is a single step above or below the old V_{REF} setting; 2) The DQS pulses a single time, or the new V_{REF} setting value on DQ[6:0] is static and meets ^tDS,train/^tDH,train for every DQS pulse applied.



- When CKE is driven LOW, the device will switch its FSP-OP registers to use the alternate (non-active) set. For example, if the device is currently using FSP-OP[0], then it will switch to FSP-OP[1] when CKE is driven LOW. All operating parameters should be written to the alternate mode registers before entering command bus training to ensure that ODT settings, RL/WL/nWR setting, and so forth, are set to the correct values. If the alternate FSP-OP has ODT_CA disabled, then termination will not be enabled in command bus training mode. If the ODT_CA pad is bonded to V_{SS} or floating, ODT_CA termination will never enable for that die.
- When CKE is driven LOW in command bus training mode, the device will change operation to the alternate FSP, that is, the inverse of the FSP programmed in the FSP-OP mode register.

Figure 109: Consecutive V_{REF(CA)} Value Update

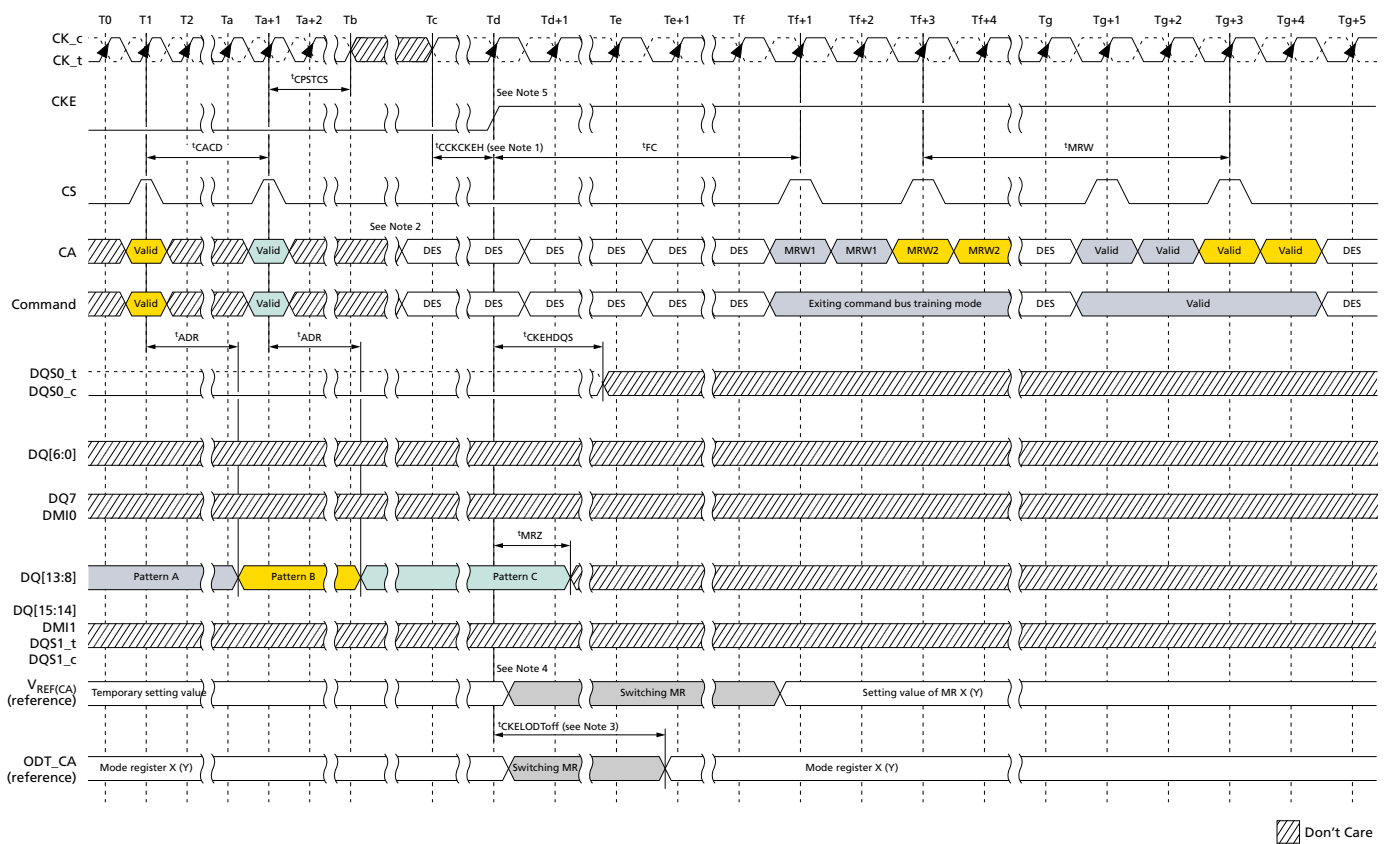


- Notes:
- After t_{CKELCK}, the clock can be stopped or the frequency changed any time.
 - The input clock condition should be satisfied t_{CKPRECS} and t_{CKPSTCS}.
 - Continue to drive CK, and hold CA and CS LOW, until t_{CKELCK} after CKE is LOW (which disables command decoding).
 - The device may or may not capture the first rising edge of DQS_t/DQS_c due to an unstable first rising edge. Therefore, at least two consecutive pulses of DQS signal input is required every for DQS input signal while capturing DQ[6:0] signals. The captured value of the DQ[6:0] signal level by each DQS edge may be overwritten at any time and the device will temporarily update the V_{REF(CA)} setting of MR12 after time t_{VREFCA_Long}.
 - t_{VREFCA_Long} may be reduced to t_{VREFCA_Short} if the following conditions are met: 1) The new V_{REF} setting is a single step above or below the old V_{REF} setting; 2) The DQS



- pulses a single time, or the new V_{REF} setting value on DQ[6:0] is static and meets $t_{DS,train} / t_{DH,train}$ for every DQS pulse applied.
- When CKE is driven LOW, the device will switch its FSP-OP registers to use the alternate (non-active) set. For example, if the device is currently using FSP-OP[0], then it will switch to FSP-OP[1] when CKE is driven LOW. All operating parameters should be written to the alternate mode registers before entering command bus training to ensure that ODT settings, RL/WL/nWR setting, and so forth, are set to the correct values. If the alternate FSP-OP has ODT_CA disabled, then termination will not be enabled in command bus training mode. If the ODT_CA pad is bonded to V_{SS} or floating, ODT_CA termination will never enable for that die.
 - When CKE is driven LOW in command bus training mode, the device will change operation to the alternate FSP, that is, the inverse of the FSP programmed in the FSP-OP mode register.

Figure 110: Command Bus Training Mode Exit with Valid Command

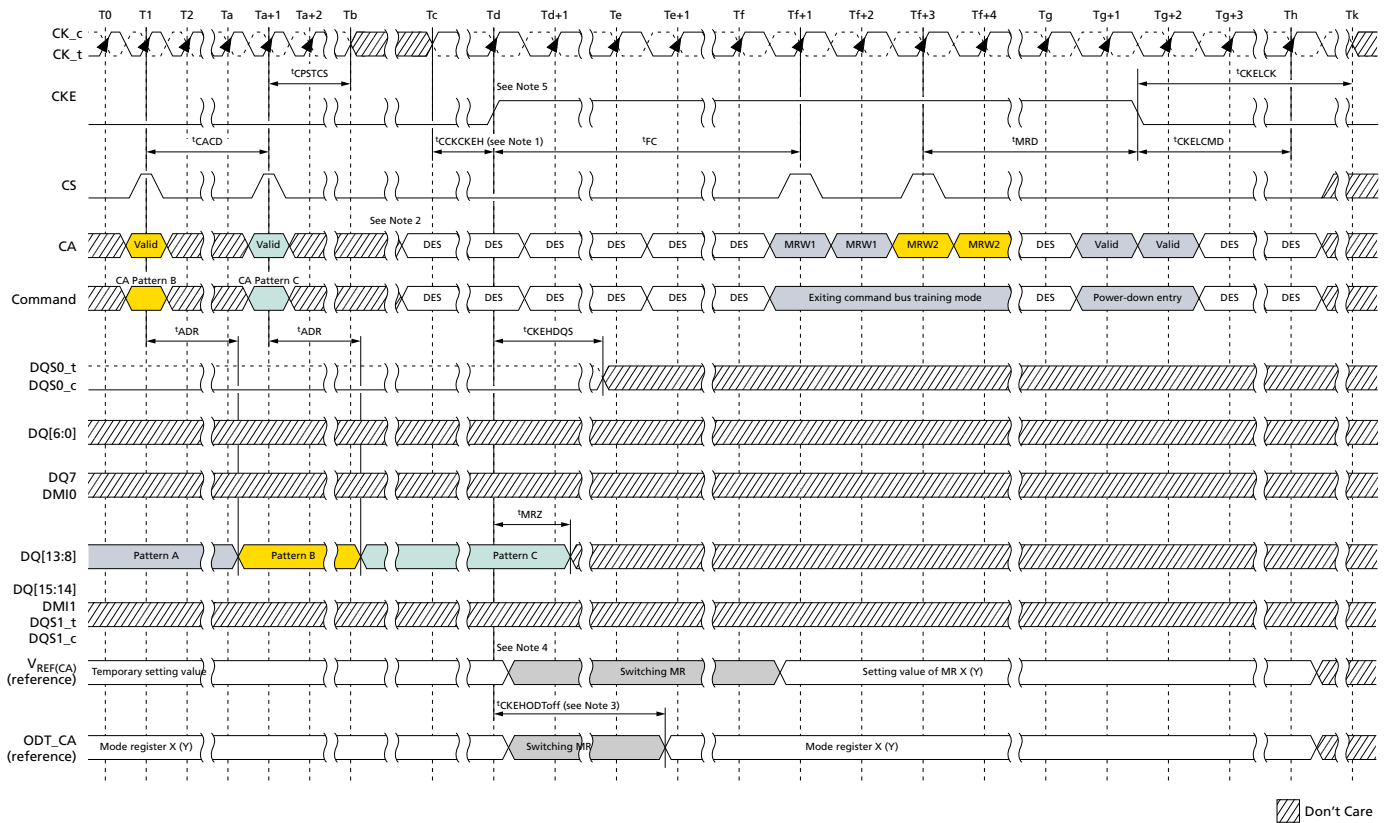


- Notes:
- The clock can be stopped or the frequency changed any time before t_{CKCKEH} . CK must meet t_{CKCKEH} before CKE is driven HIGH. When CKE is driven HIGH, the clock frequency must be returned to the original frequency (that is, the frequency corresponding to the FSP at command bus training mode entry).
 - CS and CA[5:0] must be deselected (LOW) t_{CKCKEH} before CKE is driven HIGH.
 - When CKE is driven HIGH, ODT_CA will revert to the state/value defined by FSP-OP prior to command bus training mode entry, that is, the original frequency set point (FSP-OP, MR13-OP[7]). For example, if the device was using FSP-OP[1] for training, then it will switch to FSP-OP[0] when CKE is driven HIGH.



4. Training values are not retained by the device and must be written to the FSP-OP register set before returning to operation at the trained frequency. For example, $V_{REF(CA)}$ will return to the value programmed in the original set point.
5. When CKE is driven HIGH, the device will revert to the FSP in operation at command bus training mode entry.

Figure 111: Command Bus Training Mode Exit with Power-Down Entry



- Notes:
1. The clock can be stopped or the frequency changed any time before t_{CKCKEH} . CK must meet t_{CKCKEH} before CKE is driven HIGH. When CKE is driven HIGH, the clock frequency must be returned to the original frequency (that is, the frequency corresponding to the FSP at command bus training mode entry).
 2. CS and CA[5:0] must be deselected (LOW) t_{CKCKEH} before CKE is driven HIGH.
 3. When CKE is driven HIGH, ODT_CA will revert to the state/value defined by FSP-OP prior to command bus training mode entry, that is, the original frequency set point (FSP-OP, MR13-OP[7]). For example, if the device was using FSP-OP[1] for training, then it will switch to FSP-OP[0] when CKE is driven HIGH.
 4. Training values are not retained by the device and must be written to the FSP-OP register set before returning to operation at the trained frequency. For example, $V_{REF(CA)}$ will return to the value programmed in the original set point.
 5. When CKE is driven HIGH, the device will revert to the FSP in operation at command bus training mode entry.



Write Leveling

Mode Register Write-WR Leveling Mode

To improve signal-integrity performance, the device provides a write leveling feature to compensate for CK-to-DQS timing skew, affecting timing parameters such as t_{DQSS} , t_{DSS} , and t_{DSH} . The memory controller uses the write leveling feature to receive feedback from the device, enabling it to adjust the clock-to-data strobe signal relationship for each DQS_t/DQS_c signal pair. The device samples the clock state with the rising edge of DQS signals and asynchronously feeds back to the memory controller. The memory controller references this feedback to adjust the clock-to-data strobe signal relationship for each DQS_t/DQS_c signal pair.

All data bits (DQ[7:0] for DQS[0] and DQ[15:8] for DQS[1]) carry the training feedback to the controller. Both DQS signals in each channel must be leveled independently. Write leveling entry/exit is independent between channels for dual-channel devices.

The device enters write leveling mode when mode register MR2-OP[7] is set HIGH. When entering write leveling mode, the state of the DQ pins is undefined. During write leveling mode, only DESELECT commands, or a MRW command to exit the WRITE LEVELING operation, are allowed. Depending on the absolute values of t_{QSL} and t_{QSH} in the application, the value of t_{DQSS} may have to be better than the limits provided in the AC Timing Parameters section in order to satisfy the t_{DSS} and t_{DSH} specifications. Upon completion of the WRITE LEVELING operation, the device exits write leveling mode when MR2-OP[7] is reset LOW.

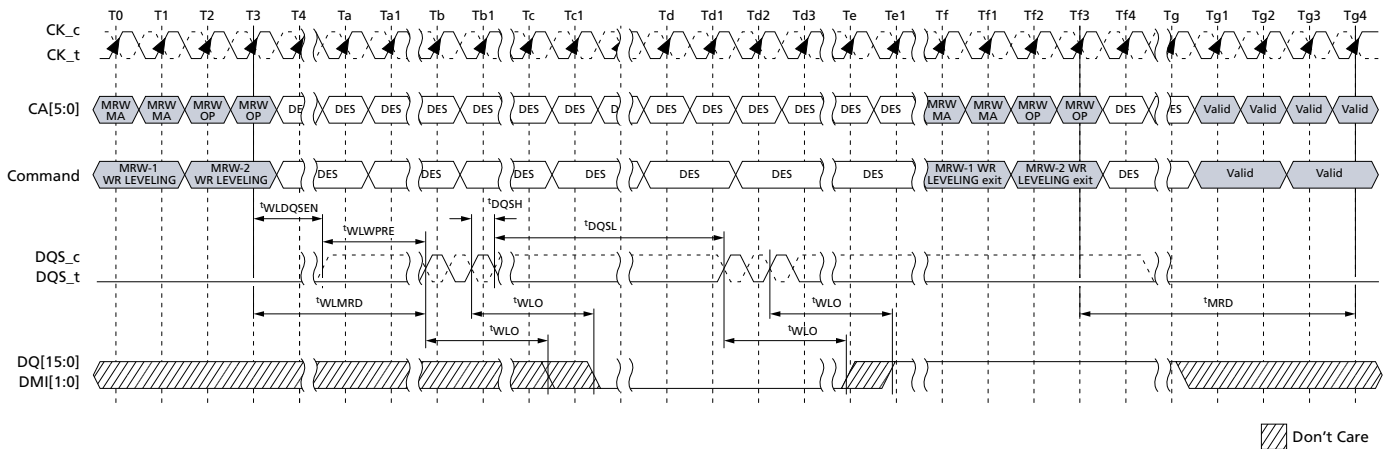
Write leveling should be performed before write training (DQS2DQ training).

Write Leveling Procedure

1. Enter write leveling mode by setting MR2-OP[7]=1.
2. Once in write leveling mode, DQS_t must be driven LOW and DQS_c HIGH after a delay of $t_{WLDQSEN}$.
3. Wait for a time $t_{WLDQSEN}$ before providing the first DQS signal input. The delay time $t_{WLMRD}(MAX)$ is controller-dependent.
4. The device may or may not capture the first rising edge of DQS_t due to an unstable first rising edge; therefore, at least two consecutive pulses of DQS signal input is required for every DQS input signal during write training mode. The captured clock level for each DQS edge is overwritten, and the device provides asynchronous feedback on all DQ bits after time t_{WLO} .
5. The feedback provided by the device is referenced by the controller to increment or decrement the DQS_t and/or DQS_c delay settings.
6. Repeat steps 4 and 5 until the proper DQS_t/DQS_c delay is established.
7. Exit write leveling mode by setting MR2-OP[7] = 0.

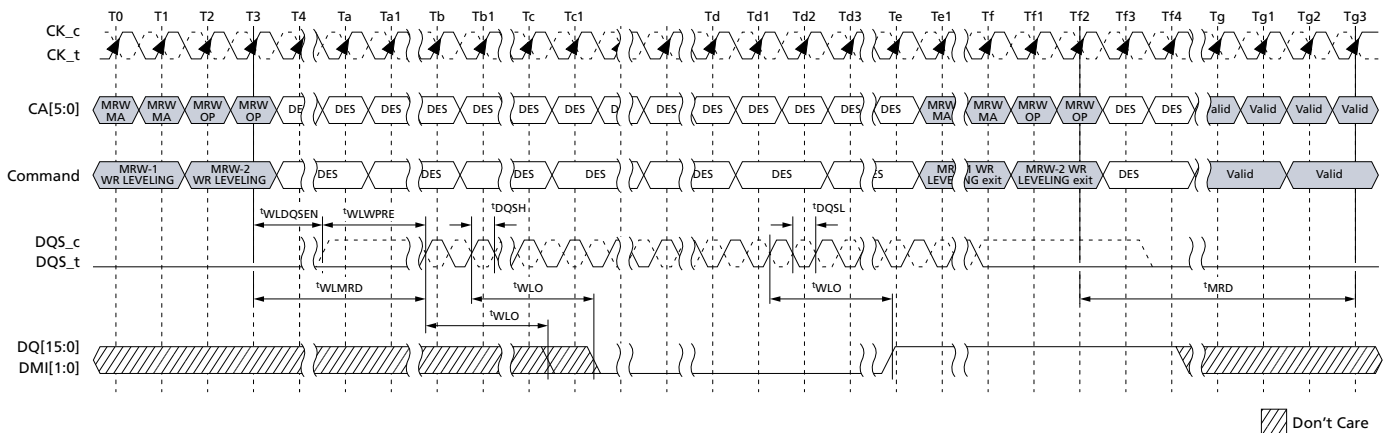


Figure 112: Write Leveling Timing – $t_{DQSL(MAX)}$



Note: 1. Clock can be stopped except during DQS toggle period ($CK_t = LOW$, $CK_c = HIGH$). However, a stable clock prior to sampling is required to ensure timing accuracy.

Figure 113: Write Leveling Timing – $t_{DQSL(MIN)}$



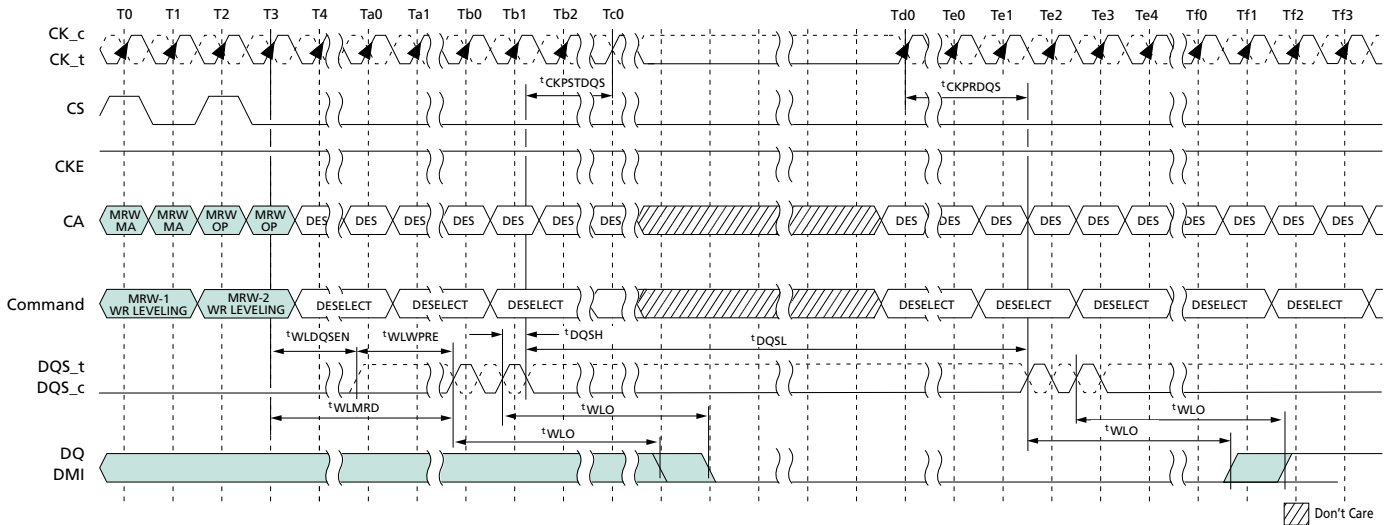
Note: 1. Clock can be stopped except during DQS toggle period ($CK_t = LOW$, $CK_c = HIGH$). However, a stable clock prior to sampling is required to ensure timing accuracy.

Input Clock Frequency Stop and Change

The input clock frequency can be stopped or changed from one stable clock rate to another stable clock rate during write leveling mode. The frequency stop or change timing is shown below.



Figure 114: Clock Stop and Timing During Write Leveling



- Notes: 1. CK_t is held LOW and CK_c is held HIGH during clock stop.
2. CS will be held LOW during clock stop.

Table 111: Write Leveling Timing Parameters

| Parameter | Symbol | Min/Max | Value | Units |
|--|-----------|---|------------------|-------|
| DQS_t/DQS_c delay after write leveling mode is programmed | tWLDQSEN | MIN | 20 | tCK |
| | | MAX | – | |
| Write preamble for write leveling | tWLWPRE | MIN | 20 | tCK |
| | | MAX | – | |
| First DQS_t/DQS_c edge after write leveling mode is programmed | tWLMRD | MIN | 40 | tCK |
| | | MAX | – | |
| Write leveling output delay | tWLO | MIN | 0 | ns |
| | | MAX | 20 | |
| MODE REGISTER SET command delay | tMRD | Refer to Mode Register Timing Parameter Table | | |
| Valid clock requirement before DQS toggle | tCKPRDQS | MIN | MAX(7.5ns, 4nCK) | – |
| | | MAX | – | |
| Valid clock requirement after DQS toggle | tCKPSTDQS | MIN | MAX(7.5ns, 4nCK) | – |
| | | MAX | – | |

Table 112: Write Leveling Setup and Hold Timing

| Parameter | Symbol | Min/Max | Data Rate | | | | | Unit |
|---------------------------|--------|---------|-----------|------|------|------|------|------|
| | | | 1600 | 2400 | 3200 | 3733 | 4267 | |
| Write leveling hold time | tWLH | MIN | 150 | 100 | 75 | 62.5 | 50 | ps |
| Write leveling setup time | tWLS | MIN | 150 | 100 | 75 | 62.5 | 50 | ps |



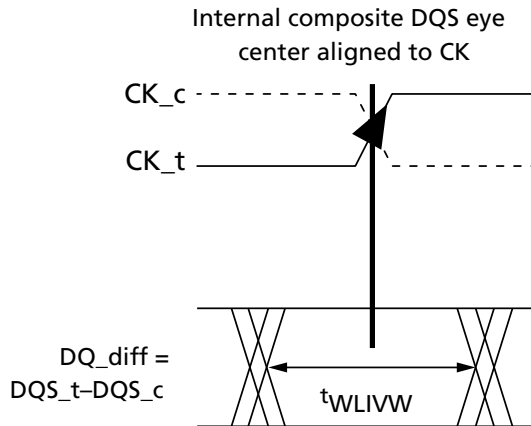
Table 112: Write Leveling Setup and Hold Timing (Continued)

| Parameter | Symbol | Min/Max | Data Rate | | | | | Unit |
|-----------------------------------|-------------|---------|-----------|------|------|------|------|------|
| | | | 1600 | 2400 | 3200 | 3733 | 4267 | |
| Write leveling input valid window | t^{WLIVW} | MIN | 240 | 160 | 120 | 105 | 90 | ps |

- Notes:
1. In addition to the traditional setup and hold time specifications, there is value in a invalid window-based specification for write leveling training. As the training is based on each device, worst case process skews for setup and hold do not make sense to close timing between CK and DQS.
 2. t^{WLIVW} is defined in a similar manner to $TdIVW_{total}$, except that here it is a DQS invalid window with respect to CK. This would need to account for all voltage and temperature (VT) drift terms between CK and DQS within the device that affect the write leveling invalid window.

The figure below shows the DQS input mask for timing with respect to CK. The “total” mask (t^{WLIVW}) defines the time the input signal must not encroach in order for the DQS input to be successfully captured by CK. The mask is a receiver property and it is not the valid data-eye.

Figure 115: DQS_t/DQS_c to CK_t/CK_c Timings at the Pins Referenced from the Internal Latch





MULTIPURPOSE Operation

The device uses the MULTIPURPOSE command to issue a NO OPERATION (NOP) command and to access various training modes. The MPC command is initiated with CS, and CA[5:0] asserted to the proper state at the rising edge of CK, as defined by the Command Truth Table. The MPC command has seven operands (OP[6:0]) that are decoded to execute specific commands in the SDRAM. OP[6] is a special bit that is decoded on the first rising CK edge of the MPC command. When OP[6] = 0, the device executes a NOP command, and when OP[6] = 1, the device further decodes one of several training commands.

When OP[6] = 1 and the training command includes a READ or WRITE operation, the MPC command must be followed immediately by a CAS-2 command. For training commands that read or write, READ latency (RL) and WRITE latency (WL) are counted from the second rising CK edge of the CAS-2 command with the same timing relationship as a typical READ or WRITE command. The operands of the CAS-2 command following a MPC READ/WRITE command must be driven LOW. The following MPC commands must be followed by a CAS-2 command:

- WRITE-FIFO
- READ-FIFO
- READ DQ CALIBRATION

All other MPC commands do not require a CAS-2 command, including the following:

- NOP
- START DQS OSCILLATOR
- STOP DQS OSCILLATOR
- ZQCAL START
- ZQCAL LATCH

Table 113: MPC Command Definition

| SDR Command | SDR Command Pins | | SDR CA Pins | | | | | | | CK_t Edge | Notes |
|---------------------|------------------|---------|-------------|-----|-----|-----|-----|-----|-----|-----------|-------|
| | CKE | | CS | CA0 | CA1 | CA2 | CA3 | CA4 | CA5 | | |
| | CK_t (n-1) | CK_t(n) | | | | | | | | | |
| MPC (Train, NOP) | H | H | H | L | L | L | L | L | OP6 | | 1, 2 |
| | | | L | OP0 | OP1 | OP2 | OP3 | OP4 | OP5 | | |

- Notes:
1. See the Command Truth Table for more information.
 2. MPC commands for READ or WRITE TRAINING operations must be immediately followed by the CAS-2 command, consecutively, without any other commands in between. The MPC command must be issued before issuing the CAS-2 command.

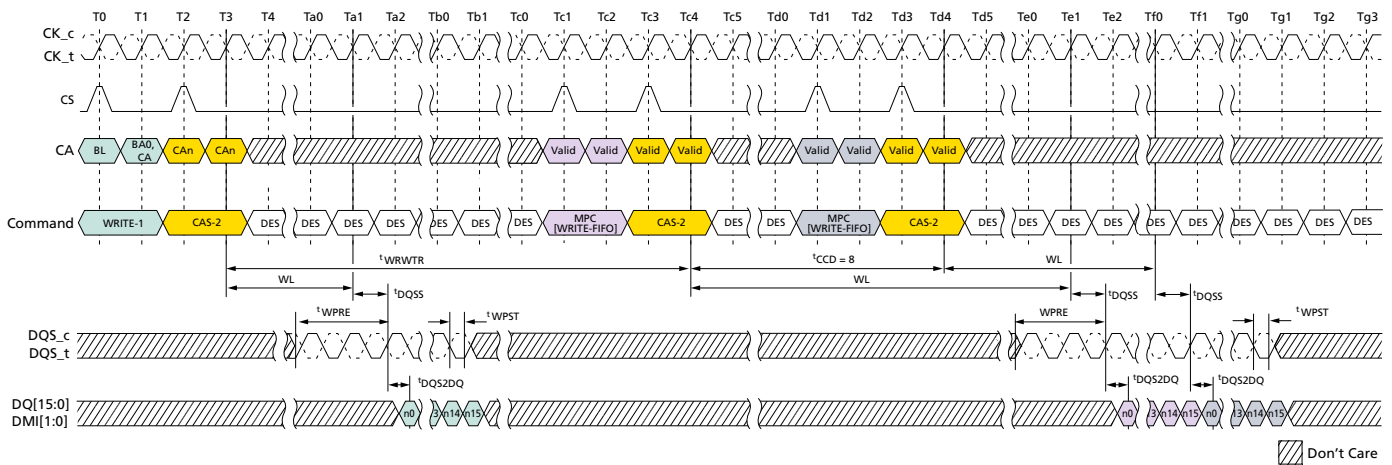


Table 114: MPC Commands

| Function | Operand | Data |
|----------------|---------|--|
| Training Modes | OP[6:0] | 0XXXXXXb: NOP 1000001b: READ-FIFO: READ-FIFO supports only BL16 operation 1000011b: READ DQ CALIBRATION (MR32/MR40) 100101b: RFU 100111b: WRITE-FIFO: WRITE-FIFO supports only BL16 operation 1001001b: RFU 1001011b: START DQS OSCILLATOR 1001101b: STOP DQS OSCILLATOR 1001111b: ZQCAL START 1010001b: ZQCAL LATCH All Others: Reserved |

- Notes:
1. See command truth table for more information.
 2. MPC commands for READ or WRITE TRAINING operations must be immediately followed by CAS-2 command consecutively without any other commands in-between. MPC command must be issued first before issuing the CAS-2 command.
 3. WRITE-FIFO and READ-FIFO commands will only operate as BL16, ignoring the burst length selected by MR1 OP[1:0].

Figure 116: WRITE-FIFO – $t^{WRPRE} = 2nCK$, $t^{WPST} = 0.5nCK$

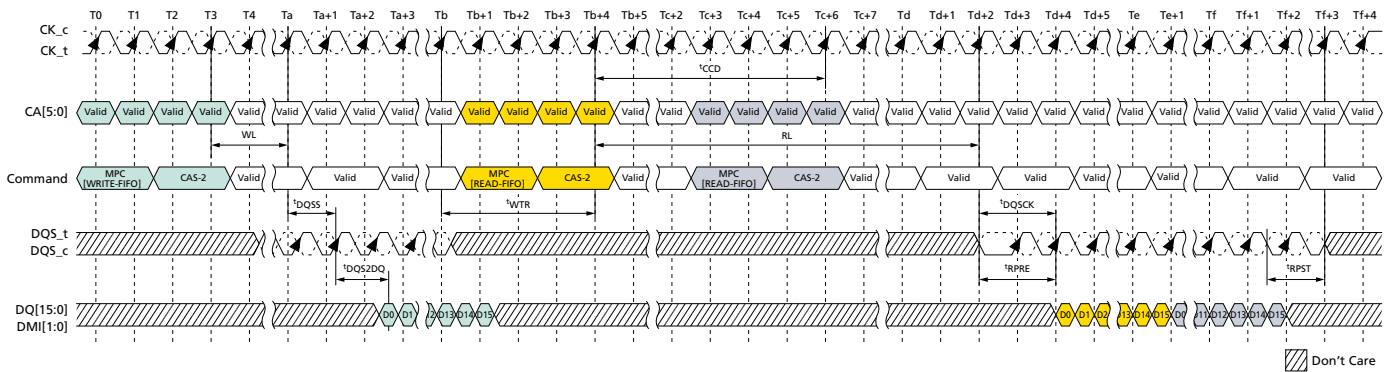


- Notes:
1. MPC[WRITE-FIFO] can be executed with a single bank or multiple banks active, during refresh or during self refresh, with CKE HIGH.
 2. Write-1 to MPC is shown as an example of command-to-command timing for MPC. Timing from Write-1 to MPC[WRITE-FIFO] is t^{WRWTR} .
 3. Seamless MPC[WRITE-FIFO] commands may be executed by repeating the command every t^{CCD} time.
 4. MPC[WRITE-FIFO] uses the same command-to-data timing relationship (W_L , t^{DQSS} , t^{DQS2DQ}) as a WRITE-1 command.
 5. A maximum of five MPC[WRITE-FIFO] commands may be executed consecutively without corrupting FIFO data. The sixth MPC[WRITE-FIFO] command will overwrite the FIFO data



- from the first command. If fewer than five MPC[WRITE-FIFO] commands are executed, then the remaining FIFO locations will contain undefined data.
- For the CAS-2 command following an MPC command, the CAS-2 operands must be driven LOW.
 - To avoid corrupting the FIFO contents, MPC[READ-FIFO] must immediately follow MPC[WRITE-FIFO]/CAS-2 without any other commands in-between. See Write Training section for more information on FIFO pointer behavior.

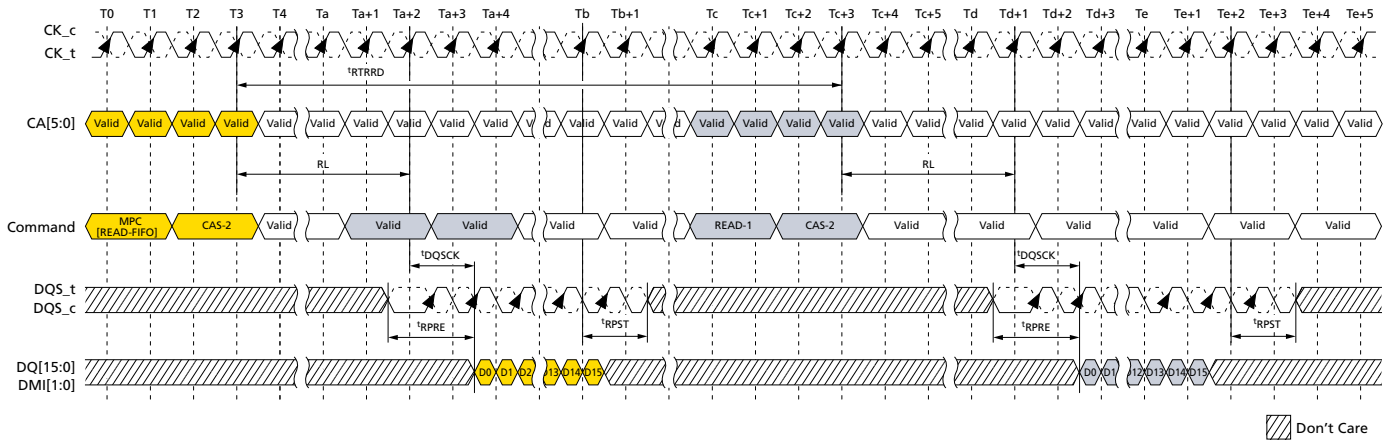
Figure 117: READ-FIFO – $t^*_{WPRE} = 2nCK$, $t^*_{WPST} = 0.5nCK$, $t^*_{RPRE} = \text{Toggle}$, $t^*_{RPST} = 1.5nCK$



- Notes:
- MPC[WRITE-FIFO] can be executed with a single bank or multiple banks active, during refresh or during self refresh with CKE HIGH.
 - Seamless MPC[READ-FIFO] commands may be executed by repeating the command every t^*_{CCD} time.
 - MPC[READ-FIFO] uses the same command-to-data timing relationship (RL, t^*_{DQ5CK}) as a READ-1 command.
 - Data may be continuously read from the FIFO without any data corruption. After five MPC[READ-FIFO] commands, the FIFO pointer will wrap back to the first FIFO and continue advancing. If fewer than five MPC[WRITE-FIFO] commands were executed, then the MPC[READ-FIFO] commands to those FIFO locations will return undefined data. See Write Training for more information on the FIFO pointer behavior.
 - For the CAS-2 command immediately following an MPC command, the CAS-2 operands must be driven LOW.
 - DMI[1:0] signals will be driven if WR-DBI, RD-DBI, or DM is enabled in the mode registers. See Write Training for more information on DMI behavior.



Figure 118: READ-FIFO – $t_{RPRE} = \text{Toggleing}$, $t_{RPST} = 1.5nCK$



- Notes:
1. MPC[WRITE-FIFO] can be executed with a single bank or multiple banks active, during refresh or during self refresh with CKE HIGH.
 2. MPC[READ-FIFO] to READ-1 operation is shown as an example of command-to-command timing for MPC. Timing from MPC[READ-FIFO] command to read is t_{RTRRD} .
 3. Seamless MPC[READ-FIFO] commands may be executed by repeating the command every t_{CCD} time.
 4. MPC[READ-FIFO] uses the same command-to-data timing relationship (RL, t_{DQSS}) as a READ-1 command.
 5. Data may be continuously read from the FIFO without any data corruption. After five MPC[READ-FIFO] commands, the FIFO pointer will wrap back to the first FIFO and continue advancing. If fewer than five MPC[WRITE-FIFO] commands are executed, then the MPC[READ-FIFO] commands to those FIFO locations will return undefined data. See Write Training for more information on the FIFO pointer behavior.
 6. For the CAS-2 command immediately following an MPC command, the CAS-2 operands must be driven LOW.
 7. DMI[1:0] signals will be driven if WR-DBI, RD-DBI, or DM is enabled in the mode registers. See Write Training for more information on DMI behavior.

Table 115: Timing Constraints for Training Commands

| Previous Command | Next Command | Minimum Delay | Unit | Notes |
|------------------|--------------------------|--|-------|-------|
| WR/MWR | MPC[WRITE-FIFO] | t_{WRWTR} | nCK | 1 |
| | MPC[READ-FIFO] | Not allowed | – | 2 |
| | MPC[READ DQ CALIBRATION] | $WL + RU(t_{DQSS}(\text{MAX})/t_{CK}) + BL/2 + RU(t_{WTR}/t_{CK})$ | nCK | |
| RD/MRR | MPC[WRITE-FIFO] | t_{RTW} | nCK | 4 |
| | MPC[READ-FIFO] | Not allowed | – | 2 |
| | MPC[READ DQ CALIBRATION] | t_{RTRRD} | nCK | 3 |


Table 115: Timing Constraints for Training Commands (Continued)

| Previous Command | Next Command | Minimum Delay | Unit | Notes |
|--------------------------|--------------------------|---|-------|-------|
| MPC[WRITE-FIFO] | WR/MWR | Not allowed | – | 2 |
| | MPC[WRITE-FIFO] | t_{CCD} | nCK | |
| | RD/MRR | Not allowed | – | 2 |
| | MPC[READ-FIFO] | $WL + RU(t_{DQSS}(MAX)/t_{CK}) + BL/2 + RU(t_{WTR}/t_{CK})$ | nCK | |
| | MPC[READ DQ CALIBRATION] | Not allowed | – | 2 |
| MPC[READ-FIFO] | WR/MWR | t_{RTW} | nCK | 4 |
| | MPC[WRITE-FIFO] | t_{RTW} | nCK | 4 |
| | RD/MRR | t_{RTRRD} | nCK | 3 |
| | MPC[READ-FIFO] | t_{CCD} | nCK | |
| | MPC[READ DQ CALIBRATION] | t_{RTRRD} | nCK | 3 |
| MPC[READ DQ CALIBRATION] | WR/MWR | t_{RTW} | nCK | 4 |
| | MPC[WRITE-FIFO] | t_{RTW} | nCK | 4 |
| | RD/MRR | t_{RTRRD} | nCK | 3 |
| | MPC[READ-FIFO] | Not allowed | – | 2 |
| | MPC[READ DQ CALIBRATION] | t_{CCD} | nCK | |

- Notes:
- $t_{WRWTR} = WL + BL/2 + RU(t_{DQSS}(MAX)/t_{CK}) + \text{MAX}(RU(7.5ns/t_{CK}), 8nCK)$.
 - No commands are allowed between MPC[WRITE-FIFO] and MPC[READ-FIFO] except the MRW commands related to training parameters.
 - $t_{RTRRD} = RL + RU(t_{DQSC}(MAX)/t_{CK}) + BL/2 + t_{RPST} + 0.5 + \text{MAX}(RU(7.5ns/t_{CK}), 8nCK)$.
 - In case of DQ ODT disable MR11 OP[2:0] = 000b,
 $t_{RTW} = RL + RU(t_{DQSC}(MAX)/t_{CK}) + BL/2 - WL + t_{WPRE} + RD(t_{RPST})$.
 In case of DQ ODT enable MR11 OP[2:0] ≠ 000b,
 $t_{RTW} = RL + RU(t_{DQSC}(MAX)/t_{CK}) + BL/2 + t_{RPST} - \text{ODTLon} - RD(t_{ODTon}(\text{Min})/t_{CK}) + 1$.



Read DQ Calibration Training

The READ DQ CALIBRATION TRAINING function outputs a 16-bit, user-defined pattern on the DQ pins. Read DQ calibration is initiated by issuing a MPC[READ DQ CALIBRATION] command followed by a CAS-2 command, which causes the device to drive the contents of MR32, followed by the contents of MR40 on each of DQ[15:0] and DMI[1:0]. The pattern can be inverted on selected DQ pins according to user-defined invert masks written to MR15 and MR20.

Read DQ Calibration Training Procedure

1. Issue MRW commands to write MR32 (first eight bits), MR40 (second eight bits), MR15 (eight-bit invert mask for byte 0), and MR20 (eight-bit invert mask for byte 1).

In the alternative, this step could be replaced with the default pattern:

- MR32 default = 5Ah
- MR40 default = 3Ch
- MR15 default = 55h
- MR20 default = 55h

2. Issue an MPC command, followed immediately by a CAS-2 command.

- Each time an MPC command, followed by a CAS-2, is received by the device, a 16-bit data burst will drive the eight bits programmed in MR32 followed by the eight bits programmed in MR40 on all I/O pins after the currently set RL.
- The data pattern will be inverted for I/O pins with a 1 programmed in the corresponding invert mask mode register bit (see table below).
- The pattern is driven on the DMI pins, but no DATA BUS INVERSION function is enabled, even if read DBI is enabled in the mode register.
- The MPC command can be issued every ^tCCD seamlessly, and ^tRTRRD delay is required between ARRAY READ command and the MPC command as well the delay required between the MPC command and an ARRAY READ.
- The operands received with the CAS-2 command must be driven LOW.

3. DQ

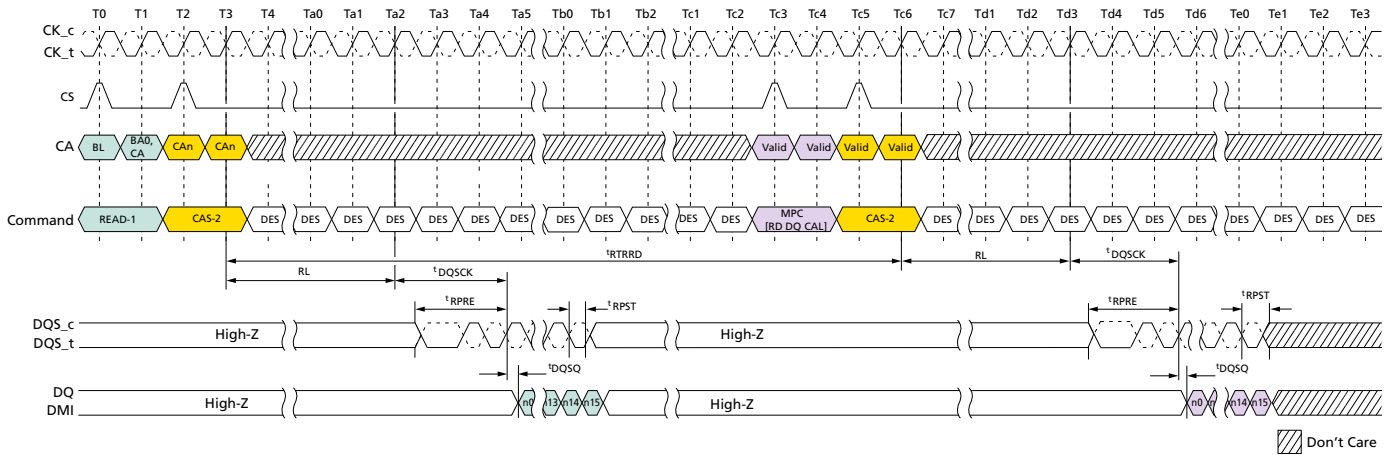
Read DQ calibration training can be performed with any or no banks active during refresh or during self refresh with CKE HIGH.

Table 116: Invert Mask Assignments

| | | | | | | | | | |
|----------|---|---|----|----|------|----|----|----|----|
| DQ pin | 0 | 1 | 2 | 3 | DMI0 | 4 | 5 | 6 | 7 |
| MR15 bit | 0 | 1 | 2 | 3 | N/A | 4 | 5 | 6 | 7 |
| DQ pin | 8 | 9 | 10 | 11 | DMI1 | 12 | 13 | 14 | 15 |
| MR20 bit | 0 | 1 | 2 | 3 | N/A | 4 | 5 | 6 | 7 |

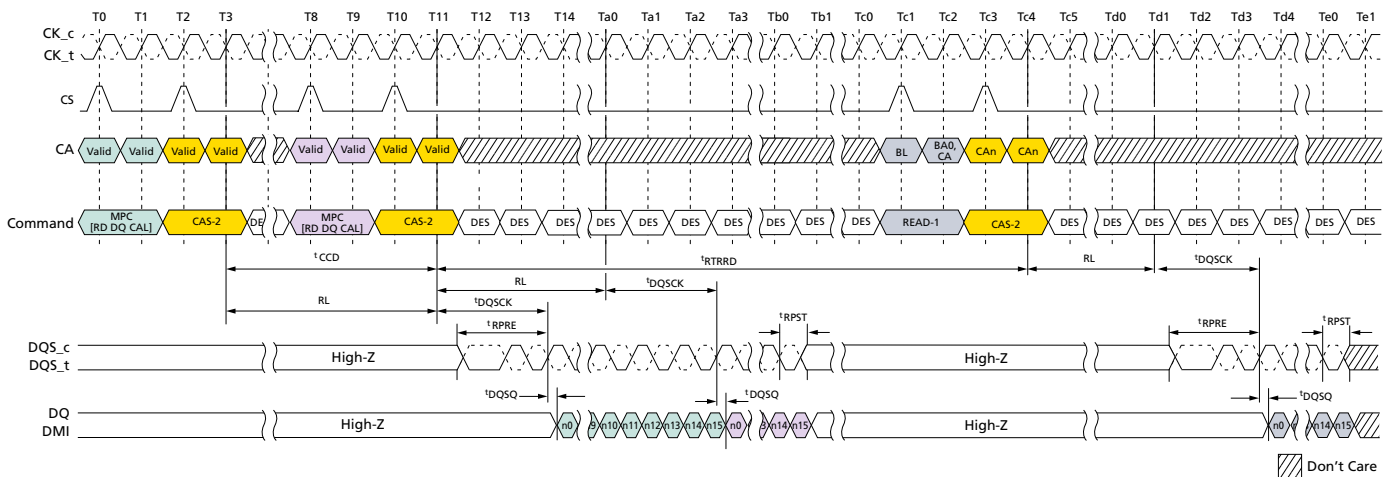


Figure 119: Read DQ Calibration Training Timing: Read-to-Read DQ Calibration



- Notes:
1. Read-1 to MPC operation is shown as an example of command-to-command timing. Timing from Read-1 to MPC command is t_{RTRRD} .
 2. MPC uses the same command-to-data timing relationship (RL , t_{DQSK} , t_{DQSQ}) as a Read-1 command.
 3. BL = 16, Read preamble: Toggle, Read postamble: 0.5nCK.
 4. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 120: Read DQ Calibration Training Timing: RTRRD DQ Calibration to Read DQ Calibration/Read



- Notes:
1. MPC[READ DQ CALIBRATION] to MPC[READ DQ CALIBRATION] operation is shown as an example of command-to-command timing.
 2. MPC[READ DQ CALIBRATION] to READ-1 operation is shown as an example of command-to-command timing.
 3. MPC[READ DQ CALIBRATION] uses the same command-to-data timing relationship (RL , t_{DQSK} , t_{DQSQ}) as a READ-1 command.
 4. Seamless MPC[READ DQ CALIBRATION] commands may be executed by repeating the command every t_{CCD} time.
 5. Timing from MPC[READ DQ CALIBRATION] command to READ-1 is t_{RTRRD} .



6. BL = 16, Read preamble: Toggle, Read postamble: $0.5nCK$.
7. DES commands are shown for ease of illustration; other commands may be valid at these times.

Read DQ Calibration Training Example

An example of read DQ calibration training output is shown in table below. This shows the 16-bit data pattern that will be driven on each DQ in byte 0 when one READ DQ CALIBRATION TRAINING command is executed. This output assumes the following mode register values are used:

- MR32 = 1CH
- MR40 = 59H
- MR15 = 55H
- MR20 = 55H

Table 117: Read DQ Calibration Bit Ordering and Inversion Example

| Pin | Bit Sequence → | | | | | | | | | | | | | | | | |
|------|----------------|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| | Invert | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DQ0 | Yes | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| DQ1 | No | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| DQ2 | Yes | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| DQ3 | No | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| DMI0 | Never | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| DQ4 | Yes | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| DQ5 | No | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| DQ6 | Yes | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| DQ7 | No | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| DQ8 | Yes | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| DQ9 | No | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| DQ10 | Yes | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| DQ11 | No | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| DMI1 | Never | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| DQ12 | Yes | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| DQ13 | No | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| DQ14 | Yes | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| DQ15 | No | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |

- Notes:
1. The patterns contained in MR32 and MR40 are transmitted on DQ[15:0] and DMI[1:0] when read DQ calibration is initiated via a MPC[READ DQ CALIBRATION] command. The pattern transmitted serially on each data lane, organized little endian such that the low-order bit in a byte is transmitted first. If the data pattern is 27H, then the first bit transmitted will be a 1, followed by 1, 1, 0, 0, 1, 0, and 0. The bit stream will be 00100111 →.
 2. MR15 and MR20 may be used to invert the MR32/MR40 data pattern on the DQ pins. See MR15 and MR20 for more information. Data is never inverted on the DMI[1:0] pins.
 3. DMI [1:0] outputs status follows MR Setting vs. DMI Status table.



- No DATA BUS INVERSION (DBI) function is enacted during read DQ calibration, even if DBI is enabled in MR3-OP[6].

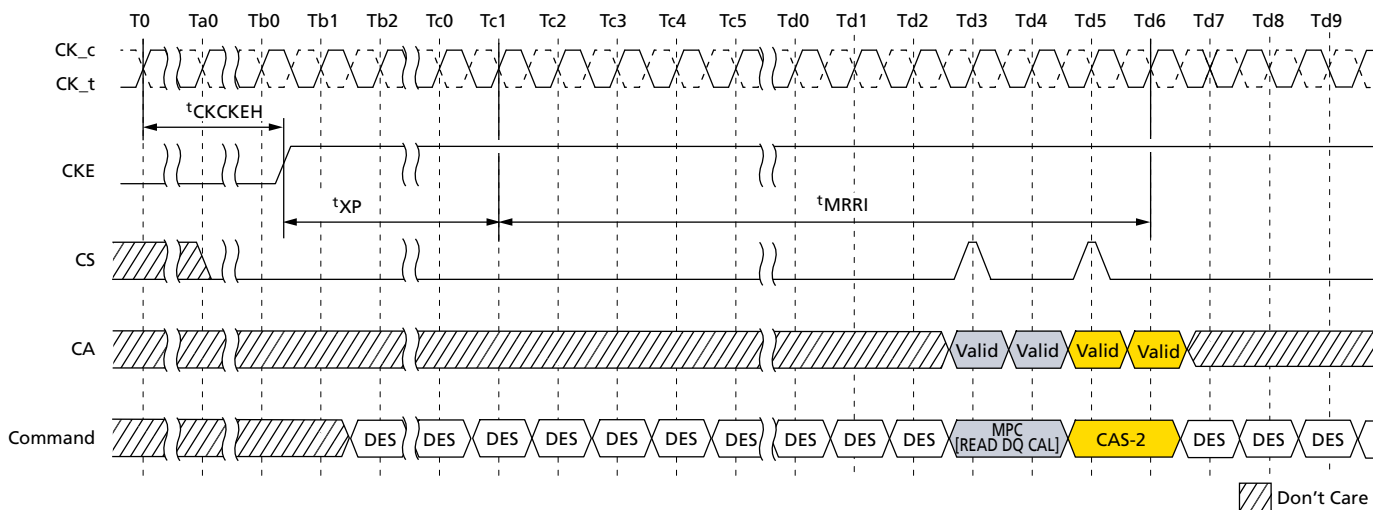
Table 118: MR Setting vs. DMI Status

| DM Function MR13 OP[5] | WRITE DBI _{dc} Function MR3 OP[7] | READ DBI _{dc} Function MR3 OP[6] DMI | Status |
|---------------------------|---|--|---------------------------------|
| 1: Disable | 0: Disable | 0: Disable | High-Z |
| 1: Disable | 1: Enable | 0: Disable | The data pattern is transmitted |
| 1: Disable | 0: Disable | 1: Enable | The data pattern is transmitted |
| 1: Disable | 1: Enable | 1: Enable | The data pattern is transmitted |
| 0: Enable | 0: Disable | 0: Disable | The data pattern is transmitted |
| 0: Enable | 1: Enable | 0: Disable | The data pattern is transmitted |
| 0: Enable | 0: Disable | 1: Enable | The data pattern is transmitted |
| 0: Enable | 1: Enable | 1: Enable | The data pattern is transmitted |

MPC[READ DQ CALIBRATION] After Power-Down Exit

Following the power-down state, an additional time, t_{MRRI} , is required prior to issuing the MPC[READ DQ CALIBRATION] command. This additional time (equivalent to t_{RCD}) is required in order to be able to maximize power-down current savings by allowing more power-up time for the read DQ data in MR32 and MR40 data path after exit from standby, power-down mode.

Figure 121: MPC[READ DQ CALIBRATION] Following Power-Down State



Write Training

The device uses an unmatched DQS-DQ path to enable high-speed performance and save power. As a result, the DQS strobe must be trained to arrive at the DQ latch center-aligned with the data eye. The DQ receiver is located at the DQ pad and has a shorter internal delay than the DQS signal. The DQ receiver will latch the data present on the



DQ bus when DQS reaches the latch, and training is accomplished by delaying the DQ signals relative to DQS such that the data eye arrives at the receiver latch centered on the DQS transition.

Two modes of training are available:

- Command-based FIFO WR/RD with user patterns
- An internal DQS clock-tree oscillator, which determines the need for, and the magnitude of, required training

The command-based FIFO WR/RD uses the MPC command with operands to enable this special mode of operation. When issuing the MPC command, if CA[5] is set LOW (OP[6] = 0), then the device will perform a NOP command. When CA[5] is set HIGH, the CA[4:0] pins enable training functions or are reserved for future use (RFU). MPC commands that initiate a read or write to the device must be followed immediately by a CAS-2 command. See the MPC Operation section for more information.

To perform write training, the controller can issue an MPC[WRITE-FIFO] command with OP[6:0] set, followed immediately by a CAS-2 command (CAS-2 operands should be driven LOW) to initiate a WRITE-FIFO. Timings for MPC[WRITE-FIFO] are identical to WRITE commands, with WL timed from the second rising clock edge of the CAS-2 command. Up to five consecutive MPC[WRITE-FIFO] commands with user-defined patterns may be issued to the device, which will store up to 80 values (BL16 × 5) per pin that can be read back via the MPC[READ-FIFO] command. (The WRITE/READ-FIFO POINTER operation is described in a different section.

After writing data with the MPC[WRITE-FIFO] command, the data can be read back with the MPC[READ-FIFO] command and results can be compared with "expected" data to determine whether further training (DQ delay) is needed. MPC[READ-FIFO] is initiated by issuing an MPC command, as described in the MPC Operation section, followed immediately by a CAS-2 command (CAS-2 operands must be driven LOW). Timings for the MPC[READ-FIFO] command are identical to READ commands, with RL timed from the second rising clock edge of the CAS-2 command.

READ-FIFO is nondestructive to the data captured in the FIFO; data may be read continuously until it is disturbed by another command, such as a READ, WRITE, or another MPC[WRITE-FIFO]. If fewer than five WRITE-FIFO commands are executed, unwritten registers will have undefined (but valid) data when read back.

For example: If five WRITE-FIFO commands are executed sequentially, then a series of READ-FIFO commands will read valid data from FIFO[0], FIFO[1]...FIFO[4] and then wrap back to FIFO[0] on the next READ-FIFO. However, if fewer than five WRITE-FIFO commands are executed sequentially (example = 3), then a series of READ-FIFO commands will return valid data for FIFO[0], FIFO[1], and FIFO[2], but the next two READ-FIFO commands will return undefined data for FIFO[3] and FIFO[4] before wrapping back to the valid data in FIFO[0].

The READ-FIFO pointer and WRITE-FIFO pointer are reset under the following conditions:

- Power-up initialization
- RESET_n asserted
- Power-down entry
- Self refresh power-down entry



The MPC[WRITE-FIFO] command advances the WRITE-FIFO pointer, and the MPC[READ-FIFO] advances the READ-FIFO pointer. Also any normal (non-FIFO) READ operation (RD, RDA) advances both WRITE-FIFO pointer and READ-FIFO pointer. Issuing (non-FIFO) READ operation command is inhibited during write training period. To keep the pointers aligned, the SoC memory controller must adhere to the following restriction at the end of Write training period:

$$b = a + (n \times c)$$

Where:

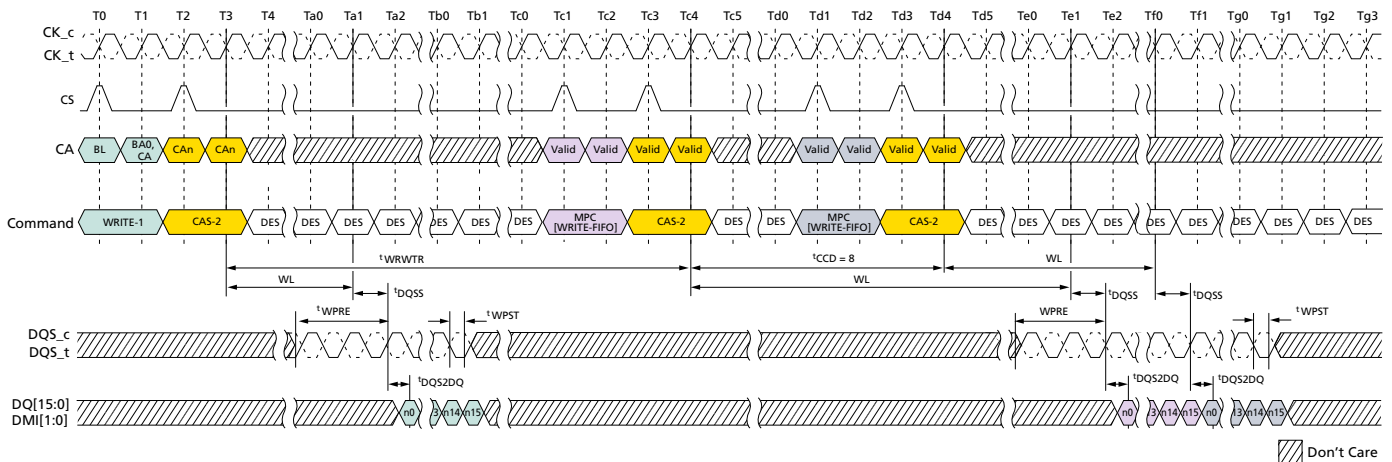
'a' is the number of MPC[WRITE-FIFO] commands

'b' is the number of MPC[READ-FIFO] commands

'c' is the FIFO depth (= 5 for LPDDR4)

'n' is a positive integer, ≥ 0

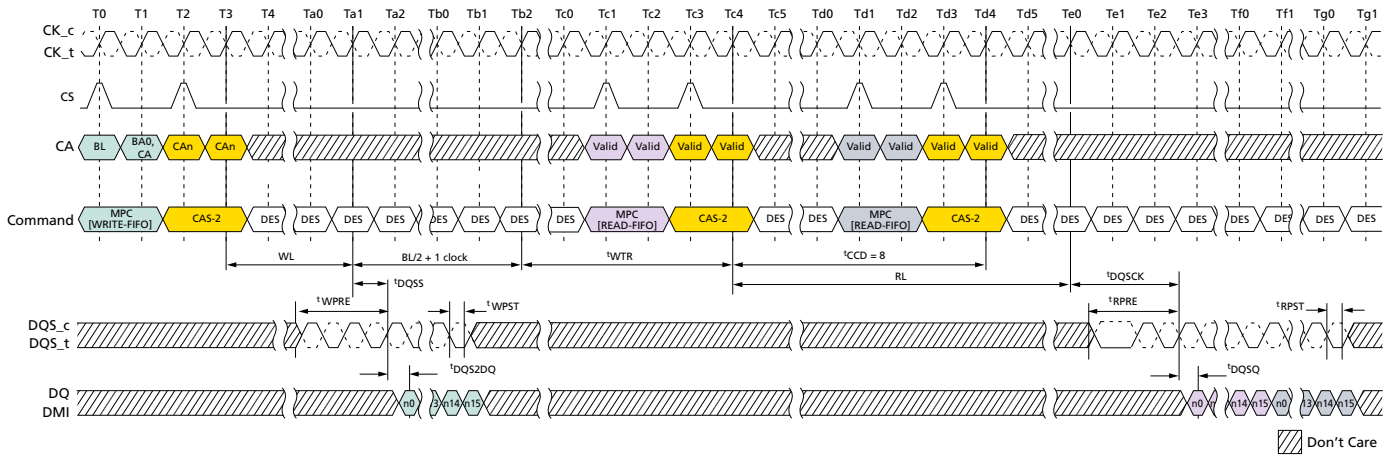
Figure 122: WRITE-to-MPC[WRITE-FIFO] Operation Timing



- Notes:
1. MPC[WRITE-FIFO] can be executed with a single bank or multiple banks active during REFRESH or during SELF REFRESH with CKE HIGH.
 2. Write-1 to MPC is shown as an example of command-to-command timing for MPC. Timing from Write-1 to MPC[WRITE-FIFO] is t_{WRWTR} .
 3. Seamless MPC[WR-FIFO] commands may be executed by repeating the command every t_{CCD} time.
 4. MPC[WRITE-FIFO] uses the same command-to-data timing relationship (WL, t_{DQSS} , t_{DQS2DQ}) as a WRITE-1 command.
 5. A maximum of five MPC[WRITE-FIFO] commands may be executed consecutively without corrupting FIFO data. The sixth MPC[WRITE-FIFO] command will overwrite the FIFO data from the first command. If fewer than five MPC[WRITE-FIFO] commands are executed, then the remaining FIFO locations will contain undefined data.
 6. For the CAS-2 command following an MPC command, the CAS-2 operands must be driven LOW.
 7. To avoid corrupting the FIFO contents, MPC[READ-FIFO] must immediately follow MPC[WRITE-FIFO]/CAS-2 without any other commands disturbing FIFO pointers in between. FIFO pointers are disturbed by CKE LOW, WRITE, MASKED WRITE, READ, READ DQ CALIBRATION, and MRR.
 8. BL = 16, Write postamble = $0.5nCK$.
 9. DES commands are shown for ease of illustration; other commands may be valid at these times.



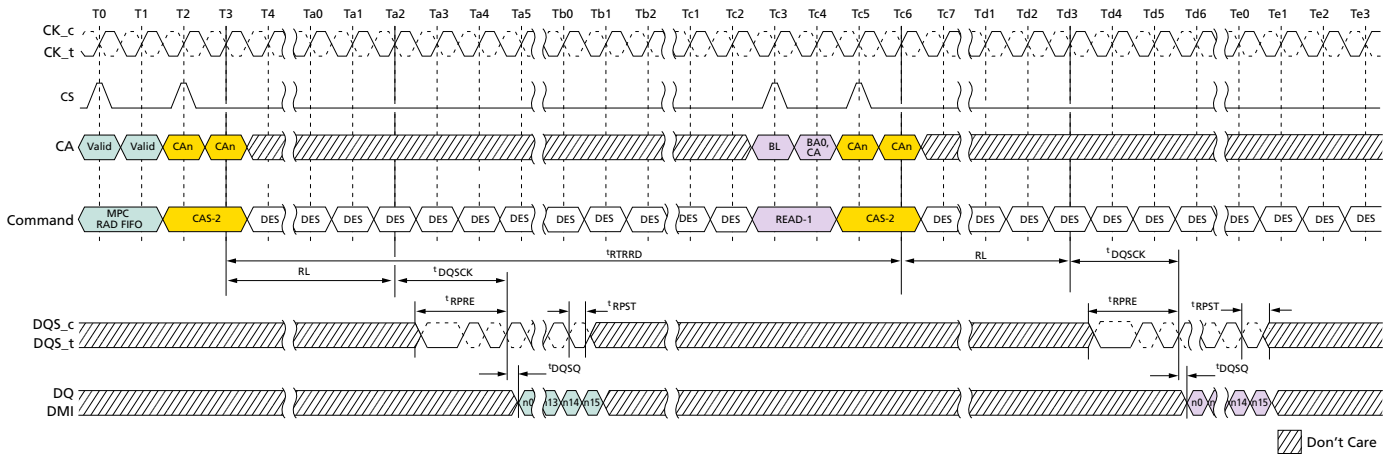
Figure 123: MPC[WRITE-FIFO]-to-MPC[READ-FIFO] Timing



- Notes:
1. MPC[WRITE-FIFO] can be executed with a single bank or multiple banks active during refresh or during self refresh with CKE HIGH.
 2. MPC[WRITE-FIFO] to MPC[READ-FIFO] is shown as an example of command-to-command timing for MPC. Timing from MPC[WRITE-FIFO] to MPC[READ-FIFO] is specified in the command-to-command timing table.
 3. Seamless MPC[READ-FIFO] commands may be executed by repeating the command every t_{CCD} time.
 4. MPC[READ-FIFO] uses the same command-to-data timing relationship (RL, t_{DQSK} , t_{DQSQ}) as a READ-1 command.
 5. Data may be continuously read from the FIFO without any data corruption. After five MPC[READ-FIFO] commands, the FIFO pointer will wrap back to the first FIFO and continue advancing. If fewer than five MPC[WRITE-FIFO] commands were executed, then the MPC[READ-FIFO] commands to those FIFO locations will return undefined data. See Write Training for more information on the FIFO pointer behavior.
 6. For the CAS-2 command immediately following an MPC command, the CAS-2 operands must be driven LOW.
 7. DMI[1:0] signals will be driven if WR-DBI, RD-DBI, or DM is enabled in the mode registers. See Write Training section for more information on DMI behavior.
 8. BL = 16, Write postamble = $0.5nCK$, Read preamble: Toggle, Read postamble: $0.5nCK$.
 9. DES commands are shown for ease of illustration; other commands may be valid at these times.



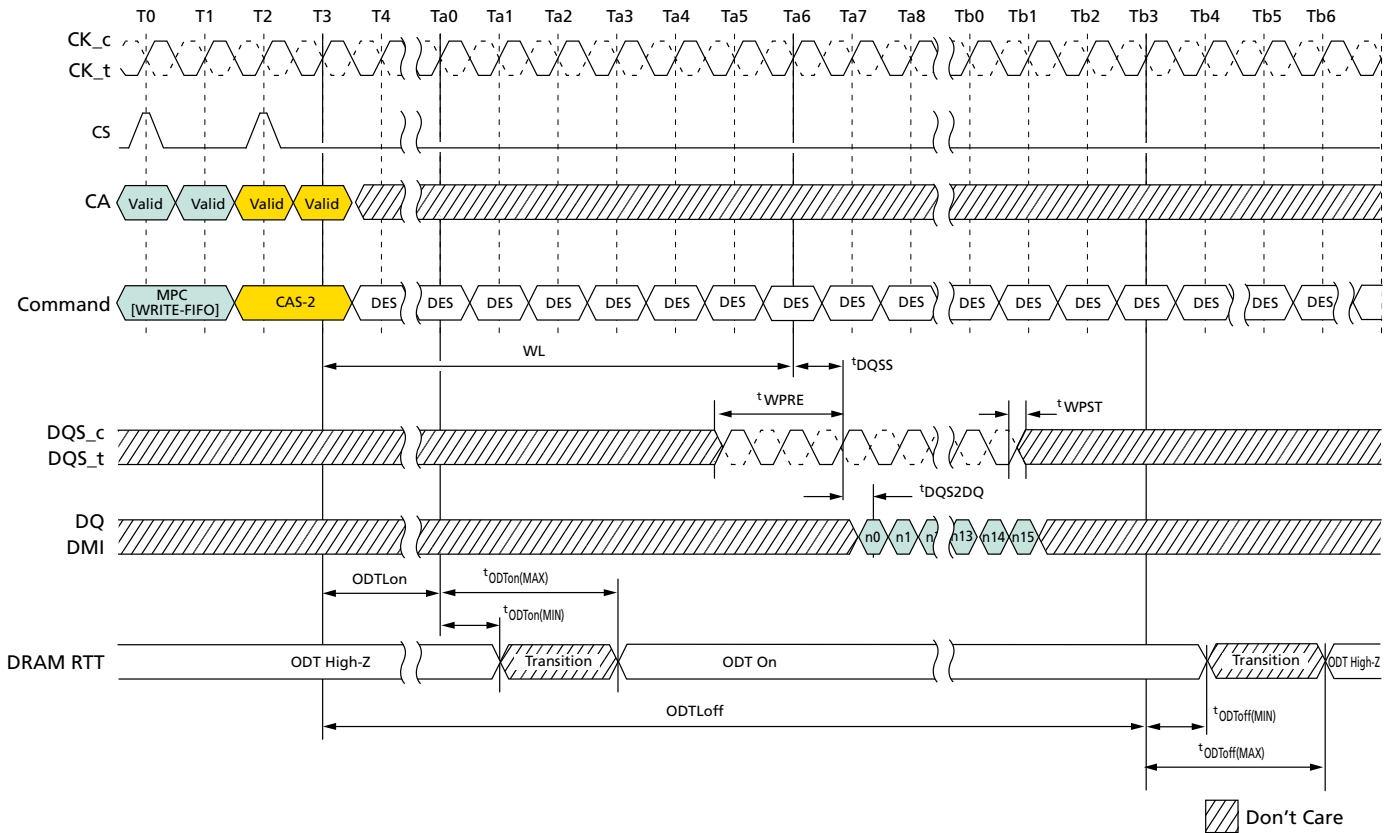
Figure 124: MPC[READ-FIFO] to Read Timing



- Notes:
1. MPC[WRITE-FIFO] can be executed with a single bank or multiple banks active during refresh or during self refresh with CKE HIGH.
 2. MPC[READ-FIFO] to READ-1 operation is shown as an example of command-to-command timing for MPC. Timing from MPC[READ-FIFO] command to READ is t_{RTRRD} .
 3. Seamless MPC[READ-FIFO] commands may be executed by repeating the command every t_{CCD} time.
 4. MPC[READ-FIFO] uses the same command-to-data timing relationship (RL , t_{DQSK} , t_{DQSQ}) as a READ-1 command.
 5. Data may be continuously read from the FIFO without any data corruption. After five MPC[READ-FIFO] commands, the FIFO pointer will wrap back to the first FIFO and continue advancing. If fewer than five MPC[WRITE-FIFO] commands were executed, then the MPC[READ-FIFO] commands to those FIFO locations will return undefined data. See Write Training for more information on the FIFO pointer behavior.
 6. For the CAS-2 command immediately following an MPC command, the CAS-2 operands must be driven LOW.
 7. DMI[1:0] signals will be driven if WR-DBI, RD-DBI, or DM is enabled in the mode registers. See Write Training for more information on DMI behavior.
 8. BL = 16, Read preamble: Toggle, Read postamble: $0.5nCK$
 9. DES commands are shown for ease of illustration; other commands may be valid at these times.



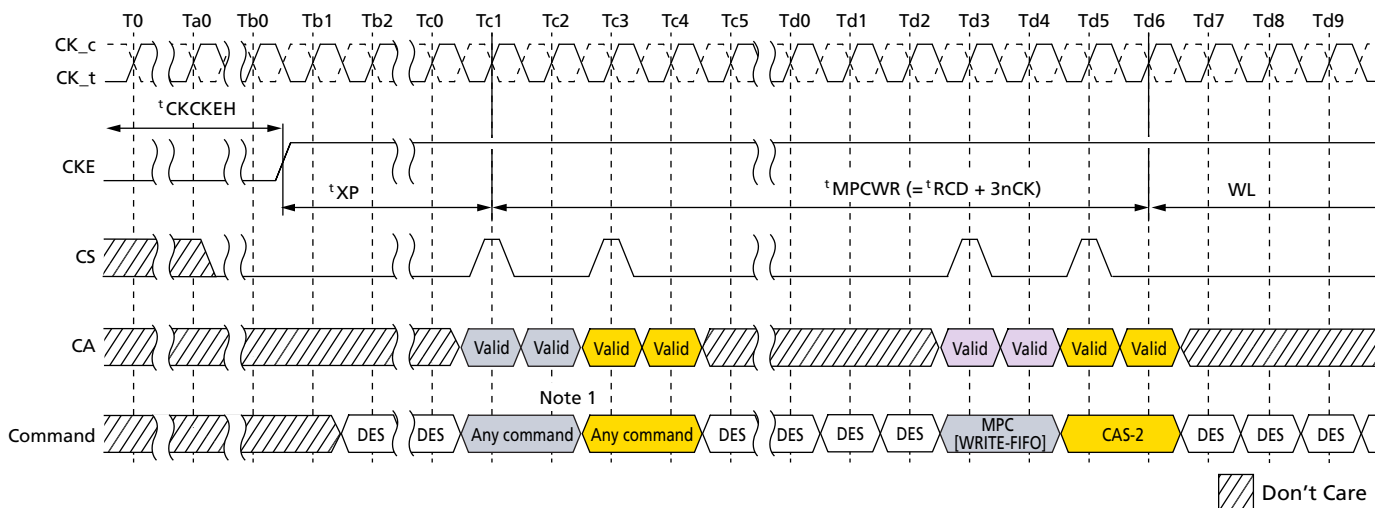
Figure 125: MPC[WRITE-FIFO] with DQ ODT Timing



- Notes:
1. MPC[WRITE-FIFO] can be executed with a single bank or multiple banks active during refresh or during self refresh with CKE HIGH.
 2. MPC[WRITE-FIFO] uses the same command-to-data/ODT timing relationship (RL, t_{DQSS} , t_{DQS2DQ} , ODTLon, ODTLoff, t_{ODTOn} , t_{ODTOff}) as a WRITE-1 command.
 3. For the CAS-2 command immediately following an MPC command, the CAS-2 operands must be driven LOW.
 4. BL = 16, Write postamble = $0.5nCK$.
 5. DES commands are shown for ease of illustration; other commands may be valid at these times.



Figure 126: Power-Down Exit to MPC[WRITE-FIFO] Timing



- Notes:
1. Any commands except MPC[WRITE-FIFO] and other exception commands defined other section in this document (for example, MPC[READ DQ CALIBRATION]).
 2. DES commands are shown for ease of illustration; other commands may be valid at these times.

Table 119: MPC[WRITE-FIFO] AC Timing

| Parameter | Symbol | MIN/MAX | Value | Unit |
|--|-------------|---------|------------------|------|
| Additional time after t_{XP} has expired until MPC[WRITE-FIFO] command may be issued | t_{MPCWR} | MIN | $t_{RCD} + 3nCK$ | – |

Internal Interval Timer

As voltage and temperature change on the device, the DQS clock-tree delay will shift, requiring retraining. The device includes an internal DQS clock-tree oscillator to measure the amount of delay over a given time interval (determined by the controller), allowing the controller to compare the trained delay value to the delay value seen at a later time. The DQS oscillator will provide the controller with important information regarding the need to retrain and the magnitude of potential error.

The DQS interval oscillator is started by issuing an MPC command with OP[6:0] set as described in MPC Operation, which will start an internal ring oscillator that counts the number of time a signal propagates through a copy of the DQS clock tree.

The DQS oscillator may be stopped by issuing an MPC[STOP DQS OSCILLATOR] command with OP[6:0] set as described in MPC Operation, or the controller may instruct the SDRAM to count for a specific number of clocks and then stop automatically (See MR23 for more information). If MR23 is set to automatically stop the DQS oscillator, then the MPC[STOP DQS OSCILLATOR] command should not be used (illegal). When the DQS oscillator is stopped by either method, the result of the oscillator counter is automatically stored in MR18 and MR19.

The controller may adjust the accuracy of the result by running the DQS interval oscillator for shorter (less accurate) or longer (more accurate) duration. The accuracy of the



result for a given temperature and voltage is determined by the following equation, where run time = total time between START and STOP commands and DQS delay = the value of the DQS clock tree delay ($t_{DQS2DQ}(\text{MIN}) / (\text{MAX})$):

$$\text{DQS oscillator granularity error} = \frac{2 \times (\text{DQS delay})}{\text{run time}}$$

Additional matching error must be included, which is the difference between DQS training circuit and the actual DQS clock tree across voltage and temperature. The matching error is vendor specific. Therefore, the total accuracy of the DQS oscillator counter is given by:

$$\text{DQS oscillator accuracy} = 1 - \text{granularity error} - \text{matching error}$$

For example, if the total time between START and STOP commands is 100ns, and the maximum DQS clock tree delay is 800ps ($t_{DQS2DQ}(\text{MAX})$), then the DQS oscillator granularity error is:

$$\text{DQS oscillator granularity error} = \frac{2 \times (0.8\text{ns})}{100\text{ns}} = 1.6\%$$

This equates to a granularity timing error of 12.8ps. Assuming a circuit matching error of 5.5ps across voltage and temperature, the accuracy is:

$$\text{DQS oscillator accuracy} = 1 - \frac{12.8 + 5.5}{800} = 97.7\%$$

For example, running the DQS oscillator for a longer period improves the accuracy. If the total time between START and STOP commands is 500ns, and the maximum DQS clock tree delay is 800ps ($t_{DQS2DQ}(\text{MAX})$), then the DQS oscillator granularity error is:

$$\text{DQS oscillator granularity error} = \frac{2 \times (0.8\text{ns})}{500\text{ns}} = 0.32\%$$

This equates to a granularity timing error of 2.56ps. Assuming a circuit matching error of 5.5ps across voltage and temperature, the accuracy is:

$$\text{DQS oscillator accuracy} = 1 - \frac{2.56 + 5.5}{800} = 99.0\%$$

The result of the DQS interval oscillator is defined as the number of DQS clock tree delays that can be counted within the run time, determined by the controller. The result is stored in MR18-OP[7:0] and MR19-OP[7:0].

MR18 contains the least significant bits (LSB) of the result, and MR19 contains the most significant bits (MSB) of the result. MR18 and MR19 are overwritten by the SDRAM when a MPC[STOP DQS OSCILLATOR] command is received.

The SDRAM counter will count to its maximum value ($= 2^{16}$) and stop. If the maximum value is read from the mode registers, the memory controller must assume that the counter overflowed the register and therefore discard the result. The longest run time for the oscillator that will not overflow the counter registers can be calculated as follows:

$$\text{Longest runtime interval} = 2^{16} \times t_{DQS2DQ}(\text{MIN}) = 2^{16} \times 0.2\text{ns} = 13.1\mu\text{s}$$



DQS Interval Oscillator Matching Error

The interval oscillator matching error is defined as the difference between the DQS training ckt (interval oscillator) and the actual DQS clock tree across voltage and temperature.

Parameters:

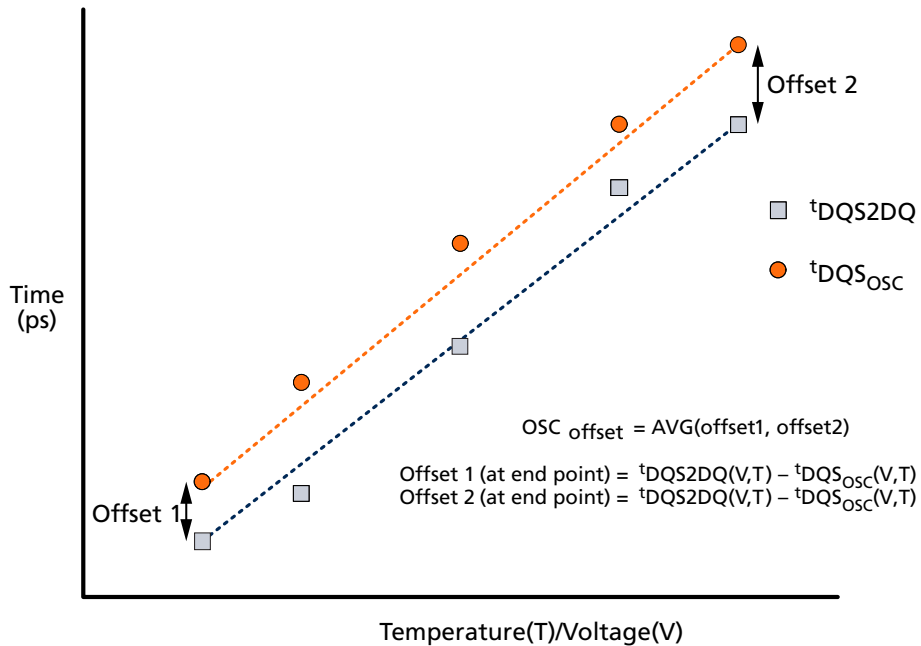
t_{DQS2DQ} : Actual DQS clock tree delay

$t_{DQS_{OSC}}$: Training ckt (interval oscillator) delay

OSC_{Offset} : Average delay difference over voltage and temperature (shown below)

OSC_{Match} : DQS oscillator matching error

Figure 127: Interval Oscillator Offset – OSC_{Offset}



OSC_{Match} :

$$OSC_{Match} = [t_{DQS2DQ}(V,T) - t_{DQS_{OSC}}(V,T) - OSC_{offset}]$$

$t_{DQS_{OSC}}$:

$$t_{DQS_{OSC}}(V,T) = [\frac{Runtime}{2 \times Count}]$$

Table 120: DQS Oscillator Matching Error Specification

| Parameter | Symbol | MIN | MAX | Unit | Notes |
|-------------------------------|----------------|------|-----|------|------------------------|
| DQS oscillator matching error | OSC_{Match} | -20 | 20 | ps | 1, 2, 3, 4, 5, 6, 7, 8 |
| DQS oscillator offset | OSC_{offset} | -100 | 100 | ps | 2, 4, 7 |

Notes: 1. The OSC_{Match} is the matching error per between the actual DQS and DQS interval oscillator over voltage and temperature.



2. This parameter will be characterized or guaranteed by design.
3. The OSC_{Match} is defined as the following:

$$OSC_{Match} = [{}^tDQS2DQ(V, T) - {}^tDQS_{OSC}(V, T) - OSC_{offset}]$$

Where ${}^tDQS2DQ(V, T)$ and ${}^tDQS_{OSC}(V, T)$ are determined over the same voltage and temperature conditions.

4. The runtime of the oscillator must be at least 200ns for determining ${}^tDQS_{OSC}(V, T)$.

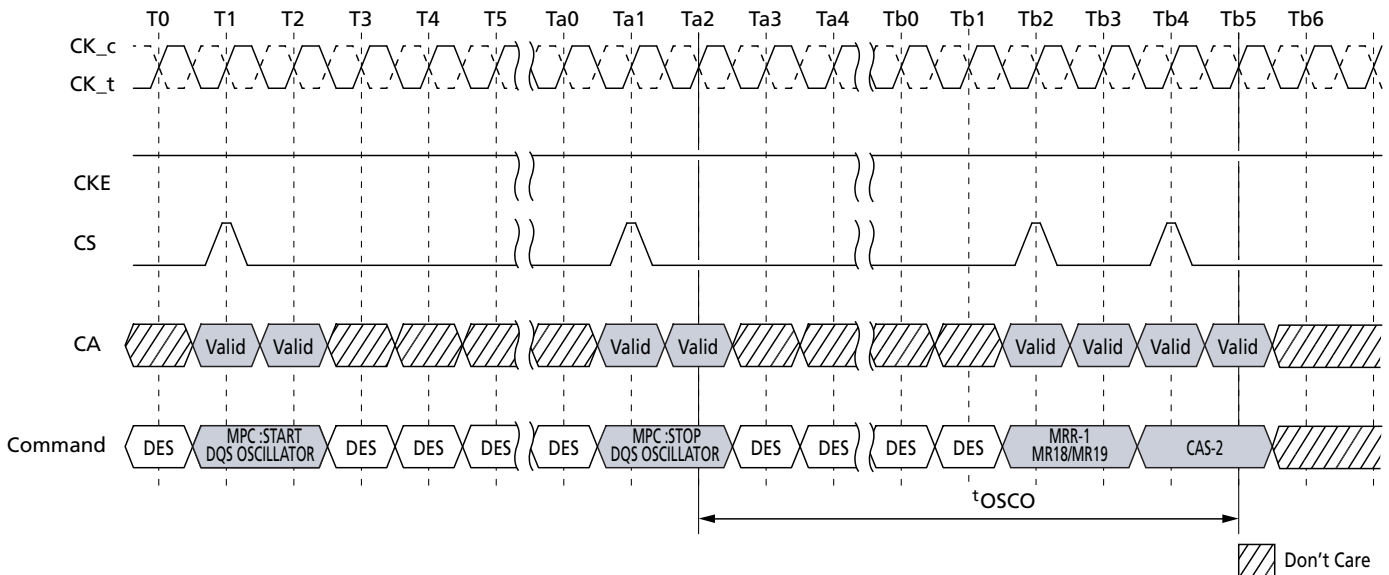
$${}^tDQS_{OSC}(V, T) = [\frac{Runtime}{2 \times Count}]$$

5. The input stimulus for tDQS2DQ will be consistent over voltage and temperature conditions.
6. The OSC_{offset} is the average difference of the endpoints across voltage and temperature.
7. These parameters are defined per channel.
8. ${}^tDQS2DQ(V, T)$ delay will be the average of DQS-to-DQ delay over the runtime period.

OSC Count Readout Time

OSC Stop to its counting value readout timing is shown in following figures.

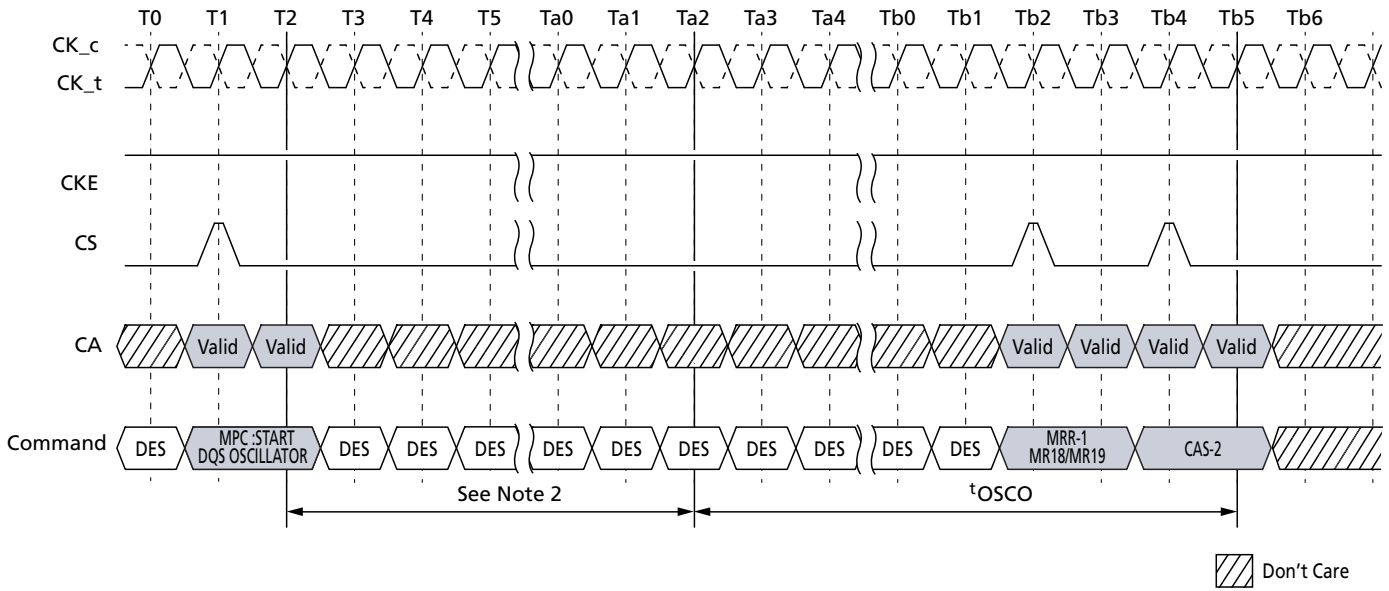
Figure 128: In Case of DQS Interval Oscillator is Stopped by MPC Command



Note: 1. DQS interval timer run time setting :MR23 OP[7:0] = 00000000b.



Figure 129: In Case of DQS Interval Oscillator is Stopped by DQS Interval Timer



- Notes: 1. DQS interval timer run time setting: MR23 OP[7:0] ≠ 00000000b.
2. Setting counts of MR23.

Table 121: DQS Interval Oscillator AC Timing

| Parameter | Symbol | MIN/MAX | Value | Unit |
|---|--------|---------|-----------------|------|
| Delay time from OSC stop to mode register readout | tOSCO | MIN | MAX(40ns, 8nCK) | ns |

- Note: 1. START DQS OSCILLATOR command is prohibited until tOSCO(MIN) is satisfied.



Thermal Offset

Because of tight thermal coupling, hot spots on an SOC can induce thermal gradients across the device. Because these hot spots may not be located near the thermal sensor, the temperature compensated self refresh (TCSR) circuit may not generate enough refresh cycles to guarantee memory retention. To address this shortcoming, the controller can provide a thermal offset that the memory can use to adjust its TCSR circuit to ensure reliable operation.

This thermal offset is provided through MR4 OP[6:5] to either or both channels (dual-channel devices). This temperature offset may modify refresh behaviour for the channel to which the offset is provided. It will take a maximum of 200 μ s to have the change reflected in MR4 OP[2:0] for the channel to which the offset is provided. If the induced thermal gradient from the device temperature sensor location to the hot spot location of the controller is greater than 15°C, self refresh mode will not reliably maintain memory contents.

To accurately determine the temperature gradient between the memory thermal sensor and the induced hot spot, the memory thermal sensor location must be provided to the controller.

Temperature Sensor

The device has a temperature sensor that can be read from MR4. This sensor can be used to determine the appropriate refresh rate, to determine whether AC timing de-rating is required at an elevated temperature range, and to monitor the operating temperature. Either the temperature sensor or the device T_{OPER} can be used to determine if operating temperature requirements are being met.

The device monitors device temperature and updates MR4 according to t_{TSI} . Upon exiting self refresh or power-down, the device temperature status bits shall be no older than t_{TSI} .

When using the temperature sensor, the actual device case temperature may be higher than the T_{OPER} specification that applies to standard or elevated temperature ranges. For example, T_{CASE} may be above 85°C when MR4[2:0] = b011. The device enables a 2°C temperature margin between the point when the device updates the MR4 value and the point when the controller reconfigures the system accordingly. When performing tight thermal coupling of the device to external hot spots, the maximum device temperature may be higher than indicated by MR4.

To ensure proper operation when using the temperature sensor, consider the following:

- TempGradient is the maximum temperature gradient experienced by the device at the temperature of interest over a range of 2°C.
- ReadInterval is the time period between MR4 reads from the system.
- TempSensorInterval (t_{TSI}) is the maximum delay between the internal updates of MR4.
- SysRespDelay is the maximum time between a read of MR4 and a response from the system.

In order to determine the required frequency of polling MR4, the system uses the TempGradient and the maximum response time of the system in the following equation:

$$\text{TempGradient} \times (\text{ReadInterval} + t_{TSI} + \text{SysRespDelay}) \leq 2^\circ\text{C}$$



Table 122: Temperature Sensor

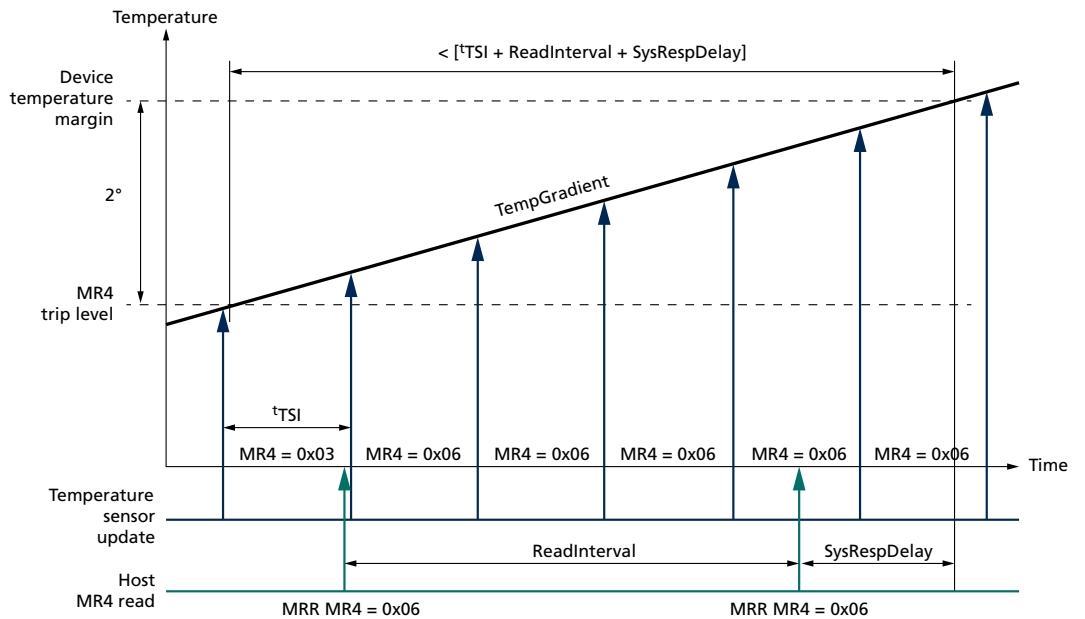
| Parameter | Symbol | Max/Min | Value | Unit |
|-----------------------------|--------------|---------|------------------|------|
| System temperature gradient | TempGradient | MAX | System Dependent | °C/s |
| MR4 read interval | ReadInterval | MAX | System Dependent | ms |
| Temperature sensor interval | t_{TSI} | MAX | 32 | ms |
| System response delay | SysRespDelay | MAX | System Dependent | ms |
| Device temperature margin | TempMargin | MAX | 2 | °C |

For example, if TempGradient is 10°C/s and the SysRespDelay is 1ms:

$$(10^{\circ}\text{C/s}) \times (\text{ReadInterval} + 32\text{ms} + 1\text{ms}) \leq 2^{\circ}\text{C}$$

In this case, ReadInterval shall be no greater than 167ms.

Figure 130: Temperature Sensor Timing



ZQ Calibration

The MPC command is used to initiate ZQ calibration, which calibrates the output driver impedance and CA/DQ ODT impedance across process, temperature, and voltage. ZQ calibration occurs in the background of device operation and is designed to eliminate any need for coordination between channels (that is, it allows for channel independence). ZQ calibration is required each time that the PU-Cal value (MR3-OP[0]) is changed. Additional ZQ CALIBRATION commands may be required as the voltage and temperature change in the system environment. CA ODT values (MR11-OP[6:4]) and DQ ODT values (MR11-OP[2:0]) may be changed without performing ZQ calibration, as long as the PU-Cal value doesn't change.



There are two ZQ calibration modes initiated with the MPC command: ZQCAL START and ZQCAL LATCH. ZQCAL START initiates the calibration procedure, and ZQCAL LATCH captures the result and loads it into the drivers.

A ZQCAL START command may be issued anytime the device is not in a power-down state. A ZQCAL LATCH command may be issued anytime outside of power-down after $t^{\prime}ZQCAL$ has expired and all DQ bus operations have completed. The CA bus must maintain a deselect state during $t^{\prime}ZQLAT$ to allow CA ODT calibration settings to be updated. The DQ calibration value will not be updated until ZQCAL LATCH is performed and $t^{\prime}ZQLAT$ has been met. The following mode register fields that modify I/O parameters cannot be changed following a ZQCAL START command and before $t^{\prime}ZQCAL$ has expired:

- PU-Cal (pull-up calibration V_{OH} point)
- PDDS (pull-down drive strength and Rx termination)
- DQ ODT (DQ ODT value)
- CA ODT (CA ODT value)

ZQCAL Reset

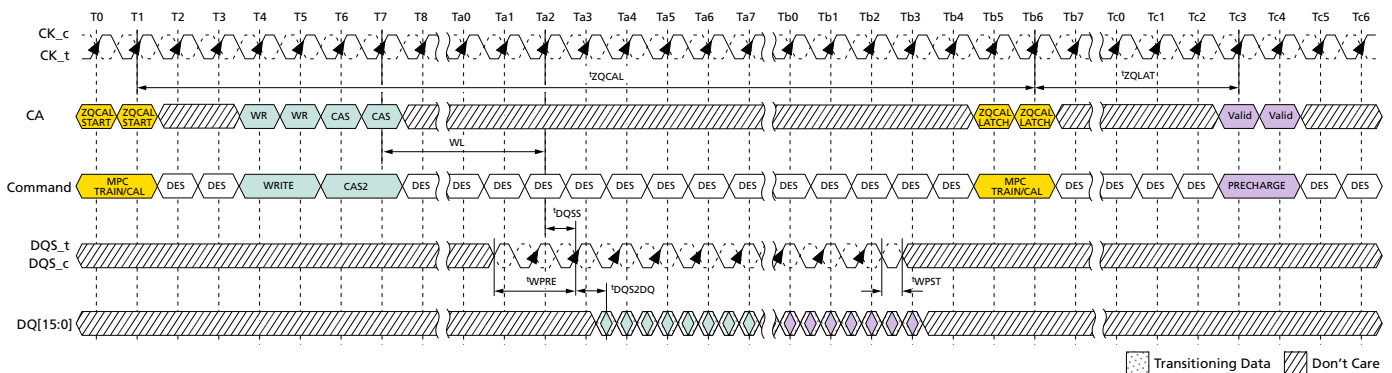
The ZQCAL RESET command resets the output impedance calibration to a default accuracy of $\pm 30\%$ across process, voltage, and temperature. This command is used to ensure output impedance accuracy to $\pm 30\%$ when ZQCAL START and ZQCAL LATCH commands are not used.

The ZQCAL RESET command is executed by writing MR10-OP[0] = 1B.

Table 123: ZQ Calibration Parameters

| Parameter | Symbol | Min/Max | Value | Unit |
|---|---------------------|---------|-----------------|---------|
| ZQCAL START to ZQCAL LATCH command interval | $t^{\prime}ZQCAL$ | MIN | 1 | μs |
| ZQCAL LATCH to next valid command interval | $t^{\prime}ZQLAT$ | MIN | MAX(30ns, 8nCK) | ns |
| ZQCAL RESET to next valid command interval | $t^{\prime}ZQRESET$ | MIN | MAX(50ns, 3nCK) | ns |

Figure 131: ZQCAL Timing



- Notes: 1. WRITE and PRECHARGE operations are shown for illustrative purposes. Any single or multiple valid commands may be executed within the $t^{\prime}ZQCAL$ time and prior to latching the results.



2. Before the ZQCAL LATCH command can be executed, any prior commands that utilize the DQ bus must have completed. WRITE commands with DQ termination must be given enough time to turn off the DQ ODT before issuing the ZQCAL LATCH command. See the ODT section for ODT timing.

Multichannel Considerations

The device includes a single ZQ pin and associated ZQ calibration circuitry. Calibration values from this circuit will be used by both channels according to the following protocol:

- The ZQCAL START command can be issued to either or both channels.
- The ZQCAL START command can be issued when either or both channels are executing other commands, and other commands can be issued during t^{ZQCAL} .
- The ZQCAL START command can be issued to both channels simultaneously.
- The ZQCAL START command will begin the calibration unless a previously requested ZQ calibration is in progress.
- If the ZQCAL START command is received while a ZQ calibration is in progress, the command will be ignored and the in-progress calibration will not be interrupted.
- The ZQCAL LATCH command is required for each channel.
- The ZQCAL LATCH command can be issued to both channels simultaneously.
- The ZQCAL LATCH command will latch results of the most recent ZQCAL START command provided t^{ZQCAL} has been met.
- ZQCAL LATCH commands that do not meet t^{ZQCAL} will latch the results of the most recently completed ZQ calibration.
- The ZQRESET MRW commands will only reset the calibration values for the channel issuing the command.

In compliance with complete channel independence, either channel may issue ZQCAL START and ZQCAL LATCH commands as needed without regard to the state of the other channel.

ZQ External Resistor, Tolerance, and Capacitive Loading

To use the ZQ CALIBRATION function, a 240 ohms, $\pm 1\%$ tolerance external resistor must be connected between the ZQ pin and V_{DDQ} .

If the system configuration shares the CA bus to form a x32 (or wider) channel, the ZQ pin of each die's x16 channel must use a separate ZQCAL resistor.

If the system configuration has more than one rank, and if the ZQ pins of both ranks are attached to a single resistor, then the SDRAM controller must ensure that the ZQCAL's don't overlap.

The total capacitive loading on the ZQ pin must be limited to 25pF. For example, if a system configuration shares a CA bus between n channels to form an n x16 wide bus, and no means are available to control the ZQCAL separately for each channel (that is, separate CS, CKE, or CK), then each x16 channel must have a separate ZQCAL resistor. For a x32, two-rank system, each x16 channel must have its own ZQCAL resistor, but the ZQCAL resistor can be shared between ranks on each x16 channel. In this configuration, the CS signal can be used to ensure that the ZQCAL commands for Rank[0] and Rank[1] don't overlap.



Frequency Set Points

Frequency set points enable the CA bus to be switched between two differing operating frequencies with changes in voltage swings and termination values, without ever being in an untrained state, which could result in a loss of communication to the device. This is accomplished by duplicating all CA bus mode register parameters, as well as other mode register parameters commonly changed with operating frequency.

These duplicated registers form two sets that use the same mode register addresses, with read/write access controlled by MR bit FSP-WR (frequency set point write/read) and the operating point controlled by MR bit FSP-OP (FREQUENCY SET POINT operation). Changing the FSP-WR bit enables MR parameters to be changed for an alternate frequency set point without affecting the current operation.

Once all necessary parameters have been written to the alternate set point, changing the FSP-OP bit will switch operation to use all of the new parameters simultaneously (within t_{FC}), eliminating the possibility of a loss of communication that could be caused by a partial configuration change.

Parameters which have two physical registers controlled by FSP-WR and FSP-OP include:

Table 124: Mode Register Function with Two Physical Registers

| MR Number | Operand | Function | Notes |
|-----------|---------|--|-------|
| MR1 | OP[1:0] | BL (Burst length) | |
| | OP[2] | WR-PRE (Write preamble length) | |
| | OP[3] | RD-PRE (Read preamble type) | |
| | OP[6:4] | n WR (Write-recovery for AUTO PRECHARGE command) | |
| | OP[7] | RD-PST (Read postamble length) | |
| MR2 | OP[2:0] | RL (READ latency) | |
| | OP[5:3] | WL (WRITE latency) | |
| | OP[6] | WLS (WRITE latency set) | |
| MR3 | OP[0] | PU-CAL (Pull-up calibration point) | 1 |
| | OP[1] | WR-PST (Write postamble length) | |
| | OP[5:3] | PDDS (Pull-down drive strength) | |
| | OP[6] | DBI-RD (DBI-read enable) | |
| | OP[7] | DBI-WR (DBI-write enable) | |
| MR11 | OP[2:0] | DQ ODT (DQ bus receiver on-die termination) | |
| | OP[6:4] | CA ODT (CA bus receiver on-die termination) | |
| MR12 | OP[5:0] | $V_{REF(CA)}$ ($V_{REF(CA)}$ setting) | |
| | OP[6] | VR_{CA} ($V_{REF(CA)}$ range) | |
| MR14 | OP[5:0] | $V_{REF(DQ)}$ ($V_{REF(DQ)}$ setting) | |
| | OP[6] | VR_{DQ} ($V_{REF(DQ)}$ range) | |


Table 124: Mode Register Function with Two Physical Registers (Continued)

| MR Number | Operand | Function | Notes |
|-----------|---------|---|-------|
| MR22 | OP[2:0] | SOC ODT (Controller ODT value for V_{OH} calibration) | |
| | OP[3] | ODTE-CK (CK ODT enabled for non-terminating rank) | |
| | OP[4] | ODTE-CS (CS ODT enable for non-terminating rank) | |
| | OP[5] | ODTD-CA (CA ODT termination disable) | |

Note: 1. PU-CAL setting is required as the same value for both Ch. A and Ch. B before issuing ZQCAL START command. See Mode Register Definition section for more details.

Table below shows how the two mode registers for each of the parameters above can be modified by setting the appropriate FSP-WR value, and how device operation can be switched between operating points by setting the appropriate FSP-OP value. The FSP-WR and FSP-OP functions operate completely independently.

Table 125: Relation Between MR Setting and DRAM Operation

| Function | MR# and Operand | Data | Operation | Notes |
|----------|-----------------|-------------|---|-------|
| FSP-WR | MR13 OP[6] | 0 (default) | Data write to mode register N for FSP-OP[0] by MRW command. | 1 |
| | | 1 | Data write to mode register N for FSP-OP[1] by MRW command. | |
| FSP-OP | MR13 OP[7] | 0 (default) | DRAM operates with mode register N for FSP-OP[0] setting. | 2 |
| | | 1 | DRAM operates with mode register N for FSP-OP[1] setting. | |

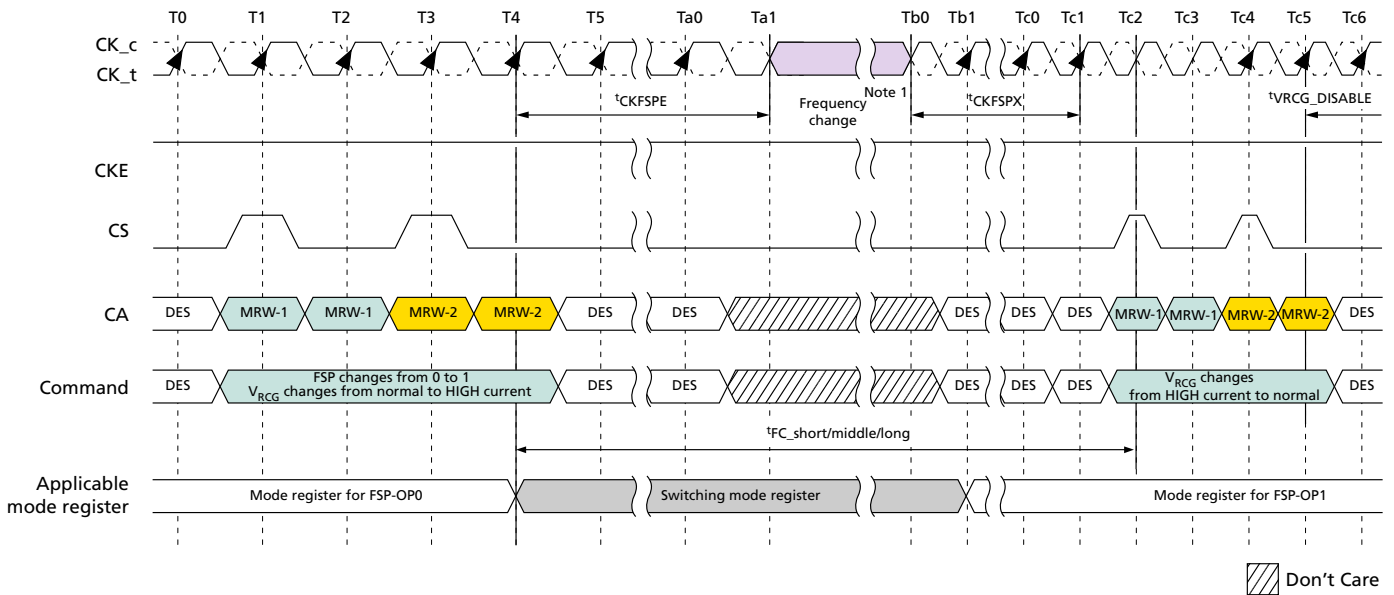
Notes: 1. FSP-WR stands for frequency set point write/read.
2. FSP-OP stands for frequency set point operating point.

Frequency Set Point Update Timing

The frequency set point update timing is shown below. When changing the frequency set point via MR13 OP[7], the V_{RCG} setting: MR13 OP[3] have to be changed into V_{REF} fast response (high current) mode at the same time. After frequency change time (t_{FC}) is satisfied, V_{RCG} can be changed into normal operation mode via MR13 OP[3].



Figure 132: Frequency Set Point Switching Timing



Note: 1. For frequency change during frequency set point switching, refer to input Clock Stop and Frequency Change section.

Table 126: Frequency Set Point AC Timing

| Parameter | Symbol | Min/Max | Data Rate | | | | Unit | Notes |
|---|------------------|---------|------------------|------|------|------|------|-------|
| | | | 1600 | 3200 | 3733 | 4267 | | |
| Frequency set point switching time | t_{FC_short} | MIN | 200 | | | | ns | 1 |
| | t_{FC_middle} | MIN | 200 | | | | ns | |
| | t_{FC_long} | MIN | 250 | | | | ns | |
| Valid clock requirement after entering FSP change | t_{CKFSPE} | MIN | MAX(7.5ns, 4nCK) | | | | - | |
| Valid clock requirement before first valid command after FSP change | t_{CKFSPX} | MIN | MAX(7.5ns, 4nCK) | | | | - | |

Note: 1. Frequency set point switching time depends on value of $V_{REF(CA)}$ setting: MR12 OP[5:0] and $V_{REF(CA)}$ range: MR12 OP[6] of FSP-OP 0 and 1. The details are shown in table below. Additionally change of frequency set point may affect $V_{REF(DQ)}$ setting. Settling time of $V_{REF(DQ)}$ level is the same as $V_{REF(CA)}$ level.

Table 127: t_{FC} Value Mapping

| Application | Step Size | | Range | |
|-----------------|--------------|--|--------------|------------|
| | From FSP-OP0 | To FSP-OP1 | From FSP-OP0 | To FSP-OP1 |
| t_{FC_short} | Base | A single step size increment/decrement | Base | No change |


Table 127: t_{FC} Value Mapping (Continued)

| Application | Step Size | | Range | |
|------------------|--------------|---|--------------|------------|
| | From FSP-OP0 | To FSP-OP1 | From FSP-OP0 | To FSP-OP1 |
| t_{FC_middle} | Base | Two or more step size increment/decrement | Base | No change |
| t_{FC_long} | – | – | Base | Change |

Note: 1. As well as change from FSP-OP1 to FSP-OP0.

Table 128: t_{FC} Value Mapping: Example

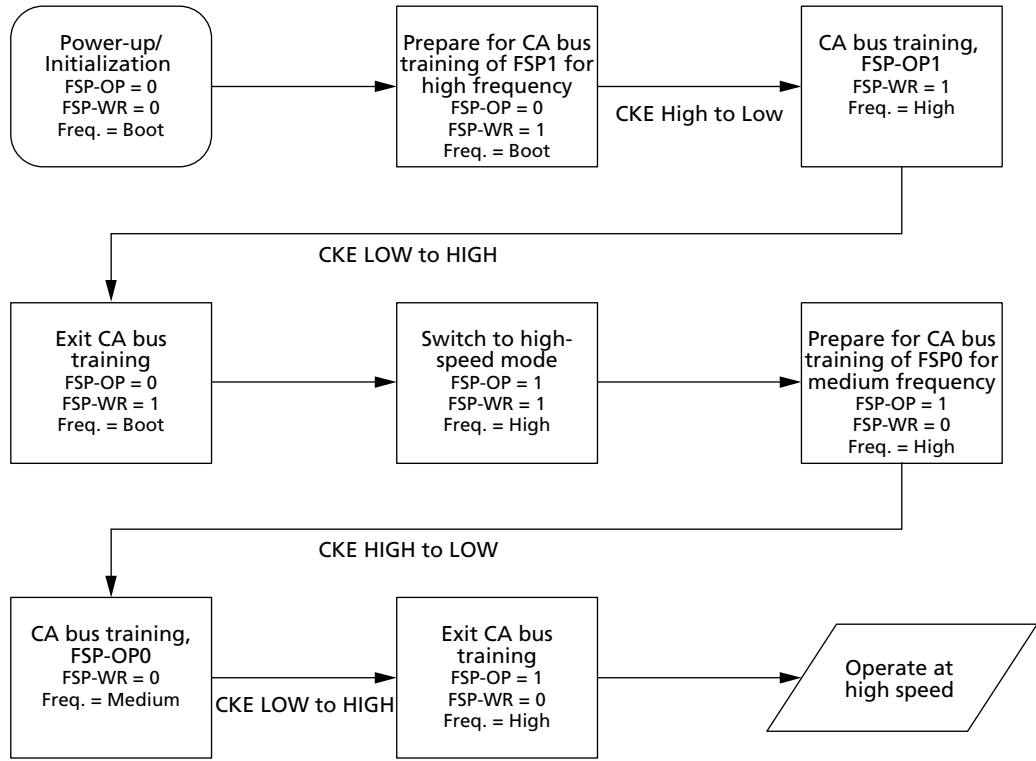
| Case | From/To | FSP-OP: MR13 OP[7] | $V_{REF(CA)}$ Setting: MR12: OP[5:0] | $V_{REF(CA)}$ Range: MR12 OP[6] | Application | Notes |
|------|---------|-----------------------|---|------------------------------------|------------------|-------|
| 1 | From | 0 | 001100 | 0 | t_{FC_short} | 1 |
| | To | 1 | 001101 | 0 | | |
| 2 | From | 0 | 001100 | 0 | t_{FC_middle} | 2 |
| | To | 1 | 001110 | 0 | | |
| 3 | From | 0 | Don't Care | 0 | t_{FC_long} | 3 |
| | To | 1 | Don't Care | 1 | | |

- Notes:
1. A single step size increment/decrement for $V_{REF(CA)}$ setting value.
 2. Two or more step size increment/decrement for $V_{REF(CA)}$ setting value.
 3. $V_{REF(CA)}$ range is changed. In this case, changing $V_{REF(CA)}$ setting doesn't affect t_{FC} value.

The LPDDR4 SDRAM defaults to FSP-OP[0] at power-up. Both set points default to settings needed to operate in un-terminated, low-frequency environments. To enable the device to operate at higher frequencies, Command bus training mode should be utilized to train the alternate frequency set point. See Command Bus Training section for more details on this training mode.

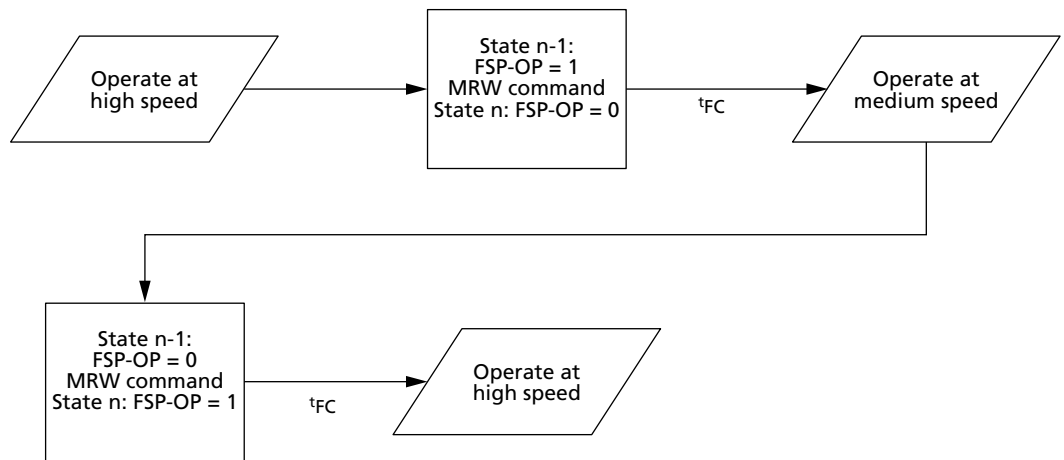


Figure 133: Training for Two Frequency Set Points



Once both of the frequency set points have been trained, switching between points can be performed with a single MRW followed by waiting for time t_{FC} .

Figure 134: Example of Switching Between Two Trained Frequency Set Points

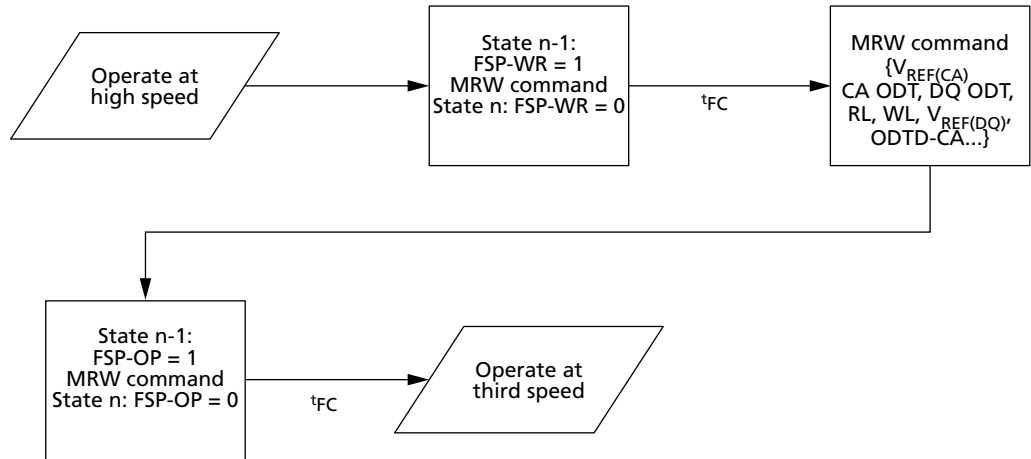


Switching to a third (or more) set point can be accomplished if the memory controller has stored the previously-trained values (in particular the $V_{REF(CA)}$ calibration value) and rewrites these to the alternate set point before switching FSP-OP.



200b: x32 LPDDR4 SDRAM Pull-Up and Pull-Down Characteristics and Calibration

Figure 135: Example of Switching to a Third Trained Frequency Set Point



Pull-Up and Pull-Down Characteristics and Calibration

Table 129: Pull-Down Driver Characteristics – ZQ Calibration

| $R_{ONPD,nom}$ | Register | Min | Nom | Max | Unit |
|----------------|---------------|------|-----|------|------------|
| 40 ohms | R_{ON40PD} | 0.90 | 1.0 | 1.10 | $R_{ZQ}/6$ |
| 48 ohms | R_{ON48PD} | 0.90 | 1.0 | 1.10 | $R_{ZQ}/5$ |
| 60 ohms | R_{ON60PD} | 0.90 | 1.0 | 1.10 | $R_{ZQ}/4$ |
| 80 ohms | R_{ON80PD} | 0.90 | 1.0 | 1.10 | $R_{ZQ}/3$ |
| 120 ohms | $R_{ON120PD}$ | 0.90 | 1.0 | 1.10 | $R_{ZQ}/2$ |
| 240 ohms | $R_{ON240PD}$ | 0.90 | 1.0 | 1.10 | $R_{ZQ}/1$ |

Note: 1. All value are after ZQ calibration. Without ZQ calibration, R_{ONPD} values are $\pm 30\%$.

Table 130: Pull-Up Characteristics – ZQ Calibration

| $V_{OHPU,nom}$ | $V_{OH,nom}$ | Min | Nom | Max | Unit |
|----------------|--------------|------|-----|------|--------------|
| $V_{DDQ}/2.5$ | 440 | 0.90 | 1.0 | 1.10 | $V_{OH,nom}$ |
| $V_{DDQ}/3$ | 367 | 0.90 | 1.0 | 1.10 | $V_{OH,nom}$ |

Notes: 1. All value are after ZQ calibration. Without ZQ calibration, R_{ONPD} values are $\pm 30\%$.
2. $V_{OH,nom}$ (mV) values are based on a nominal $V_{DDQ} = 1.1V$.

Table 131: Valid Calibration Points

| V_{OHPU} | ODT Value | | | | | |
|---------------|-----------|-------|-------|-----|-----|-----|
| | 240 | 120 | 80 | 60 | 48 | 40 |
| $V_{DDQ}/2.5$ | Valid | Valid | Valid | DNU | DNU | DNU |



Table 131: Valid Calibration Points (Continued)

| V _{OHPU} | ODT Value | | | | | |
|---------------------|-----------|-------|-------|-------|-------|-------|
| | 240 | 120 | 80 | 60 | 48 | 40 |
| V _{DDQ} /3 | Valid | Valid | Valid | Valid | Valid | Valid |

- Notes:
1. After the output is calibrated for a given V_{OH,nom} calibration point, the ODT value may be changed without recalibration.
 2. If the V_{OH,nom} calibration point is changed, then recalibration is required.
 3. DNU = Do not use.

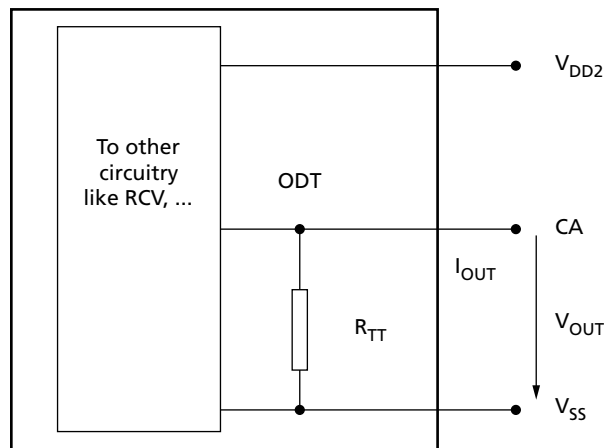
On-Die Termination for the Command/Address Bus

The on-die termination (ODT) feature allows the device to turn on/off termination resistance for CK_t, CK_c, CS, and CA[5:0] signals without the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to turn on and off termination resistance for any target DRAM devices via the mode register setting.

A simple functional representation of the DRAM ODT feature is shown below.

Figure 136: ODT for CA

$$R_{TT} = \frac{V_{OUT}}{|I_{OUT}|}$$



ODT Mode Register and ODT State Table

ODT termination values are set and enabled via MR11. The CA bus (CK_t, CK_c, CS, CA[5:0]) ODT resistance values are set by MR11 OP[6:4]. The default state for the CA is ODT disabled.

ODT is applied on the CA bus to the CK_t, CK_c, CS, and CA signals. The CA ODT of the device is designed to enable one rank to terminate the entire command bus in a multi-rank system, so only one termination load will be present even if multiple devices are



200b: x32 LPDDR4 SDRAM On-Die Termination for the Command/Address Bus

sharing the command signals. For this reason, CA ODT remains on, even when the device is in the power-down or self refresh power-down state.

The die has a bond pad (ODT_CA) for multirank operations. When the ODT_CA pad is LOW, the die will not terminate the CA bus regardless of the state of the mode register CA ODT bits (MR11 OP[6:4]). If, however, the ODT_CA bond pad is HIGH and the mode register CA ODT bits are enabled, the die will terminate the CA bus with the ODT values found in MR11 OP[6:4]. In a multirank system, the terminating rank should be trained first, followed by the non-terminating rank(s).

Table 132: Command Bus ODT State

| CA ODT MR11[6:4] | ODT_CA Bond Pad | ODTD-CA MR22 OP[5] | ODTE-CK MR22 OP[3] | ODTE-CS MR22 OP[4] | ODT State for CA | ODT State for CK | ODT State for CS |
|-----------------------|--------------------|-----------------------|-----------------------|-----------------------|---------------------|---------------------|---------------------|
| Disabled ¹ | Valid ² | Valid ³ | Valid ³ | Valid ³ | Off | Off | Off |
| Valid ³ | 0 | Valid ³ | 0 | 0 | Off | Off | Off |
| Valid ³ | 0 | Valid ³ | 0 | 1 | Off | Off | On |
| Valid ³ | 0 | Valid ³ | 1 | 0 | Off | On | Off |
| Valid ³ | 0 | Valid ³ | 1 | 1 | Off | On | On |
| Valid ³ | 1 | 0 | Valid ³ | Valid ³ | On | On | On |
| Valid ³ | 1 | 1 | Valid ³ | Valid ³ | Off | On | On |

- Notes:
1. Default value.
 2. Valid = H or L (a defined logic level)
 3. Valid = 0 or 1.
 4. The state of ODT_CA is not changed when the device enters power-down mode. This maintains termination for alternate ranks in multirank systems.

ODT Mode Register and ODT Characteristics

Table 133: ODT DC Electrical Characteristics – up to 3200 Mbps

R_{ZQ} = 240Ω ±1% over entire operating range after calibration

| MR11 OP[6:4] | R _{TT} | V _{OUT} | Min | Nom | Max | Unit | Notes |
|--------------|-----------------|---|-----|-----|-----|--------------------|-------|
| 001b | 240Ω | V _{OL(DC)} = 0.1 × V _{DD2} | 0.8 | 1.0 | 1.1 | R _{ZQ} /1 | 1, 2 |
| | | V _{OM(DC)} = 0.33 × V _{DD2} | 0.9 | 1.0 | 1.1 | | |
| | | V _{OH(DC)} = 0.5 × V _{DD2} | 0.9 | 1.0 | 1.2 | | |
| 010b | 120Ω | V _{OL(DC)} = 0.1 × V _{DD2} | 0.8 | 1.0 | 1.1 | R _{ZQ} /2 | 1, 2 |
| | | V _{OM(DC)} = 0.33 × V _{DD2} | 0.9 | 1.0 | 1.1 | | |
| | | V _{OH(DC)} = 0.5 × V _{DD2} | 0.9 | 1.0 | 1.2 | | |
| 011b | 80Ω | V _{OL(DC)} = 0.1 × V _{DD2} | 0.8 | 1.0 | 1.1 | R _{ZQ} /3 | 1, 2 |
| | | V _{OM(DC)} = 0.33 × V _{DD2} | 0.9 | 1.0 | 1.1 | | |
| | | V _{OH(DC)} = 0.5 × V _{DD2} | 0.9 | 1.0 | 1.2 | | |
| 100b | 60Ω | V _{OL(DC)} = 0.1 × V _{DD2} | 0.8 | 1.0 | 1.1 | R _{ZQ} /4 | 1, 2 |
| | | V _{OM(DC)} = 0.33 × V _{DD2} | 0.9 | 1.0 | 1.1 | | |
| | | V _{OH(DC)} = 0.5 × V _{DD2} | 0.9 | 1.0 | 1.2 | | |



200b: x32 LPDDR4 SDRAM On-Die Termination for the Command/Address Bus

Table 133: ODT DC Electrical Characteristics – up to 3200 Mbps (Continued)
 $R_{ZQ} = 240\Omega \pm 1\%$ over entire operating range after calibration

| MR11 OP[6:4] | R _{TT} | V _{OUT} | Min | Nom | Max | Unit | Notes |
|-------------------------------------|-----------------|------------------------------------|-----|-----|-----|--------------------|---------|
| 101b | 48Ω | $V_{OL(DC)} = 0.1 \times V_{DD2}$ | 0.8 | 1.0 | 1.1 | R _{ZQ} /5 | 1, 2 |
| | | $V_{OM(DC)} = 0.33 \times V_{DD2}$ | 0.9 | 1.0 | 1.1 | | |
| | | $V_{OH(DC)} = 0.5 \times V_{DD2}$ | 0.9 | 1.0 | 1.2 | | |
| 110b | 40Ω | $V_{OL(DC)} = 0.1 \times V_{DD2}$ | 0.8 | 1.0 | 1.1 | R _{ZQ} /6 | 1, 2 |
| | | $V_{OM(DC)} = 0.33 \times V_{DD2}$ | 0.9 | 1.0 | 1.1 | | |
| | | $V_{OH(DC)} = 0.5 \times V_{DD2}$ | 0.9 | 1.0 | 1.2 | | |
| Mismatch, CA -CA within clock group | | $0.33 \times V_{DD2}$ | – | – | 2 | % | 1, 2, 3 |

- Notes:
- The tolerance limits are specified after calibration with stable temperature and voltage. To understand the behavior of the tolerance limits when voltage or temperature changes after calibration, see the section on voltage and temperature sensitivity.
 - Pull-down ODT resistors are recommended to be calibrated at $0.33 \times V_{DD2}$. Other calibration points may be required to achieve the linearity specification shown above, for example, calibration at $0.5 \times V_{DD2}$ and $0.1 \times V_{DD2}$.
 - CA to CA mismatch within clock group variation for a given component including CK_t, CK_c, and CS (characterized).

$$\text{CA-to-CA mismatch} = \frac{R_{ODT}(\text{MAX}) - R_{ODT}(\text{MIN})}{R_{ODT}(\text{AVG})}$$

Table 134: ODT DC Electrical Characteristics – Beyond 3200 Mbps
 $R_{ZQ} = 240\Omega \pm 1\%$ over entire operating range after calibration

| MR11 OP[6:4] | R _{TT} | V _{OUT} | Min | Nom | Max | Unit | Notes |
|--------------|-----------------|------------------------------------|-----|-----|-----|--------------------|-------|
| 001b | 240Ω | $V_{OL(DC)} = 0.1 \times V_{DD2}$ | 0.8 | 1.0 | 1.1 | R _{ZQ} /1 | 1, 2 |
| | | $V_{OM(DC)} = 0.33 \times V_{DD2}$ | 0.9 | 1.0 | 1.1 | | |
| | | $V_{OH(DC)} = 0.5 \times V_{DD2}$ | 0.9 | 1.0 | 1.3 | | |
| 010b | 120Ω | $V_{OL(DC)} = 0.1 \times V_{DD2}$ | 0.8 | 1.0 | 1.1 | R _{ZQ} /2 | 1, 2 |
| | | $V_{OM(DC)} = 0.33 \times V_{DD2}$ | 0.9 | 1.0 | 1.1 | | |
| | | $V_{OH(DC)} = 0.5 \times V_{DD2}$ | 0.9 | 1.0 | 1.3 | | |
| 011b | 80Ω | $V_{OL(DC)} = 0.1 \times V_{DD2}$ | 0.8 | 1.0 | 1.1 | R _{ZQ} /3 | 1, 2 |
| | | $V_{OM(DC)} = 0.33 \times V_{DD2}$ | 0.9 | 1.0 | 1.1 | | |
| | | $V_{OH(DC)} = 0.5 \times V_{DD2}$ | 0.9 | 1.0 | 1.3 | | |
| 100b | 60Ω | $V_{OL(DC)} = 0.1 \times V_{DD2}$ | 0.8 | 1.0 | 1.1 | R _{ZQ} /4 | 1, 2 |
| | | $V_{OM(DC)} = 0.33 \times V_{DD2}$ | 0.9 | 1.0 | 1.1 | | |
| | | $V_{OH(DC)} = 0.5 \times V_{DD2}$ | 0.9 | 1.0 | 1.3 | | |
| 101b | 48Ω | $V_{OL(DC)} = 0.1 \times V_{DD2}$ | 0.8 | 1.0 | 1.1 | R _{ZQ} /5 | 1, 2 |
| | | $V_{OM(DC)} = 0.33 \times V_{DD2}$ | 0.9 | 1.0 | 1.1 | | |
| | | $V_{OH(DC)} = 0.5 \times V_{DD2}$ | 0.9 | 1.0 | 1.3 | | |



Table 134: ODT DC Electrical Characteristics – Beyond 3200 Mbps (Continued)

$R_{ZQ} = 240\Omega \pm 1\%$ over entire operating range after calibration

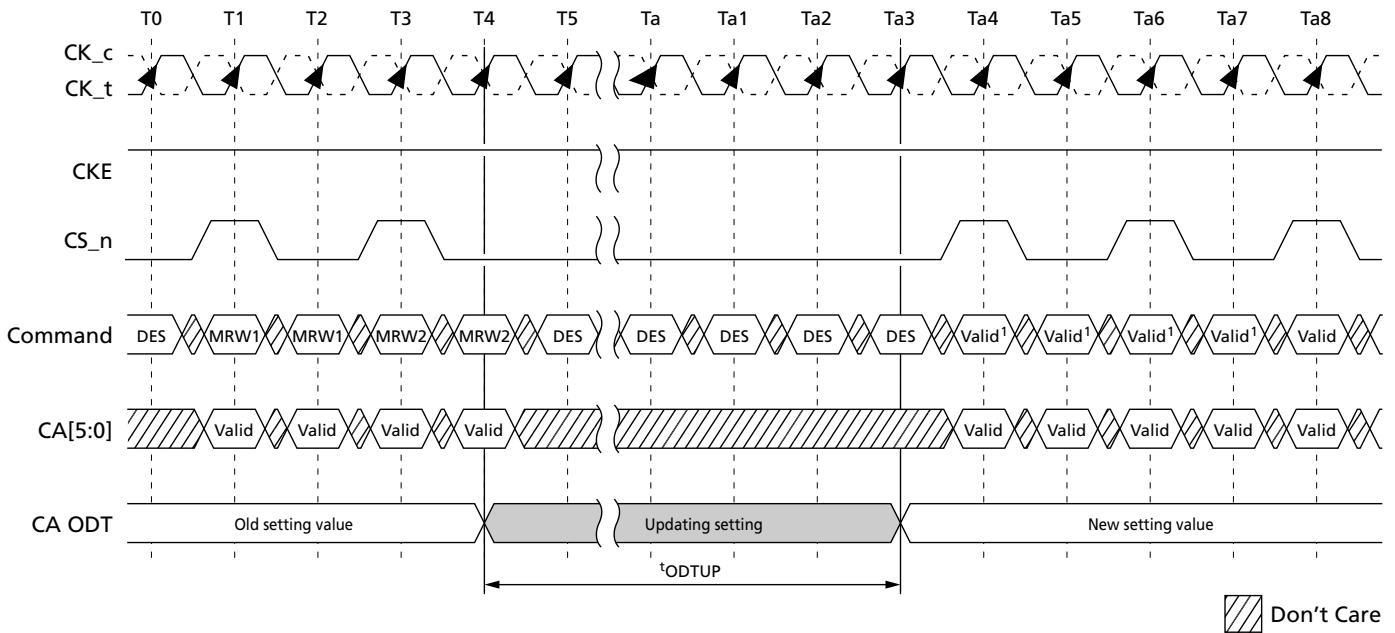
| MR11 OP[6:4] | R_{TT} | V_{OUT} | Min | Nom | Max | Unit | Notes |
|-------------------------------------|-------------|------------------------------------|-----|-----|-----|------------|---------|
| 110b | 40 Ω | $V_{OL(DC)} = 0.1 \times V_{DD2}$ | 0.8 | 1.0 | 1.1 | $R_{ZQ}/6$ | 1, 2 |
| | | $V_{OM(DC)} = 0.33 \times V_{DD2}$ | 0.9 | 1.0 | 1.1 | | |
| | | $V_{OH(DC)} = 0.5 \times V_{DD2}$ | 0.9 | 1.0 | 1.3 | | |
| Mismatch, CA -CA within clock group | | $0.33 \times V_{DD2}$ | – | – | 2 | % | 1, 2, 3 |

- Notes:
1. The tolerance limits are specified after calibration with stable temperature and voltage. To understand the behavior of the tolerance limits when voltage or temperature changes after calibration, see the section on voltage and temperature sensitivity.
 2. Pull-down ODT resistors are recommended to be calibrated at $0.33 \times V_{DD2}$. Other calibration points may be required to achieve the linearity specification shown above, e.g. calibration at $0.5 \times V_{DD2}$ and $0.1 \times V_{DD2}$.
 3. CA to CA mismatch within clock group variation for a given component including CK_t, CK_c, and CS (characterized).

$$\text{CA-to-CA mismatch} = \frac{R_{ODT}(\text{MAX}) - R_{ODT}(\text{MIN})}{R_{ODT}(\text{AVG})}$$

ODT for CA Update Time

Figure 137: ODT for CA Setting Update Timing in 4-Clock Cycle Command





DQ On-Die Termination

On-die termination (ODT) is a feature that allows the device to turn on/off termination resistance for each DQ, DQS, and DMI signal without the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to turn on and off termination resistance for any target DRAM devices during WRITE or MASK WRITE operation.

The ODT feature is off and cannot be supported in power-down and self refresh modes.

The switch is enabled by the internal ODT control logic, which uses the WRITE-1 or MASK WRITE-1 command and other mode register control information. The value of R_{TT} is determined by the MR bits.

$$R_{TT} = \frac{V_{OUT}}{|I_{OUT}|}$$

Figure 138: Functional Representation of DQ ODT

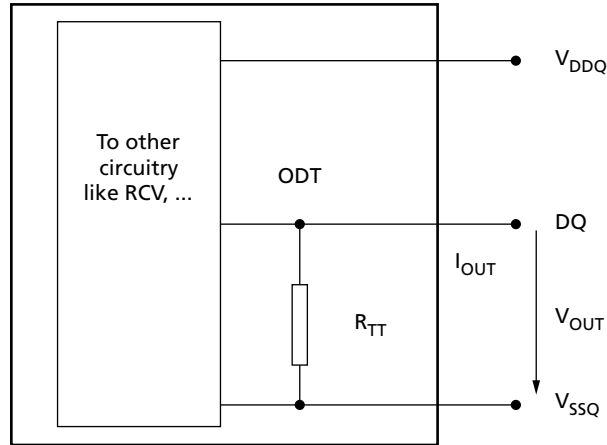


Table 135: ODT DC Electrical Characteristics – up to 3200 Mbps

$R_{ZQ} = 240\Omega \pm 1\%$ over entire operating range after calibration

| MR11 OP[2:0] | R_{TT} | V_{OUT} | Min | Nom | Max | Unit | Notes |
|--------------|--------------|------------------------------------|-----|-----|-----|------------|-------|
| 001b | 240 Ω | $V_{OL(DC)} = 0.1 \times V_{DDQ}$ | 0.8 | 1.0 | 1.1 | $R_{ZQ}/1$ | 1, 2 |
| | | $V_{OM(DC)} = 0.33 \times V_{DDQ}$ | 0.9 | 1.0 | 1.1 | | |
| | | $V_{OH(DC)} = 0.5 \times V_{DDQ}$ | 0.9 | 1.0 | 1.2 | | |
| 010b | 120 Ω | $V_{OL(DC)} = 0.1 \times V_{DDQ}$ | 0.8 | 1.0 | 1.1 | $R_{ZQ}/2$ | 1, 2 |
| | | $V_{OM(DC)} = 0.33 \times V_{DDQ}$ | 0.9 | 1.0 | 1.1 | | |
| | | $V_{OH(DC)} = 0.5 \times V_{DDQ}$ | 0.9 | 1.0 | 1.2 | | |
| 011b | 80 Ω | $V_{OL(DC)} = 0.1 \times V_{DDQ}$ | 0.8 | 1.0 | 1.1 | $R_{ZQ}/3$ | 1, 2 |
| | | $V_{OM(DC)} = 0.33 \times V_{DDQ}$ | 0.9 | 1.0 | 1.1 | | |
| | | $V_{OH(DC)} = 0.5 \times V_{DDQ}$ | 0.9 | 1.0 | 1.2 | | |



Table 135: ODT DC Electrical Characteristics – up to 3200 Mbps (Continued)

$R_{ZQ} = 240\Omega \pm 1\%$ over entire operating range after calibration

| MR11 OP[2:0] | R _{TT} | V _{OUT} | Min | Nom | Max | Unit | Notes |
|---|-----------------|------------------------------------|-----|-----|-----|--------------------|---------|
| 100b | 60Ω | $V_{OL(DC)} = 0.1 \times V_{DDQ}$ | 0.8 | 1.0 | 1.1 | R _{ZQ} /4 | 1, 2 |
| | | $V_{OM(DC)} = 0.33 \times V_{DDQ}$ | 0.9 | 1.0 | 1.1 | | |
| | | $V_{OH(DC)} = 0.5 \times V_{DDQ}$ | 0.9 | 1.0 | 1.2 | | |
| 101b | 48Ω | $V_{OL(DC)} = 0.1 \times V_{DDQ}$ | 0.8 | 1.0 | 1.1 | R _{ZQ} /5 | 1, 2 |
| | | $V_{OM(DC)} = 0.33 \times V_{DDQ}$ | 0.9 | 1.0 | 1.1 | | |
| | | $V_{OH(DC)} = 0.5 \times V_{DDQ}$ | 0.9 | 1.0 | 1.2 | | |
| 110b | 40Ω | $V_{OL(DC)} = 0.1 \times V_{DDQ}$ | 0.8 | 1.0 | 1.1 | R _{ZQ} /6 | 1, 2 |
| | | $V_{OM(DC)} = 0.33 \times V_{DDQ}$ | 0.9 | 1.0 | 1.1 | | |
| | | $V_{OH(DC)} = 0.5 \times V_{DDQ}$ | 0.9 | 1.0 | 1.2 | | |
| Mismatch error, DQ-to-DQ within a channel | | $0.33 \times V_{DDQ}$ | – | – | 2 | % | 1, 2, 3 |

- Notes:
1. The ODT tolerance limits are specified after calibration with stable temperature and voltage. To understand the behavior of the tolerance limits when voltage or temperature changes after calibration, see the following section on voltage and temperature sensitivity.
 2. Pull-down ODT resistors are recommended to be calibrated at $0.33 \times V_{DDQ}$. Other calibration points may be required to achieve the linearity specification shown above, (for example, calibration at $0.5 \times V_{DDQ}$ and $-0.1 \times V_{DDQ}$).
 3. DQ-to-DQ mismatch within byte variation for a given component, including DQS (characterized).

$$\text{DQ-to-DQ mismatch} = \frac{R_{ODT}(\text{MAX}) - R_{ODT}(\text{MIN})}{R_{ODT}(\text{AVG})}$$

Table 136: ODT DC Electrical Characteristics – Beyond 3200 Mbps

$R_{ZQ} = 240\Omega \pm 1\%$ over entire operating range after calibration

| MR11 OP[2:0] | R _{TT} | V _{OUT} | Min | Nom | Max | Unit | Notes |
|--------------|-----------------|------------------------------------|-----|-----|-----|--------------------|-------|
| 001b | 240Ω | $V_{OL(DC)} = 0.1 \times V_{DDQ}$ | 0.8 | 1.0 | 1.1 | R _{ZQ} /1 | 1, 2 |
| | | $V_{OM(DC)} = 0.33 \times V_{DDQ}$ | 0.9 | 1.0 | 1.1 | | |
| | | $V_{OH(DC)} = 0.5 \times V_{DDQ}$ | 0.9 | 1.0 | 1.3 | | |
| 010b | 120Ω | $V_{OL(DC)} = 0.1 \times V_{DDQ}$ | 0.8 | 1.0 | 1.1 | R _{ZQ} /2 | 1, 2 |
| | | $V_{OM(DC)} = 0.33 \times V_{DDQ}$ | 0.9 | 1.0 | 1.1 | | |
| | | $V_{OH(DC)} = 0.5 \times V_{DDQ}$ | 0.9 | 1.0 | 1.3 | | |
| 011b | 80Ω | $V_{OL(DC)} = 0.1 \times V_{DDQ}$ | 0.8 | 1.0 | 1.1 | R _{ZQ} /3 | 1, 2 |
| | | $V_{OM(DC)} = 0.33 \times V_{DDQ}$ | 0.9 | 1.0 | 1.1 | | |
| | | $V_{OH(DC)} = 0.5 \times V_{DDQ}$ | 0.9 | 1.0 | 1.3 | | |
| 100b | 60Ω | $V_{OL(DC)} = 0.1 \times V_{DDQ}$ | 0.8 | 1.0 | 1.1 | R _{ZQ} /4 | 1, 2 |
| | | $V_{OM(DC)} = 0.33 \times V_{DDQ}$ | 0.9 | 1.0 | 1.1 | | |
| | | $V_{OH(DC)} = 0.5 \times V_{DDQ}$ | 0.9 | 1.0 | 1.3 | | |



Table 136: ODT DC Electrical Characteristics – Beyond 3200 Mbps (Continued)

$R_{ZQ} = 240\Omega \pm 1\%$ over entire operating range after calibration

| MR11 OP[2:0] | R_{TT} | V_{OUT} | Min | Nom | Max | Unit | Notes |
|---|-------------|------------------------------------|-----|-----|-----|------------|---------|
| 101b | 48 Ω | $V_{OL(DC)} = 0.1 \times V_{DDQ}$ | 0.8 | 1.0 | 1.1 | $R_{ZQ}/5$ | 1, 2 |
| | | $V_{OM(DC)} = 0.33 \times V_{DDQ}$ | 0.9 | 1.0 | 1.1 | | |
| | | $V_{OH(DC)} = 0.5 \times V_{DDQ}$ | 0.9 | 1.0 | 1.3 | | |
| 110b | 40 Ω | $V_{OL(DC)} = 0.1 \times V_{DDQ}$ | 0.8 | 1.0 | 1.1 | $R_{ZQ}/6$ | 1, 2 |
| | | $V_{OM(DC)} = 0.33 \times V_{DDQ}$ | 0.9 | 1.0 | 1.1 | | |
| | | $V_{OH(DC)} = 0.5 \times V_{DDQ}$ | 0.9 | 1.0 | 1.3 | | |
| Mismatch error, DQ-to-DQ within a channel | | $0.33 \times V_{DDQ}$ | – | – | 2 | % | 1, 2, 3 |

- Notes:
- The ODT tolerance limits are specified after calibration with stable temperature and voltage. To understand the behavior of the tolerance limits when voltage or temperature changes after calibration, see the following section on voltage and temperature sensitivity.
 - Pull-down ODT resistors are recommended to be calibrated at $0.33 \times V_{DDQ}$. Other calibration points may be required to achieve the linearity specification shown above, for example, calibration at $0.5 \times V_{DDQ}$ and $-0.1 \times V_{DDQ}$.
 - DQ-to-DQ mismatch within byte variation for a given component, including DQS (characterized).

$$\text{DQ-to-DQ mismatch} = \frac{R_{ODT}(\text{MAX}) - R_{ODT}(\text{MIN})}{R_{ODT}(\text{AVG})}$$

Output Driver and Termination Register Temperature and Voltage Sensitivity

When temperature and/or voltage change after calibration, the tolerance limits are widened according to the tables below.

Table 137: Output Driver and Termination Register Sensitivity Definition

| Resistor | Definition Point | Min | Max | Unit | Notes |
|---------------|-----------------------|--|---|------|---------|
| R_{ONPD} | $0.33 \times V_{DDQ}$ | $90 - (dR_{ONdT} \cdot \Delta T) - (dR_{ONdV} \cdot \Delta V)$ | $110 + (dR_{ONdT} \cdot \Delta T) + (dR_{ONdV} \cdot \Delta V)$ | % | 1, 2 |
| V_{OHPU} | $0.33 \times V_{DDQ}$ | $90 - (dV_{OHdT} \cdot \Delta T) - (dV_{OHdV} \cdot \Delta V)$ | $110 + (dV_{OHdT} \cdot \Delta T) + (dV_{OHdV} \cdot \Delta V)$ | | 1, 2, 5 |
| $R_{TT(I/O)}$ | $0.33 \times V_{DDQ}$ | $90 - (dR_{ONdT} \cdot \Delta T) - (dR_{ONdV} \cdot \Delta V)$ | $110 + (dR_{ONdT} \cdot \Delta T) + (dR_{ONdV} \cdot \Delta V)$ | | 1, 2, 3 |
| $R_{TT(IN)}$ | $0.33 \times V_{DD2}$ | $90 - (dR_{ONdT} \cdot \Delta T) - (dR_{ONdV} \cdot \Delta V)$ | $110 + (dR_{ONdT} \cdot \Delta T) + (dR_{ONdV} \cdot \Delta V)$ | | 1, 2, 4 |

- Notes:
- $\Delta T = T - T(\text{@calibration})$, $\Delta V = V - V(\text{@calibration})$
 - dR_{ONdT} , dR_{ONdV} , dV_{OHdT} , dV_{OHdV} , dR_{TTdV} , and dR_{TTdT} are not subject to production test but are verified by design and characterization.
 - This parameter applies to input/output pin such as DQS, DQ, and DMI.
 - This parameter applies to input pin such as CK, CA, and CS.
 - Refer to Pull-up/Pull-down Settings table for V_{OHPU} .


Table 138: Output Driver and Termination Register Temperature and Voltage Sensitivity

| Symbol | Parameter | Min | Max | Unit |
|--------------------|---|-----|------|------|
| dR _{ONdT} | R _{ON} temperature sensitivity | 0 | 0.75 | %/°C |
| dR _{ONdV} | R _{ON} voltage sensitivity | 0 | 0.20 | %/mV |
| dV _{OHdT} | V _{OH} temperature sensitivity | 0 | 0.75 | %/°C |
| dV _{OHdV} | V _{OH} voltage sensitivity | 0 | 0.35 | %/mV |
| dR _{TTdT} | R _{TT} temperature sensitivity | 0 | 0.75 | %/°C |
| dR _{TTdV} | R _{TT} voltage sensitivity | 0 | 0.20 | %/mV |

ODT Mode Register

The ODT mode is enabled if MR11 OP[2:0] are non-zero. In this case, the value of R_{TT} is determined by the settings of those bits. The ODT mode is disabled if MR11 OP[2:0] = 0.

Asynchronous ODT

When ODT mode is enabled in MR11 OP[2:0], DRAM ODT is always High-Z. The DRAM ODT feature is automatically turned ON asynchronously after a WRITE-1, MASK WRITE-1, or MPC[WRITE-FIFO] command. After the burst write is complete, the DRAM ODT turns OFF asynchronously. The DQ bus ODT control is automatic and will turn the ODT resistance on/off if DQ ODT is enabled in the mode register.

The following timing parameters apply when the DQ bus ODT is enabled:

- ODTL_{on}, ^tODTon(MIN), ^tODTon(MAX)
- ODTL_{off}, ^tODToff(MIN), ^tODToff(MAX)

ODTL_{ON} is a synchronous parameter and is the latency from a CAS-2 command to the ^tODTon reference. ODTL_{ON} latency is a fixed latency value for each speed bin. Each speed bin has a different ODTL_{ON} latency.

Minimum R_{TT} turn-on time (^tODTon(MIN)) is the point in time when the device termination circuit leaves High-Z and ODT resistance begins to turn on.

Maximum R_{TT} turn on time (^tODTon(MAX)) is the point in time when the ODT resistance is fully on.

^tODTon(MIN) and ^tODTon(MAX) are measured after ODTL_{ON} latency is satisfied from CAS-2 command.

ODTL_{OFF} is a synchronous parameter and it is the latency from CAS-2 command to ^tODToff reference. ODTL_{OFF} latency is a fixed latency value for each speed bin. Each speed bin has a different ODTL_{OFF} latency.

Minimum R_{TT} turn-off time (^tODToff(MIN)) is the point in time when the device termination circuit starts to turn off the ODT resistance.

Maximum ODT turn off time (^tODToff(MAX)) is the point in time when the on-die termination has reached High-Z.

^tODToff(MIN) and ^tODToff(MAX) are measured after ODTL_{OFF} latency is satisfied from CAS-2 command.

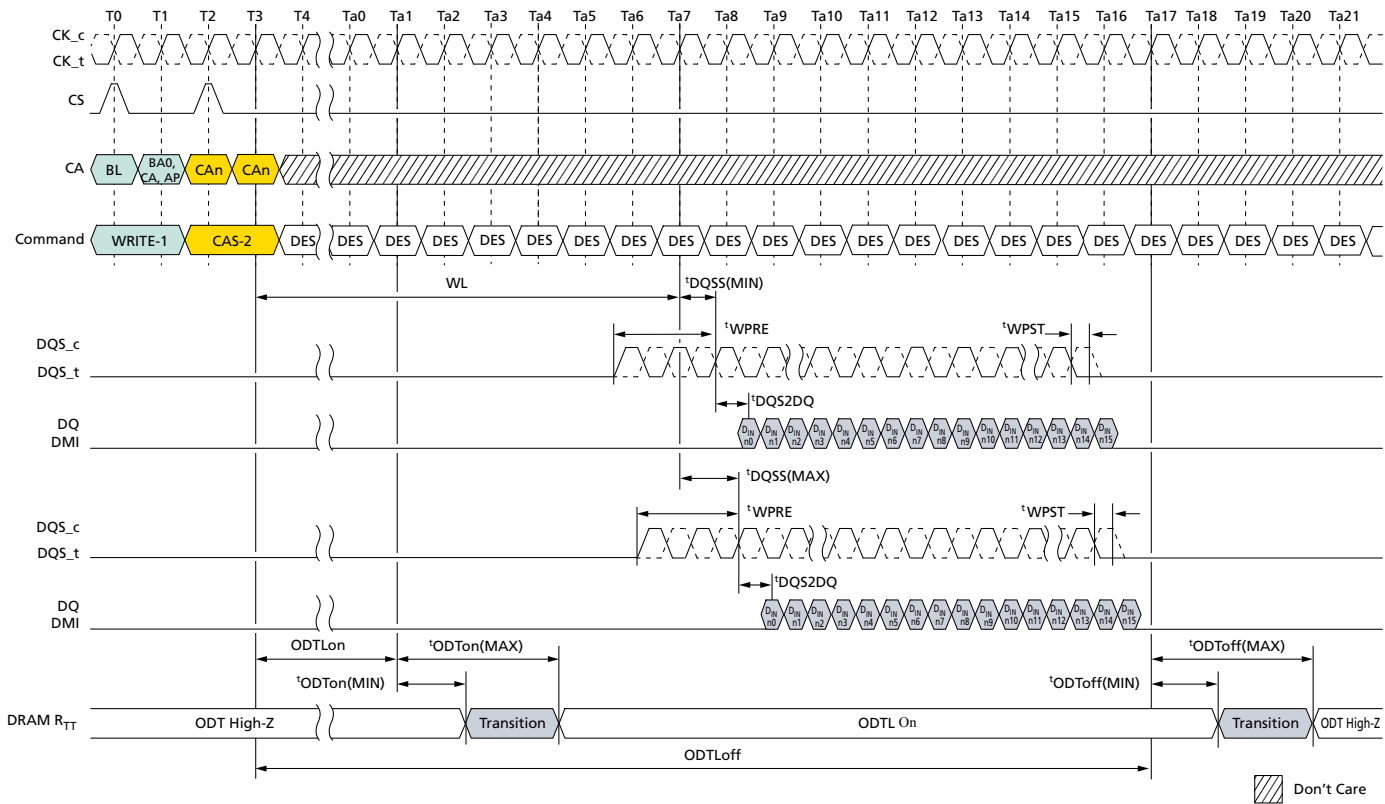


Table 139: ODT_{ON} and ODT_{OFF} Latency Values

| ODT _{ON} Latency ¹ | | ODT _{OFF} Latency ² | | Lower Frequency Limit (>) (MHz) | Upper Frequency Limit (≤) (MHz) |
|--|----------------|---|----------------|---------------------------------|---------------------------------|
| t _{WPRE} = 2 ^t CK | | | | | |
| WL Set A (nCK) | WL Set B (nCK) | WL Set A (nCK) | WL Set B (nCK) | | |
| N/A | N/A | N/A | N/A | 10 | 266 |
| N/A | N/A | N/A | N/A | 266 | 533 |
| N/A | 6 | N/A | 22 | 533 | 800 |
| 4 | 12 | 20 | 28 | 800 | 1066 |
| 4 | 14 | 22 | 32 | 1066 | 1333 |
| 6 | 18 | 24 | 36 | 1333 | 1600 |
| 6 | 20 | 26 | 40 | 1600 | 1866 |
| 8 | 24 | 28 | 44 | 1866 | 2133 |

- Notes: 1. ODT_{ON} is referenced from CAS-2 command.
2. ODT_{OFF} as shown in table assumes BL = 16. For BL32, 8^tCK should be added.

Figure 139: Asynchronous ODTon/ODToff Timing



- Notes: 1. BL = 16, Write postamble = 0.5nCK, DQ/DQS: V_{SSQ} termination.
2. D_{IN} n = data-in to column n.



3. DES commands are shown for ease of illustration; other commands may be valid at these times.

DQ ODT During Power-Down and Self Refresh Modes

DQ bus ODT will be disabled in power-down mode. In self refresh mode, the ODT will be turned off when CKE is LOW but will be enabled if CKE is HIGH and DQ ODT is enabled in the mode register.

ODT During Write Leveling Mode

If ODT is enabled in MR11 OP[2:0] in write leveling mode, the device always provides the termination on DQS signals. DQ termination is always off in write leveling mode.

Table 140: Termination State in Write Leveling Mode

| ODT State in MR11 OP[2:0] | DQS Termination | DQ[15:0]/DMI[1:0] Termination |
|---------------------------|-----------------|-------------------------------|
| Disabled | Off | Off |
| Enabled | On | Off |



Target Row Refresh Mode

The device limits the number of times that a given row can be accessed within a refresh period ($t_{REFW} \times 2$) prior to requiring adjacent rows to be refreshed. The maximum activate count (MAC) is the maximum number of activates that a single row can sustain within a refresh period before the adjacent rows need to be refreshed. The row receiving the excessive activates is the target row (TRn), the adjacent rows to be refreshed are the victim rows. When the MAC limit is reached on TRn, either the device receives all ($R \times 2$) REFRESH commands before another row activate is issued, or the device should be placed into targeted row refresh (TRR) mode. The TRR mode will refresh the rows adjacent to the TRn that encountered t_{MAC} limit.

If the device supports unlimited MAC value: MR24 OP[2:0] = 000 and MR24 OP[3] = 1, TARGET ROW REFRESH operation is not required. Even though the device allows to set MR24 OP[7] = 1: TRR mode enable, in this case the device behavior is vendor specific. For example, a certain device may ignore MRW command for entering/exiting TRR mode or a certain device may support commands related TRR mode. See vendor device data sheets for details about TRR mode definition at supporting unlimited MAC value case.

There could be a maximum of two target rows to a victim row in a bank. The cumulative value of the activates from the two target rows on a victim row in a bank should not exceed MAC value.

MR24 fields are required to support the new TRR settings. Setting MR24 OP[7] = 1 enables TRR mode and setting MR24 OP[7] = 0 disables TRR mode. MR24 OP[6:4] defines which bank (BAn) the target row is located in (refer to MR24 table for details).

The TRR mode must be disabled during initialization as well as any other device calibration modes. The TRR mode is entered from a DRAM idle state, once TRR mode has been entered, no other mode register commands are allowed until TRR mode is completed; however, setting MR24 OP[7] = 0 to interrupt and reissue the TRR mode is allowed.

When enabled, TRR mode is self-clearing. the mode will be disabled automatically after the completion of defined TRR flow (after the third BAn precharge has completed plus t_{MRD}). Optionally, the TRR mode can also be exited via another MRS command at the completion of TRR by setting MR24 OP[7] = 0. If the TRR is exited via another MRS command, the value written to MR24 OP[6:4] are "Don't Care."

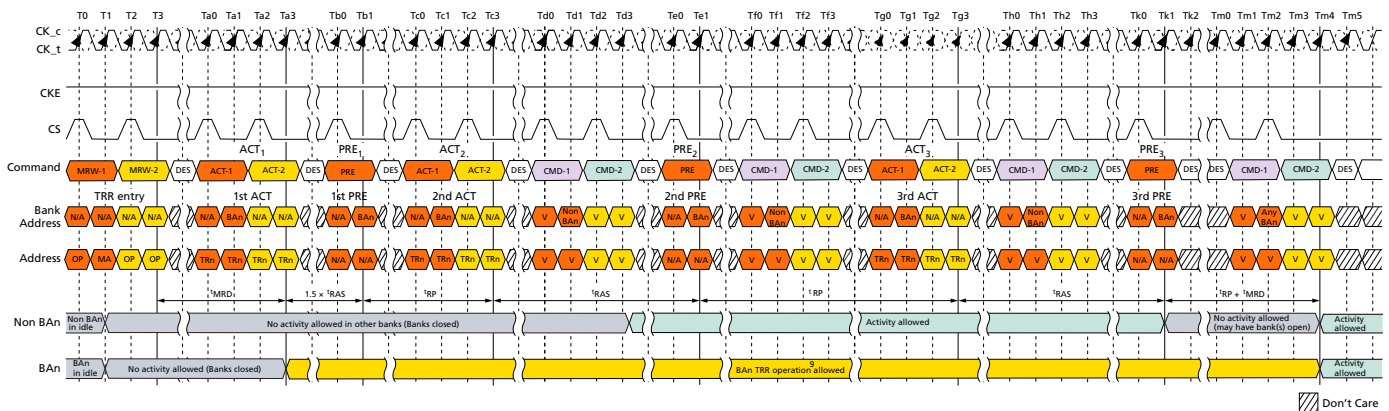
TRR Mode Operation

1. The timing diagram depicts TRR mode. The following steps must be performed when TRR mode is enabled. This mode requires all three ACT (ACT1, ACT2, and ACT3) and three corresponding PRE commands (PRE1, PRE2, and PRE3) to complete TRR mode. PRECHARGE All (PREA) commands issued while the device is in TRR mode will also perform precharge to BAn and counts towards PREn command.
2. Prior to issuing the MRW command to enter TRR mode, the device should be in the idle state. MRW command must be issued with MR24 OP[7] = 1 and MR24 OP[6:4] defining the bank in which the targeted row is located. All other MR24 bits should remain unchanged.
3. No activity is to occur with the device until t_{MRD} has been satisfied. When t_{MRD} has been satisfied, the only commands allowed BAn, until TRR mode has completed, are ACT and PRE.



4. The first ACT to the BAN with the TRn address can now be applied; no other command is allowed at this point. All other banks must remain inactive from when the first BAN ACT command is issued until $(1.5 \times t_{RAS}) + t_{RP}$ is satisfied.
5. After the first ACT to the BAN with the TRn address is issued, PRE to BAN is to be issued $(1.5 \times t_{RAS})$ later; and then followed t_{RP} later by the second ACT to the BAN with the TRn address.
6. After the second ACT to the BAN with the TRn address is issued, PRE to BAN is to be issued t_{RAS} later and then followed t_{RP} later by the third ACT to the BAN with the TRn address.
7. After the third ACT to the BAN with the TRn address is issued, PRE to BAN would be issued t_{RAS} later. TRR mode is completed once t_{RP} plus t_{MRD} is satisfied.
8. TRR mode must be completed as specified to guarantee that adjacent rows are refreshed. Anytime the TRR mode is interrupted and not completed, the interrupted TRR mode must be cleared and then subsequently performed again. To clear an interrupted TRR mode, MR24 change is required with setting MR24 OP[7] = 0, MR24 OP[6:4] are "Don't care," followed by three PRE to BAN, with t_{RP} time in between each PRE command. The complete TRR sequence (steps 2–7) must be then reissued and completed to guarantee that the adjacent rows are refreshed.
9. A REFRESH command to the device, or entering self refresh mode, is not allowed while the device is in TRR mode.

Figure 140: Target Row Refresh Mode



- Notes:
1. TRn is the targeted row.
 2. Bank BAN represents the bank in which the targeted row is located.
 3. TRR mode self-clears after $t_{MRD} + t_{RP}$ measured from the third BAN precharge PRE3 at clock edge Th4.
 4. TRR mode or any other activity can be re-engaged after $t_{RP} + t_{MRD}$ from the third BAN precharge PRE3. PRE_ALL also counts if it is issued instead of PREn. TRR mode is cleared by the device after PRE3 to the BAN bank.
 5. ACTIVATE commands to BAN during TRR mode do not provide refresh support (the refresh counter is unaffected).
 6. The device must restore the degraded row(s) caused by excessive activation of the targeted row (TRn) necessary to meet refresh requirements.
 7. A new TRR mode must wait $t_{MRD} + t_{RP}$ time after the third precharge.
 8. BAN may not be used with any other command.
 9. ACT and PRE are the only allowed commands to BAN during TRR mode.
 10. REFRESH commands are not allowed during TRR mode.



11. All timings are to be met by DRAM during TRR mode, such as t^{FAW} . Issuing ACT1, ACT2, and ACT3 counts towards t^{FAW} budget.

Post-Package Repair

The device has fail row address repair as an optional post-package repair (PPR) feature and it is readable through MR25 OP[7:0].

PPR provides simple and easy repair method in the system and fail row address can be repaired by the electrical programming of Electrical-fuse scheme. The device can correct one row per bank with PPR.

Electrical-fuse cannot be switched back to un-fused states once it is programmed. The controller should prevent unintended PPR mode entry and repair.

Failed Row Address Repair

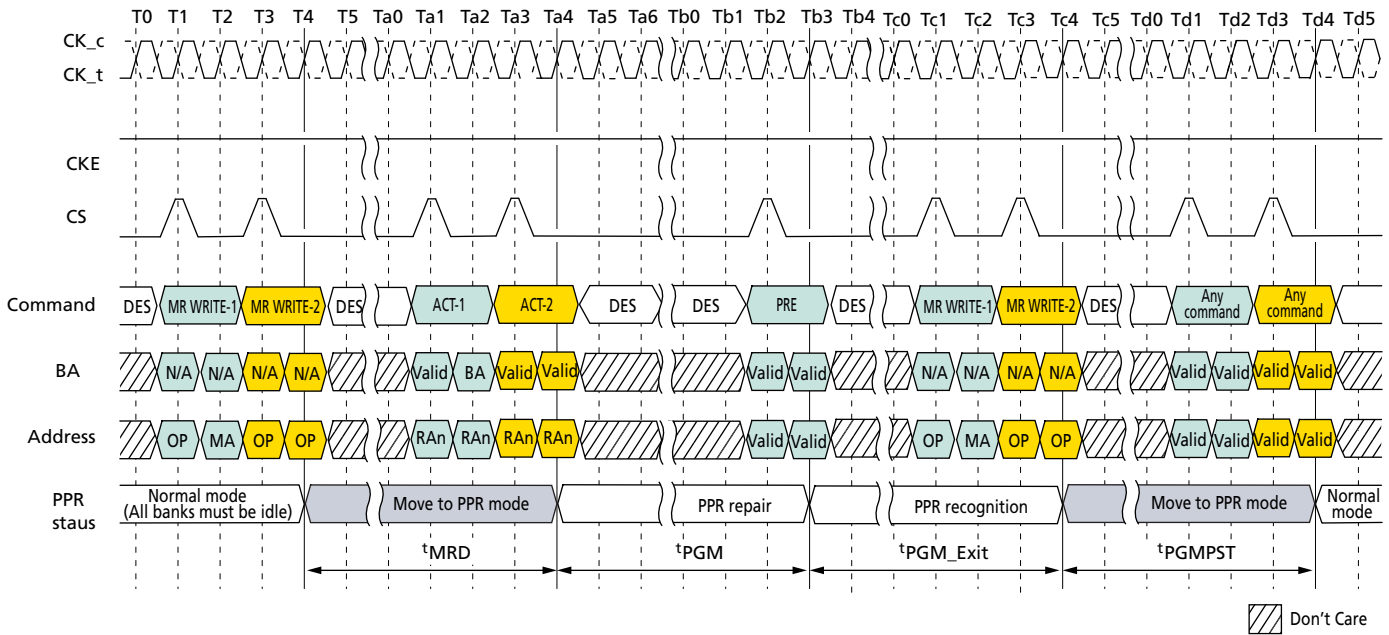
1. Before entering PPR mode, all banks must be precharged.
2. Enable PPR using MR4 OP[4] = 1 and wait t^{MRD} .
3. Issue ACT command with fail row address.
4. Wait t^{PGM} to allow the device repair target row address internally then issue PRECHARGE
5. Wait $t^{\text{PGM_EXIT}}$ after PRECHARGE, which allows the device to recognize repaired row address RAn.
6. Exit PPR mode with setting MR4 OP[4] = 0.
7. The device is ready for any valid command after t^{PGMPST} .
8. In more than one fail address repair case, repeat step 2 to 7.

Once PPR mode is exited, to confirm whether the target row has correctly repaired, the host can verify the repair by writing data into the target row and reading it back after PPR exit with MR4 OP[4] = 0 and t^{PGMPST} .

The following timing diagram shows PPR operation.



Figure 141: Post-Package Repair Timing



- Notes:
1. During t_{PGM}, any other commands (including refresh) are not allowed on each die.
 2. With one PPR command, only one row can be repaired at one time per die.
 3. When PPR procedure completes, reset procedure is required before normal operation.
 4. During PPR, memory contents are not refreshed and may be lost.

Table 141: Post-Package Repair Timing Parameters

| Parameter | Symbol | Min | Max | Units |
|--------------------------|-----------------------|------|-----|-------|
| PPR programming time | t _{PGM} | 1000 | – | ms |
| PPR exit time | t _{PGM_EXIT} | 15 | – | ns |
| New address setting time | t _{PGMPST} | 50 | – | µs |



Read Preamble Training

Read preamble training is supported through the MPC function.

This mode can be used to train or read level the DQS receivers. After read preamble training is enabled by MR13 OP[1] = 1, the device will drive DQS_t LOW and DQS_c HIGH within t^{SDO} and remain at these levels until an MPC[READ DQ CALIBRATION] command is issued.

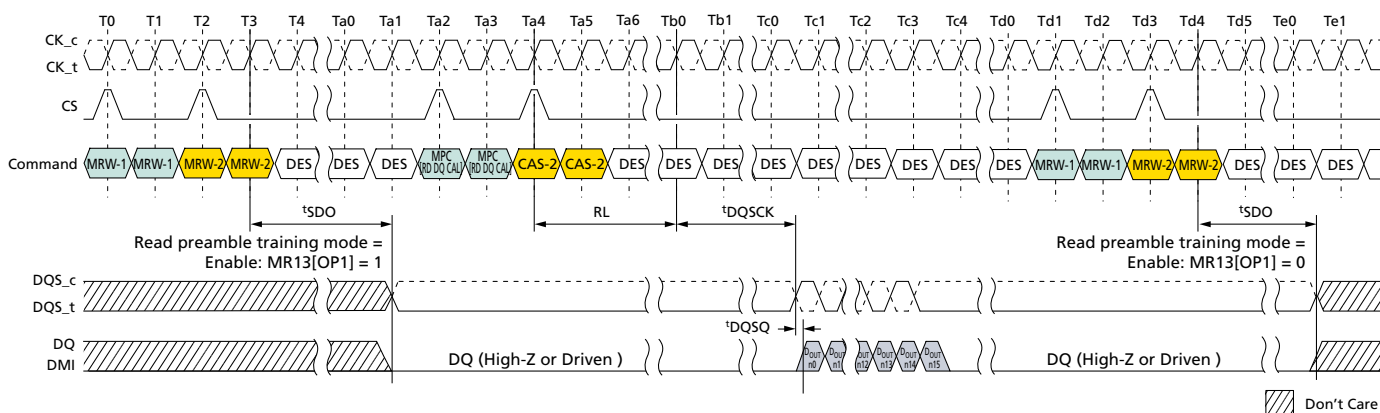
During read preamble training, the DQS preamble provided during normal operation will not be driven by the device. After the MPC[READ DQ CALIBRATION] command is issued, the device will drive DQS_t/DQS_c and DQ like a normal READ burst after RL and t^{DQSK} . Prior to the MPC[READ DQ CALIBRATION] command, the device may or may not drive DQ[15:0] in this mode.

While in read preamble training mode, only READ DQ CALIBRATION commands may be issued.

- Issue an MPC[READ DQ CALIBRATION] command followed immediately by a CAS-2 command.
- Each time an MPC[READ DQ CALIBRATION] command followed by a CAS-2 is received by the device, a 16-bit data burst will, after the currently set RL, drive the eight bits programmed in MR32 followed by the eight bits programmed in MR40 on all I/O pins.
- The data pattern will be inverted for I/O pins with a 1 programmed in the corresponding invert mask mode register bit.
- Note that the pattern is driven on the DMI pins, but no DATA BUS INVERSION function is enabled, even if read DBI is enabled in the DRAM mode register.
- This command can be issued every t^{CCD} seamlessly.
- The operands received with the CAS-2 command must be driven LOW.

Read preamble training is exited within t^{SDO} after setting MR13 OP[1] = 0.

Figure 142: Read Preamble Training



Note: 1. Read DQ calibration supports only BL16 operation.



Electrical Specifications

Absolute Maximum Ratings

Stresses greater than those listed in the table below may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these conditions, or any other conditions outside those indicated in the operational sections of this document, is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 142: Absolute Maximum DC Ratings

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|------------------------------------|------|-----|------|-------|
| V _{DD1} supply voltage relative to V _{SS} | V _{DD1} | -0.4 | 2.1 | V | 1 |
| V _{DD2} supply voltage relative to V _{SS} | V _{DD2} | -0.4 | 1.5 | V | 1 |
| V _{DDQ} supply voltage relative to V _{SS} | V _{DDQ} | -0.4 | 1.5 | V | 1 |
| Voltage on any ball relative to V _{SS} | V _{IN} , V _{OUT} | -0.4 | 1.5 | V | |
| Storage temperature | T _{STG} | -55 | 125 | °C | 2 |

- Notes:
1. For information about relationships between power supplies, see the Voltage Ramp and Device Initialization section.
 2. Storage temperature is the case surface temperature on the center/top side of the device. For measurement conditions, refer to the JE5D51-2 standard.

AC and DC Operating Conditions

Operation or timing that is not specified is illegal. To ensure proper operation, the device must be initialized properly.

Table 143: Recommended DC Operating Conditions

| Symbol | Min | Typ | Max | DRAM | Unit | Notes |
|------------------|------|------|------|---------------------------------|------|---------|
| V _{DD1} | 1.70 | 1.80 | 1.95 | Core 1 power | V | 1, 2 |
| V _{DD2} | 1.06 | 1.10 | 1.17 | Core 2 power/Input buffer power | V | 1, 2, 3 |
| V _{DDQ} | 1.06 | 1.10 | 1.17 | I/O buffer power | V | 2, 3 |

- Notes:
1. V_{DD1} uses significantly less power than V_{DD2}.
 2. The voltage range is for DC voltage only. DC voltage is the voltage supplied at the DRAM and is inclusive of all noise up to 20 MHz at the DRAM package ball.
 3. The voltage noise tolerance from DC to 20 MHz exceeding a peak-to-peak tolerance of 45mV at the DRAM ball is not included in the TdIVW.


Table 144: Input Leakage Current

| Parameter/Condition | Symbol | Min | Max | Unit | Notes |
|-----------------------|--------|-----|-----|---------------|-------|
| Input leakage current | I_L | -4 | 4 | μA | 1, 2 |

- Notes:
- For CK_t, CK_c, CKE, CS, CA, ODT_CA, and RESET_n. Any input $0\text{V} \leq V_{IN} \leq V_{DD2}$. (All other pins not under test = 0V.)
 - CA ODT is disabled for CK_t, CK_c, CS, and CA.

Table 145: Input/Output Leakage Current

| Parameter/Condition | Symbol | Min | Max | Unit | Notes |
|------------------------------|----------|-----|-----|---------------|-------|
| Input/Output leakage current | I_{OZ} | -5 | 5 | μA | 1, 2 |

- Notes:
- For DQ, DQS_t, DQS_c, and DMI. Any I/O $0\text{V} \leq V_{OUT} \leq V_{DDQ}$.
 - I/Os status are disabled: High impedance and ODT off.

Table 146: Operating Temperature Range

| Parameter/Condition | Symbol | Min | Max | Unit |
|---------------------|------------|--------|--------|--------------------|
| Standard | T_{OPER} | Note 4 | 85 | $^{\circ}\text{C}$ |
| Elevated | | 85 | Note 4 | $^{\circ}\text{C}$ |

- Notes:
- Operating temperature is the case surface temperature at the center of the top side of the device. For measurement conditions, refer to the JESD51-2 standard.
 - Some applications require the operation of LPDDR4 in the maximum temperature conditions in the elevated temperature range from 85 $^{\circ}\text{C}$ to 105 $^{\circ}\text{C}$ case temperature. For LPDDR4 devices, derating may be necessary to operate in this range. Refer to MR4.
 - Either the device case temperature rating or the temperature sensor can be used to set an appropriate refresh rate, determine the need for AC timing derating, and/or monitor the operating temperature (see Temperature Sensor). When using the temperature sensor, the actual device case temperature may be higher than the T_{OPER} rating that applies for the standard or elevated temperature range. For example, T_{CASE} could be above +85 $^{\circ}\text{C}$ when the temperature sensor indicates a temperature of less than +85 $^{\circ}\text{C}$.
 - Refer to operating temperature range on top page.



AC and DC Input Measurement Levels

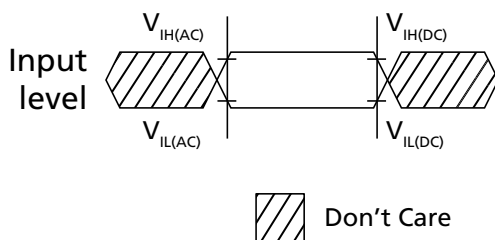
Input Levels for CKE

Table 147: Input Levels

| Parameter | Symbol | Min | Max | Unit | Notes |
|-----------------------|--------------|-----------------------|-----------------------|------|-------|
| Input HIGH level (AC) | $V_{IH(AC)}$ | $0.75 \times V_{DD2}$ | $V_{DD2} + 0.2$ | V | 1 |
| Input LOW level (AC) | $V_{IL(AC)}$ | -0.2 | $0.25 \times V_{DD2}$ | V | 1 |
| Input HIGH level (DC) | $V_{IH(DC)}$ | $0.65 \times V_{DD2}$ | $V_{DD2} + 0.2$ | V | |
| Input LOW level (DC) | $V_{IL(DC)}$ | -0.2 | $0.35 \times V_{DD2}$ | V | |

Note: 1. See the AC Overshoot and Undershoot section.

Figure 143: Input Timing Definition for CKE



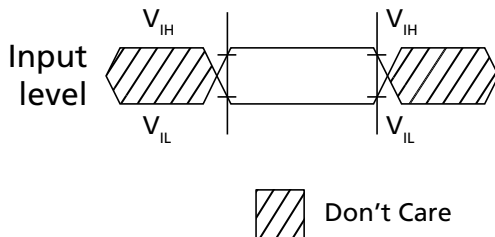
Input Levels for RESET_n

Table 148: Input Levels

| Parameter | Symbol | Min | Max | Unit | Notes |
|------------------|----------|-----------------------|-----------------------|------|-------|
| Input HIGH level | V_{IH} | $0.80 \times V_{DD2}$ | $V_{DD2} + 0.2$ | V | 1 |
| Input LOW level | V_{IL} | -0.2 | $0.20 \times V_{DD2}$ | V | 1 |

Note: 1. See the AC Overshoot and Undershoot section.

Figure 144: Input Timing Definition for RESET_n



Differential Input Voltage for CK

The minimum input voltage needs to satisfy both V_{indiff_CK} and $V_{indiff_CK}/2$ specification at input receiver and their measurement period is 1^tCK . V_{indiff_CK} is the peak-to-peak



voltage centered on 0 volts differential and $V_{\text{indiff_CK}}/2$ is maximum and minimum peak voltage from 0 volts.

Figure 145: CK Differential Input Voltage

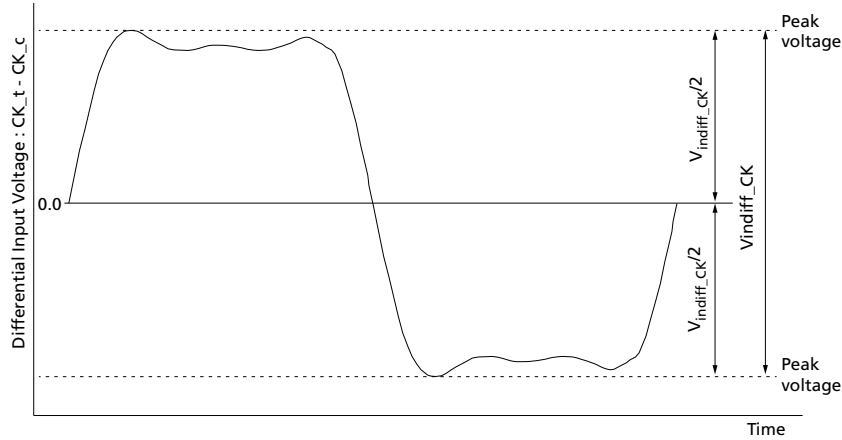


Table 149: CK Differential Input Voltage

| Parameter | Symbol | 1600/1867 | | 2133/2400/3200 | | 3733/4267 | | Unit | Note |
|-------------------------------|-------------------------|-----------|-----|----------------|-----|-----------|-----|------|------|
| | | Min | Max | Min | Max | Min | Max | | |
| CK differential input voltage | $V_{\text{indiff_CK}}$ | 420 | – | 380 | – | 360 | – | mV | 1 |

Note: 1. The peak voltage of differential CK signals is calculated in a following equation.

- $V_{\text{indiff_CK}} = (\text{Maximum peak voltage}) - (\text{Minimum peak voltage})$
- Maximum peak voltage = MAX(f(t))
- Minimum peak voltage = MIN(f(t))
- $f(t) = V_{\text{CK_t}} - V_{\text{CK_c}}$

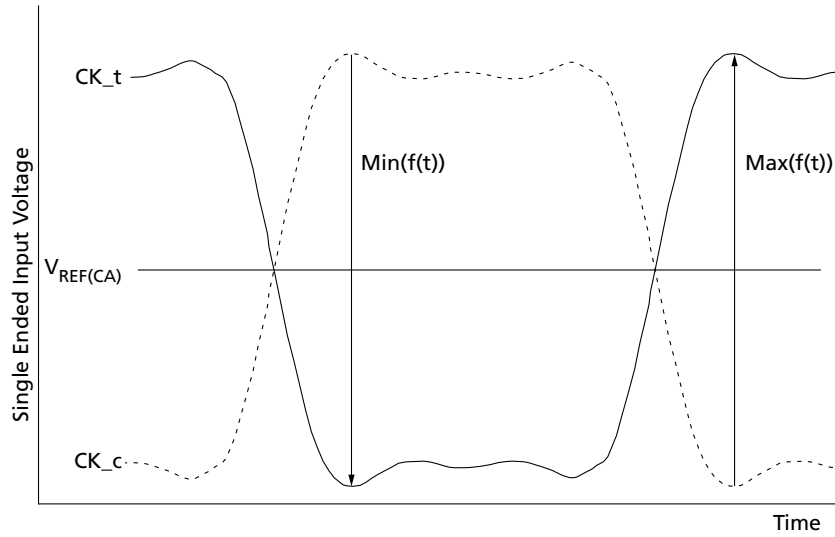
Peak Voltage Calculation Method

The peak voltage of differential clock signals are calculated in a following equation.

- $V_{\text{IH,DIFF:peak}}$ voltage = MAX(f(t))
- $V_{\text{IL,DIFF:peak}}$ voltage = MIN(f(t))
- $f(t) = V_{\text{CK_t}} - V_{\text{CK_c}}$



Figure 146: Definition of Differential Clock Peak Voltage

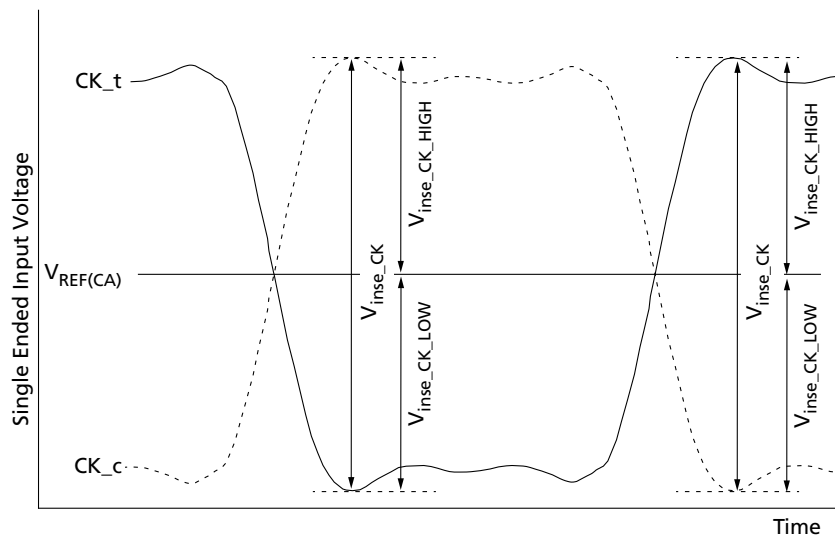


Note: 1. V_{REF(CA)} is device internal setting value by V_{REF} training.

Single-Ended Input Voltage for Clock

The minimum input voltage need to satisfy V_{inse_CK}, V_{inse_CK_HIGH}, and V_{inse_CK_LOW} specification at input receiver.

Figure 147: Clock Single-Ended Input Voltage



Note: 1. V_{REF(CA)} is device internal setting value by V_{REF} training.



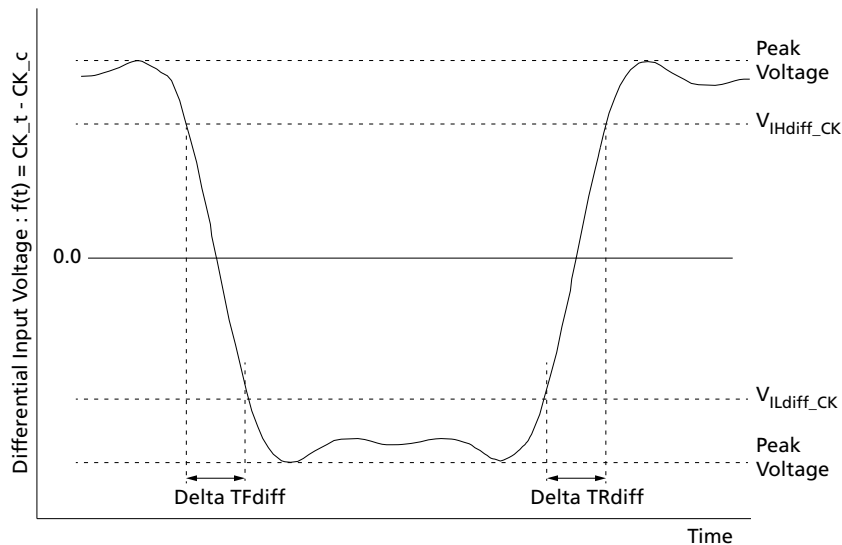
Table 150: Clock Single-Ended Input Voltage

| Parameter | Symbol | 1600/1867 | | 2133/2400/3200 | | 3733/4267 | | Unit |
|--|----------------------|-----------|-----|----------------|-----|-----------|-----|------|
| | | Min | Max | Min | Max | Min | Max | |
| Clock single-ended input voltage | V_{inse_CK} | 210 | – | 190 | – | 180 | – | mV |
| Clock single-ended input voltage HIGH from $V_{REF(CA)}$ | $V_{inse_CK_HIGH}$ | 105 | – | 95 | – | 90 | – | mV |
| Clock single-ended input voltage LOW from $V_{REF(CA)}$ | $V_{inse_CK_LOW}$ | 105 | – | 95 | – | 90 | – | mV |

Differential Input Slew Rate Definition for Clock

Input slew rate for differential signals (CK_t, CK_c) are defined and measured as shown below in figure and the tables.

Figure 148: Differential Input Slew Rate Definition for CK_t, CK_c



- Notes: 1. Differential signal rising edge from V_{ILdiff_CK} to V_{IHdiff_CK} must be monotonic slope.
2. Differential signal falling edge from V_{IHdiff_CK} to V_{ILdiff_CK} must be monotonic slope.

Table 151: Differential Input Slew Rate Definition for CK_t, CK_c

| Description | From | To | Defined by |
|---|------------------|------------------|---|
| Differential input slew rate for rising edge (CK_t - CK_c) | V_{ILdiff_CK} | V_{IHdiff_CK} | $ V_{ILdiff_CK} - V_{IHdiff_CK} / \Delta TRdiff$ |
| Differential input slew rate for falling edge (CK_t - CK_c) | V_{IHdiff_CK} | V_{ILdiff_CK} | $ V_{ILdiff_CK} - V_{IHdiff_CK} / \Delta TFdiff$ |



Table 152: Differential Input Level for CK_t, CK_c

| Parameter | Symbol | 1600/1867 | | 2133/2400/3200 | | 3733/4267 | | Unit |
|-------------------------|------------------|-----------|------|----------------|------|-----------|------|------|
| | | Min | Max | Min | Max | Min | Max | |
| Differential Input HIGH | V_{IHdiff_CK} | 175 | - | 155 | - | 145 | - | mV |
| Differential Input LOW | V_{ILdiff_CK} | - | -175 | - | -155 | - | -145 | mV |

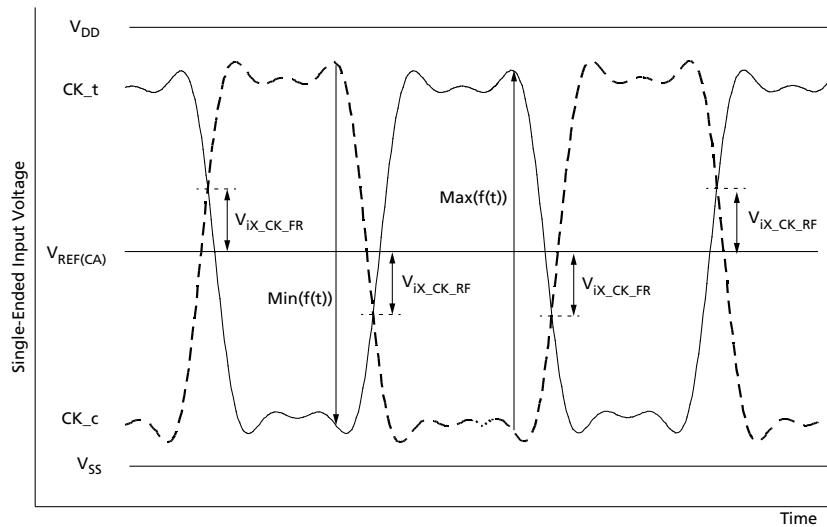
Table 153: Differential Input Slew Rate for CK_t, CK_c

| Parameter | Symbol | 1600/1867 | | 2133/2400/3200 | | 3733/4267 | | Unit |
|--|------------|-----------|-----|----------------|-----|-----------|-----|------|
| | | Min | Max | Min | Max | Min | Max | |
| Differential input slew rate for clock | SRIdiff_CK | 2 | 14 | 2 | 14 | 2 | 14 | V/ns |

Differential Input Cross-Point Voltage

The cross-point voltage of differential input signals (CK_t, CK_c) must meet the requirements in table below. The differential input cross-point voltage V_{IX} is measured from the actual cross-point of true and complement signals to the mid level that is $V_{REF(CA)}$.

Figure 149: V_{IX} Definition (Clock)



Note: 1. The base levels of $V_{IX_CK_FR}$ and $V_{IX_CK_RF}$ are $V_{REF(CA)}$ that is device internal setting value by V_{REF} training.



Table 154: Cross-Point Voltage for Differential Input Signals (Clock)

Notes 1 and 2 apply to entire table

| Parameter | Symbol | 1600/1867 | | 2133/2400/3200 | | 3733/4267 | | Unit |
|--|---------------------|-----------|-----|----------------|-----|-----------|-----|------|
| | | Min | Max | Min | Max | Min | Max | |
| Clock single-ended cross-point voltage ratio | $V_{ix_CK_ratio}$ | - | 25 | - | 25 | - | 25 | % |

- Notes: 1. $V_{ix_CK_ratio}$ is defined by this equation: $V_{ix_CK_ratio} = V_{ix_CK_FR}/|MIN(f(t))|$
 2. $V_{ix_CK_ratio}$ is defined by this equation: $V_{ix_CK_ratio} = V_{ix_CK_RF}/MAX(f(t))$

Differential Input Voltage for DQS

The minimum input voltage needs to satisfy both V_{indiff_DQS} and $V_{indiff_DQS}/2$ specification at input receiver and their measurement period is 1UI ($^tCK/2$). V_{indiff_DQS} is the peak to peak voltage centered on 0 volts differential and $V_{indiff_DQS}/2$ is maximum and minimum peak voltage from 0 volts.

Figure 150: DQS Differential Input Voltage

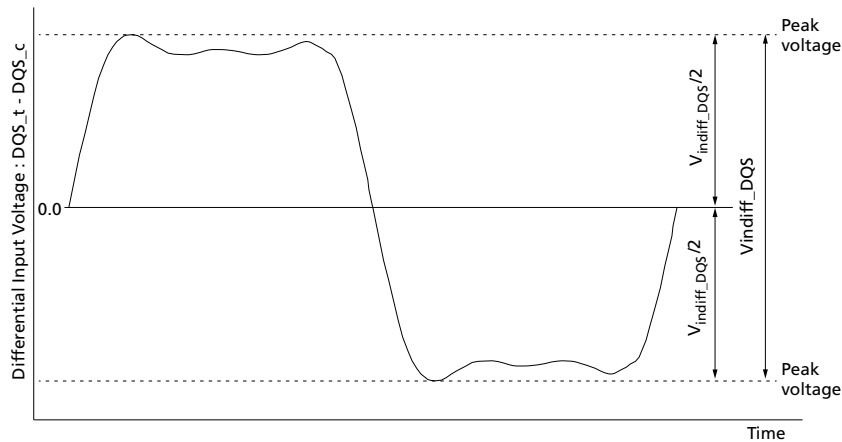


Table 155: DQS Differential Input Voltage

| Parameter | Symbol | 1600/1867 | | 2133/2400/3200 | | 3733/4267 | | Unit | Note |
|--------------------------------|-------------------|-----------|-----|----------------|-----|-----------|-----|------|------|
| | | Min | Max | Min | Max | Min | Max | | |
| DQS differential input voltage | V_{indiff_DQS} | 360 | - | 360 | - | 340 | - | mV | 1 |

Note: 1. The peak voltage of differential DQS signals is calculated in a following equation.

- $V_{indiff_DQS} = (\text{Maximum peak voltage}) - (\text{Minimum peak voltage})$
- $\text{Maximum peak voltage} = MAX(f(t))$
- $\text{Minimum peak voltage} = MIN(f(t))$
- $f(t) = V_{DQS_t} - V_{DQS_c}$

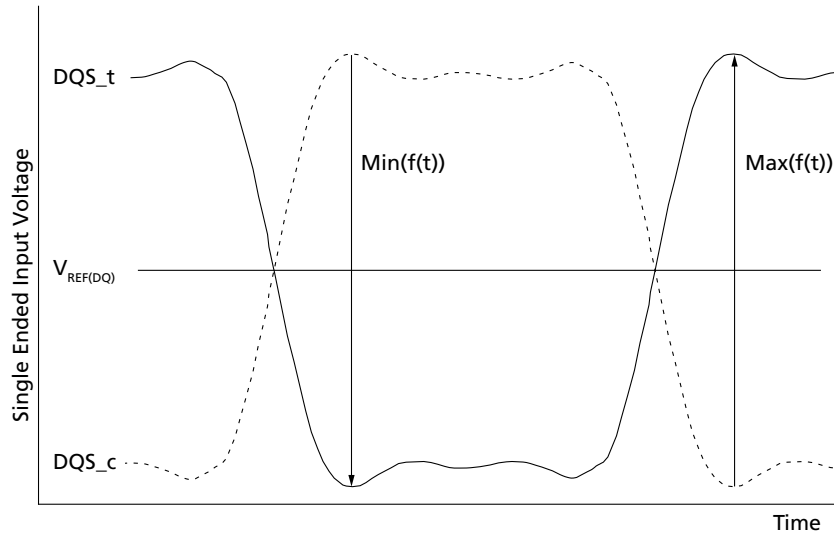
Peak Voltage Calculation Method

The peak voltage of differential DQS signals are calculated in a following equation.



- $V_{IH,DIFF,peak}$ voltage = $MAX(f(t))$
- $V_{IL,DIFF,peak}$ voltage = $MIN(f(t))$
- $f(t) = V_{DQS_t} - V_{DQS_c}$

Figure 151: Definition of Differential DQS Peak Voltage

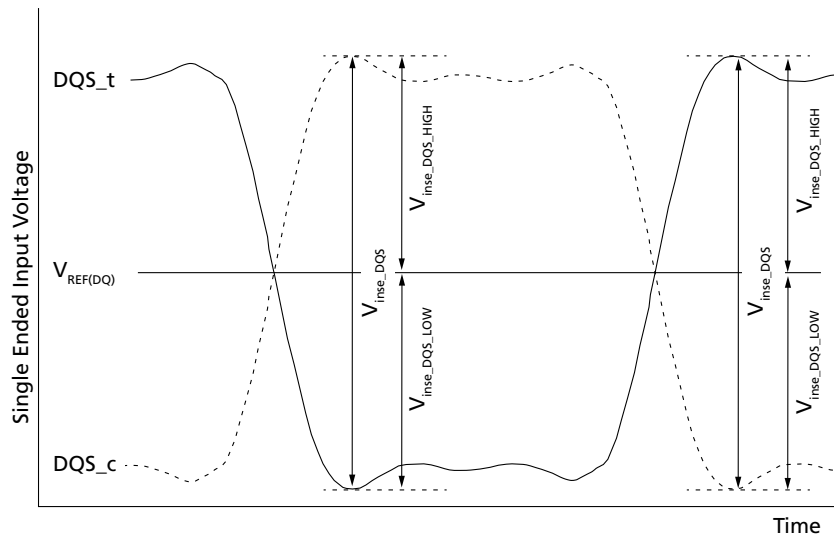


Note: 1. $V_{REF(DQ)}$ is device internal setting value by V_{REF} training.

Single-Ended Input Voltage for DQS

The minimum input voltage need to satisfy V_{inse_DQS} , $V_{inse_DQS_HIGH}$, and $V_{inse_DQS_LOW}$ specification at input receiver.

Figure 152: DQS Single-Ended Input Voltage



Note: 1. $V_{REF(DQ)}$ is device internal setting value by V_{REF} training.



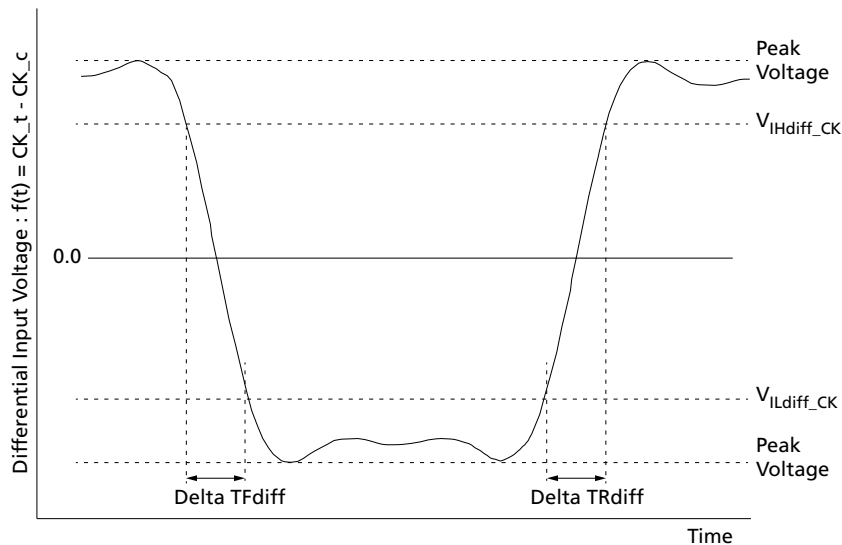
Table 156: DQS Single-Ended Input Voltage

| Parameter | Symbol | 1600/1867 | | 2133/2400/3200 | | 3733/4267 | | Unit |
|--|-----------------------|-----------|-----|----------------|-----|-----------|-----|------|
| | | Min | Max | Min | Max | Min | Max | |
| DQS single-ended input voltage | V_{inse_DQS} | 180 | – | 180 | – | 170 | – | mV |
| DQS single-ended input voltage HIGH from $V_{REF(DQ)}$ | $V_{inse_DQS_HIGH}$ | 90 | – | 90 | – | 85 | – | mV |
| DQS single-ended input voltage LOW from $V_{REF(DQ)}$ | $V_{inse_DQS_LOW}$ | 90 | – | 90 | – | 85 | – | mV |

Differential Input Slew Rate Definition for DQS

Input slew rate for differential signals (DQS_t, DQS_c) are defined and measured as shown below in figure and the tables.

Figure 153: Differential Input Slew Rate Definition for DQS_t, DQS_c



- Notes:
1. Differential signal rising edge from V_{ILdiff_DQS} to V_{IHdiff_DQS} must be monotonic slope.
 2. Differential signal falling edge from V_{IHdiff_DQS} to V_{ILdiff_DQS} must be monotonic slope.

Table 157: Differential Input Slew Rate Definition for DQS_t, DQS_c

| Description | From | To | Defined by |
|---|-------------------|-------------------|--|
| Differential input slew rate for rising edge (DQS_t - DQS_c) | V_{ILdiff_DQS} | V_{IHdiff_DQS} | $ V_{ILdiff_DQS} - V_{IHdiff_DQS} / \Delta TR_{diff}$ |
| Differential input slew rate for falling edge (DQS_t - DQS_c) | V_{IHdiff_DQS} | V_{ILdiff_DQS} | $ V_{ILdiff_DQS} - V_{IHdiff_DQS} / \Delta TF_{diff}$ |



Table 158: Differential Input Level for DQS_t, DQS_c

| Parameter | Symbol | 1600/1867 | | 2133/2400/3200 | | 3733/4267 | | Unit |
|-------------------------|-------------------|-----------|------|----------------|------|-----------|------|------|
| | | Min | Max | Min | Max | Min | Max | |
| Differential Input HIGH | V_{IHdiff_DQS} | 140 | - | 140 | - | 120 | - | mV |
| Differential Input LOW | V_{ILdiff_DQS} | - | -140 | - | -140 | - | -120 | mV |

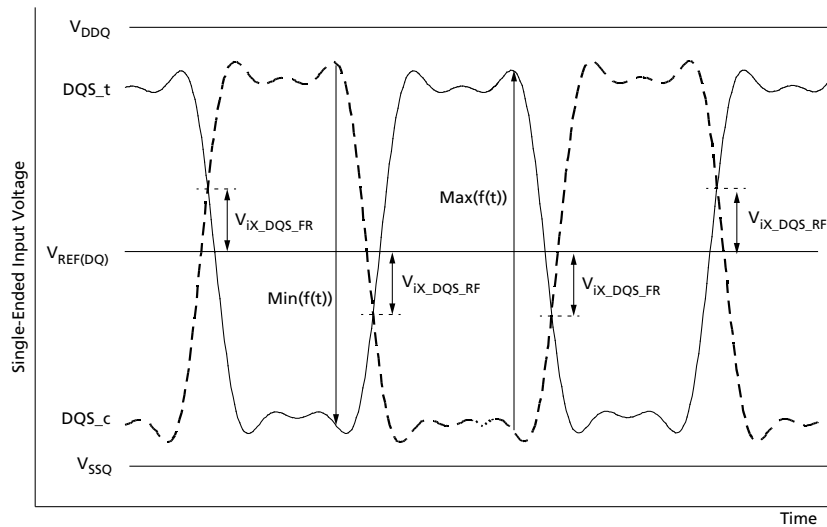
Table 159: Differential Input Slew Rate for DQS_t, DQS_c

| Parameter | Symbol | 1600/1867 | | 2133/2400/3200 | | 3733/4267 | | Unit |
|------------------------------|---------|-----------|-----|----------------|-----|-----------|-----|------|
| | | Min | Max | Min | Max | Min | Max | |
| Differential input slew rate | SRldiff | 2 | 14 | 2 | 14 | 2 | 14 | V/ns |

Differential Input Cross-Point Voltage

The cross-point voltage of differential input signals (DQS_t, DQS_c) must meet the requirements in table below. The differential input cross-point voltage V_{IX} is measured from the actual cross-point of true and complement signals to the mid level that is $V_{REF(DQ)}$.

Figure 154: V_{IX} Definition (DQS)



Note: 1. The base levels of $V_{IX_DQS_FR}$ and $V_{IX_DQS_RF}$ are $V_{REF(DQ)}$ that is device internal setting value by V_{REF} training.



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Table 160: Cross-Point Voltage for Differential Input Signals (DQS)

Notes 1 and 2 apply to entire table

| Parameter | Symbol | 1600/1867 | | 2133/2400/3200 | | 3733/4267 | | Unit |
|--|----------------------|-----------|-----|----------------|-----|-----------|-----|------|
| | | Min | Max | Min | Max | Min | Max | |
| Clock single-ended cross-point voltage ratio | $V_{ix_DQS_ratio}$ | – | 20 | – | 20 | – | 20 | % |

- Notes: 1. $V_{ix_DQS_ratio}$ is defined by this equation: $V_{ix_DQS_ratio} = V_{ix_DQS_FR}/|MIN(f(t))|$
 2. $V_{ix_DQS_ratio}$ is defined by this equation: $V_{ix_DQS_ratio} = V_{ix_DQS_RF}/MAX(f(t))$

Input Levels for ODT_CA

Table 161: Input Levels for ODT_CA

| Parameter | Symbol | Min | Max | Unit |
|----------------------|-------------|-----------------------|-----------------------|------|
| ODT input HIGH level | V_{IHODT} | $0.75 \times V_{DD2}$ | $V_{DD2} + 0.2$ | V |
| ODT input LOW level | V_{ILODT} | –0.2 | $0.25 \times V_{DD2}$ | V |

Output Slew Rate and Overshoot/Undershoot specifications

Single-Ended Output Slew Rate

Table 162: Single-Ended Output Slew Rate

Note 1-5 applies to entire table

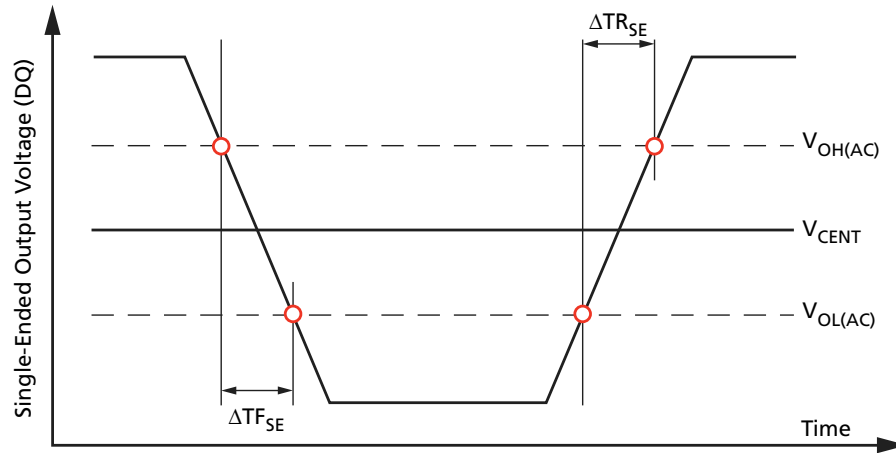
| Parameter | Symbol | Value | | Units |
|--|--------|-------|-----|-------|
| | | Min | Max | |
| Single-ended output slew rate ($V_{OH} = V_{DDQ}/3$) | SRQse | 3.5 | 9.0 | V/ns |
| Output slew rate matching ratio (rise to fall) | – | 0.8 | 1.2 | – |

- Notes: 1. SR = Slew rate; Q = Query output; se = Single-ended signal.
 2. Measured with output reference load.
 3. The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.
 4. The output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)} = 0.2 \times V_{OH(DC)}$ and $V_{OH(AC)} = 0.8 \times V_{OH(DC)}$.
 5. Slew rates are measured under average SSO conditions with 50% of the DQ signals per data byte switching.



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Output Slew Rate and Overshoot/Undershoot specifications

Figure 155: Single-Ended Output Slew Rate Definition



Differential Output Slew Rate

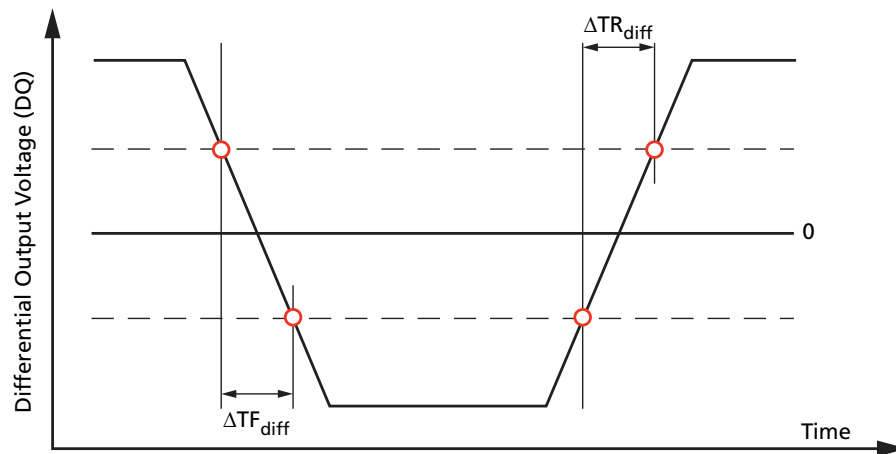
Table 163: Differential Output Slew Rate

Note 1-4 applies to entire table

| Parameter | Symbol | Value | | Units |
|--|---------|-------|-----|-------|
| | | Min | Max | |
| Differential output slew rate ($V_{OH} = V_{DDQ}/3$) | SRQdiff | 7 | 18 | V/ns |

- Notes:
1. SR = Slew rate; Q = Query output; se = Differential signal.
 2. Measured with output reference load.
 3. The output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)} = -0.8 \times V_{OH(DC)}$ and $V_{OH(AC)} = 0.8 \times V_{OH(DC)}$.
 4. Slew rates are measured under average SSO conditions with 50% of the DQ signals per data byte switching.

Figure 156: Differential Output Slew Rate Definition





Overshoot and Undershoot Specifications

Table 164: AC Overshoot/Undershoot Specifications

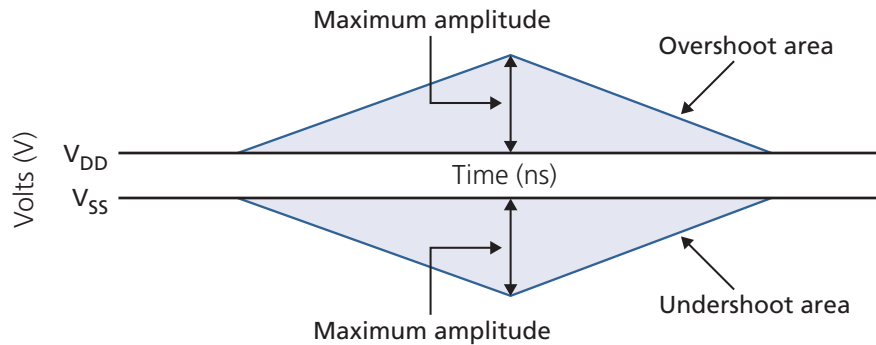
| Parameter | | 1600 | 1866 | 3200 | 3733 | 4267 | Unit |
|---|-----|------|------|------|------|------|------|
| Maximum peak amplitude provided for overshoot area | MAX | 0.3 | 0.3 | 0.3 | 0.3 | 0.3 | V |
| Maximum peak amplitude provided for undershoot area | MAX | 0.3 | 0.3 | 0.3 | 0.3 | 0.3 | V |
| Maximum area above V_{DD}/V_{DDQ} | MAX | 0.1 | 0.1 | 0.1 | 0.1 | 0.1 | V-ns |
| Maximum area below V_{SS}/V_{SSQ} | MAX | 0.1 | 0.1 | 0.1 | 0.1 | 0.1 | V-ns |

- Notes:
1. V_{DD} stands for V_{DD2} for CA[5:0], CK_t, CS_n, CE, and ODT. V_{DD} stands for V_{DDQ} for DQ, DMI, DQS_t, and DQS_c.
 2. V_{SS} stands for V_{SS} for CA[5:0], CK_t, CK_c, CS_n, CE, and ODT. V_{SS} stands for V_{SSQ} for DQ, DMI, DQS_t, and DQS_c.
 3. Maximum peak amplitude values are referenced from actual V_{DD} and V_{SS} values.
 4. Maximum area values are referenced from maximum V_{DD} and V_{SS} values.

Table 165: Overshoot/Undershoot Specification for CKE and RESET

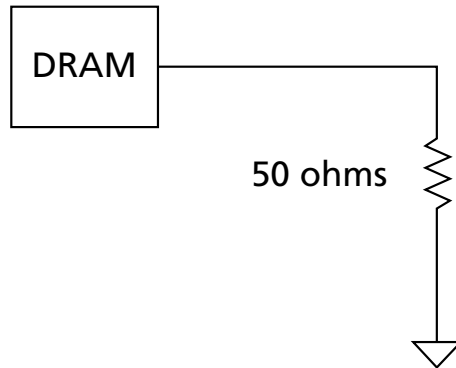
| Parameter | Specification |
|---|---------------|
| Maximum peak amplitude provided for overshoot area | 0.35V |
| Maximum peak amplitude provided for undershoot area | 0.35V |
| Maximum area above V_{DD} | 0.8 V-ns |
| Maximum area below V_{SS} | 0.8 V-ns |

Figure 157: Overshoot and Undershoot Definition



Driver Output Timing Reference Load

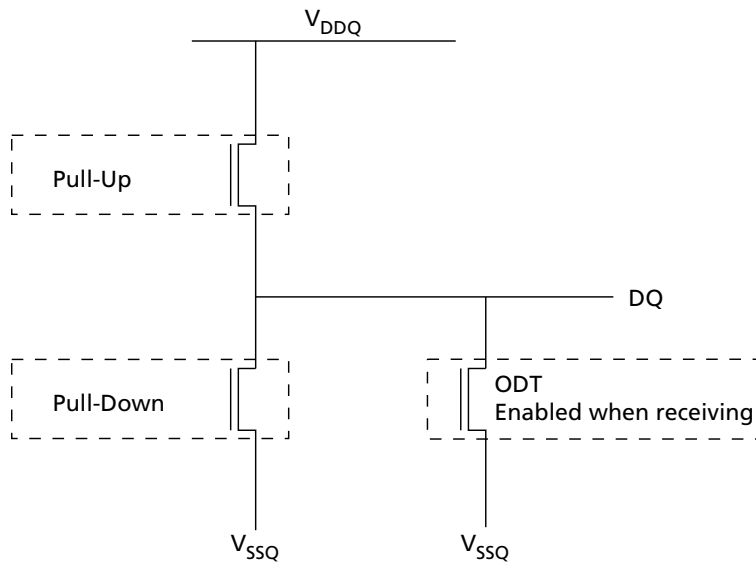
Timing reference loads are not intended as a precise representation of any particular system environment or depiction of an actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.


Figure 158: Driver Output Timing Reference Load


Note: 1. All output timing parameter values are reported with respect to this reference load; this reference load is also used to report slew rate.

LVSTL I/O System

LVSTL I/O cells are comprised of a driver pull-up and pull-down and a terminator.

Figure 159: LVSTL I/O Cell


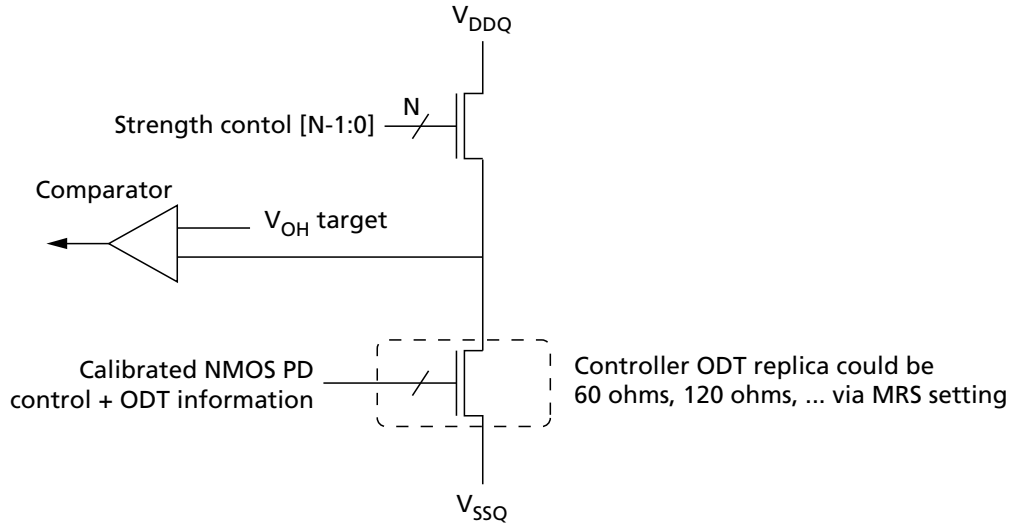
To ensure that the target impedance is achieved, calibrate the LVSTL I/O cell as following example:

1. Calibrate the pull-down device against a 240 ohm resistor to V_{DDQ} via the ZQ pin.
 - Set strength control to minimum setting
 - Increase drive strength until comparator detects data bit is less than $V_{DDQ}/3$
 - NMOS pull-down device is calibrated to 120 ohms
2. Calibrate the pull-up device against the calibrated pull-down device.
 - Set V_{OH} target and NMOS controller ODT replica via MRS (V_{OH} can be automatically controlled by ODT MRS)



- Set strength control to minimum setting
- Increase drive strength until comparator detects data bit is greater than V_{OH} target
- NMOS pull-up device is calibrated to V_{OH} target

Figure 160: Pull-Up Calibration



Input/Output Capacitance

Table 166: Input/Output Capacitance

Notes 1 and 2 apply to entire table

| Parameter | Symbol | Min | Max | Unit | Notes |
|--|------------|------|------|------|-------|
| Input capacitance, CK_t and CK_c | C_{CK} | 0.5 | 0.9 | pF | |
| Input capacitance delta, CK_t and CK_c | C_{DCK} | 0 | 0.09 | | 3 |
| Input capacitance, all other input-only pins | C_I | 0.5 | 0.9 | | 4 |
| Input capacitance delta, all other input-only pins | C_{DI} | -0.1 | 0.1 | | 5 |
| Input/output capacitance, DQ, DMI, DQS_t, DQS_c | C_{IO} | 0.7 | 1.3 | | 6 |
| Input/output capacitance delta, DQS_t, DQS_c | C_{DDQS} | 0 | 0.1 | | 7 |
| Input/output capacitance delta, DQ, DMI | C_{DIO} | -0.1 | 0.1 | | 8 |
| Input/output capacitance, ZQ pin | C_{ZQ} | 0 | 5.0 | | |

- Notes:
1. This parameter applies to LPDDR4 die only (does not include package capacitance).
 2. This parameter is not subject to production testing; it is verified by design and characterization. The capacitance is measured according to JEP147 (procedure for measuring input capacitance using a vector network analyzer), with V_{DD1} , V_{DD2} , V_{DDQ} , and V_{SS} applied; all other pins are left floating.
 3. Absolute value of $C_{CK_t} - C_{CK_c}$.
 4. C_I applies to CS, CKE, and CA[5:0].
 5. $C_{DI} = C_I - 0.5 \times (C_{CK_t} + C_{CK_c})$; it does not apply to CKE.
 6. DMI loading matches DQ and DQS.
 7. Absolute value of C_{DQS_t} and C_{DQS_c} .



8. $C_{D10} = C_{I0} - 0.5 \times (C_{DQS_t} + C_{DQS_c})$ in byte-lane.

I_{DD} Specification Parameters and Test Conditions

Table 167: I_{DD} Measurement Conditions

| Switching for CA | | | | | | | | |
|------------------|------|------|------|------|------|------|------|------|
| CK_t edge | R1 | R2 | R3 | R4 | R5 | R6 | R7 | R8 |
| CKE | HIGH | HIGH | HIGH | HIGH | HIGH | HIGH | HIGH | HIGH |
| CS | LOW | LOW | LOW | LOW | LOW | LOW | LOW | LOW |
| CA0 | HIGH | LOW | LOW | LOW | LOW | HIGH | HIGH | HIGH |
| CA1 | HIGH | HIGH | HIGH | LOW | LOW | LOW | LOW | HIGH |
| CA2 | HIGH | LOW | LOW | LOW | LOW | HIGH | HIGH | HIGH |
| CA3 | HIGH | HIGH | HIGH | LOW | LOW | LOW | LOW | HIGH |
| CA4 | HIGH | LOW | LOW | LOW | LOW | HIGH | HIGH | HIGH |
| CA5 | HIGH | HIGH | HIGH | LOW | LOW | LOW | LOW | HIGH |

- Notes:
1. LOW = $V_{IN} \leq V_{IL(DC)}$ MAX
HIGH = $V_{IN} \geq V_{IH(DC)}$ MIN
STABLE = Inputs are stable at a HIGH or LOW level
 2. CS must always be driven LOW.
 3. 50% of CA bus is changing between HIGH and LOW once per clock for the CA bus.
 4. The pattern is used continuously during I_{DD} measurement for I_{DD} values that require switching on the CA bus.

Table 168: CA Pattern for I_{DD4R}

| Clock Cycle Number | CKE | CS | Command | CA0 | CA1 | CA2 | CA3 | CA4 | CA5 |
|--------------------|------|------|---------|-----|-----|-----|-----|-----|-----|
| N | HIGH | HIGH | Read-1 | L | H | L | L | L | L |
| N+1 | HIGH | LOW | | L | H | L | L | L | L |
| N+2 | HIGH | HIGH | CAS-2 | L | H | L | L | H | L |
| N+3 | HIGH | LOW | | L | L | L | L | L | L |
| N+4 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+5 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+6 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+7 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+8 | HIGH | HIGH | Read-1 | L | H | L | L | L | L |
| N+9 | HIGH | LOW | | L | H | L | L | H | L |
| N+10 | HIGH | HIGH | CAS-2 | L | H | L | L | H | H |
| N+11 | HIGH | LOW | | H | H | H | H | H | H |
| N+12 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+13 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+14 | HIGH | LOW | DES | L | L | L | L | L | L |



200b: x32 LPDDR4 SDRAM I_{DD} Specification Parameters and Test Conditions

Table 168: CA Pattern for I_{DD4R} (Continued)

| Clock Cycle Number | CKE | CS | Command | CA0 | CA1 | CA2 | CA3 | CA4 | CA5 |
|--------------------|------|-----|---------|-----|-----|-----|-----|-----|-----|
| N+15 | HIGH | LOW | DES | L | L | L | L | L | L |

- Notes:
1. BA[2:0] = 010; CA[9:4] = 000000 OR 111111; Burst order CA[3:2] = 00 or 11 (same as LPDDR3 I_{DDR3} specification).
 2. CA pins are kept LOW with DES CMD to reduce ODT current (different from LPDDR3 I_{DDR3} specification).

Table 169: CA Pattern for I_{DD4W}

| Clock Cycle Number | CKE | CS | Command | CA0 | CA1 | CA2 | CA3 | CA4 | CA5 |
|--------------------|------|------|---------|-----|-----|-----|-----|-----|-----|
| N | HIGH | HIGH | Write-1 | L | L | H | L | L | L |
| N+1 | HIGH | LOW | | L | H | L | L | L | L |
| N+2 | HIGH | HIGH | CAS-2 | L | H | L | L | H | L |
| N+3 | HIGH | LOW | | L | L | L | L | L | L |
| N+4 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+5 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+6 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+7 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+8 | HIGH | HIGH | Write-1 | L | L | H | L | L | L |
| N+9 | HIGH | LOW | | L | H | L | L | H | L |
| N+10 | HIGH | HIGH | CAS-2 | L | H | L | L | H | H |
| N+11 | HIGH | LOW | | L | L | H | H | H | H |
| N+12 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+13 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+14 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+15 | HIGH | LOW | DES | L | L | L | L | L | L |

- Notes:
1. BA[2:0] = 010; CA[9:4] = 000000 or 111111 (same as LPDDR3 specification).
 2. No burst ordering (different from LPDDR3 specification).
 3. CA pins are kept LOW with DES CMD to reduce ODT current (different from LPDDR3 specification).

Table 170: Data Pattern for I_{DD4W} (DBI Off)

| DBI Off Case | | | | | | | | | | |
|--------------|-------|-------|-------|-------|-------|-------|-------|-------|-----|---------|
| | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI | # of 1s |
| BL0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL3 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |



200b: x32 LPDDR4 SDRAM I_{DD} Specification Parameters and Test Conditions

Table 170: Data Pattern for I_{DD4W} (DBI Off) (Continued)

| DBI Off Case | | | | | | | | | | |
|--------------|-------|-------|-------|-------|-------|-------|-------|-------|-----|---------|
| | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI | # of 1s |
| BL4 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL5 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL6 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL7 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL8 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL9 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL10 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL11 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL12 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL13 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL14 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL15 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL16 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL17 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL18 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL19 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL20 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL21 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL22 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL23 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL24 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL25 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL26 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL27 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL28 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL29 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL30 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL31 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| # of 1s | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | | |

Note: 1. Simplified pattern; same data pattern was applied to DQ[4], DQ[5], DQ[6], and DQ[7] to reduce complexity for I_{DD4W} pattern programming.

Table 171: Data Pattern for I_{DD4R} (DBI Off)

| DBI Off Case | | | | | | | | | | |
|--------------|-------|-------|-------|-------|-------|-------|-------|-------|-----|---------|
| | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI | # of 1s |
| BL0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |



200b: x32 LPDDR4 SDRAM I_{DD} Specification Parameters and Test Conditions

Table 171: Data Pattern for I_{DD4R} (DBI Off) (Continued)

| DBI Off Case | | | | | | | | | | |
|--------------|-------|-------|-------|-------|-------|-------|-------|-------|-----|---------|
| | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI | # of 1s |
| BL1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL3 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL4 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL5 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL6 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL7 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL8 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL9 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL10 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL11 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL12 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL13 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL14 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL15 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL16 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL17 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL18 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL19 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL20 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL21 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL22 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL23 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL24 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL25 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL26 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL27 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL28 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL29 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL30 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL31 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| # of 1s | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | | |

Note: 1. Simplified pattern; same data pattern was applied to DQ[4], DQ[5], DQ[6], and DQ[7] to reduce complexity for I_{DD4W} pattern programming.



200b: x32 LPDDR4 SDRAM I_{DD} Specification Parameters and Test Conditions

Table 172: Data Pattern for I_{DD4W} (DBI On)

| DBI On Case | | | | | | | | | | |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-----|---------|
| | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI | # of 1s |
| BL0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL3 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL4 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL5 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL6 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL7 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL9 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL10 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL11 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL12 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL13 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL14 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL15 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL16 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL17 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL18 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL19 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL20 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL21 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL22 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL23 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL24 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL25 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL26 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL27 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL28 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL29 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL30 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL31 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| # of 1s | 8 | 8 | 8 | 8 | 8 | 8 | 16 | 16 | 8 | |



200b: x32 LPDDR4 SDRAM I_{DD} Specification Parameters and Test Conditions

Table 173: Data Pattern for I_{DD4R} (DBI On)

| DBI On Case | | | | | | | | | | |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-----|---------|
| | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI | # of 1s |
| BL0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL3 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL4 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL5 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL6 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL7 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL9 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL10 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL11 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL12 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL13 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL14 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL15 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL16 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL17 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL18 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL19 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL20 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL21 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL22 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL23 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL24 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL25 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL26 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL27 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL28 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL29 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL30 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL31 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| # of 1s | 8 | 8 | 8 | 8 | 8 | 8 | 16 | 16 | 8 | |



200b: x32 LPDDR4 SDRAM I_{DD} Specification Parameters and Test Conditions

I_{DD} Specifications

I_{DD} values are for the entire operating voltage range, and all of them are for the entire standard temperature range.

Table 174: I_{DD} Specification Parameters and Operating Conditions

V_{DD2}, V_{DDQ} = 1.06–1.17V; V_{DD1} = 1.70–1.95V

| Parameter/Condition | Symbol | Power Supply | Notes |
|---|---------------------|------------------|-------|
| Operating one bank active-precharge current: $t_{CK} = t_{CK}$ (MIN); $t_{RC} = t_{RC}$ (MIN); CKE is HIGH; CS is LOW between valid commands; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled | I _{DD01} | V _{DD1} | |
| | I _{DD02} | V _{DD2} | |
| | I _{DD0Q} | V _{DDQ} | 2 |
| Idle power-down standby current: $t_{CK} = t_{CK}$ (MIN); CKE is LOW; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled | I _{DD2P1} | V _{DD1} | |
| | I _{DD2P2} | V _{DD2} | |
| | I _{DD2PQ} | V _{DDQ} | 2 |
| Idle power-down standby current with clock stop: CK _t = LOW, CK _c = HIGH; CKE is LOW; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled | I _{DD2PS1} | V _{DD1} | |
| | I _{DD2PS2} | V _{DD2} | |
| | I _{DD2PSQ} | V _{DDQ} | 2 |
| Idle non-power-down standby current: $t_{CK} = t_{CK}$ (MIN); CKE is HIGH; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled | I _{DD2N1} | V _{DD1} | |
| | I _{DD2N2} | V _{DD2} | |
| | I _{DD2NQ} | V _{DDQ} | 2 |
| Idle non-power-down standby current with clock stopped: CK _t = LOW; CK _c = HIGH; CKE is HIGH; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled | I _{DD2NS1} | V _{DD1} | |
| | I _{DD2NS2} | V _{DD2} | |
| | I _{DD2NSQ} | V _{DDQ} | 2 |
| Active power-down standby current: $t_{CK} = t_{CK}$ (MIN); CKE is LOW; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled | I _{DD3P1} | V _{DD1} | |
| | I _{DD3P2} | V _{DD2} | |
| | I _{DD3PQ} | V _{DDQ} | 2 |
| Active power-down standby current with clock stop: CK _t = LOW, CK _c = HIGH; CKE is LOW; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled | I _{DD3PS1} | V _{DD1} | |
| | I _{DD3PS2} | V _{DD2} | |
| | I _{DD3PSQ} | V _{DDQ} | 3 |
| Active non-power-down standby current: $t_{CK} = t_{CK}$ (MIN); CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled | I _{DD3N1} | V _{DD1} | |
| | I _{DD3N2} | V _{DD2} | |
| | I _{DD3NQ} | V _{DDQ} | 3 |
| Active non-power-down standby current with clock stopped: CK _t = LOW, CK _c = HIGH; CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled | I _{DD3NS1} | V _{DD1} | |
| | I _{DD3NS2} | V _{DD2} | |
| | I _{DD3NSQ} | V _{DDQ} | 3 |
| Operating burst READ current: $t_{CK} = t_{CK}$ (MIN); CS is LOW between valid commands; One bank is active; BL = 16 or 32; RL = RL (MIN); CA bus inputs are switching; 50% data change each burst transfer; ODT is disabled | I _{DD4R1} | V _{DD1} | |
| | I _{DD4R2} | V _{DD2} | |
| | I _{DD4RQ} | V _{DDQ} | 4 |



200b: x32 LPDDR4 SDRAM I_{DD} Specification Parameters and Test Conditions

Table 174: I_{DD} Specification Parameters and Operating Conditions (Continued)
 $V_{DD2}, V_{DDQ} = 1.06\text{--}1.17\text{V}; V_{DD1} = 1.70\text{--}1.95\text{V}$

| Parameter/Condition | Symbol | Power Supply | Notes |
|---|---------------------|------------------|---------|
| Operating burst WRITE current: $t_{CK} = t_{CK}(\text{MIN})$; CS is LOW between valid commands; One bank is active; BL = 16 or 32; WL = WL (MIN); CA bus inputs are switching; 50% data change each burst transfer; ODT is disabled | I _{DD4W1} | V _{DD1} | |
| | I _{DD4W2} | V _{DD2} | |
| | I _{DD4WQ} | V _{DDQ} | 3 |
| All-bank REFRESH burst current: $t_{CK} = t_{CK}(\text{MIN})$; CKE is HIGH between valid commands; $t_{RC} = t_{RFCab}(\text{MIN})$; Burst refresh; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled | I _{DD51} | V _{DD1} | |
| | I _{DD52} | V _{DD2} | |
| | I _{DD5Q} | V _{DDQ} | 3 |
| All-bank REFRESH average current: $t_{CK} = t_{CK}(\text{MIN})$; CKE is HIGH between valid commands; $t_{RC} = t_{REFI}$; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled | I _{DD5AB1} | V _{DD1} | |
| | I _{DD5AB2} | V _{DD2} | |
| | I _{DD5ABQ} | V _{DDQ} | 3 |
| Per-bank REFRESH average current: $t_{CK} = t_{CK}(\text{MIN})$; CKE is HIGH between valid commands; $t_{RC} = t_{REFI}/8$; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled | I _{DD5PB1} | V _{DD1} | |
| | I _{DD5PB2} | V _{DD2} | |
| | I _{DD5PBQ} | V _{DDQ} | 3 |
| Power-down self refresh current: CK _t = LOW, CK _c = HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable; Maximum 1x self refresh rate; ODT is disabled | I _{DD61} | V _{DD1} | 5, 6 |
| | I _{DD62} | V _{DD2} | 5, 6 |
| | I _{DD6Q} | V _{DDQ} | 3, 5, 6 |

- Notes:
1. ODT disabled: MR11[2:0] = 000b.
 2. I_{DD} current specifications are tested after the device is properly initialized.
 3. Measured currents are the summation of V_{DDQ} and V_{DD2}.
 4. Guaranteed by design with output load = 5pF and R_{ON} = 40 ohm.
 5. The 1x self refresh rate is the rate at which the device is refreshed internally during self refresh before going into the elevated temperature range.
 6. This is the general definition that applies to full-array self refresh.
 7. For all I_{DD} measurements, V_{IHCKE} = 0.8 × V_{DD2}; V_{ILCKE} = 0.2 × V_{DD2}.



AC Timing

Table 175: Clock Timing

| Parameter | Symbol | Min/ Max | Data Rate | | | | Unit |
|--|-----------------------|-------------|------------------------------------|------|------|------|---------------|
| | | | 1600 | 3200 | 3733 | 4267 | |
| Average clock period | $t_{CK(avg)}$ | Min | 1250 | 625 | 535 | 468 | ps |
| | | Max | 100 | 100 | 100 | 100 | ns |
| Average HIGH pulse width | $t_{CH(avg)}$ | Min | 0.46 | | | | $t_{CK(avg)}$ |
| | | Max | 0.54 | | | | |
| Average LOW pulse width | $t_{CL(avg)}$ | Min | 0.46 | | | | $t_{CK(avg)}$ |
| | | Max | 0.54 | | | | |
| Absolute clock period | $t_{CK(abs)}$ | Min | $t_{CK(avg)min} + t_{JIT(per)min}$ | | | | ps |
| Absolute clock HIGH pulse width | $t_{CH(abs)}$ | Min | 0.43 | | | | $t_{CK(avg)}$ |
| | | Max | 0.57 | | | | |
| Absolute clock LOW pulse width | $t_{CL(abs)}$ | Min | 0.43 | | | | $t_{CK(avg)}$ |
| | | Max | 0.57 | | | | |
| Clock period jitter | $t_{JIT(per)allowed}$ | Min | -70 | -40 | -34 | -30 | ps |
| | | Max | 70 | 40 | 34 | 30 | |
| Maximum clock jitter between two consecutive clock cycles (includes clock period jitter) | $t_{JIT(cc)allowed}$ | Max | 140 | 80 | 68 | 60 | ps |

Table 176: Read Output Timing

| Parameter | Symbol | Min/ Max | Data Rate | | | | | | | Unit | Notes |
|---|------------------------|-------------|------------------------------|------|------|------|------|------|------|-------|-------|
| | | | 533 | 1066 | 1600 | 2133 | 2667 | 3200 | 3733 | | |
| DQS output access time from CK_t/CK_c | t_{DQSCK} | Min | 1500 | | | | | | | ps | 1 |
| | | Max | 3500 | | | | | | | | |
| DQS output access time from CK_t/CK_c - voltage variation | t_{DQSCK_VOLT} | Max | 7 | | | | | | | ps/mV | 2 |
| DQS output access time from CK_t/CK_c - temperature variation | t_{DQSCK_TEMP} | Max | 4 | | | | | | | ps°/C | 3 |
| CK to DQS rank to rank variation | $t_{DQSCK_rank2rank}$ | Max | 1.0 | | | | | | | ns | 4, 5 |
| DQS_t, DQS_c to DQ skew total, per group, per access (DBI Disabled) | t_{DQSQ} | Max | 0.18 | | | | | | | UI | 6 |
| DQ output hold time total from DQS_t, DQS_c (DBI Disabled) | t_{QH} | Min | MIN(t_{QSH} , t_{QSL}) | | | | | | | ps | 6 |



Table 176: Read Output Timing (Continued)

| Parameter | Symbol | Min/ Max | Data Rate | | | | | | | Unit | Notes |
|---|----------------------|-------------|--|------|------|------|------|------|------|---------------|--------|
| | | | 533 | 1066 | 1600 | 2133 | 2667 | 3200 | 3733 | | |
| Data output valid window time total, per pin (DBI-Disabled) | t_{QW_total} | Min | 0.75 | | 0.73 | | 0.68 | | | UI | 6, 11 |
| DQS _t , DQS _c to DQ skew total, per group, per access (DBI-Enabled) | t_{DQSQ_DBI} | Max | 0.18 | | | | | | | UI | 6 |
| DQ output hold time total from DQS _t , DQS _c (DBI-Enabled) | t_{QH_DBI} | Min | MIN(t_{QSH_DBI} , t_{QSL_DBI}) | | | | | | | ps | 6 |
| Data output valid window time total, per pin (DBI-Enabled) | $t_{QW_total_DBI}$ | Min | 0.75 | | 0.73 | | 0.68 | | | UI | 6, 11 |
| DQS _t , DQS _c differential output LOW time (DBI-Disabled) | t_{QSL} | Min | $t_{CL(ABS)} - 0.05$ | | | | | | | $t_{CK(AVG)}$ | 9, 11 |
| DQS _t , DQS _c differential output HIGH time (DBI-Disabled) | t_{QSH} | Min | $t_{CH(ABS)} - 0.05$ | | | | | | | $t_{CK(AVG)}$ | 10, 11 |
| DQS _t , DQS _c differential output LOW time (DBI-Enabled) | t_{QSL_DBI} | Min | $t_{CL(ABS)} - 0.045$ | | | | | | | $t_{CK(AVG)}$ | 9, 11 |
| DQS _t , DQS _c differential output HIGH time (DBI-Enabled) | t_{QSH_DBI} | Min | $t_{CH(ABS)} - 0.045$ | | | | | | | $t_{CK(AVG)}$ | 10, 11 |
| Read preamble | t_{RPRE} | Min | 1.8 | | | | | | | $t_{CK(AVG)}$ | |
| Read postamble | t_{RPST} | Min | 0.4 (or 1.4 if extra postamble is programmed in MR) | | | | | | | $t_{CK(AVG)}$ | |
| DQS Low-Z from clock | $t_{LZ(DQS)}$ | Min | $(RL \times t_{CK}) + t_{DQSCK(MIN)} - (t_{RPRE(MAX)} \times t_{CK}) - 200ps$ | | | | | | | ps | |
| DQ Low-Z from clock | $t_{LZ(DQ)}$ | Min | $(RL \times t_{CK}) + t_{DQSCK(MIN)} - 200ps$ | | | | | | | ps | |
| DQS High-Z from clock | $t_{HZ(DQS)}$ | Min | $(RL \times t_{CK}) + t_{DQSCK(MAX)} + (BL/2 \times t_{CK}) + (t_{RPST(MAX)} \times t_{CK}) - 100ps$ | | | | | | | ps | |
| DQ High-Z from clock | $t_{HZ(DQ)}$ | Min | $(RL \times t_{CK}) + t_{DQSCK(MAX)} + t_{DQSQ(MAX)} + (BL/2 \times t_{CK}) - 100ps$ | | | | | | | ps | |

- Notes:
1. This parameter includes DRAM process, voltage, and temperature variation. It also includes the AC noise impact for frequencies >20 MHz and a MAX voltage of 45mV peak-to-peak from DC-20 MHz at a fixed temperature on the package. The voltage supply noise must comply with the component MIN/MAX DC operating conditions.
 2. t_{DQSCK_volt} MAX delay variation as a function of DC voltage variation for V_{DDQ} and V_{DD2} . The voltage supply noise must comply with the component MIN/MAX DC operating conditions. The voltage variation is defined as the $MAX[abs(t_{DQSCKmin@V1} - t_{DQSCKmax@V2}), abs(t_{DQSCKmax@V1} - t_{DQSCKmin@V2})]/abs(V1 - V2)$. For tester measurement $V_{DDQ} = V_{DD2}$ is assumed.
 3. t_{DQSCK_temp} MAX delay variation as a function of temperature.
 4. The same voltage and temperature are applied to $t_{DQSCK_rank2rank}$.



5. $t_{DQSK_rank2rank}$ parameter is applied to multi-ranks per byte lane within a package consisting of the same design dies.
6. DQ-to-DQS differential jitter where the total includes the sum of deterministic and random timing terms for a specified BER.
7. The deterministic component of the total timing.
8. This parameter will be characterized and guaranteed by design.
9. t_{QSL} describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as measured from one falling edge to the next consecutive rising edge.
10. t_{QSH} describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as measured from one falling edge to the next consecutive rising edge.
11. This parameter is a function of input clock jitter. These values assume MIN $t_{CH(abs)}$ and $t_{CL(abs)}$. When the input clock jitter MIN $t_{CH(abs)}$ and $t_{CL(abs)}$ is 0.44 or greater than $t_{CK(avg)}$, the MIN value of t_{QSL} will be $t_{CL(abs)} - 0.04$ and t_{QSH} will be $t_{CH(abs)} - 0.04$.

Table 177: Write Voltage and Timing

 Note UI = $t_{CK(AVG)}(MIN)/2$

| Parameter | Symbol | Min/ Max | Data Rate | | | | | | | Unit | Notes |
|---|--------------------|-------------|---|------|------|------|------|------|------|---------------|---------|
| | | | 533 | 1066 | 1600 | 2133 | 2667 | 3200 | 3733 | | |
| Rx timing window total at V_{dIVW} voltage levels | $TdIVW_{total}$ | Max | 0.22 | | | | 0.25 | | | UI | 1, 2, 3 |
| DQ and DMI input pulse width (at V_{CENT_DQ}) | $TdIPW$ | Min | 0.45 | | | | | | | UI | 7 |
| DQ-to-DQS offset | t_{DQS2DQ} | Min | 200 | | | | | | | ps | 6 |
| | | Max | 800 | | | | | | | | |
| DQ-to-DQ offset | t_{DQDQ} | Max | 30 | | | | | | | ps | 7 |
| DQ-to-DQS offset temperature variation | t_{DQS2DQ_temp} | Max | 0.6 | | | | | | | ps/°C | 8 |
| DQ-to-DQS offset voltage variation | t_{DQS2DQ_volt} | Max | 33 | | | | | | | ps/50mV | 9 |
| WRITE command to first DQS transition | t_{DQSS} | Min | 0.75 | | | | | | | $t_{CK(avg)}$ | |
| | | Max | 1.25 | | | | | | | | |
| DQS input HIGH-level width | t_{DQSH} | - | 0.4 | | | | | | | $t_{CK(avg)}$ | |
| DQS input LOW-level width | t_{DQSL} | Min | 0.4 | | | | | | | $t_{CK(avg)}$ | |
| DQS falling edge to CK setup time | t_{DSS} | Min | 0.2 | | | | | | | $t_{CK(avg)}$ | |
| DQS falling edge from CK hold time | t_{DSH} | Min | 0.2 | | | | | | | $t_{CK(avg)}$ | |
| Write postamble | t_{WPST} | Min | 0.4 (or 1.4 if extra postamble is programmed in MR) | | | | | | | $t_{CK(avg)}$ | |
| Write preamble | t_{WPRE} | Min | 1.8 | | | | | | | $t_{CK(avg)}$ | |

- Notes: 1. Data Rx mask voltage and timing parameters are applied per pin and include the DRAM DQ-to-DQS voltage AC noise impact for frequencies >20 MHz with a maximum voltage of 45mV peak-to-peak at a fixed temperature on the package. The voltage supply noise must comply to the component MIN/MAX DC operating conditions.



2. Rx differential DQ-to-DQS jitter total timing window at the V_{DIVV} voltage levels.
3. Defined over the DQ internal V_{REF} range. The Rx mask at the pin must be within the internal V_{REF} DQ range irrespective of the input signal common mode.
4. Rx mask defined for one pin toggling with other DQ signals in a steady state.
5. DQ-only minimum input pulse width defined at the $V_{CENT_DQ(pin_mid)}$.
6. DQ-to-DQS offset is within byte from DRAM pin to DRAM internal latch. Includes all DRAM process, voltage, and temperature variations.
7. DQ-to-DQ offset defined within byte from DRAM pin to DRAM internal latch for a given component.
8. t_{DQS2DQ} (MAX) delay variation as a function of temperature.
9. t_{DQS2DQ} (MAX) delay variation as a function of the DC voltage variation for V_{DDQ} and V_{DD2} . It includes the V_{DDQ} and V_{DD2} AC noise impact for frequencies >20 MHz and MAX voltage of 45mV peak-to-peak from DC-20 MHz at a fixed temperature on the package. For tester measurement, $V_{DDQ} = V_{DD2}$ is assumed.

Table 178: CKE Input Timing

| Parameter | Symbol | Min/ Max | Data Rate | | | | Unit | Notes |
|---|---------------|-------------|-------------------|------|------|------|------|-------|
| | | | 1600 | 3200 | 3733 | 4267 | | |
| CKE minimum pulse width (HIGH and LOW pulse width) | t_{CKE} | Min | MAX(7.5ns, 4nCK) | | | | ns | 1 |
| Delay from valid command to CKE input LOW | t_{CMDCKE} | Min | MAX(1.75ns, 3nCK) | | | | ns | 1 |
| Valid clock requirement after CKE input LOW | t_{CKELCK} | Min | MAX(5ns, 5nCK) | | | | ns | 1 |
| Valid CS requirement before CKE input LOW | t_{CSCKE} | Min | 1.75 | | | | ns | |
| Valid CS requirement after CKE input LOW | t_{CKELCS} | Min | MAX(5ns, 5nCK) | | | | ns | 1 |
| Valid Clock requirement before CKE Input HIGH | t_{CKCKEH} | Min | MAX(1.75ns, 3nCK) | | | | ns | 1 |
| Exit power-down to next valid command delay | t_{XP} | Min | MAX(7.5ns, 5nCK) | | | | ns | 1 |
| Valid CS requirement before CKE input HIGH | t_{CSCKEH} | Min | 1.75 | | | | ns | |
| Valid CS requirement after CKE input HIGH | t_{CKEHCS} | Min | MAX(7.5ns, 5nCK) | | | | ns | 1 |
| Valid clock and CS requirement after CKE input LOW after MRW command | $t_{MRWCKEL}$ | Min | MAX(14ns, 10nCK) | | | | ns | 1 |
| Valid clock and CS requirement after CKE input LOW after ZQ calibration start command | t_{ZQCKE} | Min | MAX(1.75ns, 3nCK) | | | | ns | 1 |

- Note: 1. Delay time has to satisfy both analog time (ns) and clock count (nCK). For example, t_{CMDCKE} will not expire until CK has toggled through at least 3 full cycles ($3t_{CK}$) and 3.75ns has transpired. The case which $3nCK$ is applied to is shown below.



Figure 161: t_{CMDCKE} Timing

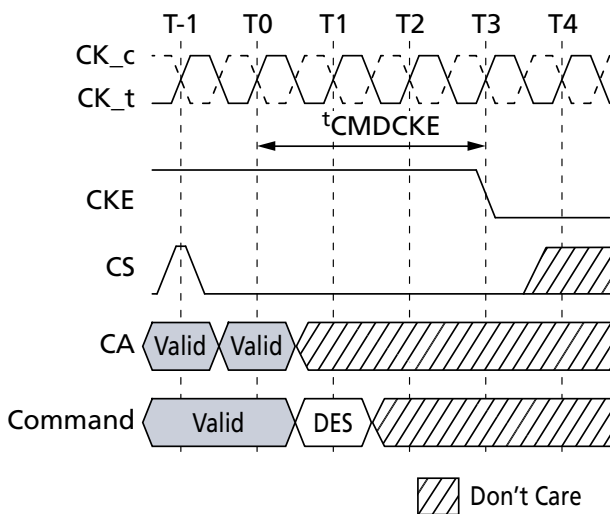


Table 179: Command Address Input Timing

| Parameter | Symbol | Min/ Max | Data Rate | | | | | | | | Unit | Notes |
|---|-------------------|-------------|-----------|------|------|------|------|------|------|------|----------------------|---------|
| | | | 533 | 1066 | 1600 | 2133 | 2667 | 3200 | 3733 | 4267 | | |
| Command/address valid window (referenced from CA V_{IL}/V_{IH} to CK V_{IX}) | t_{cIVW} | Min | 0.3 | | | | | | 0.35 | 0.4 | $t_{\text{CK(avg)}}$ | 1, 2, 3 |
| Address and control input pulse width (referenced to V_{REF}) | t_{cIPW} | Min | 0.55 | 0.55 | 0.55 | 0.6 | 0.6 | 0.6 | 0.7 | 0.8 | $t_{\text{CK(avg)}}$ | 4 |

- Notes:
1. CA Rx mask timing parameters at the pin including voltage and temperature drift.
 2. Rx differential CA to CK jitter total timing window at the V_{cIVW} voltage levels.
 3. Defined over the CA internal V_{REF} range. The Rx mask at the pin must be within the internal $V_{\text{REF(CA)}}$ range irrespective of the input signal common mode.
 4. CA only minimum input pulse width defined at the $V_{\text{CENT_CA}}$ (pin mid).

Table 180: Boot Timing Parameters (10–55 MHz)

| Parameter | Symbol | Min/ Max | Value | Unit |
|-------------------------------------|----------------------|-------------|-------|------|
| Clock cycle time | t_{CKb} | Min | 18 | ns |
| | | Max | 100 | |
| DQS output data access time from CK | $t_{\text{DQSCk b}}$ | Min | 1.0 | ns |
| | | Max | 10.0 | |
| DQS edge to output data edge | t_{DQSQb} | Max | 1.2 | ns |


Table 181: Mode Register Timing Parameters

| Parameter | Symbol | Min/ Max | Data Rate | | | | Unit |
|--|------------|-------------|-------------------------------------|------|------|------|----------------------|
| | | | 1600 | 3200 | 3733 | 4267 | |
| MODE REGISTER WRITE (MRW) command period | t^{MRW} | Min | MAX(10ns, 10nCK) | | | | ns |
| MODE REGISTER SET command delay | t^{MRD} | Min | MAX(14ns, 10nCK) | | | | ns |
| MODE REGISTER READ (MRR) command period | t^{MRR} | Min | 8 | | | | $t^{CK}(\text{avg})$ |
| Additional time after t^{XP} has expired until the MRR command may be issued | t^{MRRI} | Min | $t^{RCD}(\text{min}) + 3n\text{CK}$ | | | | ns |
| Delay from MRW command to DQS driven out | t^{SDO} | Max | MAX(12nCK, 20ns) | | | | ns |

Table 182: Core Timing Parameters

Refresh rate is determined by the value in MR4 OP[2:0]

| Parameter | Symbol | Min/ Max | Data Rate | | | | | | | | Unit | Notes |
|---|-------------|-------------|--|------|------|------|------|------|------|------|----------------------|-------|
| | | | 533 | 1066 | 1600 | 2133 | 2667 | 3200 | 3733 | 4267 | | |
| READ latency (DBI disabled) | RL-A | Min | 6 | 10 | 14 | 20 | 24 | 28 | 32 | 36 | $t^{CK}(\text{avg})$ | |
| READ latency (DBI enabled) | RL-B | Min | 6 | 12 | 16 | 22 | 28 | 32 | 36 | 40 | $t^{CK}(\text{avg})$ | |
| WRITE latency (Set A) | WL-A | Min | 4 | 6 | 8 | 10 | 12 | 14 | 16 | 18 | $t^{CK}(\text{avg})$ | |
| WRITE latency (Set B) | WL-B | Min | 4 | 8 | 12 | 18 | 22 | 26 | 30 | 34 | $t^{CK}(\text{avg})$ | |
| ACTIVATE-to-ACTIVATE command period (same bank) | t^{RC} | Min | $t^{RAS} + t^{RPab}$ (with all-bank precharge) $t^{RAS} + t^{RPpb}$ (with per-bank precharge) | | | | | | | | ns | 1 |
| Minimum self refresh time (entry to exit) | t^{SR} | Min | MAX(15ns, 3nCK) | | | | | | | | ns | |
| Self refresh exit to next valid command delay | t^{XSR} | Min | MAX($t^{RFCab} + 7.5\text{ns}$, 2nCK) | | | | | | | | ns | |
| CAS-to-CAS delay | t^{CCD} | Min | 8 | | | | | | | | $t^{CK}(\text{avg})$ | |
| CAS-to-CAS delay masked write | t^{CCDMW} | MIN | 32 | | | | | | | | $t^{CK}(\text{avg})$ | |
| Internal READ-to-PRE-CHARGE command delay | t^{RTP} | Min | MAX(7.5ns, 8nCK) | | | | | | | | ns | |
| RAS-to-CAS delay | t^{RCD} | Min | MAX(18ns, 4nCK) | | | | | | | | ns | |
| Row precharge time (single bank) | t^{RPpb} | Min | MAX(18ns, 3nCK) | | | | | | | | ns | |
| Row precharge time (all banks) | t^{RPab} | Min | MAX(21ns, 3nCK) | | | | | | | | ns | |



Table 182: Core Timing Parameters (Continued)

Refresh rate is determined by the value in MR4 OP[2:0]

| Parameter | Symbol | Min/ Max | Data Rate | | | | | | | Unit | Notes |
|---|--------------------|-------------|---|------|------|------|------|------|------|-----------------------|-------|
| | | | 533 | 1066 | 1600 | 2133 | 2667 | 3200 | 3733 | | |
| Row active time | t _{RAS} | Min | MAX(42ns, 3nCK) | | | | | | | ns | 1 |
| | | Max | MIN(9 × t _{REFI} × Refresh Rate ¹ , 70.2) | | | | | | | μs | |
| Write recovery time | t _{WR} | Min | MAX(18ns, 4nCK) | | | | | | | ns | |
| Write-to-read delay | t _{WTR} | Min | MAX(10ns, 8nCK) | | | | | | | ns | |
| Active bank A to active bank B | t _{RRD} | Min | MAX(10ns, 4nCK) | | | | | | | ns | |
| Precharge-to-precharge delay | t _{PPD} | Min | 4 | | | | | | | t _{CK} (avg) | 2 |
| Four-bank activate window | t _{FAW} | Min | 40 | | | | | | | ns | |
| Delay from SRE command to CKE input LOW | t _{ESCKE} | Min | MAX(1.75ns, 3nCK) | | | | | | | – | 3 |

- Notes:
1. DRAM devices should be evenly addressed when being accessed. Disproportionate accesses to a particular row address may result in reduction of the product lifetime.
 2. Precharge to precharge timing restriction does not apply to AUTO PRECHARGE commands.
 3. Delay time has to satisfy both analog time (ns) and clock count (nCK). It means that t_{ESCKE} will not expire until CK has toggled through at least three full cycles (3 t_{CK}) and 1.75ns has transpired. The case which 3nCK is applied to is shown below.

Figure 162: t_{ESCKE} Timing

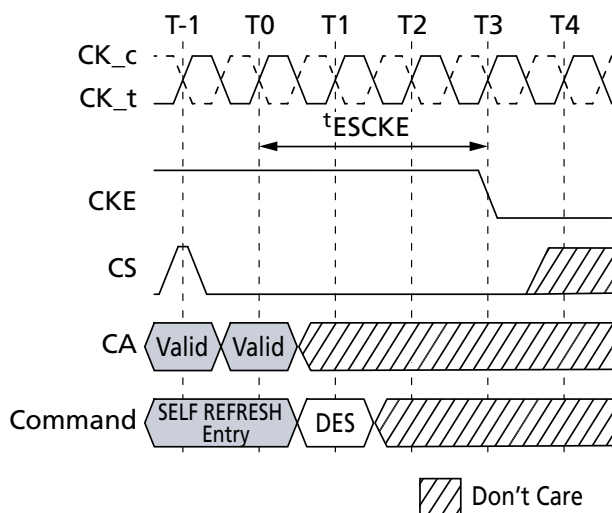



Table 183: CA Bus ODT Timing

| Parameter | Symbol | Min/ Max | Data Rate |
|--------------------------|-------------|-------------|-------------------------|
| | | | 533-4267 |
| CA ODT value update time | t_{ODTUP} | Min | RU(20ns/ t_{CK} ,avg) |

Table 184: CA Bus Training Parameters

| Parameter | Symbol | Min/ Max | Data Rate | | | | Unit | Notes |
|---|----------------------|-------------|------------------------|------|------|------|----------|-------|
| | | | 1600 | 3200 | 3733 | 4267 | | |
| Valid clock requirement after CKE Input LOW | t_{CKELCK} | Min | MAX(5ns, 5nCK) | | | | t_{CK} | |
| Data setup for V_{REF} training mode | $t_{DStrain}$ | Min | 2 | | | | ns | |
| Data hold for V_{REF} training mode | $t_{DHtrain}$ | Min | 2 | | | | ns | |
| Asynchronous data read | t_{ADR} | Max | 20 | | | | ns | |
| CA BUS TRAINING command-to-command delay | t_{CACD} | Min | RU(t_{ADR}/t_{CK}) | | | | t_{CK} | 1 |
| Valid strobe requirement before CKE LOW | t_{DQSCKE} | Min | 10 | | | | ns | |
| First CA BUS TRAINING command following CKE LOW | t_{CAENT} | Min | 250 | | | | ns | |
| V_{REF} step time – multiple steps | $t_{VREF-ca_LONG}$ | Max | 250 | | | | ns | |
| V_{REF} step time – one step | $t_{VREF-ca_SHORT}$ | Max | 80 | | | | ns | |
| Valid clock requirement before CS HIGH | $t_{CKPRECS}$ | Min | $2t_{CK} + t_{XP}$ | | | | – | |
| Valid clock requirement after CS HIGH | $t_{CKPSTCS}$ | Min | MAX(7.5ns, 5nCK) | | | | – | |
| Minimum delay from CS to DQS toggle in command bus training | t_{CS_VREF} | Min | 2 | | | | t_{CK} | |
| Minimum delay from CKE HIGH to strobe High-Z | $t_{CKEHDQS}$ | Min | 10 | | | | ns | |
| CA bus training CKE HIGH to DQ tri-state | t_{MRZ} | Min | 1.5 | | | | ns | |
| ODT turn-on latency from CKE | $t_{CKELODTon}$ | Min | 20 | | | | ns | |
| ODT turn-off latency from CKE | $t_{CKEHODT-off}$ | Min | 20 | | | | ns | |

Note: 1. If t_{CACD} is violated, the data for samples that violate t_{CACD} will not be available, except for the last sample (where t_{CACD} after this sample is met). Valid data for the last sample will be available after t_{ADR} .


Table 185: Asynchronous ODT Turn On and Turn Off Timing

| Symbol | 800–2133 MHz | Unit |
|------------------|--------------|------|
| $t_{ODTon,min}$ | 1.5 | ns |
| $t_{ODTon,max}$ | 3.5 | ns |
| $t_{ODToff,min}$ | 1.5 | ns |
| $t_{ODToff,max}$ | 3.5 | ns |

Table 186: Temperature Derating Parameters

| Parameter | Symbol | Min/ Max | Data Rate | | | | Unit |
|---|--------------|-------------|-------------------|------|------|------|------|
| | | | 1600 | 3200 | 3733 | 4267 | |
| DQS output access time from CK_t/ CK_c (derated) | t_{DQSCKd} | Max | 3600 | | | | ps |
| RAS-to-CAS delay (derated) | t_{RCDd} | Min | $t_{RCD} + 1.875$ | | | | ns |
| ACTIVATE-to-ACTIVATE command pe- riod (same bank, derated) | t_{RCd} | Min | $t_{RC} + 3.75$ | | | | ns |
| Row active time (derated) | t_{RASd} | Min | $t_{RAS} + 1.875$ | | | | ns |
| Row precharge time (derated) | t_{RPd} | Min | $t_{RP} + 1.875$ | | | | ns |
| Active bank A to active bank B (derat- ed) | t_{RRD} | Min | $t_{RRD} + 1.875$ | | | | ns |

Note: 1. Timing derating applies for the operation at 85°C to 105°C.



CA Rx Voltage and Timing

The command and address (CA), including CS input receiver compliance mask for voltage and timing, is shown in the CA Receiver (Rx) Mask figure below. All CA and CS signals apply the same compliance mask and operate in single data rate mode.

The CA input Rx mask for voltage and timing is applied across all pins, as shown in the figure below. The Rx mask defines the area that the input signal must not encroach if the DRAM input receiver is expected to successfully capture a valid input signal; it is not the valid data eye.

Figure 163: CA Receiver (Rx) Mask

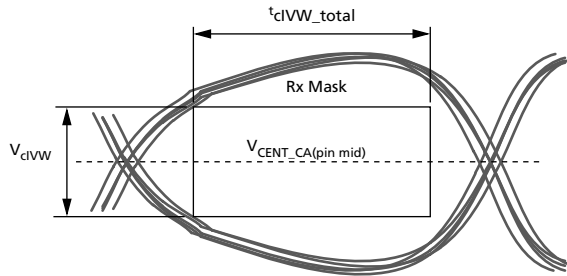
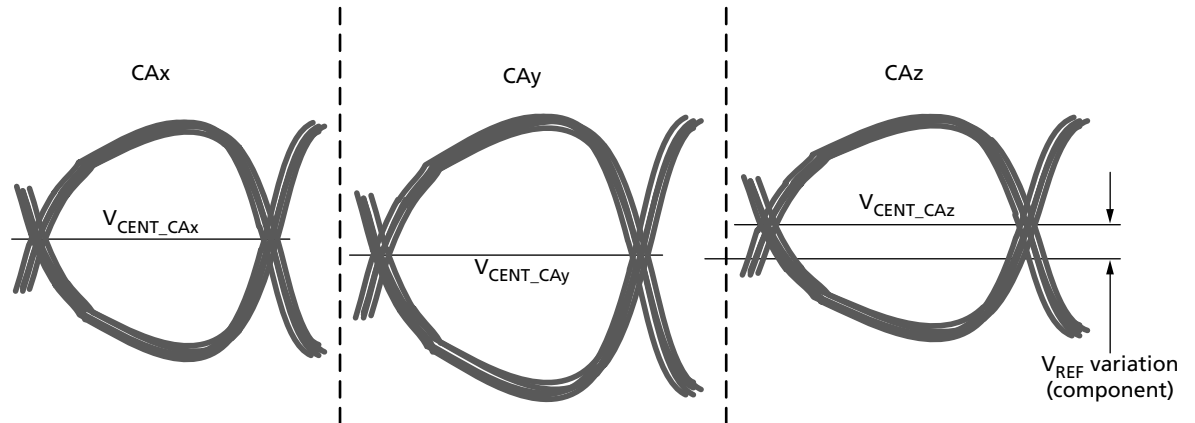
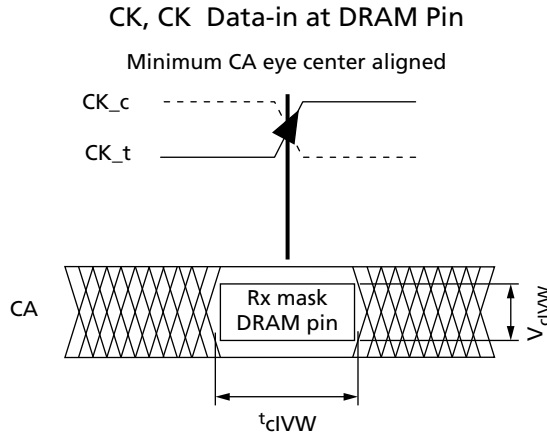


Figure 164: Across Pin V_{REF} (CA) Voltage Variation



$V_{CENT_CA(pin\ mid)}$ is defined as the midpoint between the largest V_{CENT_CA} voltage level and the smallest V_{CENT_CA} voltage level across all CA and CS pins for a given DRAM component. Each CA V_{CENT} level is defined by the center, which is, the widest opening of the cumulative data input eye, as depicted in the figure above. This clarifies that any DRAM component level variation must be accounted for within the CA Rx mask. The component-level V_{REF} will be set by the system to account for R_{ON} and ODT settings.

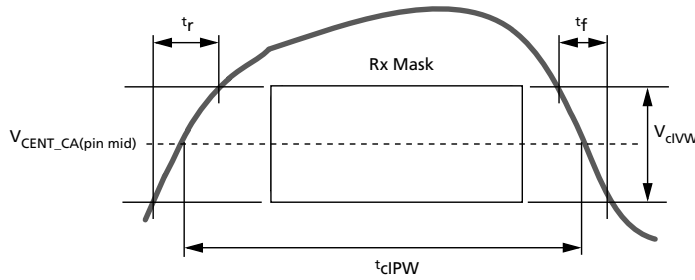
Figure 165: CA Timings at the DRAM Pins



t_{cIVW} for all CA signals is defined as centered on the CK_t/CK_c crossing at the DRAM pin.

Note: 1. All of the timing terms in above figure are measured from the CK_t/CK_c to the center (midpoint) of the t_{cIVW} window taken at the V_{cIVW_total} voltage levels centered around $V_{CENT_CA(pin\ mid)}$.

Figure 166: CA t_{cIPW} and SRIN_cIVW Definition (for Each Input Pulse)



Note: 1. $SRIN_cIVW = V_{dIVW_total} / (t_r \text{ or } t_f)$; signal must be monotonic within t_r and t_f range.

Figure 167: CA V_{IHL_AC} Definition (for Each Input Pulse)

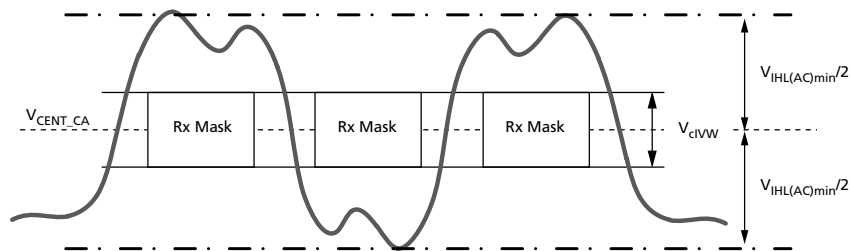



Table 187: DRAM CMD/ADR, CS
 $UI = t_{CK(AVG)MIN}$

| Symbol | Parameter | DQ – 1333 ⁷ | | DQ – 1600/1867 | | DQ – 3200/3733 | | DQ – 4267 | | Unit | Notes |
|---------------|--|------------------------|-----|----------------|-----|----------------|-----|-----------|-----|------|---------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | | |
| V_{cIVW} | Rx mask voltage peak-to-peak | – | 175 | – | 175 | – | 155 | – | 145 | mV | 1, 2, 3 |
| $V_{IHL(AC)}$ | CA AC input pulse amplitude peak-to-peak | 210 | – | 210 | – | 190 | – | 180 | – | mV | 4, 6 |
| SRIN_cIVW | Input slew rate over V_{cIVW} | 1 | 7 | 1 | 7 | 1 | 7 | 1 | 7 | V/ns | 5 |

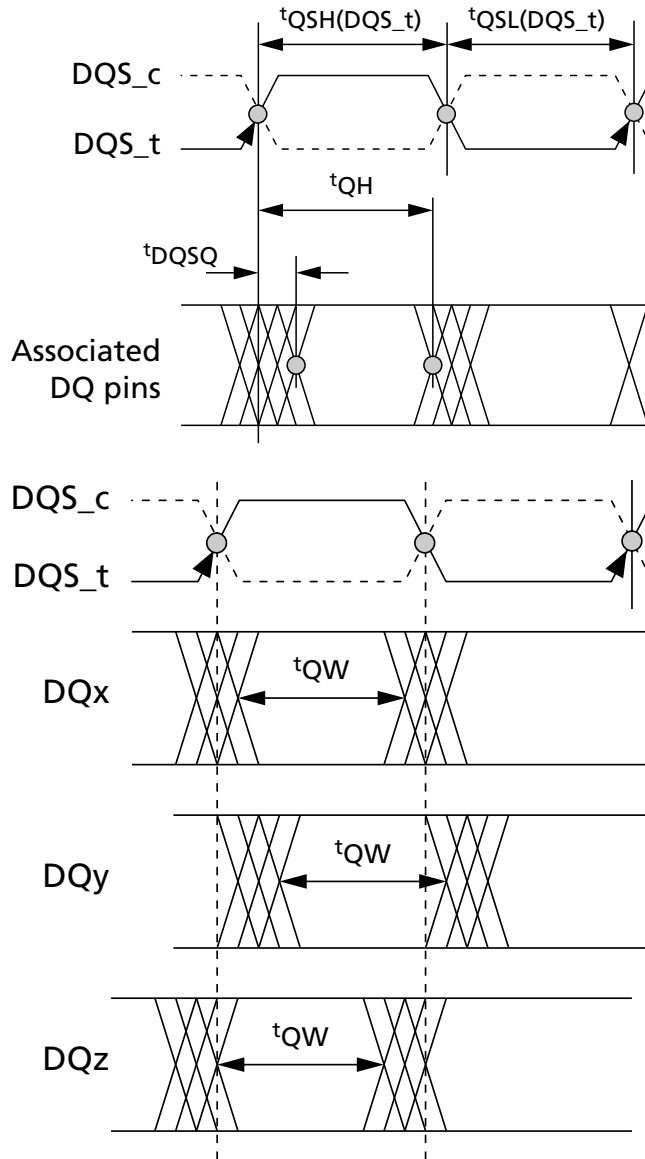
- Notes:
1. CA Rx mask voltage and timing parameters at the pin, including voltage and temperature drift.
 2. Rx mask voltage V_{cIVW} total(MAX) must be centered around $V_{CENT_CA(pin\ mid)}$.
 3. Defined over the CA internal V_{REF} range. The Rx mask at the pin must be within the internal $V_{REF(CA)}$ range irrespective of the input signal common mode.
 4. CA-only input pulse signal amplitude into the receiver must meet or exceed $V_{IHL(AC)}$ at any point over the total UI. No timing requirement above level. $V_{IHL(AC)}$ is the peak-to-peak voltage centered around $V_{CENT_CA(pin\ mid)}$, such that $V_{IHL(AC)}/2$ (MIN) must be met both above and below V_{CENT_CA} .
 5. Input slew rate over V_{cIVW} mask is centered at $V_{CENT_CA(pin\ mid)}$.
 6. $V_{IHL(AC)}$ does not have to be met when no transitions are occurring.
 7. The Rx voltage and absolute timing requirements apply for DQ operating frequencies at or below 1333 for all speed bins. For example the t_{cIVW} (ps) = 450ps at or below 1333 operating frequencies.



DQ Tx Voltage and Timing

DRAM Data Timing

Figure 168: Read Data Timing Definitions – t_{QH} and t_{DQSQ} Across DQ Signals per DQS Group





DQ Rx Voltage and Timing

The DQ input receiver mask for voltage and timing is applied per pin, as shown in the DQ Receiver (Rx) Mask figure below. The total mask (V_{dIVW_total} , $TdIVW_total$) defines the area that the input signal must not encroach in order for the DQ input receiver to successfully capture an input signal. The mask is a receiver property, and it is not the valid data eye.

Figure 169: DQ Receiver (Rx) Mask

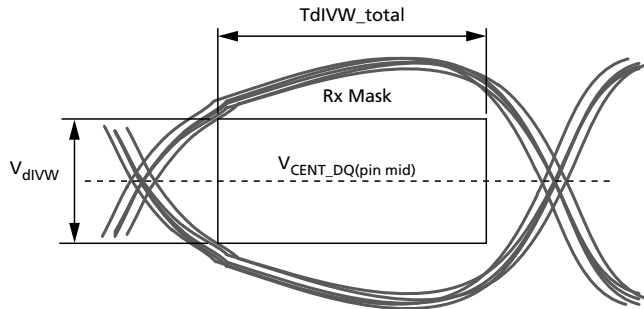
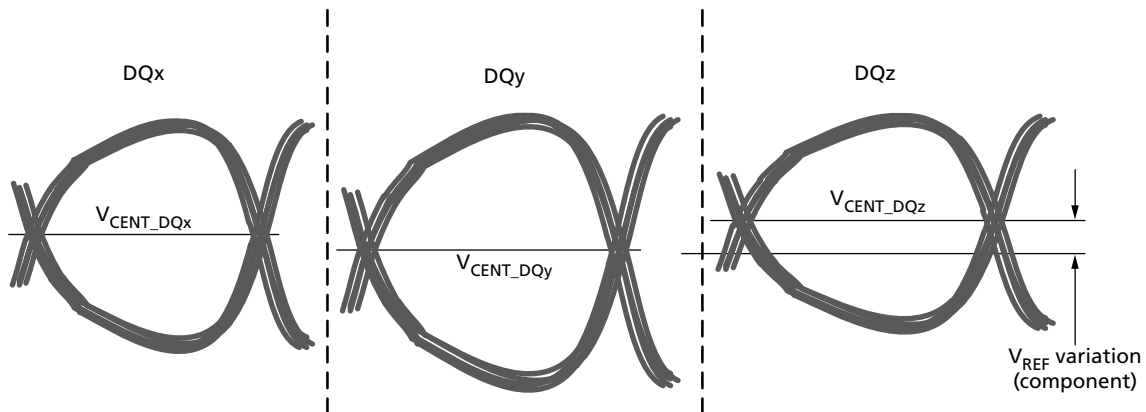


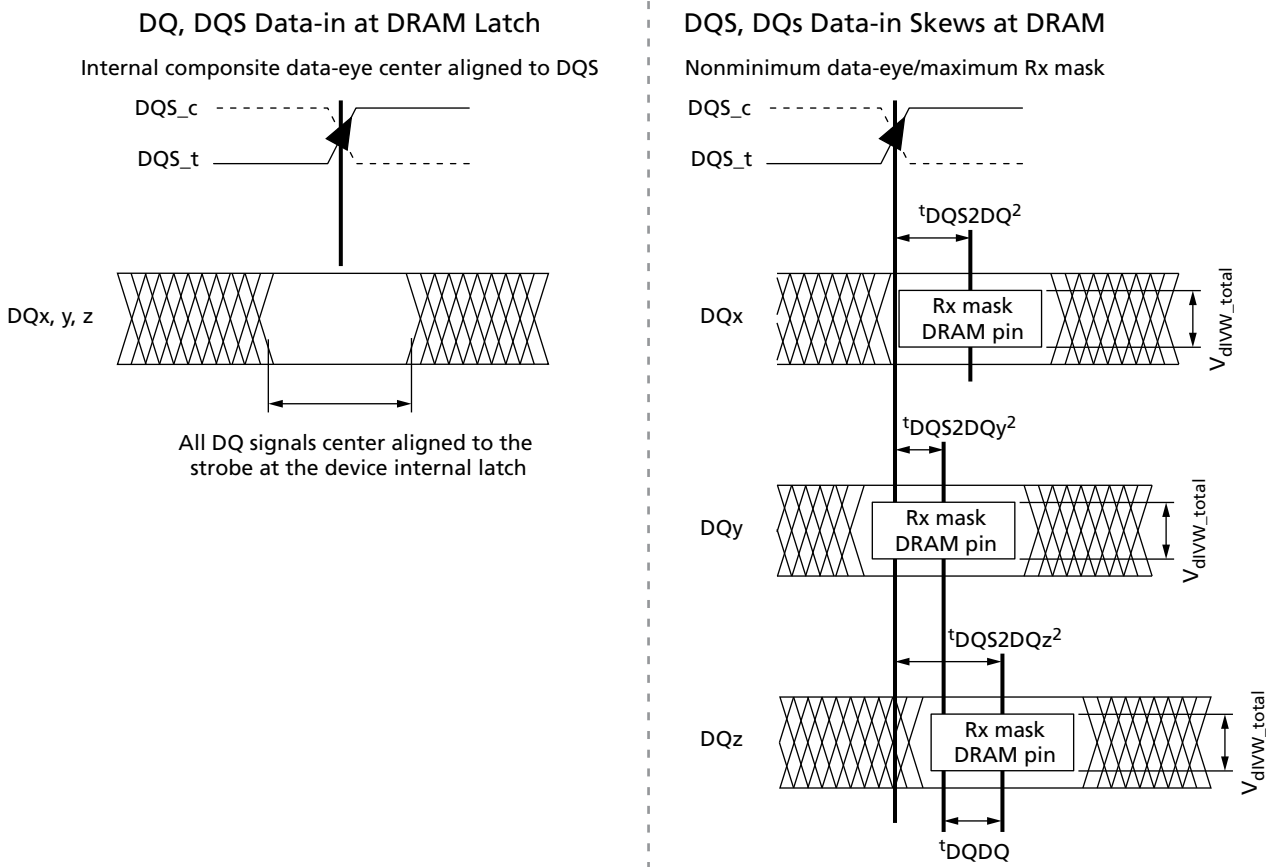
Figure 170: Across Pin V_{REF} DQ Voltage Variation



$V_{CENT_DQ(pin_mid)}$ is defined as the midpoint between the largest V_{CENT_DQ} voltage level and the smallest V_{CENT_DQ} voltage level across all DQ pins for a given DRAM component. Each V_{CENT_DQ} is defined by the center, which is the widest opening of the cumulative data input eye as shown in the figure above. This clarifies that any DRAM component level variation must be accounted for within the DRAM Rx mask. The component-level V_{REF} will be set by the system to account for R_{ON} and ODT settings.



Figure 171: DQ-to-DQS t_{DQS2DQ} and t_{DQDQ}

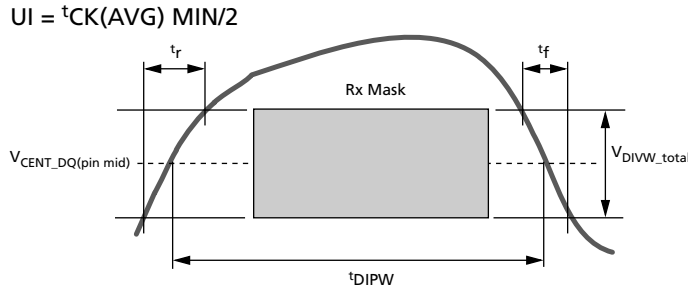


- Notes:
1. These timings at the DRAM pins are referenced from the internal latch.
 2. t_{DQS2DQ} is measured at the center (midpoint) of the TdIVW window.
 3. DQz represents the MAX t_{DQS2DQ} in this example.
 4. DQy represents the MIN t_{DQS2DQ} in this example.

All of the timing terms in DQ to DQS_t are measured from the DQS_t/DQS_c to the center (midpoint) of the TdIVW window taken at the V_{dIVW_total} voltage levels centered around $V_{CENT_DQ(pin_mid)}$. In figure above, the timings at the pins are referenced with respect to all DQ signals center-aligned to the DRAM internal latch. The data-to-data offset is defined as the difference between the MIN and MAX t_{DQS2DQ} for a given component.



Figure 172: DQ t_{DIPW} and SRIN_divW Definition for Each Input Pulse



Note: 1. $SRIN_divW = V_{dIVW_total} / (t_r \text{ or } t_f)$ signal must be monotonic within t_r and t_f range.

Figure 173: DQ $V_{IHL(AC)}$ Definition (for Each Input Pulse)

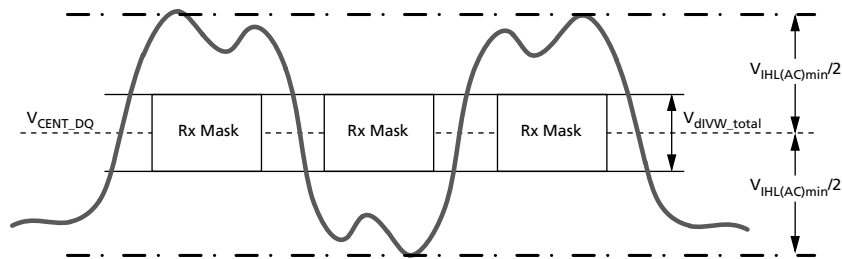


Table 188: DQs In Receive Mode

Note UI = $t_{CK(AVG)}(MIN)/2$

| Symbol | Parameter | 1600/1867 | | 2133/2400 | | 3200/3733 | | 4267 | | Unit | Notes |
|-------------------|--|-----------|-----|-----------|-----|-----------|-----|------|-----|------|---------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | | |
| V_{dIVW_total} | Rx mask voltage – peak-to-peak | – | 140 | – | 140 | – | 140 | – | 120 | mV | 1, 2, 3 |
| $V_{IHL(AC)}$ | DQ AC input pulse amplitude peak-to-peak | 180 | – | 180 | – | 180 | – | 170 | – | mV | 5, 7 |
| SRIN_divW | Input slew rate over V_{dIVW_total} | 1 | 7 | 1 | 7 | 1 | 7 | 1 | 7 | V/ns | 6 |

- Notes:
1. Data Rx mask voltage and timing parameters are applied per pin and include the DRAM DQ-to-DQS voltage AC noise impact for frequencies >20 MHz with a maximum voltage of 45mV peak-to-peak at a fixed temperature on the package. The voltage supply noise must comply to the component MIN/MAX DC operating conditions.
 2. Rx mask voltage $V_{dIVW_total}(MAX)$ must be centered around $V_{CENT_DQ(pin_mid)}$.
 3. Defined over the DQ internal V_{REF} range. The Rx mask at the pin must be within the internal V_{REF} DQ range irrespective of the input signal common mode.
 4. Deterministic component of the total Rx mask voltage or timing. Parameter will be characterized and guaranteed by design.
 5. DQ-only input pulse amplitude into the receiver must meet or exceed $V_{IHL(AC)}$ at any point over the total UI. No timing requirement above level. $V_{IHL(AC)}$ is the peak-to-peak voltage centered around $V_{CENT_DQ(pin_mid)}$, such that $V_{IHL(AC)}/2$ (MIN) must be met both above and below V_{CENT_DQ} .
 6. Input slew rate over V_{dIVW} mask centered at $V_{CENT_DQ(pin_mid)}$.



7. $V_{IHL(AC)}$ does not have to be met when no transitions are occurring.

Clock Specification

The specified clock jitter is a random jitter with Gaussian distribution. Input clocks violating minimum or maximum values may result in device malfunction.

Table 189: Definitions and Calculations

| Symbol | Description | Calculation | Notes |
|-------------------------|--|---|-------|
| $t_{CK(avg)}$ and nCK | <p>The average clock period across any consecutive 200-cycle window. Each clock period is calculated from rising clock edge to rising clock edge.</p> <p>Unit $t_{CK(avg)}$ represents the actual clock average $t_{CK(avg)}$ of the input clock under operation. Unit nCK represents one clock cycle of the input clock, counting from actual clock edge to actual clock edge.</p> <p>$t_{CK(avg)}$ can change no more than $\pm 1\%$ within a 100-clock-cycle window, provided that all jitter and timing specifications are met.</p> | $t_{CK(avg)} = \left(\sum_{j=1}^N t_{CK_j} \right) / N$ <p>Where $N = 200$</p> | |
| $t_{CK(abs)}$ | The absolute clock period, as measured from one rising clock edge to the next consecutive rising clock edge. | | 1 |
| $t_{CH(avg)}$ | The average HIGH pulse width, as calculated across any 200 consecutive HIGH pulses. | $t_{CH(avg)} = \left(\sum_{j=1}^N t_{CH_j} \right) / (N \times t_{CK(avg)})$ <p>Where $N = 200$</p> | |
| $t_{CL(avg)}$ | The average LOW pulse width, as calculated across any 200 consecutive LOW pulses. | $t_{CL(avg)} = \left(\sum_{j=1}^N t_{CL_j} \right) / (N \times t_{CK(avg)})$ <p>Where $N = 200$</p> | |
| $t_{JIT(per)}$ | The single-period jitter defined as the largest deviation of any signal t_{CK} from $t_{CK(avg)}$. | $t_{JIT(per)} = \min/\max \text{ of } \left(t_{CK_i} - t_{CK(avg)} \right)$ <p>Where $i = 1$ to 200</p> | 1 |
| $t_{JIT(per),act}$ | The actual clock jitter for a given system. | | |
| $t_{JIT(per),allowed}$ | The specified clock period jitter allowance. | | |
| $t_{JIT(cc)}$ | The absolute difference in clock periods between two consecutive clock cycles. $t_{JIT(cc)}$ defines the cycle-to-cycle jitter. | $t_{JIT(cc)} = \max \text{ of } \left(t_{CK_{i+1}} - t_{CK_i} \right)$ | 1 |
| $t_{ERR(nper)}$ | The cumulative error across n multiple consecutive cycles from $t_{CK(avg)}$. | $t_{ERR(nper)} = \left(\sum_{j=i}^{i+n-1} t_{CK_j} \right) - (n \times t_{CK(avg)})$ | 1 |
| $t_{ERR(nper),act}$ | The actual clock jitter over n cycles for a given system. | | |


Table 189: Definitions and Calculations (Continued)

| Symbol | Description | Calculation | Notes |
|--------------------------|--|--|-------|
| $t_{ERR(nper), allowed}$ | The specified clock jitter allowance over n cycles. | | |
| $t_{ERR(nper), min}$ | The minimum $t_{ERR(nper)}$. | $t_{ERR(nper), min} = (1 + 0.68LN(n)) \times t_{JIT(per), min}$ | 2 |
| $t_{ERR(nper), max}$ | The maximum $t_{ERR(nper)}$. | $t_{ERR(nper), max} = (1 + 0.68LN(n)) \times t_{JIT(per), max}$ | 2 |
| $t_{JIT(duty)}$ | Defined with absolute and average specifications for t_{CH} and t_{CL} , respectively. | $t_{JIT(duty), min} =$ $\text{MIN}((t_{CH(abs), min} - t_{CH(avg), min}),$ $(t_{CL(abs), min} - t_{CL(avg), min})) \times t_{CK(avg)}$ $t_{JIT(duty), max} =$ $\text{MAX}((t_{CH(abs), max} - t_{CH(avg), max}),$ $(t_{CL(abs), max} - t_{CL(avg), max})) \times t_{CK(avg)}$ | |

- Notes: 1. Not subject to production testing.
 2. Using these equations, $t_{ERR(nper)}$ tables can be generated for each $t_{JIT(per), act}$ value.

$t_{CK(abs)}$, $t_{CH(abs)}$, and $t_{CL(abs)}$

These parameters are specified with their average values; however, the relationship between the average timing and the absolute instantaneous timing (defined in the following table) is applicable at all times.

Table 190: $t_{CK(abs)}$, $t_{CH(abs)}$, and $t_{CL(abs)}$ Definitions

| Parameter | Symbol | Minimum | Unit |
|---------------------------------|----------------|---|-----------------|
| Absolute clock period | $t_{CK(abs)}$ | $t_{CK(avg), min} + t_{JIT(per), min}$ | ps ¹ |
| Absolute clock HIGH pulse width | $t_{CH(abs)}$ | $t_{CH(avg), min} + t_{JIT(duty), min}^2 / t_{CK(avg), min}$ | $t_{CK(avg)}$ |
| Absolute clock LOW pulse width | $t_{CL(abs)}$ | $t_{CL(avg), min} + t_{JIT(duty), min}^2 / t_{CK(avg), min}$ | $t_{CK(avg)}$ |

- Notes: 1. $t_{CK(avg), min}$ is expressed in ps for this table.
 2. $t_{JIT(duty), min}$ is a negative value.

Clock Period Jitter

LPDDR4 devices can tolerate some clock period jitter without core timing parameter derating. This section describes device timing requirements with clock period jitter ($t_{JIT(per)}$) in excess of the values found in the AC Timing table. Calculating cycle time derating and clock cycle derating are also described.

Clock Period Jitter Effects on Core Timing Parameters

Core timing parameters (t_{RCD} , t_{RP} , t_{RTP} , t_{WR} , t_{WRA} , t_{WTR} , t_{RC} , t_{RAS} , t_{RRD} , t_{FAW}) extend across multiple clock cycles. Clock period jitter impacts these parameters when measured in numbers of clock cycles. Within the specification limits, the device is characterized and verified to support $t_{nPARAM} = RU[t_{PARAM} / t_{CK(avg)}]$. During device operation where clock jitter is outside specification limits, the number of clocks, or $t_{CK(avg)}$, may need to be increased based on the values for each core timing parameter.



Cycle Time Derating for Core Timing Parameters

For a given number of clocks (t_{nPARAM}), when $t_{CK(avg)}$ and $t_{ERR}(t_{nPARAM},act)$ exceed $t_{ERR}(t_{nPARAM},allowed)$, cycle time derating may be required for core timing parameters.

$$\text{CycleTimeDerating} = \max\left\{\left\{\frac{t_{PARAM} + t_{ERR}(t_{nPARAM},act) - t_{ERR}(t_{nPARAM},allowed)}{t_{nPARAM}} - t_{CK(avg)}\right\}, 0\right\}$$

Cycle time derating analysis should be conducted for each core timing parameter. The amount of cycle time derating required is the maximum of the cycle time deratings determined for each individual core timing parameter.

Clock Cycle Derating for Core Timing Parameters

For each core timing parameter and a given number of clocks (t_{nPARAM}), clock cycle derating should be specified with $t_{JIT(per)}$.

For a given number of clocks (t_{nPARAM}), when $t_{CK(avg)}$ plus $t_{ERR}(t_{nPARAM},act)$ exceed the supported cumulative $t_{ERR}(t_{nPARAM},allowed)$, derating is required. If the equation below results in a positive value for a core timing parameter (t_{CORE}), the required clock cycle derating will be that positive value (in clocks).

$$\text{ClockCycleDerating} = RU \left\{ \frac{t_{PARAM} + t_{ERR}(t_{nPARAM},act) - t_{ERR}(t_{nPARAM},allowed)}{t_{CK(avg)}} \right\} - t_{nPARAM}$$

Cycle-time derating analysis should be conducted for each core timing parameter.

Clock Jitter Effects on Command/Address Timing Parameters

Command/address timing parameters (t_{IS} , t_{IH} , t_{ISb} , t_{IHb}) are measured from a command/address signal (CS or CA[5:0]) transition edge to its respective clock signal (CK_t/CK_c) crossing. The specification values are not affected by the $t_{JIT(per)}$ applied, because the setup and hold times are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values must be met.

Clock Jitter Effects on READ Timing Parameters

t_{RPRE}

When the device is operated with input clock jitter, t_{RPRE} must be derated by the $t_{JIT(per),act,max}$ of the input clock that exceeds $t_{JIT(per),allowed,max}$. Output deratings are relative to the input clock:

$$t_{RPRE}(min,derated) = 0.9 - \left(\frac{t_{JIT(per),act,max} - t_{JIT(per),allowed,max}}{t_{CK(avg)}} \right)$$

For example, if the measured jitter into a LPDDR4 device has $t_{CK(avg)} = 625ps$, $t_{JIT(per),act,min} = -xx$, and $t_{JIT(per),act,max} = +xx$ ps, then $t_{RPRE,min,derated} = 0.9 - (t_{JIT(per),act,max} - t_{JIT(per),allowed,max}) / t_{CK(avg)} = 0.9 - (xx - xx) / xx = yy$ $t_{CK(avg)}$.


 $t_{LZ(DQ)}$, $t_{HZ(DQ)}$, t_{DQSCK} , $t_{LZ(DQS)}$, $t_{HZ(DQS)}$

These parameters are measured from a specific clock edge to a data signal transition (DM_n or DQ_m , where: $n = 0, 1$; and $m = 0-15$, and specified timings must be met with respect to that clock edge. Therefore, they are not affected by $t_{JIT(per)}$.

 t_{QSH} , t_{QSL}

These parameters are affected by duty cycle jitter, represented by $t_{CH(abs)min}$ and $t_{CL(abs)min}$. These parameters determine the absolute data-valid window at the device pin. The absolute minimum data-valid window at the device pin = $\text{MIN} \{ (t_{QSH(abs)min} - t_{DQSQmax}), (t_{QSL(abs)min} - t_{DQSQmax}) \}$. This minimum data valid window must be met at the target frequency regardless of clock jitter.

 t_{RPST}

t_{RPST} is affected by duty cycle jitter, represented by $t_{CL(abs)}$. Therefore, $t_{RPST(abs)min}$ can be specified by $t_{CL(abs)min}$. $t_{RPST(abs)min} = t_{CL(abs)min} - 0.05 = t_{QSL(abs)min}$.

Clock Jitter Effects on WRITE Timing Parameters
 t_{DS} , t_{DH}

These parameters are measured from a data signal (DM_n or DQ_m , where $n = 0, 1$ and $m = 0-15$) transition edge to its respective data strobe signal (DQS_n_t , DQS_n_c ; $n = 0, 1$) crossing. The specification values are not affected by the amount of $t_{JIT(per)}$ applied, because the setup and hold times are relative to the data strobe signal crossing that latches the command/address. Regardless of clock jitter values, these values must be met.

 t_{DSS} , t_{DSH}

These parameters are measured from a data signal (DQS_t , DQS_n_c) crossing to its respective clock signal (CK_t , CK_c) crossing. When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{JIT(per)act}$ of the input clock in excess of the allowed period jitter $t_{JIT(per)allowed}$.

 t_{DQSS}

t_{DQSS} is measured from a data strobe signal (DQS_n_t , DQS_n_c) crossing to its respective clock signal (CK_t , CK_c) crossing. When the device is operated with input clock jitter, this parameter must be derated by the actual $t_{JIT(per),act}$ of the input clock in excess of $t_{JIT(per)allowed}$.

$$t_{DQSS(min,derated)} = 0.75 - \left(\frac{t_{JIT(per),act,min} - t_{JIT(per),allowed,min}}{t_{CK(avg)}} \right)$$

$$t_{DQSS(max,derated)} = 1.25 - \left(\frac{t_{JIT(per),act,max} - t_{JIT(per),allowed,max}}{t_{CK(avg)}} \right)$$

For example, if the measured jitter into an LPDDR4 device has $t_{CK(avg)} = 625\text{ps}$, $t_{JIT(per),act,min} = -xx\text{ps}$, and $t_{JIT(per),act,max} = +xx\text{ps}$, then:

$$t_{DQSS(min,derated)} = 0.75 - (-xx + yy)/625 = xxxx t_{CK(avg)}$$

$$t_{DQSS(max,derated)} = 1.25 - (xx - yy)/625 = xxxx t_{CK(avg)}$$



Revision History

Rev. E – 7/18

- Added Important Notes and Warnings section for further clarification aligning to industry standards

Rev. D – 3/17

- Added QDP die
- Added DS, DT, and NQ package codes
- Added XT temperature range

Rev. C – 11/16

- Added -053 speed grade

Rev. B – 8/16

- Production release

Rev. A – 5/16

- Initial Preliminary release (reference document: PDF: 09005aef865c23a1366b_z0am_qdp_mobile_lpddr4.pdf – Rev. B 3/16 EN)

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.