



- Class: DRAM_BANK0 Net Class
- Class: DRAM_BANK1 Net Class
- Class: DRAM_BANK2 Net Class
- Class: DRAM_BANK3 Net Class

Clock terminators: Place at end of route at each DDR pair

DESIGN NOTE:
DRAM_SDCKE0 no longer requires external 10kΩ resistors to GND to minimize current draw during deep sleep mode (DSM). We keep the option to stay compatible with old CPU resistors.

DESIGN NOTE:
DDR_VREF voltage is generated by PMIC controller by default. To use resistor divider instead, do not fit RES 0 (Ohm) on (pin31 vrefddr) and fit resistor divider

Project:	*
File:	[H] -iMX6_DDR3.SchDoc
Date:	27.06.2019
Designed by:	
Rev:	1.0
Sheet:	8 of 14

