## Excerpt from i.MX 7 Dual Applications Processor Reference Manual

### 6.2.4.3 Power mode transitions

Table 6-8. Power mode transitions

| Power mode | Configuration with external PMIC | Configuration with internal PMIC |
|---|---|---|
| ON, first time | 1. Either coin cell or SoC power supply is connected to SNVS.<br>2. When button is pressed, PMIC powers on. | 1. Either coin cell or SoC power supply is connected to SNVS.<br>2. When button is pressed, 'idle' goes ON. PMIC_ON_REQ goes '1'.<br>3. External regulator is enabled. |
| Normal ON to OFF, by button | 1. Button is pressed for a short duration on the external PMIC.<br>2. Interrupt request (irq) is sent to SoC from external PMIC.<br>3. SoC is programming PMIC for power off when standby is asserted. asserted. PMIC gates SoC supplies. | 1. SoC button is pressed for a short duration.<br>2. Interrupt request (irq) is sent to SoC from FSM.<br>3. Alarm timer is set up by software routine and started.<br>4. Upon alarm_in assertion to '1', PMIC_ON_REQ goes '0'. |
| Emergency ON to OFF, by button | 1. Button is pressed for an extended time on the external PMIC.<br>2. PMIC is powering off. | 1. Button is pressed for longer than 5 seconds on the SoC.<br>2. FSM validates button pressed for 5 seconds.<br>3. Emergency power off is logged. PMIC_ON_REQ goes '0', alarm_mask goes '1'.<br>4. External regulator goes OFF. |
| OFF to ON, by button | 1. Button is pressed on the external PMIC.<br>2. PMIC powers ON. | 1. Button is pressed on the SoC.<br>2. PMIC_ON_REQ goes '1', alarm_mask goes '0'.<br>3. External regulator powers ON. |
| OFF to ON, by timer alarm | 1. Timer alarm in SNVS is programmed by software before SoC goes OFF.<br>2. SoC enters OFF mode.<br>3. Upon timer limit, wake up alarm goes '0'. PMIC_ON_REQ goes '1'.<br>4. PMIC receives assertion of PMIC_ON_REQ and wakes up. | 1. Timer alarm in SNVS is programmed by software before SoC goes OFF.<br>2. SoC enters OFF mode.<br>3. Upon timer limit, wake up alarm goes '0'. PMIC_ON_REQ goes '1'.<br>4. External regulator is enabled by PMIC_ON_REQ = 1. |

not support?

only configuration with external PMIC ?

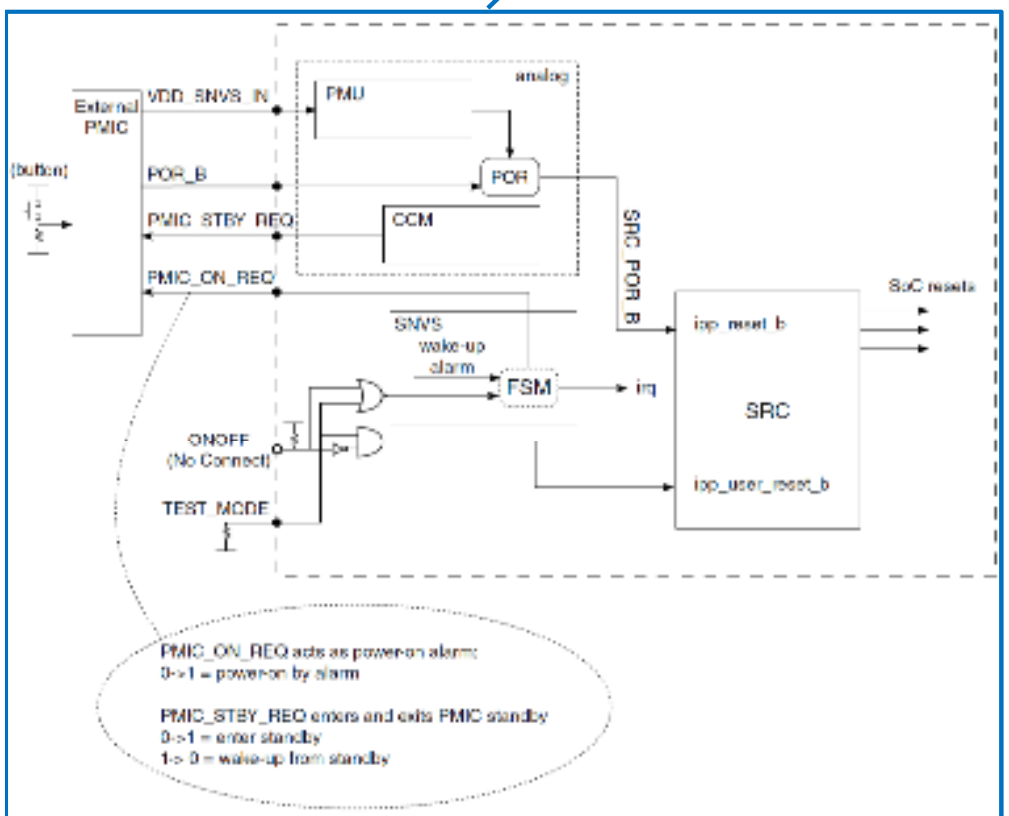


Figure 6-5. Chip reset scheme under external PMIC control

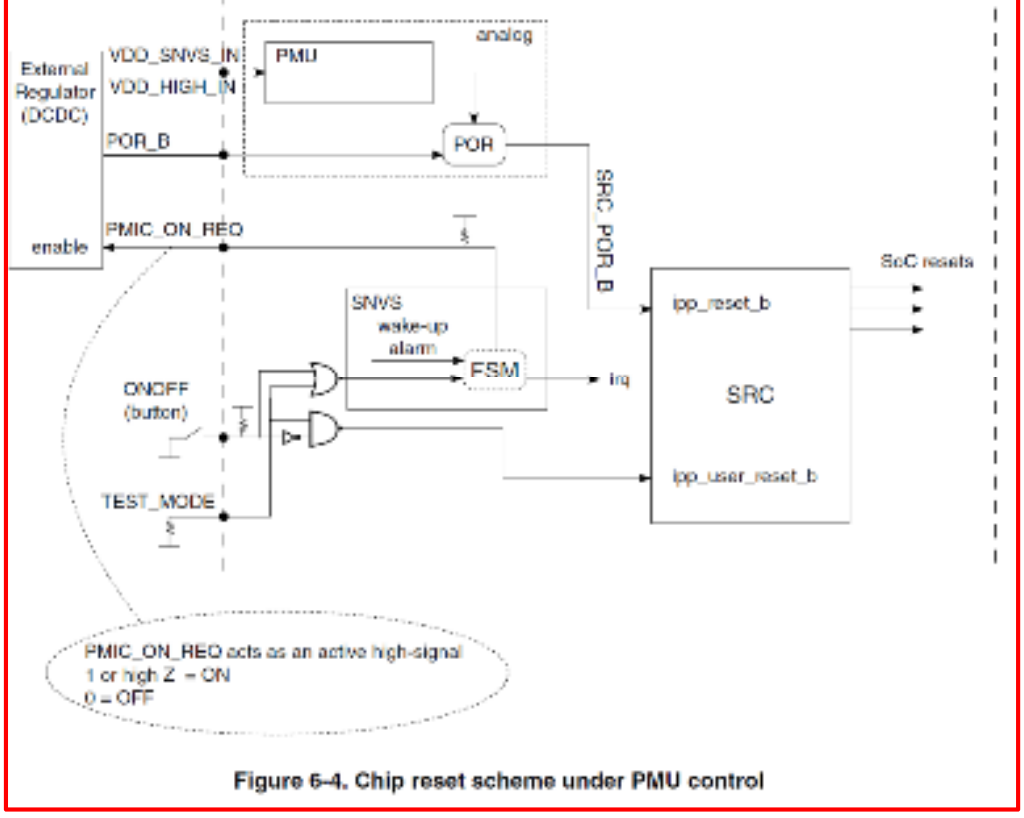


Figure 6-4. Chip reset scheme under PMU control

## Excerpt from the schematic of sch-28590_i.mx7d_saber_rev_d