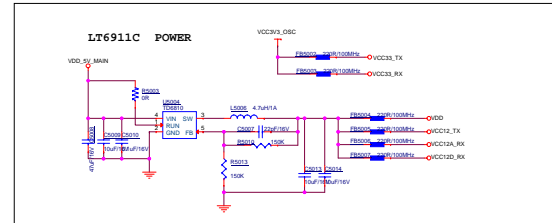
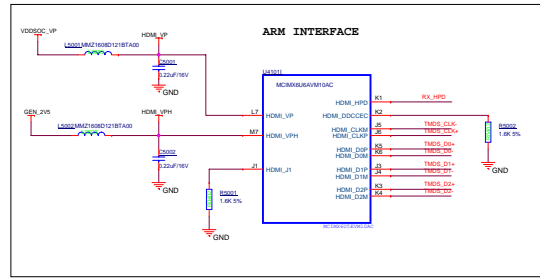
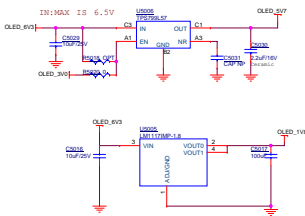
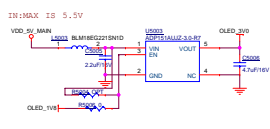
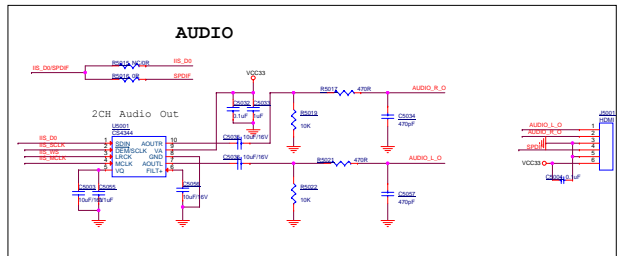
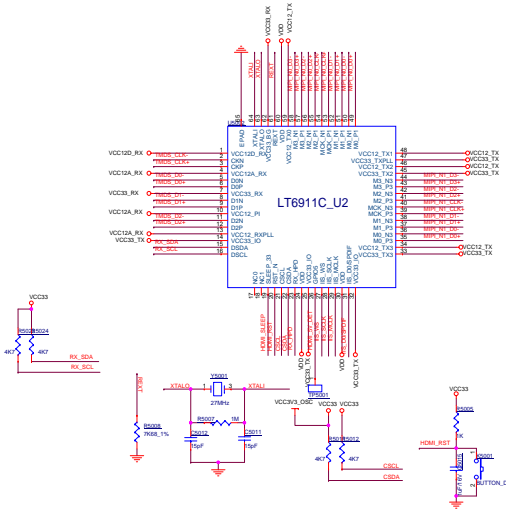
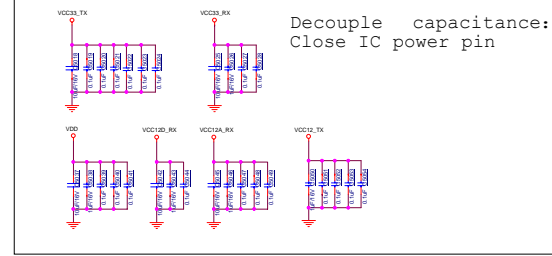


OLED POWER



Decouple capacitance:
Close IC power pin



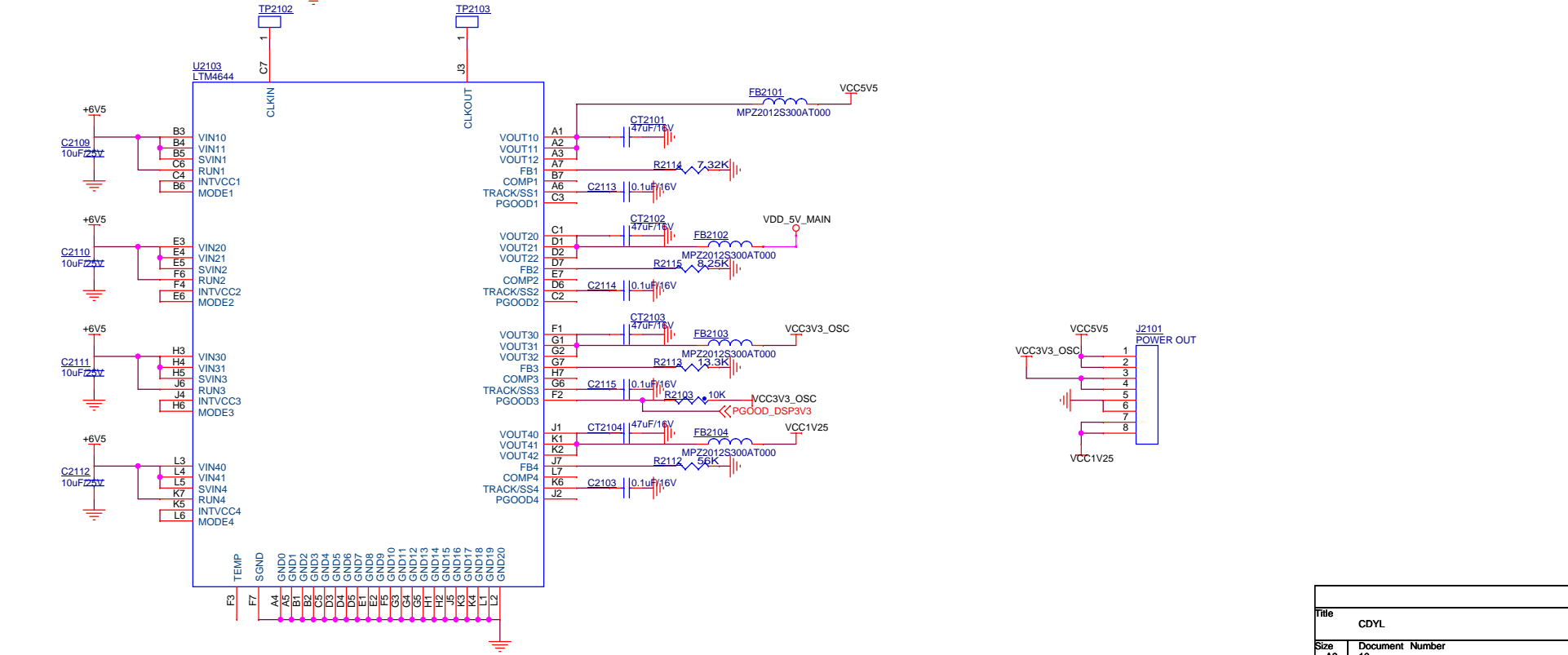
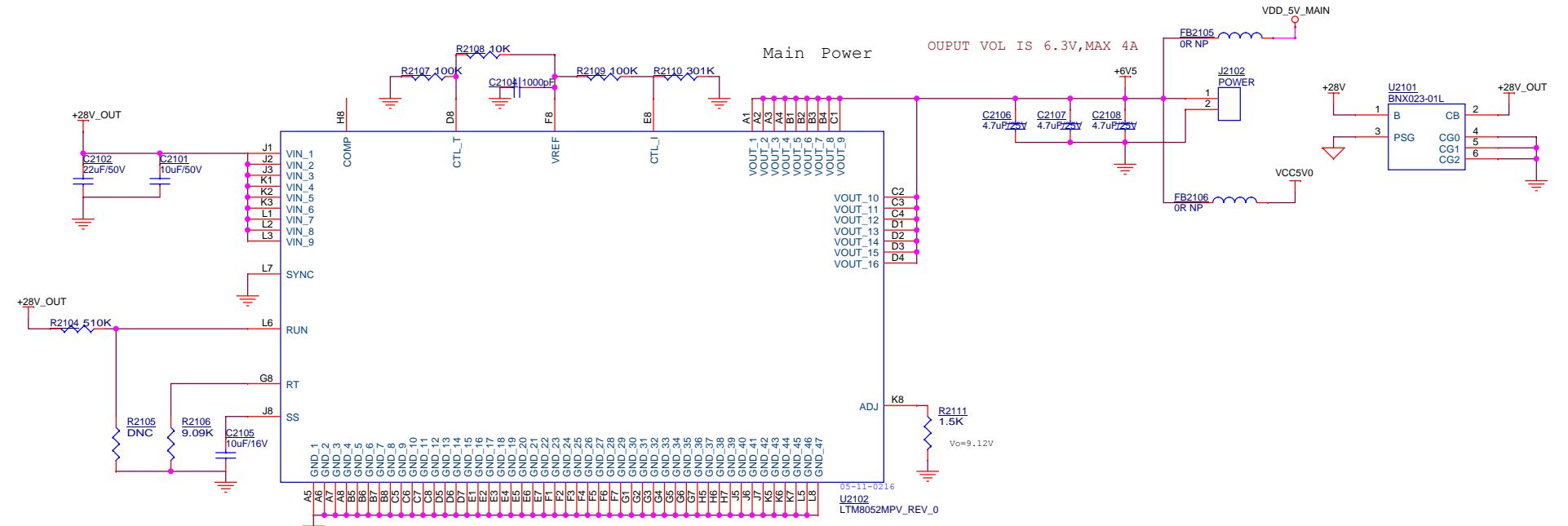
LT6911C



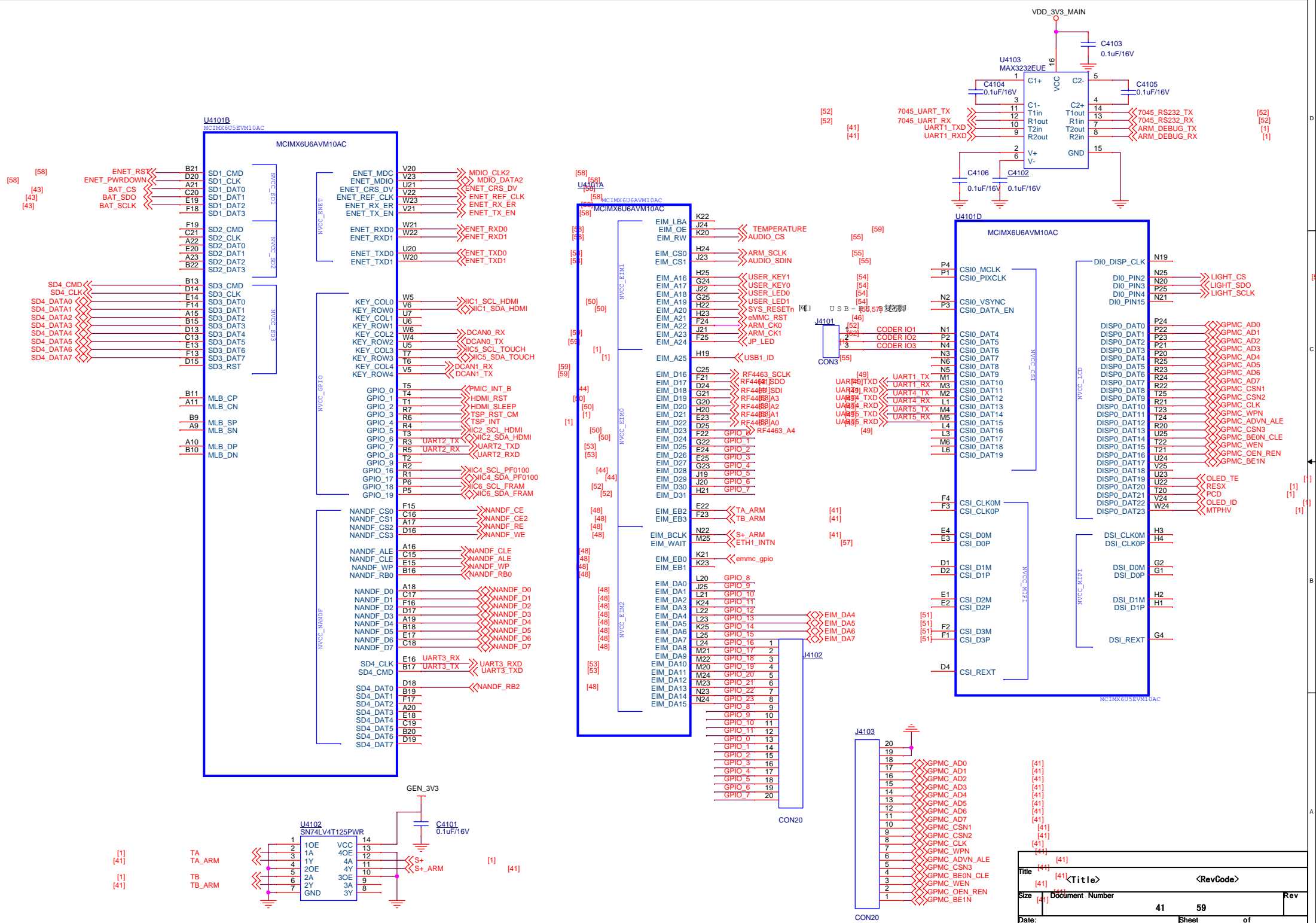
MIPI OUT



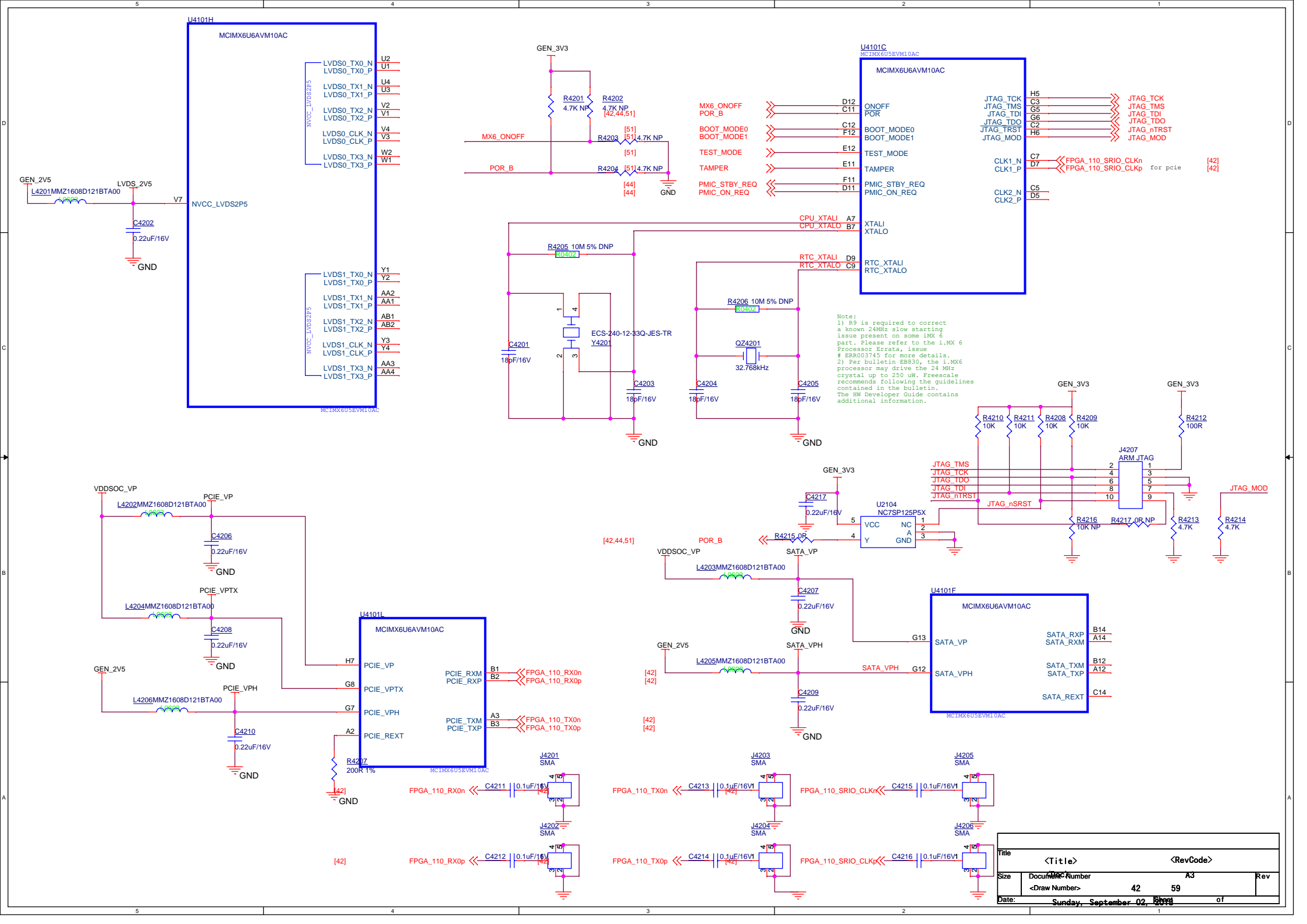
H enter sleep mode
L exit sleep mode



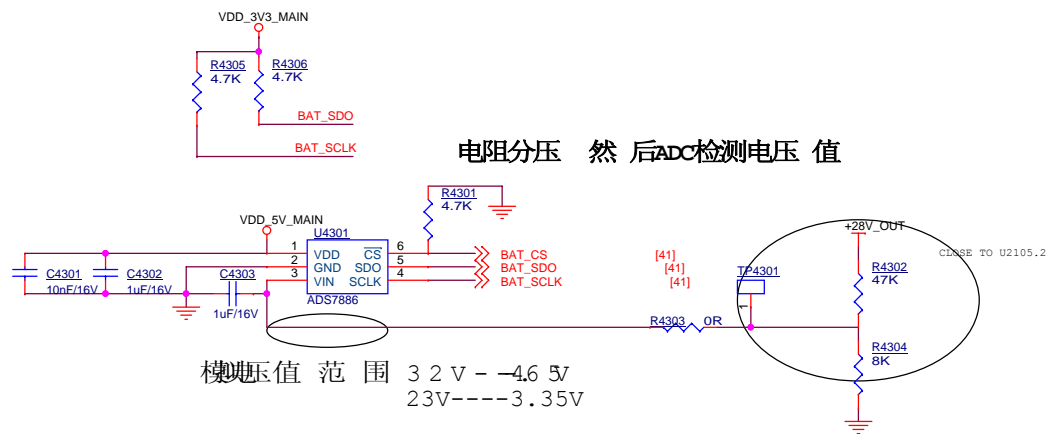
Title			CDYL
Size	Document Number	Rev	
A3	10	v0.1	
Date:	Monday, September 03, 2018	Sheet	21 of 59



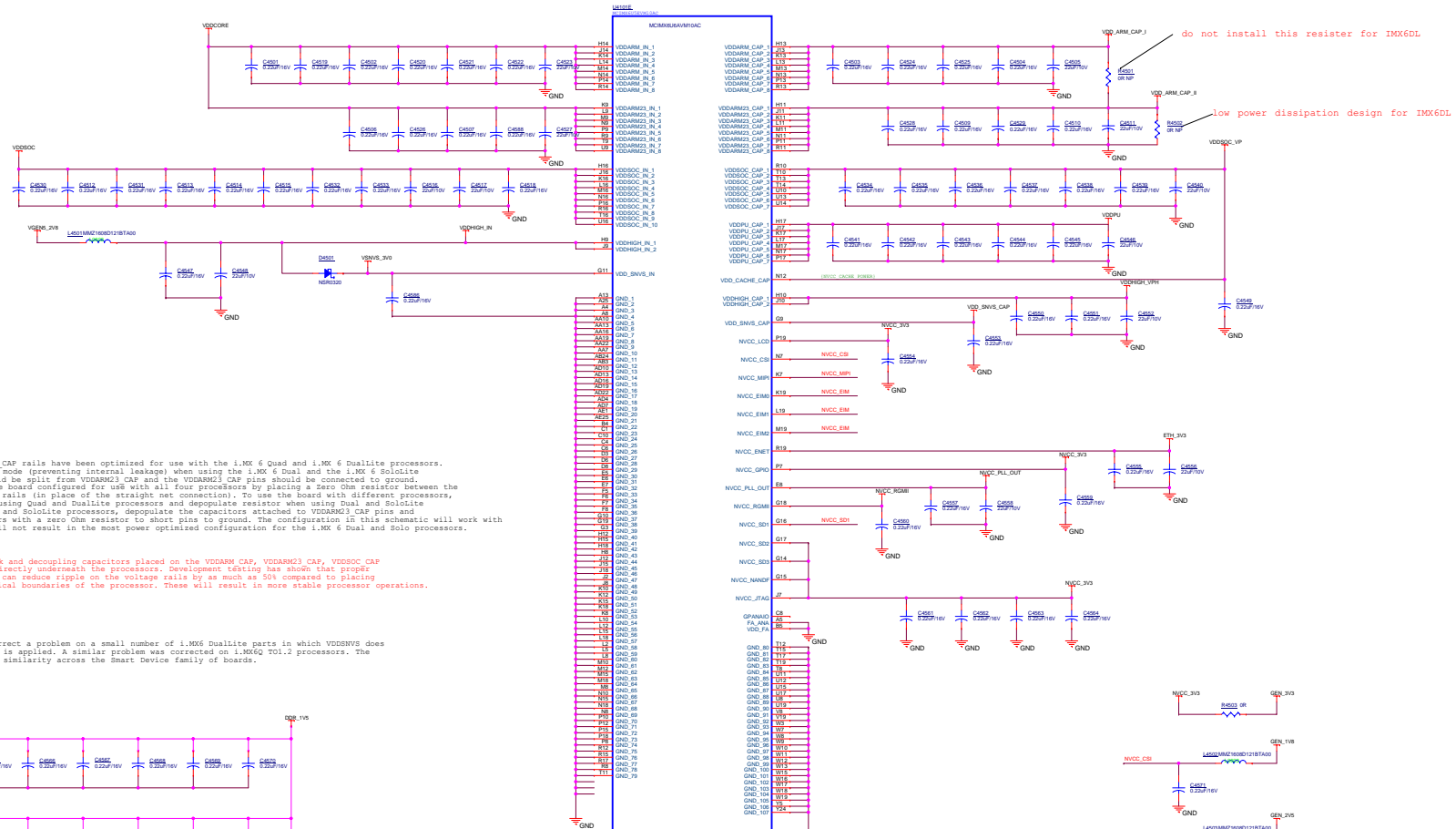
Title	[44]	[41]	<Title>	<RevCode>
Size	[41]	[41]	Document Number	41 59
Date:	[41]	[41]		Sheet of



Title		<Title>		<RevCode>	
Size	Document Number	A3		Rev	
	<Draw Number>	42		59	
Date:	Sunday, September 02, 2012				



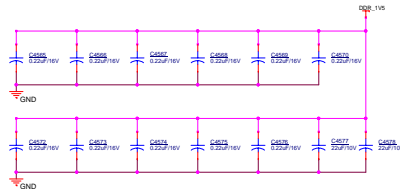
Title		<Title>		<RevCode>	
Size	Document Number	43	59	Rev	
Date:	Sunday, September 02, 2013				



NOTE:
 The VDDARM_CAP and VDDARM2_CAP rails have been optimized for use with the i.MX 6 Quad and i.MX 6 Dualite processors. To achieve the lowest power mode (preventing internal leakage) when using the i.MX 6 Dual and the i.MX 6 SoloLite processors, VDDARM_CAP should be split from VDDARM2_CAP and the VDDARM2_CAP pins should be connected to ground. This can be done on a single board configured for use with all four processors by placing a zero Ohm resistor between the VDDARM_CAP and VDDARM2_CAP rails (in place of the straight net connection). To use the board with different processors, populate the resistor when using Quad and Dualite processors and depopulate resistor when using Dual and SoloLite processors. When using Dual and SoloLite processors, depopulate the capacitors attached to VDDARM2_CAP pins and replace one of the capacitors with a zero Ohm resistor to short pins to ground. The configuration in this schematic will work with all four processors, but will not result in the most power optimized configuration for the i.MX 6 Dual and Solo processors.

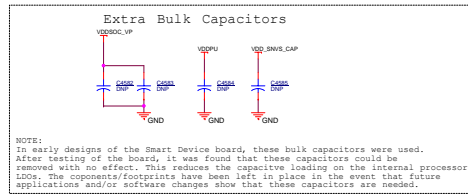
LAYOUT NOTE:
 It is critical that the bulk and decoupling capacitors placed on the VDDARM_CAP, VDDARM2_CAP, VDDSOC_CAP and VDDPU rails be placed directly underneath the processors. Development testing has shown that proper placement of the capacitors can reduce ripple on the voltage rails by as much as 50% compared to placing capacitors outside the physical boundaries of the processor. These will result in more stable processor operations.

NOTE:
 Diode D10 is required to correct a problem on a small number of i.MX6 Dualite parts in which VDDSVNS does not come up when VDDHIGH_IN is applied. A similar problem was corrected on i.MX6Q T01.2 processors. The diode is left populated for similarity across the Smart Device family of boards.

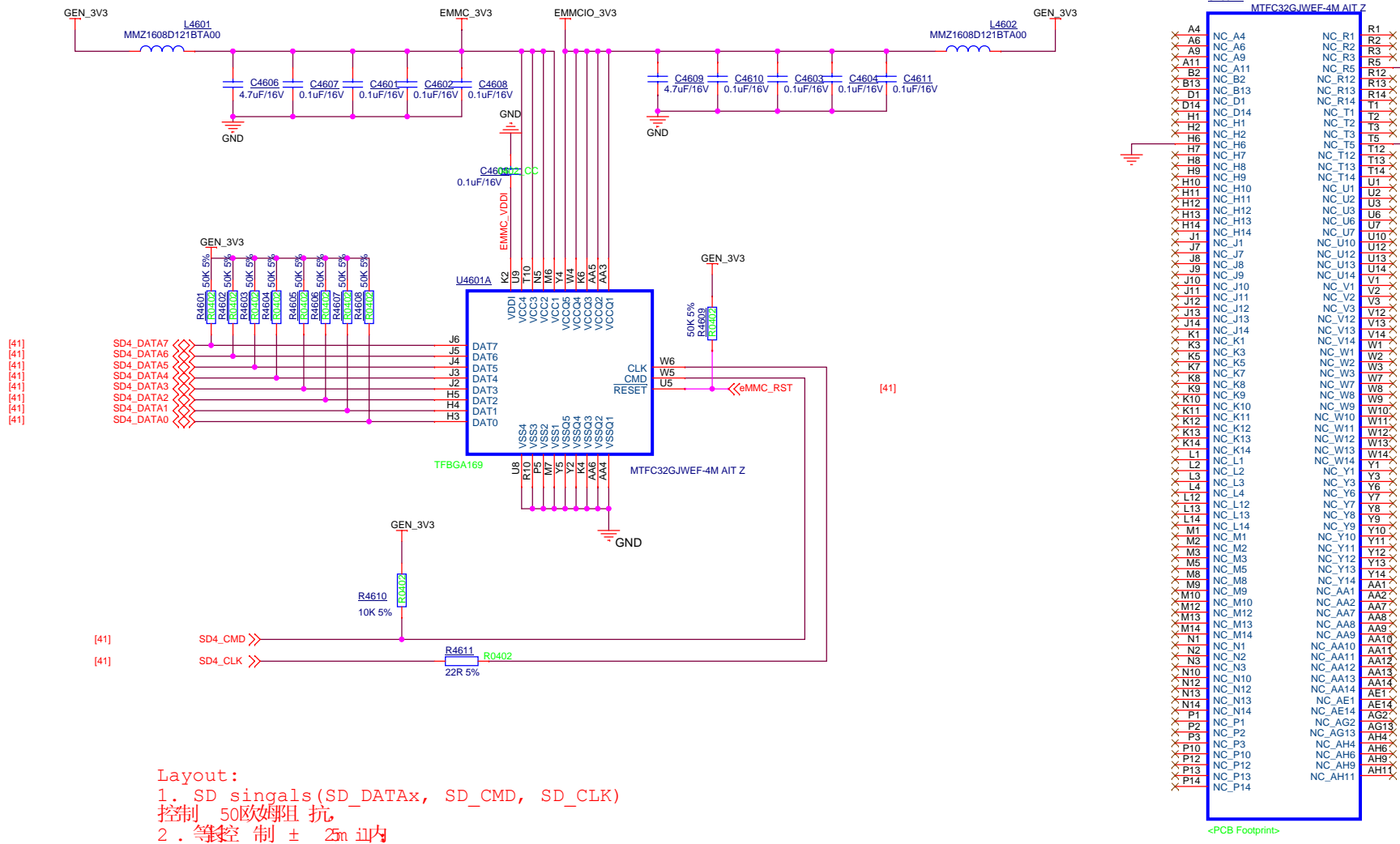


[These capacitors are part of i.MX6 DDR3 Power Domain. They decouple pins shown on Page 4 of these schematics]

NOTE:
 Freescale has validated two different sets of decoupling capacitors and board layouts for use with the i.MX 6 processor. The customer is free to choose the desired decoupling scheme. This scheme uses fewer components. The alternate scheme can be found on the xRD board. Refer to SCR-27142 and LAR-27142.



NOTE:
 In early designs of the Smart Device board, these bulk capacitors were used. After testing of the board, it was found that these capacitors could be removed with no effect. This reduces the capacitive loading on the internal processor I/Os. The components/footprints have been left in place in the event that future applications and/or software changes show that these capacitors are needed.



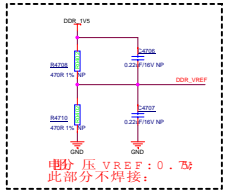
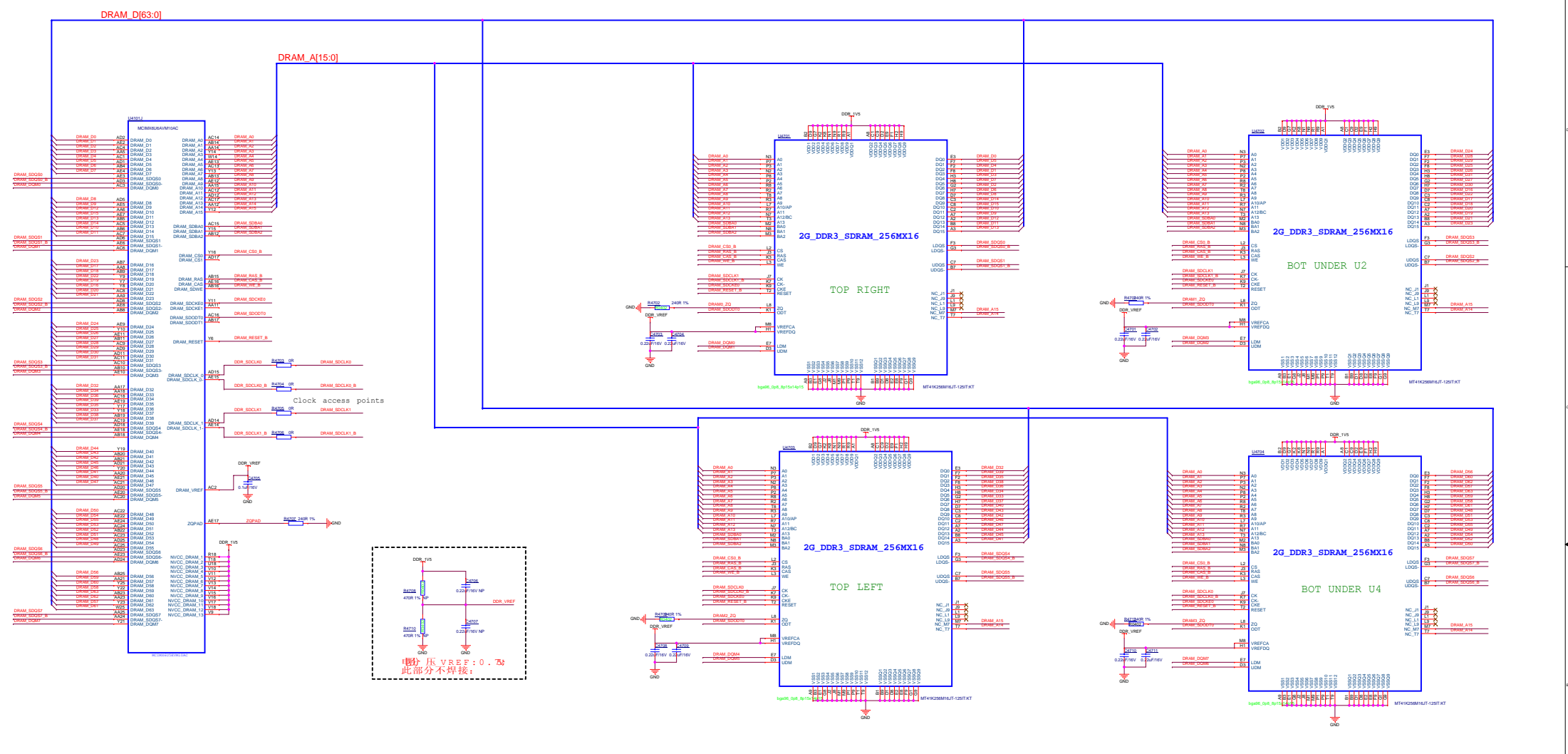
Layout:
 1. SD singals(SD_DATAx, SD_CMD, SD_CLK)
 控制 50欧姆阻抗,
 2. 等控 制 ± 2m il内

U4601B MTF32GJWEF-4M AIT Z

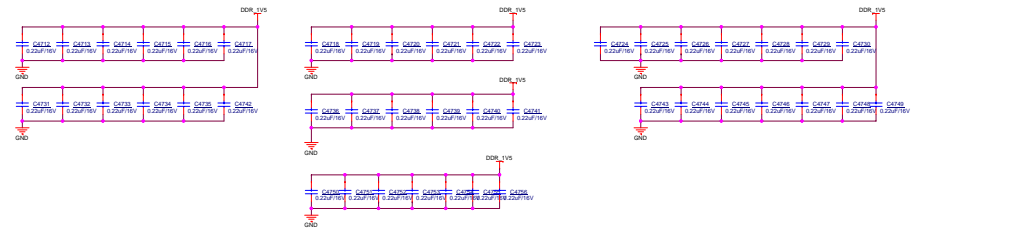
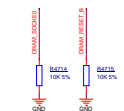
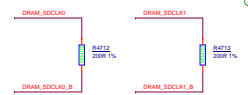
A4	NC_A4	NC_R1	R1
A6	NC_A6	NC_R2	R2
A9	NC_A9	NC_R3	R3
A11	NC_A11	NC_R5	R5
B2	NC_A11	NC_R5	R12
B13	NC_B13	NC_R13	R13
D1	NC_D1	NC_R14	R14
H1	NC_D14	NC_T1	T1
H2	NC_H1	NC_T2	T2
H6	NC_H2	NC_T3	T3
H7	NC_H6	NC_T5	T5
H8	NC_H8	NC_T12	T12
H9	NC_H9	NC_T13	T13
H10	NC_H10	NC_T14	T14
H11	NC_H11	NC_U1	U1
H12	NC_H12	NC_U2	U3
H13	NC_H13	NC_U3	U6
H14	NC_H14	NC_U6	U7
J1	NC_J1	NC_U10	U10
J7	NC_J7	NC_U12	U13
J8	NC_J8	NC_U13	U14
J9	NC_J9	NC_U14	V1
J10	NC_J10	NC_V1	V2
J11	NC_J11	NC_V2	V3
J12	NC_J12	NC_V3	V12
J13	NC_J13	NC_V12	V12
J14	NC_J14	NC_V13	V13
K1	NC_K1	NC_V14	V14
K3	NC_K3	NC_W1	W1
K5	NC_K5	NC_W2	W2
K7	NC_K7	NC_W3	W3
K8	NC_K8	NC_W7	W7
K9	NC_K9	NC_W8	W8
K10	NC_K10	NC_W9	W10
K11	NC_K11	NC_W10	W11
K12	NC_K12	NC_W11	W12
K13	NC_K13	NC_W12	W13
K14	NC_K14	NC_W13	W13
L1	NC_L1	NC_W14	W14
L2	NC_L2	NC_Y1	Y1
L3	NC_L3	NC_Y6	Y6
L4	NC_L4	NC_Y7	Y7
L12	NC_L12	NC_Y7	Y8
L13	NC_L13	NC_Y8	Y9
L14	NC_L14	NC_Y9	Y10
M1	NC_M1	NC_Y10	Y11
M2	NC_M2	NC_Y11	Y12
M3	NC_M3	NC_Y12	Y13
M5	NC_M5	NC_Y13	Y13
M8	NC_M8	NC_Y14	Y14
M9	NC_M9	NC_AA1	AA1
M10	NC_M10	NC_AA2	AA2
M12	NC_M12	NC_AA7	AA7
M13	NC_M13	NC_AA8	AA8
M14	NC_M14	NC_AA9	AA9
N1	NC_N1	NC_AA9	AA10
N2	NC_N2	NC_AA10	AA11
N3	NC_N3	NC_AA11	AA12
N10	NC_N10	NC_AA12	AA13
N12	NC_N12	NC_AA13	AA14
N13	NC_N13	NC_AA14	AE1
N14	NC_N14	NC_AE1	AE14
P1	NC_P1	NC_AG2	AG2
P2	NC_P2	NC_AG13	AG13
P3	NC_P3	NC_AH4	AH4
P10	NC_P10	NC_AH6	AH6
P12	NC_P12	NC_AH9	AH9
P13	NC_P13	NC_AH9	AH11
P14	NC_P14		

<PCB Footprints>

Title		<Title>	<RevCode>
Size	Document Number	A3	Rev
	<Draw Number>	46	59
Date:	Wednesday, September 03, 2014		of

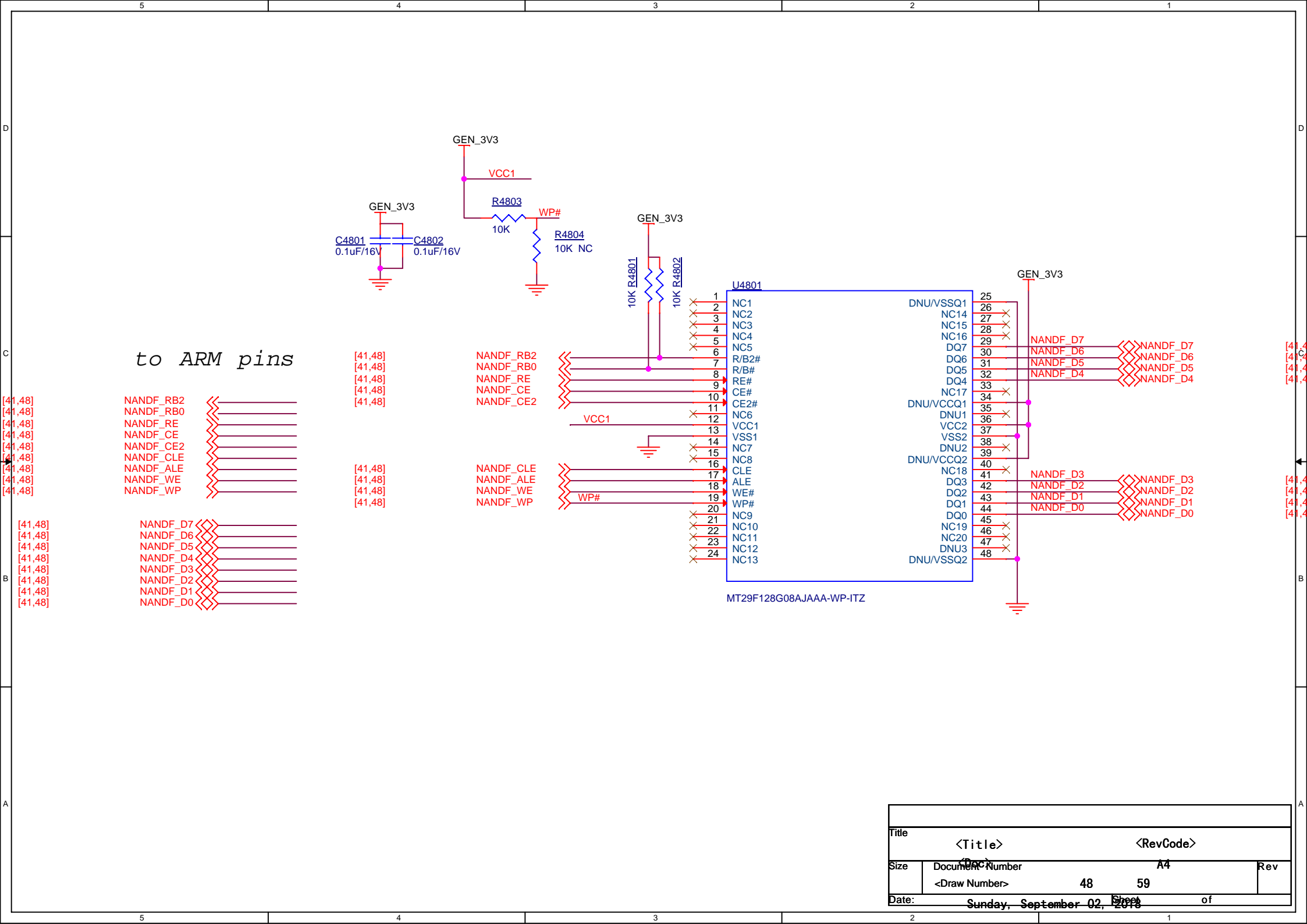


Clock terminators: Place at end of route at each DDR pair
GND probe pads



CLK 的端接电阻值根据拓扑结构而定：
4 片采用 4 个电阻并联 电阻选择 200Ω，并放置中点
4 片采用 Fly-by 电阻并联 电阻选择 100Ω，并放置末端；

靠近 T 型分支中点



to ARM pins

- NANDF_RB2
- NANDF_RB0
- NANDF_RE
- NANDF_CE
- NANDF_CE2
- NANDF_CLE
- NANDF_ALE
- NANDF_WE
- NANDF_WP

- [41,48]
- [41,48]
- [41,48]
- [41,48]
- [41,48]
- [41,48]
- [41,48]
- [41,48]
- [41,48]

- NANDF_RB2
- NANDF_RB0
- NANDF_RE
- NANDF_CE
- NANDF_CE2
- NANDF_CLE
- NANDF_ALE
- NANDF_WE
- NANDF_WP

- [41,48]
- [41,48]
- [41,48]
- [41,48]

- NANDF_D7
- NANDF_D6
- NANDF_D5
- NANDF_D4
- NANDF_D3
- NANDF_D2
- NANDF_D1
- NANDF_D0

- [41,48]
- [41,48]
- [41,48]
- [41,48]
- [41,48]
- [41,48]
- [41,48]
- [41,48]

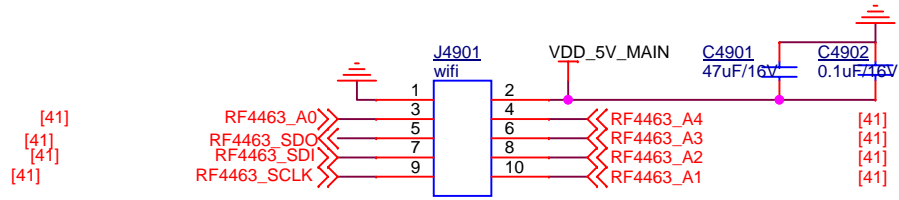
Title		<Title>		<RevCode>	
Size	Document Number	A4		Rev	
	<Draw Number>	48	59		
Date:	Sunday, September 02, 2018		Sheet 1 of 1		

D

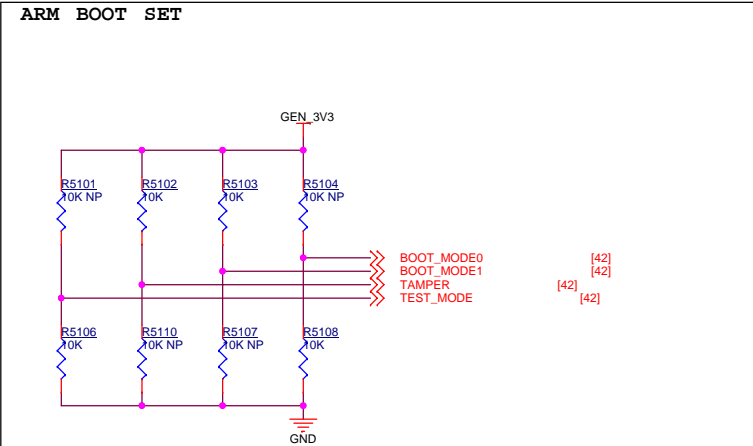
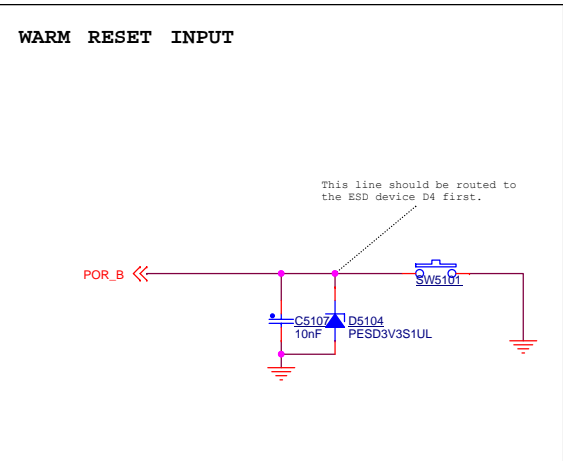
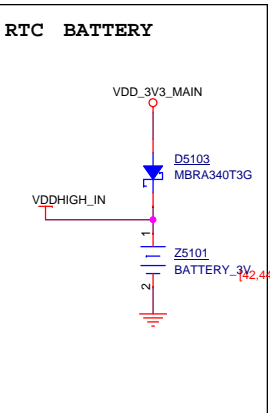
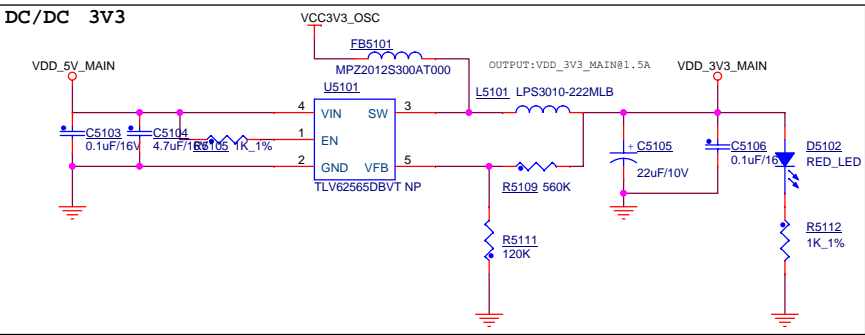
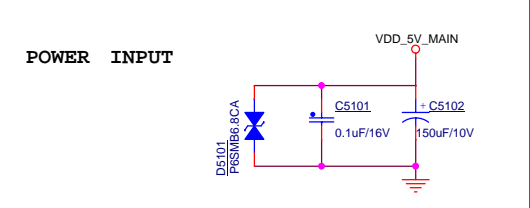
C

B

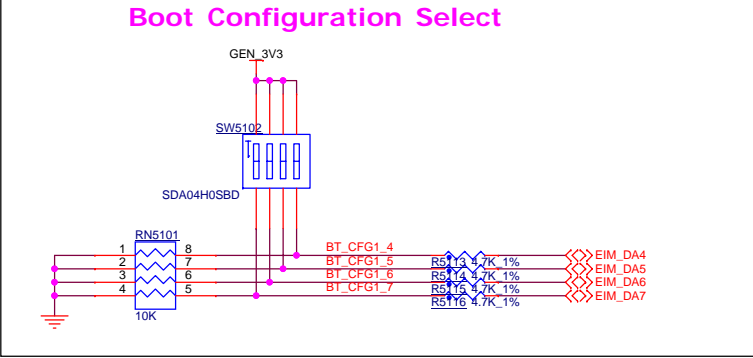
A



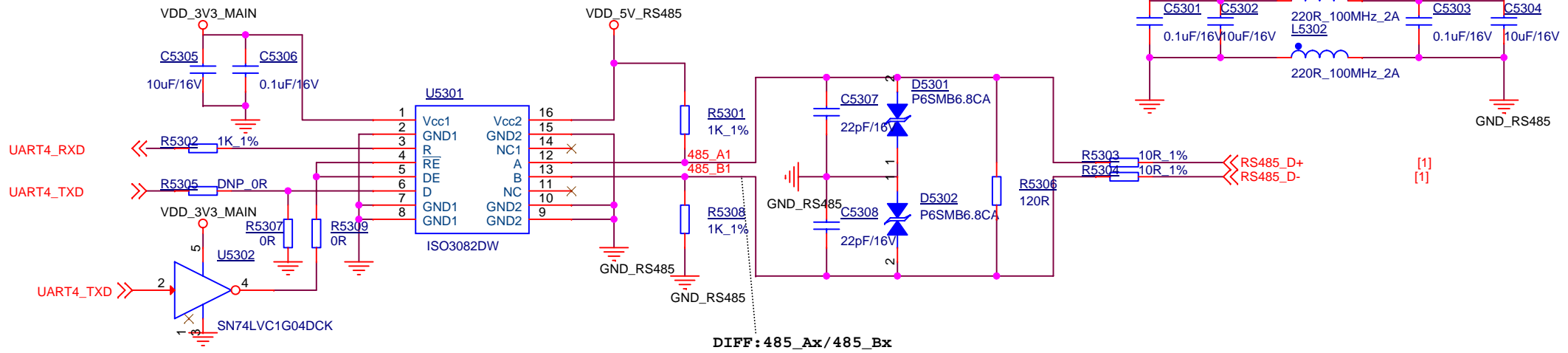
Title		
CDYL		
Size	Document Number	Rev
A4	10	v0.1
Date:	Sunday, September 02, 2018	Sheet 49 of 59



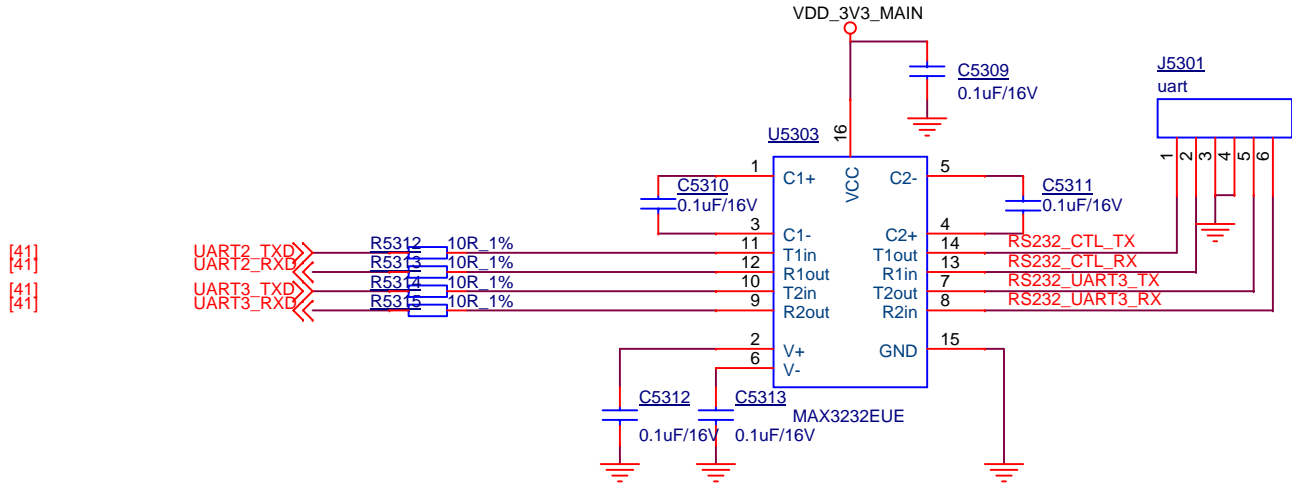
BOOT MODES:
 00 Boot from fuses
 01 Serial downloader
 10 Boot from board settings (DEFAULT)
 11 Reserved



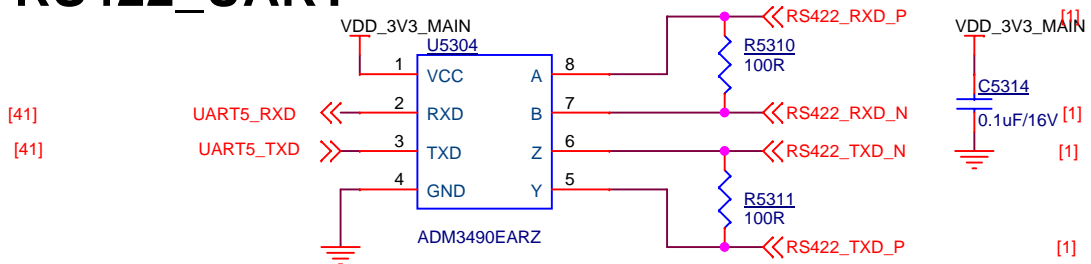
RS485



RS232

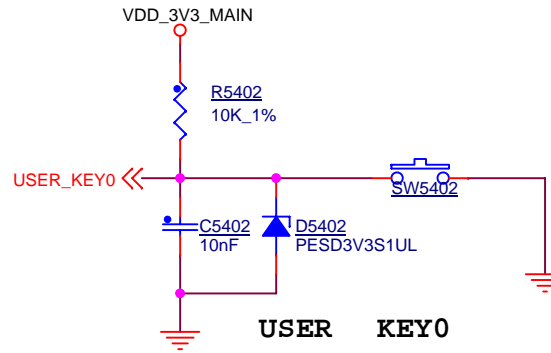
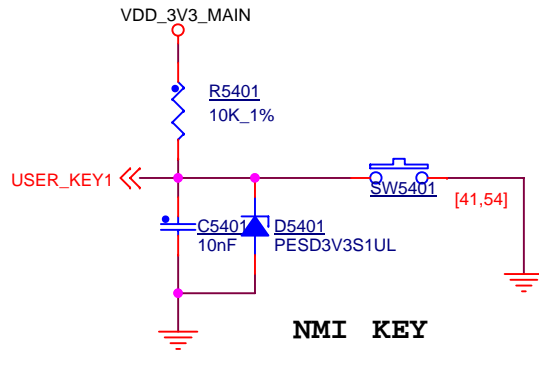


RS422_UART



Title		
<Title>		
Size	Document Number	Rev
A4	<Doc>	<RevCode>
Date:	Sunday, September 02, 2018	Sheet 53 of 59

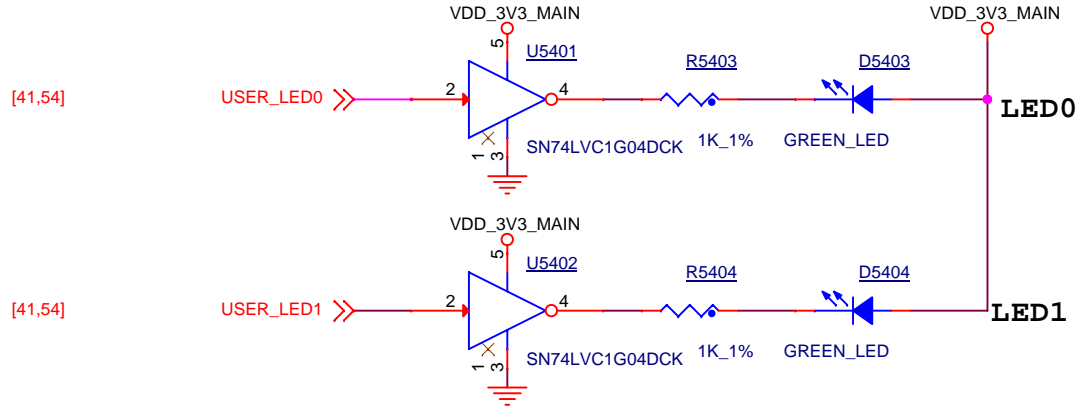
USER KEY



[41,54]
[41,54]

USER_KEY1 <<—
USER_KEY0 <<—

USER LED



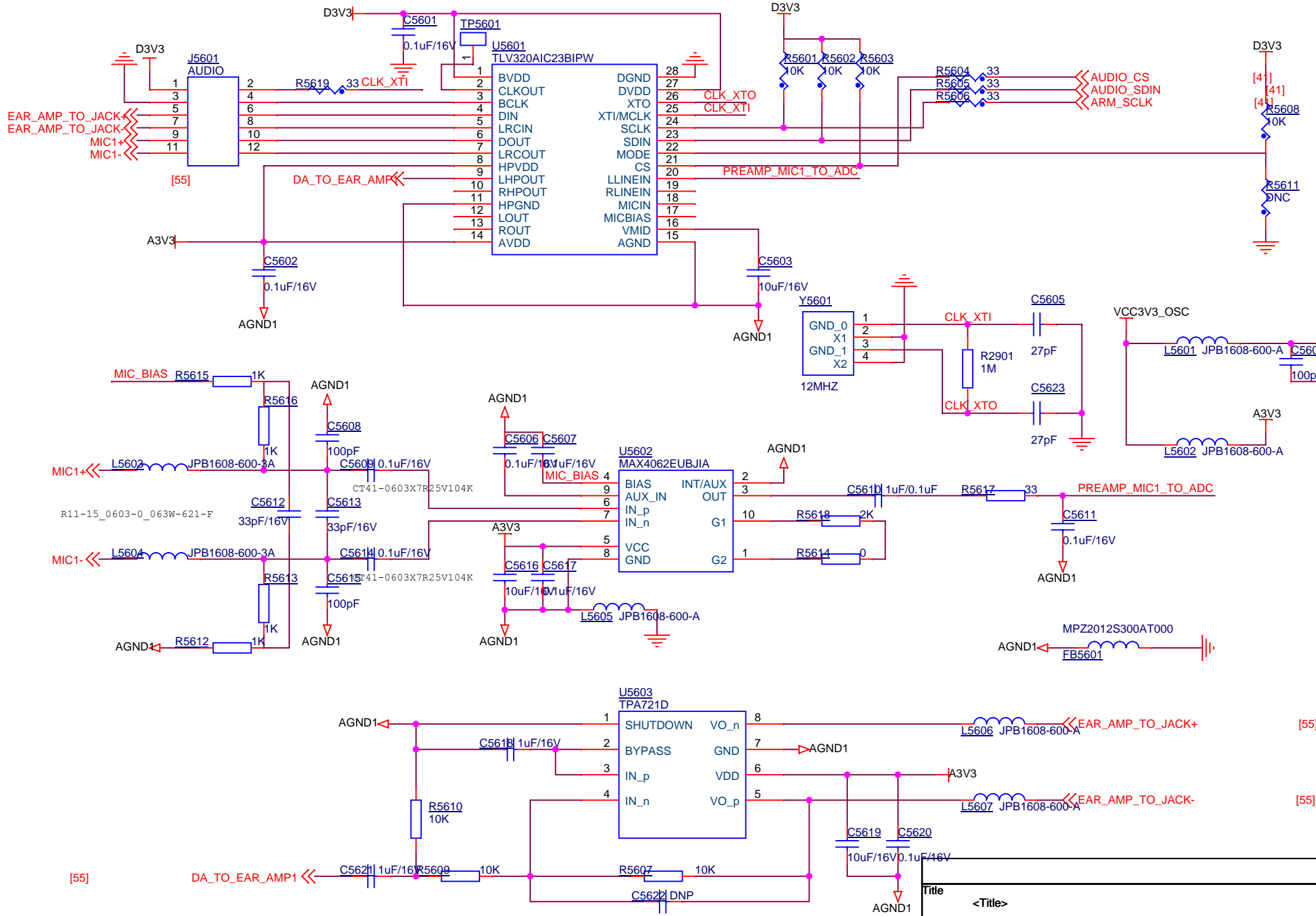
[41,54]

[41,54]

[41,54]
[41,54]

USER_LED0 >>—
USER_LED1 >>—

Title		
<Title>		
Size	Document Number	Rev
A4	<Doc>	<RevCode>
Date:	Sunday, September 02, 2018	Sheet 54 of 59



[55]
[55]

[55]

[55]

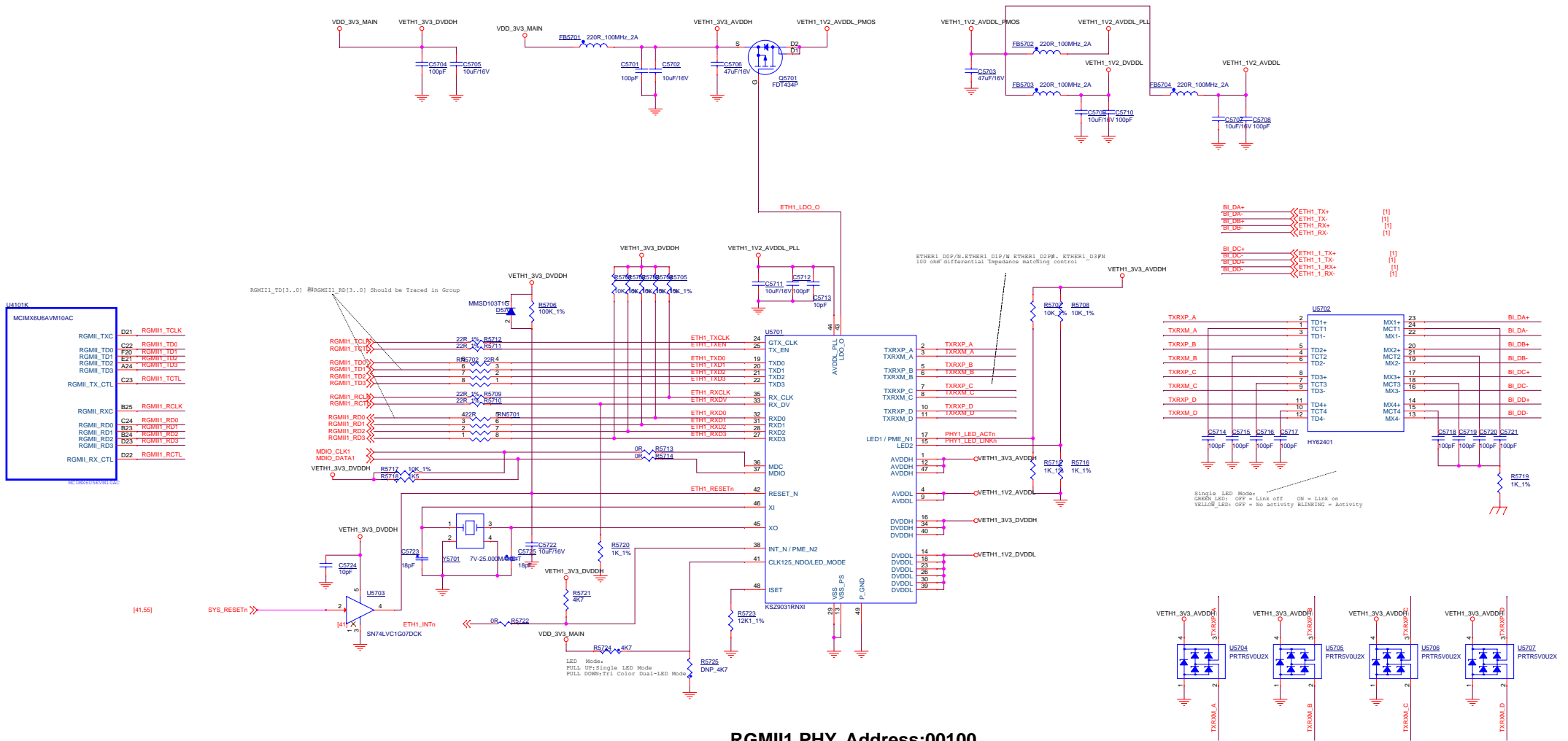
[55]

[55]

[55]

Title		
<Title>		
Size	Document Number	Rev
A4	<Doc>	<Rev>
Date:	Tuesday, September 04, 2018	Sheet 55 of 59

RGMI11

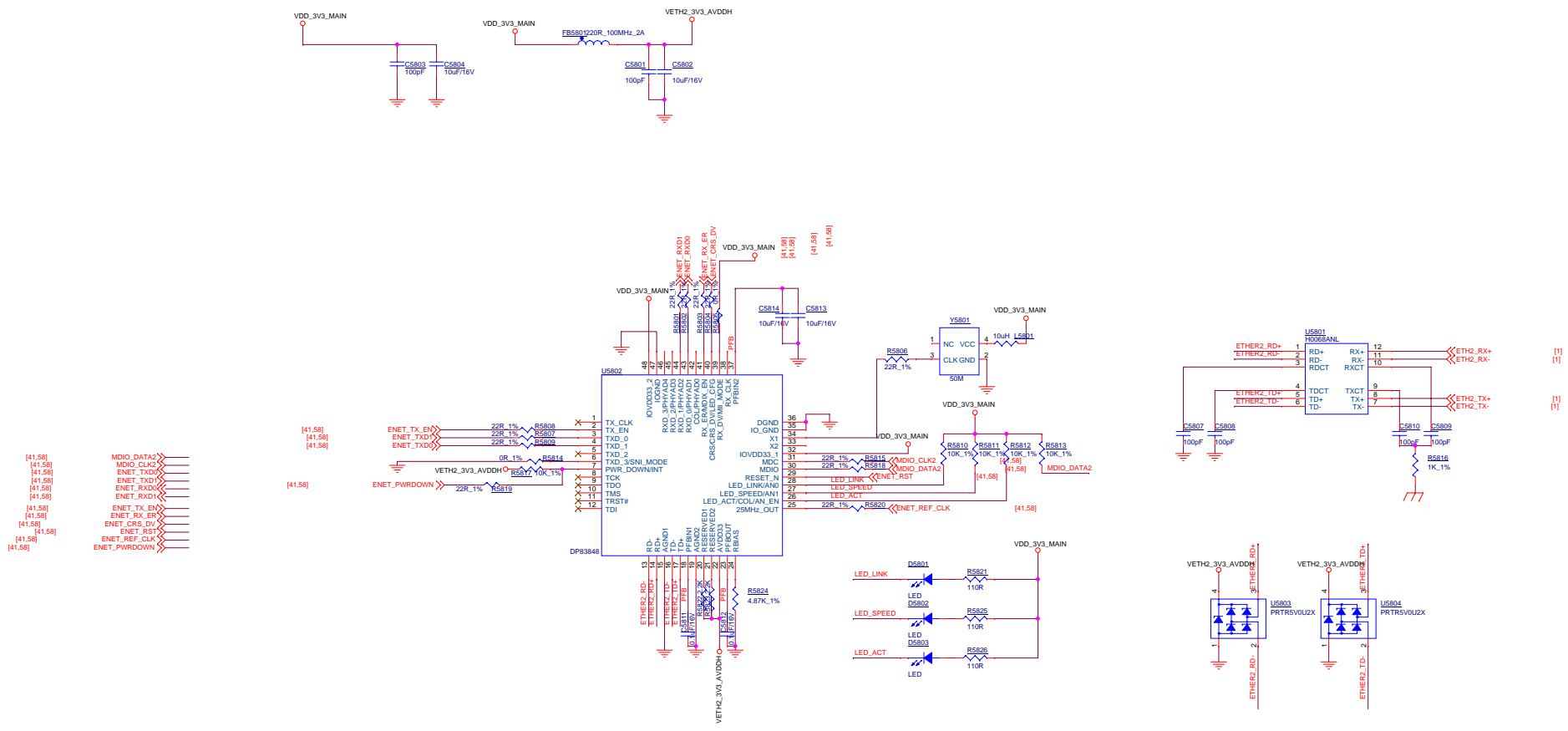


U4101K
MCIMX8UGAVM10AC

D21	RGMI1_TCLK
C22	RGMI1_TDO
F23	RGMI1_TDI
E21	RGMI1_TDZ
A24	RGMI1_TDS
C23	RGMI1_TCTL
B25	RGMI1_RCLK
C24	RGMI1_RDO
B23	RGMI1_RDH
B24	RGMI1_RODZ
D23	RGMI1_RDS
D22	RGMI1_RCTL

MCIMX8UGAVM10AC

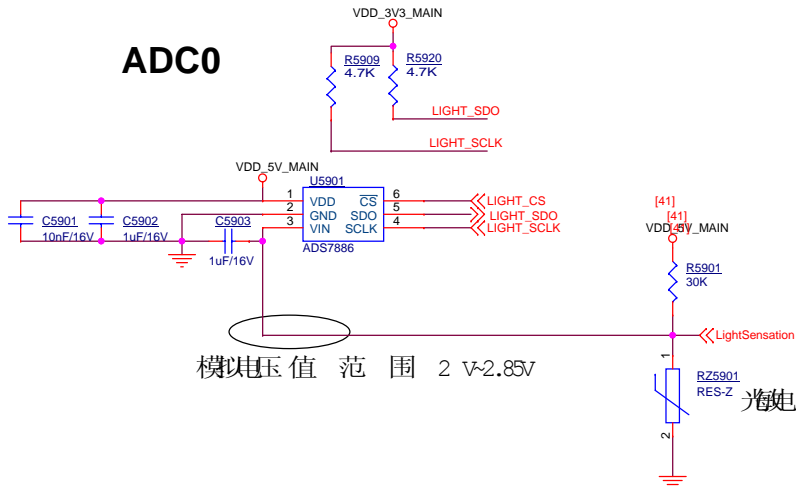
[41.55]



RGMII2 PHY Address:00101

File	<Title>	Rev
Size	Document Number	<Rev>
A2	<Doc>	
Date:	Sundsv, September 02, 2018	Sheet 58 of 59

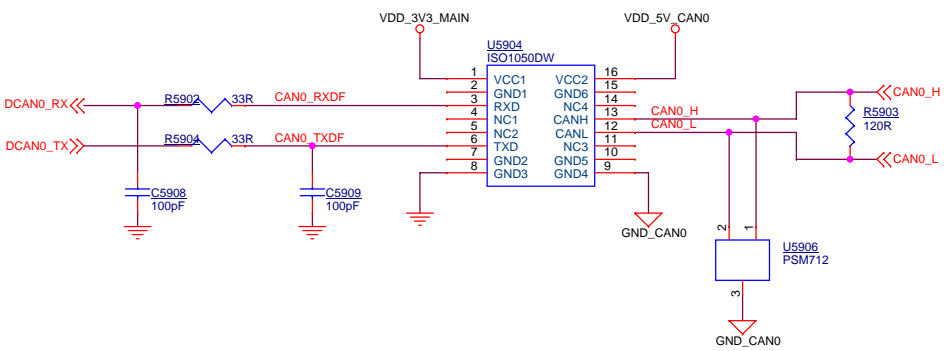
ADC0



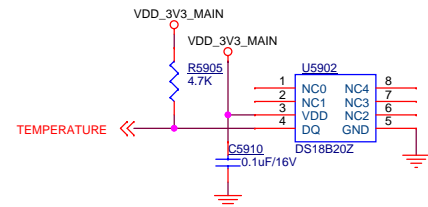
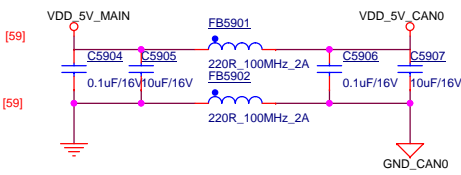
模块电压范围 2V~2.85V

光敏电阻 20k~40k

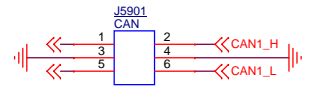
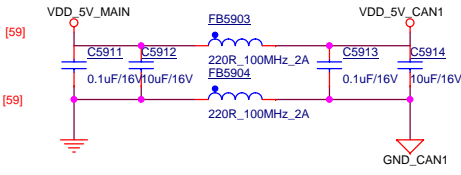
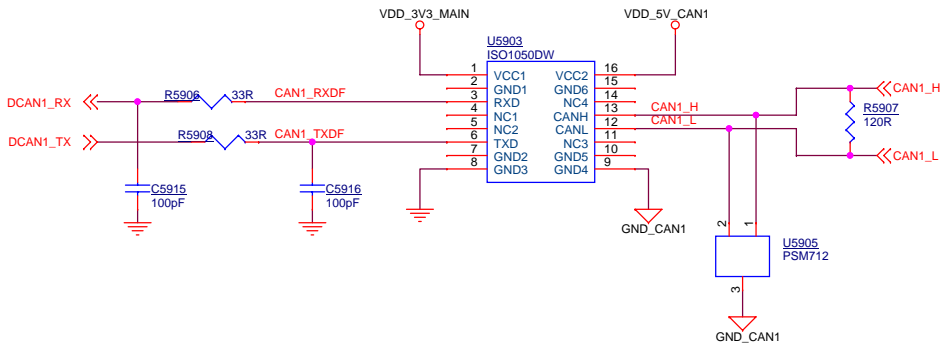
CAN0



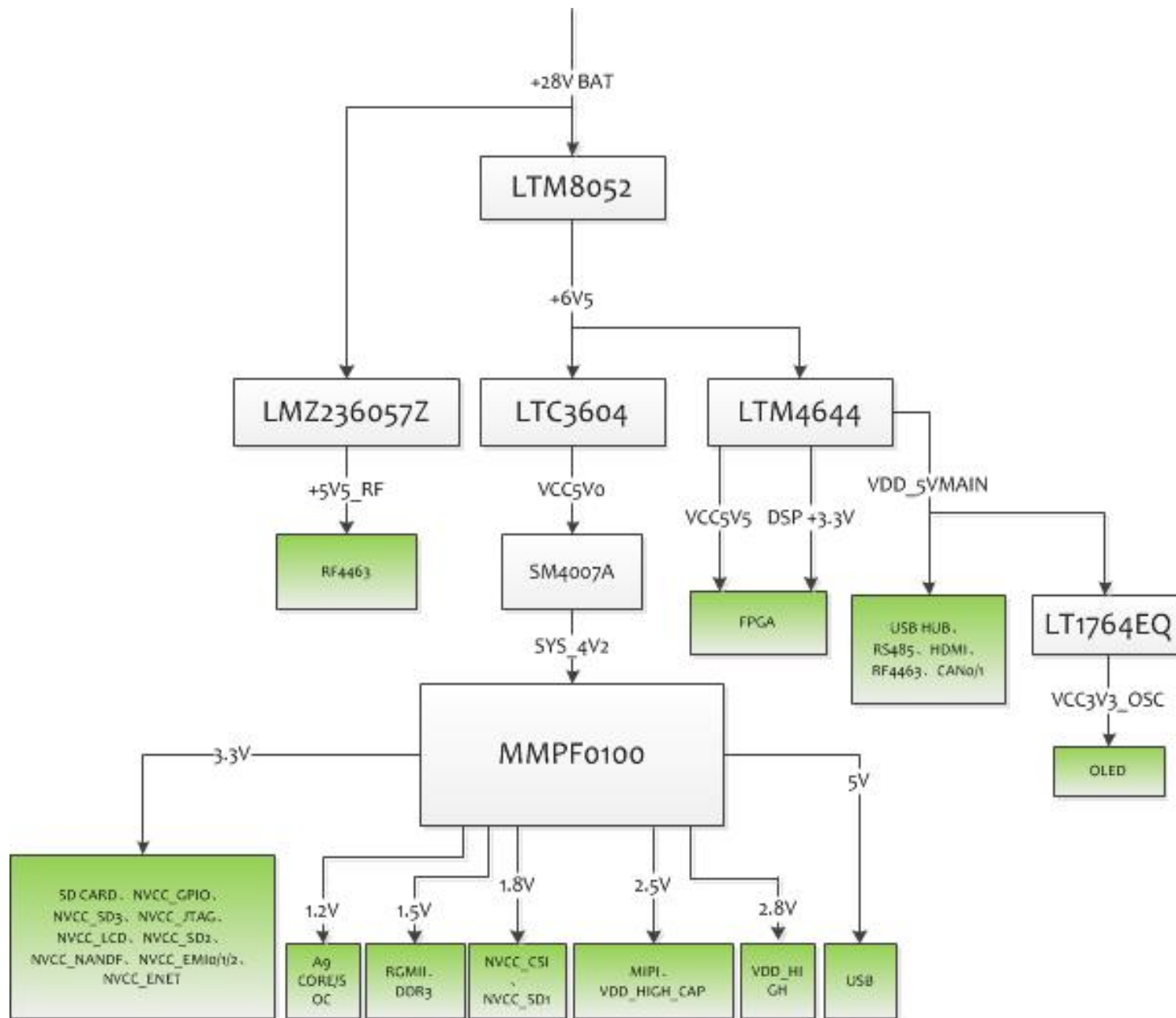
DS18B20Z



CAN1



Title	<Title>	
Size	Document Number	Rev
A3	<Doc>	<RevCode>
Date:	Sunday, September 02, 2018	Sheet 59 of 59



Title		
Size	Document Number	Rev
	60 59	
Date:	Sheet of	