MODEL NO : TM050JVZG33

MODEL VERSION: 00

SPEC VERSION : 1.0

ISSUED DATE: 2017-09-01

■**Preliminary Specification**
□**Final Product Specification**

Customer :_____

Approved by	Notes

TIANMA Confirmed :

Prepared by	Checked by	Approved by
haiping_luo	Lizhi_zhang Yu_huang	Guangkun_an

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Record of Revision

Rev	Issued Date	Description	Editor
V1.0	2017-09-01	Preliminary Specification Release	Haiping_luo

1.0 General Specifications

Feature		Spec
Display Spec.	Size	5 inch
	Resolution	720×RGB×1280
	Technology Type	a-Si SFT
	Pixel Configuration	Vertical Stripe
	Pixel pitch(mm)	0.08625×0.08625
	Display Mode	SFT
	Surface Treatment	HC
	Viewing Direction	ALL
Mechanical Characteristics	Outline Dimension (W x H x D) (mm)	LCM: 64.90×118.95×1.90
		CTP+LCM:73.59x137.98x3.05
	LCD A.A(W x H)(mm)	62.10×110.40
	Cover V.A(W x H)(mm)	62.70x111.00
	CTP Touch Method	Bare finger
	Number of simultaneous touches	5
	Minimum Touch Area(mm)	Φ7
	Finger Touch Pitch(mm)	≥13
	CTP Structure	GFF
	I^2C Addressing of CTP	0x14
	Matching Connection Type	ZIF
		ZIF
	LED Numbers	12 LEDS
	Weight (g)	TBD
Electrical Characteristics	Interface	MIPI 4 Lanes
	Color Depth	16.7M
	Driver IC	CTP: GT5668
		TFT: ILI9881C

Note 1: Requirements on Environmental Protection: Q/S0002

Note 2: LCM weight tolerance: ± 5%

2.0 Input/Output Terminals

2.1 LCM Pin Assignment

(Matching connector: ZIF)

Pin No.	Symbol	I/O	Function Description	Remark
1	LEDK	P	Backlight cathode.	
2	LEDA	P	Backlight anode.	
3	GND	P	Ground	
4	TE	O	Tearing effect output	
5	ID	I	LCD ID	
6	RESET	I	Reset pin	
7	GND	P	Ground	
8	VDDI1.8V	P	power supply 1.8V	
9	AVDD2.8V	P	power supply 2.8V	
10	D3P	I	MIPI DSI 3 lane(+)	
11	MESH	P	mesh	
12	D3N	I	MIPI DSI 3 lane(-)	
13	D2P	I	MIPI DSI 2 lane(+)	
14	D2N	I	MIPI DSI 2 lane(-)	
15	MESH	P	mesh	
16	GND	P	Ground	
17	CLKP	I	MIPI DSI CLK(+)	
18	CLKN	I	MIPI DSI CLK(-)	
19	GND	P	Ground	
20	D1P	I	MIPI DSI 1 lane(+)	
21	D1N	I	MIPI DSI 1 lane(-)	
22	GND	P	Ground	
23	D0P	I/o	MIPI DSI 0 lane(+)	
24	D0N	I/o	MIPI DSI 0 lane(-)	
25	GND	P	Ground	

2.2 CTP Pin Assignment

(Matching ZIF)

Pin No:	Symbol	I/O	Function Description	Remark
1	GND	P	Ground	
2	MESH	P	mesh	
3	GND	P	Ground	
4	VDD(3.3)	P	Voltage power	
5	VDD(3.3)	P	Voltage power	
6	SCL	I	I^2C SCL signal	
7	SDA	I/O	I2C data input and output	
8	INT	I/O	External interrupt to the host	
9	RST	I	Reset Pin	
10	GND	P	Ground	
11	MESH	P	mesh	
12	GND	P	Ground	

3.0 Absolute Maximum Ratings

3.0.1 LCM absolute maximum reatings

GND=0V

Item	Symbol	MIN	MAX	Unit	Remark
Power Supply Voltage	AVDD	-0.3	5.5	V	Note1
Logic Supply Voltage	VDDI	-0.3	4.5	V	
Logic Input voltage	I/O PINs	-0.3	VDDI+0.3	V	
Operating Temperature	Top	-20	70	℃	
Storage Temperature	Tst	-30	80	℃	
Relative Humidity Note2	RH	--	≤95	%	Ta≤40℃
		--	≤85	%	40℃＜Ta≤50℃
		--	≤55	%	50℃＜Ta≤60℃
		--	≤36	%	60℃＜Ta≤70℃
		--	≤24	%	70℃＜Ta≤80℃
Absolute Humidity	AH	--	≤70	g/m³	Ta＞70℃

Table 3 Absolute Maximum Ratings

Note1: Input voltage include R0~R5, G0~G5, B0~B5, Dotclk, Hsync, Vsync, Enable, R/L, U/D.

3.0.2 CTP absolute maximum reatings

参数	最小值	最大值	单位
模拟电源 AVDD28（参考 AGND）	-0.3	4.2	V
VDDIO（参考 DGND）	-0.3	4.2	V
数字 I/O 可承受电压	-0.3	4.2	V
模拟 I/O 可承受电压	-0.3	4.2	V
工作温度范围	-20	85	℃
存储温度范围	-60	125	℃
ESD 保护电压（HB Model）	±4		kV

4.0 Electrical Characteristics

4.0.1 LCD electrical characteristics

GND=0V,Ta=25℃

Item		Symbol	MIN	TYP	MAX	Unit	Remark
Analog operating voltage		AVDD	2.7	2.8	2.9	V	
Logic operating voltage		VDDI	1.7	1.8	1.9	V	
Input Signal Voltage	High Level	VIH	0.7* VDDI	-	VDDI	V	
	Low Level	VIL	-0.3	-	0.3* VDDI		
Output Voltage	High Level	V_{OH}	0.8VDDI	-	VDDI		
	Low Level	V_{OL}	0	-	0.2VDDI		

Table 4.1 LCD module electrical characteristics

4.0.2 CTP operating characteristics

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Support voltage	VDD	2.8	-	3.3	V	
VDD active current	VDD _ACT	-	20	-	mA	
VDDdeep sleep current	VDD _DS	39	-	135	uA	
Operate temperature;		-20	25	70	℃	

4.0.3 CTP function

（环境温度为 **25**℃）

序号	项目	标准
1	驱动 IC	GT5668
2	通讯协议	IIC
3	IIC 地址	0x14
4	原点坐标	左上
5	Sensor pitch	---
6	Finger	5 指
7	触控分辨率	720x1280
8	报点率	＞60HZ 多指，＞80HZ 单指
9	响应时间	≤25ms（Active state response time）
10	线性度（7mm 铜柱）	中心：±1.0mm；边缘：±1.5mm
11	两指间距	Ø=13mm

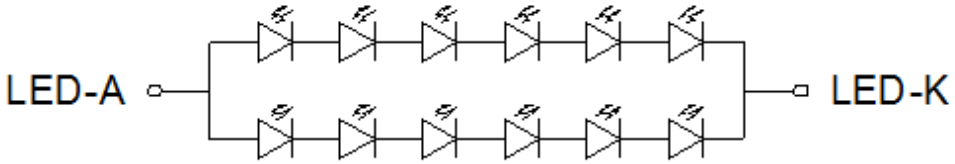
4.0.4 Backlight Unit

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward Current	IF	--	40	50	mA	12 LEDs (6 LED Serial, 2 LED Parallel)
Forward Current Voltage	VF	18	19.2	20.4	V	
Backlight Power Consumption	WBL	--	768	—	mW	
LED life time	--	10000	(20000)	-	Hrs	

Note1: Under LCM operating, the stable forward current should be inputted. And forward voltage is for reference only.

Note2: Optical performance should be evaluated at Ta=25℃ only if LED is driven by high current, high ambient temperature & Humidity condition. The life time of LED will be reduced. Operating life means brightness goes down to 50% initial brightness. Typical operating life time is estimated data.

Note3: Diagram of LED



CIRCUIT DIAGRAM

(If=40mA / Vf=19.2V TYP)

5.0 Timing Chart

5.0.1 Reset timing characteristics

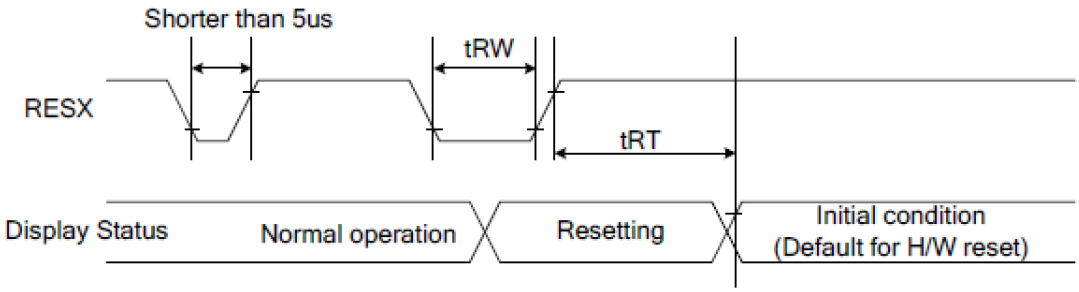


Figure 124: Reset Timing

Table 47: Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

Notes:

1. *The reset cancel also includes required time for loading ID bytes, VCOM setting and other settings from EEPROM to registers. This loading is done every time when there is H/W reset cancel time (tRT) within 5 ms after a rising edge of RESX.*
2. *Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Table 48.*

Table 48: Reset Descript

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

3. During the Resetting period, the display will be blanked (The display enters the blanking sequence, which maximum time is 120 ms, when Reset Starts in the Sleep Out mode. The display remains the blank state in the Sleep In mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection can also be applied during a valid reset pulse, as shown below:

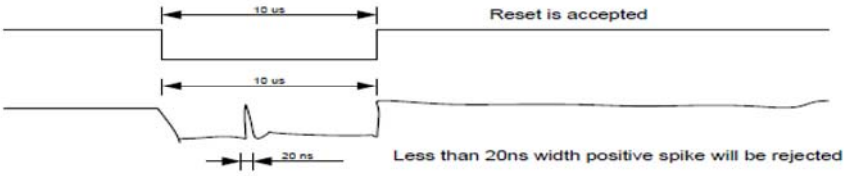


Figure 125: Positive Noise Pulse during Reset Low

5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

5.0.2 High Speed Mode

18.4.2. High Speed Mode – Clock Channel Timing

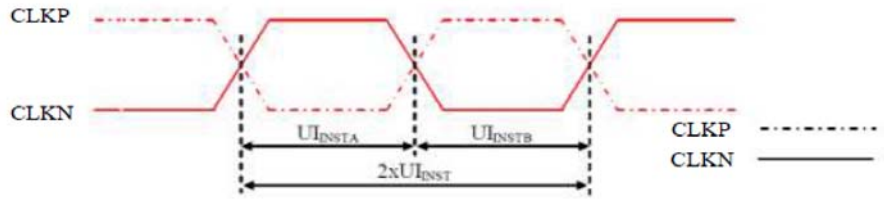


Figure 116: DSI Clock Channel Timing

Table 38: DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N	$2xUI_{INST}$	Double UI instantaneous	*Note 2*	25	ns
CLKP/N	UI_{INSTA}, UI_{INSTB} (Note 1)	UI instantaneous Half	*Note 2*	12.5	ns

Notes:

1. UI = UIINSTA = UIINSTB

2. Define the minimum value, see Table 39.

Table 39: Limited Clock Channel Speed

Data type	Two Lanes speed	Three Lanes speed	Four Lanes speed
Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel	566 Mbps	466 Mbps	366 Mbps
Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel	637 Mbps	525 Mbps	412 Mbps
Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel	850 Mbps	700 Mbps	550 Mbps
Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	850 Mbps	700 Mbps	550 Mbps

18.4.3. High Speed Mode – Data Clock Channel Timing

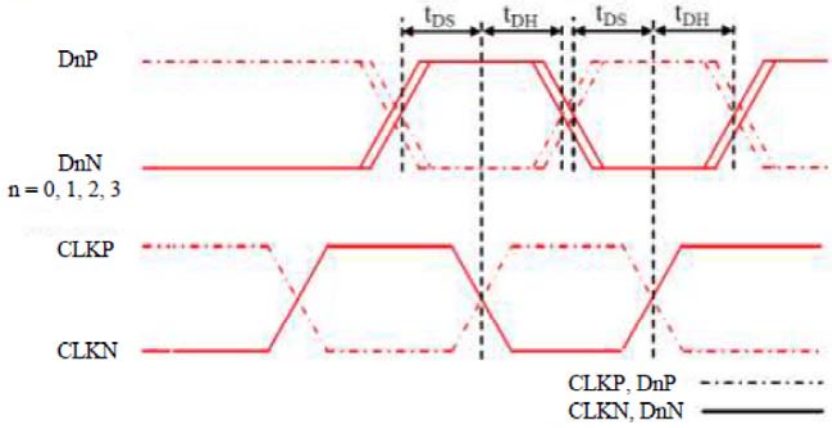


Figure 117: DSI Data to Clock Channel Timings

Table 40: DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DnP/N , n=0 and 1	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

18.4.4. High Speed Mode – Rising and Falling Timings

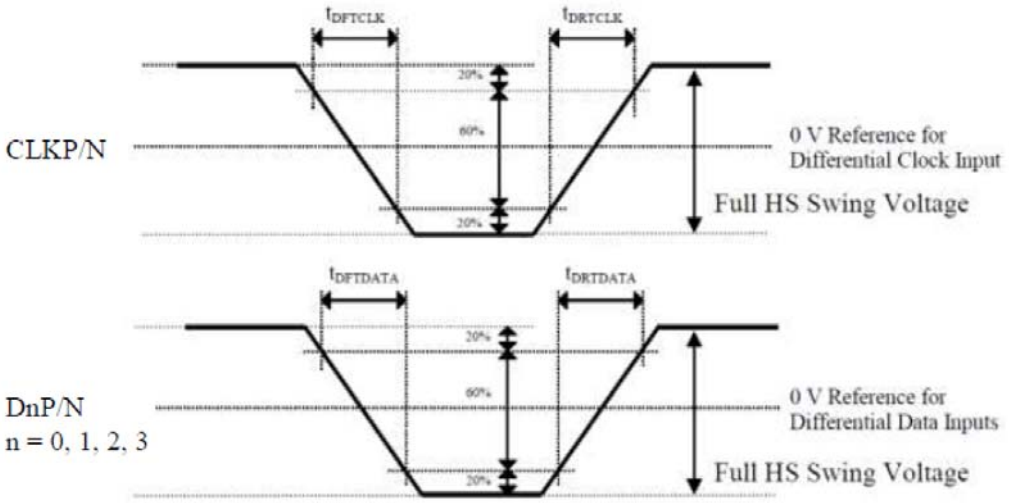


Figure 118: Rising and Falling Timings on Clock and Data Channels

Table 41: Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification		
			Min	Typ	Max
Differential Rise Time for Clock	t_{DRTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)
Differential Fall Time for Clock	t_{DFTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)

Note: *The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.*

5.0.3 Low Speed Mode

18.4.5. Low Speed Mode – Bus Turn Around

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the MCU to the Display Module (ILI9881C) are illustrated for reference purposes below.

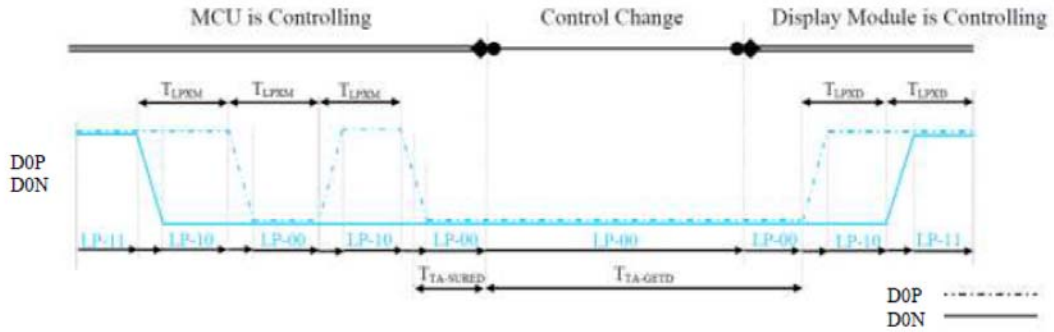


Figure 119: BTA from the MCU to the Display Module

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the Display Module (ILI9881C) to the MCU are illustrated for reference purposes below.

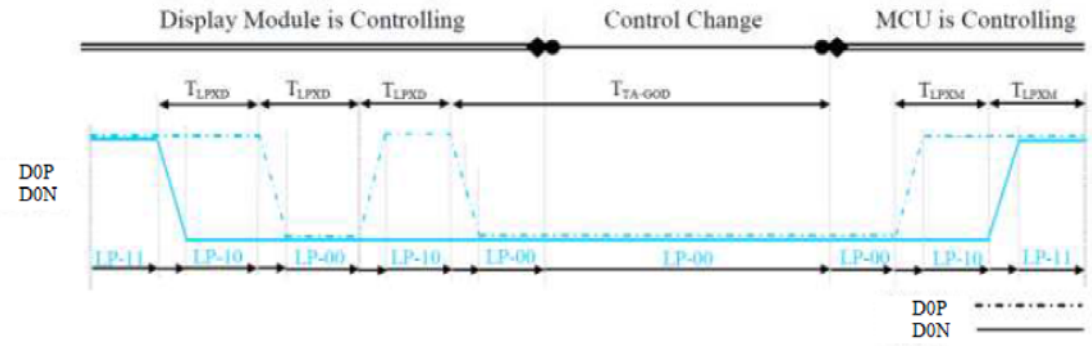


Figure 120: BTA from the Display Module to the MCU

Table 42: Low Power State Period Timings – A

Signal	Symbol	Description	Min	Max	Unit
D0P/N	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MCU → Display Module (ILI9881C)	50	75	ns
D0P/N	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (ILI9881C) → MCU	50	75	ns
D0P/N	$T_{TA-SURED}$	Time-out before the Display Module (ILI9881C) starts driving	T_{LPXD}	$2xT_{LPXD}$	ns

Table 43: Low Power State Period Timings – B

Signal	Symbol	Description	Time	Unit
D0P/N	$T_{TA-GETD}$	Time to drive LP-00 by Display Module (ILI9881C)	$5xT_{LPXD}$	ns
D0P/N	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MCU	$4xT_{LPXD}$	ns

18.4.6. Data Lanes from Low Power Mode to High Speed Mode

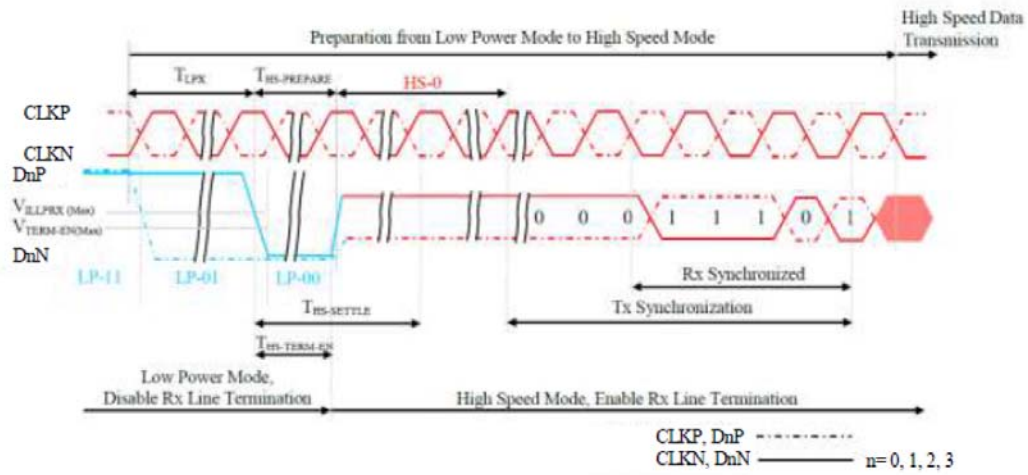


Figure 121: Data Lanes - Low Power Mode to High Speed Mode Timings

Table 44: Data Lanes - Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	T_{LPX}	Length of any Low Power State Period	50	-	ns
DnP/N, n = 0 and 1	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DnP/N, n = 0 and 1	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

18.4.7. Data Lanes from High Speed Mode to Low Power Mode

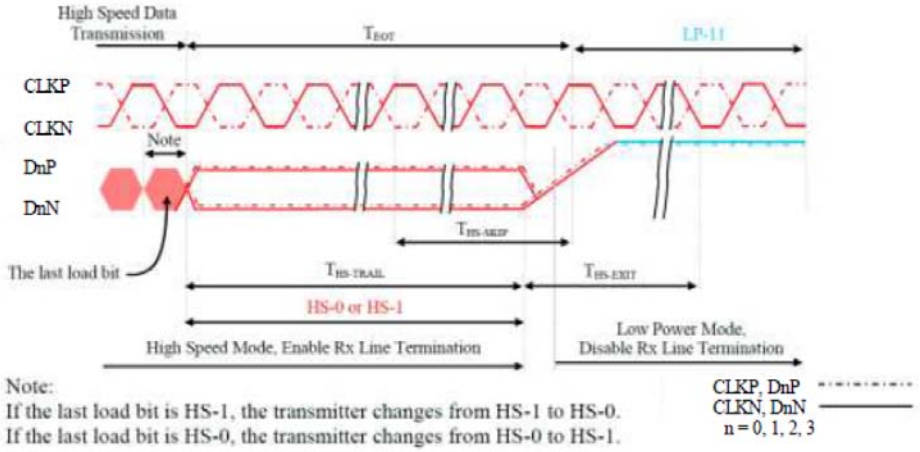
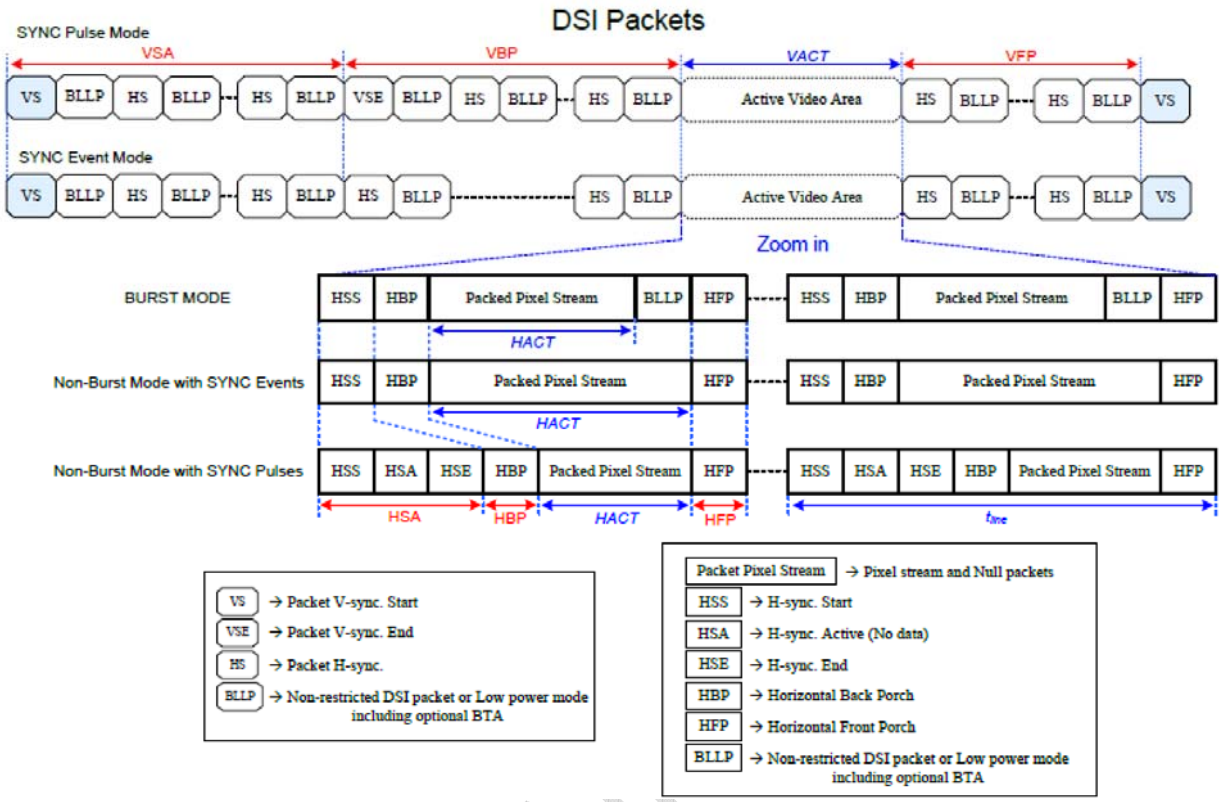


Figure 122: Data Lanes - High Speed Mode to Low Power Mode Timings

Table 45: Data Lanes - High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	$T_{HS-SKIP}$	Time-Out at Display Module (ILI9881C) to ignore transition period of EoT	40	55+4xUI	ns
DnP/N, n = 0 and 1	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns

18.4.9. Timing for DSI video mode



Parameters	Symbols	Min.	Typ.	Max.	Units
Vertical sync. active	VSA	2 (Note 6)	-	-	Line
Vertical Back Porch	VBP	14 (Note 6)	-	-	Line
Vertical Front Porch	VFP	8 (Note 6)	-	-	Line
Active lines per frame	VACT	-	1280	-	Line
Horizontal sync. active	HSA	2	-	-	Pixel
Horizontal Porch period	HSA + HBP + HFP	1.6	-	-	us
Active pixels per line	HACT	-	720	-	Pixel
Bit rate	BR_{bps}	385		Note 5	Mbps/lane

1 UI=1/Bit rate

HSA(pixel)= (tHSA*lane number) / (UI* pixel format)

HBP(pixel)= (tHBP*lane number) / (UI* pixel format)

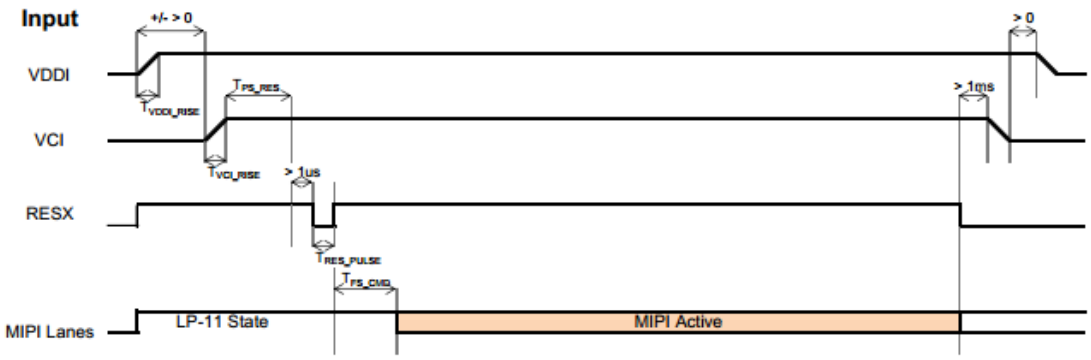
HFP(pixel)= (tHFP*lane number) / (UI* pixel format)

$$\text{Frame Rate} = \frac{BR_{bps} \times Lane_{num}}{(VACT+VSA+VBP+VFP) \times (HACT+HSA+HBP+HFP) \times \text{Pixel Format}}$$

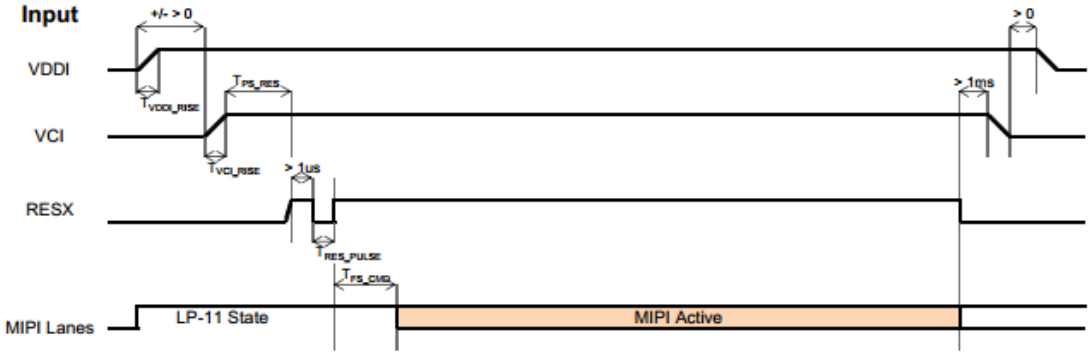
Example : BR_{bps} = 457Mbps/lane, 1UI=2.1883ns, Frame rate=60Hz, VACT=1280, VSA=2, VBP=30, VFP=20, HACT=720, HSA=33, HBP=100, HFP=100, $Lane_{num}$=4(lane), Pixel Format=24(bit).

5.0.4 POWER ON/OFF SEQUENCE

Case A:



Case B:



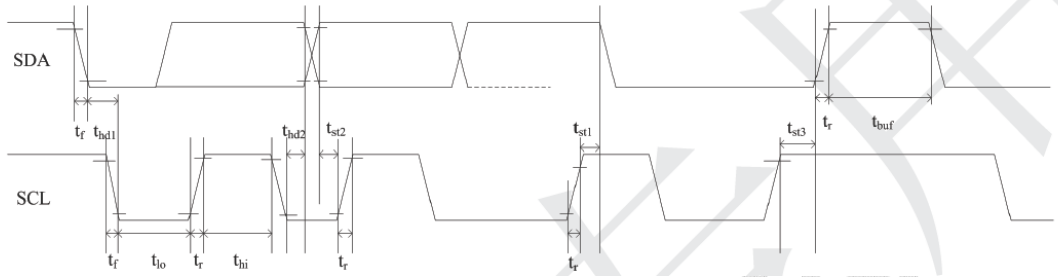
Symbol	Characteristics	Min.	Typ.	Max.	Units
T_{VDDI_RISE}	VDDI Rise time	10	-	-	us
T_{VCI_RISE}	Case A: VCI Rise time	130	-	-	us
	Case B: VCI Rise time	40			
T_{PS_RES}	VDDI/VCI on to Reset high	5	-	-	ms
T_{RES_PULSE}	Reset low pulse time	10	-	-	us
T_{FS_CMD}	Reset to first command	10	-	-	ms

Figure 105: Power on/off sequence with Power Mode 3

5.0.5 CTP Timing

5.0.5.1 IIC 时序

GT5668 提供标准的 I²C 通讯接口，由 SCL 和 SDA 与主 CPU 进行通讯。 在系统中 GT5668 始终作为从设备，所有通讯都是由主 CPU 发起，建议通讯速度为 400Kbps 或以下。其支持的 I²C 硬件电路支持时序如下：



测试条件 1：1.8V 通讯接口，400Kbps 通讯速度，上拉电阻 2K

Parameter	Symbol	Min.	Max.	Unit
SCL low period	t_{lo}	1.3	-	us
SCL high period	t_{hi}	0.6	-	us
SCL setup time for START condition	t_{st1}	0.6	-	us
SCL setup time for STOP condition	t_{st3}	0.6	-	us
SCL hold time for START condition	t_{hd1}	0.6	-	us
SDA setup time	t_{st2}	0.1	-	us
SDA hold time	t_{hd2}	0	-	us

6.0 Optical Characteristics

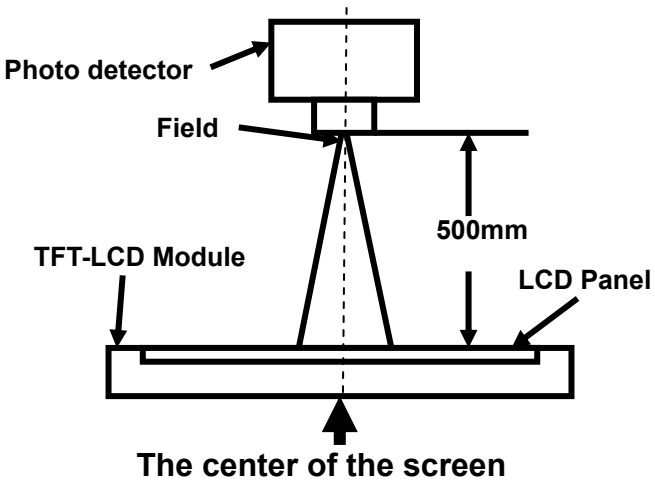
Item		Symbol	Condition	Min	Typ	Max	Unit	Remark
View Angles		θT	CR≧10	70	80	-	Degree	Note2
		θB		70	80	-		
		θL		70	80	-		
		θR		70	80	-		
Contrast Ratio		CR	θ=0°	600	800	-		Note 3
Response Time		T_{ON}	25℃	-	25	35	ms	Note 4
		T_{OFF}						
Chromaticity	White	x	Backlight is on	0.242	0.292	0.342		Note 1,5
		y		0.266	0.316	0.366		
	Red	x		-	-	-		Note 1,5
		y		-	-	-		
	Green	x		-	-	-		Note 1,5
		y		-	-	-		
	Blue	x		-	-	-		Note 1,5
		y		-	-	-		
Uniformity		U		80	85	-	%	Note 6
NTSC		-	-	65	70	-	%	Note 5
Luminance		L	-	260	350	-	cd/m^2	Note 7
Image Sticking		-	6x8 checker 25℃ 1hour burn-in 186 grey can disappear within 30min	-	-	-	-	Note 1,5

Test Conditions:

1. I_F= 20 mA(one LED), and the ambient temperature is 25℃.
2. The test systems refer to Note 1 and Note 2.

Note 1: Definition of optical measurement system.

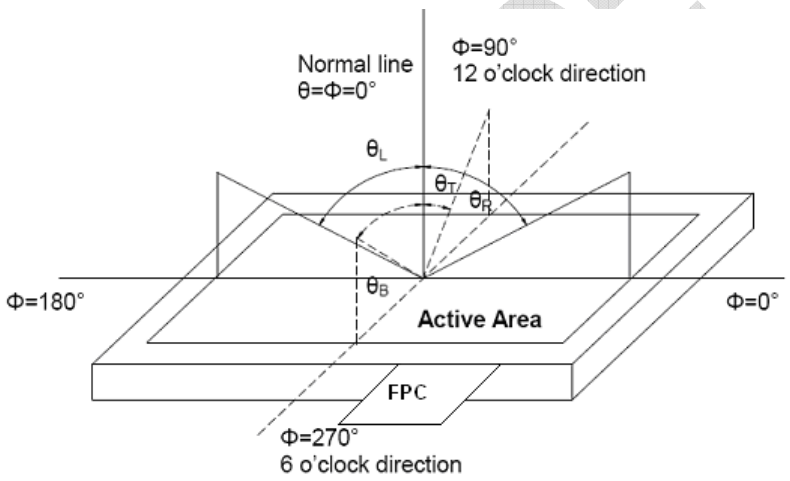
The optical characteristics should be measured in dark room. After 5 Minutes operation, the optical properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.



Item	Field
Contrast Ratio	1°
Luminance	
Chromaticity	
Lum Uniformity	
Response Time	2°

Note 2: Definition of viewing angle range and measurement system.

Viewing angle is measured at the center point of the LCD。



Note 3: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD is on the "White" state}}{\text{Luminance measured when LCD is on the "Black" state}}$$

"White state ": The state is that the LCD should drive by Vwhite.

"Black state": The state is that the LCD should drive by Vblack.

Vwhite: To be determined Vblack: To be determined.

Note 4: Definition of Response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (T_{ON}) is the time between photo detector output intensity changed from 90% to 10%. And fall time (T_{OFF}) is the time between photo detector output intensity changed from 10% to 90%.

Note 5: Definition of color chromaticity (CIE1931)

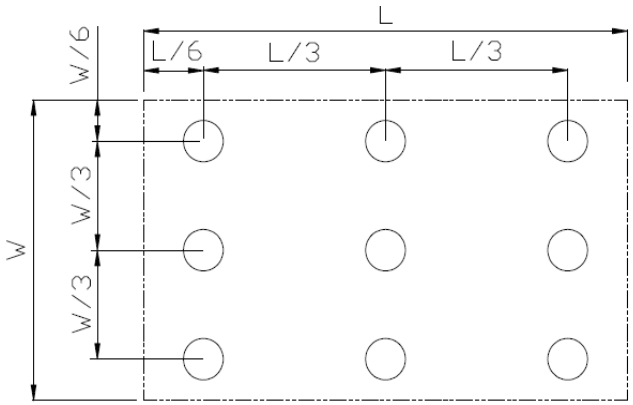
Color coordinates measured at center point of LCD.

Note 6: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity (U) = Lmin/ Lmax

L-------Active area length W----- Active area width



Lmax: The measured Maximum luminance of all measurement position.

Lmin: The measured Minimum luminance of all measurement position.

Note 7: Definition of Luminance:

Measure the luminance of white state at center point.

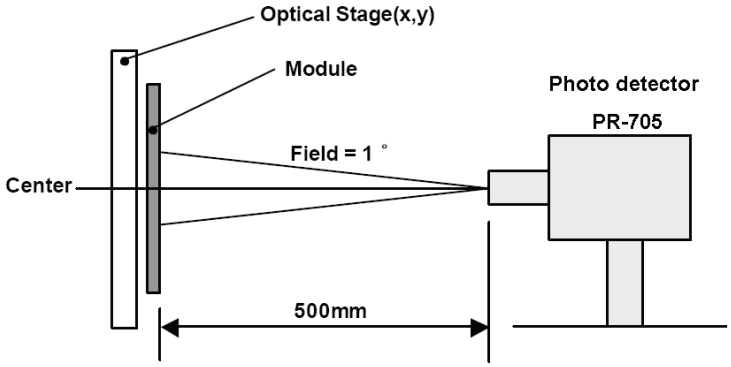
6.0.1 Optical Characteristics For CTP

No.	Item	Min.	Typ.	Max.	Unit	Remark
1	Transmission	86	88		%	Note 1，Note2
2	Reflectivity				%	AR 产品应用
3	HAZE	-	-	-	%	AG 产品应用

Note1:Measuring equipments: DMS-501, @550nm

Measuring condition:

- After stabilizing and leaving the panel alone at a given temperature for 30 min, the measurement should be executed,
- Measuring surroundings: a stable, windless and dark room,
- Measuring temperature: Ta=25°C,
- 30 min after lighting the back-light.



Note2: conform to National standard GB2410—80 /ASTM D1003—61(1997)

7.0 Environmental / Reliability Test

No	Test Item	Condition	Remarks
1	High Temperature Operation	Ts=+70℃， 96 hours	IEC60068-2-1:2007 GB2423.2-2008
2	Low Temperature Operation	Ta=-20℃， 96 hours	IEC60068-2-1:2007 GB2423.1-2008
3	High Temperature Storage	Ta=+80℃， 96 hours	IEC60068-2-1:2007 GB2423.2-2008
4	Low Temperature Storage	Ta=-30℃， 96 hours	IEC60068-2-1:2007 GB2423.1-2008
5	Storage at High Temperature and Humidity	Ta=+60℃， 90% RH 96 hours	IEC60068-2-78 :2001 GB/T2423.3—2006
6	Thermal Shock (non-operation)	-30℃ 30min ~+80℃ 30min， Change time：5min， 20 cycles	Start with cold temperature, End with high temperature, IEC60068-2-14:1984 GB2423.22-2002
7	ESD	C=150pF,R=330Ω, 5 point/panel, Air: ±8KV, 5 times; Contact ±4KV,5times (Environment:15℃~35℃,30%~60%,86Kpa~106Kpa)	IEC61000-4-2:2001 GB/T17626.2-2006

Note1: Ts is the temperature of panel's surface.

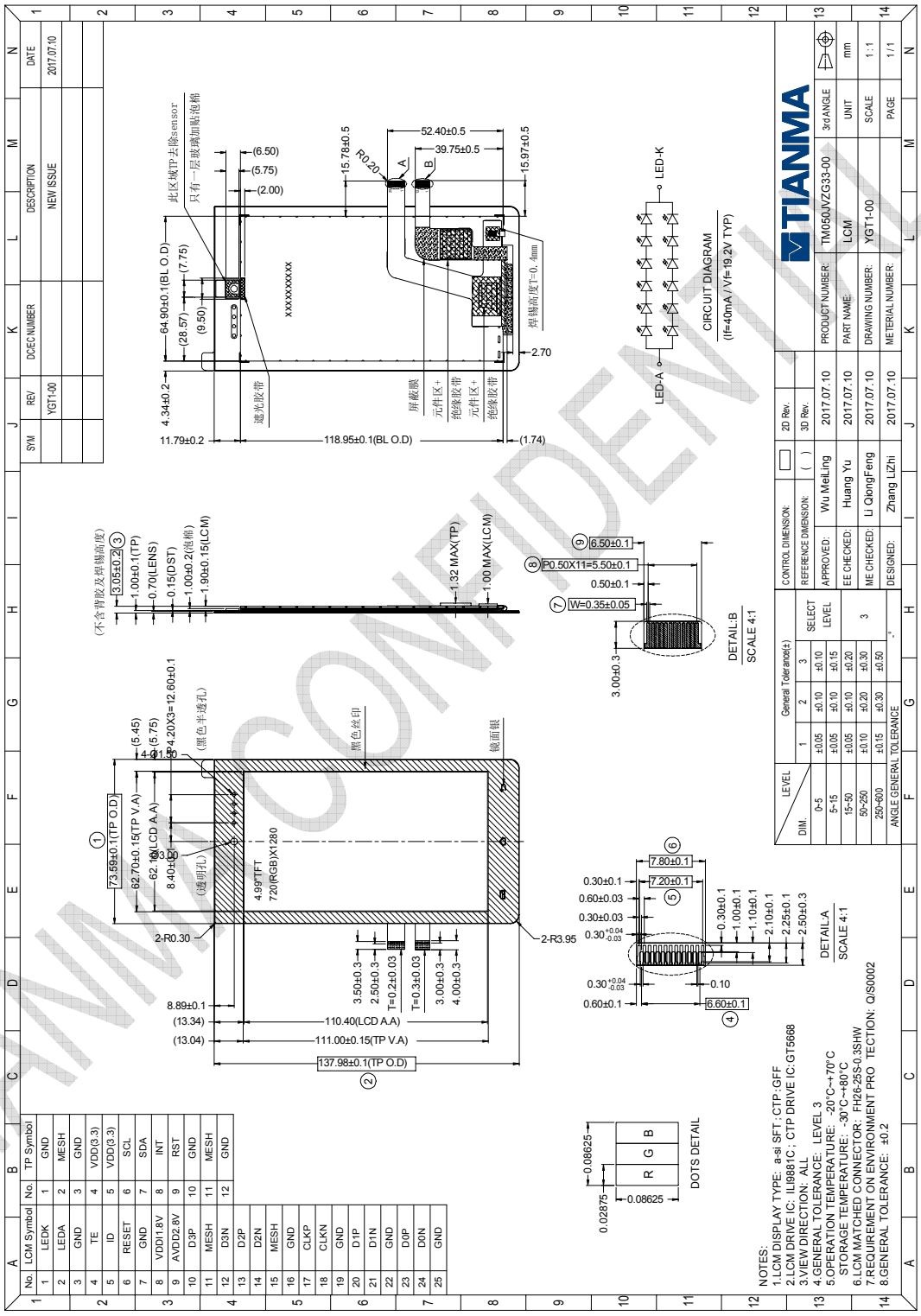
Note2: Ta is the ambient temperature of sample.

Note3: Before cosmetic and function test, the product must have enough recovery time, at least 2 hours at room temperature.

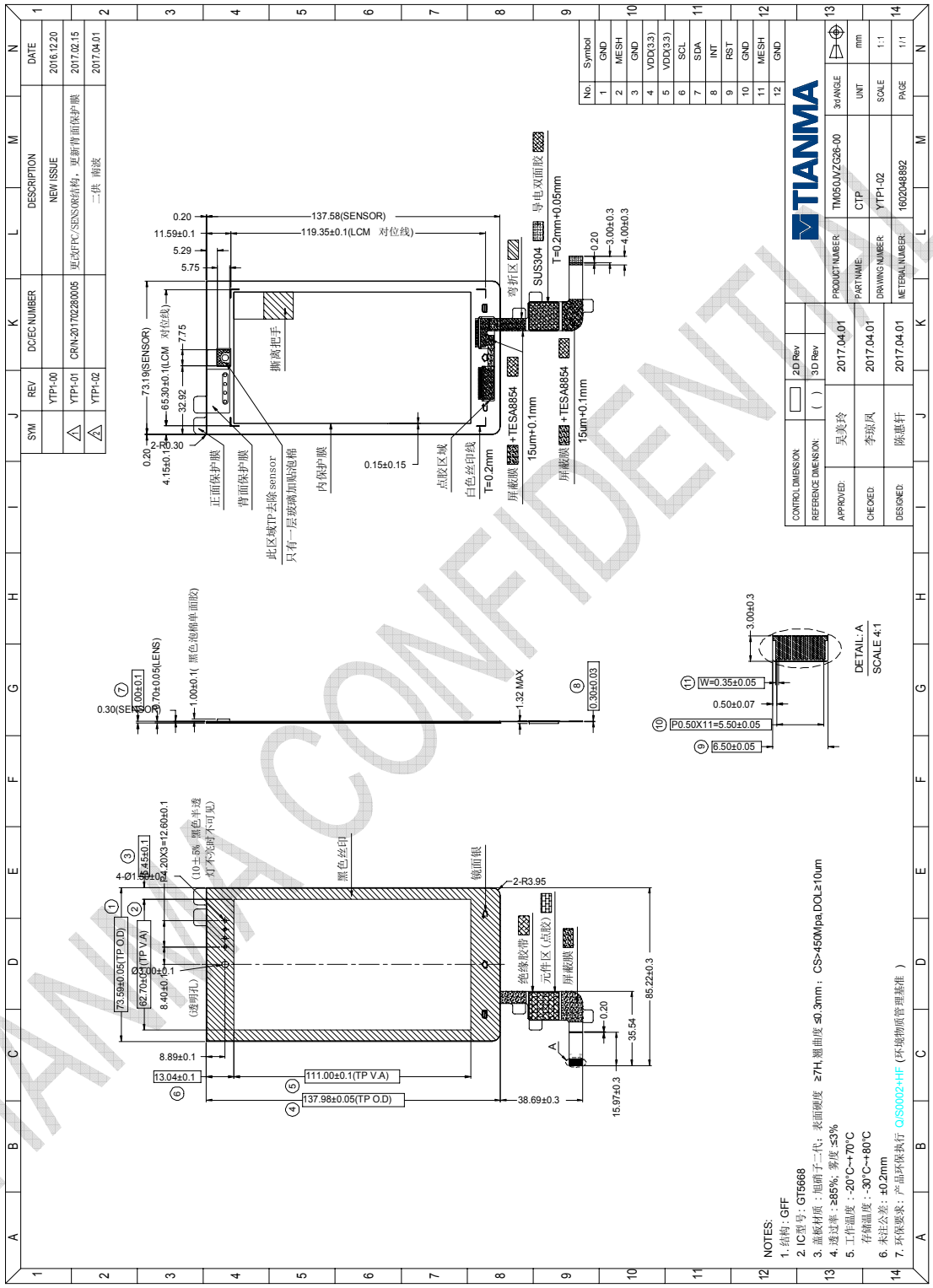
Note 4: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but don't guarantee all of the cosmetic specification.

8.0 Mechanical Drawing

8.0.1 LCM +CTP Mechanical Drawing



8.0.2 CTP Mechanical Drawing



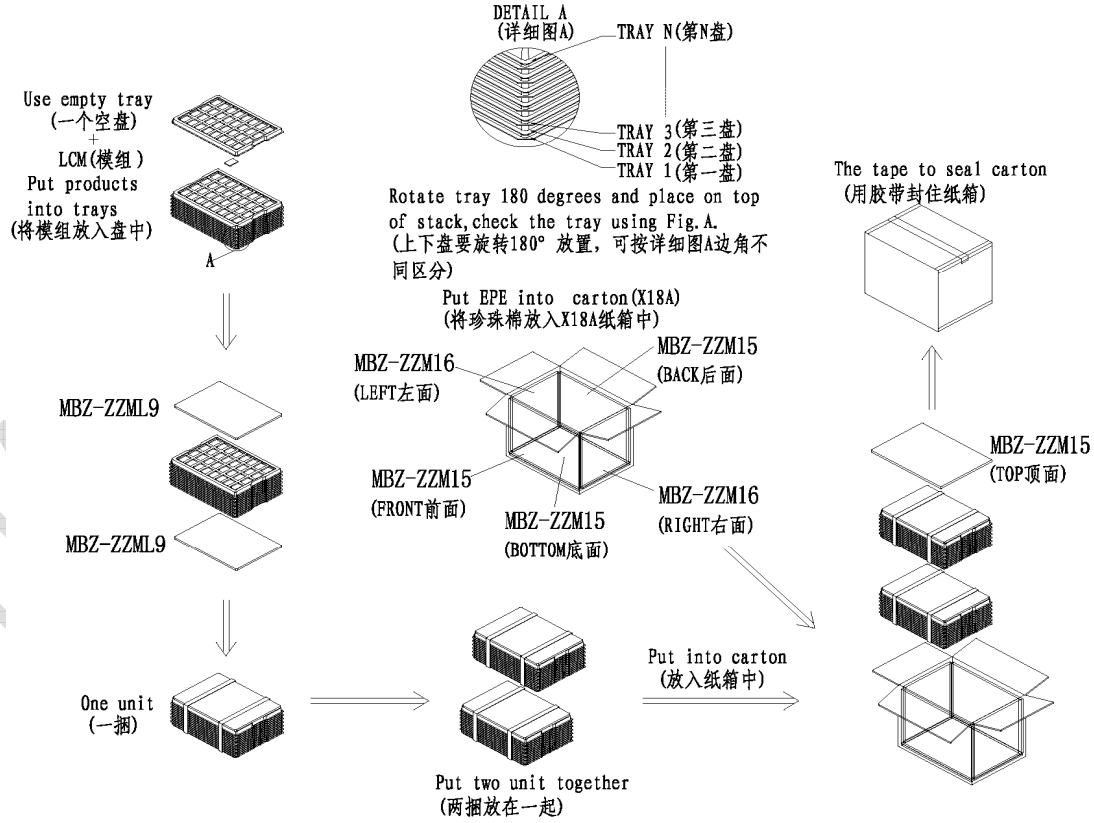
9.0 Packing Drawing

9.0.1 Packaging Material List

No	Item	Model (Materiel)	Dimensions(mm)	Unit Weight(Kg)	Quantity	Remark
1	LCM module	TM050JVZG33-00	73.59×137.98×3.05	TBD	84	
2	Tray	TM050JVZG33-00 YBZ1-00	356x256x15.0	TBD	24	
3	EPE（珍珠棉)	TM050JVZG33-00 YPF1-00	249.42×183.99×1.0	TBD	21	
4	EPE（珍珠棉1)	MBZ-ZZML1	336×246×6	TBD	6	
5	EPE（珍珠棉2）	MBZ-ZZM15	375×275×10	TBD	4	
6	EPE（珍珠棉3）	MBZ-ZZM16	250×280×12	TBD	2	
7	Carton（纸箱）	X18A	395×290×315	TBD	1	
8	Total weight	TBD				

9.0.2 Packaging Specification and Quantity

(1) LCM quantity per tray（每盘模组数量）: 4 pcs
(2) Total LCM quantity per group（每组模组总数量）: 28 pcs（7Tray 盘+1 Enpty tray 空盘）
(3) Total LCM quantity per Carton（每箱模组总数量）: quantity per group（每组模组总数量） 28 pcs×group quantity per Carton（每箱组数量）3= 84 pcs



10 .0 Precautions for Use of LCD Modules

10.0.1 Handling Precautions

The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

10.0.2 If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

10.03 Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

10.0.4 The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

10.0.5 If the display surface is contaMinated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketone
- Aromatic solvents

10.0.6 Do not attempt to disassemble the LCD Module.

10.0.7 If the logic circuit power is off, do not apply the input signals.

10.0.8 To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

10.0.9 Be sure to ground the body when handling the LCD Modules.

10.0.10 Tools required for assembly, such as soldering irons, must be properly ground.

10.0.11 To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

10.0.12 The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

10.0.13 Storage precautions

10.0.14 When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

10.0.15 The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:

Temperature : 0℃ ～ 40℃ Relatively humidity: ≤80%

10.0.16 The LCD modules should be stored in the room without acid, alkali and harmful gas.

10.0.17 Transportation Precautions

10.0.18 The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.