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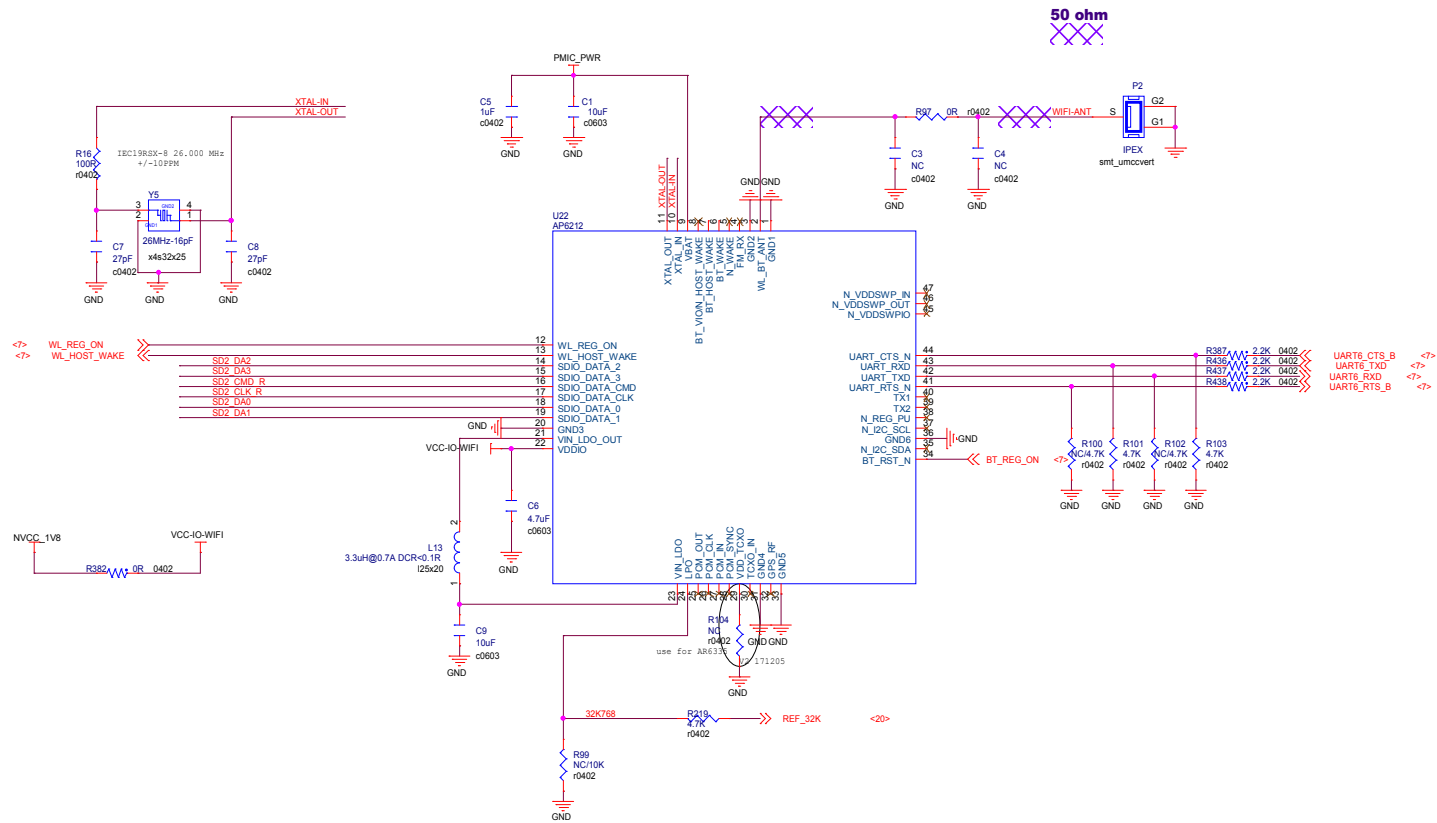
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# MCIMX7D-SABRE

## Revision History

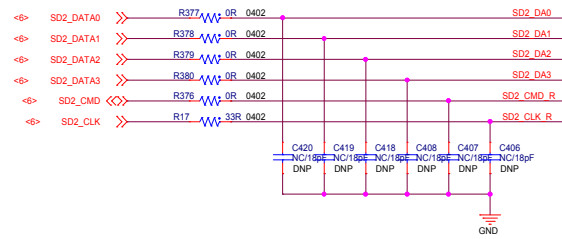
Rev. Code	Date	Description
B	22/09/2015	Initial Draft
B1	21/01/2016	<ul style="list-style-type: none"> <li>- Changed Q8 from 2N7002 to MMBT3904.</li> <li>- Reconnection U43 SW with the anode of D25.</li> <li>- DNP the capacitor:C6,C121.</li> <li>- Changed the power of JTAG from PERI_3V3 to VLDO3_3V3.</li> <li>- PCIE                             <ul style="list-style-type: none"> <li>DNP the resistor:R605,R606,R607,R608.</li> <li>Changed C442 and C443 to Ohm resistor (R632,R633).</li> <li>Add 49.9 1% 0402 resistors (R634,R635) on PCIE_REFCLKOUT_P/N to GND.</li> <li>Add the mosfet Q36 on the NET "CSI_PWDN".</li> <li>Add blocking capacitor(C458,C459) Before the terminal resistor.</li> <li>Add Schottky diode(D26) to isolate POR_B with JTAG interface.</li> <li>Use the LDO U44 instead of Q11.</li> <li>Add the Ohm resistor(R641) connect the pin CCM_CLK2 to GND.</li> <li>Add the U45 to match electrical level.</li> </ul> </li> </ul>
C	28/01/2016	<ul style="list-style-type: none"> <li>- Changed the revision from "B1" to "C".</li> <li>- Delete the capacitors C312 and C314.</li> <li>- Add several GND test points TP68--TP75 around the DDR3.</li> <li>- Changed connectors type of the J29&amp;J30</li> </ul>
D	09/03/2016	<ul style="list-style-type: none"> <li>- Changed the revision from "C" to "D".</li> <li>- Corrected the PCB decal of the Q8.</li> <li>- Changed connection of the J20.</li> </ul>

		<b>Multimedia Application Division, Wireless &amp; Mobile System Group</b>	
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Designer:		Doc Classification: ECP	
Design Date:		Rev. D	
Drawn by:		<b>MCIMX7D-SABRE</b>	
Page Title:		<b>01 Title Sheet</b>	
Approved: <Approver>		Document Number	Rev D
		SOURCE: SCH-28590-SPF-28590	
Date:		Wednesday, December 08, 2017	
		Sheet 1 of 23	

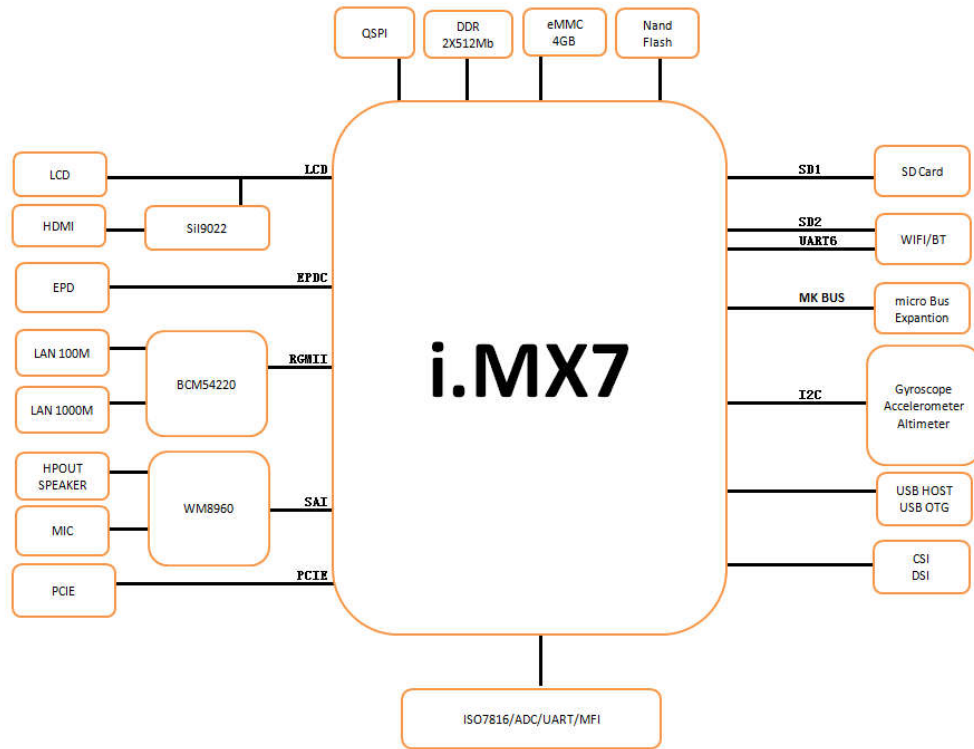


50 ohm

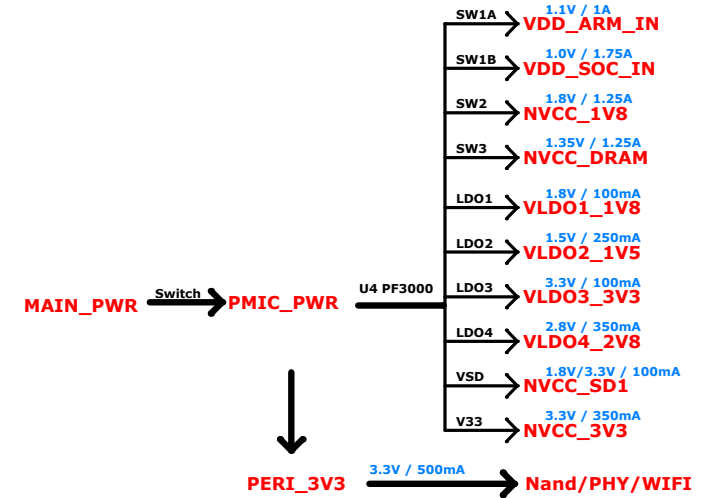
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	a	b/g/n	ac	5Ghz				
AP6181		Yes				26MHz	1.71-3.6V	3.3-4.8V
AP6212		Yes			Yes	26MHz	1.71-3.6V	3.3-4.8V
AP6330	Yes	Yes		Yes	Yes	26MHz	1.2-2.9V	3.3-4.8V
AP6335	Yes	Yes	Yes	Yes	Yes	37.4MHz	1.2-2.9V	3.3-4.8V



# MCIMX7D-SABRE Block Diagram



# Power Distribution Diagram



**freescale**

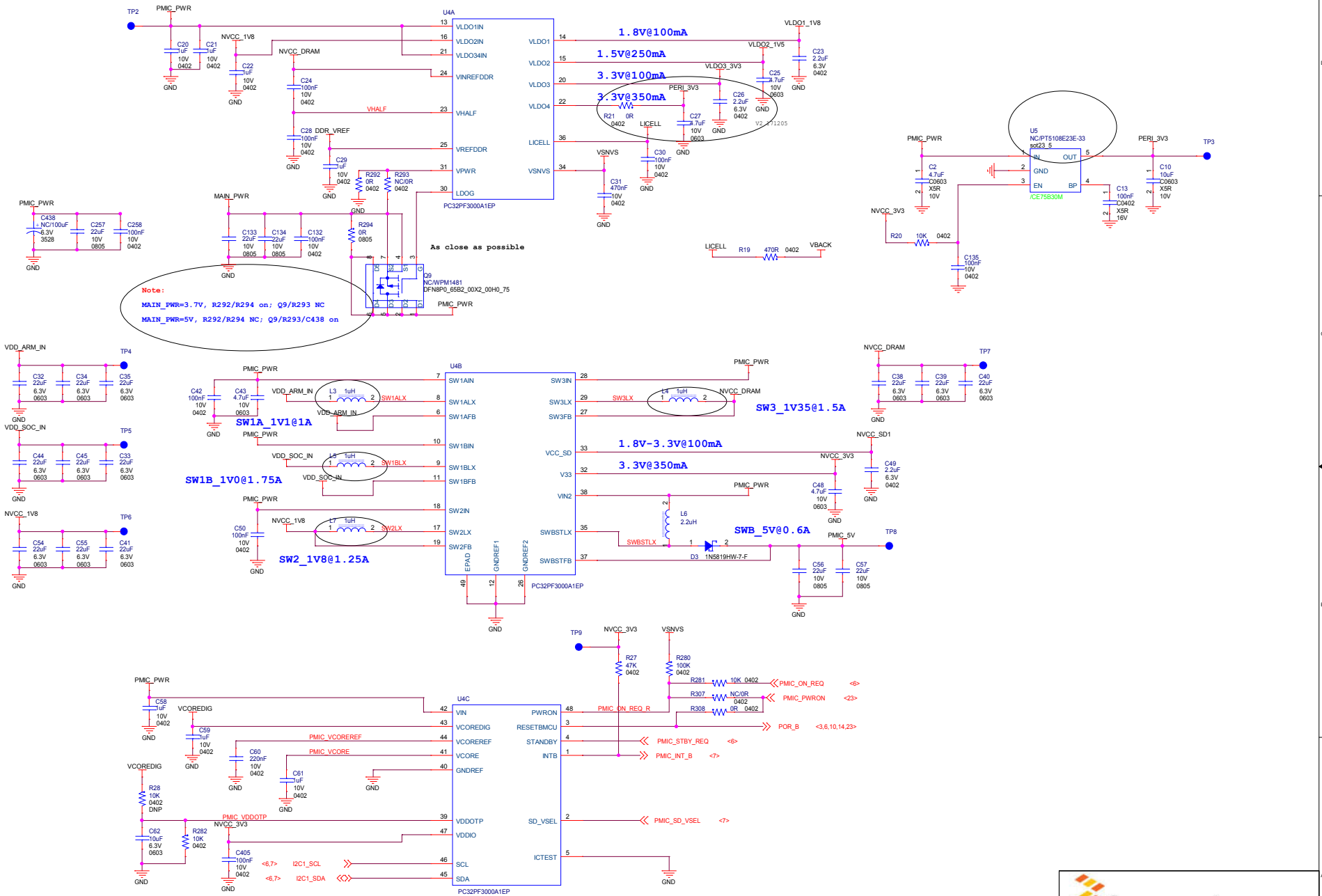
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Drawing Title: **MCIMX7D-SABRE**

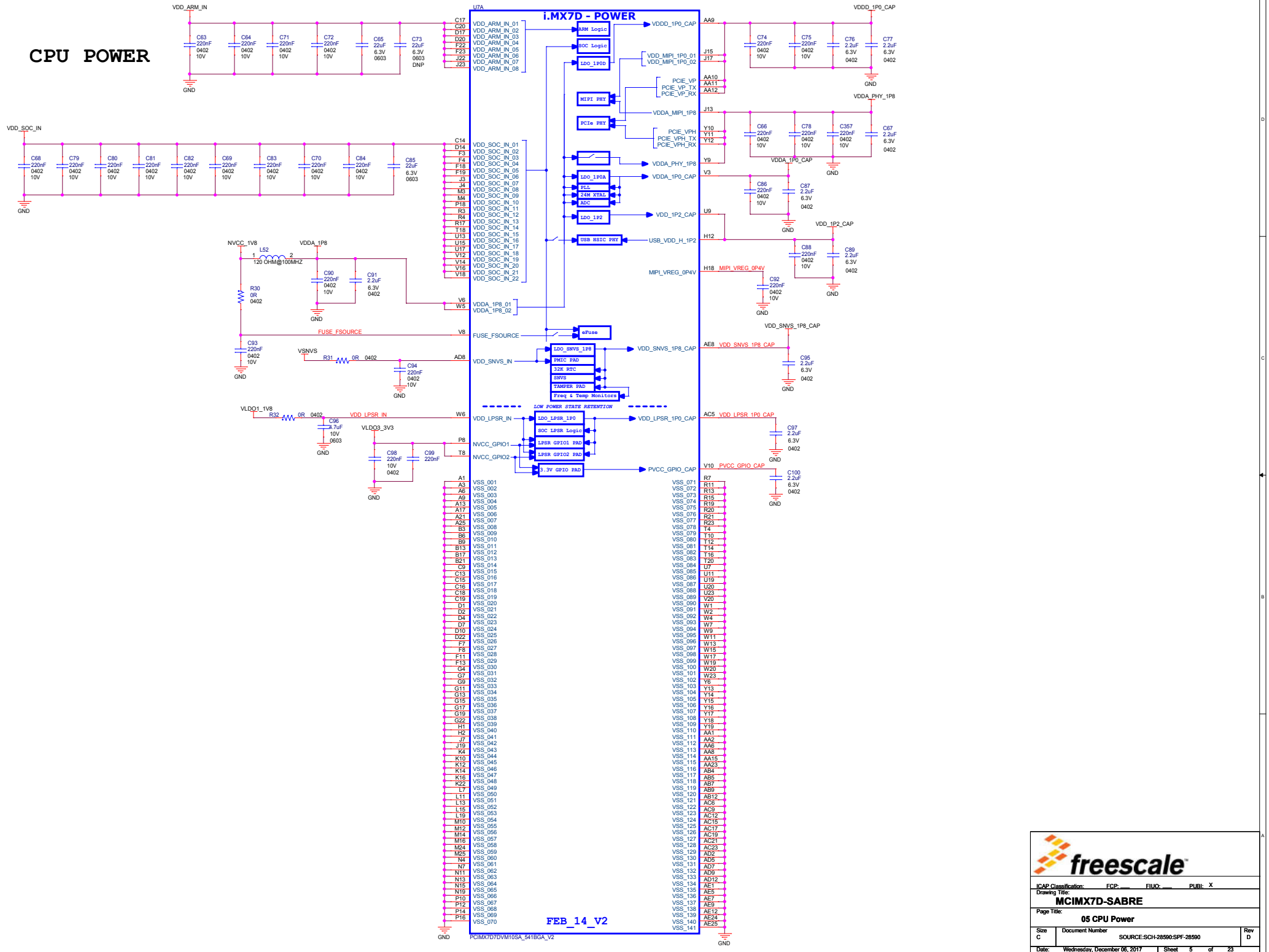
Page Title: **02 Block Diagram**

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# PMIC



# CPU POWER



**i.MX7D - POWER**

**U7A**

C17	VDD_ARM_IN_01
C20	VDD_ARM_IN_02
D17	VDD_ARM_IN_03
D20	VDD_ARM_IN_04
F22	VDD_ARM_IN_05
F23	VDD_ARM_IN_06
F22	VDD_ARM_IN_07
J23	VDD_ARM_IN_08
C14	VDD_SOC_IN_01
F3	VDD_SOC_IN_02
F4	VDD_SOC_IN_03
F18	VDD_SOC_IN_04
F19	VDD_SOC_IN_05
J24	VDD_SOC_IN_06
M3	VDD_SOC_IN_08
M4	VDD_SOC_IN_09
P18	VDD_SOC_IN_10
R3	VDD_SOC_IN_11
R4	VDD_SOC_IN_12
R17	VDD_SOC_IN_13
T18	VDD_SOC_IN_14
U15	VDD_SOC_IN_15
U16	VDD_SOC_IN_16
U17	VDD_SOC_IN_17
V12	VDD_SOC_IN_18
V14	VDD_SOC_IN_19
V16	VDD_SOC_IN_20
V18	VDD_SOC_IN_22
V6	VDDA_1P8_01
W5	VDDA_1P8_02
V8	FUSE_FSOURCE
A8	VDD_SNVS_IN
W6	VDD_LPSR_IN
P8	NVCC_GPIO1
T8	NVCC_GPIO2
A1	VSS_001
A3	VSS_002
A6	VSS_003
A9	VSS_004
A13	VSS_005
A17	VSS_006
A21	VSS_007
A25	VSS_008
B3	VSS_009
B6	VSS_010
B9	VSS_011
B15	VSS_012
B17	VSS_013
B21	VSS_014
C1	VSS_015
C13	VSS_016
C15	VSS_017
C18	VSS_018
C19	VSS_019
D1	VSS_020
D2	VSS_021
D4	VSS_022
D7	VSS_023
D10	VSS_024
D22	VSS_025
F7	VSS_026
F8	VSS_027
F11	VSS_028
F13	VSS_029
G4	VSS_030
G7	VSS_031
G9	VSS_032
G11	VSS_033
G13	VSS_034
G16	VSS_035
G17	VSS_036
G22	VSS_037
H1	VSS_038
H2	VSS_039
H4	VSS_040
J7	VSS_041
J19	VSS_042
K4	VSS_043
K10	VSS_044
K12	VSS_045
K14	VSS_046
K16	VSS_047
K22	VSS_048
L7	VSS_049
L11	VSS_050
L13	VSS_051
L16	VSS_052
L19	VSS_053
M10	VSS_054
M12	VSS_055
M14	VSS_056
M16	VSS_057
M24	VSS_058
M25	VSS_059
N1	VSS_060
N7	VSS_061
N11	VSS_062
N13	VSS_063
N16	VSS_064
N19	VSS_065
P10	VSS_066
P12	VSS_067
P14	VSS_068
P16	VSS_069
VSS_070	
VSS_071	
VSS_072	
R13	VSS_073
R15	VSS_074
R19	VSS_075
R20	VSS_076
R21	VSS_077
R23	VSS_078
T4	VSS_079
T10	VSS_080
T12	VSS_081
T14	VSS_082
T16	VSS_083
T20	VSS_084
U7	VSS_085
U11	VSS_086
U19	VSS_087
U20	VSS_088
U23	VSS_089
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W19	VSS_099
W20	VSS_100
W23	VSS_101
Y5	VSS_102
Y13	VSS_103
Y14	VSS_104
Y15	VSS_105
Y16	VSS_106
Y17	VSS_107
Y18	VSS_108
Y19	VSS_109
AA1	VSS_110
AA2	VSS_111
AA6	VSS_112
AA8	VSS_113
AA15	VSS_114
AA23	VSS_115
AA4	VSS_116
AA5	VSS_117
AA7	VSS_118
AA9	VSS_119
AB12	VSS_120
AC6	VSS_121
AC9	VSS_122
AC12	VSS_123
AC15	VSS_124
AC17	VSS_125
AC19	VSS_126
AC21	VSS_127
AC23	VSS_128
AD2	VSS_129
AD5	VSS_130
AD7	VSS_131
AD9	VSS_132
AE1	VSS_133
AE12	VSS_134
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AE12	VSS_138
AE24	VSS_139
AE25	VSS_140
VSS_141	

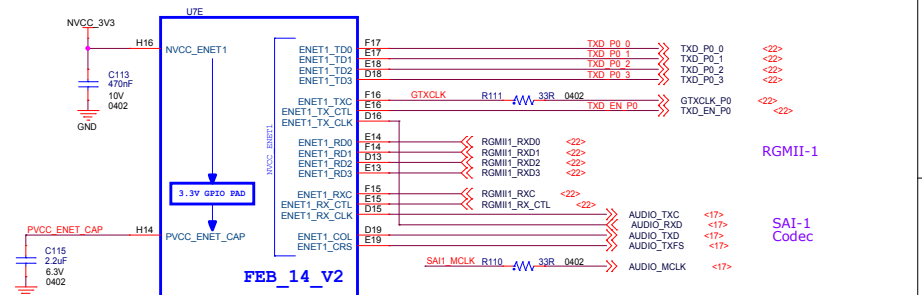
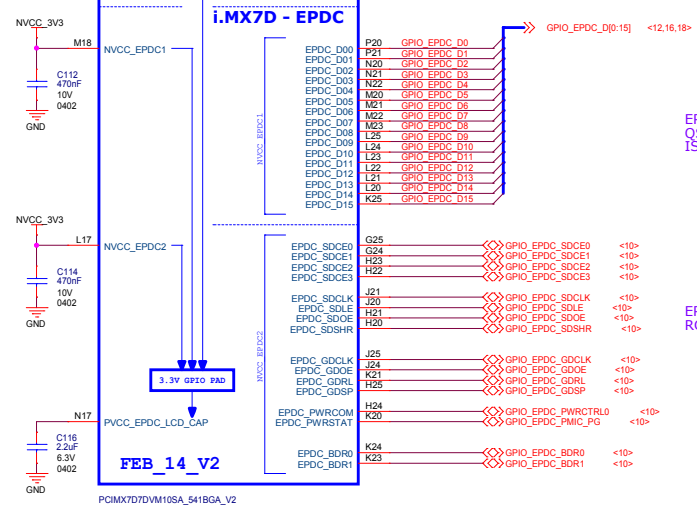
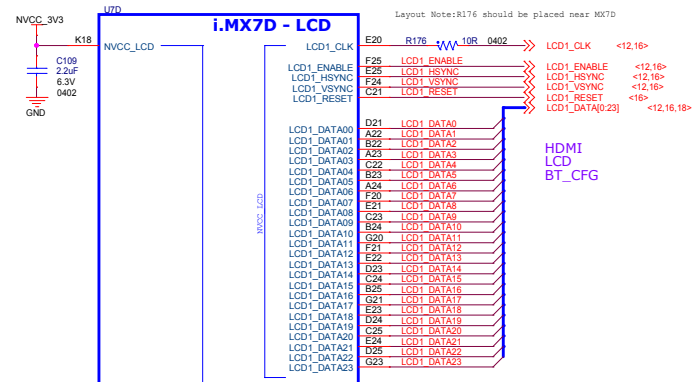
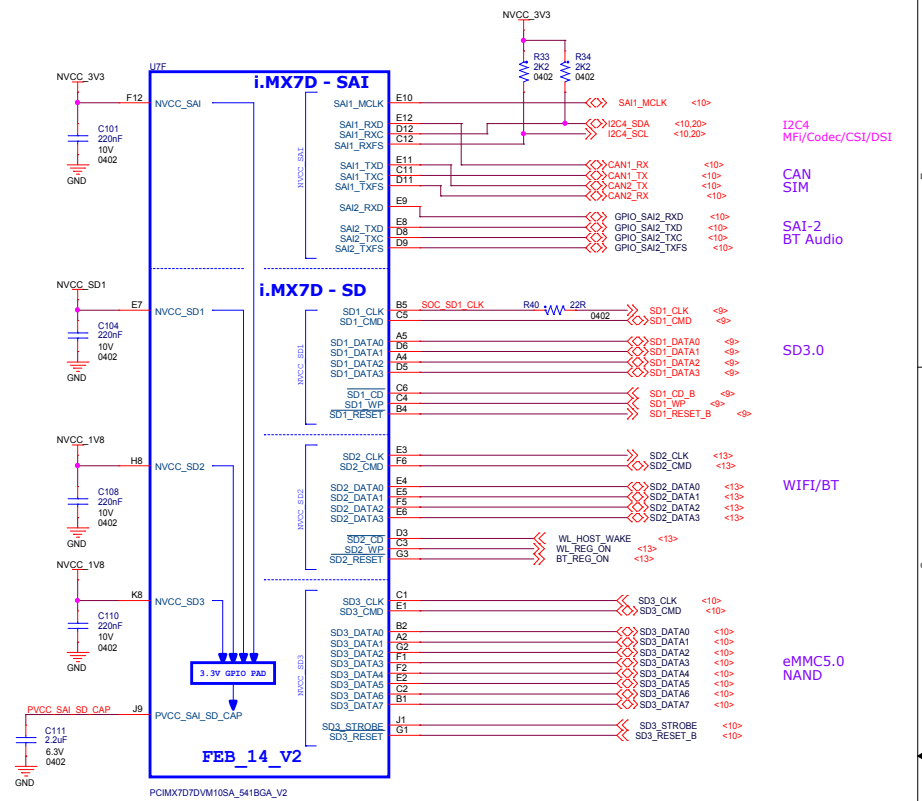
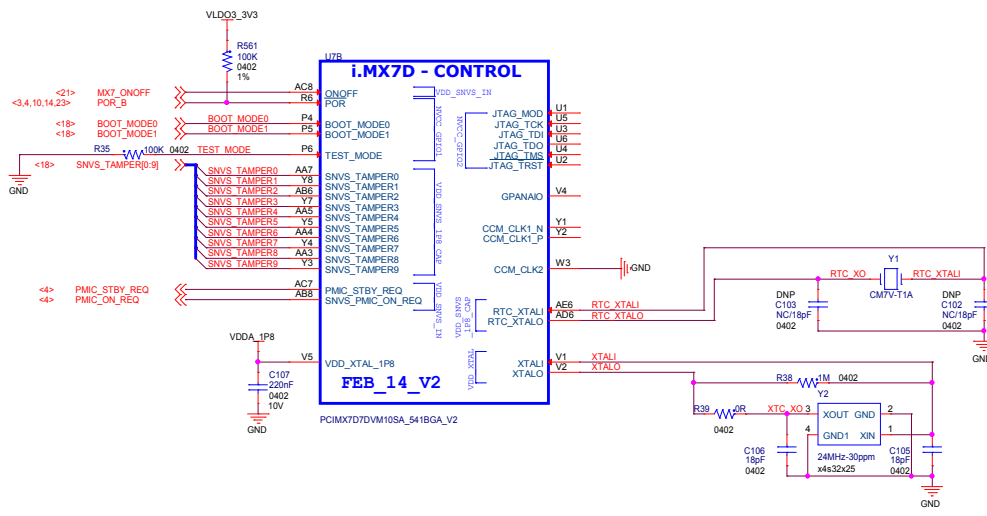
FEB 14 V2

**freescale**

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 Drawing Title: **MCIMX7D-SABRE**  
 Page Title: **05 CPU Power**

Size	Document Number	Source	Rev
C	SCH-28590	SCH-28590:SPF-28590	D

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I2C4 MFI/Codec/CSI/DSI

CAN SIM

SAI-2 BT Audio

SD3.0

WiFi/BT

eMMC5.0 NAND

**freescale**

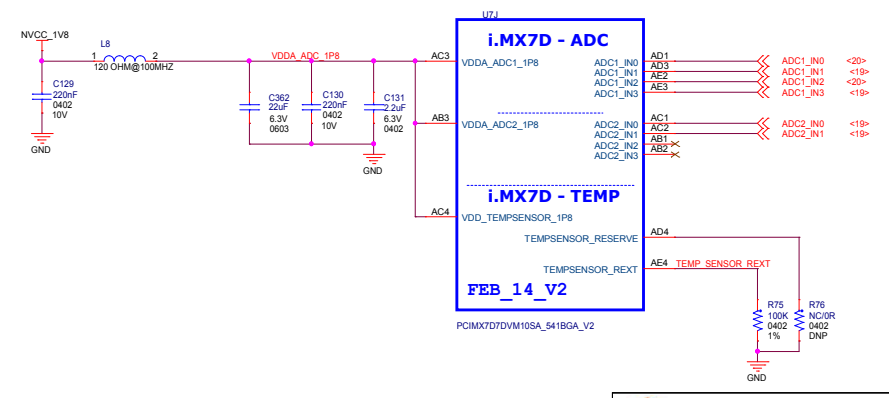
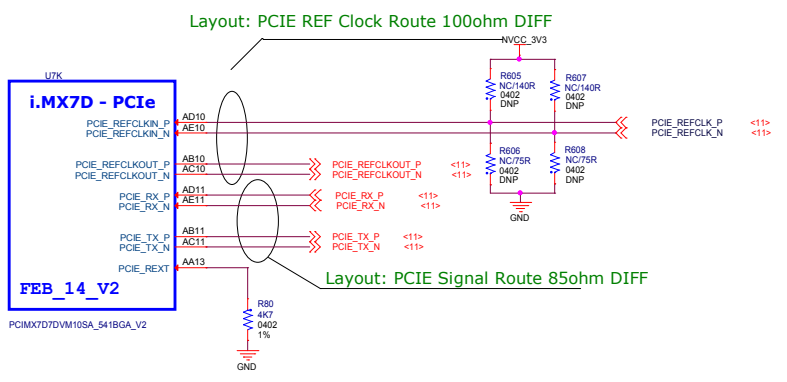
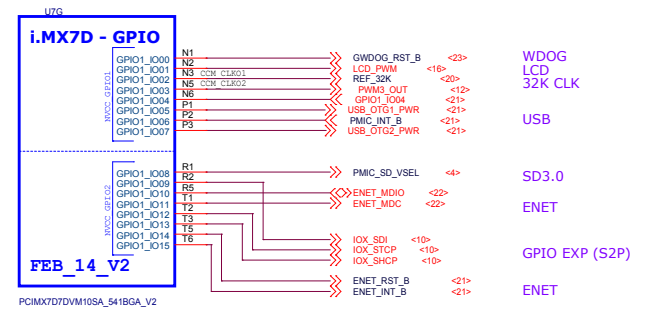
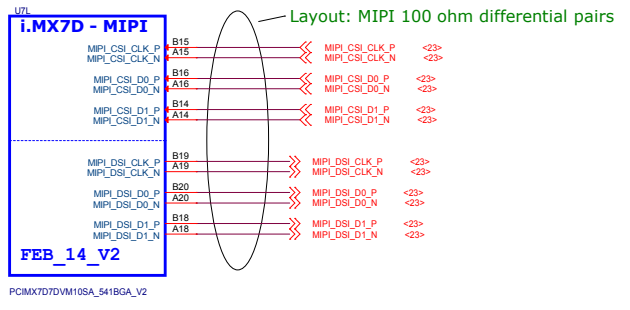
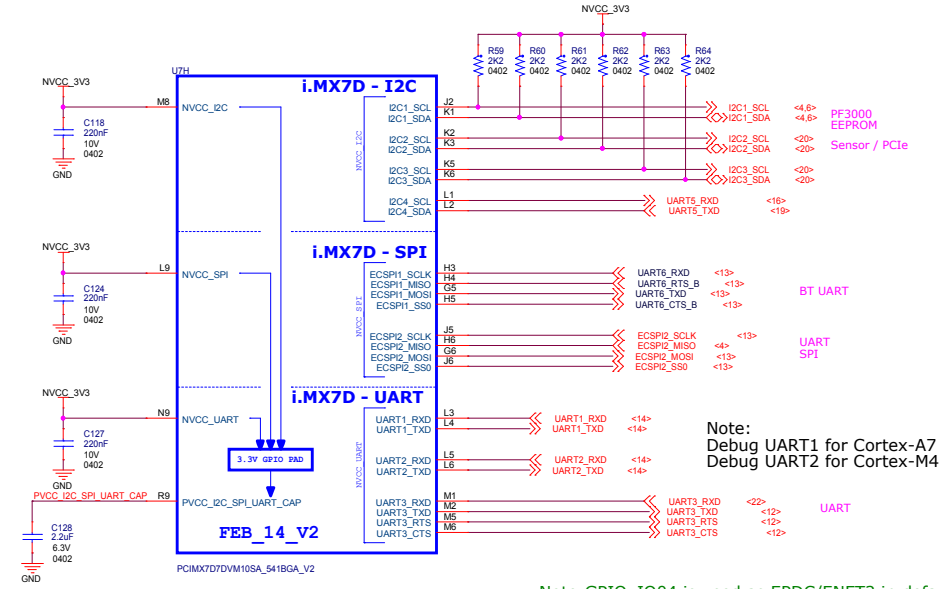
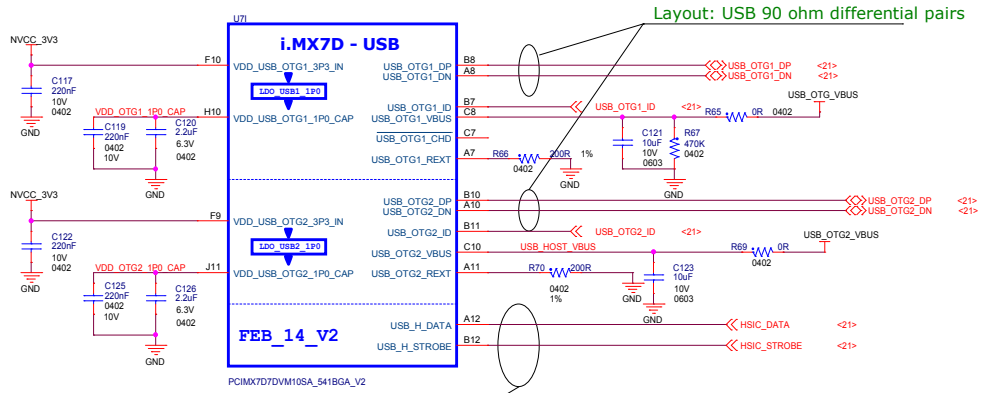
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Page Title: **06 CPU Signal 1**

Size C Document Number SOURCE: SCH-28590: SPF-28590 Rev D

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**freescale**

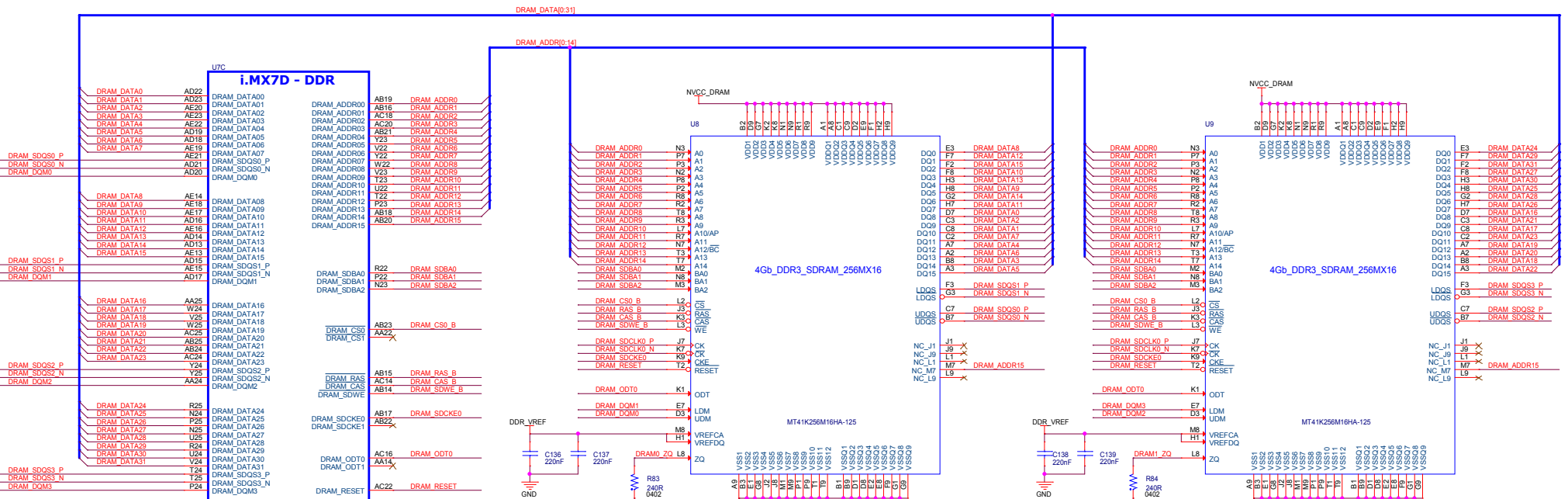
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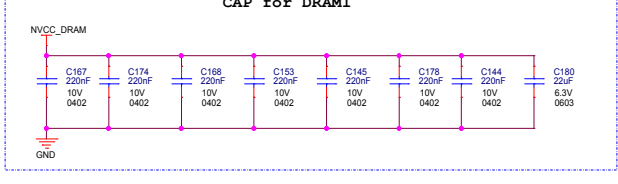
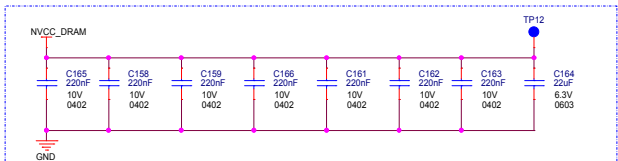
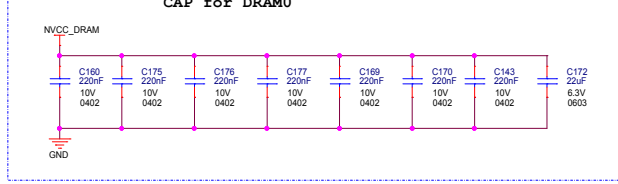
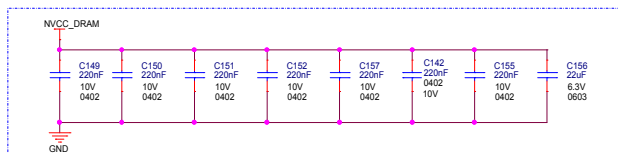
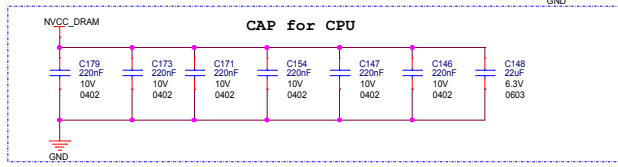
Page Title: **07 CPU Signal 2**

Date: Wednesday, December 06, 2011 Sheet 7 of 23

# DDR



Clock terminators: Place termination resistor on each of the chip of CLK signals

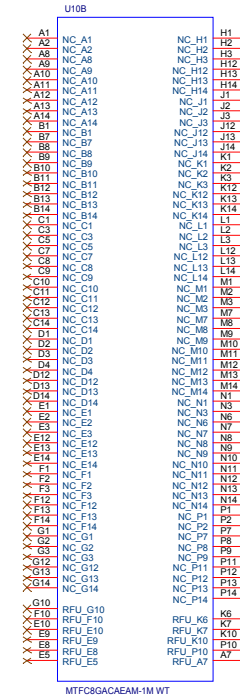
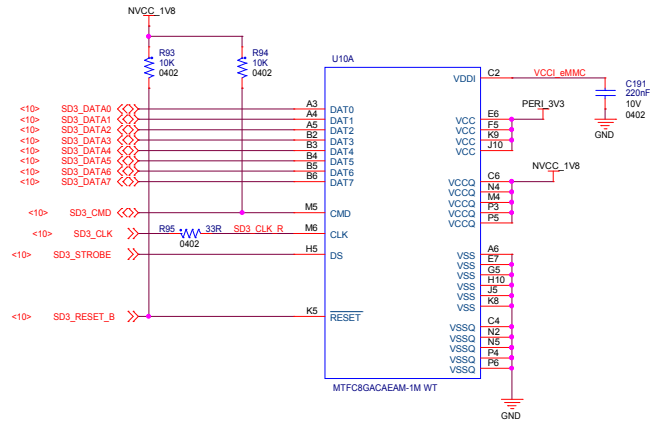
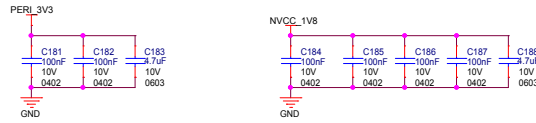


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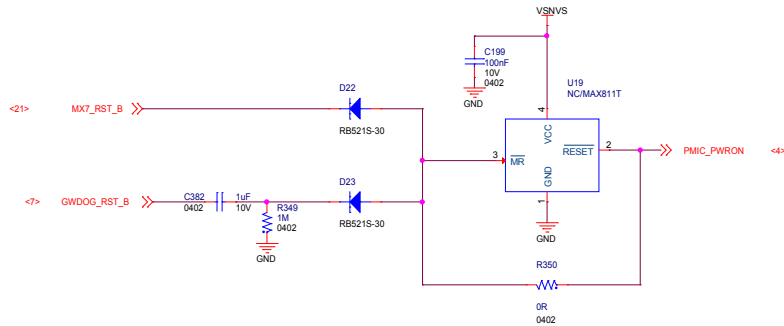
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 Page Title: **08 DDR3 Memory**  
 Size C Document Number SOURCE: SCH-28590-SPF-28590 Rev D  
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# eMMC 5.0



# WATCH DOG

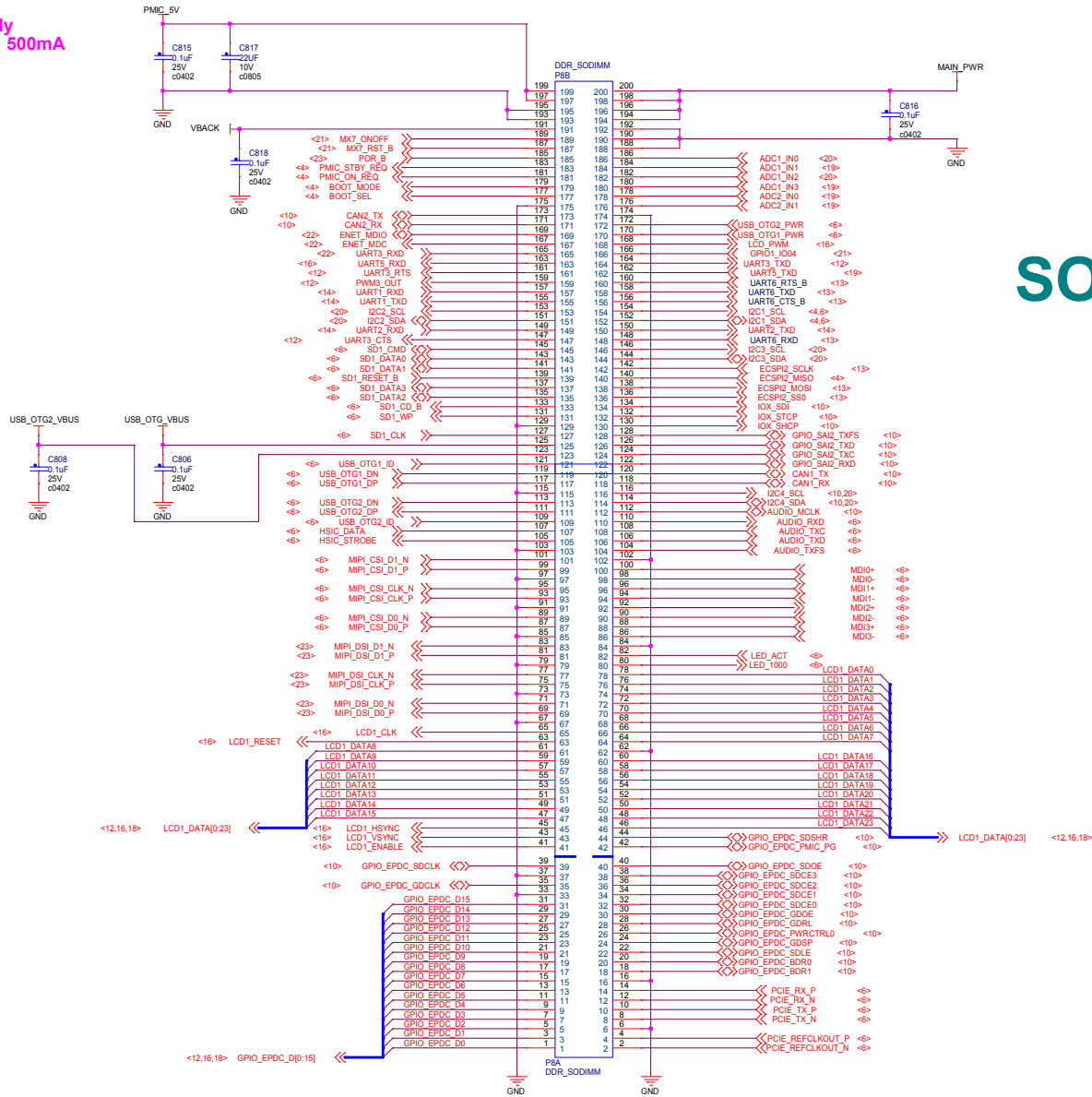


**freescale**

ICAP Classification: FCP: \_\_\_\_\_ FIUO: \_\_\_\_\_ PUBI: X  
 Drawing Title: **MCIMX7D-SABRE**  
 Page Title: **09 eMMC/NAND/QSPI/SD**

Size C	Document Number	SOURCE: SCH-28590:SPF-28590	Rev D
Date: Wednesday, December 06, 2017		Sheet 8 of 23	

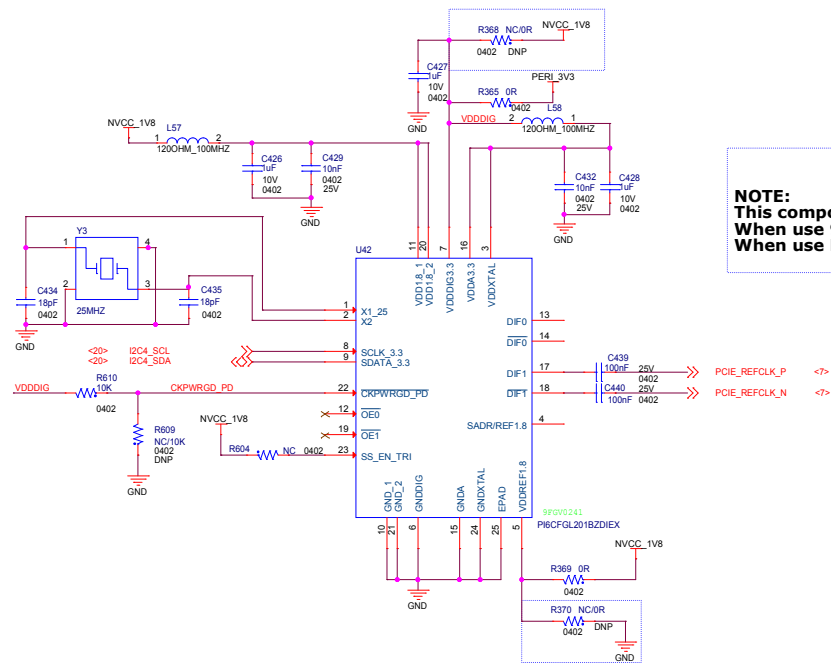
# Maxim PMIC 5v supply  
current for Base Board: 500mA



# SODIMM 200

		<b>Microcontroller Solutions Group</b> 6501 William Cannon Drive West Austin, TX 78735-8598	
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Designer: DESIGNER	Drawing Title: <b>MCIMX6UL-CM</b>	ICAP Classification: FCP	FIUC: X PUBL
Drawn by: DRAWN_BY	Page Title: <b>CPU-SODIMM200</b>		
Approved: APPROVER	Size C	Document Number SCH-28617 PDF: SPF-28617	Rev C1
Date: Wednesday, December 06, 2017		Sheet 11 of 13	

# PCI-E CLK Generator

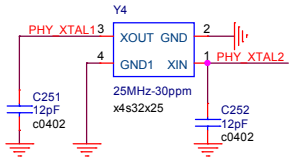


**NOTE:**  
 This component share PCB package  
 When use 9FGV0241 populate R368 & R370, de-populate R365 & R369.  
 When use PI6CFG201BZDIEX populate R365 & R369, de-populate R368 & R370 (default).

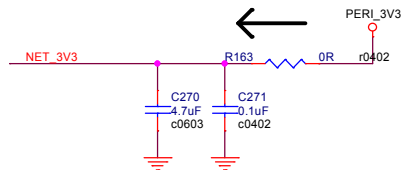
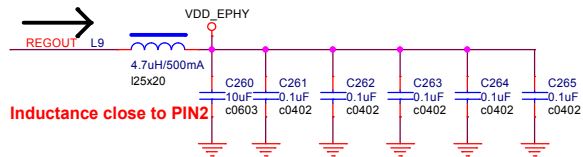
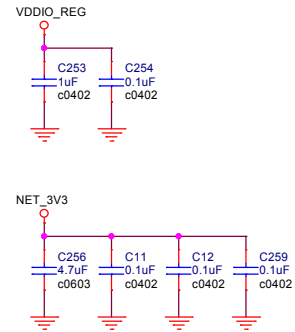
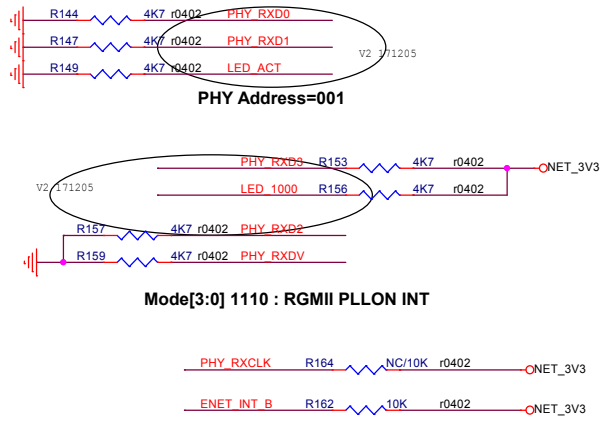
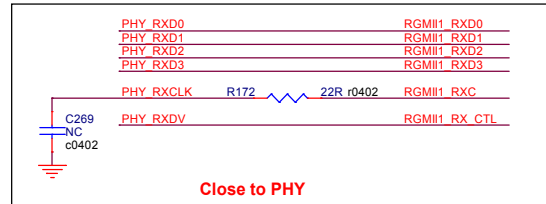
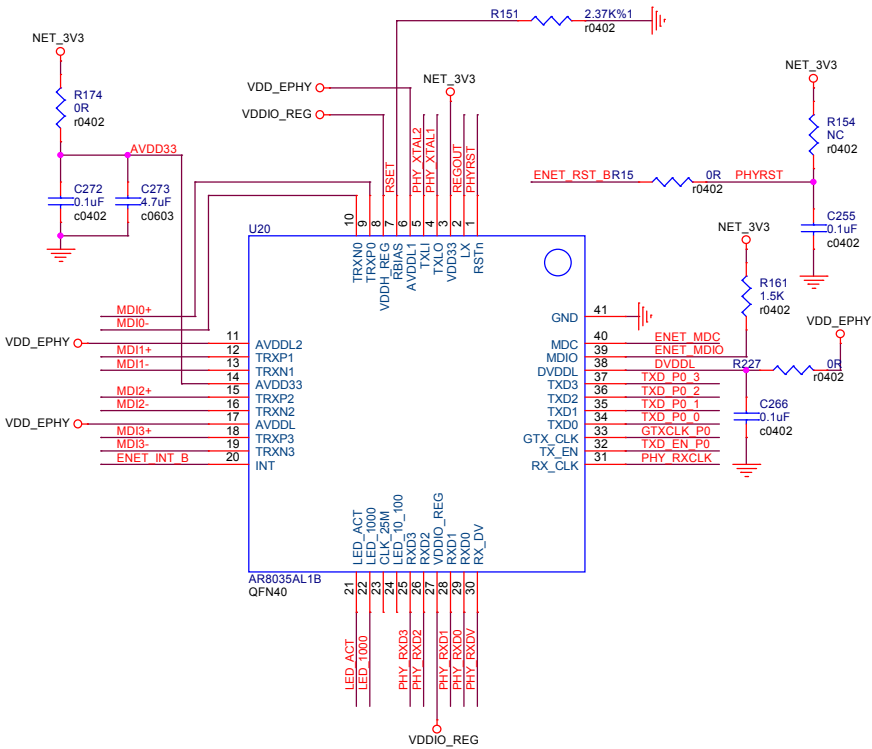
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 TXD\_P0\_3 <<22>>  
 GTXCLK\_P0 <<22>>  
 TXD\_EN\_P0 <<22>>

RGMIH1\_RXD0 16  
 RGMIH1\_RXD1 16  
 RGMIH1\_RXD2 16  
 RGMIH1\_RXD3 16  
 RGMIH1\_RX\_CTL 16  
 RGMIH1\_RXC 16

ENET\_RST\_B 16  
 ENET\_INT\_B 11  
 ENET\_MDC 16  
 ENET\_MDIO 16



MDI3+ >>MDI3+ 16  
 MDI3- >>MDI3- 16  
 MDI1+ >>MDI1+ 16  
 MDI1- >>MDI1- 16  
 MDI2+ >>MDI2+ 16  
 MDI2- >>MDI2- 16  
 MDI0+ >>MDI0+ 16  
 MDI0- >>MDI0- 16  
 LED\_ACT >>LED\_ACT 16  
 LED\_1000 >>LED\_1000 16



**Boardcon Confidential**

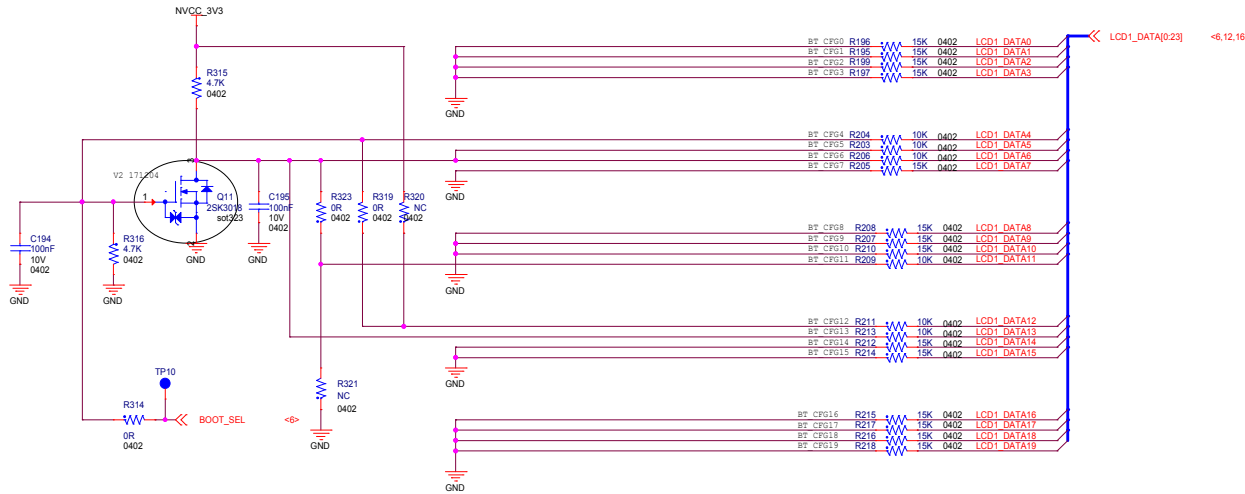
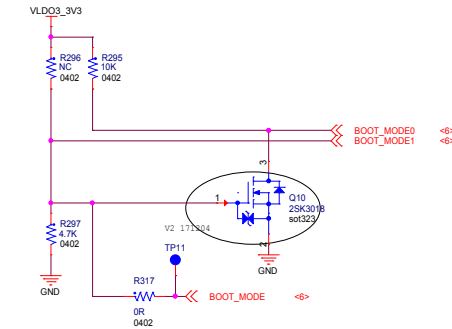
**Boardcon Inc** Room702-710, XinAn Business Building, 45Zone, BaoAn District, Shenzhen China +86-755-27571591

**Title** 10/100/1000M-PHY

<b>Size</b> A3	<b>Document Number</b> CMX7D	<b>Drawn</b> Dawen	<b>Rev</b> 2
<b>Date:</b> Wednesday, December 06, 2017		<b>Sheet</b> 17	<b>of</b> 17

# BOOT MODE

BOOT_MODE	[1]	[0]
FUSES	0	0
<b>Serial Downloader</b>	<b>0</b>	<b>1</b>
INTERNAL BOOT	1	0
TEST MODE	1	1



BOOT\_SEL

	Boot Sel	R319	R320	R323	R321
SD	H	0R	NC	0R	NC
<b>EMMC</b>	<b>L</b>	<b>0R</b>	<b>NC</b>	<b>0R</b>	<b>NC</b>

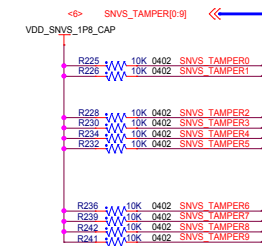
## Boot Config

	SD	EMMC	Nand
BT_CFG4	1	0	0
BT_CFG5	0	1	1
BT_CFG6	0	1	1
BT_CFG11	0	1	0
BT_CFG12	1	0	1
BT_CFG13	0	1	1

## BOOT TABLE

1	2	3	4	5	6	7	8
BT_CFG[14]	BT_CFG[13]	BT_CFG[12]	BT_CFG[11]	BT_CFG[10]	BT_CFG[6]	BT_CFG[5]	BT_CFG[4]
001 = SD/eSD Boot					0	0	<b>Bus Width:</b> 0 - 1-bit 1 - 4-bit
010 = MMC/eMMC Boot			<b>Port Select:</b> 00 - eSDHC1 01 - eSDHC2 10 - eSDHC3		<b>Bus Width:</b> 000 - 1-bit 001 - 4-bit 010 - 8-bit 101 - 4-bit DDR (MMC 4.4) 110 - 8-bit DDR (MMC 4.4)		
011 = NAND Boot			<b>Pages In Block:</b> 00 - 128 01 - 64 10 - 32 11 - 256		<b>BOOT_SEARCH_COUNT:</b> 00 - 2 01 - 2 10 - 4 11 - 8		0
100 = QSPI Boot			0	0	0	0	0

# TAMPER



ICAP Classification: FCP: FIUO: PUB: X

Drawing Title: **MCIMX7D-SABRE**

Page Title: **18 Boot Config/Tamper**

Size C Document Number SOURCE: SCH-28590-SPF-28590 Rev D

Date: Thursday, December 07, 2017 Sheet 18 of 23