Table of Content

Revision History

Rev. Code	Date	Description
B	22/09/2015	Initial Draft
B1	21/01/2016	- Changed Q8 from 2N7002 to MMBT3904. - Reconnection U43 SW with the anode of D25. - DNP the capacitor:C6,C121. - Changed the power of JTAG from PERI_3V3 to VLDO3_3V3. - PCIe DNP the resistor:R605,R606,R607,R608. Changed C442 and C443 to 0ohm resistor (R632,R633). Add 49.9 1% 0402 resistors (R634,R635) on PCIE_REFCLKOUT_P/N to GND. - Add the mosfet Q36 on the NET "CSI_PWDN". - Add blocking capacitor(C458,C459) before the terminal reisistor. - Add Schottky diode(D26) to isolate POR_B with JTAG interface. - Use the LDO U44 instead of Q11. - Add the 0ohm resistor(R641) connect the pin CCM_CLK2 to GND. - Add the U45 to match electrical level.
C	28/01/2016	- Changed the revision from "B1" to "C". - Delete the capacitors C312 and C314. - Add several GND test points TP68--TP75 around the DDR3. - Changed connectors type of the J29&J30
D	09/03/2016	- Changed the revision from "C" to "D". - Corrected the PCB decal of the Q8. - Changed connection of the J20.

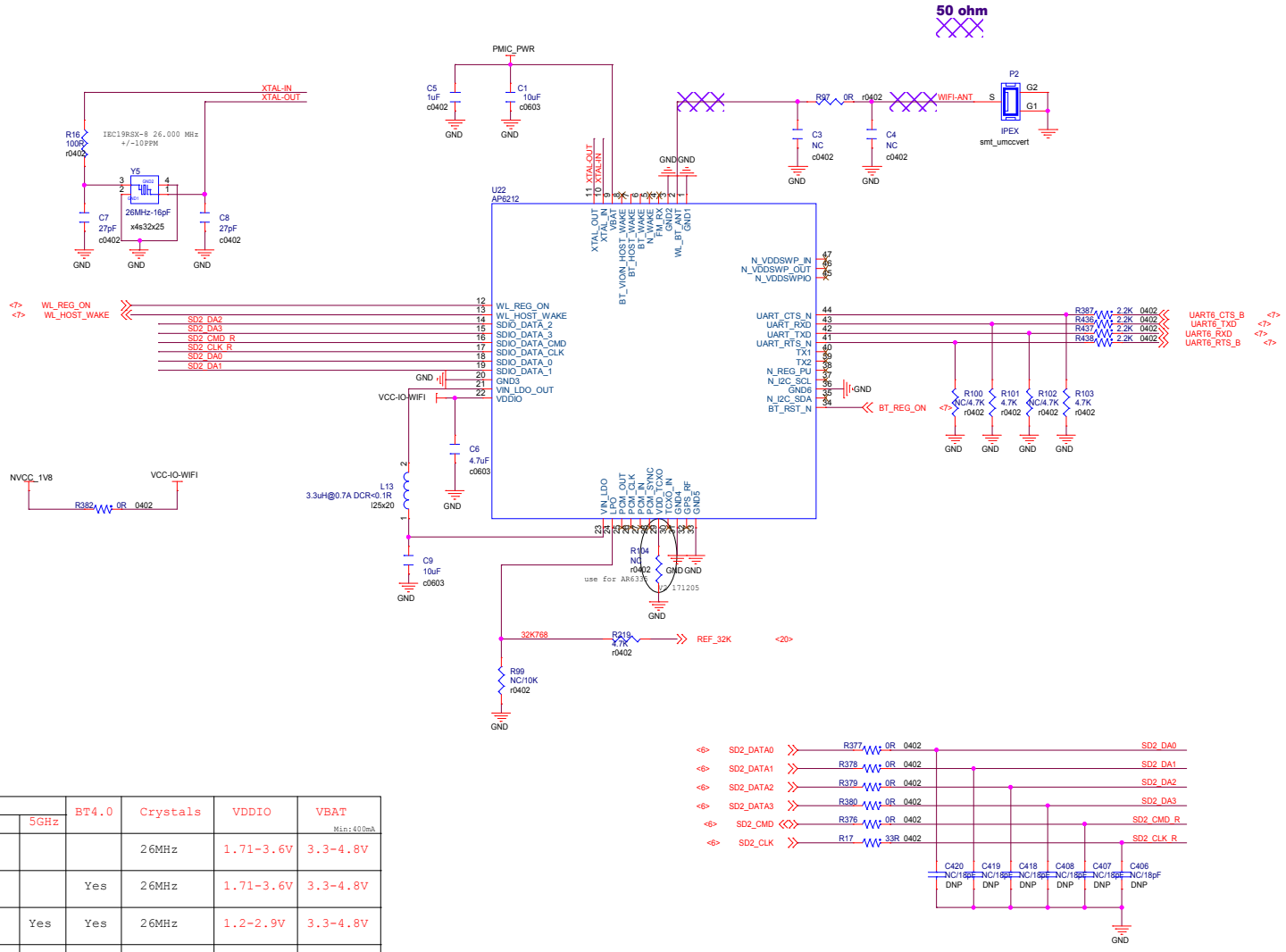
MCIMX7D-SABRE

freescale

Multimedia Application Division,
Wireless & Mobile System Group

ICAP Classification: FCP: FIUO: PUBI:

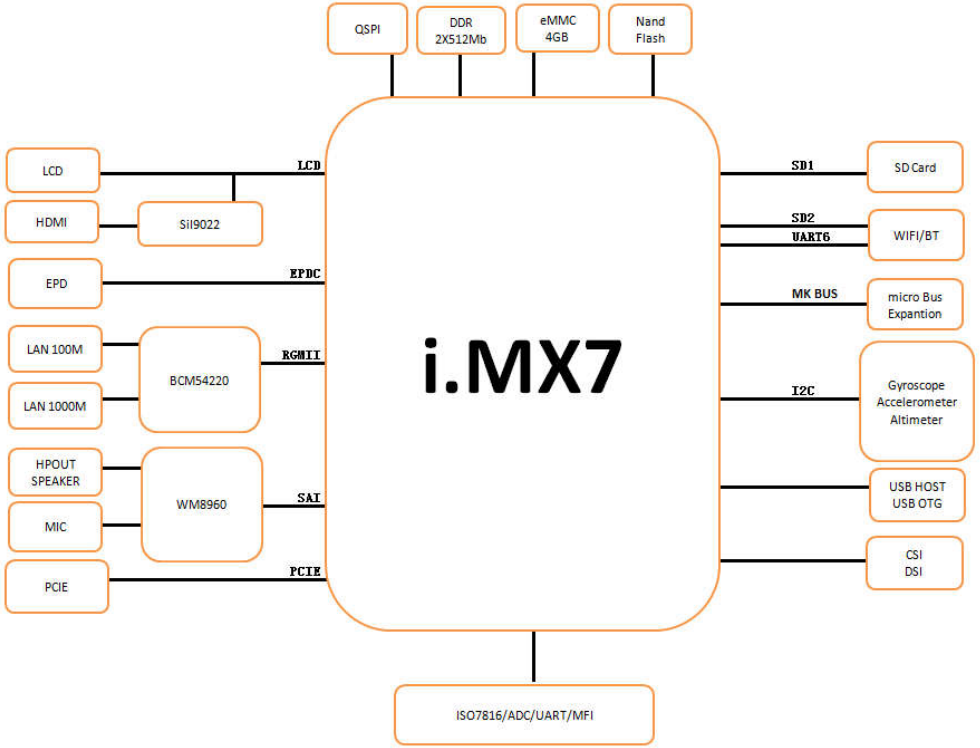
Designer:	Drawing Title: MCIMX7D-SABRE	
Drawn by:	Page Title: 01 Title Sheet	
Approved: <Approver>	Size A2	Document Number SOURCE:SCH-28590:SPF-28590 Rev D
	Date: Wednesday, December 06, 2017	Sheet 1 of 23



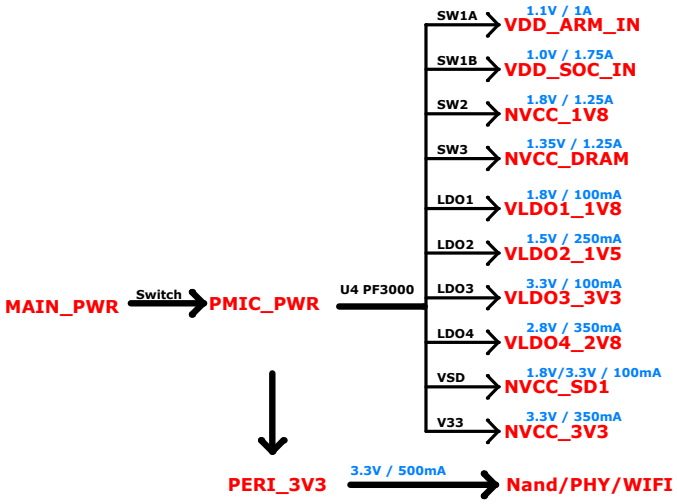
OPTION	WIFI				BT4.0	Crystals	VDDIO	VBAT
	a	b/g/n	ac	5GHz				Min:400mA
AP6181		Yes				26MHz	1.71-3.6V	3.3-4.8V
AP6212		Yes			Yes	26MHz	1.71-3.6V	3.3-4.8V
AP6330	Yes	Yes		Yes	Yes	26MHz	1.2-2.9V	3.3-4.8V
AP6335	Yes	Yes	Yes	Yes	Yes	37.4MHz	1.2-2.9V	3.3-4.8V

Title	<Title>	
Size C	Document Number <Doc>	Rev <RevCode>
Date: Wednesday, December 06, 2017	Sheet 1 of 1	

MCIMX7D-SABRE Block Diagram



Power Distribution Diagram



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ICAP Classification: FCP: ___ FIUO: ___ PUBI: X

Drawing Title: MCIMX7D-SABRE

Page Title: 02 Block Diagram

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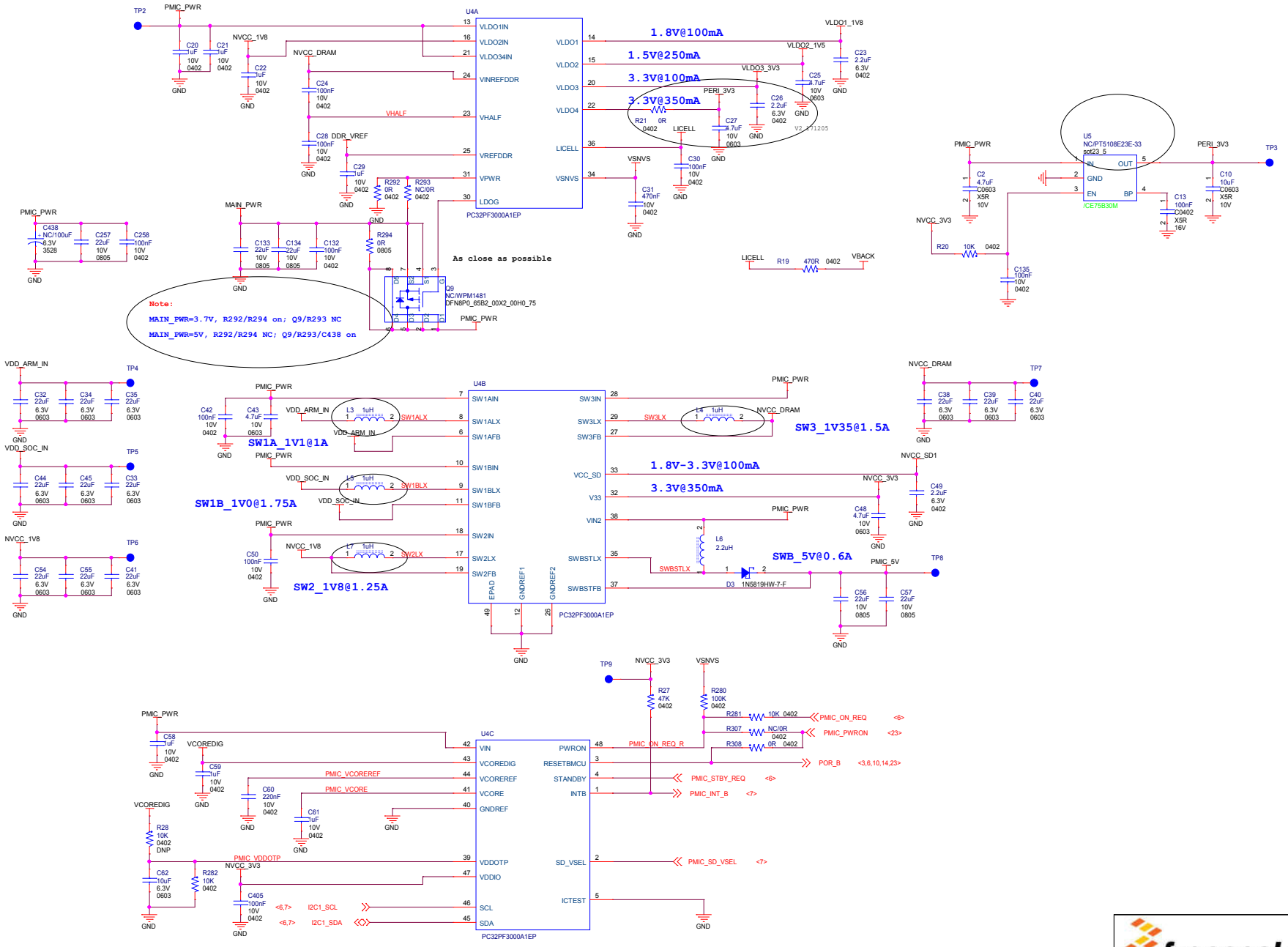
PMIC



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Drawing Title: MCIMX7D-SABRE

Page Title: 04 PMIC

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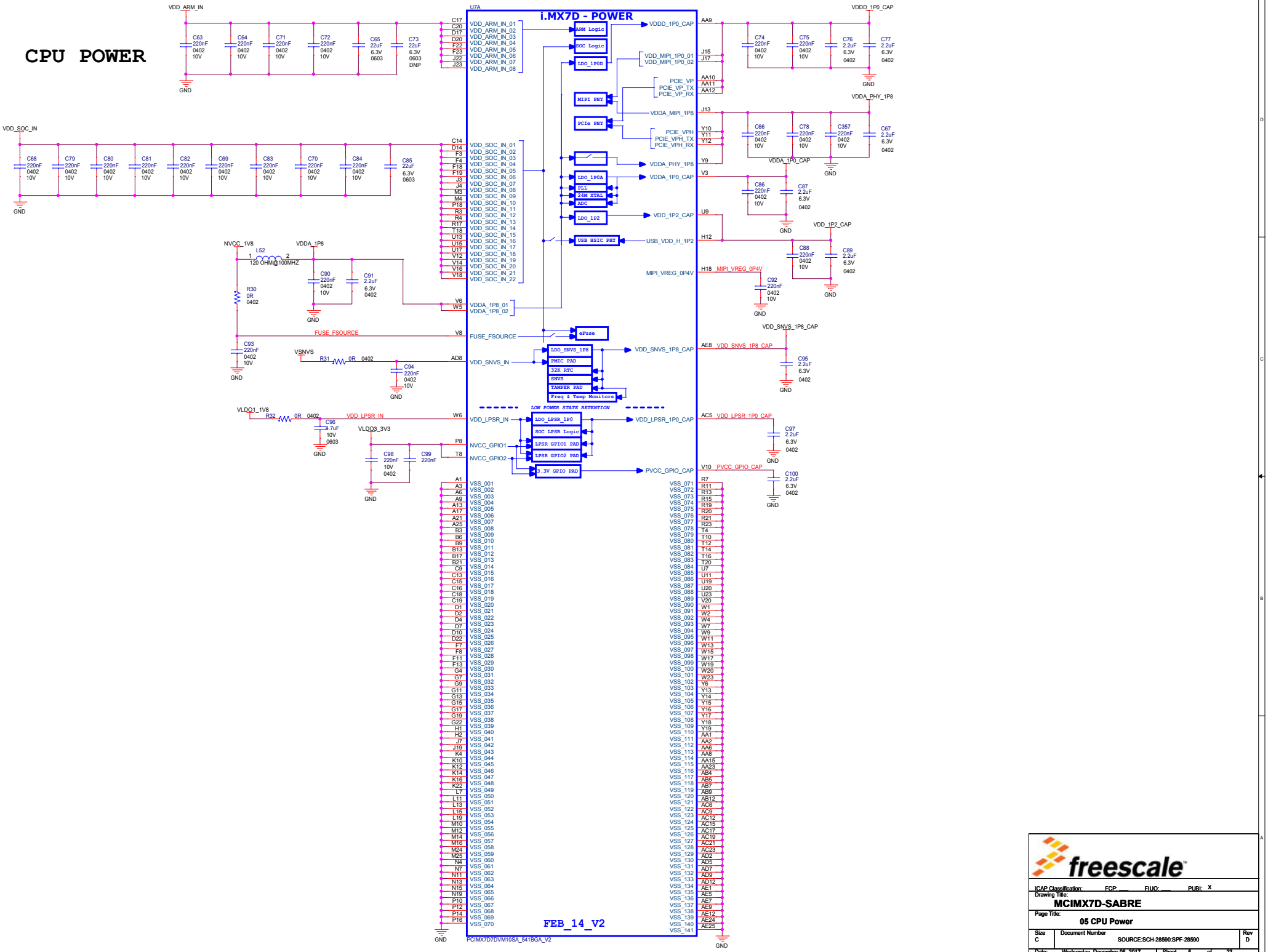
CPU POWER



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ICAP Classification: FCP: ___ FIUO: ___ PUBI: X

Drawing Title: MCIMX7D-SABRE

Page Title: 05 CPU Power

Size	Document Number	Rev
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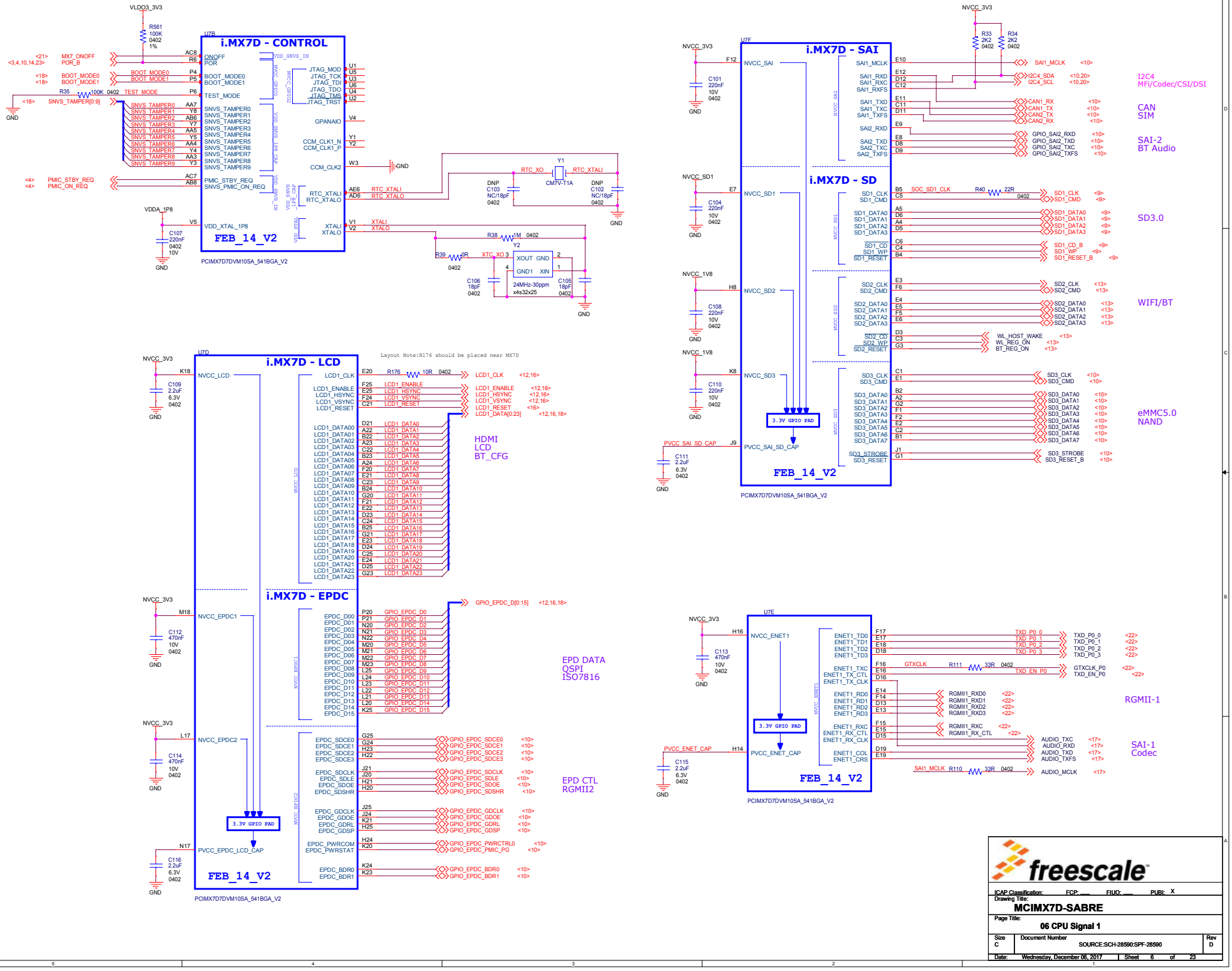

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ICAP Classification: FCP: ___ FIUO: ___ PUBI: X

Drawing Title: MCIMX7D-SABRE

Page Title: 06 CPU Signal 1

Size	Document Number	Rev
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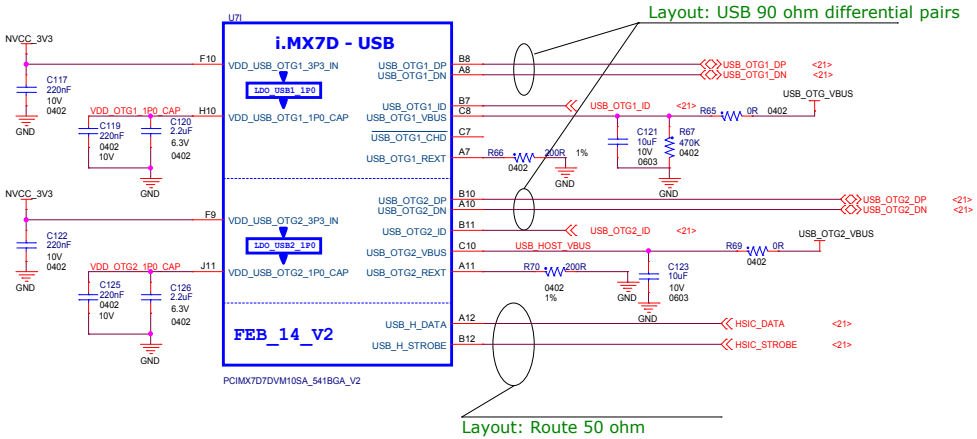
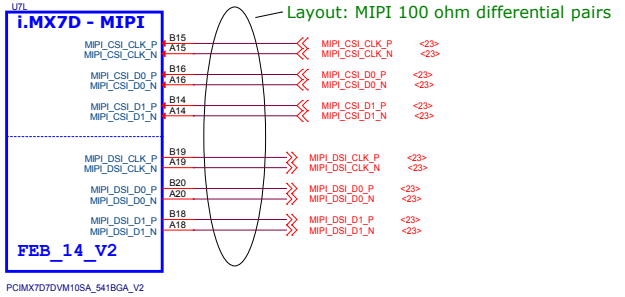
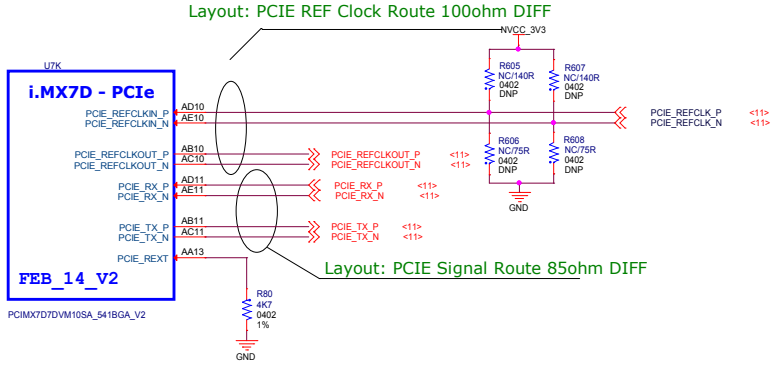
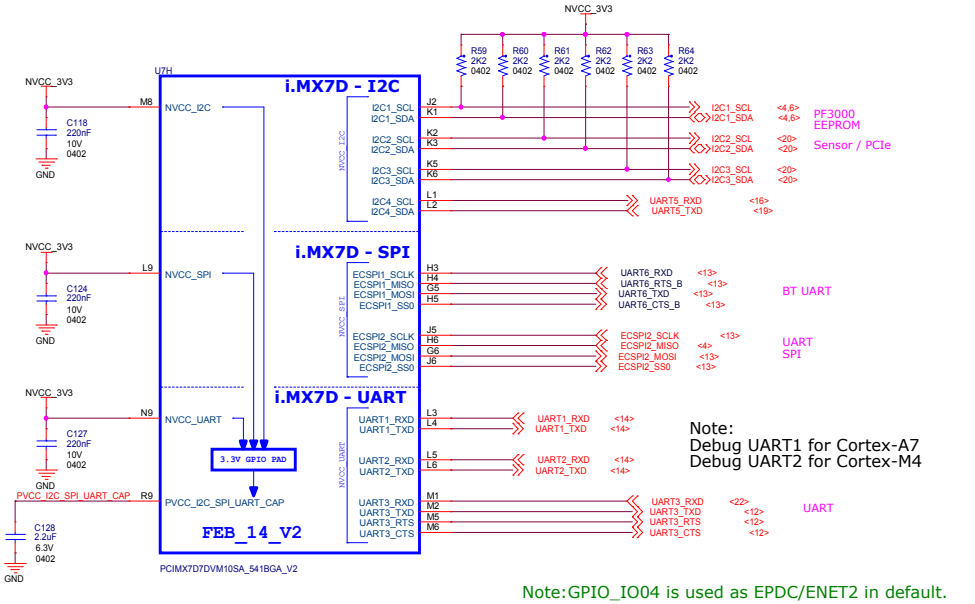
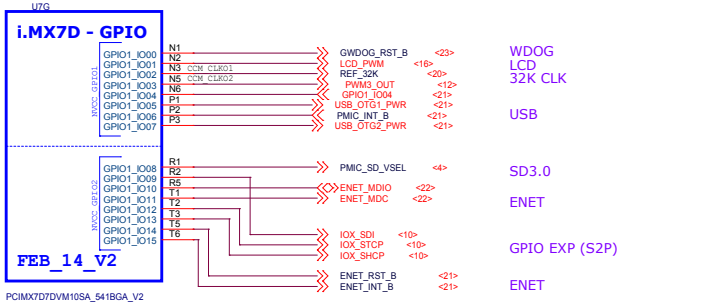


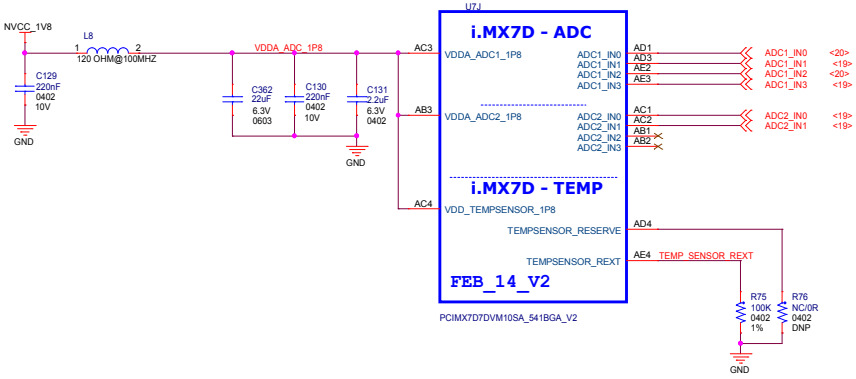






Note:GPIO_IO04 is used as EPDC/ENET2 in default.





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Drawing Title: **MCIMX7D-SABRE**

Page Title: **07 CPU Signal 2**

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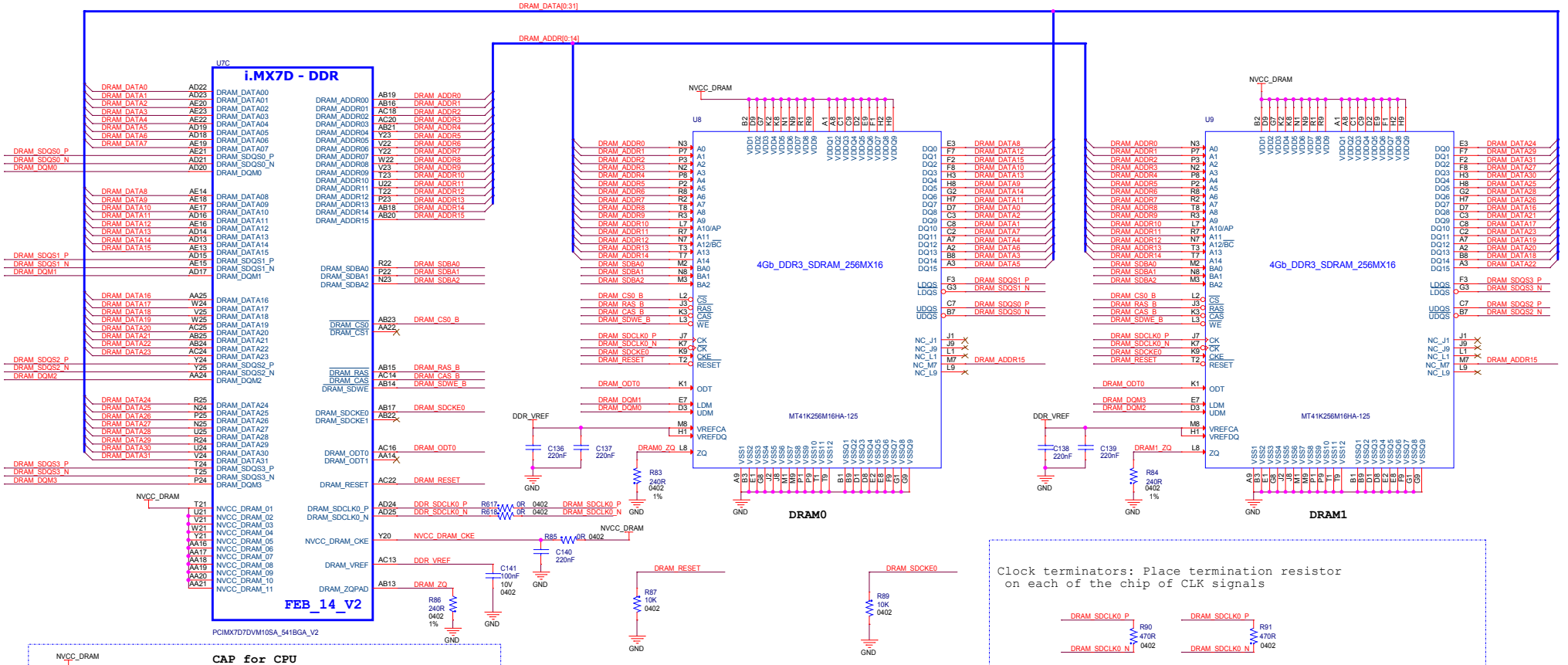
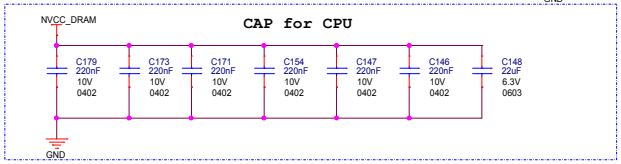
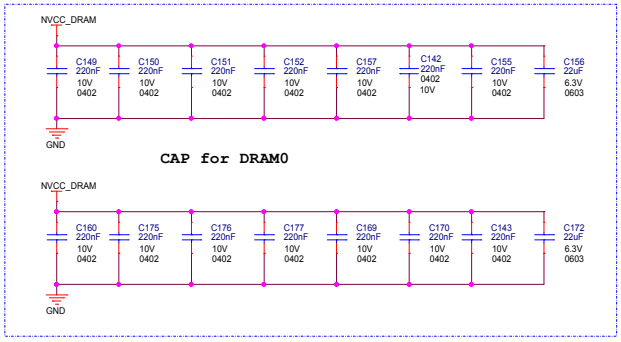
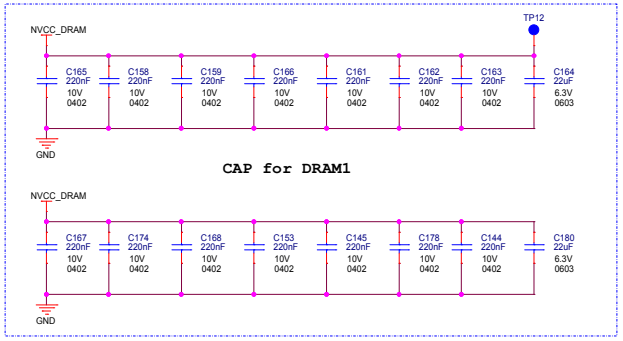
DDR









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Drawing Title: MCIMX7D-SABRE

Page Title: 08 DDR3 Memory

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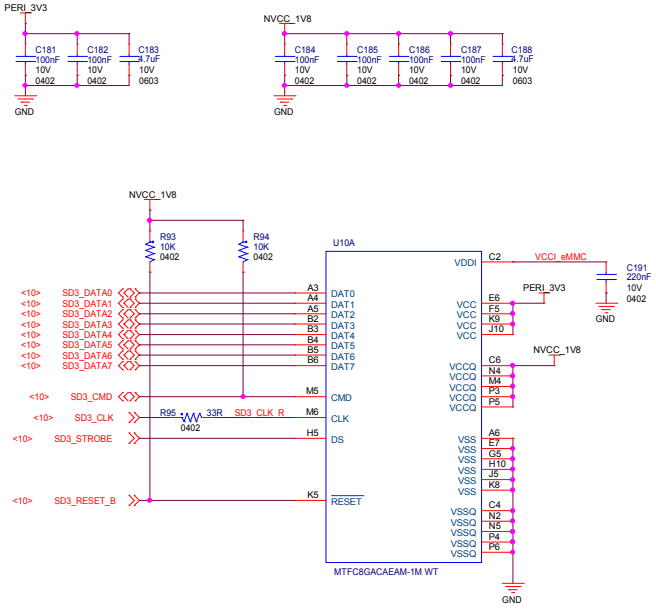
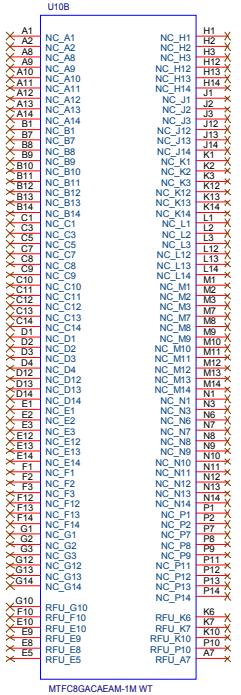
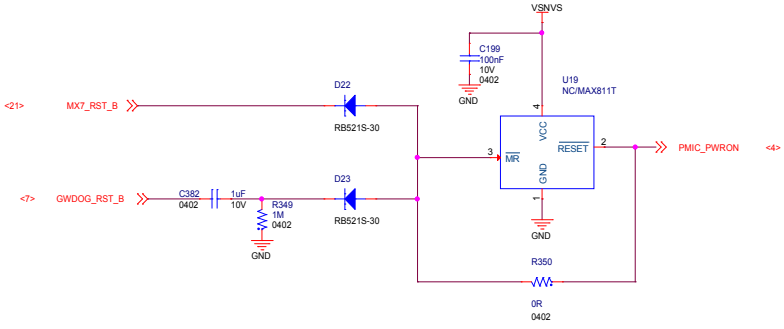
eMMC 5.0





WATCH DOG



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ICAP Classification: FCP: ___ FIUO: ___ PUBI: X

Drawing Title: MCIMX7D-SABRE

Page Title: 09 eMMC/NAND/QSPI/SD

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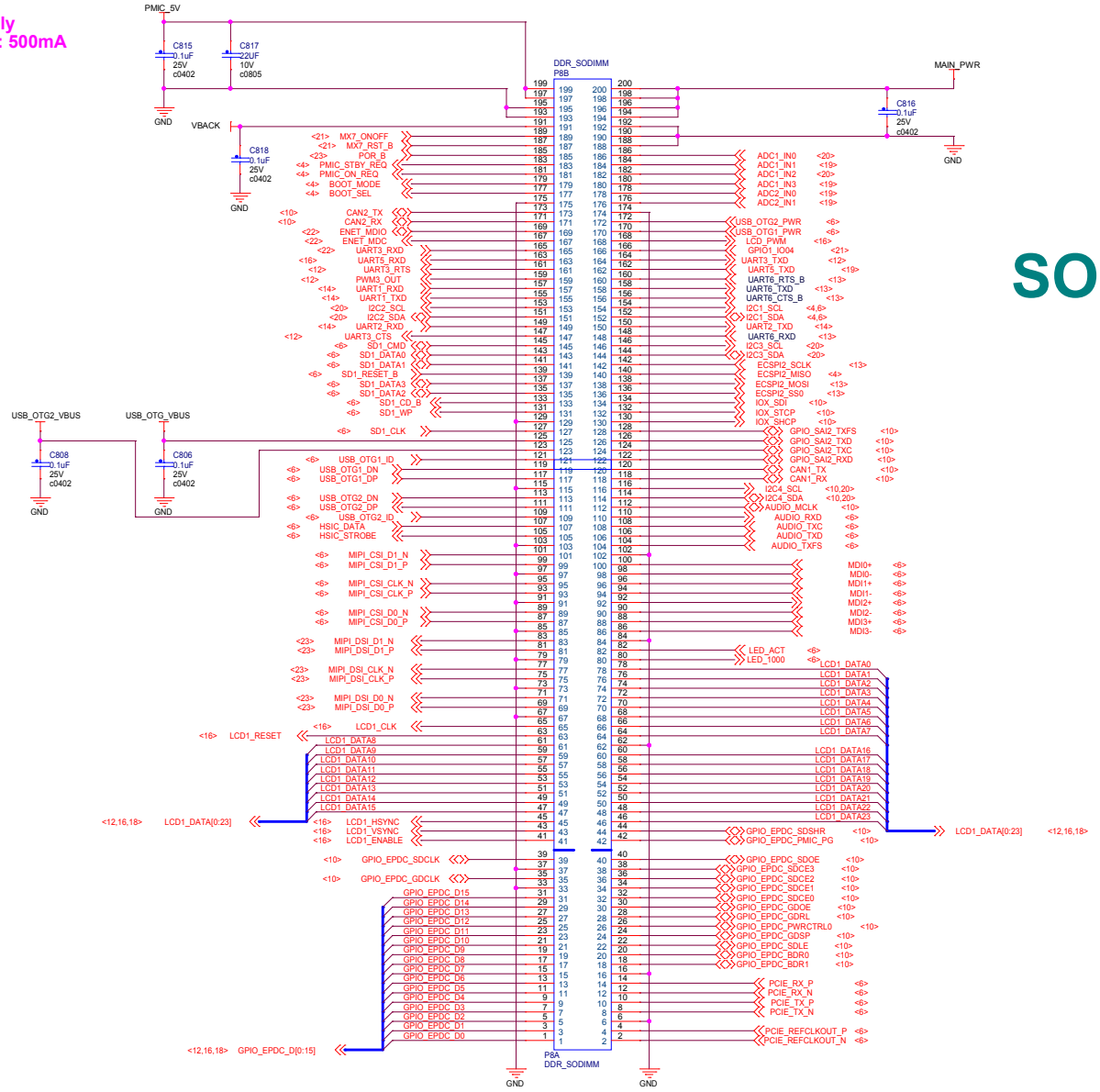
Maxim PMIC_5v supply current for Base Board: 500mA



SODIMM 200

freescale semiconductor
Microcontroller Solutions Group
6501 William Cannon Drive West
Austin, TX 78735-8598

ICAP Classification: FCP: FIUO: X PUBI:

Designer: DESIGNER	Drawing Title: MCIMX6UL-CM		
Drawn by: DRAWN_BY	Page Title: CPU-SODIMM200		
Approved: APPROVER	Size C	Document Number SCH-28617 PDF: SPF-28617	Rev C1
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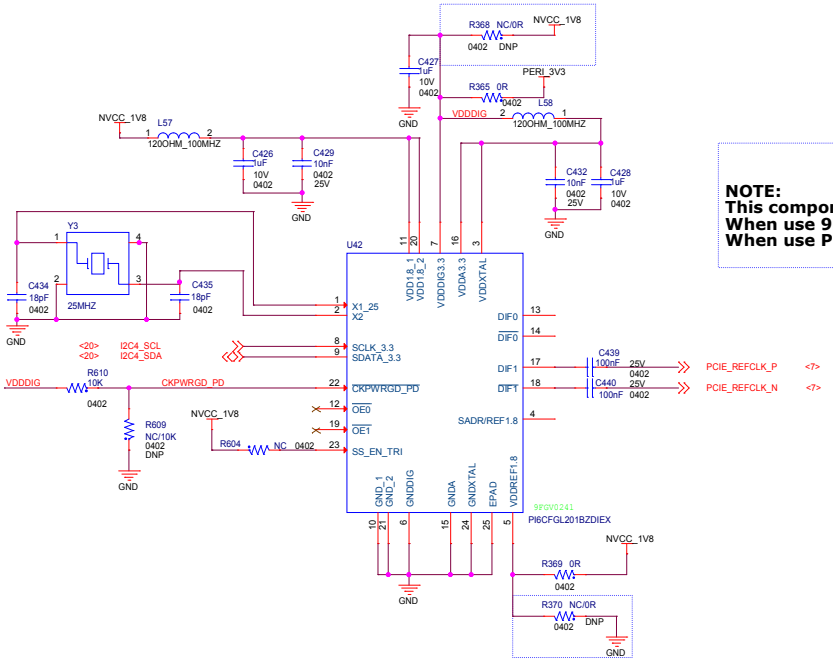
PCI-E CLK Generator



NOTE:
This component share PCB package
When use 9FGV0241 populate R368 & R370, de-populate R365 & R369.
When use PI6CFGL201BZDIEX populate R365 & R369, de-populate R368 & R370 (default).

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Drawing Title: MCIMX7D-SABRE

Page Title: PCIE CLK Generator

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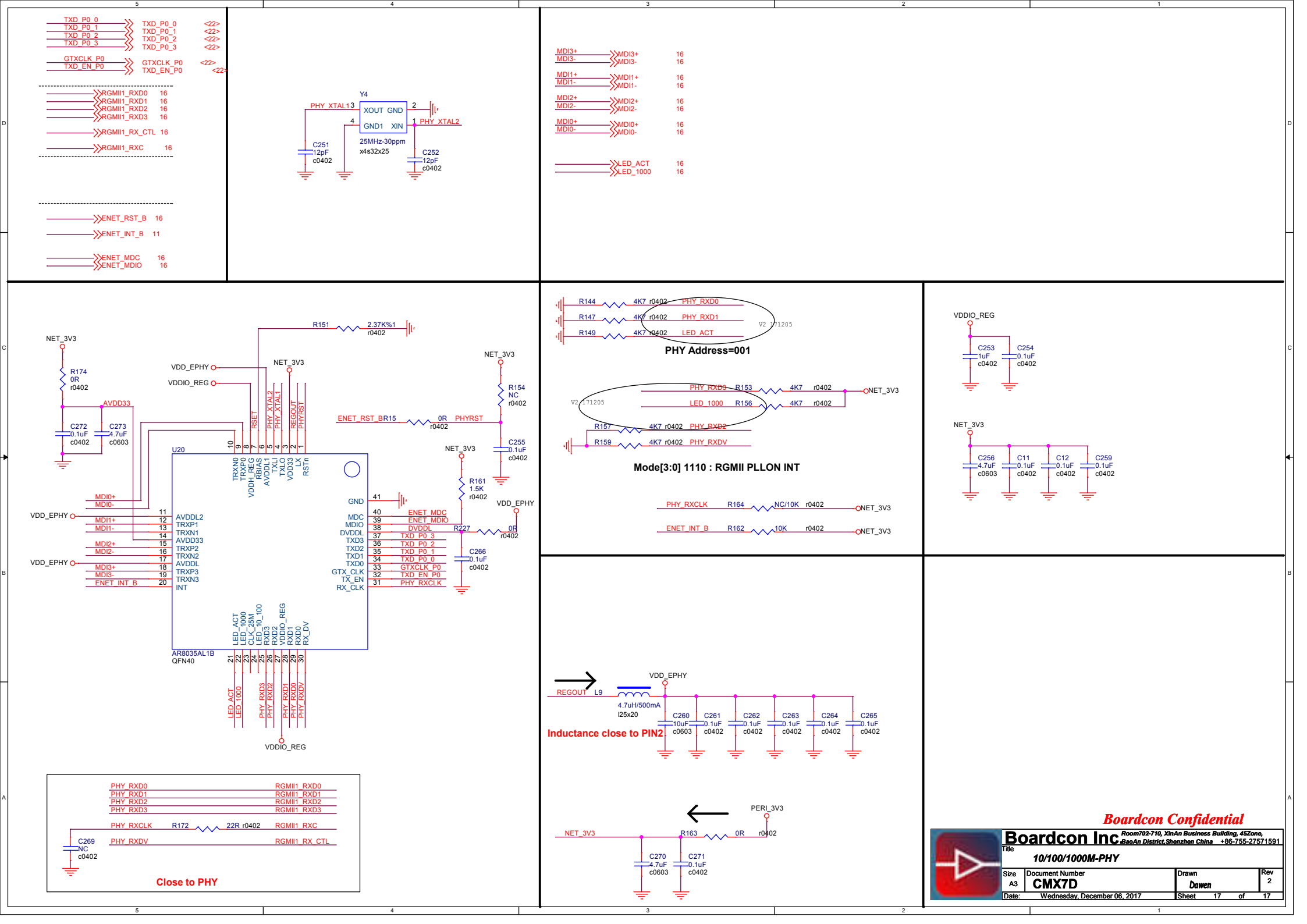
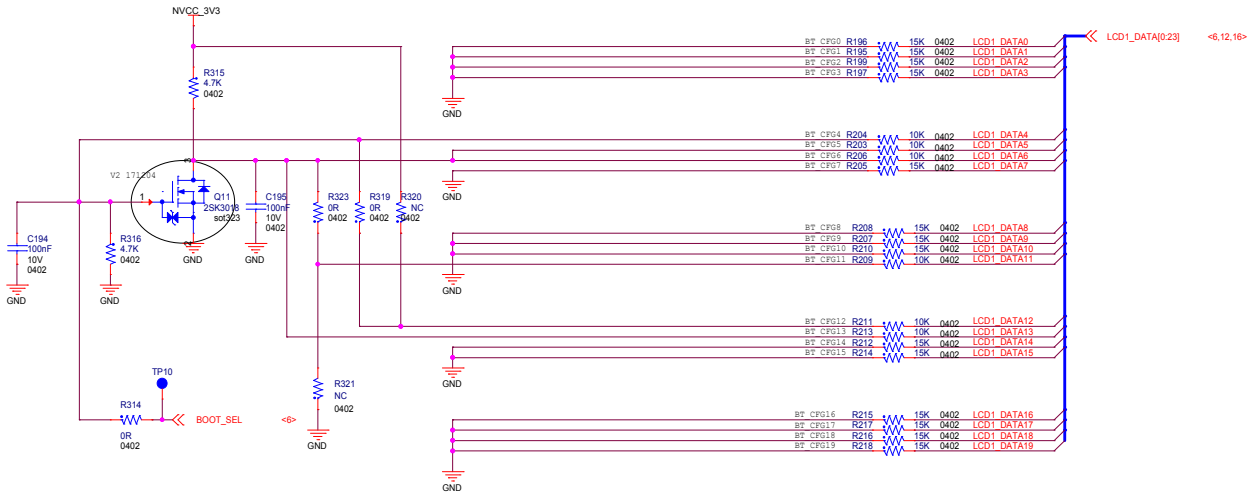
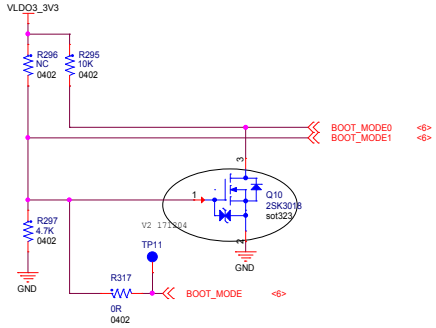

TXD_P0_0
TXD_P0_1
TXD_P0_2
TXD_P0_3
GTXCLK_P0
TXD_EN_P0
RGMII1_RXD0
RGMII1_RXD1
RGMII1_RXD2
RGMII1_RXD3
RGMII1_RX_CTL
RGMII1_RXC
ENET_RST_B
ENET_INT_B
ENET_MDC
ENET_MDIO
Y4
PHY_XTAL1
PHY_XTAL2
XOUT GND
GND1 XIN
25MHz-30ppm
x4s32x25
C251 12pF c0402
C252 12pF c0402
MDI3+
MDI3-
MDI1+
MDI1-
MDI2+
MDI2-
MDI0+
MDI0-
LED_ACT
LED_1000
NET_3V3
R174 0R r0402
AVDD33
C272 0.1uF c0402
C273 4.7uF c0603
VDD_EPHY
VDDIO_REG
R151 2.37K%1 r0402
U20
AR8035AL1B
QFN40
R154 NC r0402
ENET_RST_B
R15 0R r0402
PHYRST
C255 0.1uF c0402
R161 1.5K r0402
R227 0R r0402
C266 0.1uF c0402
MDI0+
MDI0-
MDI1+
MDI1-
MDI2+
MDI2-
MDI3+
MDI3-
ENET_INT_B
AVDDL2
TRXP1
TRXN1
AVDD33
TRXP2
TRXN2
AVDDL
TRXP3
TRXN3
INT
GND
MDC
MDIO
DVDDL
TXD3
TXD2
TXD1
TXD0
GTX_CLK
TX_EN
RX_CLK
ENET_MDC
ENET_MDIO
TXD_P0_3
TXD_P0_2
TXD_P0_1
TXD_P0_0
GTXCLK_P0
TXD_EN_P0
PHY_RXCLK
LED_ACT
LED_1000
CLK_25M
LED_10_100
RXD3
RXD2
VDDIO_REG
RXD1
RXD0
RX_DV
PHY_RXD3
PHY_RXD2
PHY_RXD1
PHY_RXD0
PHY_RXDV
R172 22R r0402
C269 NC c0402
Close to PHY
R144 4K7 r0402 PHY_RXD0
R147 4K7 r0402 PHY_RXD1
R149 4K7 r0402 LED_ACT
V2 171205
PHY Address=001
R153 4K7 r0402
R156 4K7 r0402
R157 4K7 r0402 PHY_RXD2
R159 4K7 r0402 PHY_RXDV
Mode[3:0] 1110 : RGMII PLLON INT
R164 NC/10K r0402
R162 10K r0402
C253 1uF c0402
C254 0.1uF c0402
C256 4.7uF c0603
C11 0.1uF c0402
C12 0.1uF c0402
C259 0.1uF c0402
REGOUT
L9
4.7uH/500mA
l25x20
Inductance close to PIN2
C260 10uF c0603
C261 0.1uF c0402
C262 0.1uF c0402
C263 0.1uF c0402
C264 0.1uF c0402
C265 0.1uF c0402
PERI_3V3
R163 0R r0402
C270 4.7uF c0603
C271 0.1uF c0402
Boardcon Confidential
Boardcon Inc
Room702-710, XinAn Business Building, 45Zone, BaoAn District,Shenzhen China +86-755-27571591
Title
10/100/1000M-PHY
Size A3
Document Number CMX7D
Drawn Dawen
Rev 2
Date: Wednesday, December 06, 2017
Sheet 17 of 17



BOOT MODE

BOOT_MODE	[1]	[0]
FUSES	0	0
Serial Downloader	0	1
INTERNAL BOOT	1	0
TEST MODE	1	1



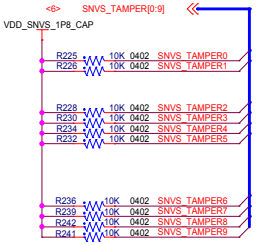
BOOT_SEL

	Boot Sel	R319	R320	R323	R321
SD	H	0R	NC	0R	NC
EMMC	L	0R	NC	0R	NC

Boot Config

	SD	EMMC	Nand
BT_CFG4	1	0	0
BT_CFG5	0	1	1
BT_CFG6	0	1	1
BT_CFG11	0	1	0
BT_CFG12	1	0	1
BT_CFG13	0	1	1

TAMPER



BOOT TABLE

1	2	3	4	5	6	7	8
BT_CFG[14]	BT_CFG[13]	BT_CFG[12]	BT_CFG[11]	BT_CFG[10]	BT_CFG[6]	BT_CFG[5]	BT_CFG[4]
001 = SD/eSD Boot			Port Select: 00 – eSDHC1 01 – eSDHC2 10 – eSDHC3		0	0	Bus Width: 0 – 1-bit 1 – 4-bit
010 = MMC/eMMC Boot					Bus Width: 000 – 1-bit 001 – 4-bit 010 – 8-bit 101 – 4-bit DDR (MMC 4.4) 110 – 8-bit DDR (MMC 4.4)		
011 = NAND Boot			Pages In Block: 00 – 128 01 – 64 10 – 32 11 – 256		BOOT_SEARCH_COUNT: 00 – 2 01 – 2 10 – 4 11 – 8		0
100 = QSPI Boot			0	0	0	0	0

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ICAP Classification: FCP: ___ FIUO: ___ PUBI: X

Drawing Title: MCIMX7D-SABRE

Page Title: 18 Boot Config/Tamper

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