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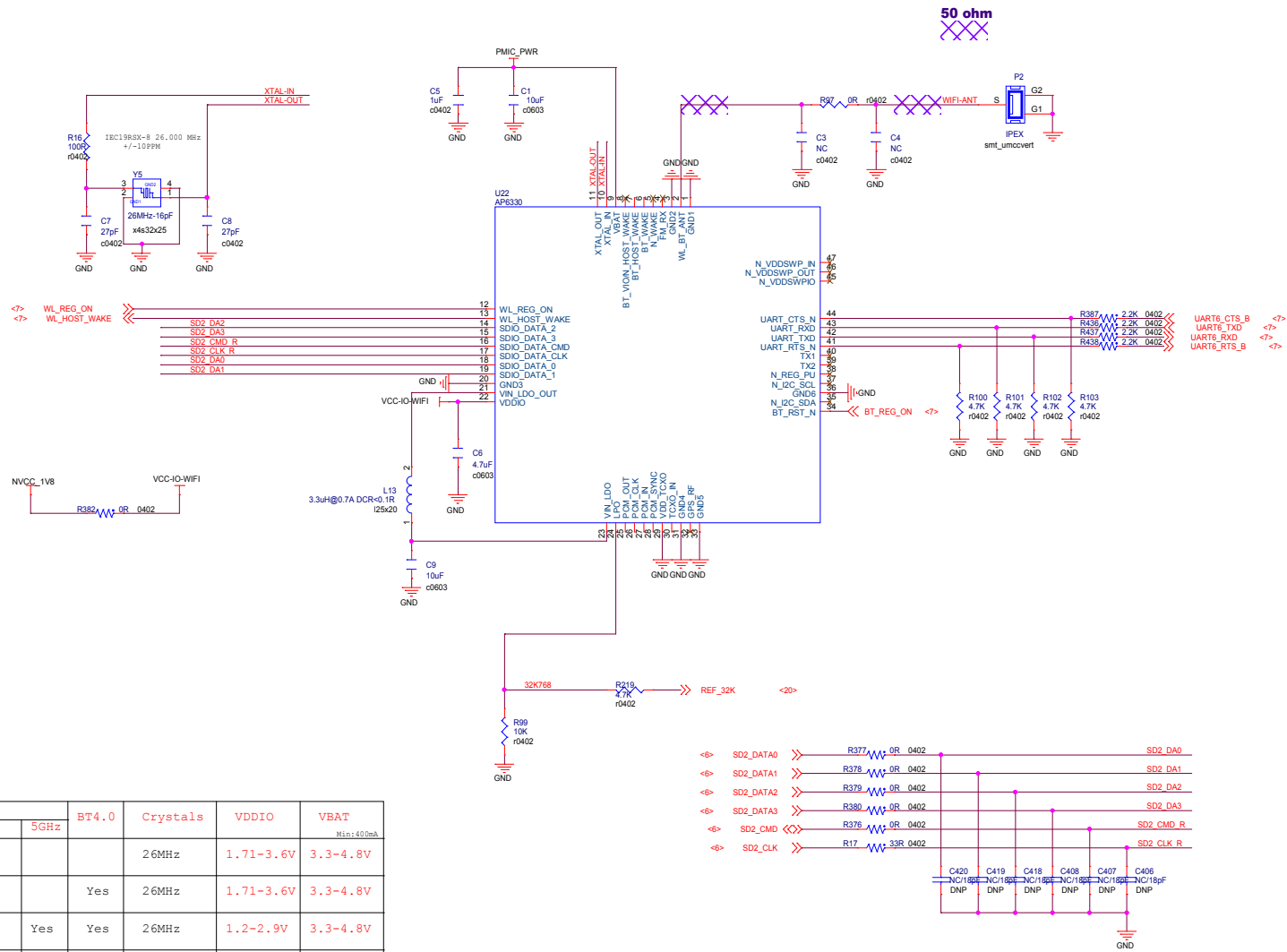
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# MCIMX7D-SABRE

**Revision History**

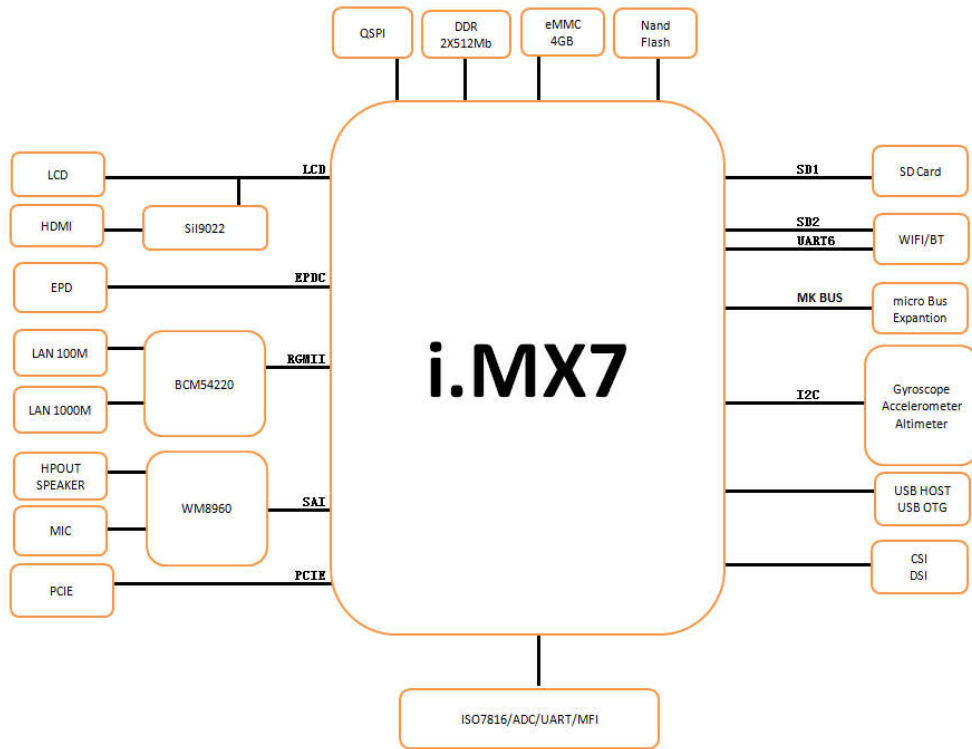
Rev. Code	Date	Description
B	22/09/2015	Initial Draft
B1	21/01/2016	<ul style="list-style-type: none"> <li>- Changed Q8 from 2N7002 to MMBT3904.</li> <li>- Reconnection U43 SW with the anode of D25.</li> <li>- DNP the capacitor:C6,C121.</li> <li>- Changed the power of JTAG from PERI_3V3 to VLDO3_3V3.</li> <li>- PCIE                             <ul style="list-style-type: none"> <li>DNP the resistor:R605,R606,R607,R608.</li> <li>Changed C442 and C443 to 0ohm resistor (R632,R633).</li> <li>Add 49.9 1% 0402 resistors (R634,R635) on PCIE_REFCLKOUT_P/N to GND.</li> <li>Add the mosfet Q36 on the NET "CSI_FWDM".</li> <li>Add blocking capacitor(C458,C459) Before the terminal resistor.</li> <li>Add Schottky diode(D26) to isolate POR_B with JTAG interface.</li> <li>Use the LDO U44 instead of Q11.</li> <li>Add the 0ohm resistor(R641) connect the pin CCM_CLK2 to GND.</li> <li>Add the U45 to match electrical level.</li> </ul> </li> </ul>
C	28/01/2016	<ul style="list-style-type: none"> <li>- Changed the revision from "B1" to "C".</li> <li>- Delete the capacitors C312 and C314.</li> <li>- Add several GND test points TP68--TP75 around the DDR3.</li> <li>- Changed connectors type of the J29&amp;J30</li> </ul>
D	09/03/2016	<ul style="list-style-type: none"> <li>- Changed the revision from "C" to "D".</li> <li>- Corrected the PCB decal of the Q8.</li> <li>- Changed connection of the J20.</li> </ul>

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Designer:		Page Classification: ECP FUD FUBI	
Design Title:		<b>MCIMX7D-SABRE</b>	
Drawn by:		<b>01 Title Sheet</b>	
Approved: <Approver>		Size: A2	Document Number: SOURCE: SCH-28590-SPF-28590
Date: Thursday, June 28, 2017		Rev D Sheet 1 of 23	

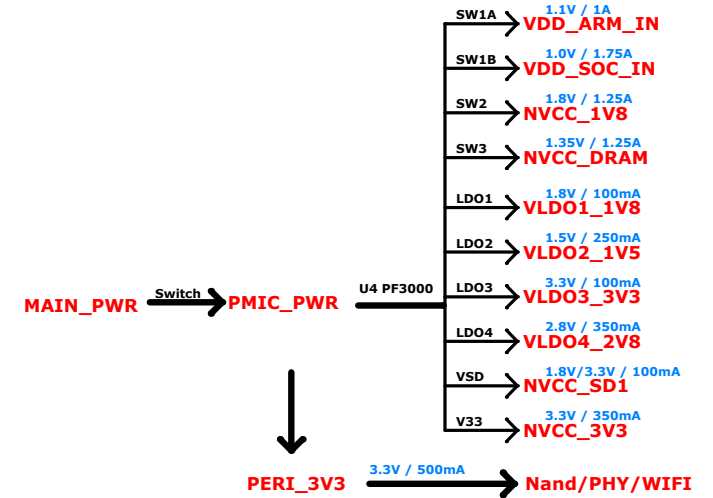


OPTION	WIFI				BT4.0	Crystals	VDDIO	VBAT Min=400mA
	a	b/g/n	ac	5Ghz				
AP6181		Yes				26MHz	1.71-3.6V	3.3-4.8V
AP6212		Yes			Yes	26MHz	1.71-3.6V	3.3-4.8V
AP6330	Yes	Yes		Yes	Yes	26MHz	1.2-2.9V	3.3-4.8V

# MCIMX7D-SABRE Block Diagram



# Power Distribution Diagram



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ICAP Classification: FCP: \_\_\_\_\_ FILO: \_\_\_\_\_ PUB: X

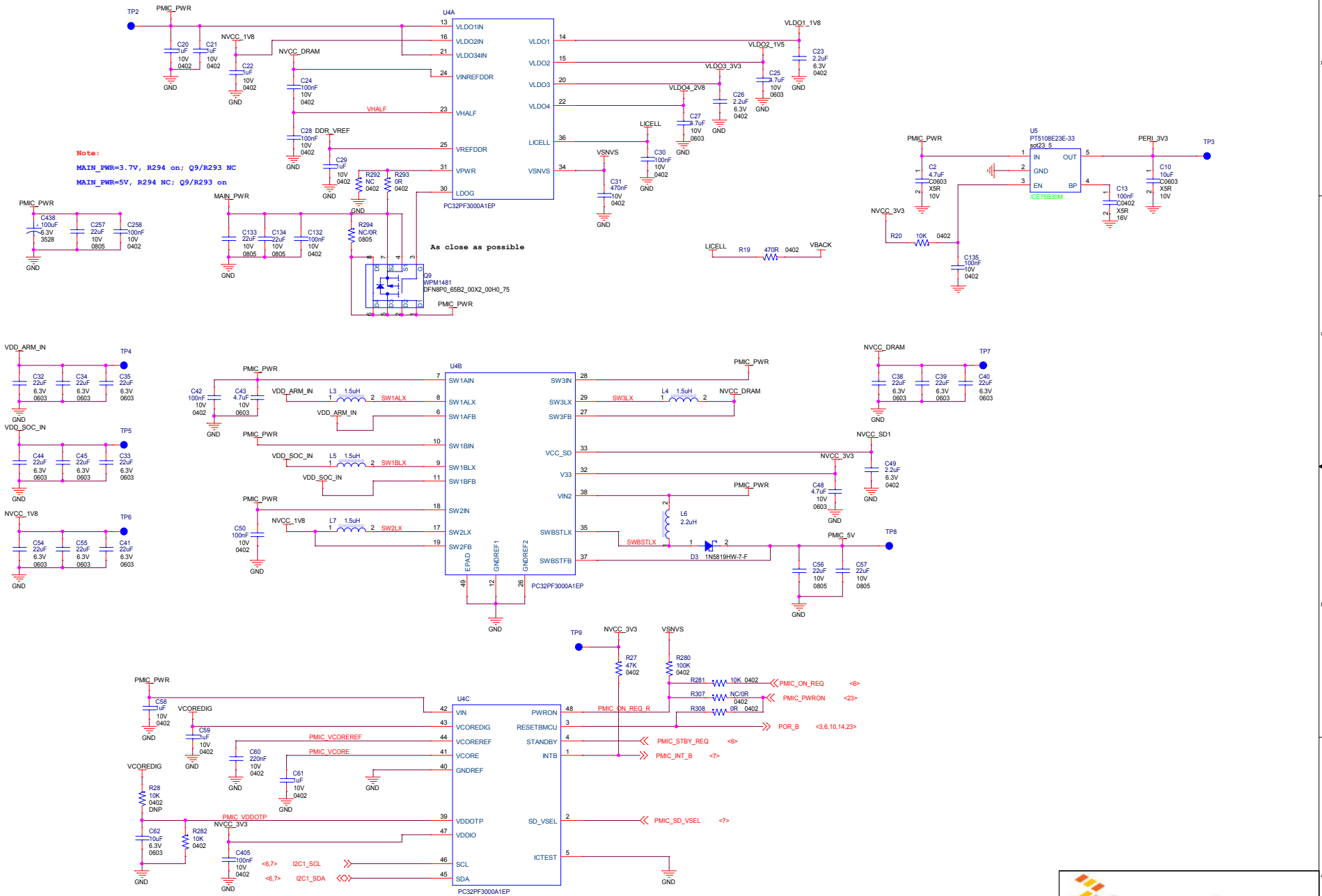
Drawing Title: **MCIMX7D-SABRE**

Page Title: **02 Block Diagram**

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Date: Thursday, June 29, 2017 | Sheet 2 of 23

# PMIC

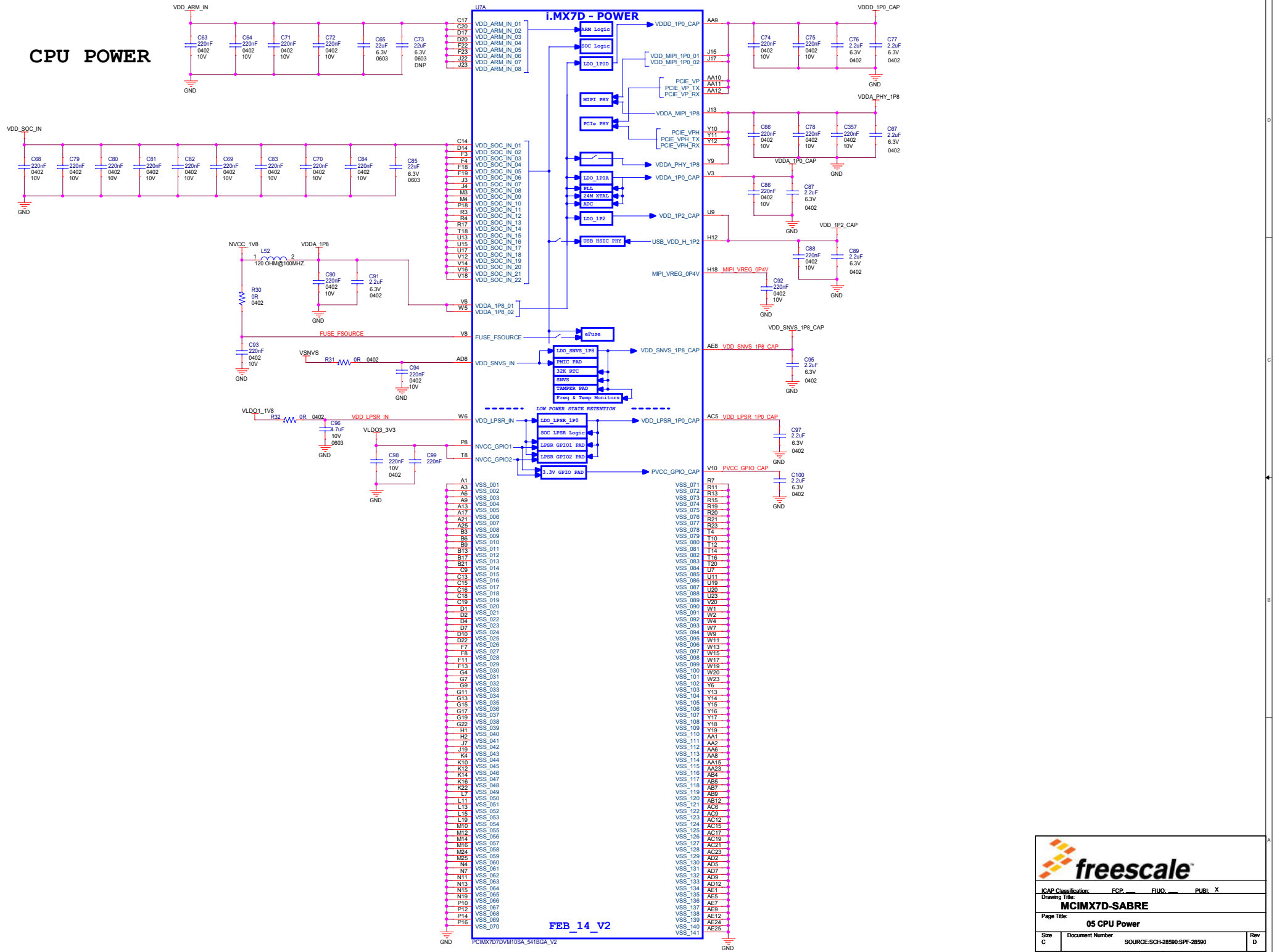


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 Page Title: **04 PMIC**

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# CPU POWER

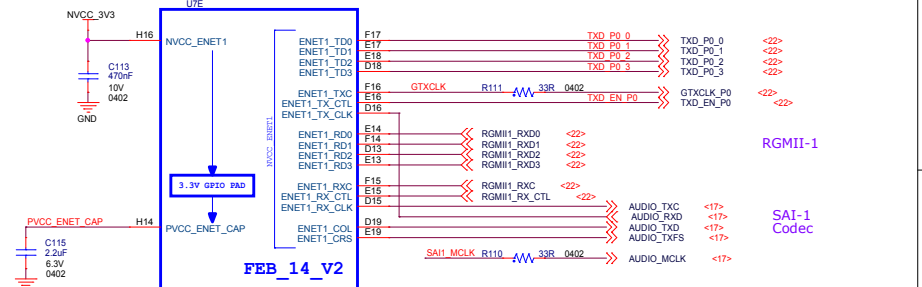
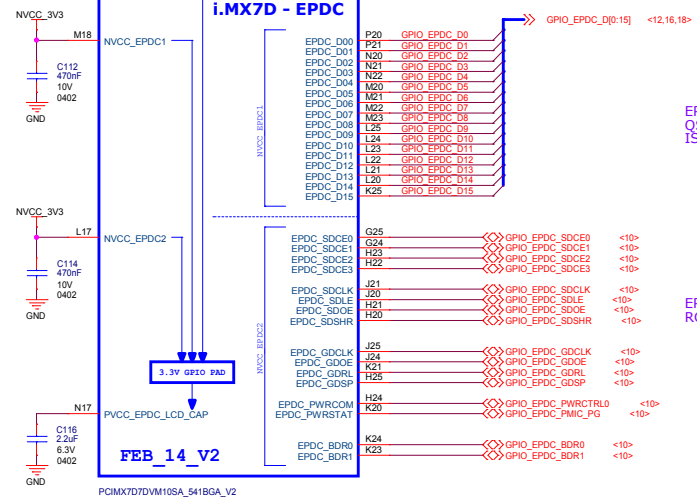
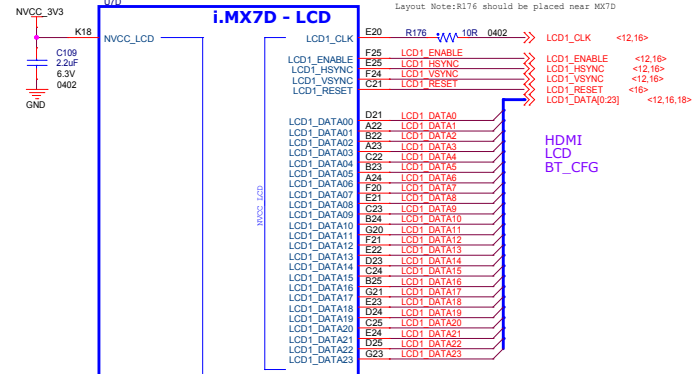
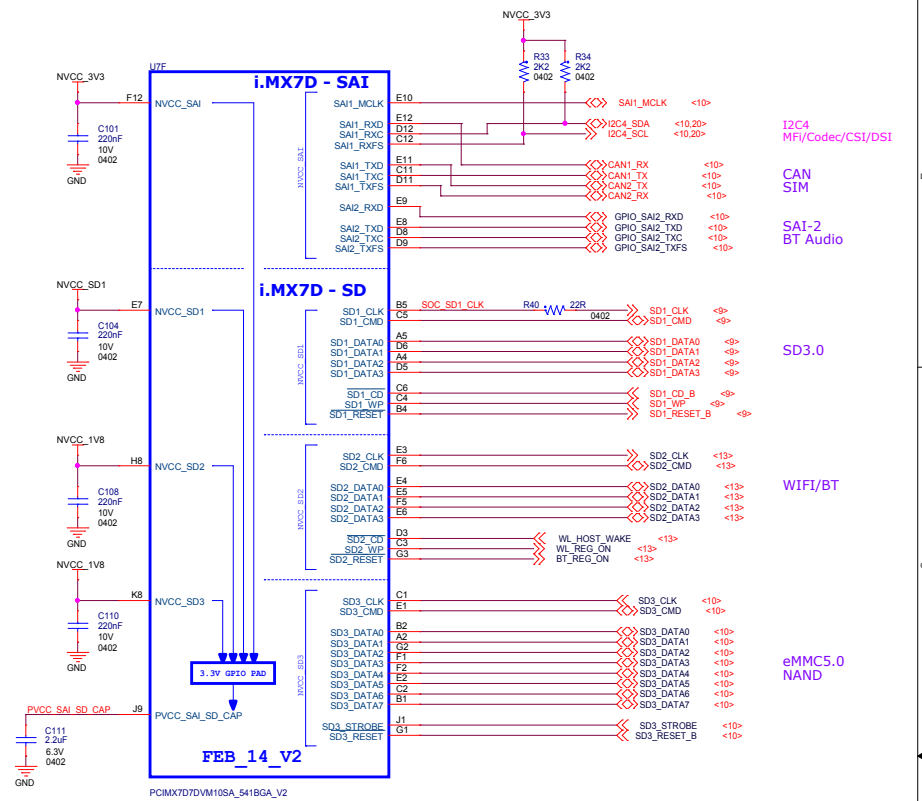
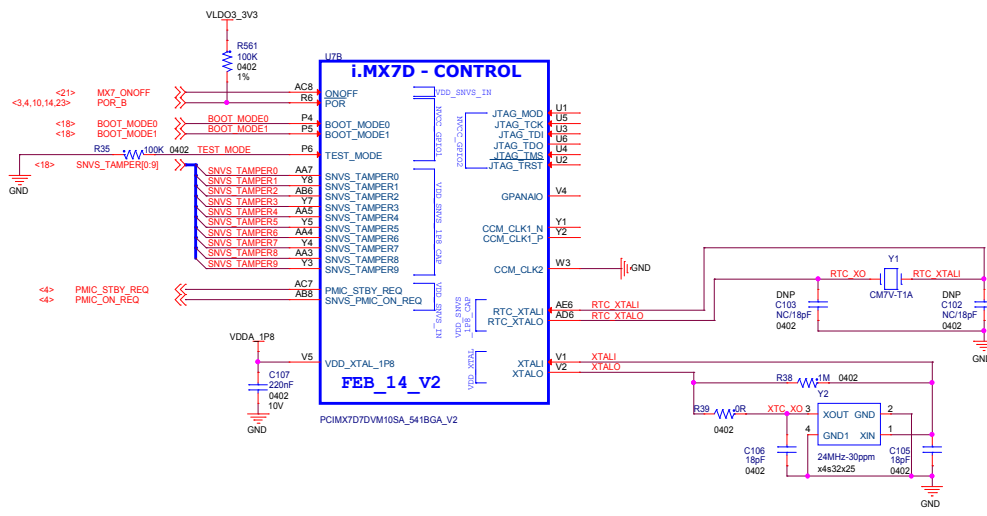


FEB 14 V2

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ICAP Classification: FCP: FLUO: PUBI: X  
Drawing Title: **MCIMX7D-SABRE**  
Page Title: **05 CPU Power**

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I2C4  
MFI/Codec/CSI/DSI

CAN  
SIM

SAI-2  
BT Audio

SD3.0

WiFi/BT

eMMC5.0  
NAND

**freescale**

ICAP Classification: FCP, FIUO, PUBI: X

Drawing Title: **MCIMX7D-SABRE**

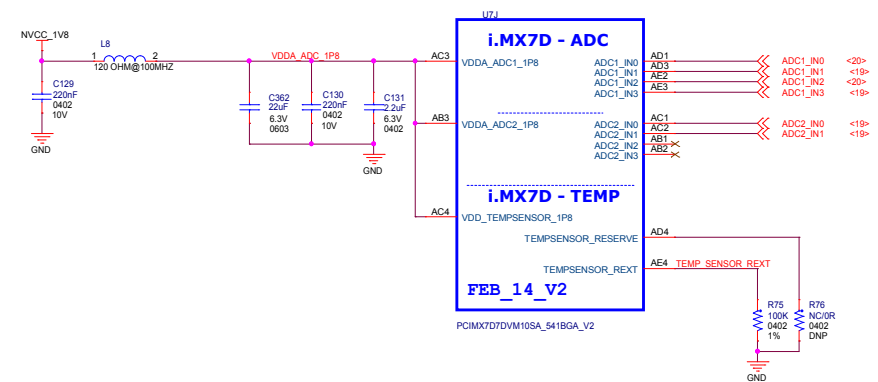
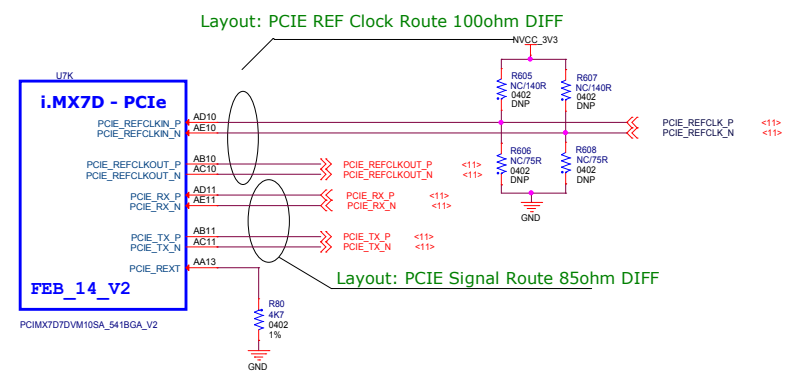
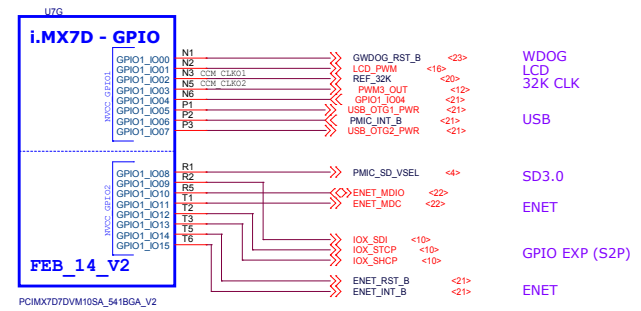
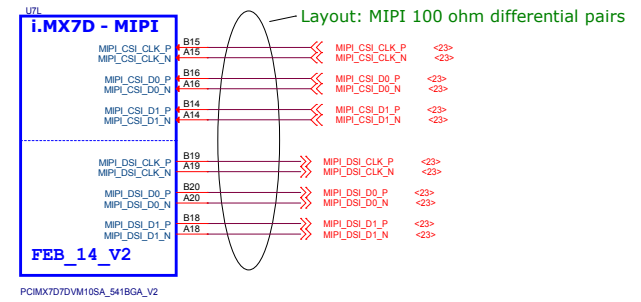
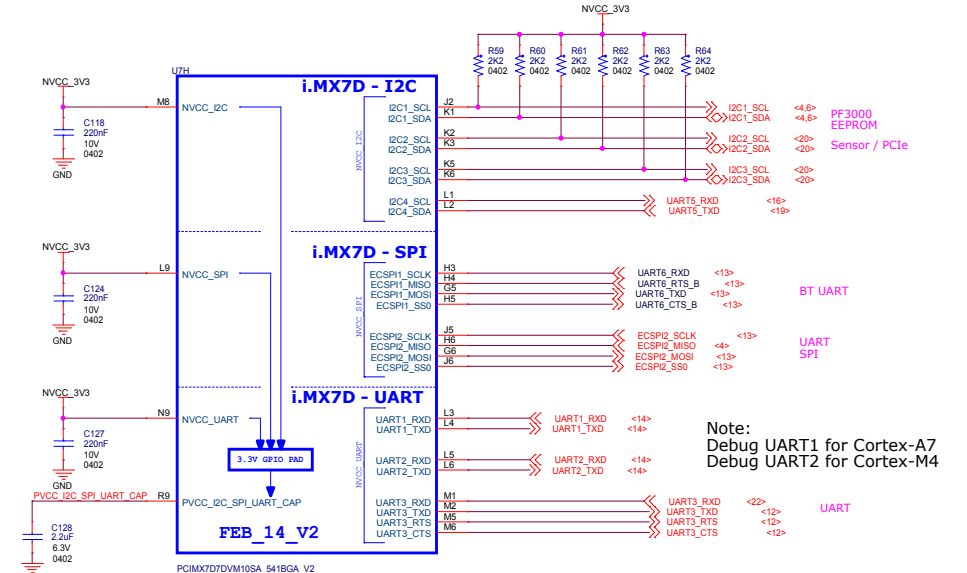
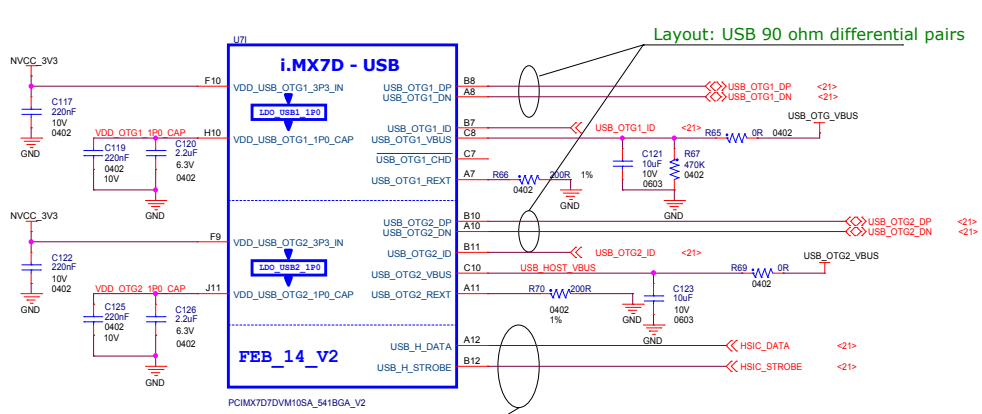
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Size: C

Document Number: SOURCE:SCH-28590:SPF-28590

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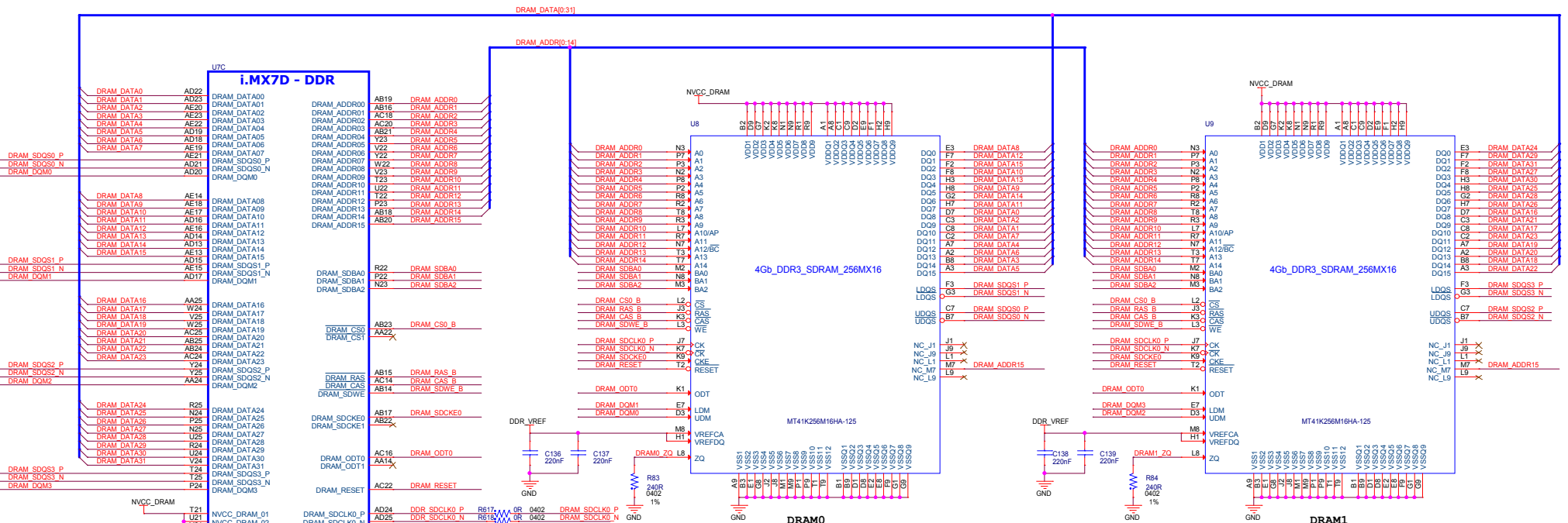
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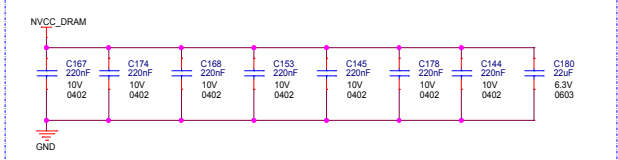
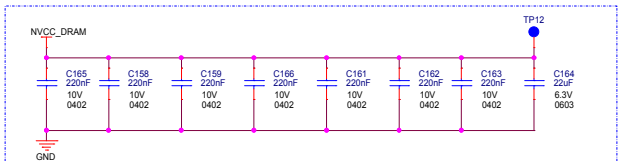
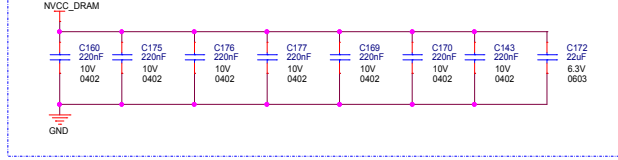
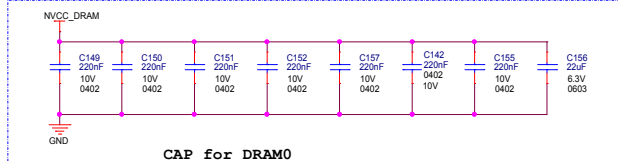
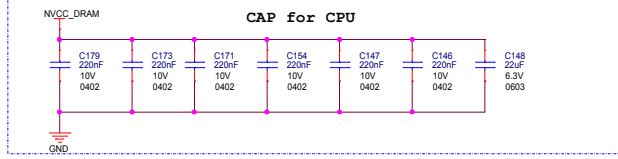
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# DDR



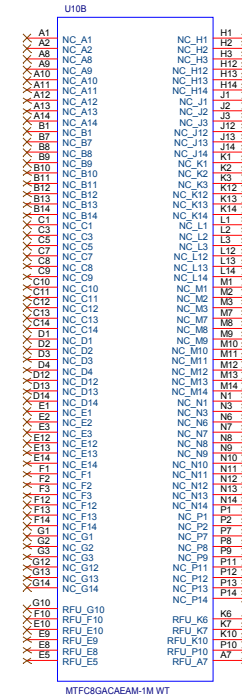
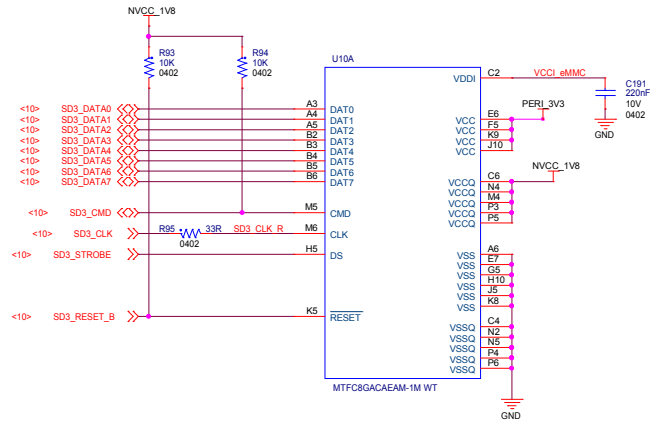
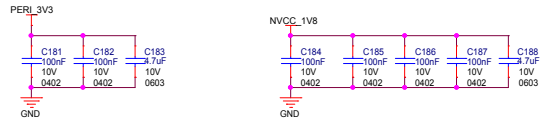
Clock terminators: Place termination resistor on each of the chip of CLK signals



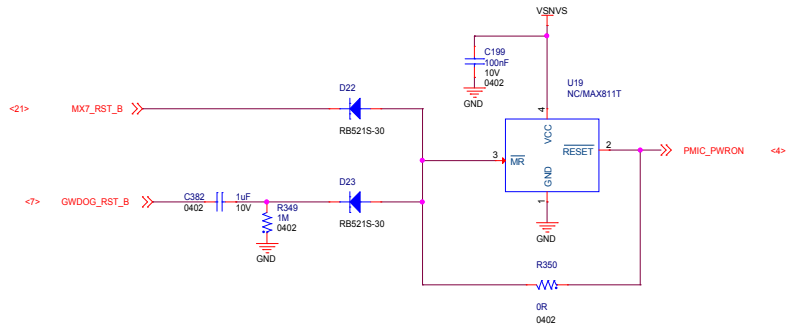
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**Page Title:** **08 DDR3 Memory**  
**Size C** | **Document Number** SOURCE: SCH-28590-SPF-28590 | **Rev D**  
**Date:** Thursday, June 29, 2017 | **Sheet 8 of 23**



# eMMC 5.0

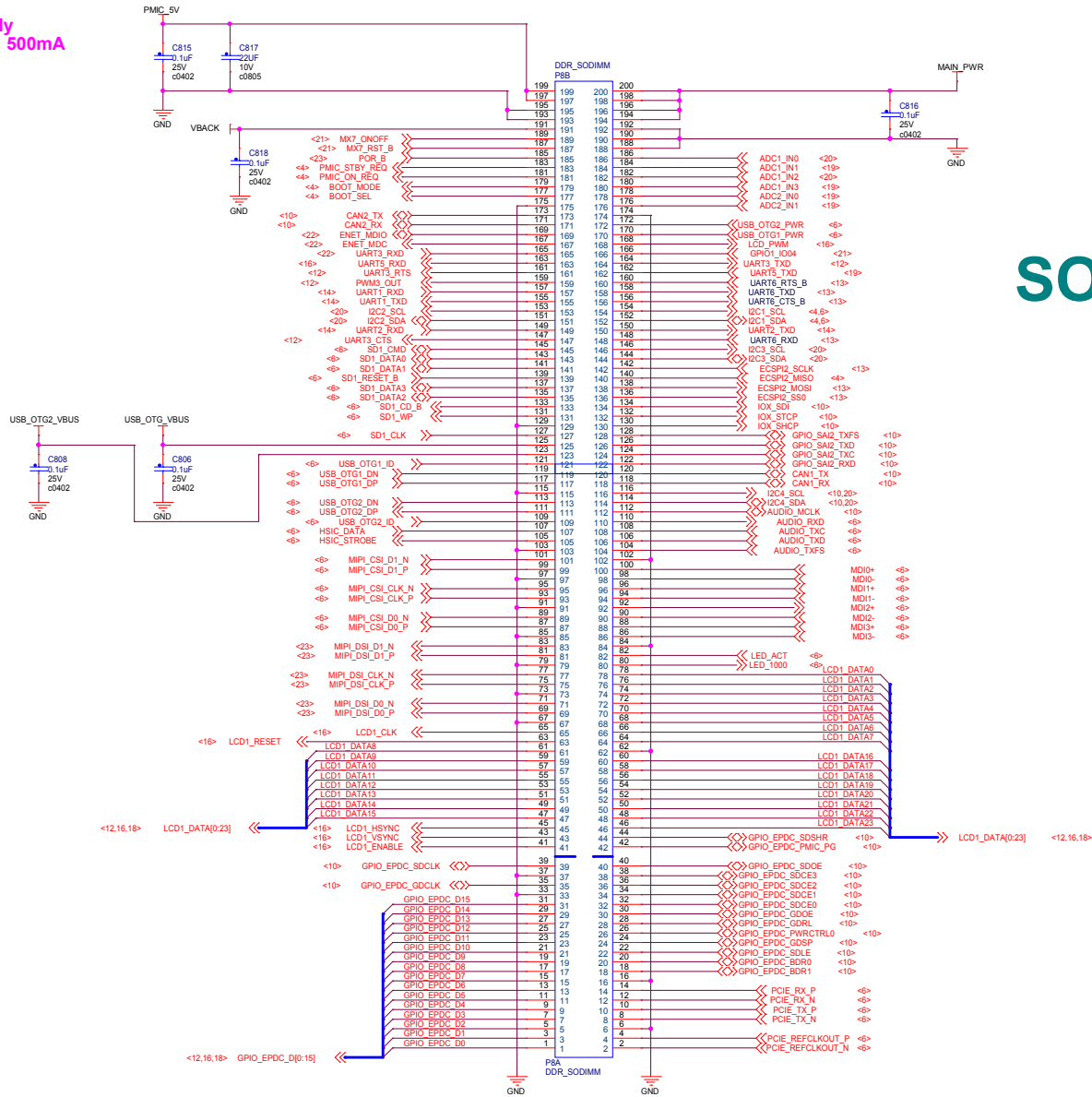


# WATCH DOG



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 Drawing Title: **MCIMX7D-SABRE**  
 Page Title: **09 eMMC/NAND/QSPI/SD**  
 Size C Document Number SOURCE: SCH-28590:SPF-28590 Rev D  
 Date: Wednesday, July 12 2017 Sheet 8 of 23

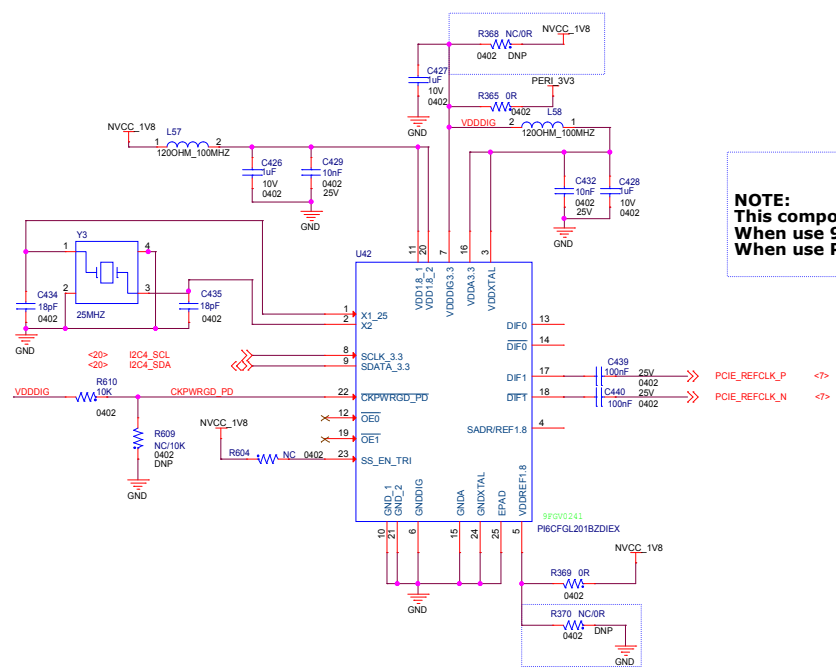
# Maxim PMIC 5v supply  
current for Base Board: 500mA



# SODIMM 200

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Designer: DESIGNER	Drawing Title: <b>MCIMX6UL-CM</b>	ICAP Classification: FCP	FIUC: X PUBL
Drawn by: DRAWN_BY	Page Title: <b>CPU-SODIMM200</b>		
Approved: APPROVER	Size C	Document Number SCH-28617 PDF: SPF-28617	Rev C1
Date: Wednesday, July 12, 2017		Sheet 11 of 13	

# PCI-E CLK Generator

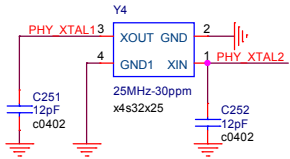


**NOTE:**  
 This component share PCB package  
 When use 9FGV0241 populate R368 & R370, de-populate R365 & R369.  
 When use PI6CFG201BZDIEX populate R365 & R369, de-populate R368 & R370 (default).

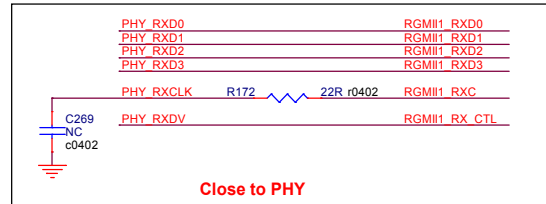
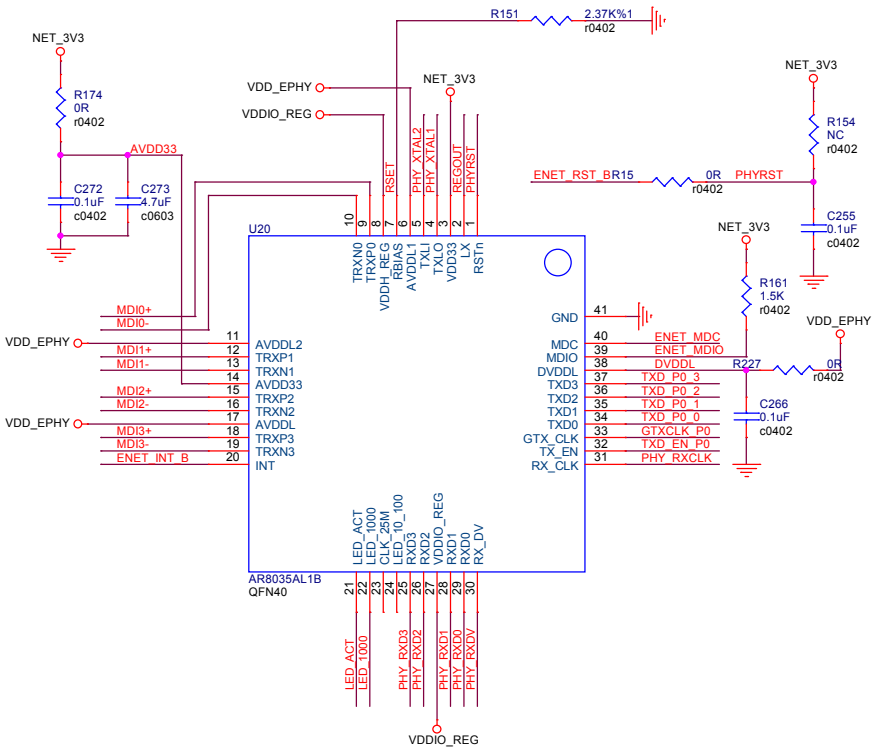
TXD\_P0\_0 <<22>> TXD\_P0\_0  
 TXD\_P0\_1 <<22>> TXD\_P0\_1  
 TXD\_P0\_2 <<22>> TXD\_P0\_2  
 TXD\_P0\_3 <<22>> TXD\_P0\_3  
 GTXCLK\_P0 <<22>> GTXCLK\_P0  
 TXD\_EN\_P0 <<22>> TXD\_EN\_P0

RGMII1\_RXD0 16  
 RGMII1\_RXD1 16  
 RGMII1\_RXD2 16  
 RGMII1\_RXD3 16  
 RGMII1\_RX\_CTL 16  
 RGMII1\_RXC 16

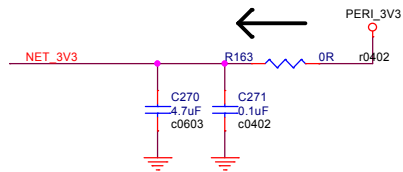
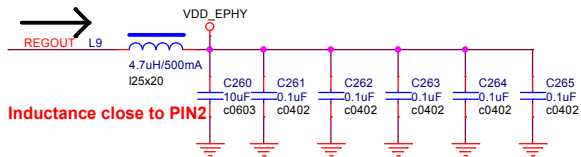
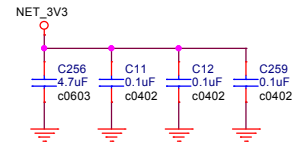
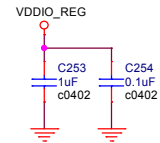
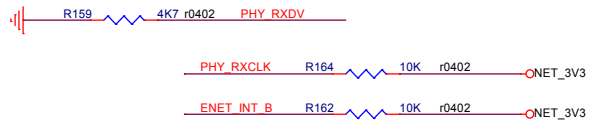
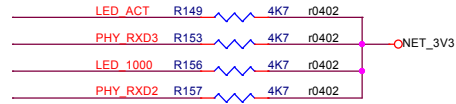
ENET\_RST\_B 16  
 ENET\_INT\_B 11  
 ENET\_MDC 16  
 ENET\_MDIO 16



MDI3+ >>MDI3+ 16  
 MDI3- >>MDI3- 16  
 MDI1+ >>MDI1+ 16  
 MDI1- >>MDI1- 16  
 MDI2+ >>MDI2+ 16  
 MDI2- >>MDI2- 16  
 MDI0+ >>MDI0+ 16  
 MDI0- >>MDI0- 16  
 LED\_ACT >>LED\_ACT 16  
 LED\_1000 >>LED\_1000 16



**PHY Address=000**

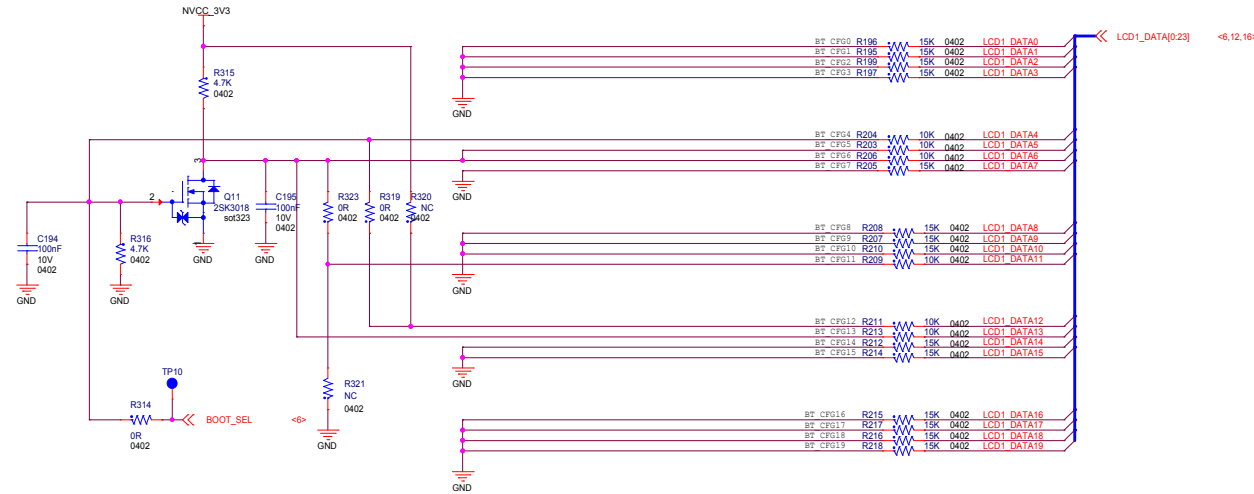
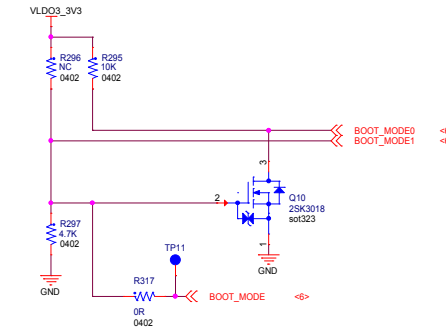


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<b>Boardcon Inc</b>		Room702-710, XinAn Business Building, 45Zone, BaoAn District, Shenzhen China +86-755-27571591	
Title: <b>10/100/1000M-PHY</b>			
Size: A3	Document Number: <b>CMX7D</b>	Drawn: <b>Dawen</b>	Rev: <b>2</b>
Date: Wednesday, July 12, 2017	Sheet 17 of 17		

# BOOT MODE

BOOT_MODE	[1]	[0]
FUSES	0	0
<b>Serial Downloader</b>	<b>0</b>	<b>1</b>
INTERNAL BOOT	1	0
TEST MODE	1	1



BOOT\_SEL

	Boot Sel	R319	R320	R323	R321
SD	L	0R	NC	0R	NC
<b>EMMC</b>	<b>H</b>	<b>0R</b>	<b>NC</b>	<b>0R</b>	<b>NC</b>
Nand	H	NC	0R	NC	0R

## Boot Config

	SD	EMMC	Nand
BT_CFG4	1	0	0
BT_CFG5	0	1	1
BT_CFG6	0	1	1
BT_CFG11	0	1	0
BT_CFG12	1	0	1
BT_CFG13	0	1	1

## BOOT TABLE

1	2	3	4	5	6	7	8
BT_CFG[14]	BT_CFG[13]	BT_CFG[12]	BT_CFG[11]	BT_CFG[10]	BT_CFG[6]	BT_CFG[5]	BT_CFG[4]
001 = SD/eSD Boot					0	0	<b>Bus Width:</b> 0 - 1-bit 1 - 4-bit
010 = MMC/eMMC Boot			<b>Port Select:</b> 00 - eSDHC1 01 - eSDHC2 10 - eSDHC3		<b>Bus Width:</b> 000 - 1-bit 001 - 4-bit 010 - 8-bit 101 - 4-bit DDR (MMC 4.4) 110 - 8-bit DDR (MMC 4.4)		
011 = NAND Boot			<b>Pages In Block:</b> 00 - 128 01 - 64 10 - 32 11 - 256		<b>BOOT_SEARCH_COUNT:</b> 00 - 2 01 - 2 10 - 4 11 - 8		0
100 = QSPI Boot			0	0	0	0	0

## TAMPER

