MCIMX6SX SDB

Table of Content

Revision History

Rev. Code	Date	Description
A	2013/12/10	First Release
A1	2014/04/23	1. On P.10, change description from "2 x 256Mbit QSPI FLASH" to "2 x 128Mbit QSPI FLASH". 2. Change the Agile P/N of U23 & U24 to 312-80902 as 315-76544 is obsolete. 3. Change R40 (DNP by default) from 10R to 0R. 4. Rev.A Board with TDA4952: - MBRA340T3G is added (by hand soldering) between VDD_SOC_IN and VDD_SOC_CAP as the workaround of a TO1.0 silicon bug. - R100 is removed and a wire is hand-soldered to connect SW2_3V0 to U29 VIN2 (Pin 27). - C228 is changed to 0.22uF. - D19 & R229 are removed. R230 is populated. Hand-soldered a wire to connect JTAG_nSRST to POR_B. Hand-soldered a wire to connect RESET button to PMIC_PWRON.
B	2014/08/28	1. Change L24 to VLP6045LT-1R0N for better power rating margin. 2. Change C176 & C177 to 47uF/0805 to improve DCDC input routing in layout. 3. Change U29 from PF0100A to PF0200, and the corresponding circuits - a) Change L26 to higher power rating inductor, NRS5030T1R0NMGJV, to supply VDD_ARM_IN & VDD_SOC_IN thru the SW1AB output. b) Change C190 from DNP to POP. c) Change C195, L30, C205, C206, R374 to DNP. d) Change R91 to DNP and R200 to POP. e) Connect i.MX6SX VDD_ARM_IN & VDD_SOC_IN pins to VDD_ARM_SOC_IN (SW1AB output). f) Change R350 to DNP and R98 to POP to supply Audio Codec (U13) by VGEN4_1V8. 4. ENGR00299970 - Change C228 to 0.22uF. 5. ENGR00299968 - Change the supply to R100 (VIN2) from SYS_3V8 to SW2_3V3. 6. ENGR00321431 - a) Add D26, R446 & C363 to compensate the weak output drive from i.MX6SX PMIC_ON_REQ. b) Add C365 for ESD purpose. 7. Add R314 to limit current to/from coin cell. 8. Change Y1 to 230-77452 (24MHz xtal used on i.MX6SL EVK). 9. Add 0.01uF/0402 (C361,C362) on NVCC_RGMII1/2. 10. Change eMMC footprint (U4, DNP) to MTFC8GLCDM. 11. Add R463 (DNP) and R464 (DNP) for testing purpose. 12. Change U7 and U9 to N25Q256A13EF840 and add 10k pull-up (R347 & R348) on QSPI2A_SS0_B and QSPI2B_SS0_B. 13. Change L1 and L2 to 470ohm@100MHz ferrite bead. 14. Change ESD diode for USBHOST_DP/N and USBOTG1_DP/N to ESD7C3.3DT5G, and change ESD diode on USBOTG1_ID to ESD5B5.0ST1G. 15. Change Audio Codec (U13) from WM8962 to WM8962BECSN/R. 16. ENGR00301123 - Change Camera connector footprint to CON_BBC_40P_0P4_SM_MIRROR, and correct LCD1_DATA[8..17] mapping to CSI_D[0..9]. 17. Add L38 and L39 (470ohm@100MHz) close to LVDS connector (J12) to improve EMC performance. 18. Change U15 & U17 to MC34901WEF and the corresponding circuit. 19. Change L14, L17, L36 & L37 to 470ohm@100MHz ferrite bead to improve EMC performance. 20. ENGR00322416 - Change R179 & R180 to 56R and add 470 ohm pull-up (R442 & R443) on PCIE_CREFCLKP/M to change to HCSL DC offset. 21. Add external PCIe CLK generator and corresponding circuit (DNP by default) for GEN2 clock jitter test. 22. ENGR00302230 - i) Connect RESET button (thru D19) to PMIC_PWRON by default ii) Set D18 to POP. iii) Add R444 to connect JTAG_nSRST to POR_B. iv) Change R82 to 100R and C174 to 1000pF. 23. Remove J21 and the corresponding circuit. 24. Change the pull-up voltage of BOOT_MODE0/1 to VSNVS_3V0 (thru R233 and R234). 25. Change C335 & C336 to 30pF/0402 (DNP by default).
B1	2014/11/20	1. TDA5159 for power reset the whole system (including QSPI) by SW control: i) D18 is DNP. ii) Change the capacitor on C174 to 1Mohm/0402. iii) Hand solder C380 (1.0uF/X5R) Pin 2 to D18 Pin C. iv) Hand solder C380 Pin 1 to R82 Pin 2. 2. Change L26 to LTF5022T-1R2N4R2-LC (180-78310) to improve the magnetic shielding. PF0200 SW1AB is sensitive to magnetic field when operating at PFM mode. 3. Change D27 & D28 to ESD7C5.0DT5G (480-78836). 4. Change R60 from 10k to 100k to reduce the USB unconfigured current. 5. Change J18 to DNP. 6. Change P1 from WM-64PCT (510-77873) to POM-2244P-C3310-2-R (510-77976), as WM-64PCT is obsolete. 7. Change U5 (default DNP) from NC7SZ08P5 to NC7SZ08P5X, as NC7SZ08P5 is obsolete.
C	2014/12/18	1. U41 and its related circuit are added for two purposes (see P.20) - i) Fix the SW reboot issue by togling WDOG_B to issue power reset (ENGR00338067). ii) Delay the PMIC_PWRON >500ms for the 1st-time power-on (VSNVS_3V0 is first applied), to ensure 32.768kHz xtal osc output is stable. 2. U42 and its related circuit are added for future USB OTG Certification Test (see P.11). All those components are DNP by default. 3. Remove J18, set D26, R446 & R316 to DNP, as the PMIC_ON_REQ weak output drive strength issue is fixed in TO1.2.

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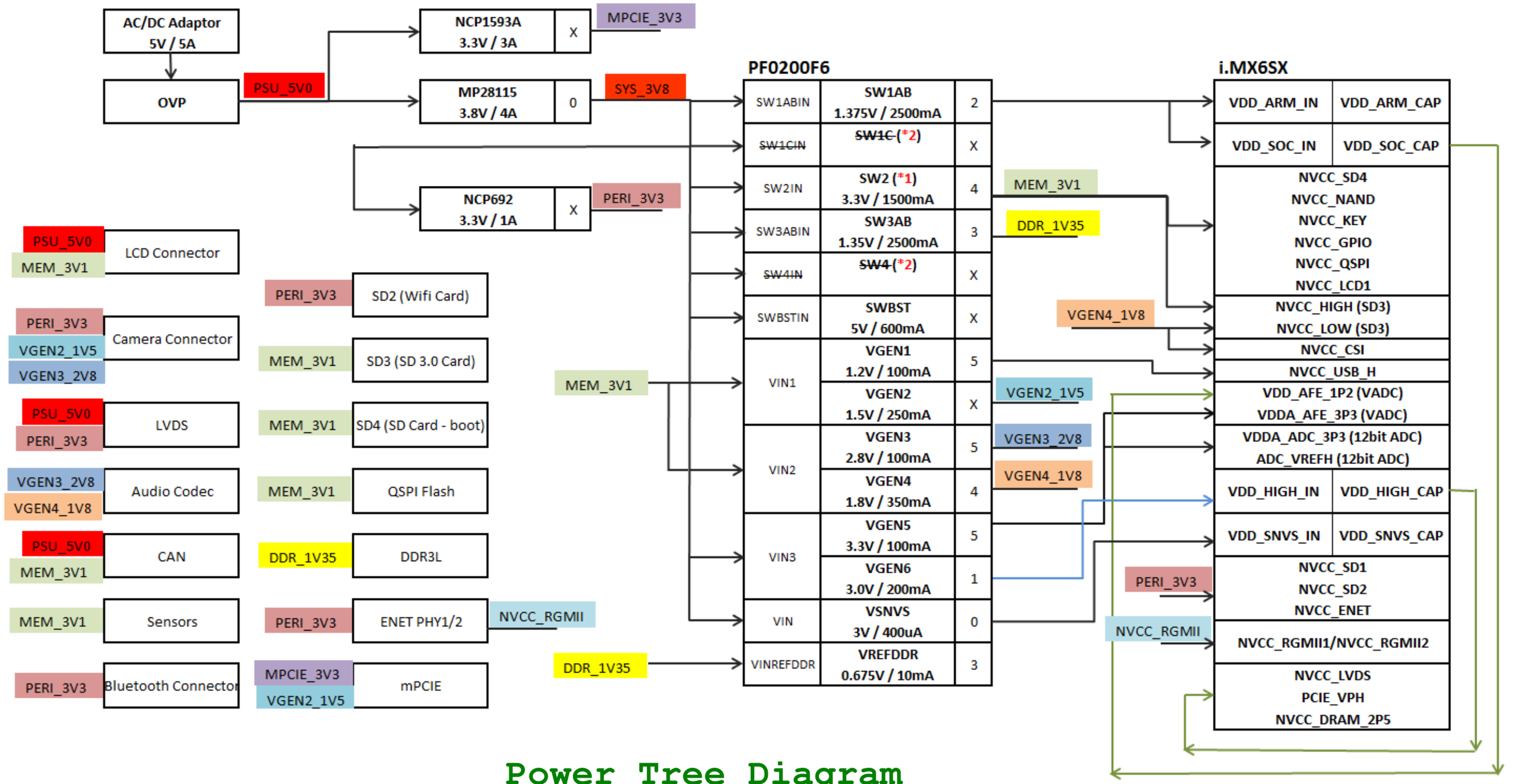
Microcontroller Solutions Group
6501 William Cannon Drive West
Austin, TX 78735-8598

ICAP Classification: FCP: FIUO: X PUB:

Designer: RAYMOND CHOI	Drawing Title: MCIMX6SX SDB		
Drawn by: RAYMOND CHOI	Page Title: Title and Rev History		
Approved: APPROVER	Size: D	Document Number: SCH-27962 PDF: SPF-27962	Rev: C
	Date: Thursday, December 18, 2014	Sheet 1 of 22	



Power Tree Diagram

Legend:

SW1AB 1.375V / 2500mA	2

Power-up Sequence

0 – Always On
1 – First start-up supply rail
X – Default Off

Note:
(*1) – SW2 of PF0200 can be changed to 3.1V after boot-up (by SW) to lower power consumption
(*2) – No SW1C and SW4 in PF0200.

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Drawing Title: **MCIMX6SX SDB**

Page Title: **Power Tree Diagram**

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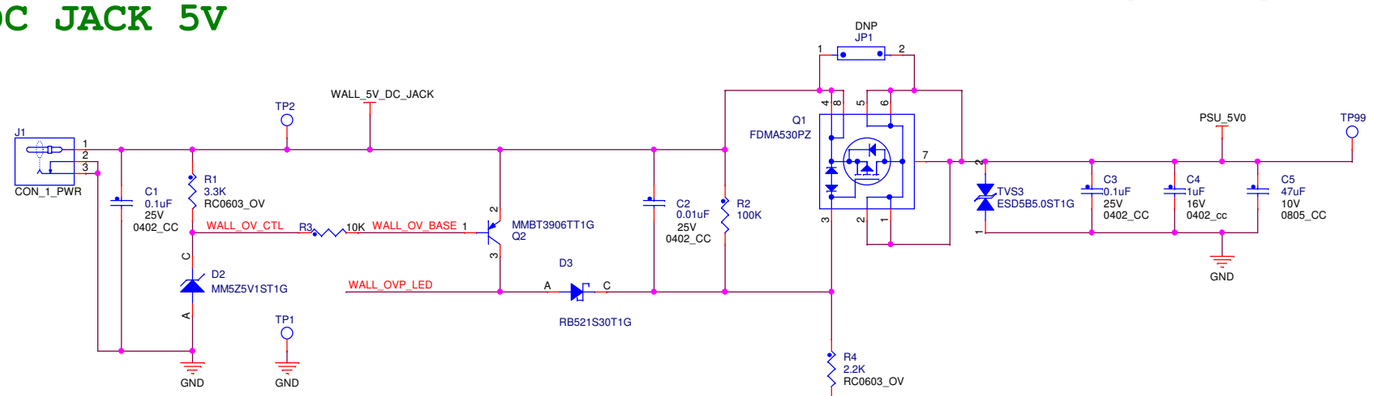
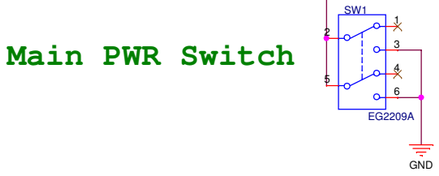
DC JACK 5V



Over Voltage Protection

Note:
Over-voltage protection is designed to protect up to +20V.

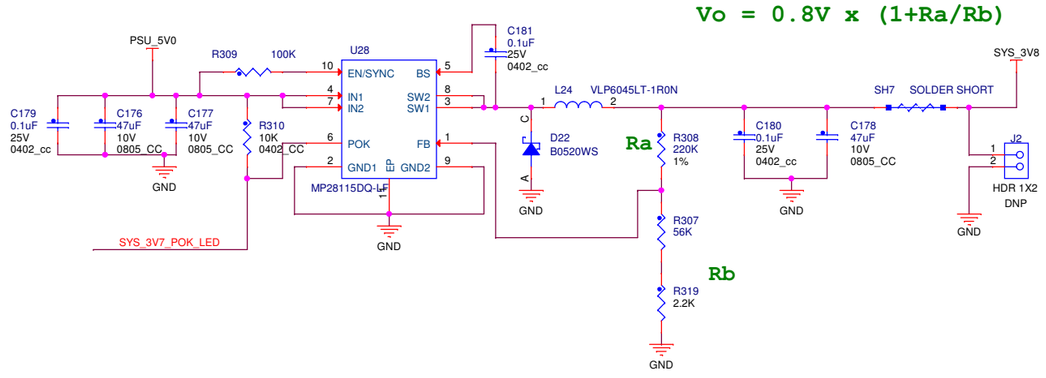
Main PWR Switch



Step-down DCDC for PF0200 Input

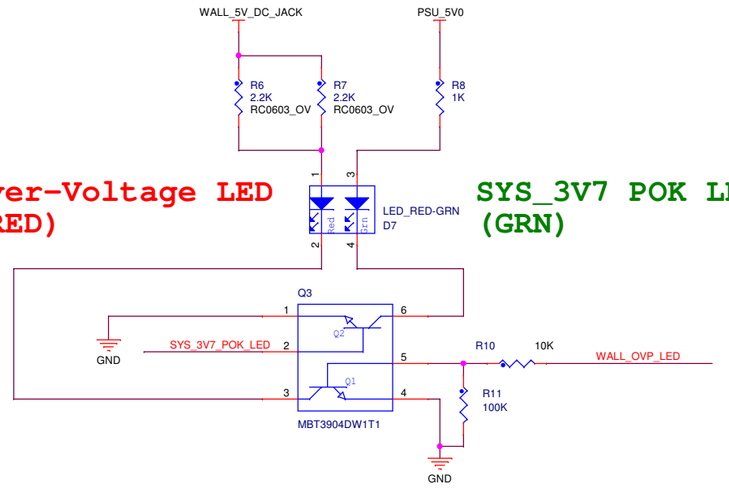
Max output current from MP28115 is 4A

Vo = 0.8V x (1+Ra/Rb)



Over-Voltage LED (RED)

SYS_3V7 POK LED (GRN)



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Drawing Title: **MCIMX6SX SDB**

Page Title: **Main Power**

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1.0uH is recommended for PF0200 SW1AB.

Note:
This block is reserved for backward compatible for PF0100A testing.

SW Note:
Default power-up voltage of SW2_3V3 is 3.3V.
Need to change it to 3.1V after boot-up to lower power consumption.

Capacitors reserved for EMC purpose

LDO decouples are 4.7 uF for BOM consolidation.

Max output current from NCP692 is 1A

Note:
This block is used to compensate the weak output drive of PMIC_ON_REQ in TO1.0. TO1.2 or later does not need this.

PMIC-ON LED

ICAP Classification:	FCP:___	FIUO: X	PUBI:___
Drawing Title:	MCIMX6SX SDB		
Page Title:	System PMIC		
Size: C	Document Number: SCH-27962 PDF: SPF-27962		Rev: C
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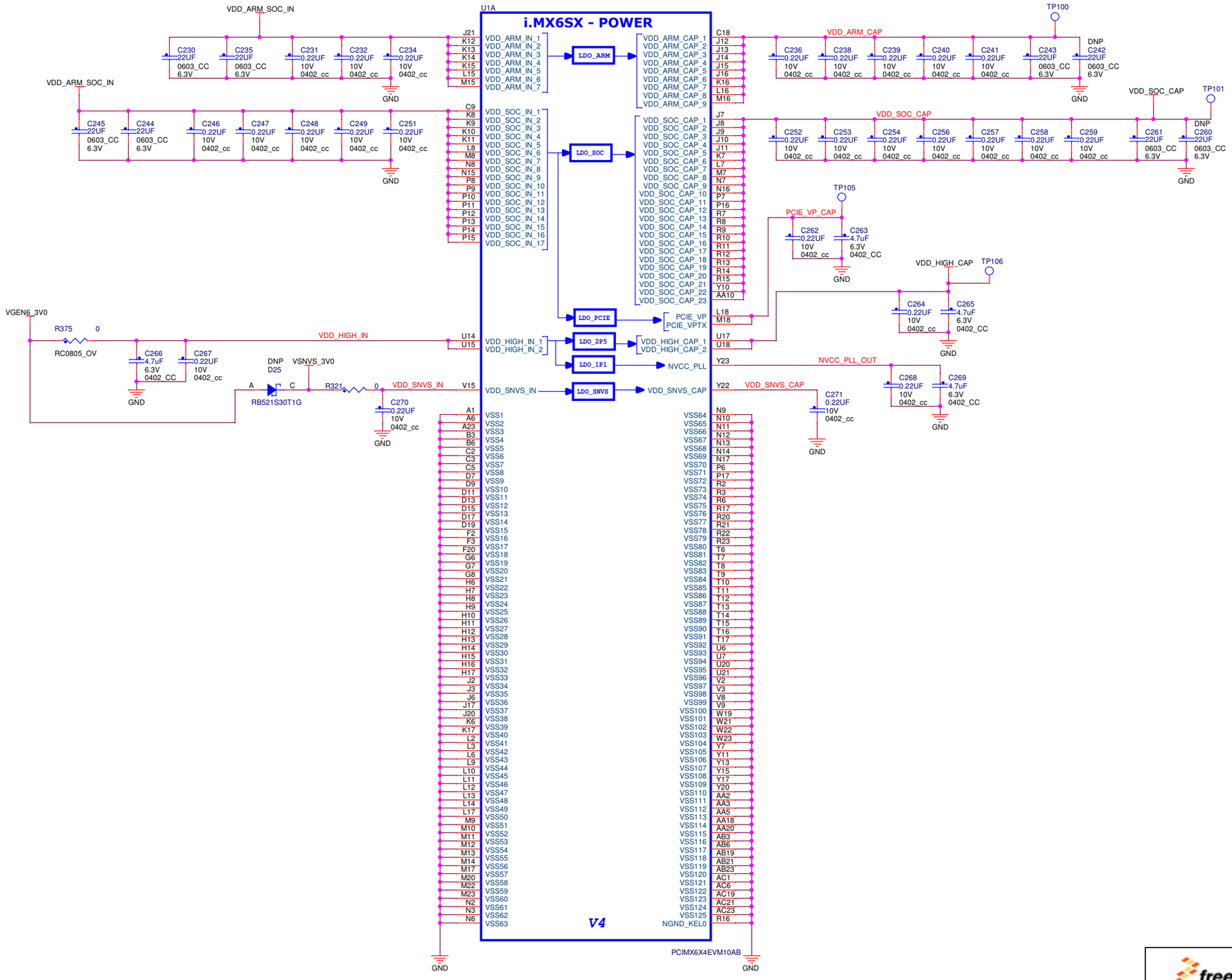

ICAP Classification:	FCP:___ FIUO: X PUBI:___
Drawing Title:	MCIMX6SX SDB
Page Title:	i.MX6SX Power
Size: C	Document Number: SCH-27962 PDF: SPF-27962 Rev: C
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Note:
When U40 is populated, need to populate
these four termination resistors (HCSL-to-LVDS)
for PCIe reference clock to i.MX6SX.

C365 reserved for ESD purpose

Pin G11 & G12 share the same de-coupling capacitor.

Pin G15 & G16 share the same de-coupling capacitor on Pin G14.

ICAP Classification:	FCP: ___ FIUO: X PUBI: ___
Drawing Title:	MCIMX6SX SDB
Page Title:	i.MX6SX SoC I
Size: D	Document Number: SCH-27962 PDF: SPF-27962 Rev: C
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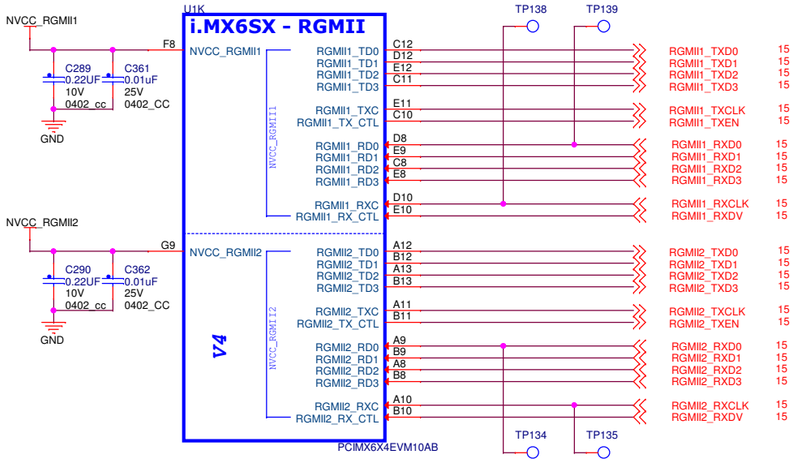
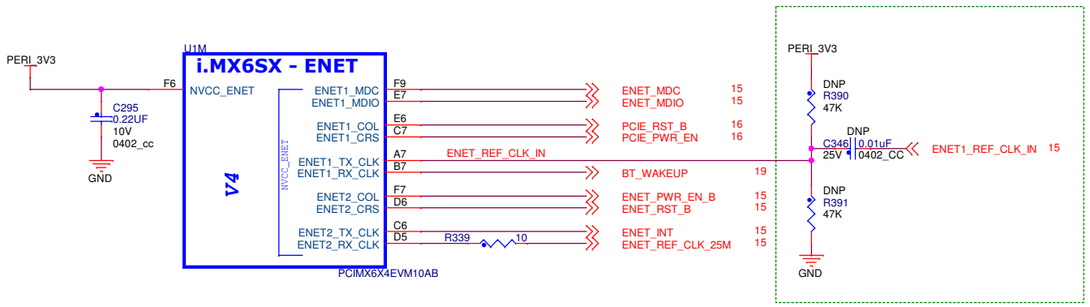
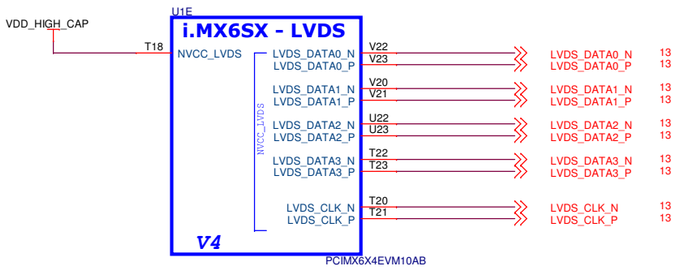
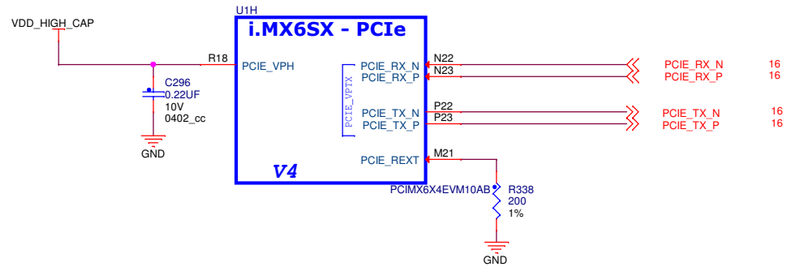


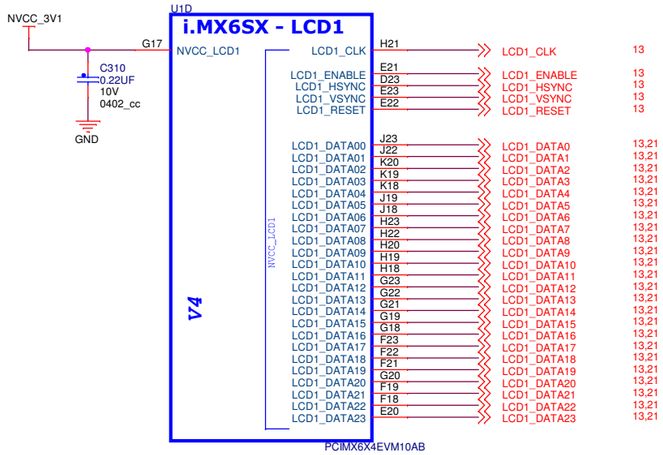


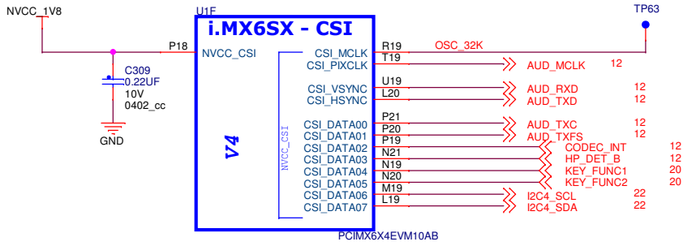
Note:
This block is reserved for testing external ENET reference clock to i.MX6SX.

Pin R18 & T18 share the same de-coupling capacitor.









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ICAP Classification: FCP: ___ FIUO: X PUBI: ___

Drawing Title: **MCIMX6SX SDB**

Page Title: **i.MX6SX SoC II**

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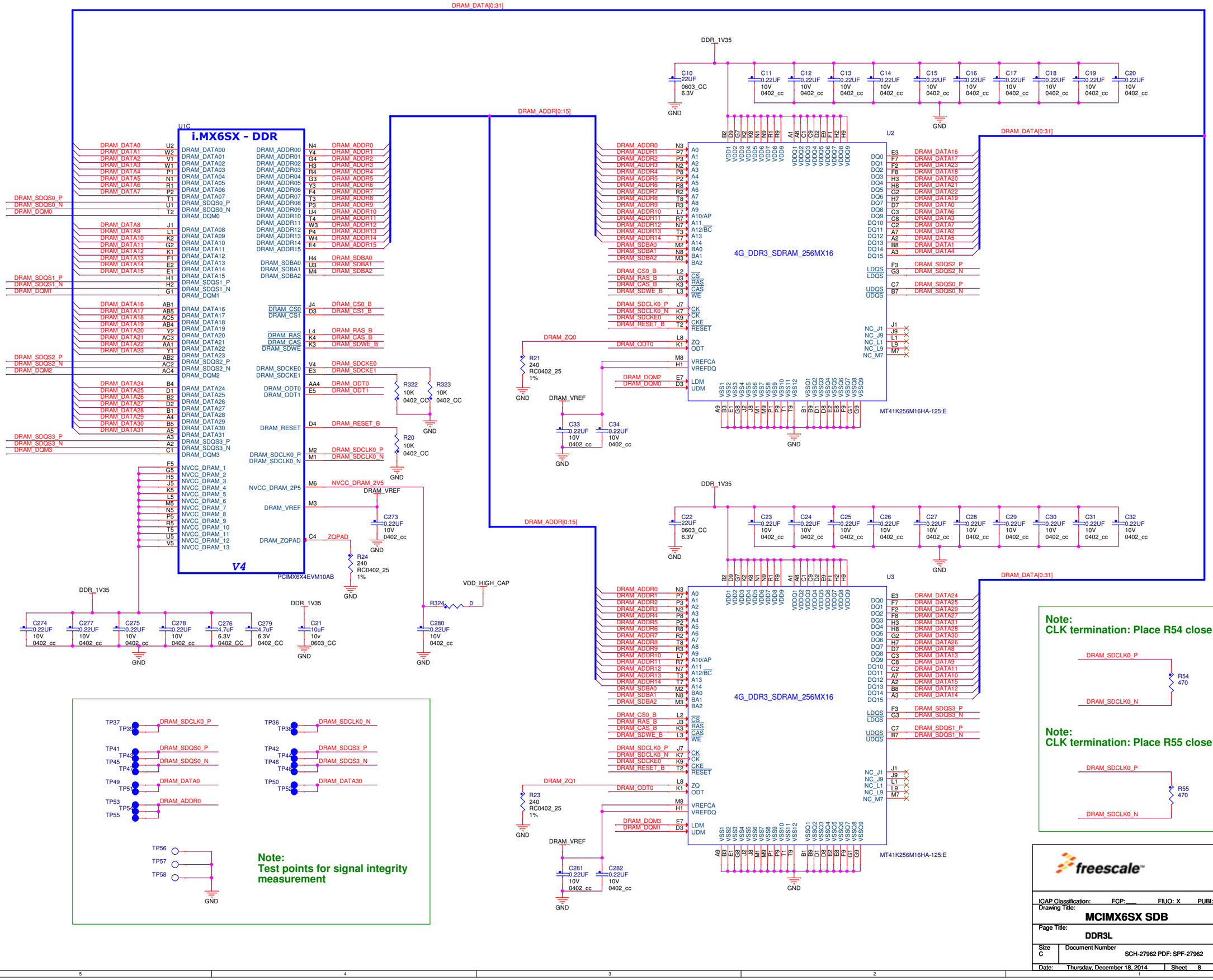
DRAM_DATA[0:31]
DRAM_ADDR[0:15]
U1C
i.MX6SX - DDR
V4
PCIMX6X4EVM10AB
DDR_1V35
U2
U3
4G_DDR3_SDRAM_256MX16
MT41K256M16HA-125:E
DRAM_VREF
DRAM_ZQ0
DRAM_ZQ1
GND
Note:
Test points for signal integrity measurement
Note:
CLK termination: Place R54 close to U2.
Note:
CLK termination: Place R55 close to U3.
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ICAP Classification: FCP:___ FIUO: X PUBI:___
Drawing Title:
MCIMX6SX SDB
Page Title:
DDR3L
Size C
Document Number SCH-27962 PDF: SPF-27962
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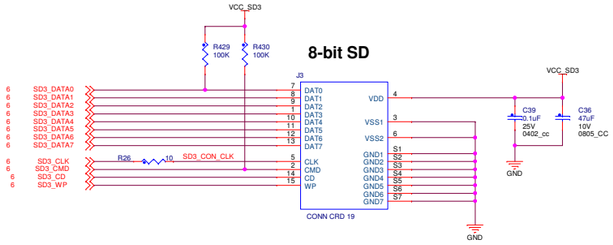
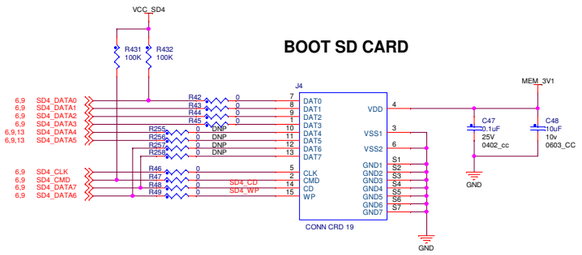
SD3 - For Primary External Card Slot (SD3.0)

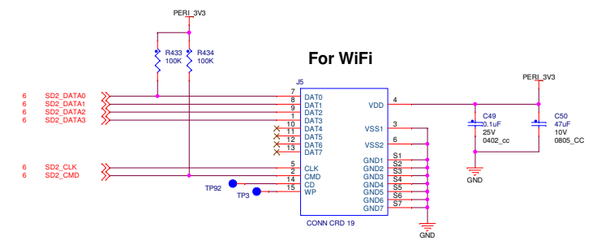


SD4 - For Boot Code

Either SD Card on SD4 or
eMMC on SD4 is used as boot device

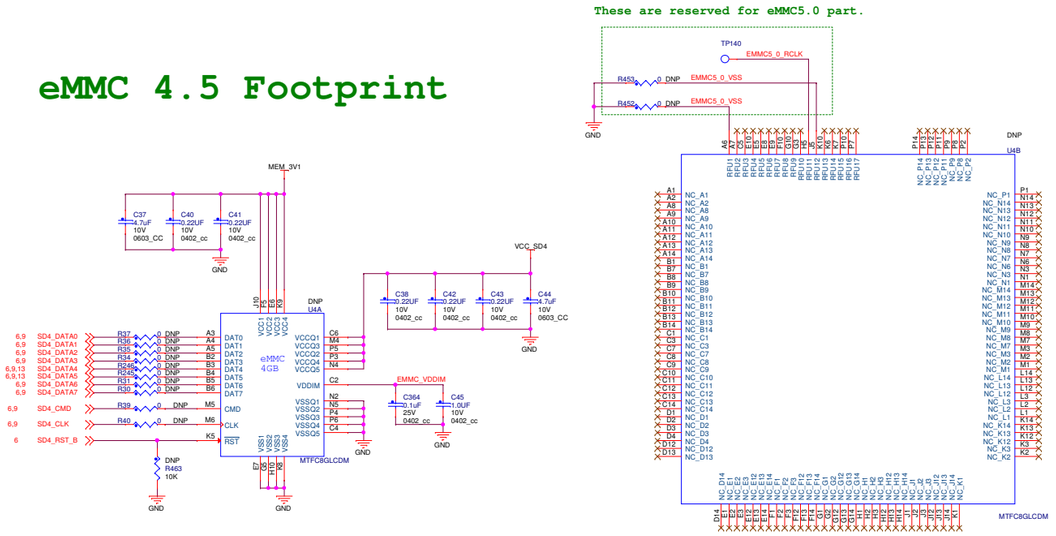


SD2 - for WiFi and SD Accessories



eMMC 4.5 Footprint

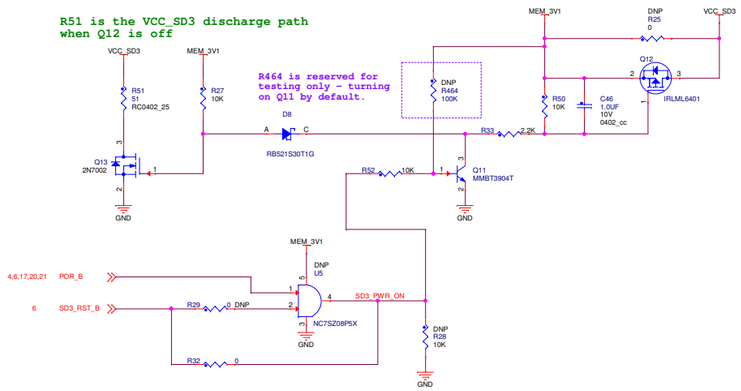
These are reserved for eMMC5.0 part.



Power switch circuit for External SD Card (SD3)

Remove R51 when R25 is populated.

R51 is the VCC_SD3 discharge path when Q12 is off



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ICAP Classification:	FCP: ___ FIUO: X PUBI: ___	
Drawing Title:	MCIMX6SX SDB	
Page Title:	SD & eMMC	
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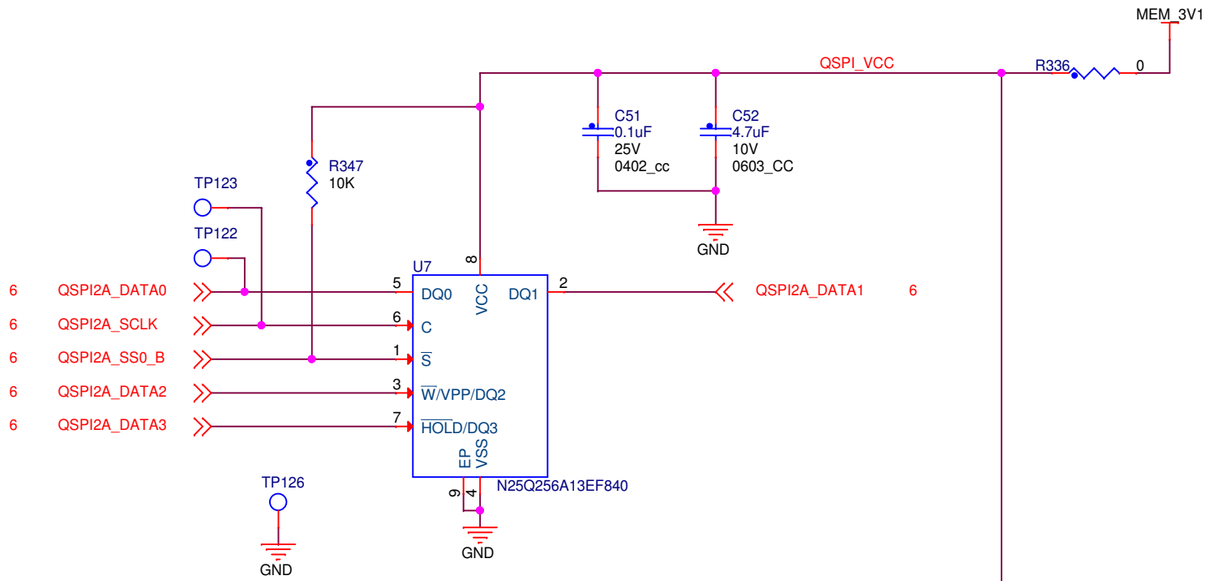
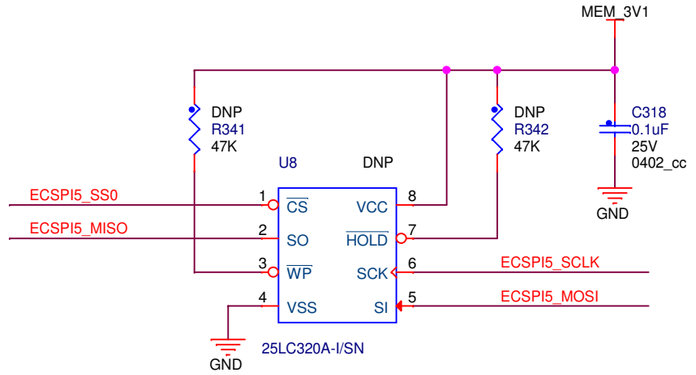
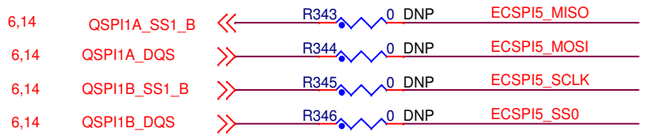
2 x 256Mbit QSPI FLASH



SPI EEPROM FOOTPRINT





These four signals are routed to CAN transceivers also. For SPI EEPROM test, the 0-ohm jumpers on CAN transceiver side are required to be removed.

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Drawing Title: **MCIMX6SX SDB**

Page Title: **QSPI Flash & EEPROM**

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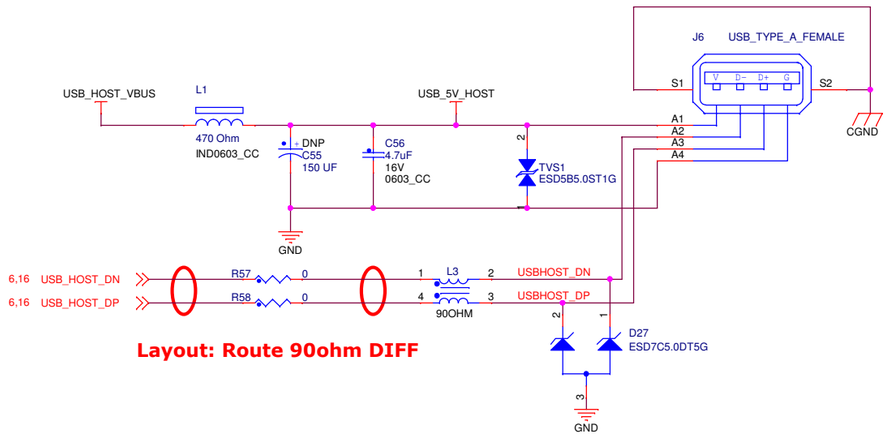
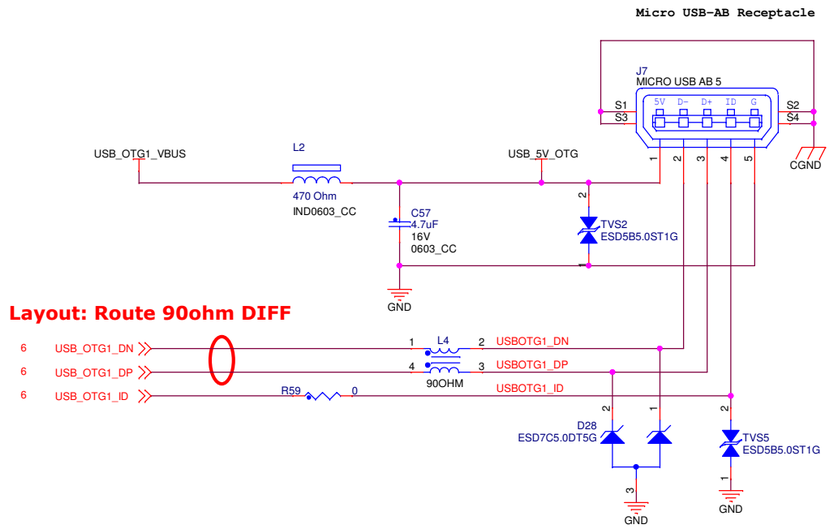
USB Host Port

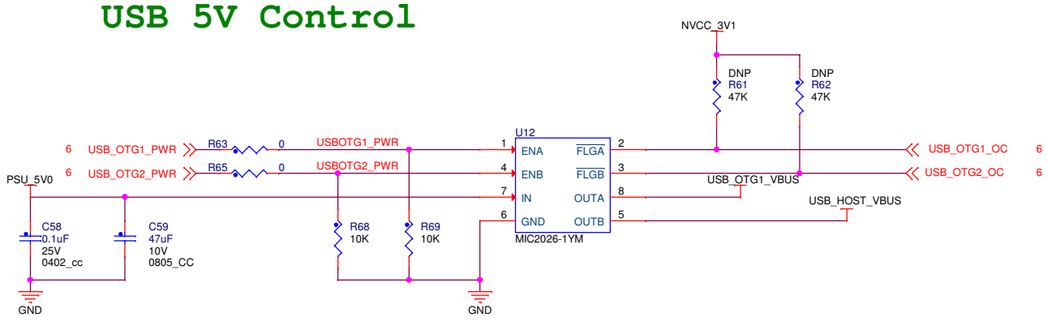


Layout: Route 90ohm DIFF

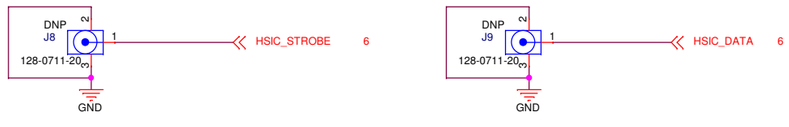
USB Boot/Host/Device Port

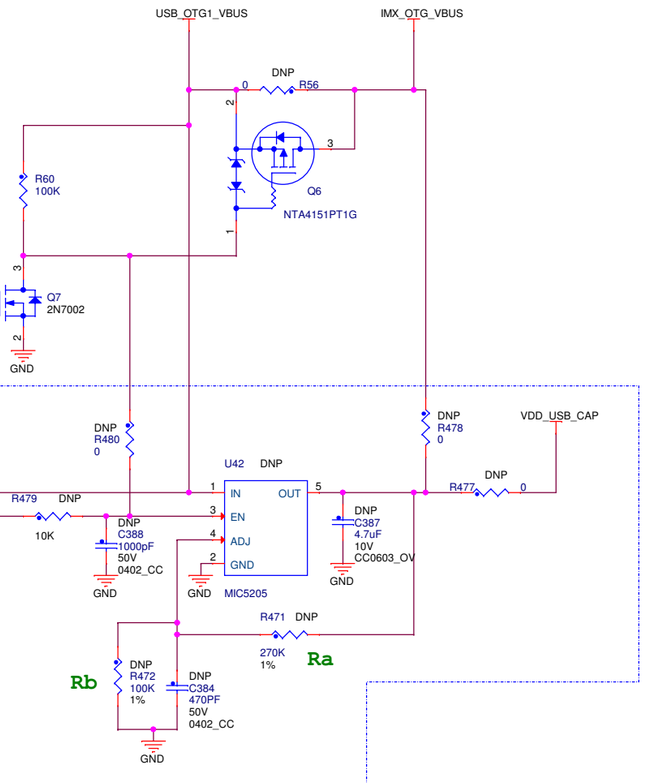


USB 5V Control



USB HSIC





This block is reserved for USB OTG certification test.

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ICAP Classification: FCP:___ FIUO: X PUBI:___

Drawing Title: **MCIMX6SX SDB**

Page Title: **USB**

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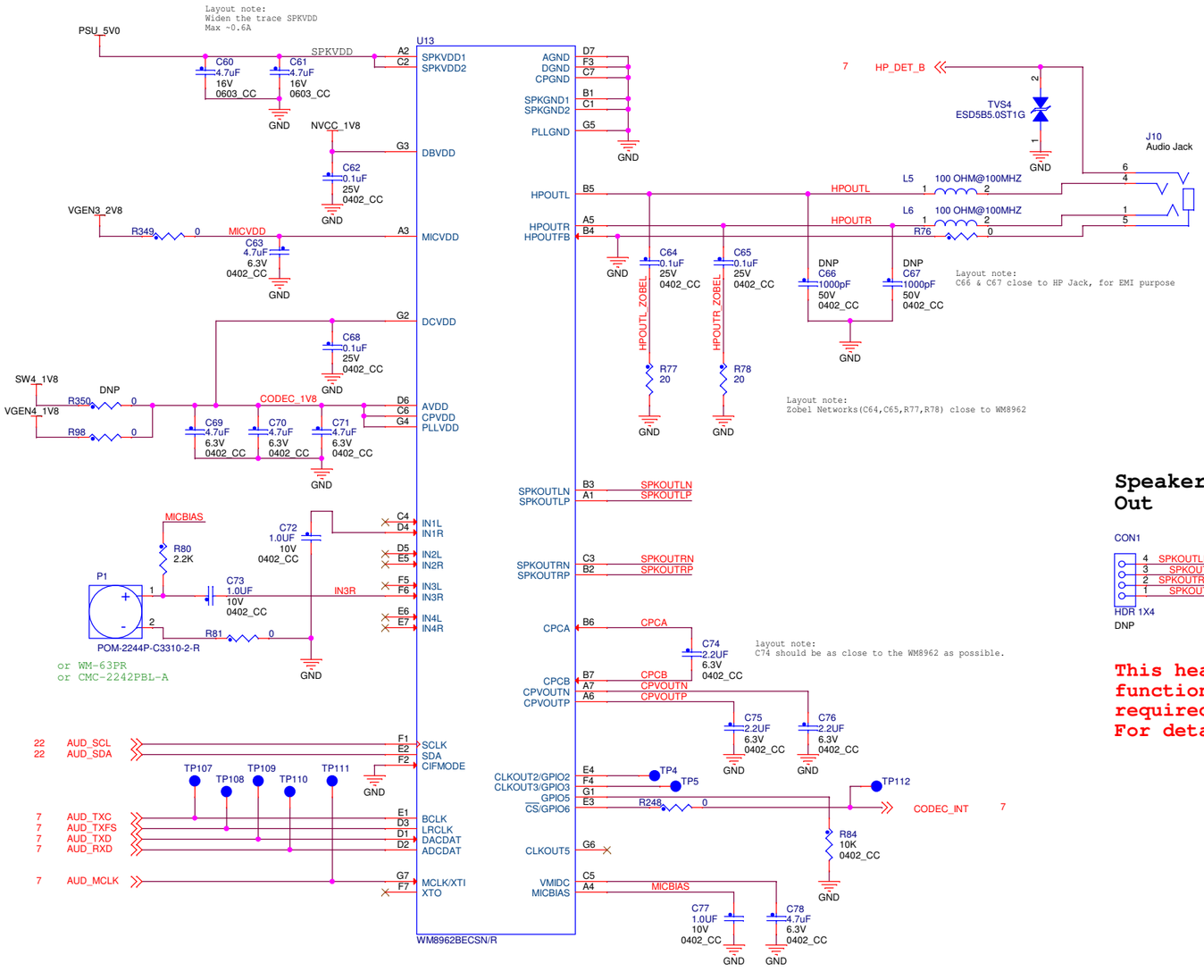
Audio CODEC



Speaker Out

CON1

HDR 1X4

DNP

4	SPKOUTLP
3	SPKOUTLN
2	SPKOUTRP
1	SPKOUTRN

This header footprint is provided for functional test only. A L-C filter may be required for actual application and EMC purpose. For details, consult Wolfson Microelectronics.

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ICAP Classification: FCP:___ FIUO: X PUBI:___

Drawing Title: **MCIMX6SX SDB**

Page Title: **Audio**

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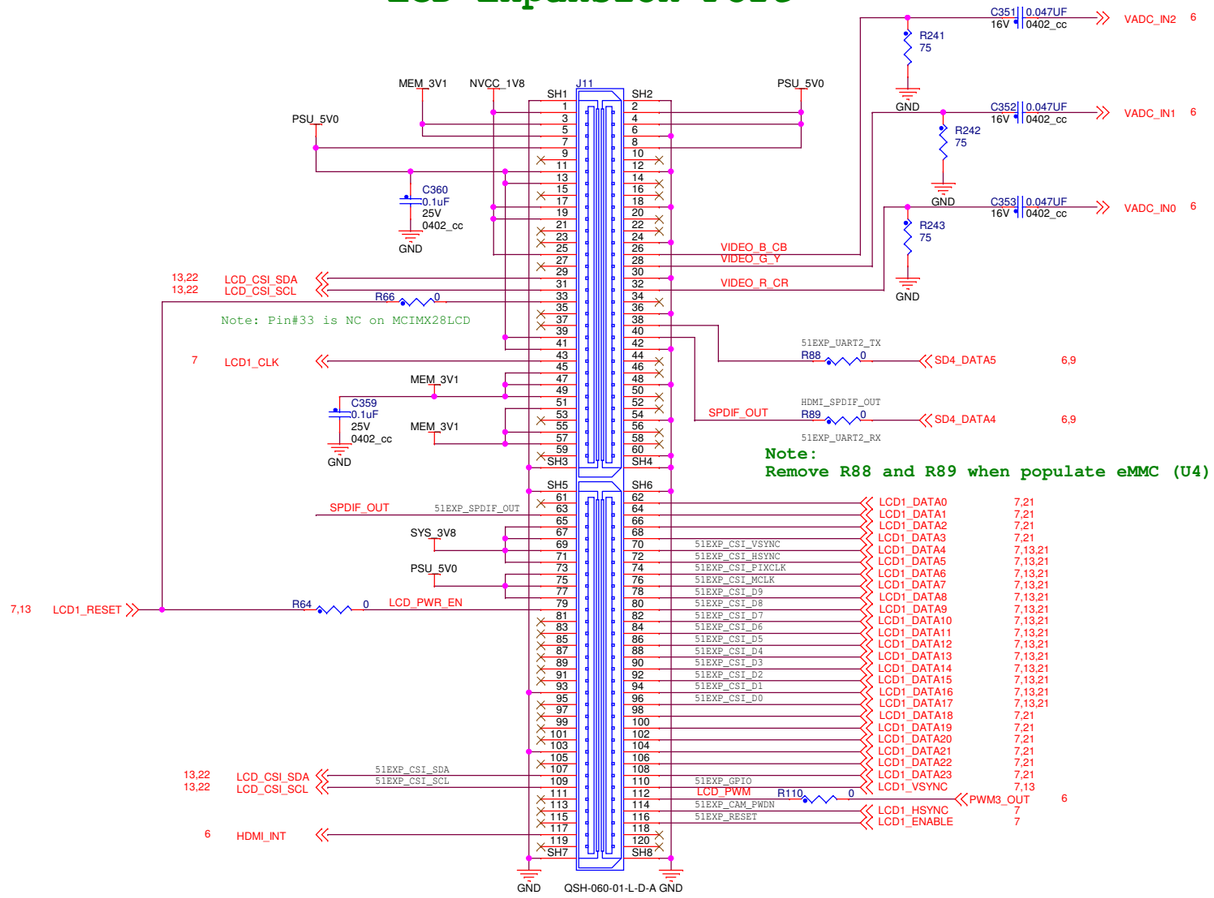
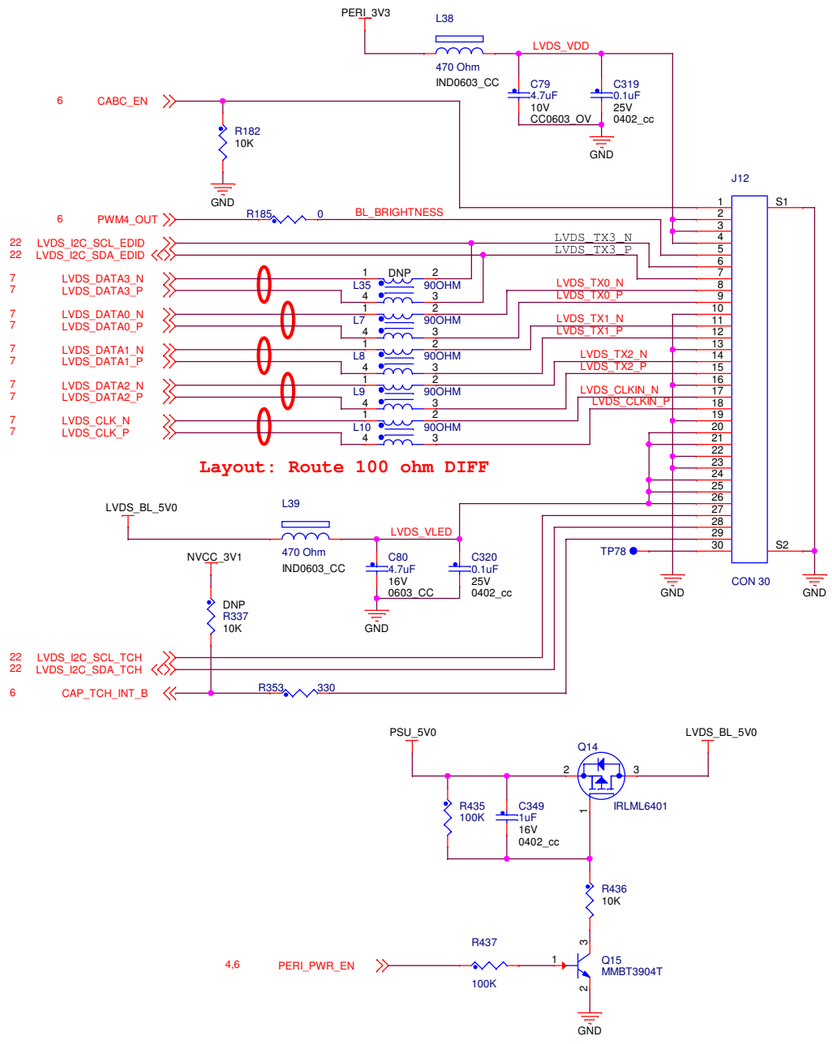
LCD Expansion Port



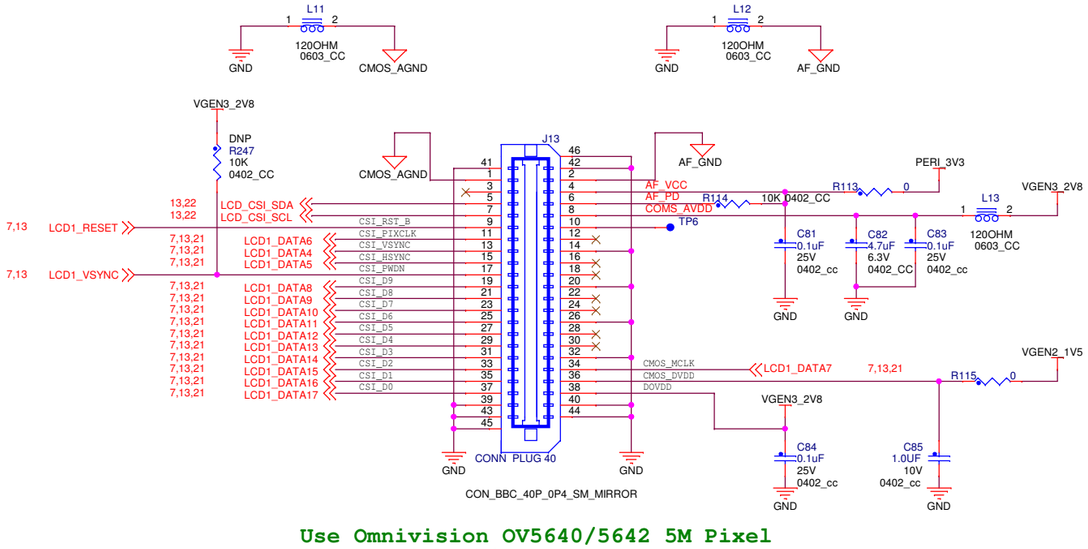
Note:
Remove R88 and R89 when populate eMMC (U4)

LVDS



Layout: Route 100 ohm DIFF

Camera Expansion Connector



Use Omnivision OV5640/5642 5M Pixel Sensor with this connector (not included)

Important Note:

The camera connector (J13) and the LCD Expansion connector (J11) share the same signals and CANNOT be used at the same time.

One of these two peripherals MUST BE REMOVED when a developer wishes to use the other.

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ICAP Classification: FCP:___ FIUO: X PUBI:___

Drawing Title: **MCIMX6SX SDB**

Page Title: **LCD, LVDS & Camera**

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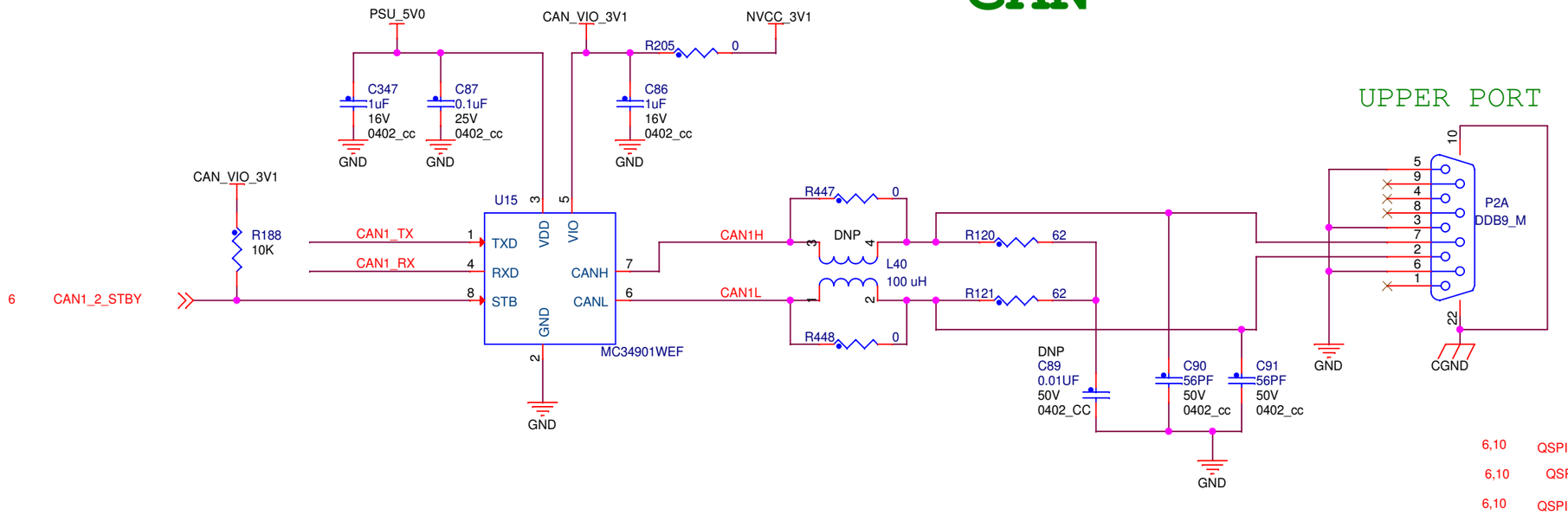
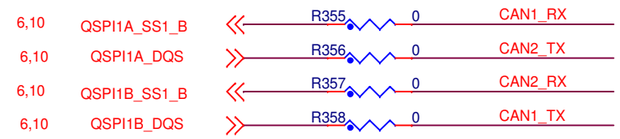
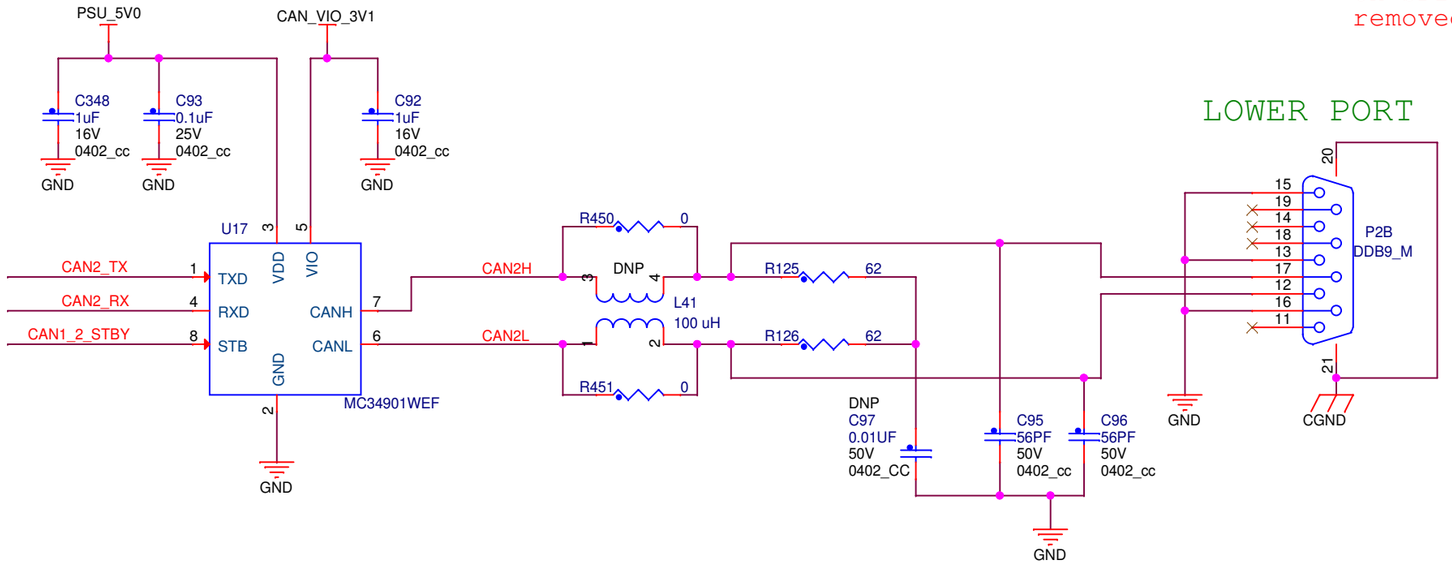
CAN





These four signals are routed to SPI EEPROM also. For CAN test, the 0-ohm jumpers on SPI EEPROM side are required to be removed.



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ICAP Classification: FCP:___ FIUO: X PUBI:___

Drawing Title:
MCIMX6SX SDB

Page Title:
CAN

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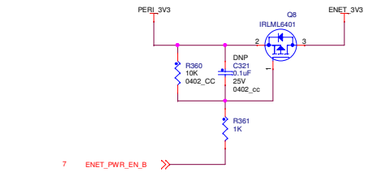
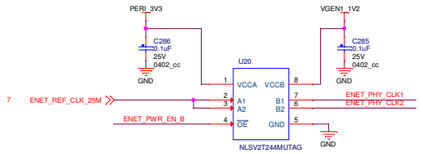
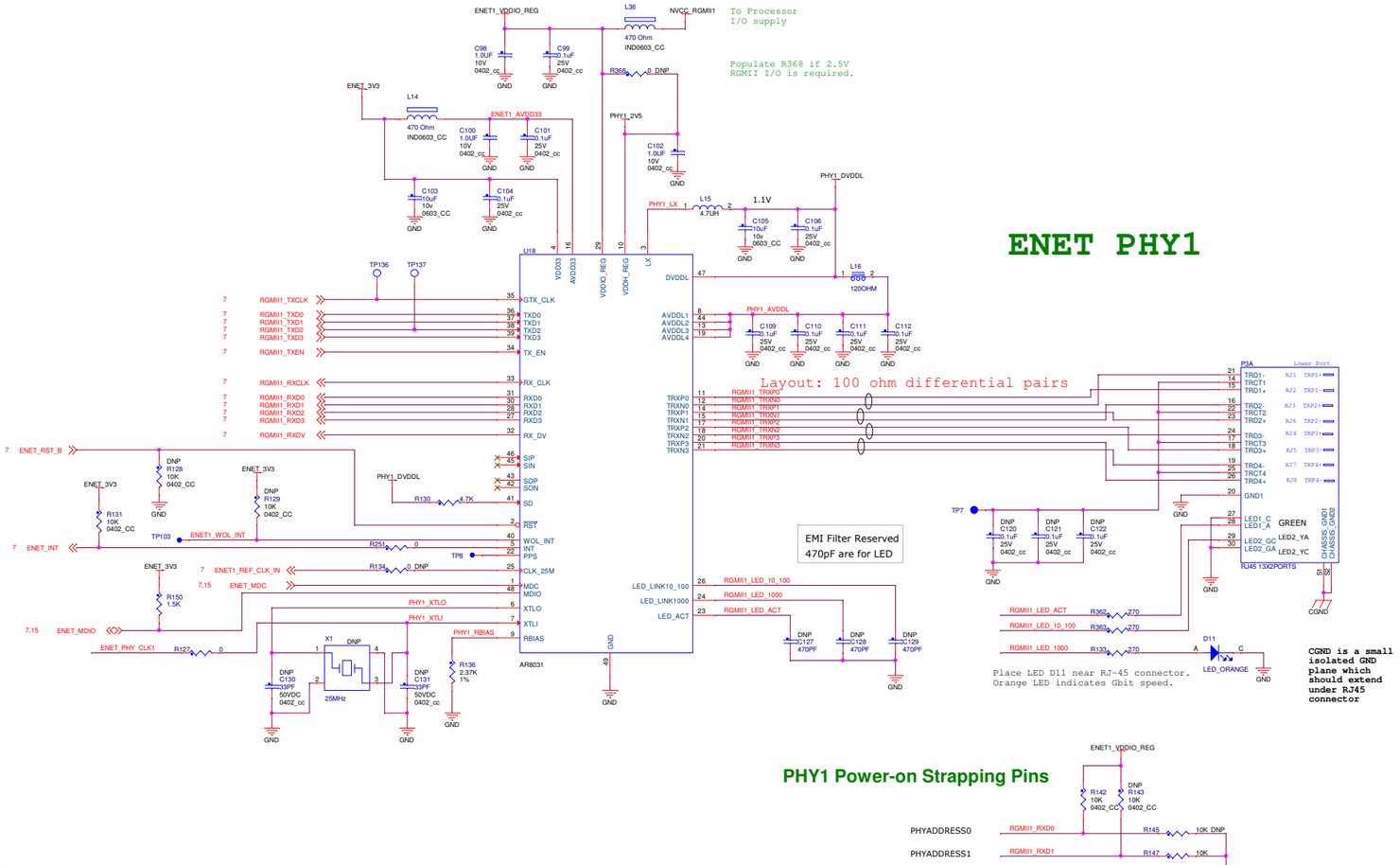
ENET PHY POWER SWITCH



ENET PHY CLK LEVEL SHIFTER



ENET PHY1

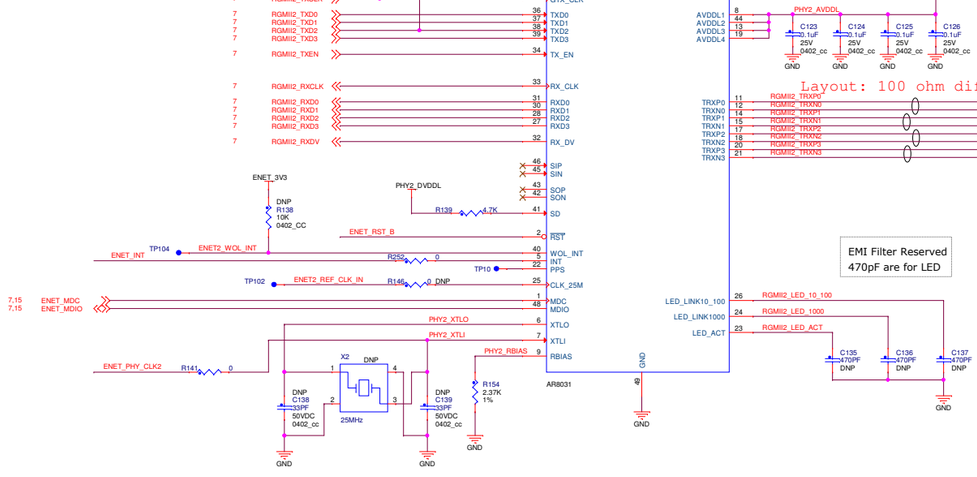


PHY1 Power-on Strapping Pins

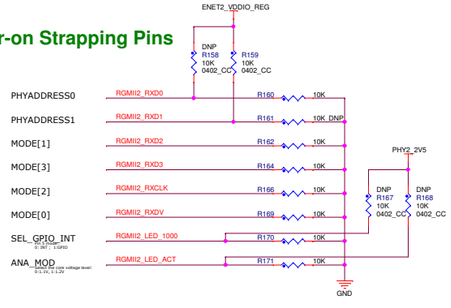
MODE[3:0]

(Default assemble: 0000)
0000 10Base-T/100Base-T/1000Base-T, RGMII

ENET PHY2



PHY2 Power-on Strapping Pins



MODE[3:0]

(Default assemble: 0000)
0000 10Base-T/100Base-T/1000Base-T, RGMII

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ICAP Classification:	FCP: ___ FIUO: X PUBI: ___
Drawing Title:	MCIMX6SX SDB
Page Title:	Ethernet
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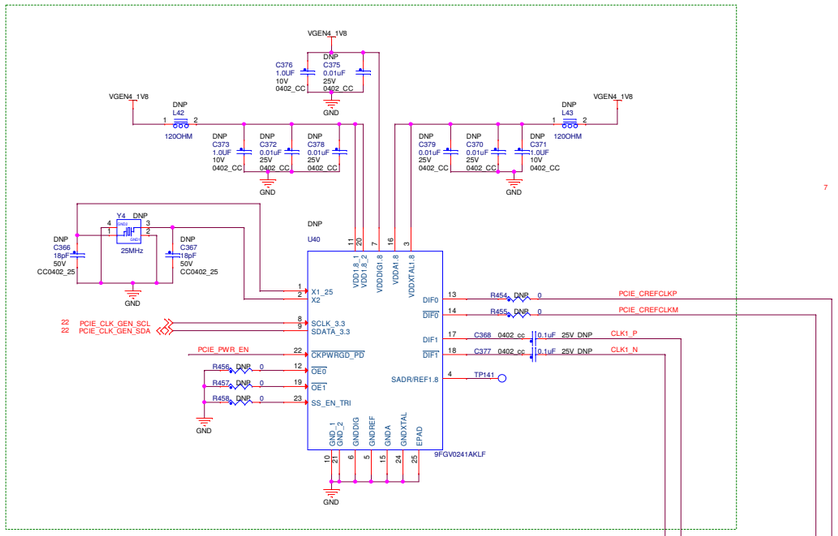
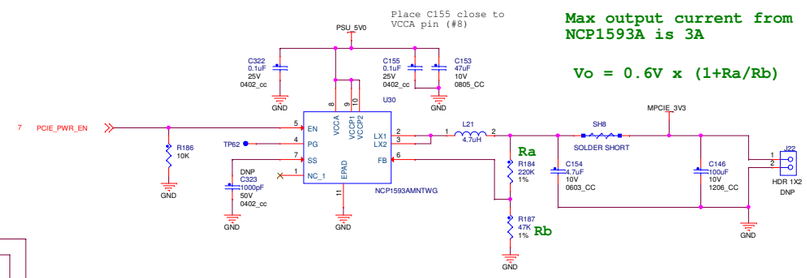
Mini-PCIE

Note:
All components in this block are needed
to be populated for PCIe GEN2 clock jitter test.



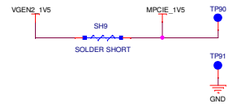
Step-down DCDC for mPCIe +3.3V



Max output current from NCP1593A is 3A

Vo = 0.6V x (1+Ra/Rb)

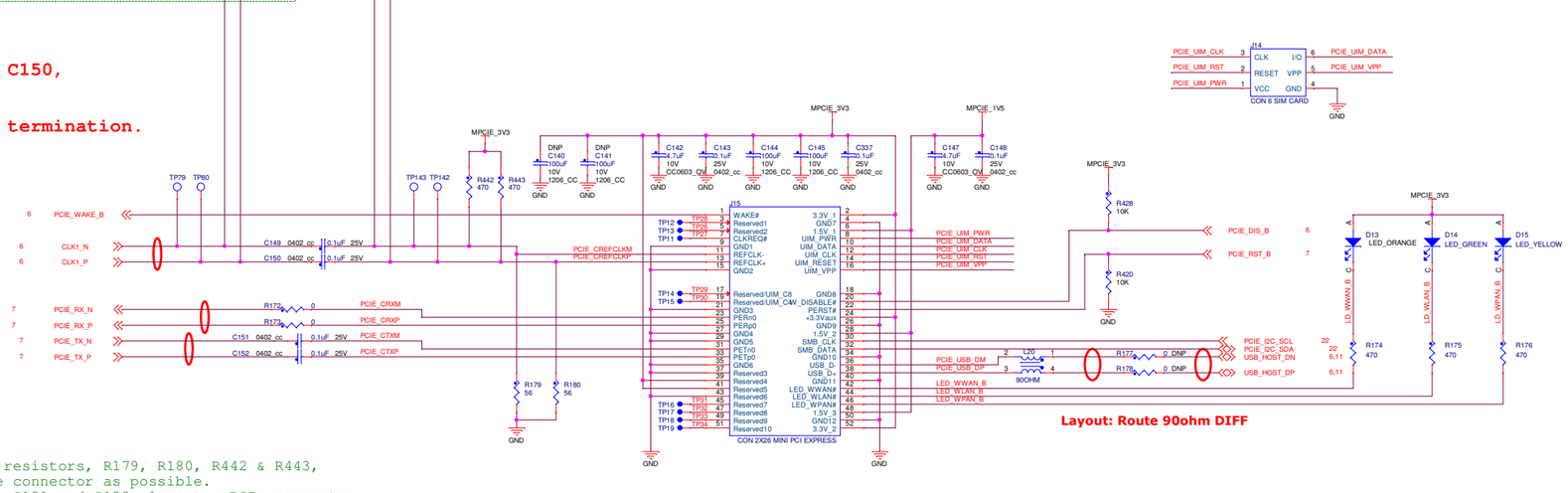
Max output current from VGEN2_1V5 is 250mA



When U40 is populated –
i) Remove R442, R443, R179, R180, C149, C150,
and use U40 to output PCIe refclk to
i.MX6SX and mPCIe connector.
ii) Mount R459-R462 on i.MX6SX side for termination.

Layout: Route 100 ohm DIFF for CLK1_P/N

Layout: Route 85 ohm DIFF for PCIE_TX/RX



Layout: Route 90ohm DIFF

Layout Note:
i) Place termination resistors, R179, R180, R442 & R443,
as close to the mPCIe connector as possible.
ii) Place C149, C150, C151 and C152 close to mPCIe connector.
iii) Place R454, R455 close to C149 and C150.
iv) Place C368, C377 close to C149 and C150.

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ICAP Classification: FCP: ___	FIUO: X	PUBI: ___
Drawing Title: MCIMX6SX SDB		
Page Title: mPCIe		
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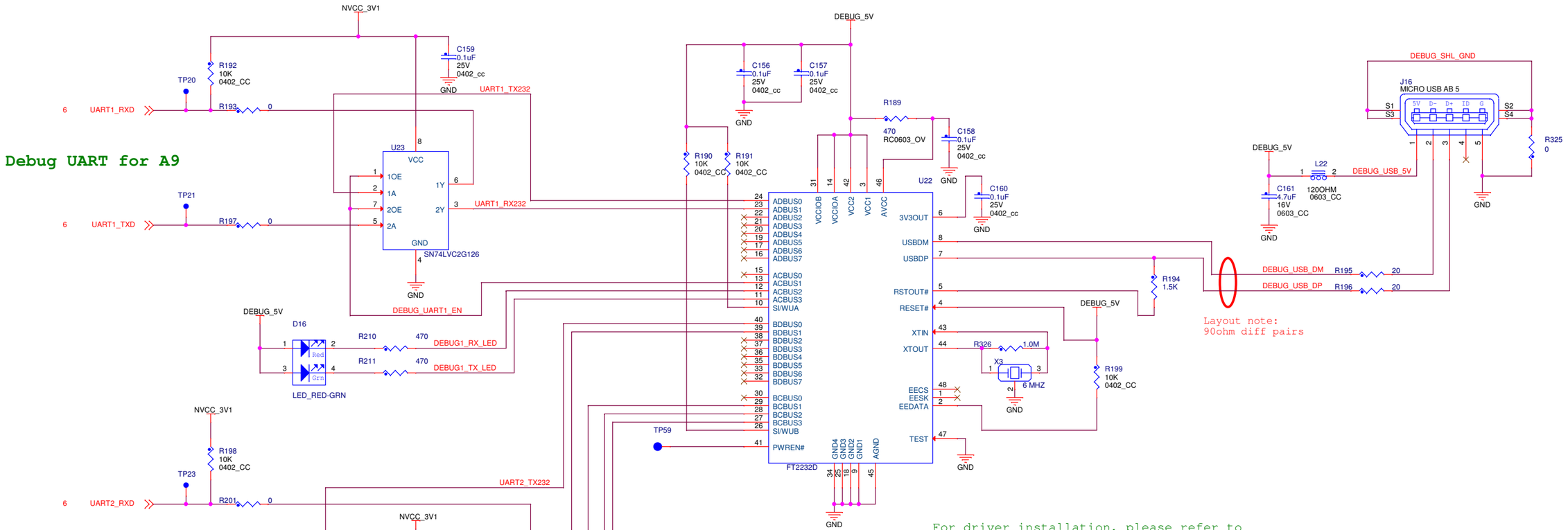
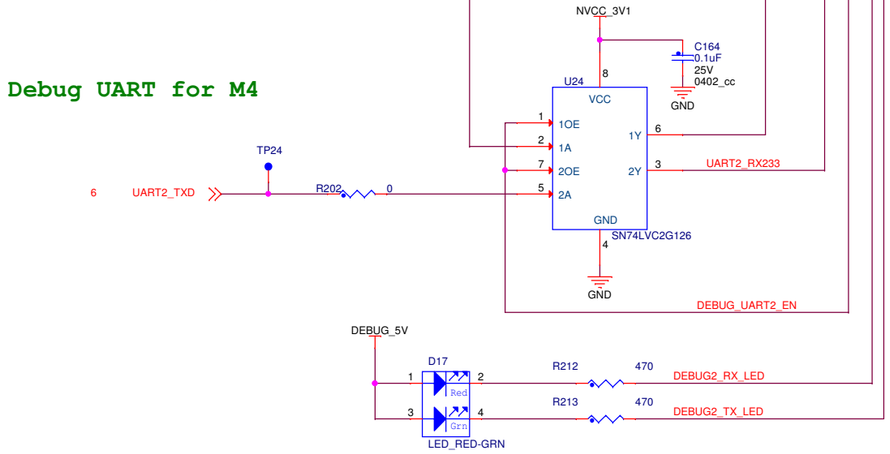
Debug UART to USB Converter

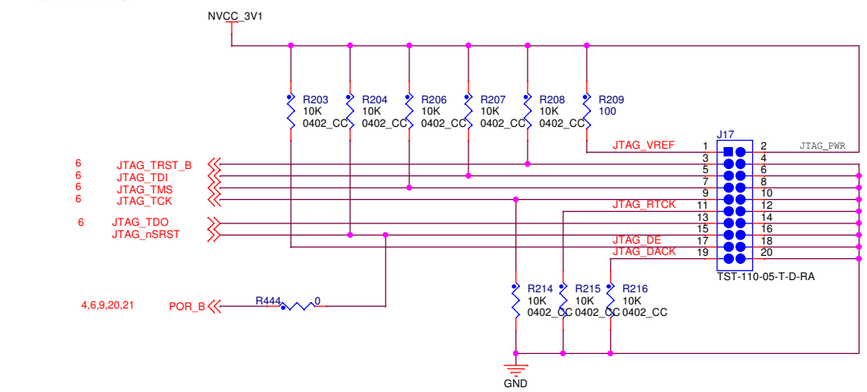
Debug UART for A9

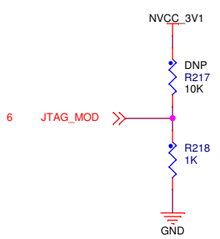


Debug UART for M4



JTAG





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ICAP Classification: FCP:___ FIUO: X PUBI:___

Drawing Title:
MCIMX6SX SDB

Page Title:
UART & JTAG

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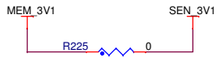
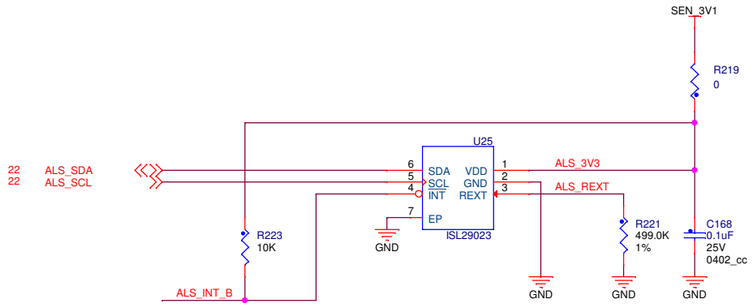
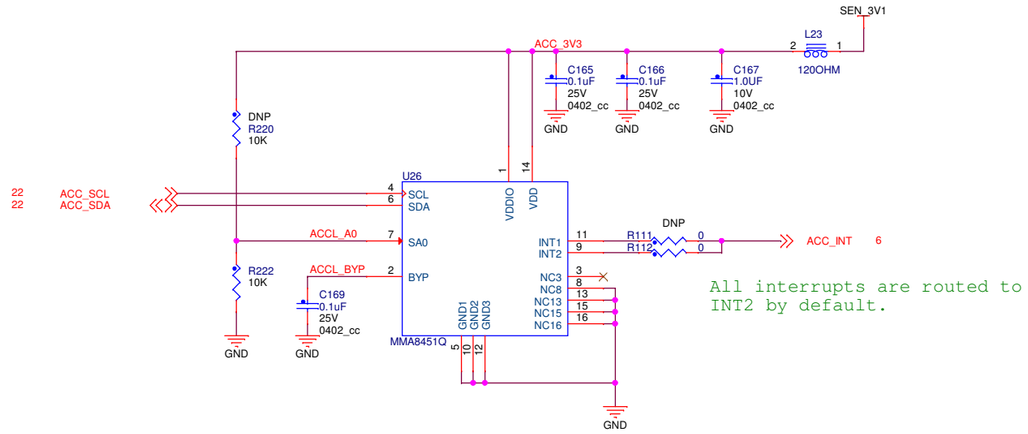
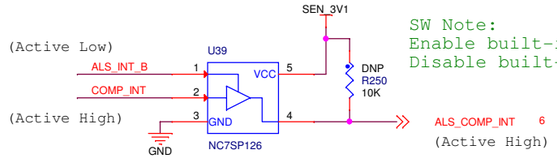


Ambient Light Sensor



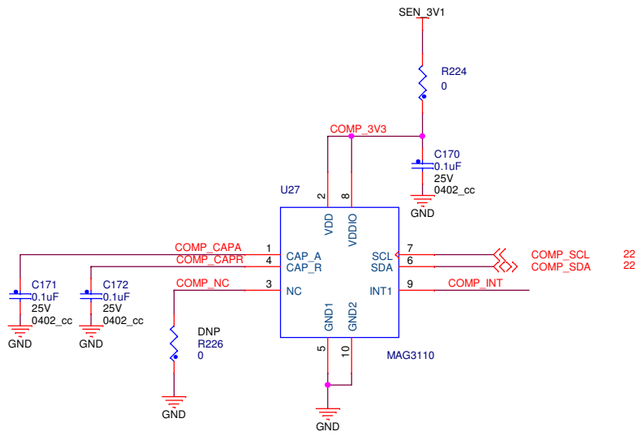
3-AXIS ACC



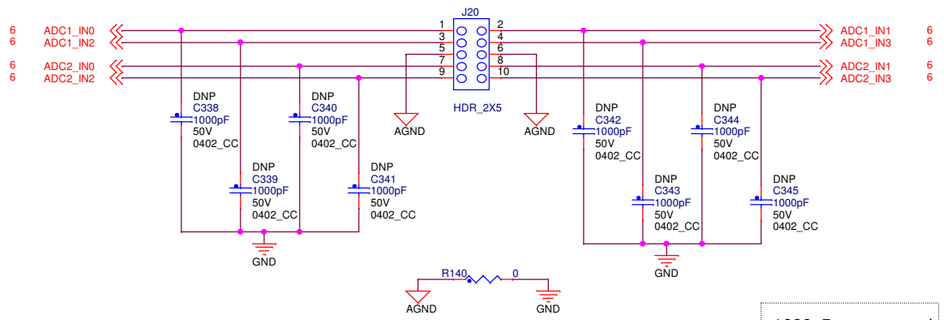


SW Note:
Enable built-in Pull-up for normal operation;
Disable built-in Pull-up during DSM.

Digital eCompass



12-bit ADC Connector



1000pF are reserved
for EMC purpose

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ICAP Classification: FCP:___ FIUO: X PUBI:___

Drawing Title:
MCIMX6SX SDB

Page Title:
Sensors & 12-bit ADC

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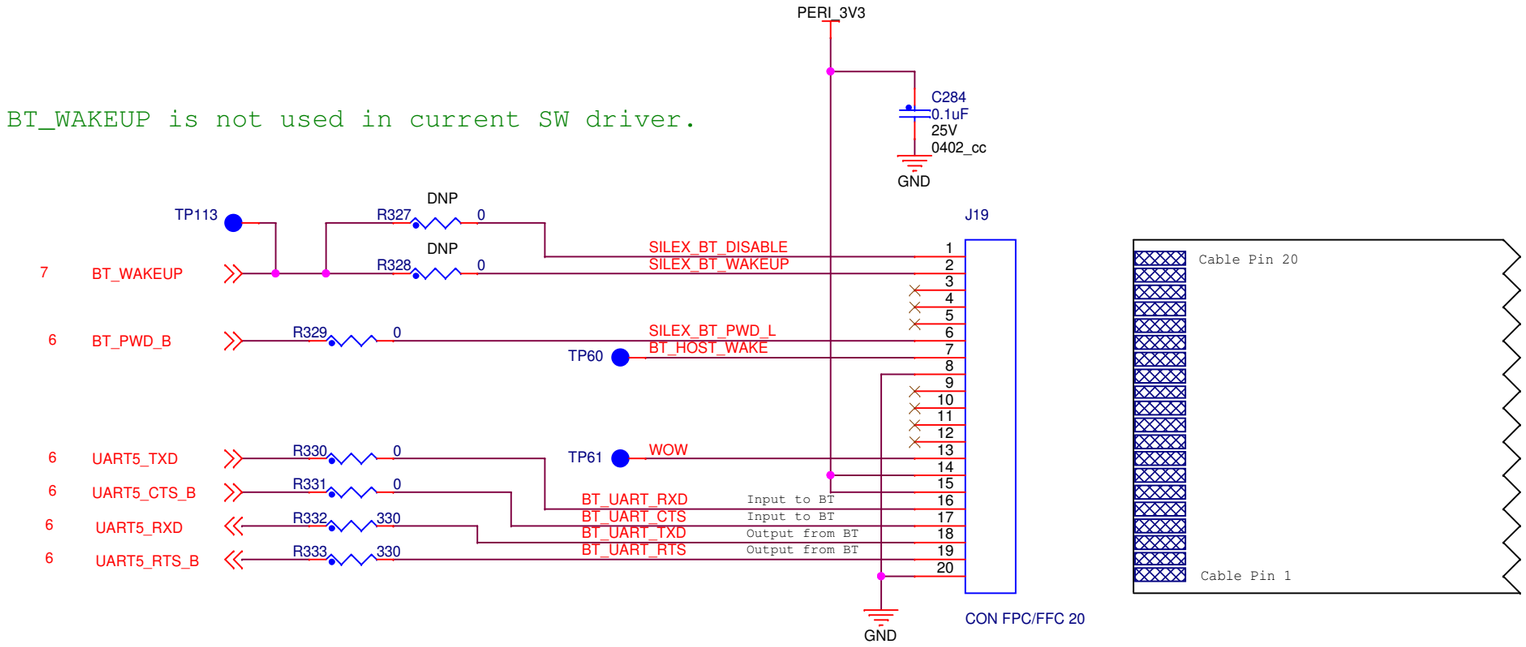
BLUETOOTH CABLE CONNECTOR



NOTE:
The AUX SDIO CARD SOCKET and the BLUETOOTH CABLE CONNECTOR have been designed and tested specifically for use with the WIFI/BT combo card SX-SDCAN-2830BT Developed and sold by Silex Technolgy. The developer may need to consult the datasheet of other WIFI solutions for compatibility with this card socket.

NOTE:
Pin 1 of the cable connector on the Smart Device board is opposite Pin 20 of the WIFI/BT module. For the FFC to lie flat, the pin order number needs to be reversed on the schematics.

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ICAP Classification: FCP:___ FIUO: X PUBI:___

Drawing Title: **MCIMX6SX SDB**

Page Title: **Bluetooth**

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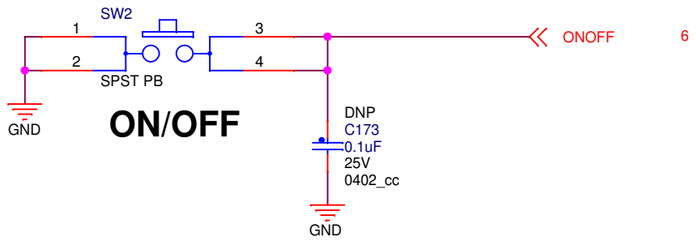
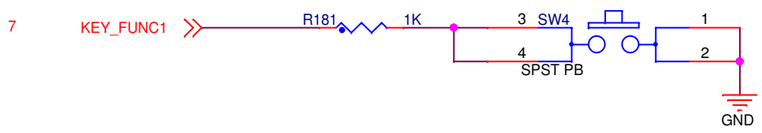
On/Off

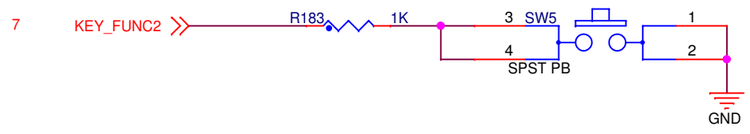


Buttons

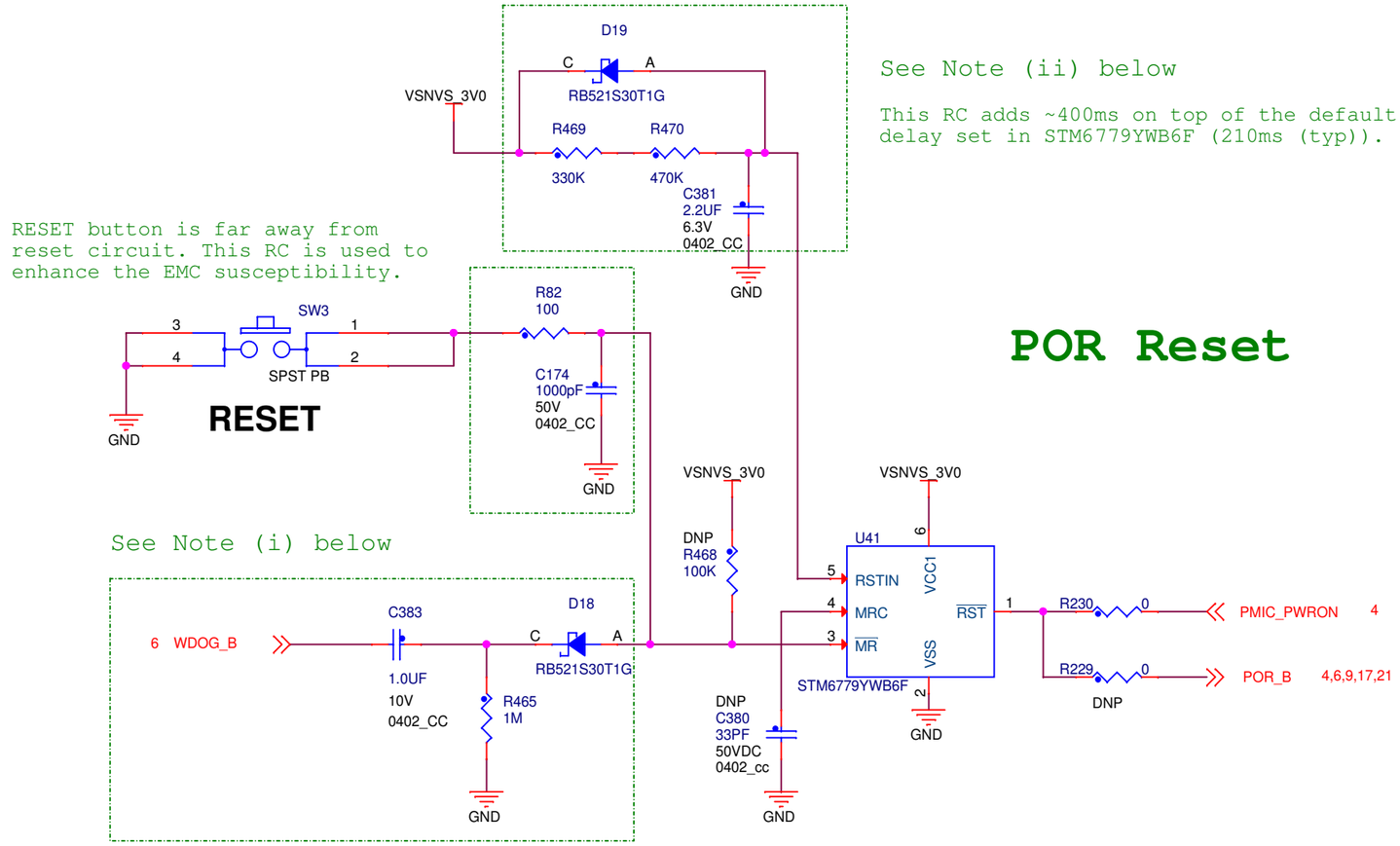
FUNC1



FUNC2



POR Reset



Note:
This block is added in Rev.C for two purposes -
i) Fix the SW reboot issue by togling WDOG_B to issue power reset (ENGR00338067).
ii) Delay the PMIC_PWRON >500ms for the 1st-time power-on (VSNVS_3V0 is first applied), to ensure 32.768kHz xtal osc output is stable.

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ICAP Classification: FCP:___ FIUO: X PUBI:___

Drawing Title: **MCIMX6SX SDB**

Page Title: **Buttons**

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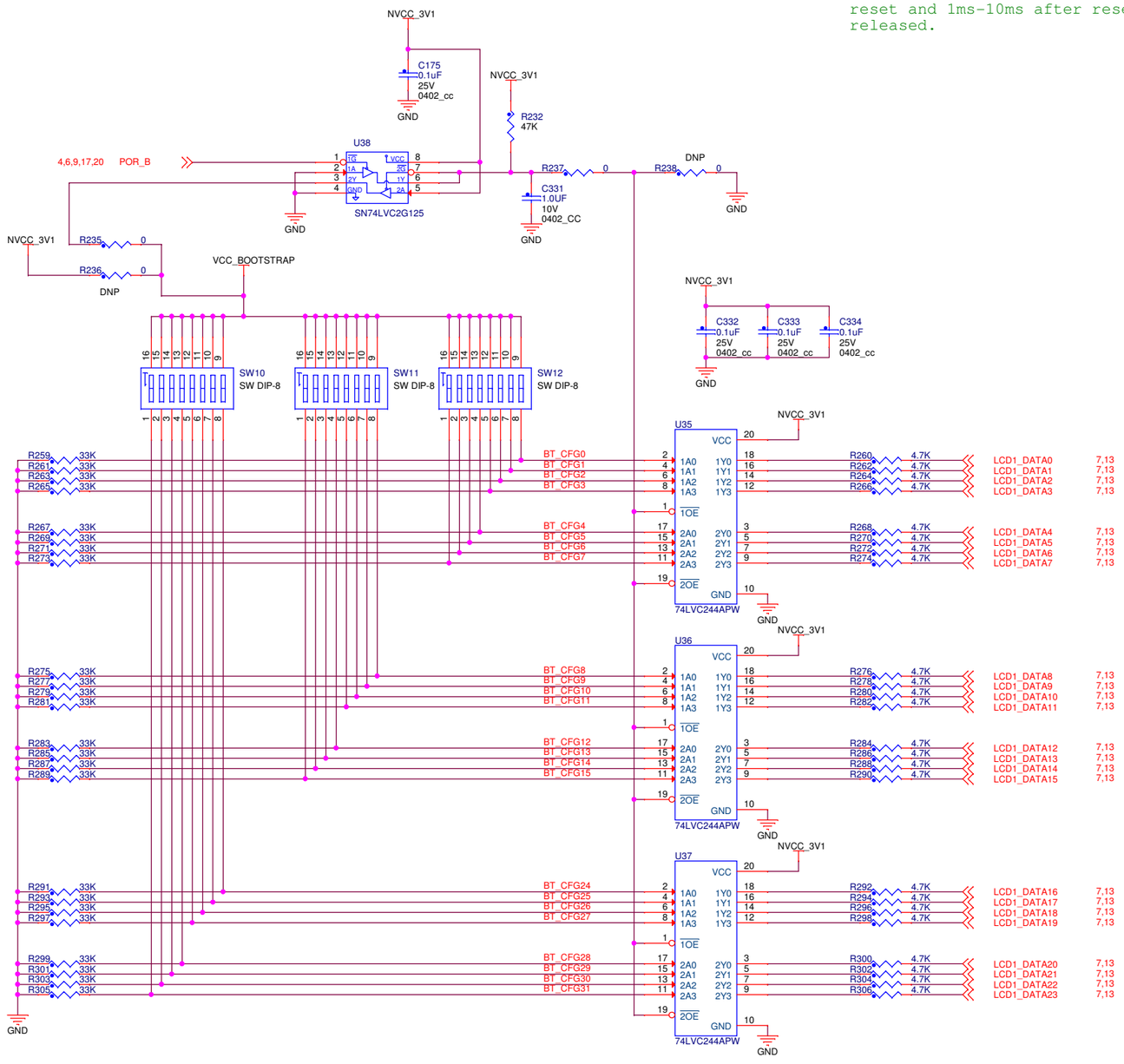
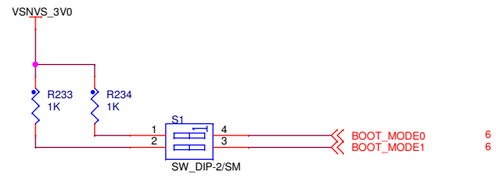
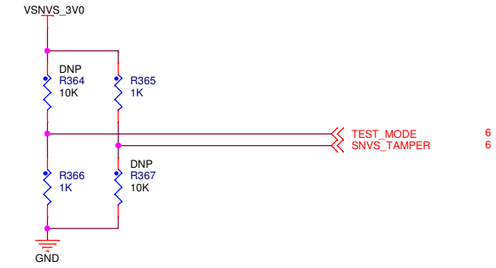
Note:
i.MX6SX reads values approximately
300uS to 1mS after reset released.
Buffers are active while unit is in
reset and 1ms-10ms after reset is
released.







SW Design Note:
LCD_DATA lines should be set at Input with Keeper enable
during Deep Sleep Mode.

Note:
i) SW10 settings are all "0".
ii) BT_CFG1 must be "1" for SD3 operation on SDB,
as it has a power switch control for VCC_SD3.

BOOT MODE

SW12							
1	2	3	4	5	6	7	8
BT_CFG7	BT_CFG6	BT_CFG5	BT_CFG4	BT_CFG3	BT_CFG2	BT_CFG1	BT_CFG0
0001 = QSPI Boot				0 = QSPI1 1 = QSPI2	000		
010 = SD/eSD Boot			0 = Regular 1 = Fast Boot	00 = Normal (3.3V) 01 = High (3.3V)		0 = No PWR Cycle 1 = Enable PWR Cycle	0

SW11							
1	2	3	4	5	6	7	8
BT_CFG15	BT_CFG14	BT_CFG13	BT_CFG12	BT_CFG11	BT_CFG10	BT_CFG9	BT_CFG8
00000000							
00		0 = 1-bit 1 = 4-bit	00 = eSDHC1 01 = eSDHC2 10 = eSDHC3 11 = eSDHC4		0	0	0

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ICAP Classification: FCP:___ FIUO: X PUBI:___

Drawing Title: **MCIMX6SX SDB**

Page Title: **Boot Strap**

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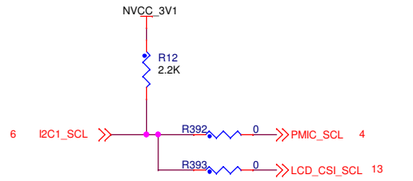
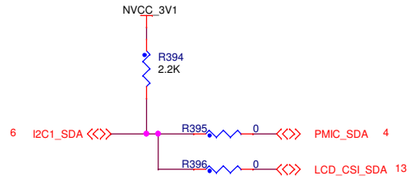
I2C1

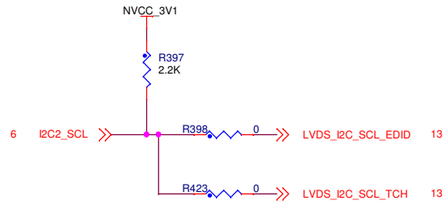


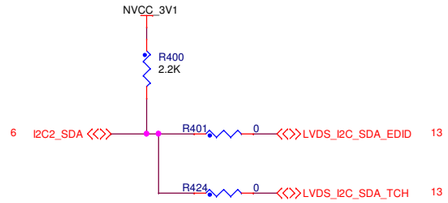


Note: Pull-up resistor must be sized to meet the signal rise times and also the Vil spec of all the bus components.

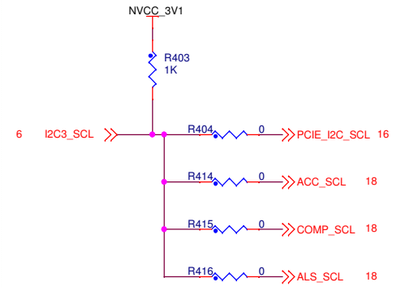
Due to board loadings this resistor was reduced. Validate your design, with the largest allowable resistor to reduce current consumption.

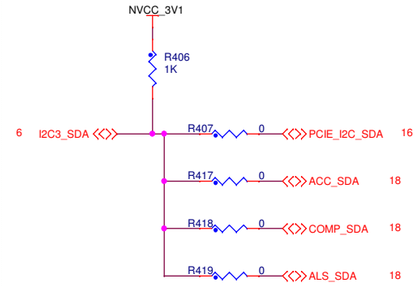
I2C2



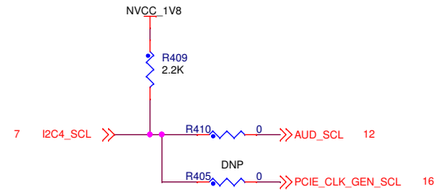


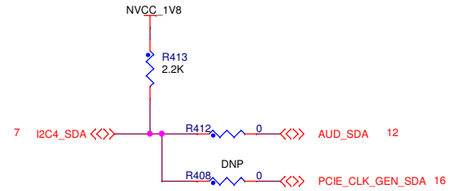
I2C3



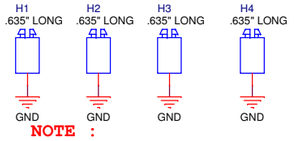


I2C4





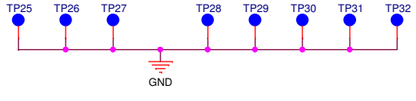
Board Mounting Holes for 4-40 Screws



IMPORTANT NOTE :

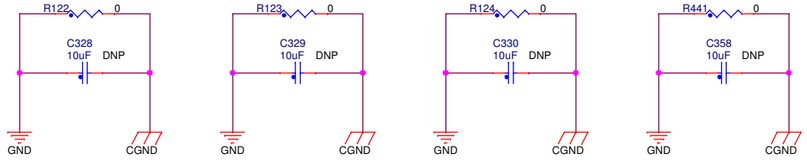
Use non-conducting nut/bolts to mount the board on a metallic chasis connected to external GND. Not doing so may cause board damage due to GND potential difference.

GND TEST POINTS



System GND and Chassis GND Connections

CGND is connected to the connectors enclosure or chassis.
Resistor and capacitor footprints are arranged for ESD test.



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