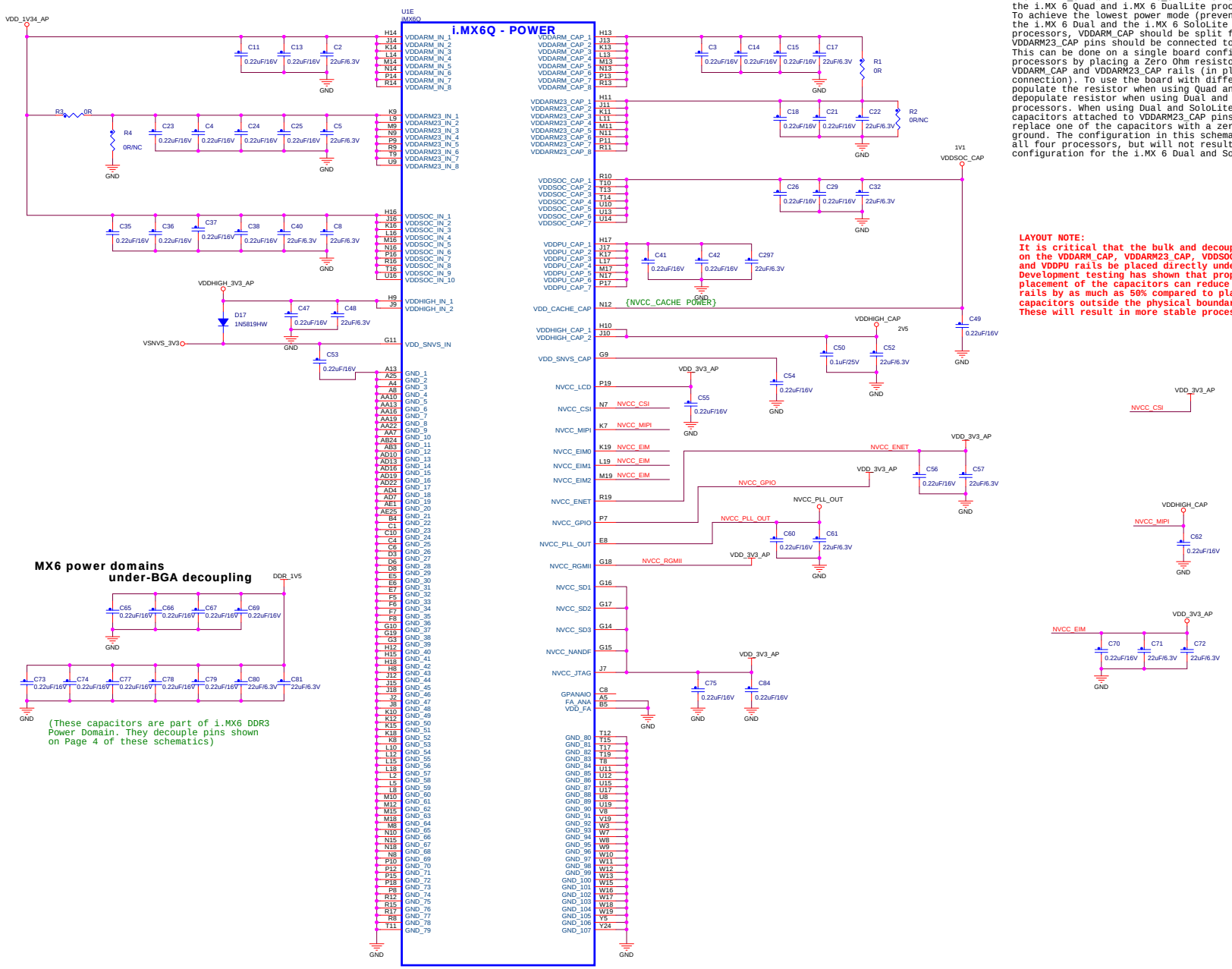
Revision History

V1.0 Initial Released


i.MX6Q - POWER
U1E
IMX6Q
VDD_1V34_AP
VDDARM_IN_1
VDDARM_IN_2
VDDARM_IN_3
VDDARM_IN_4
VDDARM_IN_5
VDDARM_IN_6
VDDARM_IN_7
VDDARM_IN_8
VDDARM23_IN_1
VDDARM23_IN_2
VDDARM23_IN_3
VDDARM23_IN_4
VDDARM23_IN_5
VDDARM23_IN_6
VDDARM23_IN_7
VDDARM23_IN_8
VDDSOC_IN_1
VDDSOC_IN_2
VDDSOC_IN_3
VDDSOC_IN_4
VDDSOC_IN_5
VDDSOC_IN_6
VDDSOC_IN_7
VDDSOC_IN_8
VDDSOC_IN_9
VDDSOC_IN_10
VDDHIGH_3V3_AP
VDDHIGH_IN_1
VDDHIGH_IN_2
VSNVS_3V3
VDD_SNVS_IN
GND_1
GND_2
GND_3
GND_4
GND_5
GND_6
GND_7
GND_8
GND_9
GND_10
GND_11
GND_12
GND_13
GND_14
GND_15
GND_16
GND_17
GND_18
GND_19
GND_20
GND_21
GND_22
GND_23
GND_24
GND_25
GND_26
GND_27
GND_28
GND_29
GND_30
GND_31
GND_32
GND_33
GND_34
GND_35
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GND_38
GND_39
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GND_41
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GND_47
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GND_50
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GND_52
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GND_61
GND_62
GND_63
GND_64
GND_65
GND_66
GND_67
GND_68
GND_69
GND_70
GND_71
GND_72
GND_73
GND_74
GND_75
GND_76
GND_77
GND_78
GND_79
VDDARM_CAP_1
VDDARM_CAP_2
VDDARM_CAP_3
VDDARM_CAP_4
VDDARM_CAP_5
VDDARM_CAP_6
VDDARM_CAP_7
VDDARM_CAP_8
VDDARM23_CAP_1
VDDARM23_CAP_2
VDDARM23_CAP_3
VDDARM23_CAP_4
VDDARM23_CAP_5
VDDARM23_CAP_6
VDDARM23_CAP_7
VDDARM23_CAP_8
VDDSOC_CAP_1
VDDSOC_CAP_2
VDDSOC_CAP_3
VDDSOC_CAP_4
VDDSOC_CAP_5
VDDSOC_CAP_6
VDDSOC_CAP_7
VDDPU_CAP_1
VDDPU_CAP_2
VDDPU_CAP_3
VDDPU_CAP_4
VDDPU_CAP_5
VDDPU_CAP_6
VDDPU_CAP_7
VDD_CACHE_CAP
{NVCC_CACHE_POWER}
VDDHIGH_CAP_1
VDDHIGH_CAP_2
VDD_SNVS_CAP
NVCC_LCD
NVCC_CSI
NVCC_MIPI
NVCC_EIM0
NVCC_EIM1
NVCC_EIM2
NVCC_ENET
NVCC_GPIO
NVCC_PLL_OUT
NVCC_RGMII
NVCC_SD1
NVCC_SD2
NVCC_SD3
NVCC_NANDF
NVCC_JTAG
GPANAIO
FA_ANA
VDD_FA
1V1
VDDSOC_CAP
VDDHIGH_CAP
2V5
VDD_3V3_AP
DDR_1V5
D17
1N5819HW
R1
0R
R2
0R/NC
R3
0R
R4
0R/NC
C2
C3
C4
C5
C8
C11
C13
C14
C15
C17
C18
C21
C22
C23
C24
C25
C26
C29
C32
C35
C36
C37
C38
C40
C41
C42
C47
C48
C49
C50
C52
C53
C54
C55
C56
C57
C60
C61
C62
C65
C66
C67
C69
C70
C71
C72
C73
C74
C77
C78
C79
C80
C81
C84
C297
0.22uF/16V
22uF/6.3V
0.1uF/25V
GND
MX6 power domains
under-BGA decoupling
(These capacitors are part of i.MX6 DDR3
Power Domain. They decouple pins shown
on Page 4 of these schematics)
NOTE:
The VDDARM_CAP and VDDARM23_CAP rails have been optimized for use with
the i.MX 6 Quad and i.MX 6 DualLite processors.
To achieve the lowest power mode (preventing internal leakage) when using
the i.MX 6 Dual and the i.MX 6 SoloLite
processors, VDDARM_CAP should be split from VDDARM23_CAP and the
VDDARM23_CAP pins should be connected to ground.
This can be done on a single board configured for use with all four
processors by placing a Zero Ohm resistor between the
VDDARM_CAP and VDDARM23_CAP rails (in place of the straight net
connection). To use the board with different processors,
populate the resistor when using Quad and DualLite processors and
depopulate resistor when using Dual and SoloLite
processors. When using Dual and SoloLite processors, depopulate the
capacitors attached to VDDARM23_CAP pins and
replace one of the capacitors with a zero Ohm resistor to short pins to
ground. The configuration in this schematic will work with
all four processors, but will not result in the most power optimized
configuration for the i.MX 6 Dual and Solo processors.
LAYOUT NOTE:
It is critical that the bulk and decoupling capacitors placed
on the VDDARM_CAP, VDDARM23_CAP, VDDSOC_CAP
and VDDPU rails be placed directly underneath the processors.
Development testing has shown that proper
placement of the capacitors can reduce ripple on the voltage
rails by as much as 50% compared to placing
capacitors outside the physical boundaries of the processor.
These will result in more stable processor operations.
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A2
Document Number
CPU POWER
Rev
3
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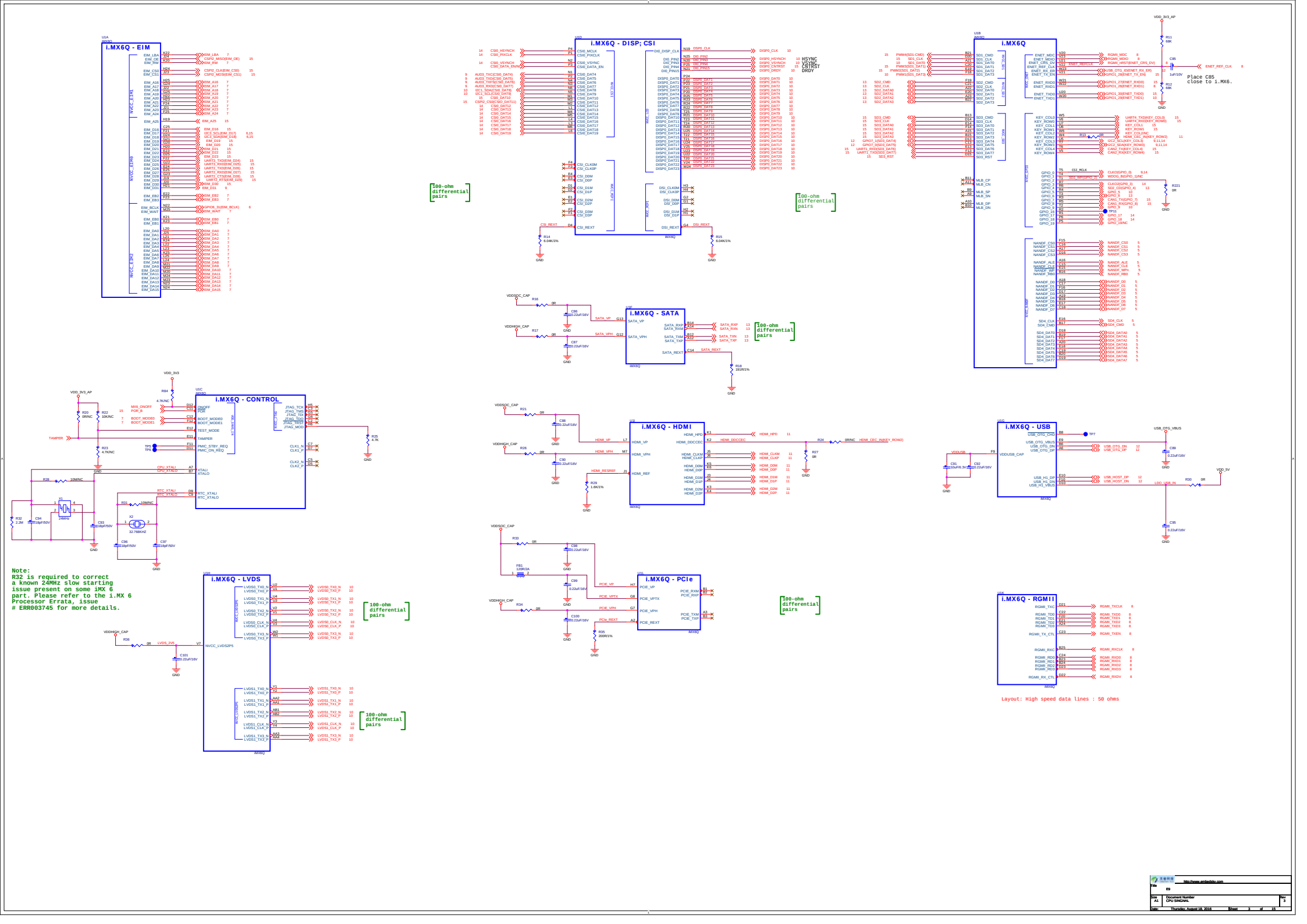
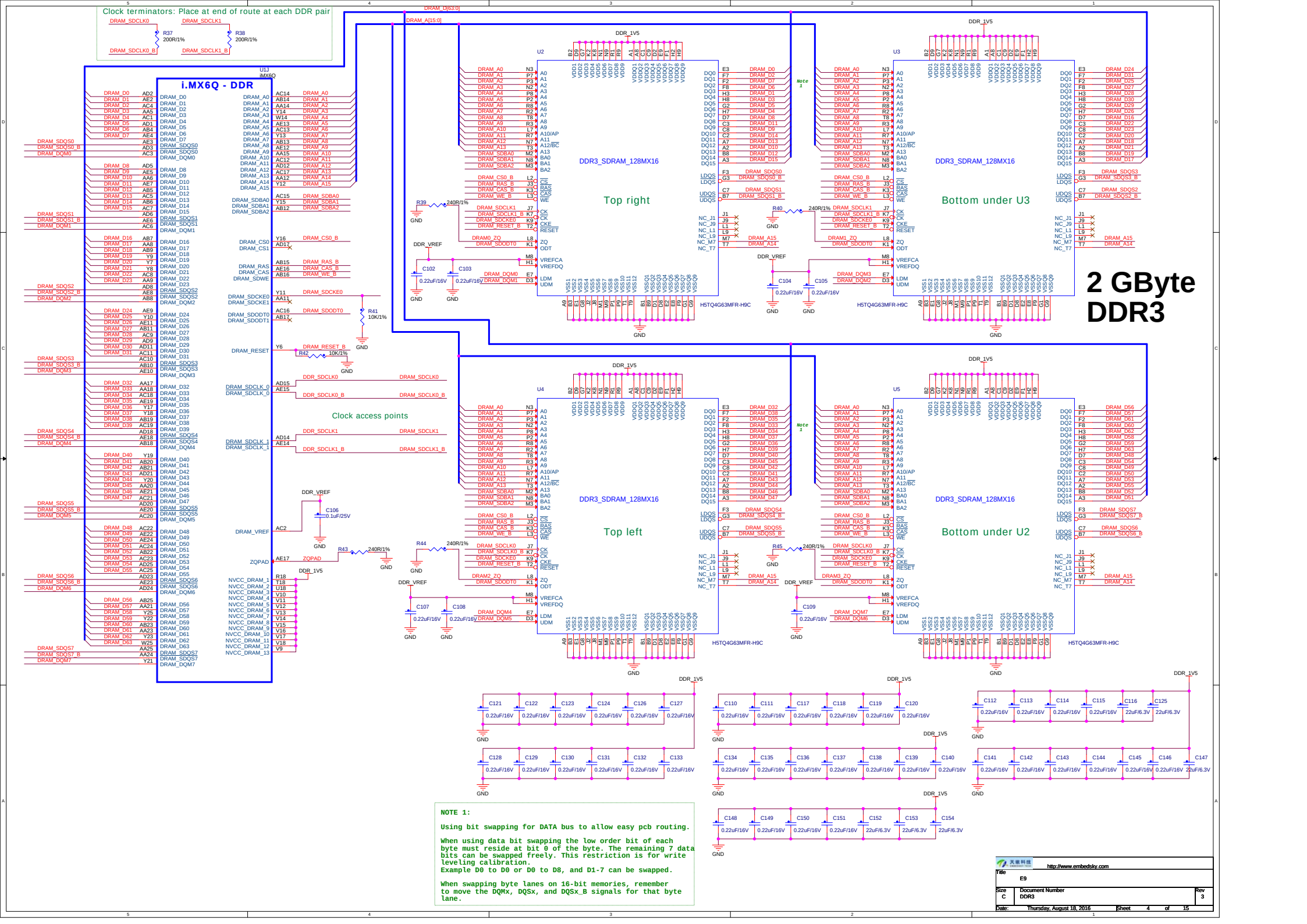

i.MX6Q - EIM
i.MX6Q - DISP; CSI
i.MX6Q
i.MX6Q - SATA
i.MX6Q - CONTROL
i.MX6Q - HDMI
i.MX6Q - USB
i.MX6Q - LVDS
i.MX6Q - PCIe
i.MX6Q - RGMII
HSYNC
VSYNC
CNTRST
DRDY
100-ohm differential pairs
Place C85 close to i.MX6.
Note:
R32 is required to correct a known 24MHz slow starting issue present on some iMX 6 part. Please refer to the i.MX 6 Processor Errata, issue # ERR003745 for more details.
Layout: High speed data lines : 50 ohms


Clock terminators: Place at end of route at each DDR pair
DRAM_SDCLK0
DRAM_SDCLK1
R37 200R/1%
R38 200R/1%
DRAM_SDCLK0_B
DRAM_SDCLK1_B
i.MX6Q - DDR
U1J iMX6Q
DRAM_D[63:0]
DRAM_A[15:0]
U2
U3
U4
U5
DDR3_SDRAM_128MX16
Top right
Bottom under U3
Top left
Bottom under U2
H5TQ4G63MFR-H9C
Note 1
2 GByte DDR3
Clock access points
R39 240R/1%
R40 240R/1%
R41 10K/1%
R42 10K/1%
R43 240R/1%
R44 240R/1%
R45 240R/1%
DDR_VREF
DDR_1V5
GND
NOTE 1:
Using bit swapping for DATA bus to allow easy pcb routing.
When using data bit swapping the low order bit of each byte must reside at bit 0 of the byte. The remaining 7 data bits can be swapped freely. This restriction is for write leveling calibration.
Example D0 to D0 or D0 to D8, and D1-7 can be swapped.
When swapping byte lanes on 16-bit memories, remember to move the DQMx, DQSx, and DQSx_B signals for that byte lane.
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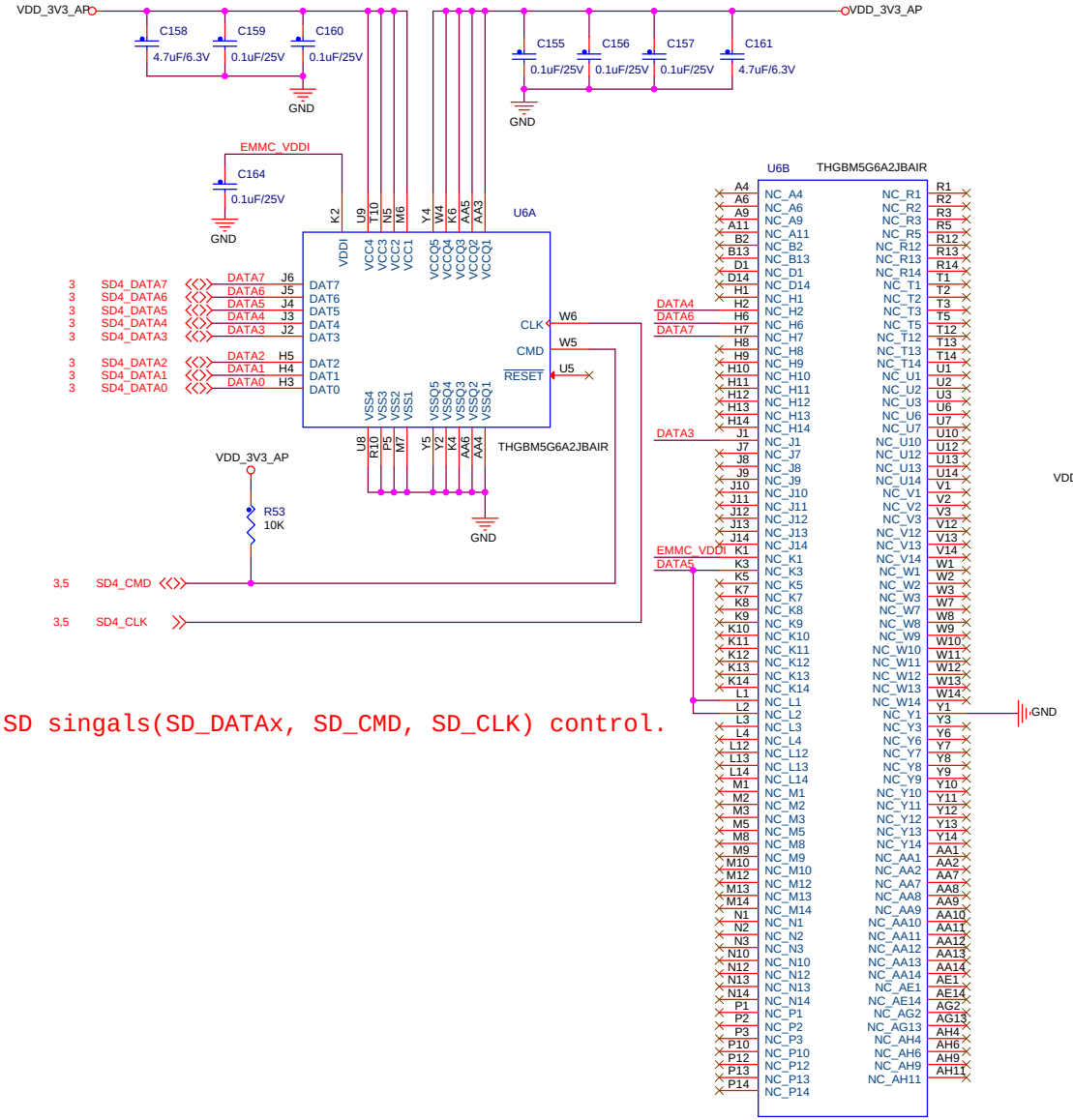
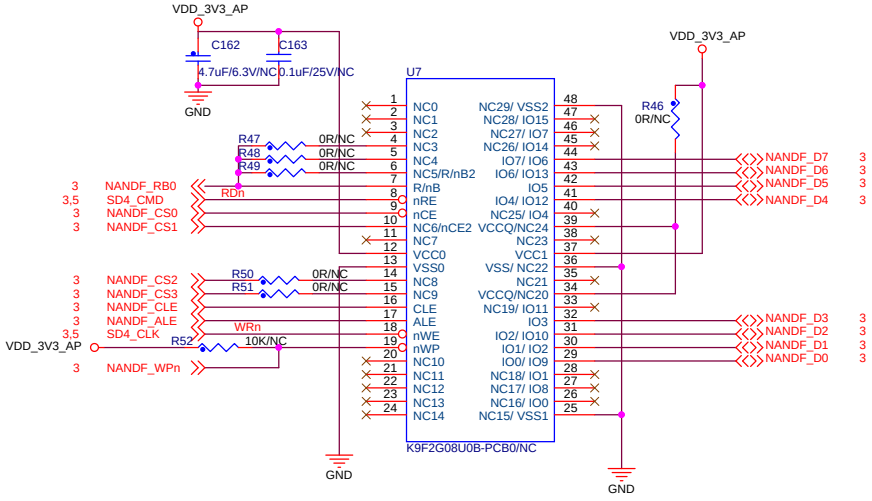
8GB eMMC MEMORY



NAND Flash memory



Layout:
50ohm, SD singals(SD_DATAx, SD_CMD, SD_CLK) control.

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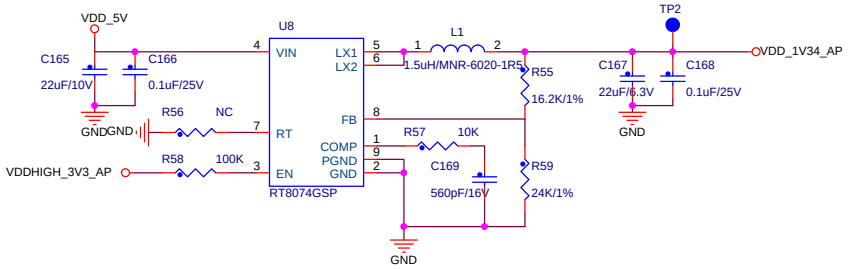
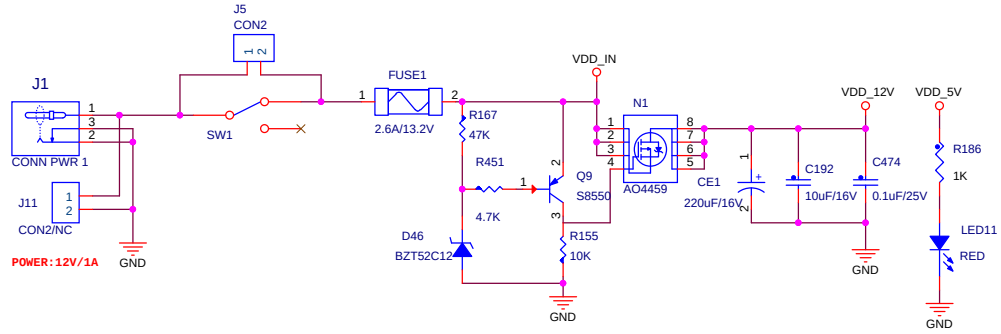
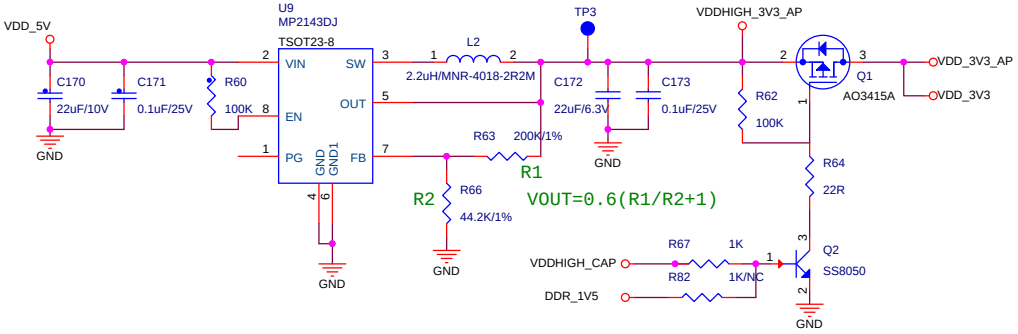
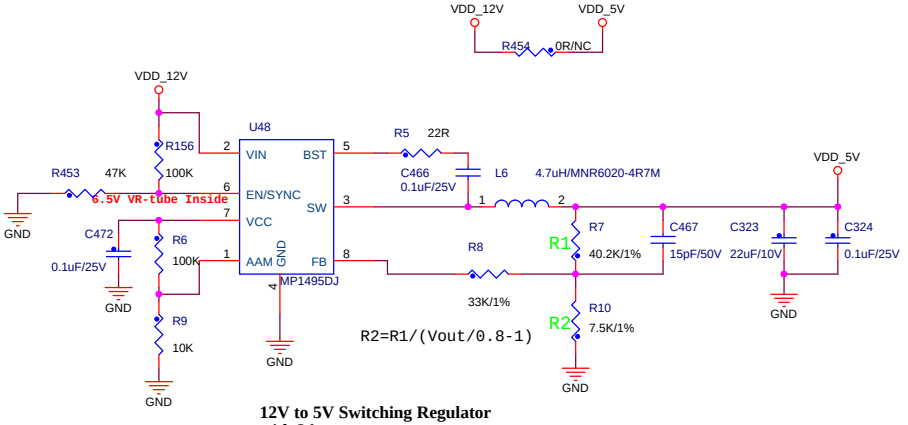
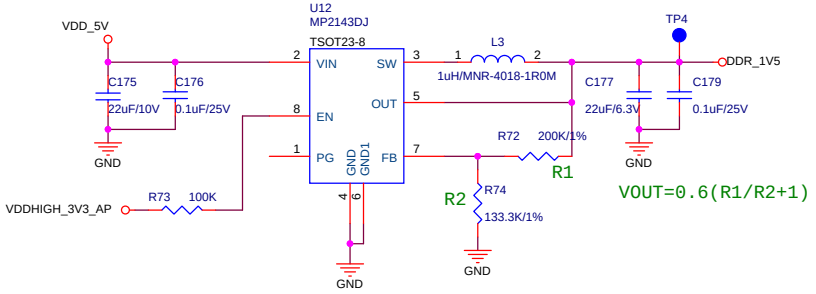


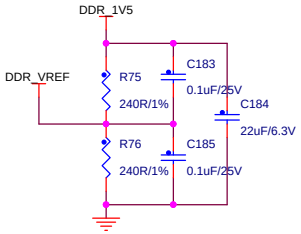


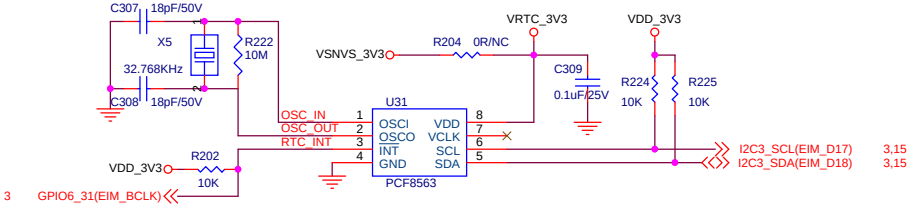




12V to 5V Switching Regulator with 2A output current







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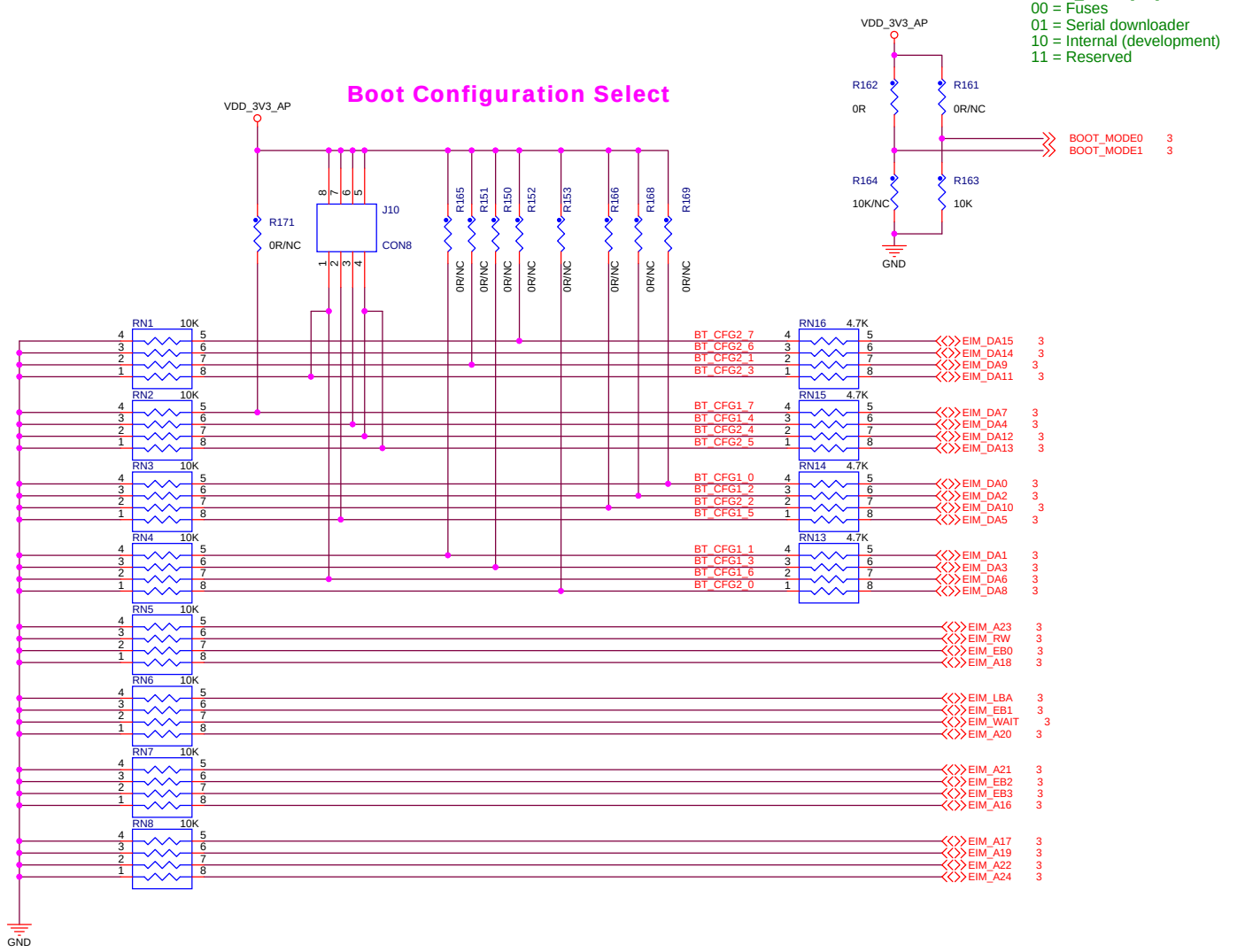
BOOT_MODE[1:0] SETTINGS
00 = Fuses
01 = Serial downloader
10 = Internal (development)
11 = Reserved



Boot Configuration Select

G1-6 G2-3	G1-5	G1-4	G2-5 G2-4	MODE
1	0	0	0	SD2_Boot
1	1	0	1	eMMC_Boot
0	1	1	0	DownLoad

BT_CFG2_3 BT_CFG1_6 | BT_CFG1_5 | BT_CFG1_4 | BT_CFG2_4 BT_CFG2_5

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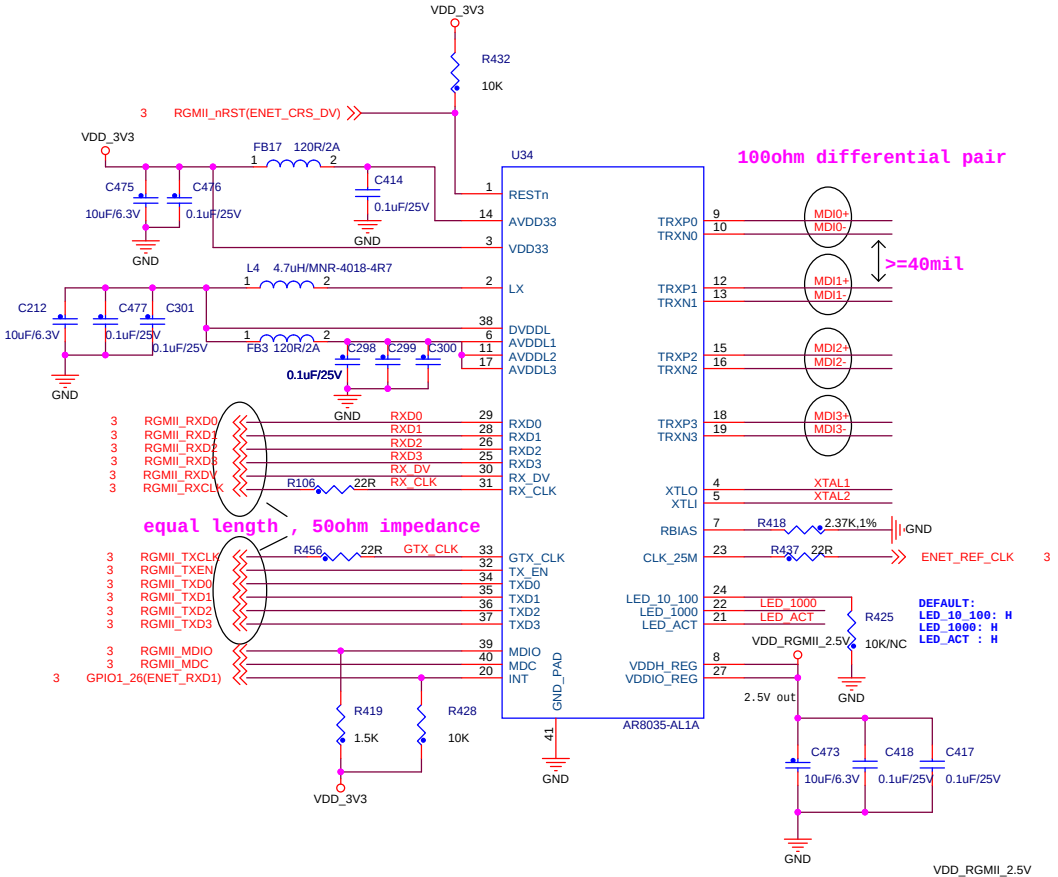
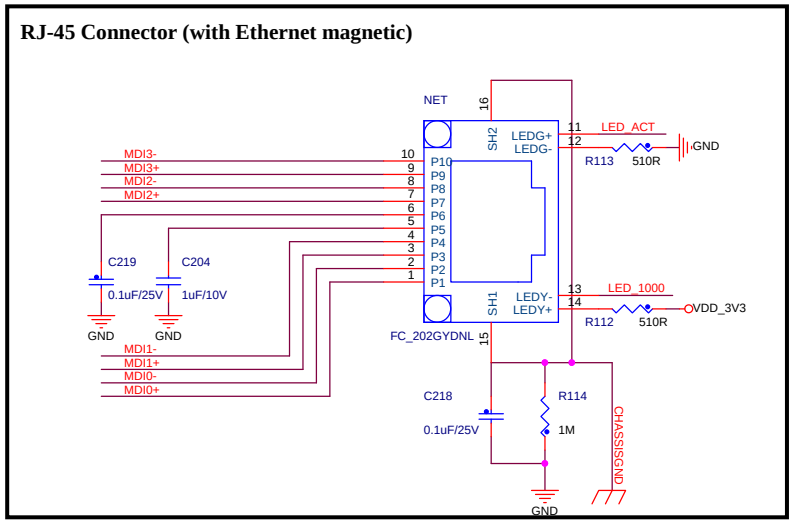
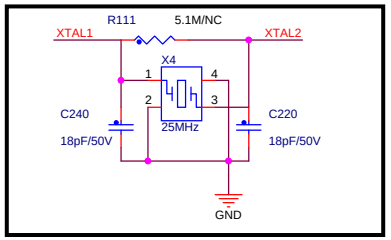
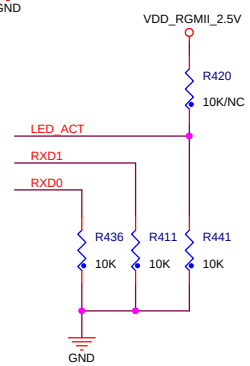




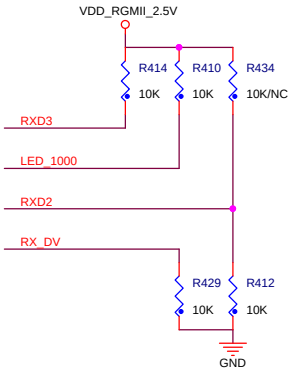
***Note:**
L5 (4.7uH) should be as close to AR8035-AL1A LX pin (within 200mils).
TheCT14 and C424 capacitors as close to L5 if possible.

25MHz +- 50ppm Crystal

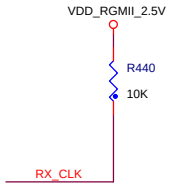




PHY address:100
CHANGE:000



MODE[0:3]:
1110:RGMII,PLLON,INT
1100:RGMII,PLLOFF,INT



RX_CLK:
0:1.5V I/O
1:1.8V I/O
2.5V I/O:PULL UP/DOWN

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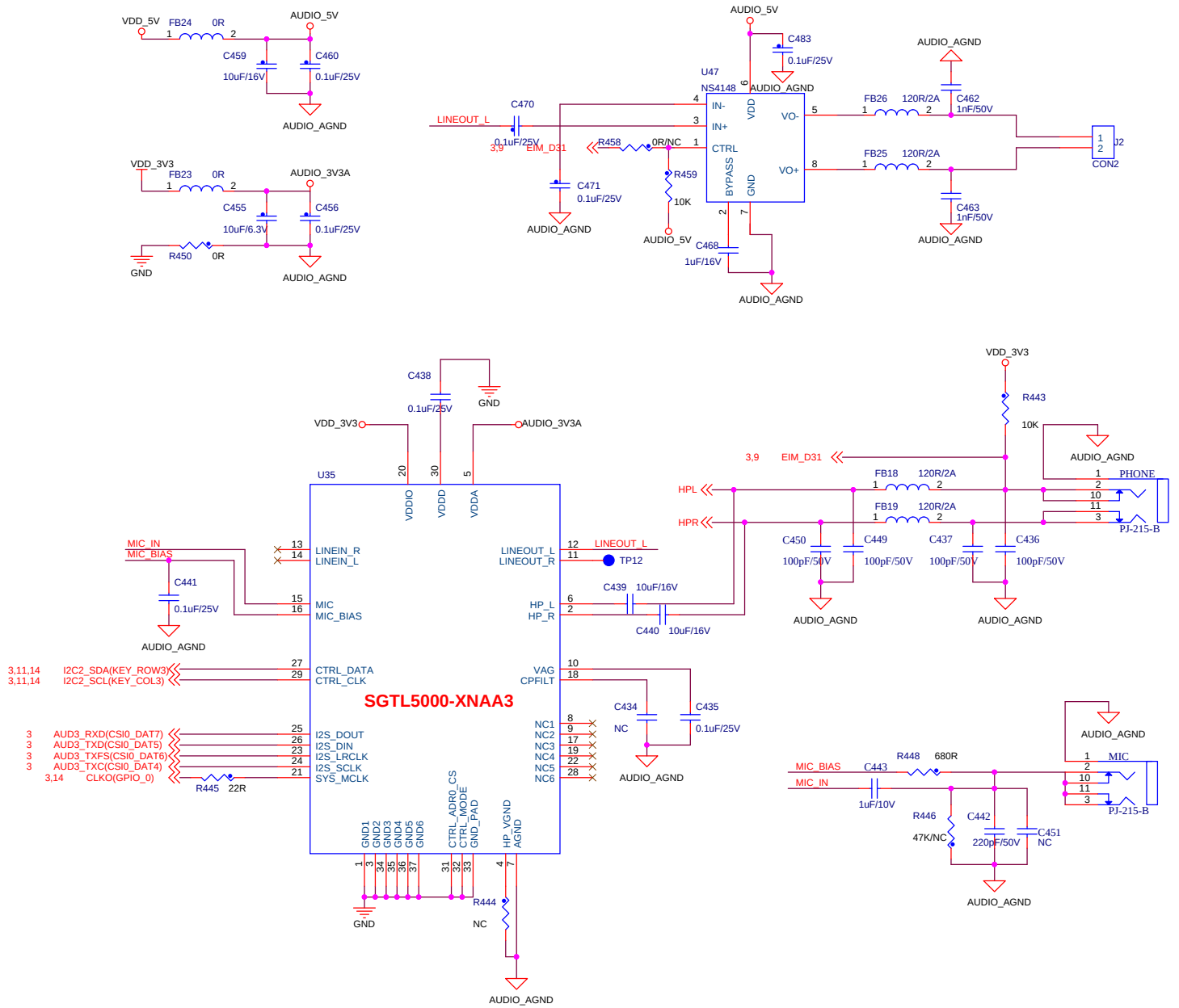

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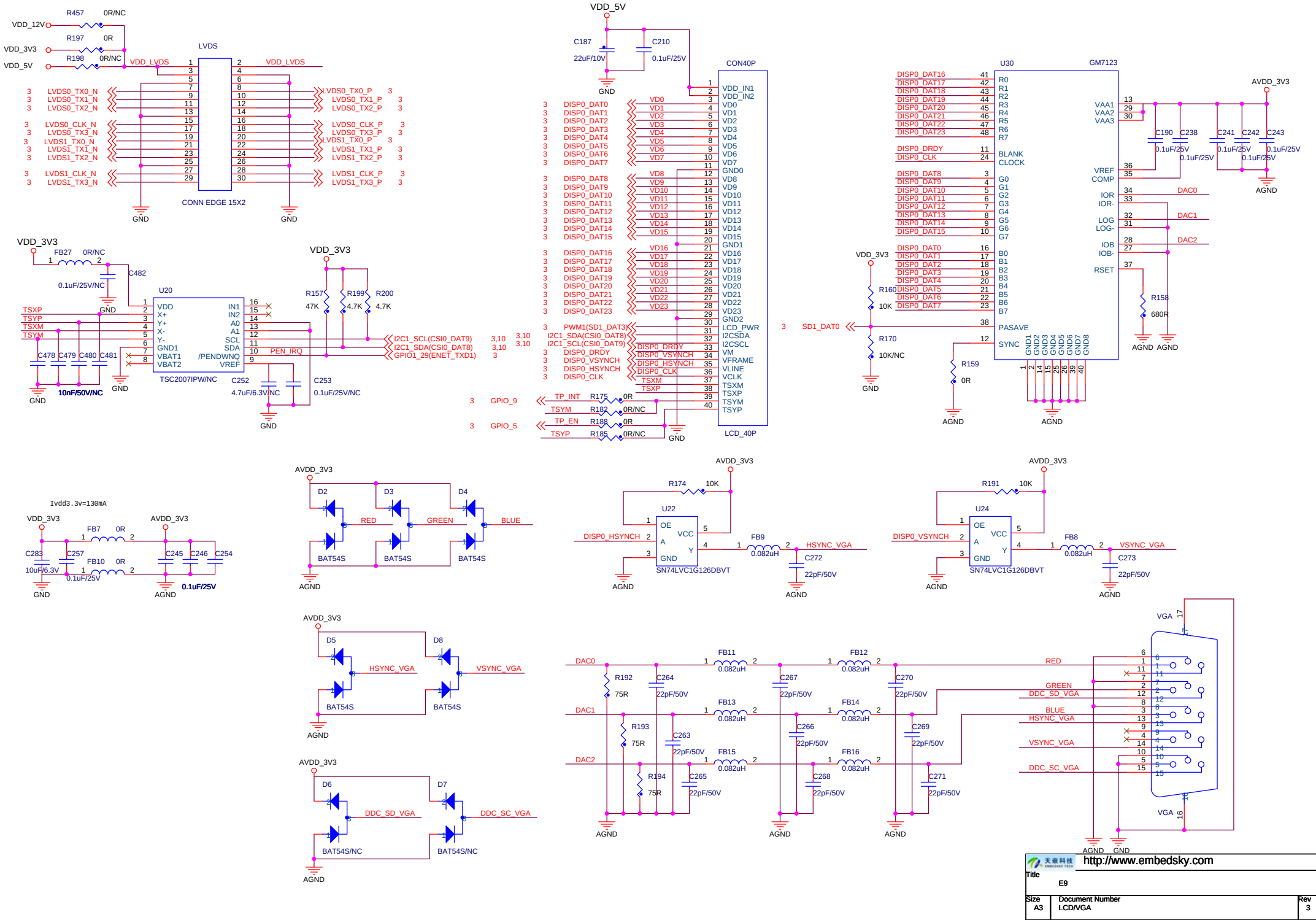

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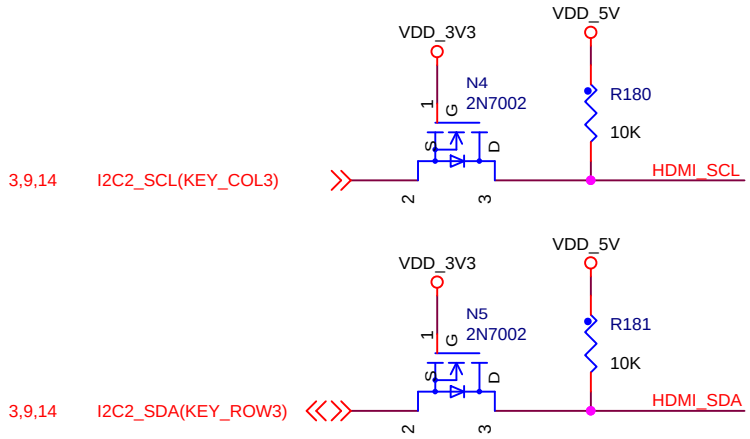
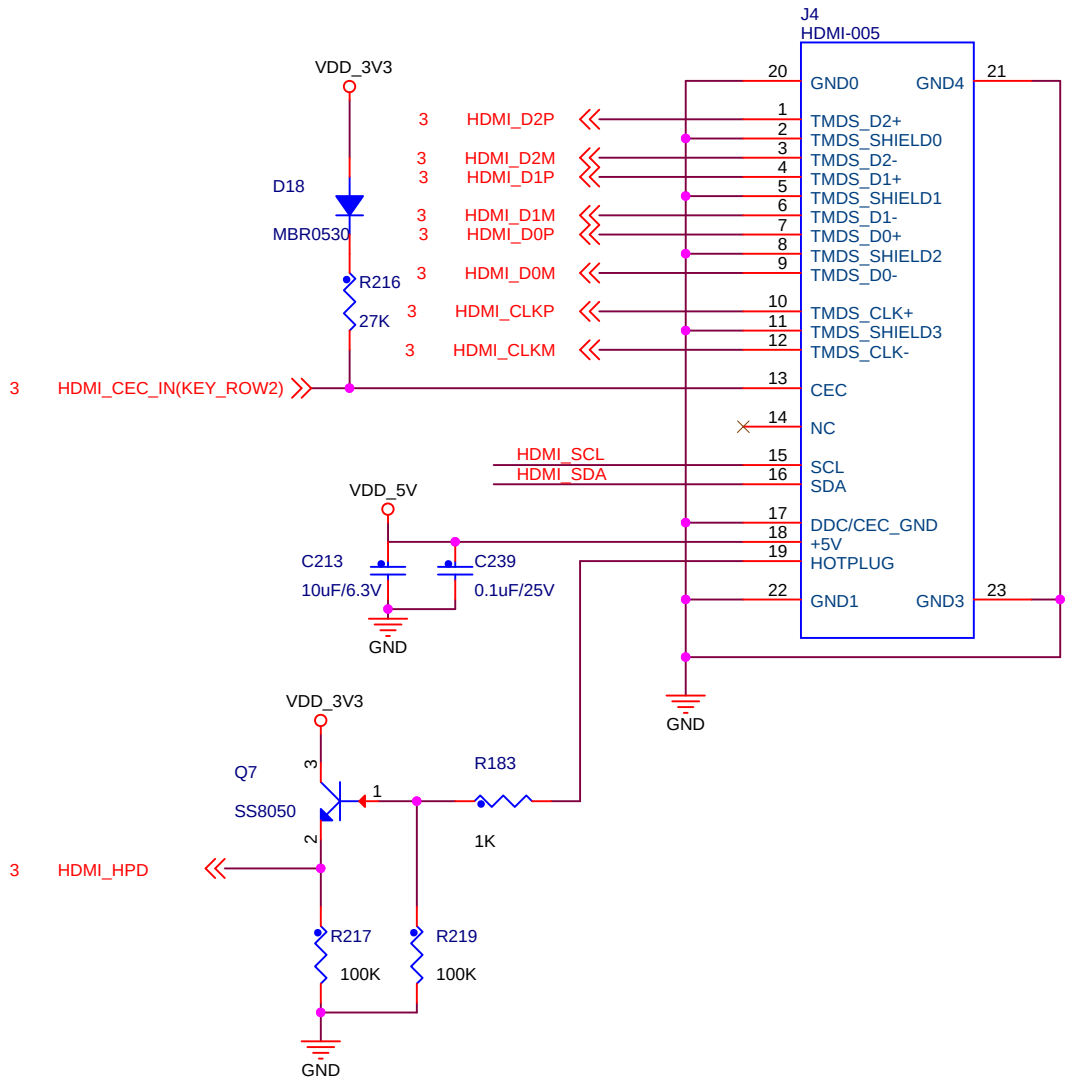
HDMI



HDMI A TYPE



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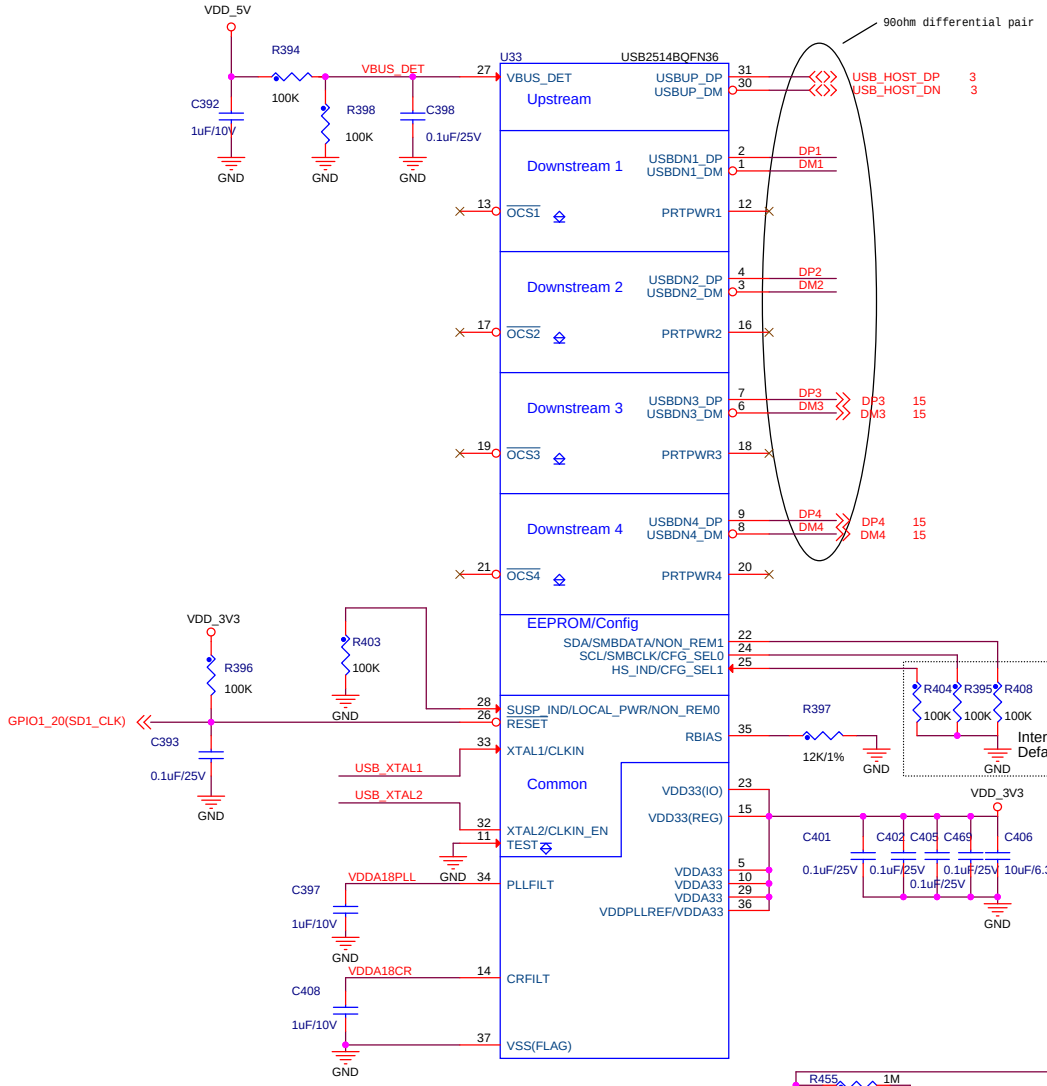
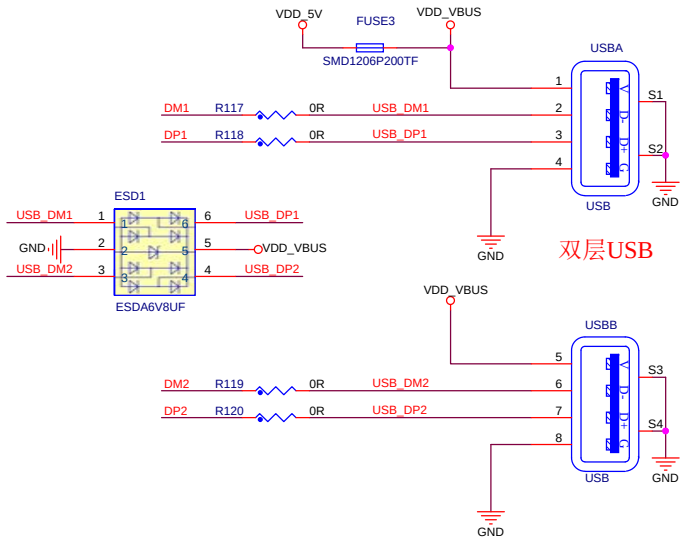
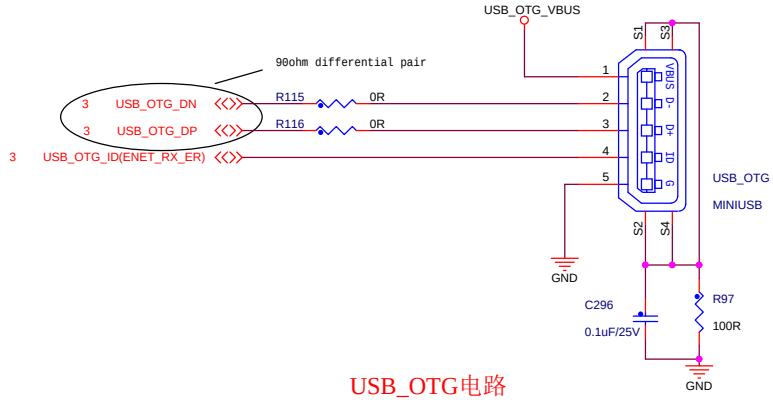
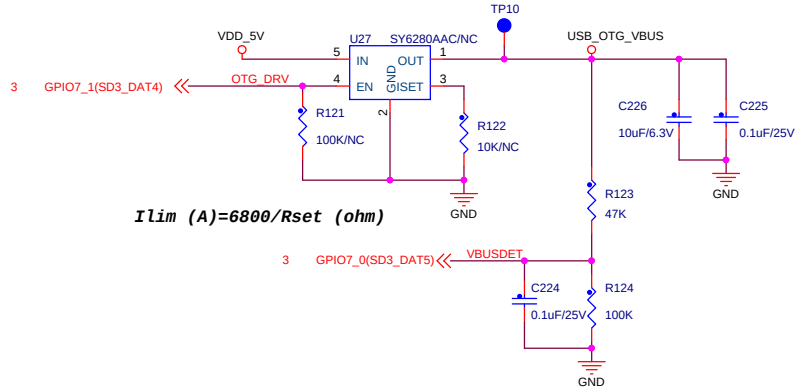


PRTPWR[4:1] Status
1 : Battery charging feature is supported for port x
0 : Battery charging feature is not supported for port x





USB_OTG电路



Ilim (A)=6800/Rset (ohm)

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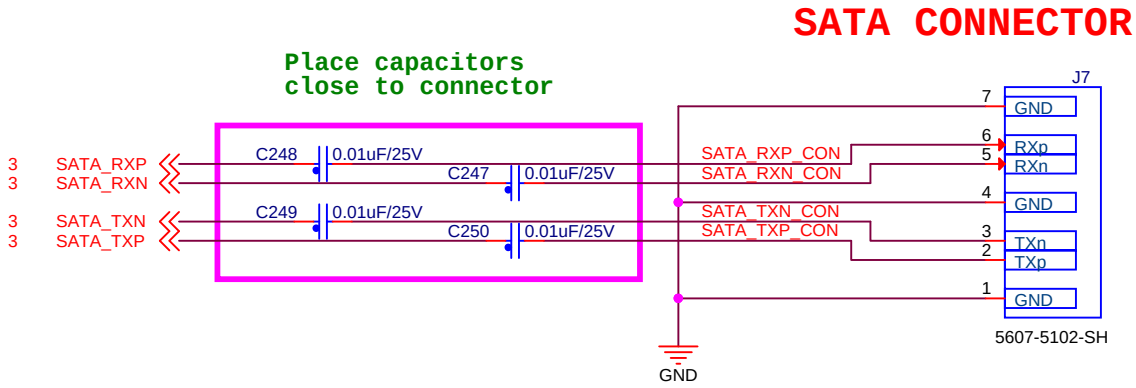
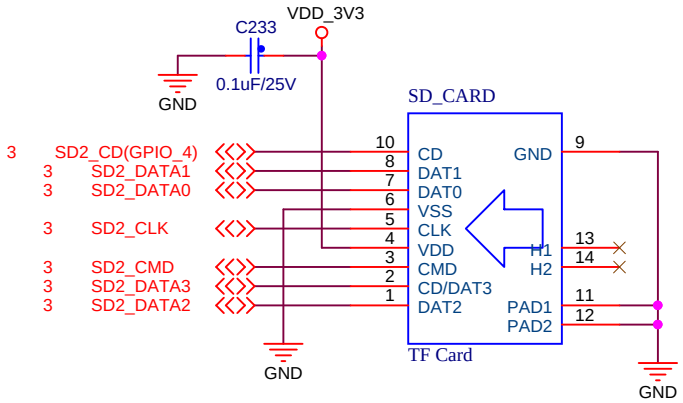
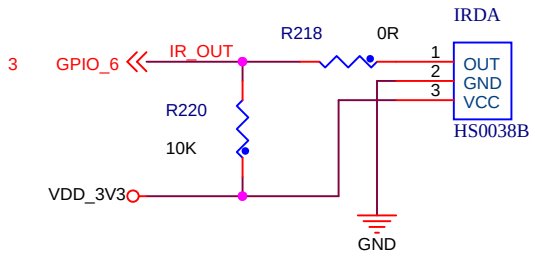
SATA CONNECTOR





红外电路



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Size: A4	Document Number: TF/SATA	Rev: 3
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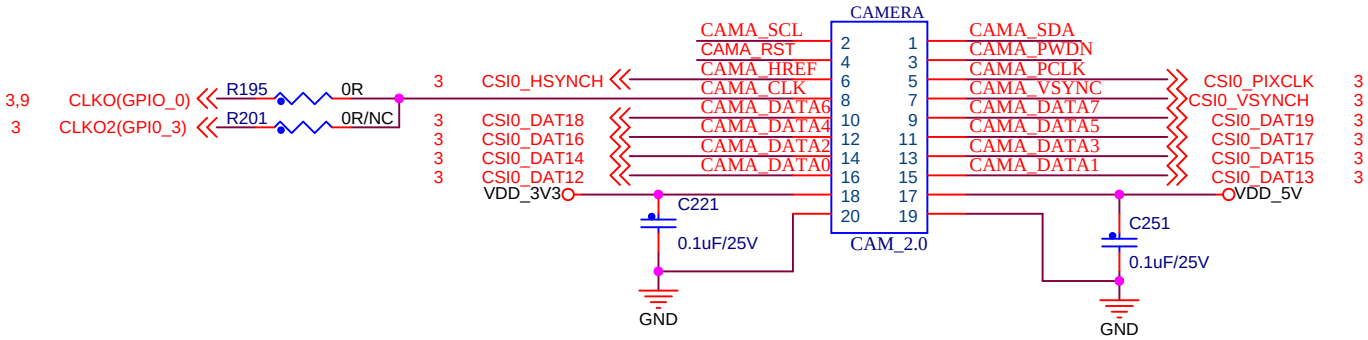
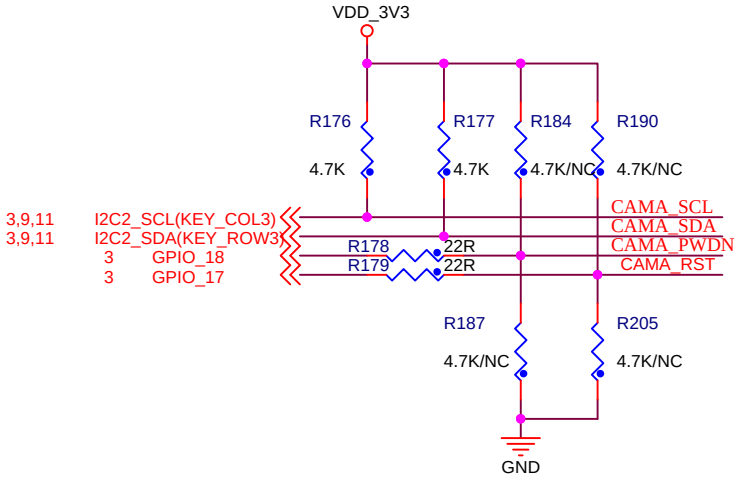
CAMMER A





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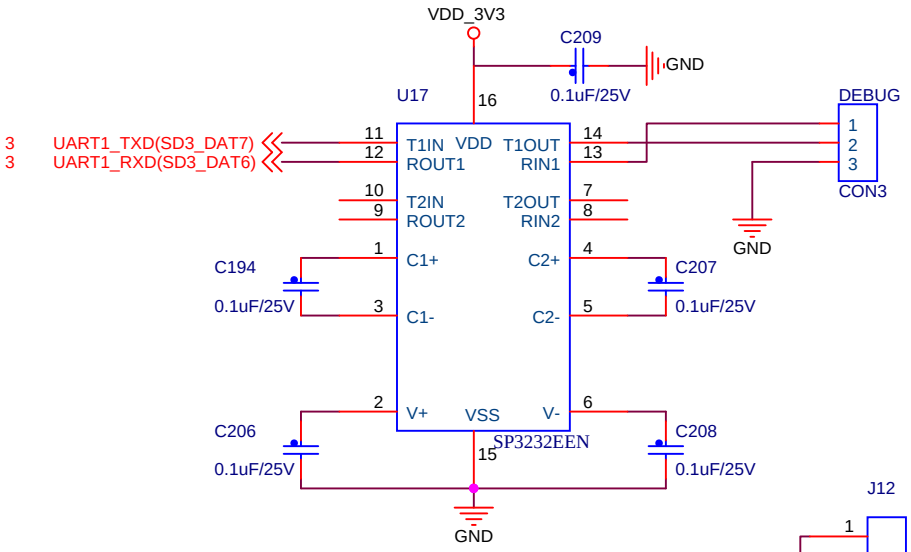
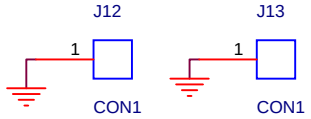
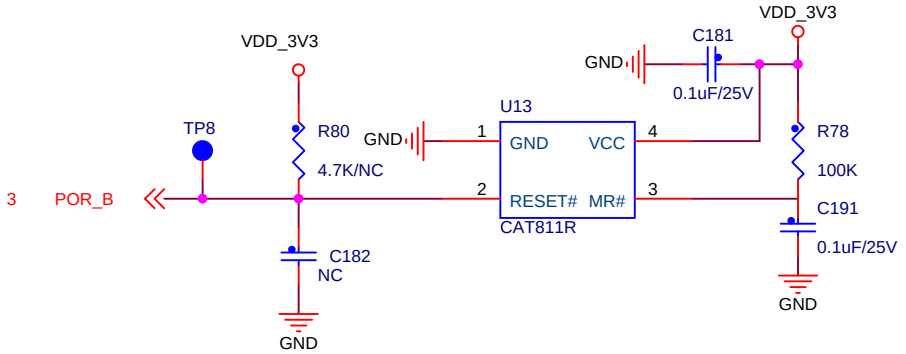
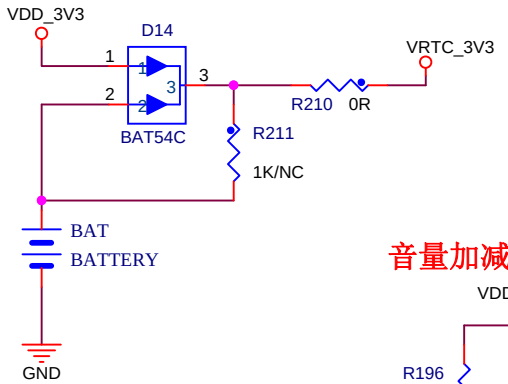






RTC电路



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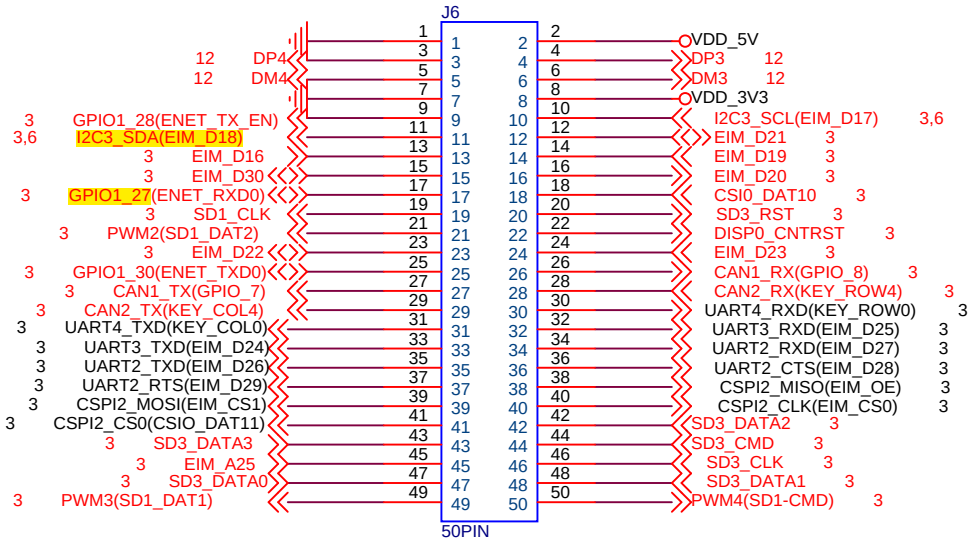

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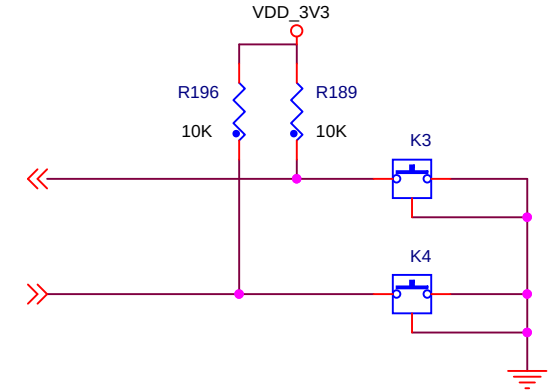

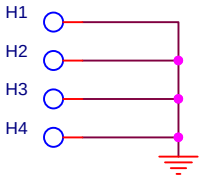

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