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5	Board-to-Board Connector
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Atheros Ethernet PHY Daughter Card

Revision D

Consumer devices were utilized in this design when lead time for equivalent automotive-grade devices conflicted with production schedules.
Freescale suggests consulting component suppliers for equivalent automotive-grade device information.

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Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

ICAP Classification: FCP: FIUO: PUBI: X

Designer: David B	Drawing Title: Atheros Ethernet PHY		
Drawn by: David B.	Page Title: Cover		
Approved: Apps and Test Team	Size C	Document Number SCH-27953 PDF: SPF-27953	Rev D
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System Block Diagram

Board set for customers shown below.

Atheros
Ethernet PHY Card - RGMII

Schematic SCH-27953
Part No. IMXAI2ETH-ATH

Broadcom
Ethernet PHY Card - RGMII

Schematic SCH-27954
Part No. IMXAI2ETH-BRC

Broadcom
Ethernet Switch Card - RGMII

Schematic SCH-27955
Part No. IMXAI2SWCH-BRC

Components with "Hard_Location" displayed are similar in function for the 3 daughter cards shown above. These components have the same reference designators on the 3 daughter cards shown above.

MX6 Quad CPU2 Card

Schematic SCH-27925
Part No. MCIMX6QAICPU2

MX6 DualLite CPU2 Card

Schematic SCH-27xxx
Part No. MCIMX6DLAICPU2

Each CPU2 Card is shipped as a kit which includes the Atheros PHY Daughter Card.

Automotive Base Board

Schematic SCH-26662
Part No. MCIMXABASEV1

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Drawing Title: **Atheros Ethernet PHY**

Page Title: **System Block Diagram**

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Ethernet PHY

drivers are included in the receive path due to long signal paths and board-to-board connector. Adopters should place the PHY and processor on the same board, and eliminate the drivers. Refer to Atheros documentation for additional guidance.

RGMII Single-Ended Signals = 50 ohm

Default = 1.5 V
PHY software-configurable option = 1.8 V
Requires 1.8 V regulator configuration on sheet 4.

Fed to configuration resistors below

Optional feed from external regulator for variable voltage

Local Supply 2.7 V per Atheros spec

Local Supply 1.1 V

Local Supply

100 ohm diff pairs

Power-on reset and software reset provided by CPU Card.

MDIO pull-up on CPU2 Card.

3.3 V Signal Swing feed to CPU Card.

No longer used; REFCLK sourced from processor.

Ra, Rb, and Ca level shift the 125 MHz reference clock to accommodate the 2.7 to 3.3 V supply difference. (Unique to Atheros PHY)

Software should turn off MX6 on-chip pull-up and keeper for optimum operation without driver chip.

~ 2.7 V Signal Swing

EMI Filter Reserved 470pF for LED

2.37k used for BOM consolidation

1 Gb/s

L A Y O U T N O T E
Mount near pin 5 of each NC7WV16 driver chip.

Power-on Strapping Pins

Addr = 1

PHYADDRESS0	RXD0	R21 DNP 10K
PHYADDRESS1	RXD1	R17 10K
MODE2[1]	RXD2	R24 10K
MODE2[3]	RXD3	R30 10K
MODE2[2]	RGMII_RX_CLK	R14 10K
MODE2[0]	RXDV	R15 10K
SEL_GPIO_INT	LED_1000	R505 10K
ANA_MOD	LED_ACT	R506 10K

Pin 5 mode: 0: INT ; 1:GPIO

Select the core voltage level: 0:1.1V, 1:1.2V

MODE2[3:0]

(Default assemble: 0000)
1100 BaseT, RMII1;
1101 BaseT, RMII2;
1110 100X, RGMII, 75OHMS;
1111 100X, TRANS, 75OHMS;
0000 BaseT, RGMII;
0001 BaseT, SGMII;
0010 1000X, RGMII, 50OHMS;
0011 1000X, RGMII, 75OHMS;
0100 1000X, TRANS, 50OHMS;
0101 1000X, TRANS, 75OHMS;
0110 100X, RGMII, 50OHMS;
0111 100X, TRANS, 50OHMS;
Others Reserved

This design utilizes a consumer device. For the compatible automotive-grade PHY, consult Atheros.

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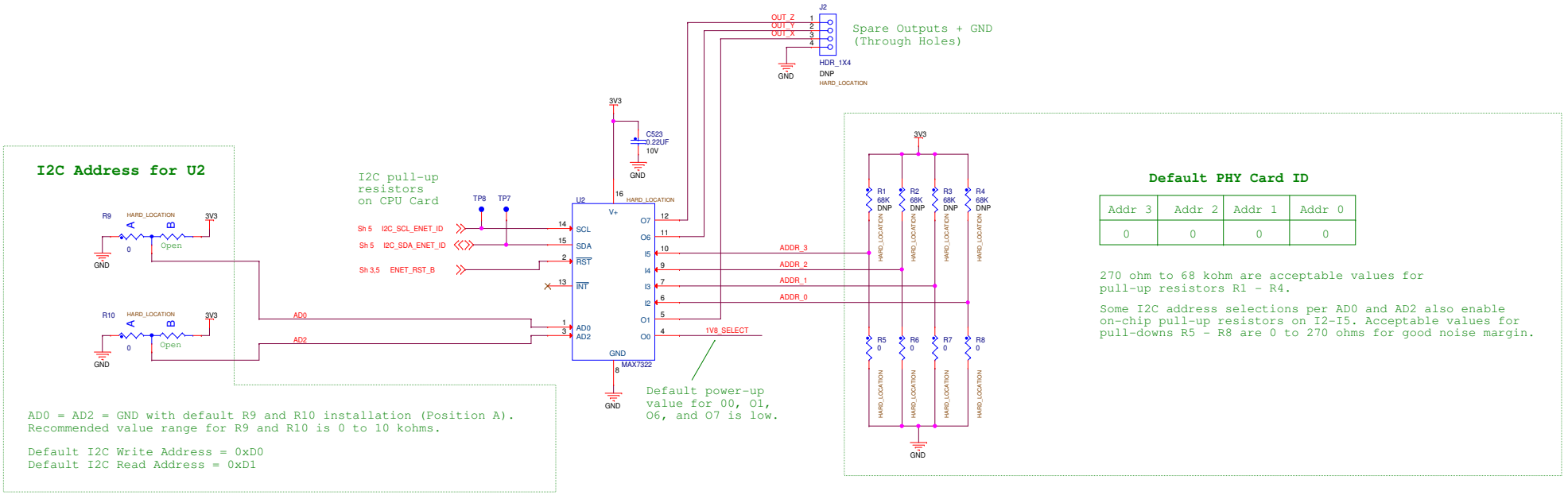
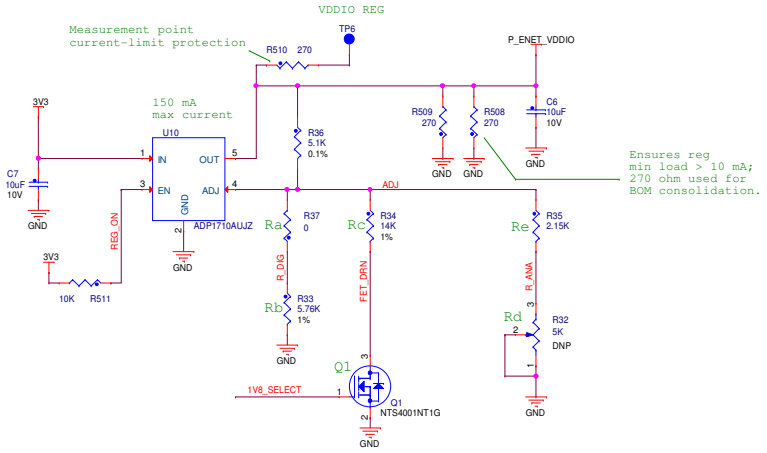
Card Identification and Control



Regulator --- 1.5, 1.8 V, Variable



RGMII I/O	Mode	Ra	Q1	Rd	Note
1.5 V	Digital Control	Install	Turned off	Remove	Hardware default
1.8 V	Digital Control	Install	Turned on	Remove	Also configure PHY for 1.8 V
1.4-2.7 V	Analog Variable	Remove	Turned off	Install	Freescale characterization use only Install Rx at top of sheet 3

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Drawing Title: **Atheros Ethernet PHY**

Page Title: **Card Identification and Regulator**

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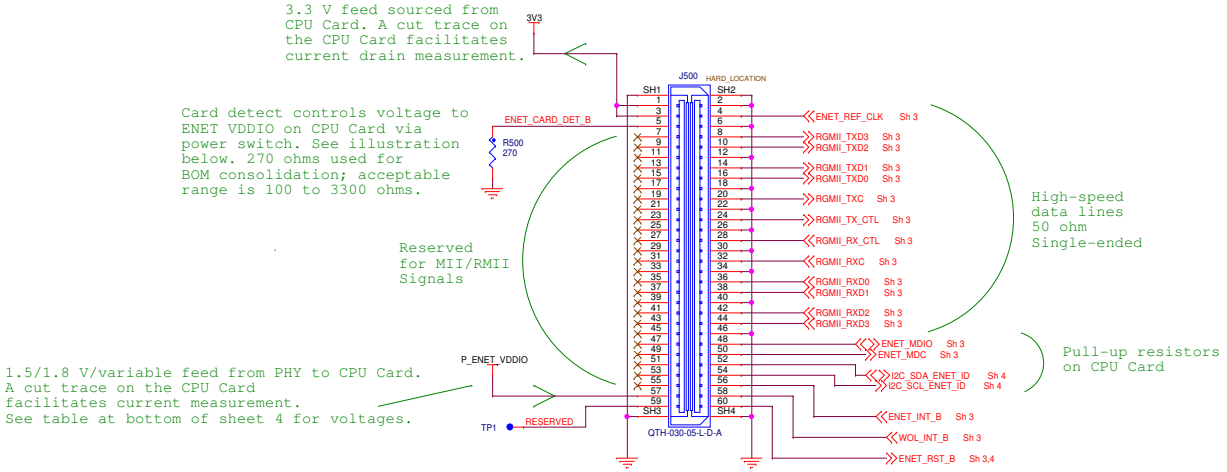
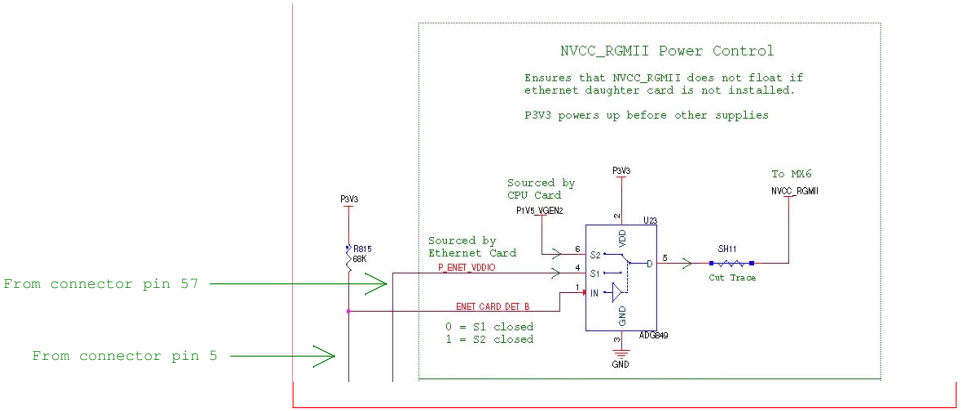
Board to Board Interface

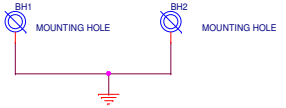


Connector pin assignment per Agile document DOC-01898.

Mating connector part number: QSH-030-01-L-D-A-K-TR

Mating height to CPU Card = 19 mm (clearance required by CPU Card). See Notes sheet for detail.





Power switch implementation on CPU2 Card

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Page Title: **Board-to-Board Connector**

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A	Initial release.	7/29/13
B	Sheet 3 - Deleted 3 unused resistors from Power-on Strapping area to make room for new ICs. Deleted series passives on all RX lines. Added drivers on ENET_REF_CLK and all RX lines. Added TP3 (on top) since P_ENET_VDDIO caps are on bottom. Updated J1 center-tap caps to DNP to align with CPU1. Changed 2V5_RGMII net to 2V7_RGMII to match updated Atheros data sheet. Change D1 resistor from 510 ohms to two 2.37k for BOM consolidation. Changed series ENET_REF_CLK resistor to 20 ohms for drive control. Sheet 4 - Changed J2 from 1x5 to 1x4 to match other ENET daughter cards. Sheet 5 - Updated J500.59 net from "Spare" to "5V0" to match other ENET cards. Changed J500.5 resistor from 510 ohms to 270 ohms for BOM consolidation.	10/14/13
BX1	Sheet 3 - Isolated VDDIO power on PHY; added option resistor. Added DNP pulldown to RXD0 address selector to accommodate dual ENET cards. Sheet 4 - Added regulator to supply added RGMII drivers. Accommodated VDDIO for MX6 1.5 V production, future 1.8 V chips, and characterization variable voltage. Sheet 5 - Changed J500.59 from 5V0 to Reserved.	11/1/13
BX2	Sheet 4 - Added VDDIO test point and series resistor. Added 270 ohm resistors to ensure min load for reg.	11/5/13
BX3	Backannotated.	11/6/13
C	Incremented to rev C after Fab Readiness Review.	11/11/13
C1	Sheet 3 - Corrected R26 BOM error. Changed from DNP to Installed.	1/15/14
D	Sheet 3 - Changed R26 and R27 to DNP because REFCLK now sourced from processor. Sheet 5 - Added two plated mounting holes to gnd, BH1 and BH2, for FCC compliance.	4/21/14

Internal Design
No prototypes built

1. Unless Otherwise Specified:
   All resistors are in ohms, 5%.
   All voltages are DC.
   All polarized capacitors are aluminum electrolytic.

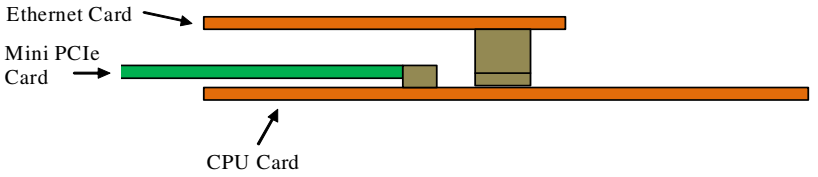
2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals
   Green Text Denotes - Extra Notes to be considered.

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

Board Assembly



CPU Card attaches to Automotive Base Board per Sheet 2.

Assembly Drawing Info
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Two board standoffs are required.
SAMTEC SO-1915-05-01-01
Freescale internal part number 280-76823

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Drawing Title: **Atheros Ethernet PHY**

Page Title: **Notes and Revision History**

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