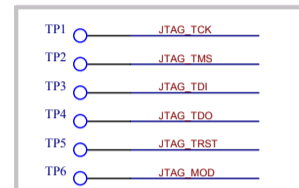


SOC CONTROL

JTAG PORT



POWER-ON/OFF

DESIGN NOTE:
PMIC asserts POR_n when all PWR rails are OK, internally Pulled-Up (100K) to SNVS then, 2ms after the last rail on the sequence is up, PMIC releases POR_n (Open Drain) and remains to +SNVS

DESIGN NOTE:
Internally Pulled-Up to +SNVS, this button is read by the iMX PMU which includes de-bouncing logic and detects both large and short "shorts" to ground to power ON and OFF the system

Place to control ONOFF from Bios MCU

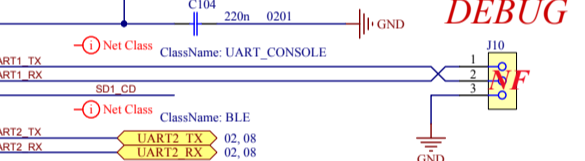
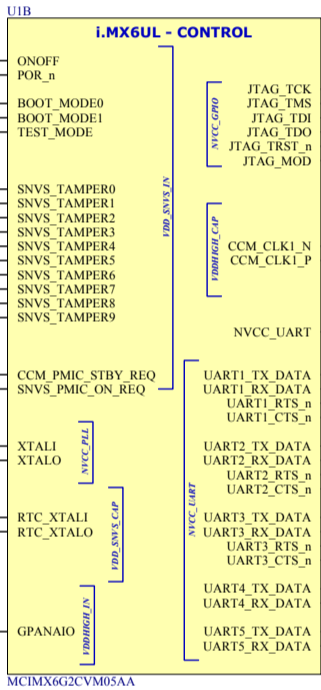
DESIGN NOTE:
Outputs to PMIC_ON_REQ and PMIC_STBY_REQ from iMX6 PMU (see TRM page 345/367)
Pulled up and down by iMX T9 (both 100K) to +3.0V_SNVS and GND respectively
PMIC_STBY_REQ currently unused

DESIGN NOTE:
Resistor R20 from CPU_XTALI to GND is required to correct a known 24MHz slow starting issue present on some iMX6 part. Please refer to the iMX6 Processor Errata

DESIGN NOTE:
UART1_RTS_B is configured as SD1_CD signal during SD boot!
Table 8-18 (SD/MMC IOMUX Pin Configuration) of the iMX6 UL RM (Rev. 1, 04/2015).

SOC NOTE 1:

- POR_B – configurable on-chip pullup
- ONOFF – on-chip pullup
- BOOT_MODE0 – on-chip pulldown
- BOOT_MODE1 – on-chip pulldown
- TAMPER – on-chip keeper
- PMIC_STBY_REQ – configurable output
- PMIC_ON_REQ – push-pull output
- TEST_MODE – on-chip pulldown



Title		
EBMULDPB-REV A10		
Size	Number	Revision
A3	Ignacio Diz Castro	
Date:	23/10/2017	Sheet of
File:	C:\Proyectos\021 - SOC - CONTROL\1.1\BOM\SWN_I2C, JTAG_SchDoc	