SOC CONTROL

POWER-ON/OFF

+3.3V_ALWAYS
C124 0402 100n
GND
R43 10K 0402 1%
R37 10K 0402 1%
U11
R44 100 0402
R42 10K 0402 1%
BIOS_ONOFF
02, 14
OPEN DRAIN
SN74AHC1G09DCKR
R41 NF 0 0402
0R
GND
Place to control ONOFF from Bios MCU

SW3
KMR221GLFS

DESIGN NOTE:
PMIC asserts POR_n when all PWR rails are OK, internally Pulled-Up (100K) to SNVS then, 2ms after the last rail on the sequence is up, PMIC releases POR_n (Open Drain) and remains to +SNVS

DESIGN NOTE:
Internally Pulled-Up to +SNVS, this button is readed by the iMX PMU wich includes de-bouncing logic and detects both large and short "shorts" to ground to power ON and OFF the system

DESIGN NOTE:
Outputs to PMIC_ON_REQ and PMIC STBY REQ from iMX6 PMU (see TRM page 345/3667)
Pulled up and down by iMX T9 (both 100K) to +3.0V_SNVS and GND respectively
PMIC_STBY_REQ currently unused

DESIGN NOTE:
Resistor R20 from CPU_XTALI to GND is required to correct a known 24MHz slow starting issue present on some i.MX6 part. Please refer to the i.MX6 Processor Errata

Y1 CS325S24000000ABJT
R20 2.2M 0402
C95 18p 0402
C96 18p 0402
Y2 ABS07-32.768KHZ-T
C97 18p 0402
C98 18p 0402

U1B
i.MX6UL - CONTROL
MCIMX6G2CVM05AA

ONOFF R8
POR_n P8
BOOT_MODE0 T10
BOOT_MODE1 U10
TEST_MODE N7
SNVS_TAMPER0 R10
SNVS_TAMPER1 R9
SNVS_TAMPER2 P11
SNVS_TAMPER3 P10
SNVS_TAMPER4 P9
SNVS_TAMPER5 N8
SNVS_TAMPER6 N11
SNVS_TAMPER7 N10
SNVS_TAMPER8 N9
SNVS_TAMPER9 R6
CCM_PMIC_STBY_REQ U9
SNVS_PMIC_ON_REQ T9
XTALI T16
XTALO T17
RTC_XTALI T11
RTC_XTALO U11
GPANAIO R13

SOC_ONOFF
SOC_POR_n
BOOT_MODE0
BOOT_MODE1
02, 10, 14 SOC_POR_n
02, 01 BOOT_MODE0
02, 01 BOOT_MODE1
ClassName: PWRST_MAN
ClassName: BOOT_MODE
02, 15 ACC_INT
02, 10 AUD_INT
R38 0 0402
R36 0 0402
ClassName: PWRST_MAN
ClassName: SOC_UNUSED_TAMPER
TP17
TP18
02, 10 PMIC_STB_REQ
02, 10 PMIC_ON_REQ
IMX6_XTALI
IMX6_XTALO
IMX6_RTXTALI
IMX6_RTXTALO

JTAG_TCK M14
JTAG_TMS P14
JTAG_TDI N16
JTAG_TDO N15
JTAG_TRST_n N14
JTAG_MOD P15
CCM_CLK1_N P16
CCM_CLK1_P P17
NVCC_UART H13
UART1_TX_DATA K14
UART1_RX_DATA K16
UART1_RTS_n J14
UART1_CTS_n K15
UART2_TX_DATA J17
UART2_RX_DATA J16
UART2_RTS_n H14
UART2_CTS_n J15
UART3_TX_DATA H17
UART3_RX_DATA H16
UART3_RTS_n G14
UART3_CTS_n H15
UART4_TX_DATA G17
UART4_RX_DATA G16
UART5_TX_DATA F17
UART5_RX_DATA G13

ClassName: JTAG
R35 10K 0402 1%
R27 10K 0402 1%
ClassName: SOC_UNUSED_CCM
+3.3V_PERIPH
C104 220n 0201
ClassName: UART_CONSOLE
SD1_CD
ClassName: BLE
UART2_TX 02, 08
UART2_RX 02, 08
ClassName: CAN1_RXTX
CAN1_RX 02, 08
CAN1_TX 02, 08
ClassName: I2C1
PMIC I2C !
I2C1_SCL 02, 10
I2C1_SDA 02, 10
ClassName: I2C2
I2C2_SCL 02, 15
I2C2_SDA 02, 15

R117 10K 0402 1%
+3.3V_PERIPH
SD1_CD

DESIGN NOTE:
UART1_RTS_B is configured as SD CD_B signal during SD boot :
Table 8-18 (SD/MMC IOMUX Pin Configuration) of the i.MX6 UL RM (Rev. 1, 04/2016).

JTAG PORT

TP1 JTAG_TCK
TP2 JTAG_TMS
TP3 JTAG_TDI
TP4 JTAG_TDO
TP5 JTAG_TRST
TP6 JTAG_MOD

DEBUG

J10 NF

I2C1_SCL TP19
I2C1_SDA TP20
I2C2_SCL TP21
I2C2_SDA TP22

SOC NOTE 1:

- POR_B – configurable on-chip pullup
- ONOFF – on-chip pullup
- BOOT_MODE0 – on-chip pulldown
- BOOT_MODE1 – on-chip pulldown
- TAMPER – on-chip keeper
- PMIC_STBY_REQ – configurable output
- PMIC_ON_REQ – push-pull output
- TEST_MODE – on-chip pulldown

Cannot open file C:\Proyectos\eBikemotion\eBikemotion_BHD\[10

Title: EBMULDPB-REV A10		
Size: A3	Number: Ignacio Diz Castro	Revision:
Date: 23/10/2017	Sheet of	
File: C:\Proyectos\..\[02] - SOC - CONTROL, UART, CAN, I2C, JTAG.SchDoc	Drawn By:	