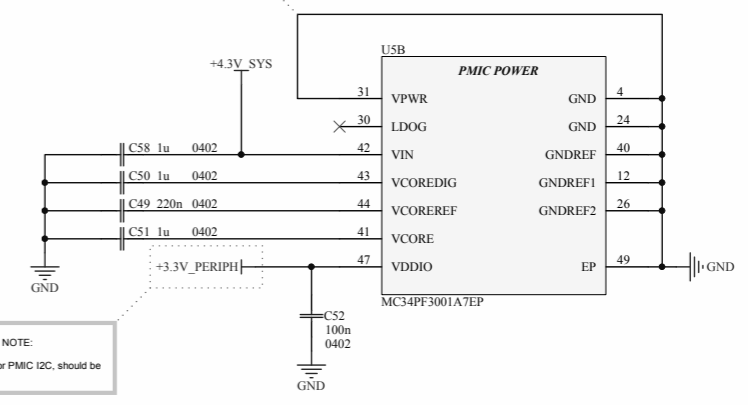
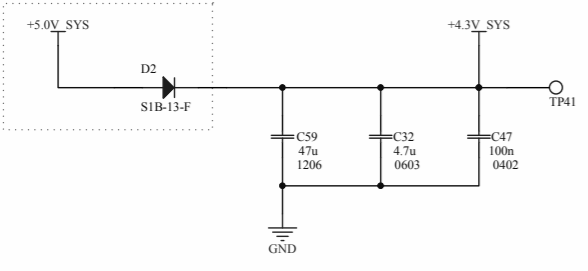


POWER PMIC

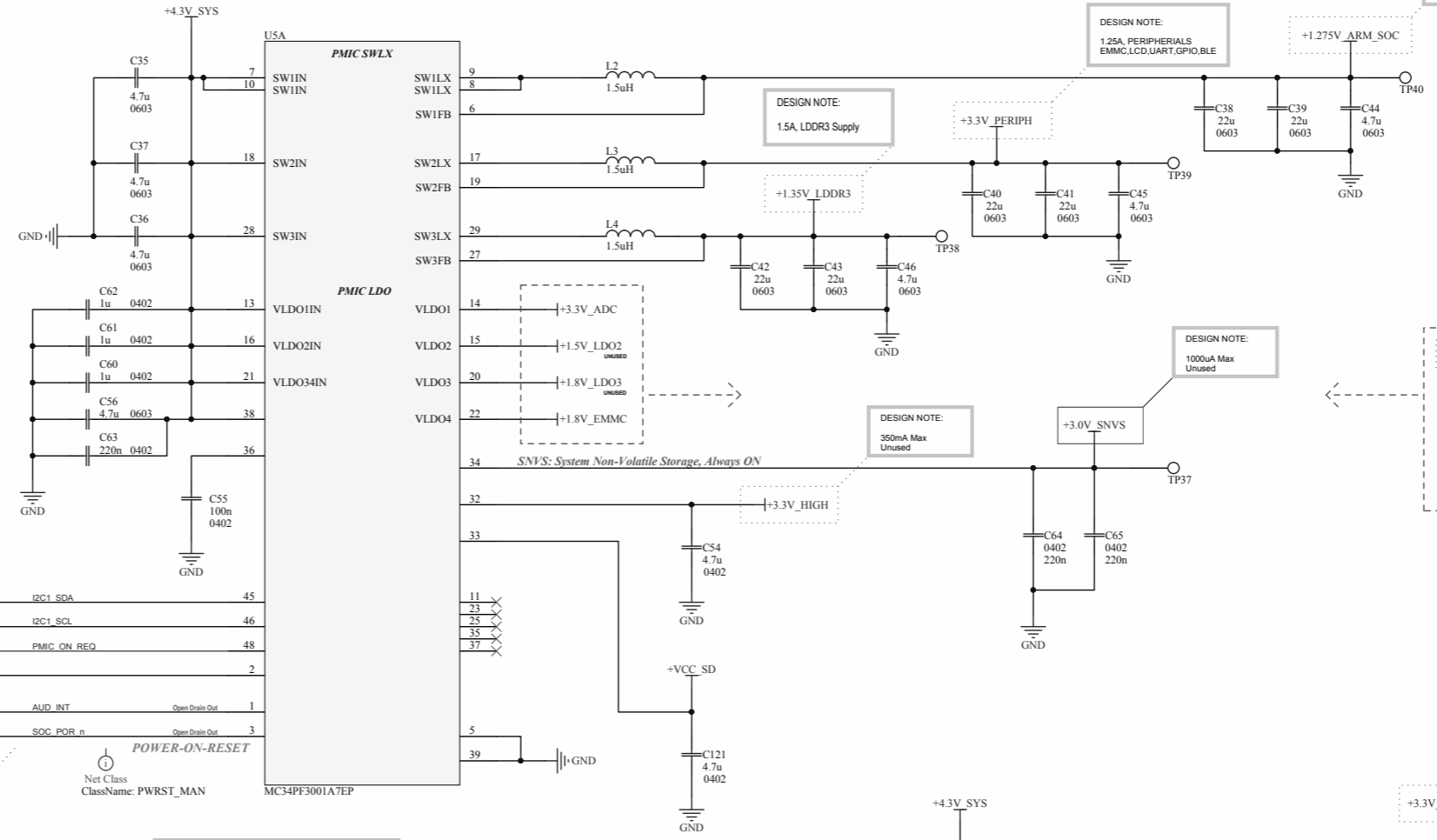
DESIGN NOTE:
 - PMIC only supports up to 4.5V In
 - With D1, the more the load, the less V Cathode
 - Find more info on PF3001 page 30

DESIGN NOTE:
 From PF3001 DSheet P79. If Front End LDO is not used, VPWR Should be tied to GND



DESIGN NOTE:
 Supply for PMIC I2C, should be <= VIN

DESIGN NOTE:
 2.75 A ARM Interconnect, Core Domain



DESIGN NOTE:
 1.5A, LDDR3 Supply

DESIGN NOTE:
 1.25A, PERIPHERALS EMMC,LCD,UART,GPIO,BLE

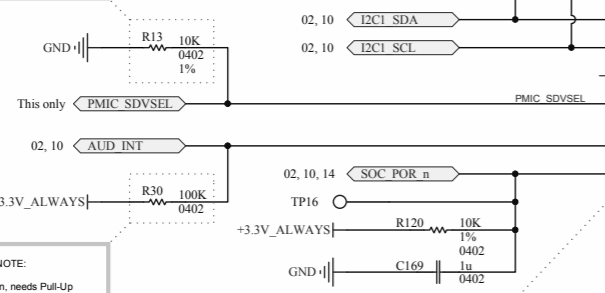
DESIGN NOTE:
 1000uA Max Unused

DESIGN NOTE:
 350mA Max Unused

DESIGN NOTE:
 PSRR @75 mA: 52 60 dB

DESIGN NOTE:
 Pulldown Defaults +VCC_SD to 2.85V 3.3V

DEFAULT ADDRESS 0X08



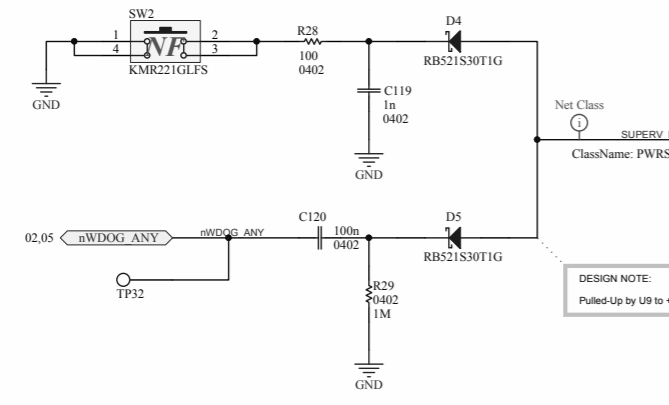
DESIGN NOTE:
 Open Drain, needs Pull-Up

DESIGN NOTE:
 Pulled-Up by SOC P8 to +SNVS, see SOC note (Sheet 02)

DESIGN NOTE:
 Undervoltage threshold set when +4.3V_SYS Rail falls below +3.72V. Threshold +3.07V. At this situation, +5.0V_SYS will be < +4.2V

DESIGN NOTE:
 Supply for: SNVS + VDDHIGH BIOS MCU 300mA MAX

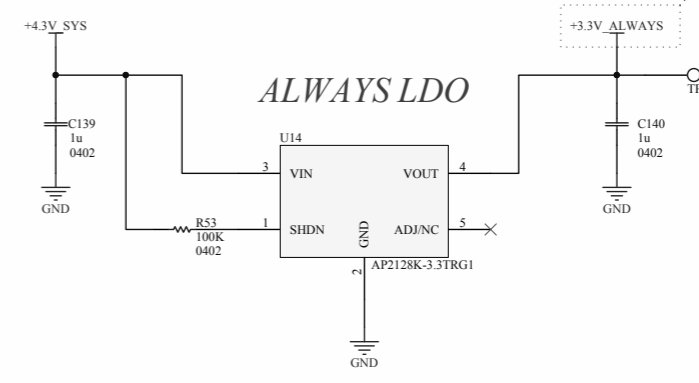
HARD RESET



DESIGN NOTE:
 Delay 300 mS, UM805RE is 240mS

DESIGN NOTE:
 Pulled-Up by U9 to +4.3V with 90K

DESIGN NOTE:
 PMIC ON REQ is Pulled-Up by MX T9 with 100K to +SNVS



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Title			EBMULDPEB-REV A10		
Size	Number			Revision	
A2	Ignacio Diz Castro				
Date:	23/10/2017	Sheet of			
File:	C:\Projects\..._110 - POWER - PMIC Sch	Drawn By:			