POWER PMIC

DESIGN NOTE:

- PMIC only supports up to 4.5V In
- With D1, the more the load, the less V Cathode
- Find more info on PF3001 page 30

+5.0V_SYS — D2 S1B-13-F — +4.3V_SYS — TP41

C59 47u 1206 | C32 4.7u 0603 | C47 100n 0402 — GND

DESIGN NOTE:

From PF3001 DSheet P79, If Front End LDO is not used, VPWR Should be tied to NGD

U5B — PMIC POWER — MC34PF3001A7EP

31	VPWR	GND	4
30	LDOG	GND	24
42	VIN	GNDREF	40
43	VCOREDIG	GNDREF1	12
44	VCOREREF	GNDREF2	26
41	VCORE		
47	VDDIO	EP	49

+4.3V_SYS — C58 1u 0402 — C50 1u 0402 — C49 220n 0402 — C51 1u 0402 — GND

+3.3V_PERIPH — C52 100n 0402 — GND — GND

DESIGN NOTE:

Supply for PMIC I2C, should be <= VIN

DESIGN NOTE:

2.75 A, ARM Interconnect, Core Domain

DESIGN NOTE:

1.25A, PERIPHERIALS EMMC,LCD,UART,GPIO,BLE

+1.275V_ARM_SOC — TP40

+4.3V_SYS — U5A — PMIC SWLX

C35 4.7u 0603	7, 10	SW1IN, SW1IN	9, 8 SW1LX, SW1LX
		SW1FB	6
C37 4.7u 0603	18	SW2IN	17 SW2LX
		SW2FB	19
C36 4.7u 0603 — GND	28	SW3IN	29 SW3LX
		SW3FB	27

L2 1.5uH — L3 1.5uH — L4 1.5uH

DESIGN NOTE:

1.5A, LDDR3 Supply

+1.35V_LDDR3 — C42 22u 0603 — C43 22u 0603 — C46 4.7u 0603 — GND — TP38

+3.3V_PERIPH — C40 22u 0603 — C41 22u 0603 — C45 4.7u 0603 — GND — TP39

C38 22u 0603 — C39 22u 0603 — C44 4.7u 0603 — GND

PMIC LDO

C62 1u 0402	13	VLDO1IN	VLDO1 14 — +3.3V_ADC
C61 1u 0402	16	VLDO2IN	VLDO2 15 — +1.5V_LDO2 UNUSED
C60 1u 0402	21	VLDO34IN	VLDO3 20 — +1.8V_LDO3 UNUSED
C56 4.7u 0603	38		VLDO4 22 — +1.8V_EMMC
C63 220n 0402	36		

C55 100n 0402 — GND

DESIGN NOTE:

PSRR @75 mA: 52 60 dB

+3.3V_ADC — C66 0603 4.7u | +1.5V_LDO2 — C67 0603 4.7u | +1.8V_LDO3 — C68 0603 4.7u | +1.8V_EMMC — C69 0603 4.7u — GND

DESIGN NOTE:

1000uA Max Unused

DESIGN NOTE:

350mA Max Unused

+3.0V_SNVS — TP37

SNVS: System Non-Volatile Storage, Always ON

+3.3V_HIGH — C54 4.7u 0402 — GND

C64 0402 220n | C65 0402 220n — GND

11, 23, 25, 35, 37 — GND

+VCC_SD — C121 4.7u 0402 — GND

5, 39 — GND

DESIGN NOTE:

Pulldown Defaults +VCC_SD to 2.85V 3.3V

DEFAULT ADDRESS 0X08

+3.3V_PERIPH — R11 2.2K 0402 | R12 2.2K 0402

02, 10 I2C1_SDA — I2C1_SDA 45

02, 10 I2C1_SCL — I2C1_SCL 46

PMIC_ON_REQ 48

GND — R13 10K 0402 1%

This only PMIC_SDVSEL — PMIC_SDVSEL 2

02, 10 AUD_INT — AUD_INT Open Drain Out 1

02, 10, 14 SOC_POR_n — SOC_POR_n Open Drain Out 3

+3.3V_ALWAYS — R30 100K 0402

DESIGN NOTE:

Open Drain, needs Pull-Up

TP16 — +3.3V_ALWAYS — R120 10K 1% 0402 — GND — C169 1u 0402

POWER-ON-RESET

Net Class ClassName: PWRST_MAN

MC34PF3001A7EP

DESIGN NOTE:

Pulled-Up by SOC P8 to +SNVS, see SOC note (Sheet 02)

DESIGN NOTE:

Undervoltage threshold set when +4.3V_SYS Rail falls below +3.72V. Threshold +3.07 V. At this situation, +5.0V_SYS will be < +4.2V

HARD RESET

SW2 KMR221GLFS — GND — R28 100 0402 — D4 RB521S30T1G — C119 1n 0402 — GND

+4.3V_SYS — R33 2.05K 0402 1% | R32 10K 0402 1% — GND

+4.3V_SYS — C122 0402 100n — GND

U9 — TPS3808G33DBVR

5	SENSE	VDD	6
4	CT	RST	1
3	MR	GND	2

R31 100K 0402 — SUPERV_MR — Net Class ClassName: PWRST_MAN

PMIC_ON_REQ — 02, 10

+3.3V_ALWAYS — R121 0402 1% 10K — C170 1u 0402 — GND

02,05 nWDOG_ANY — nWDOG_ANY — C120 100n 0402 — D5 RB521S30T1G — R29 0402 1M — GND — TP32

DESIGN NOTE:

Delay 300 mS, UM805RE is 240mS

DESIGN NOTE:

Pulled-Up by U9 to +4.3V with 90K

DESIGN NOTE:

PMIC ON REQ is Pulled-Up by iMX T9 with 100K to +SNVS

ALWAYS LDO

DESIGN NOTE:

Supply for:
SNVS + VDDHIGH
BIOS MCU
300mA MAX

+4.3V_SYS — C139 1u 0402 — GND

U14 — AP2128K-3.3TRG1

3	VIN	VOUT	4
1	SHDN	GND	ADJ/NC 5
2			

R53 100K 0402

+3.3V_ALWAYS — TP35 — C140 1u 0402 — GND

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