Dual LVDS for High Resolution Display

For i.MX6DQ/DLS

Update On 8/30/2017

i.MX6DQ/DLS display port limitation

For single-channel output: Up to 85 MHz per interface. (e.g. WXGA - 1366x768 @ 60 Hz + 35% blanking).

If the resolution is greater than above, needs two port work together under split mode to get higher resolution.

Notes(First pixel and Channel mapping)

Mapping of Parallel input interfaces (DI0, DI1) to output LVDS channels (Channel 0, Channel 1). See Table 39-5.

Table 39-5. Channel Mapping

Use Case	LVDS Channel 0	LVDS Channel 1
Single Channel DI0	DI0	Disabled
Single Channel DI1 on Channel 1	Disabled	DI1
Separate Channels	DI0	DI1
Dual Channels DI0	DI0	DI0
Dual Channels DI1	DI1	DI1
Split Channel DI0	DI0 (first pixel)	DI0 (second pixel)
Split Channel DI1	DI1 (first pixel)	DI1 (second pixel)

Notes(Clock)

A table with the LDB Clock Sources can be found here.

Table 39-4. LDB Clock Sources

Name	Symbol	Source	Rate	Comments
IPU DI0 interface pixel clock	IPU_DI0_CLK	Clock control Module	Up to 170 MHz	See note below [1]
IPU DI1 interface pixel clock	IPU_DI1_CLK	Clock control Module	Up to 170 MHz	This input also goes to IPU DI1 as input. See note below
CH0 interface serializer clock	DI0_SERIAL_CLK	Clock control Module	Up to 595 MHz	This is x7 the rate of the DI0 interface pixel clock. See note below.
CH1 interface serializer clock	DI1_SERIAL_CLK	Clock control Module	Up to 595 MHz	This is x7 the rate of the DI1 interface pixel clock. See note below

1. In case of single-channel or separate-channels use-case, the IPU DI_CLK is identical to the LVDS DI_CLK. In case of dual-channel use-case, the IPU DI_CLK has x2 higher frequency than that of the LVDS DI_CLK. Still both need to be synchronized

Need two separate clock to work. Only one of the clock for one interface could not use split mode.

ldb display

ldb Binding Guide:
Documentation/devicetree/bindings/video/fsl,ldb.txt

IPU Binding Guide:
Documentation/devicetree/bindings/fb/fsl_ipuv3_fb.txt

Display Timing Binding Guide:
Documentation/devicetree/bindings/video/display-timing.txt

Note : Linux Kernel Version 3.10.53

ldb Binding Guide

fsl,ldb.txt

……
14 Required properties:
15 - **compatible: Should be "fsl,<soc>-ldb".**

……
27 - **split-mode**: Provide this bool property if your board uses LDB split
28 mode to drive a high resolution display, say 1080P@60. In this
29 mode, two LVDS channels will drive one display.
30 - **dual-mode**: Provide this bool property if your board uses LDB dual
31 mode to drive two displays. In this mode, one display engine will
32 drive two displays which have the same timings and display content.

34 Subnode for LVDS Channel
35 ==========
36
37 Each LVDS Channel has to contain a **display-timings** node that describes the
38 video timings for the connected LVDS display. For detailed information, also
39 **have a look at Documentation/devicetree/bindings/video/display-timing.txt.**
.....

Please note the **Bold** text.
In the **3.0.35_410**, the **split mode** and **dual mode** are passed by the uboot. **(ldb=spl0/1, ldb=dul0/1)**
In the ldb binding guide, it highlights the binding guide for **display -timings**.

IPU Binding Guide

fsl_ipuv3_fb.txt

22 Required properties for fb:
23 - **compatible : should be "fsl,mxc_sdc_fb".**
24 - disp_dev : display device: "ldb", "lcd", "hdmi", "mipi_dsi".
25 - mode_str : "CLAA-WVGA" for lcd, "TRULY-WVGA" for TRULY mipi_dsi lcd panel,
26 "1920x1080M@60" for hdmi.
27 - **default_bpp** : default bits per pixel: 8/16/24/32
28 - int_clk : use internal clock as pixel clock: 0 or 1
29 - late_init : to avoid display channel being re-initialized
30 as we've probably setup the channel in bootloader: 0 or 1
31 - **interface_pix_fmt** : display interface pixel format as below:
32 RGB666 IPU_PIX_FMT_RGB666
33 RGB565 IPU_PIX_FMT_RGB565
34 RGB24 IPU_PIX_FMT_RGB24
.

display-timings Binding Guide

display-timing.txt

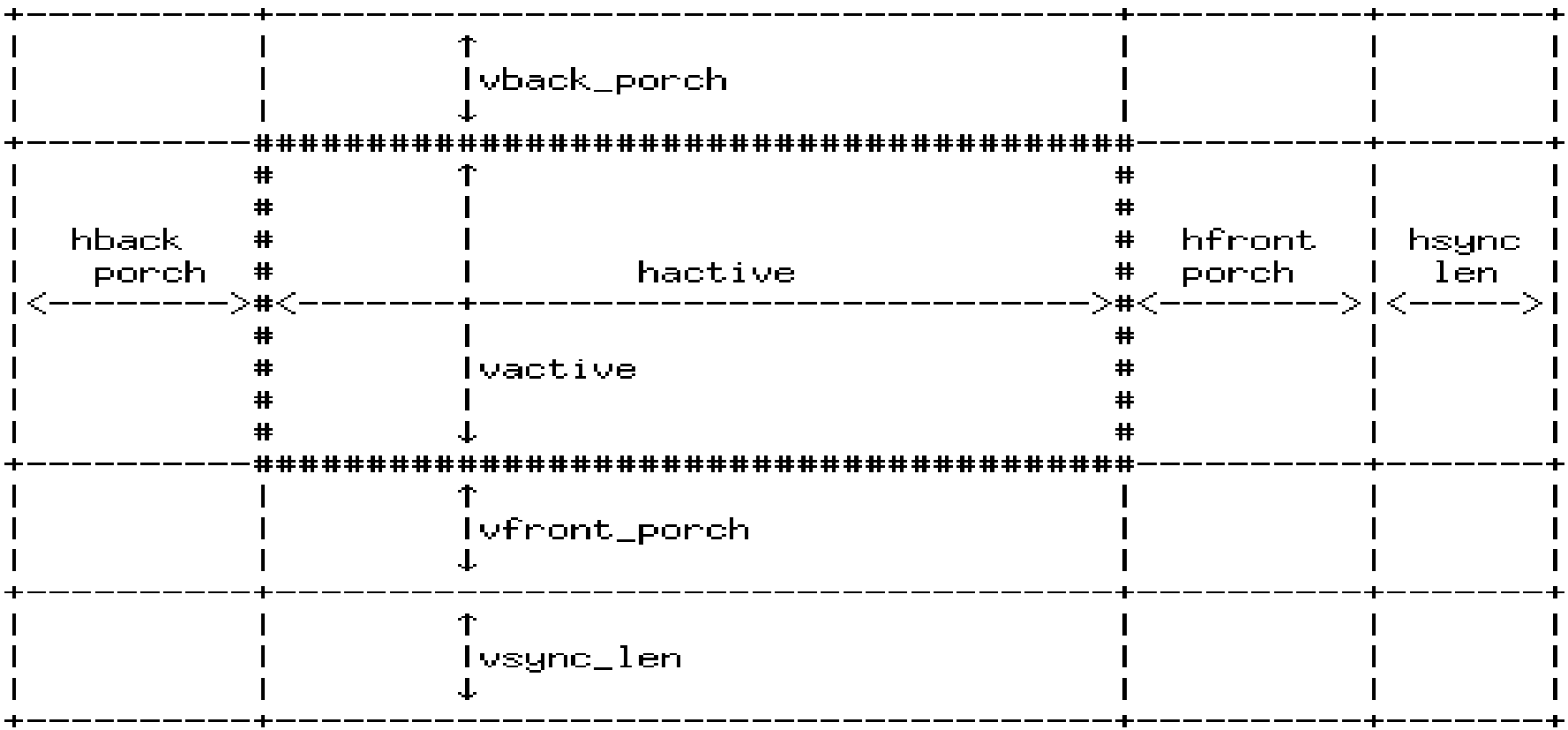
17 required properties:
18 - hactive, vactive: display resolution
19 - hfront-porch, hback-porch, hsync-len: horizontal display timing parameters
20   in pixels
21   vfront-porch, vback-porch, vsync-len: vertical display timing parameters in
22   lines
23 - clock-frequency: display clock in Hz
24
25 optional properties:
26 - hsync-active: hsync pulse is active low/high/ignored
27 - vsync-active: vsync pulse is active low/high/ignored
28 - de-active: data-enable pulse is active low/high/ignored
29 - pixelclk-active: with
30   - active high = drive pixel data on rising edge/
31   sample data on falling edge
32   - active low = drive pixel data on falling edge/
33   sample data on rising edge
34   - ignored   = ignored
35 - interlaced (bool): boolean to enable interlaced mode

display-timings Parameters

clock-frequency is display clock(DCLK) in Hz.
 Note: In the 3.0.35_410 is using the pixel clock of the fb_mode structure.
Pixel clock = 1000000/DCLK

```
struct fb_videomode {
        const char *name;       /* optional */
        u32 refresh;            /* optional */
        u32 xres;
        u32 yres;
        u32 pixclock;
        u32 left_margin;
……
        u32 vsync_len;
        u32 sync;
        u32 vmode;
        u32 flag;
};
```

display-timings Parameters (Cont.)

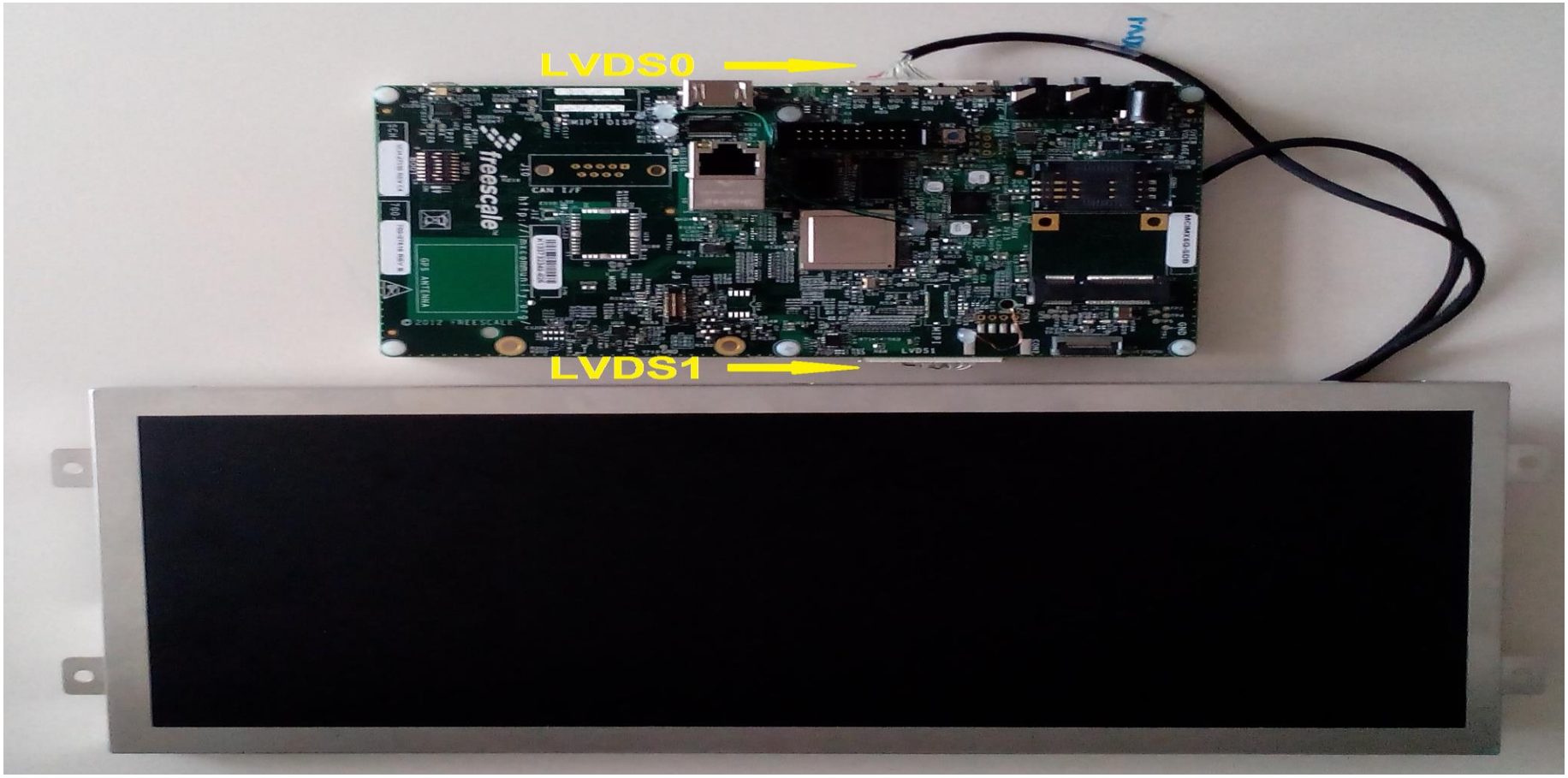


In the DE mode
hback-porch + hfront-porch + hsync-len = Horizontal Black Time
vback-porch + vfront-porch + vsync-len = Vertical Black Time
hback-porch, hfront-porch,hsync-len are no-zero value
vback-porch, vfront-porch,vsync-len are no-zero value

LVDS LCD CLAA123FBA1

CLAA123FBA1XN example

CLAA123FBA1XN 12.3” color TFT-LCD (Thin Film Transistor Liquid Crystal Display) module composed of LCD panel, driver ICs ,control circuit and LED backlight. By applying 1920X720 images are displayed on the 12.3” diagonal screen. Display 16.7M colors by R.G.B signal input.



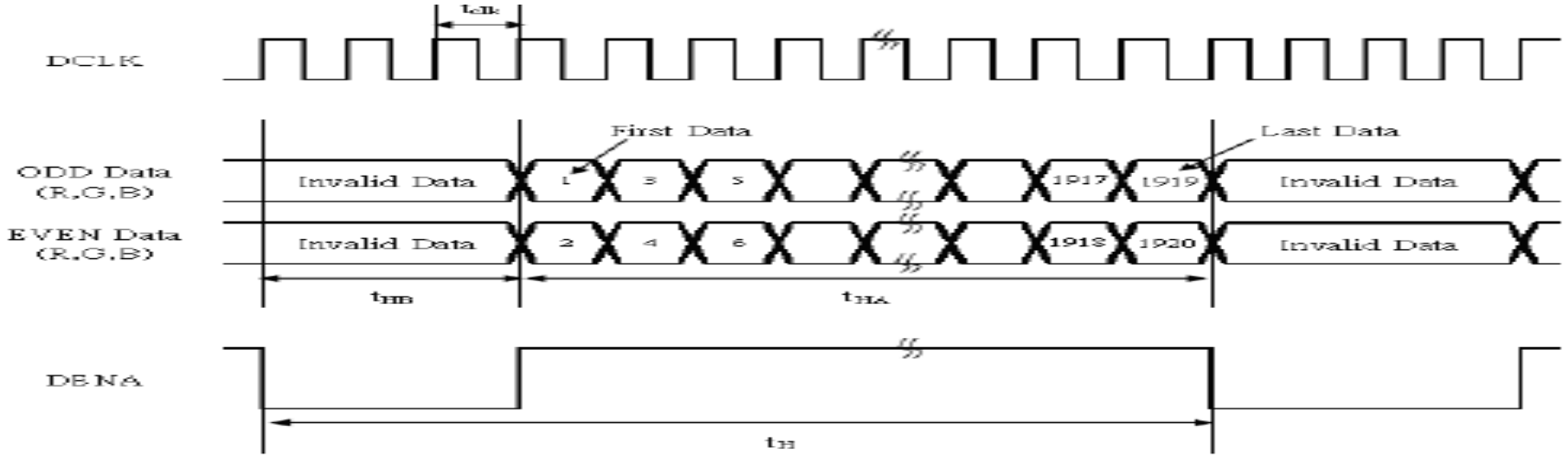
CLAA123FBA1XN Datasheet

Timing Specification

Item				Symbol	Min	Typ	Max	Unit
LVDS input signal sequence	CLK Frequency			fCLKin	40	52.3	66.12	MHz
LCD input signal sequence （Input LVDS Transmitter）	DENA	Horizontal	Horizontal total Time	t_H	1070	1150	1230	tCLK
			Horizontal effective Time	t_{HA}		960		tCLK
			Horizontal Blank Time	t_{HB}	110	190	270	tCLK
			Vertical total Time	t_V	748	758	768	t_H
			Vertical effectiveTime	t_{VA}		720		t_H
			Vertical Blank Time	t_{VB}	28	38	48	t_H

fCLKin 52.3 MHz: DCLK=ODD+EVEN=2XfCLKin=2X52.3=104.6MHz

tHA 960 : Resolution 1920X720=960X2X720
tHB 190 : hback-porch + hfront-porch + hsync-len = 190
tVB 38 : vback-porch + vfront-porch + vsync-len = 38



CLAA123FBA1XN Parameters DTS (3.10.53)

imx6qdl-sabresd.dtsi

```
&ldb {
        status = "okay";

        split-mode;

        lvds-channel@0 {
                fsl,data-mapping = "spwg";
                fsl,data-width = <24>;
                status = "okay";

                display-timings {
                        native-mode = <&timing0>;
                        timing0: CLAA123FBA1_1920X720 {
                                clock-frequency = <104600000>;
                                hactive = <1920>;
                                vactive = <720>;
                                hback-porch = <90>;
                                hfront-porch = <90>;
                                vback-porch = <15>;
                                vfront-porch = <15>;
                                hsync-len = <10>;
                                vsync-len = <8>;
                        };
                };
        };

        lvds-channel@1 {
                fsl,data-mapping = "spwg";
                fsl,data-width = <24>;
                primary;
                status = "okay";

                display-timings {
                        native-mode = <&timing1>;
                        timing1: CLAA123FBA1_1920X720 {
                                clock-frequency = <104600000>;
                                hactive = <1920>;
                                vactive = <720>;
                                hback-porch = <90>;
                                hfront-porch = <90>;
                                vback-porch = <15>;
                                vfront-porch = <15>;
                                hsync-len = <10>;
                                vsync-len = <8>;
                        };
                };
        };
};
```

split-mode

imx6q-sabresd.dts

```
&mxcfb1 {
        status = "okay";
        interface_pix_fmt = "RGB24";
        default_bpp = <32>;
};
```

interface_pix_fmt = "RGB24"

fCLKin 52.3 MHz: DCLK=ODD+EVEN=2XfCLKin=2X52.3=104.6MHz

tHA 960 : Resolution 1920X720=960X2X720

tHB 190 : hback-porch + hfront-porch + hsync-len = 190

tVB 38 : vback-porch + vfront-porch + vsync-len = 38

Note: Linux Kernel 3.10.53

CLAA123FBA1XN Parameters fb_videomode(3.0.35)

```
{
 "LDB-1080P60", 60, 1920, 720, 9560,
 90, 90,
 15, 15,
 10, 8,
 0,
 FB_VMODE_NONINTERLACED,
 FB_MODE_IS_DETAILED,},
```

```
struct fb_videomode {
        const char *name;       /* optional */
        u32 refresh;            /* optional */
        u32 xres;
        u32 yres;
        u32 pixclock;
        u32 left_margin;
        u32 right_margin;
        u32 upper_margin;
        u32 lower_margin;
        u32 hsync_len;
        u32 vsync_len;
        u32 sync;
        u32 vmode;
        u32 flag;
};
```

pixclock : 1000000/104.6=9560.22

fCLKin 52.3 MHz: DCLK=ODD+EVEN=2XfCLKin=2X52.3=104.6MHz
tHA 960 : Resolution 1920X720=960X2X720
tHB 190 : hback-porch + hfront-porch + hsync-len = 190
tVB 38 : vback-porch + vfront-porch + vsync-len = 38

Note: Linux Kernel 3.0.35