12x12mm i.MX 7D LPDDR3 VALIDATION BOARD
Elastomer Mat Socket Version

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GENERAL DESIGN NOTES

1. Unless Otherwise Specified:
   All resistors are in ohms, 5%, 1/16 Watt
   All splitter resistors are 0-ohms, 5%, 1/16 Watt
   All capacitors are in uF, 20%, 50V
   All voltages are DC
   All polarized capacitors are Tantalum

2. Critical compenents that require tolerances tighter than listed in Note 1are labeled with required tolerance on schematic. Non-critical components may be filled with tighter tolerance parts for BOM consolidation purposes, but may be changed to meet the general tolerances of Note 1 if desired.

3. Interrupted lines coded with the same letter or letter combinations are electrically connected.

4. Device type number is for reference only. The number varies with the manufacturer.

5. Special signal usage:
   _B or 'n' Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

6. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

AC ADAPTER SPECIFICATIONS

DC Voltage Output: 5VDC

Current Output: ~ 5A (depending on application)

Polarity: 

Inner Diameter: 2.1mm

Outer Diameter: 5.5mm

Revision History

Rev. Code	Date	Description
X1	07/31/14	Rev X1 Draft
X2	08/07/14	- Changed Test Point net names to be different than Test Point REFDES. (For Verilog) - Changes decoupling capacitors underneatch processor per SOC team recommendation. - Deleted ADC2. Moved PMIC sense to ADC1. - Changed FB sense points from PMIC to after current sense resistors. - Change decoupling caps on LPDDR3 to 0.22uF. - PMIC_ON_REQ and PMIC_STBY_REQ_B signals swapped. - PMIC_ON_REQ pull up resistor changed to DNP.
X3	08/12/14	- Connected PVCC_SAI_SD_CAP with PVCC_ENET_CAP - Pull down resistors to USB Supervisory chip now populated. - Updated OrCAD decal to new ball map. - Added 3-pin resistor options to USB_OTG2 to eliminate stubs. - Added voltage divider network to VBUS_IN. Removed capacitor. - Added option to connect USER_LED GPIO to GPIO1_09 - U14 is now DNP. LDO is only for validation board debug purposes. - Removed DNP on R1080. LDO should be held off unless NVCC_3V3 supplied. - R264, R280, R780, R786 and R985 are now populated by default. - Added C861 and C862 capacitor footprints for QSPI high speed validation. - Added Pull up resistors to QSPI Chip selects and Pull down resistors to clock. - Changed Q510 NVCC_DRAM control FET to a load switch. - Added VREFCA to switched VREF source. - Added pull up to SD3_RST_B trace. - Added pull ups to SPI1/2/3 Chip Select traces. - Default Touch Screen sensor changed to LCD connector. - Added traces to support LCD operations from the EPDC connector. - AUD2 frame clock switch to primary frame clock source. - Separated VADC and ADC inputs. - Added 27R resistors to DEBUG UART traces. - Added 7-pin connection header for SIM Port testing. - Added pull down resistor on SIM Card detect circuit. - Pull down resistor added on ADV RESET_B pin to keep in reset when not used. - Added jumpers across VDDARM, VDDSOC current sense resistors. - Changed 0.02 Ohm sense resistors to 1 Ohm on low current supplies. - Boot I2C EEPROM moved to I2C1 by default. - Deleted R222 and R225 as unnecessary.
X4	08/14/14	- Modified SIM Port Card detect circuit to match validation requirements. - Changed decoupling capacitors on eMMC to match vendor recommendations. - Connected ADC_VDDA_1P8 rail to source VDDA_1P8 rail.
X5	08/14/14	- Layout resequenced. Refdes renumbered per back annotation.
X6	08/15/14	- Changed power source for SIM Card detect circuit to GEN_3V3 (always supplied).
X7	08/17/14	- Changed Classification of Schematics to FIUO. - Changed pull up source on SDx_RST traces. - Changed OrCAD decals for PMIC connector and processor. - Changed alternate source of FUSE_FSOURCE. - Changed additional Capacitor values under processor. - Moved ADC connections to CPU Sigals page. - Split CPU Signals into two pages. - Changed switch for DRAM_VREF to NFET. - Default NVCC_DRAM now through 0805 shorting traces. - Added DNP pull up to SD3 Data0 trace, if needed. - Moved VADC connectors to CSI page. - Deleted SPI3 IC. Moved connections to LCD header to support EPDC. - Headphone detect signal changed to show active low. - Deleted unneccessary resistors from USB traces. - Changed ENET1 LED resistor to 1K. - Added DNP pull up resistors to MPCIE Clock traces if needed. - Changed pull up resistor on USB_CHD_B to 100K.
X8	08/20/14	- Added Oscillator to PCIE Ref Clock input. - Changed level translator U509 to true Bi-Directional switch. - Connected RGMII traces to MII pins on J21 to support ETH DCs. - User LED now connected by default. - Corrected USER_LED net cross connect.
X9	08/26/14	- Updated all parts status to FCL library parts. - Changed pull ups on JTAG domain to NVCC_GPIO2
A	08/29/14	- Release to fabrication - Added footprint for resistor on LPSR_1P0_CAP in case extra current needed. - Added additional decoupling capacitor to NVCC_DRAM_SW. - Changed R202 to 0.02 Ohm sense resistor. - Changed ferrite bead L501 to short trace SH501.
A1	10/03/14	- Change population option on resistors R105 and R111 from position "A" to Position "B". - Change resistors R104, R615, R618, R620, R630 to DNP. - Populate resistors R102, R103, R106, R112, R613.

Preliminary - Subject to Change without Notice
Freescale Internal Use Only

This board was designed for maximum flexibility in software development and demonstrates multiple functions possible with i.MX processors. Although best design practices have been applied, some areas may not be suitable for a mass-production design. For an added resource, refer to the i.MX 7D Hardware Development Guide document (number TBD).

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Multimedia Application Division, Wireless & Mobile System Group

ICAP Classification: FCP: FIUO: XPUBI:

Designer: Mark Middleton	Drawing Title: i.MX 7D 12MM LPDDR3 CPU VAL BOARD		
Drawn by: Mark Middleton	Page Title: COVER PAGE		
Approved: <Approver>	Size C	Document Number SOURCE:SCH-28484 PDF:SPF-28484	Rev A1
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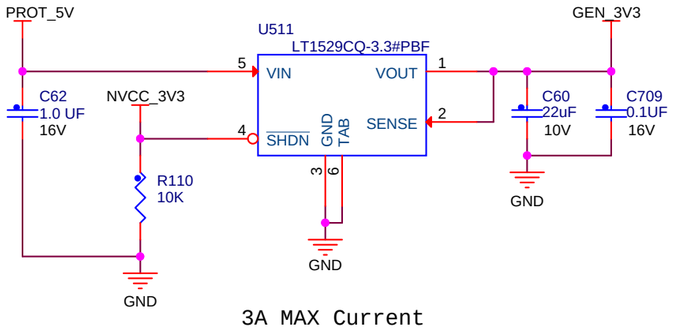
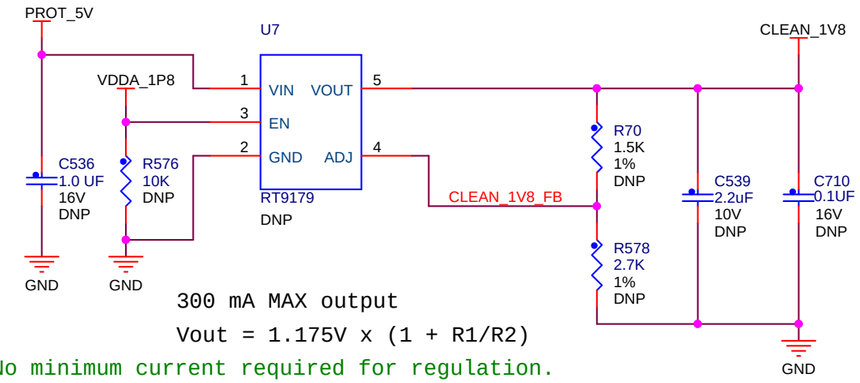
ALTERNATE POWER SUPPLIES



3A MAX Current

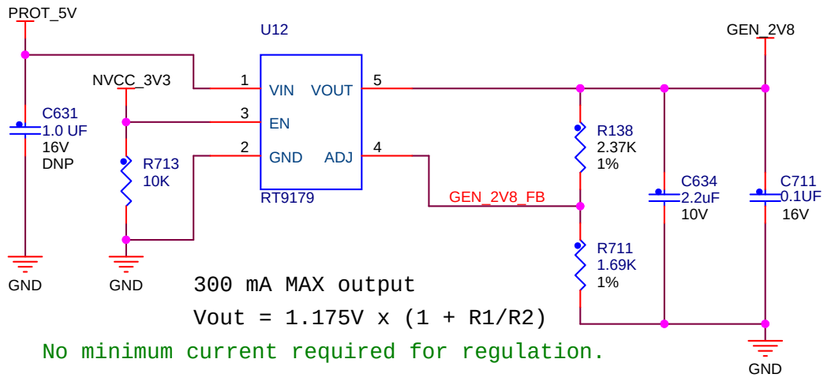
No minimum current required for regulation.



300 mA MAX output

Vout = 1.175V x (1 + R1/R2)

No minimum current required for regulation.

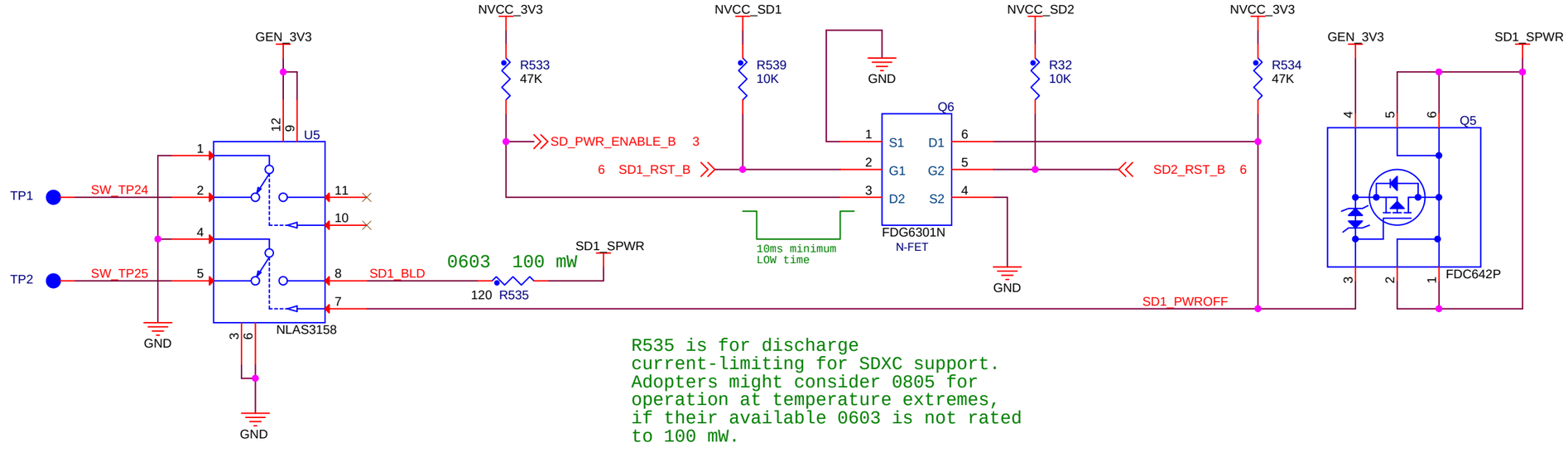


300 mA MAX output

Vout = 1.175V x (1 + R1/R2)

No minimum current required for regulation.

SD1 SOCKET POWER SUPPLY



R535 is for discharge current-limiting for SDXC support. Adopters might consider 0805 for operation at temperature extremes, if their available 0603 is not rated to 100 mW.

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AUX POWER

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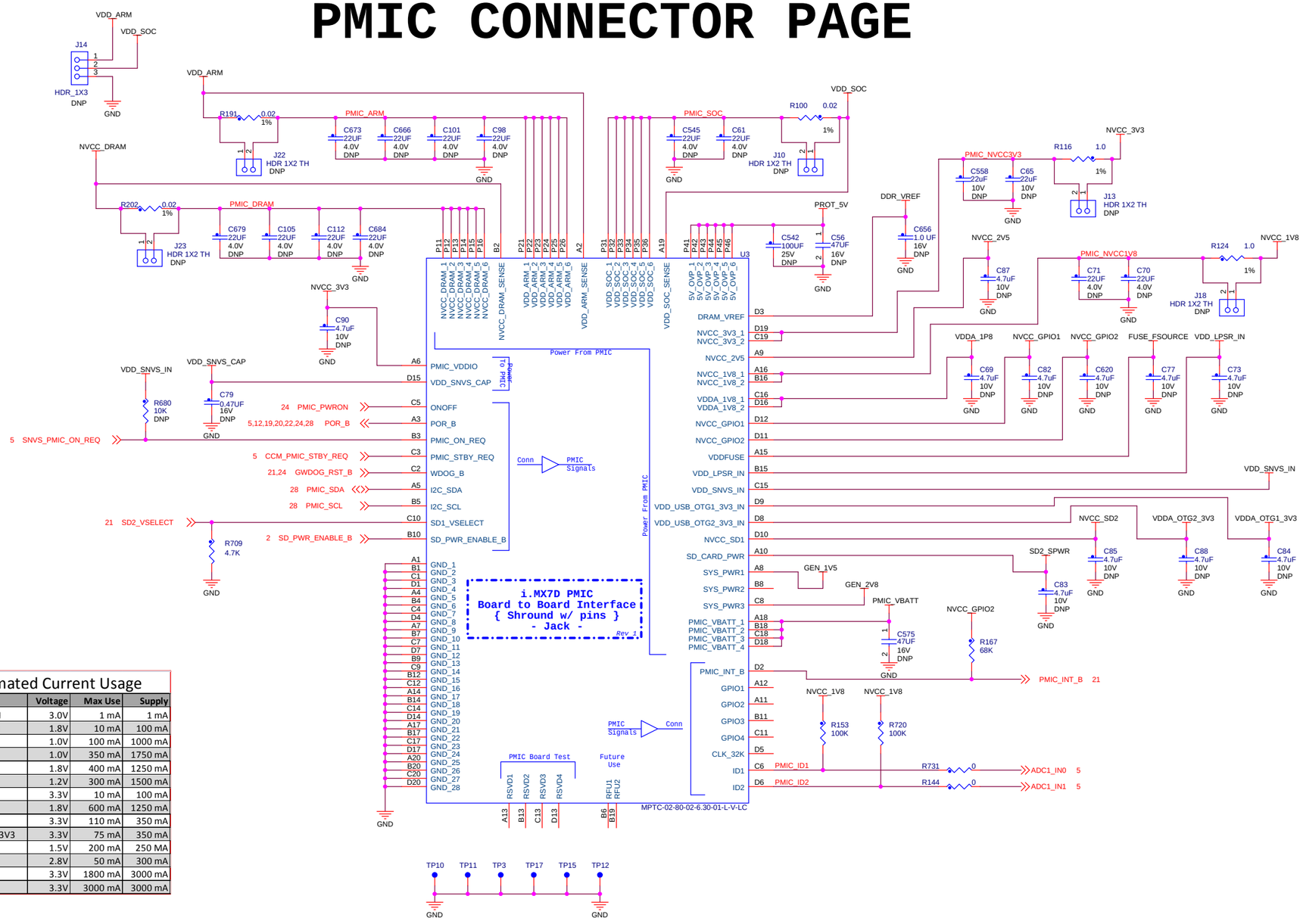
PMIC CONNECTOR PAGE



Estimated Current Usage

Rail Name	Voltage	Max Use	Supply
VDD_SNVS_IN	3.0V	1 mA	1 mA
VDD_LPSR_IN	1.8V	10 mA	100 mA
VDDARM	1.0V	100 mA	1000 mA
VDDSOC	1.0V	350 mA	1750 mA
VDDA_1P8	1.8V	400 mA	1250 mA
NVCC_DRAM	1.2V	300 mA	1500 mA
NVCC_GPIO	3.3V	10 mA	100 mA
NVCC_1V8	1.8V	600 mA	1250 mA
NVCC_3V3	3.3V	110 mA	350 mA
VDDA_OTGX_3V3	3.3V	75 mA	350 mA
GEN_1V5	1.5V	200 mA	250 MA
GEN_2V8	2.8V	50 mA	300 mA
GEN_3V3	3.3V	1800 mA	3000 mA
MPCIE_3V3	3.3V	3000 mA	3000 mA

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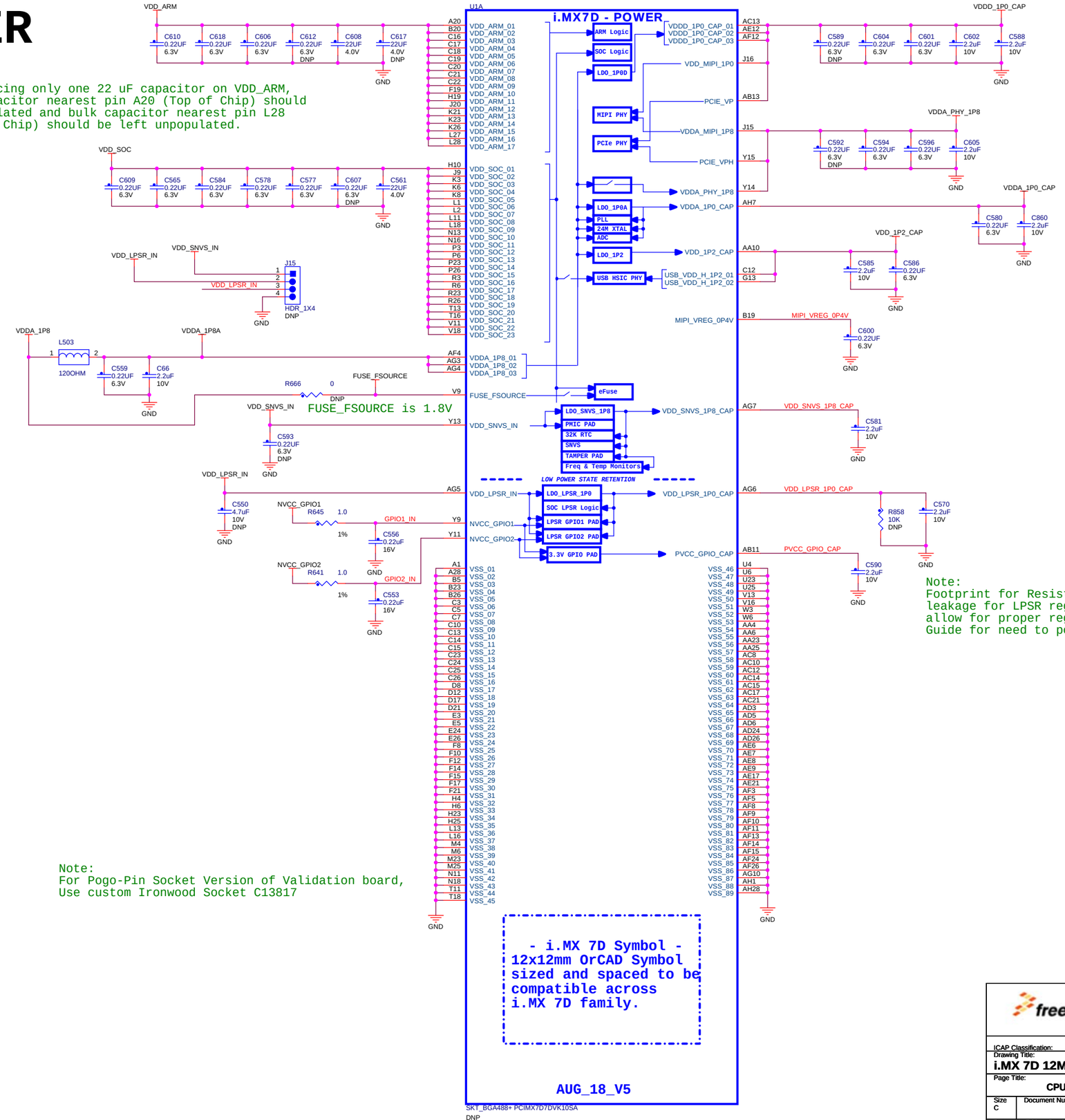
CPU POWER

NOTE:
When placing only one 22 uF capacitor on VDD_ARM,
bulk capacitor nearest pin A20 (Top of Chip) should
be popoulated and bulk capacitor nearest pin L28
(Side of Chip) should be left unpopulated.



Note:
For Pogo-Pin Socket Version of Validation board,
Use custom Ironwood Socket C13817

Note:
Footprint for Resistor R858 added in case
leakage for LPSR regulator not enough to
allow for proper regulation. See HW Users
Guide for need to populate this resistor.

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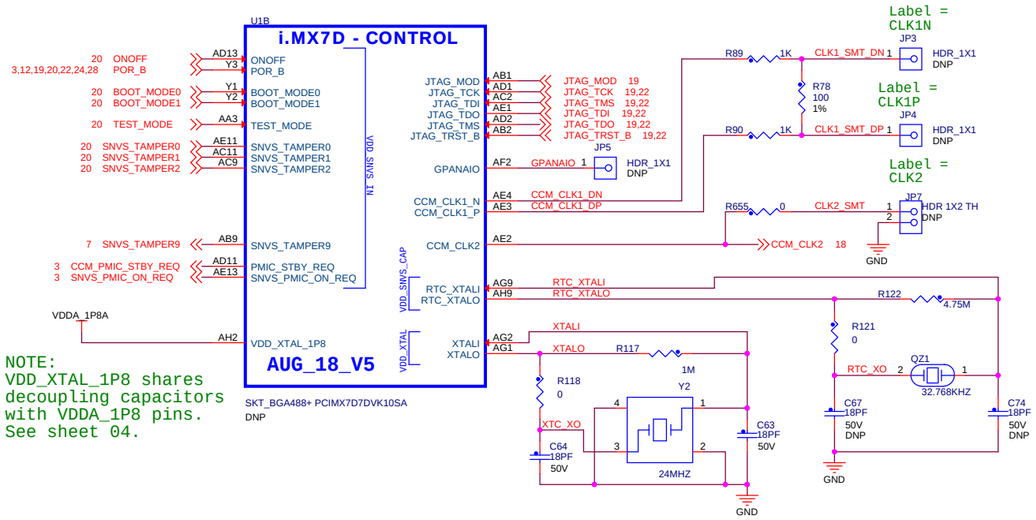
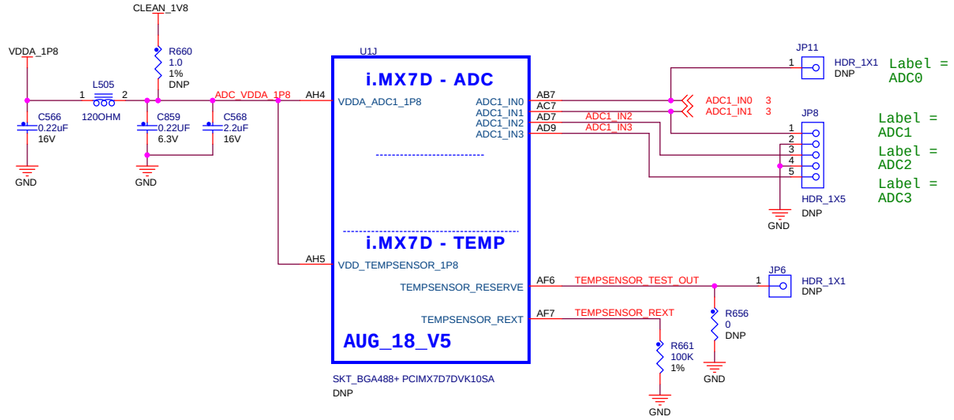
CPU SIGNALS - 1

NOTE:
Unless otherwise noted, all 3-way resistors will be populated in the "A" position with 0 Ohm resistors.



NOTE:
VDD_XTAL_1P8 shares decoupling capacitors with VDDA_1P8 pins.
See sheet 04.



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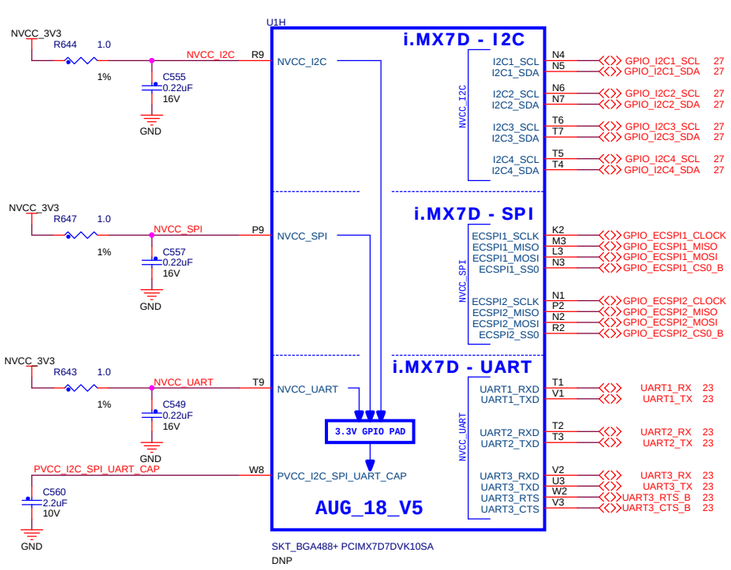
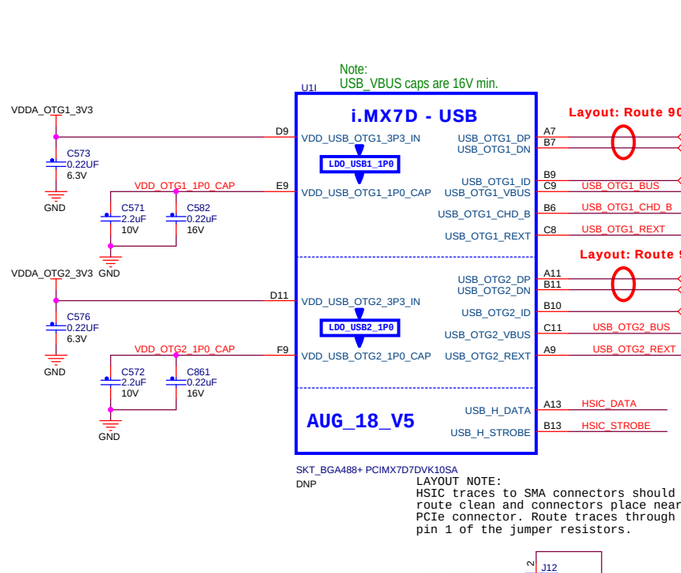
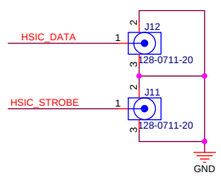




LAYOUT NOTE:
HSIC traces to SMA connectors should route clean and connectors place near PCIe connector. Route traces through pin 1 of the jumper resistors.



NOTE:
Resistors R653/R652 and R670/R665 form a resistor divider network in case transients on VBUS cause damage to the i.MX 7D.

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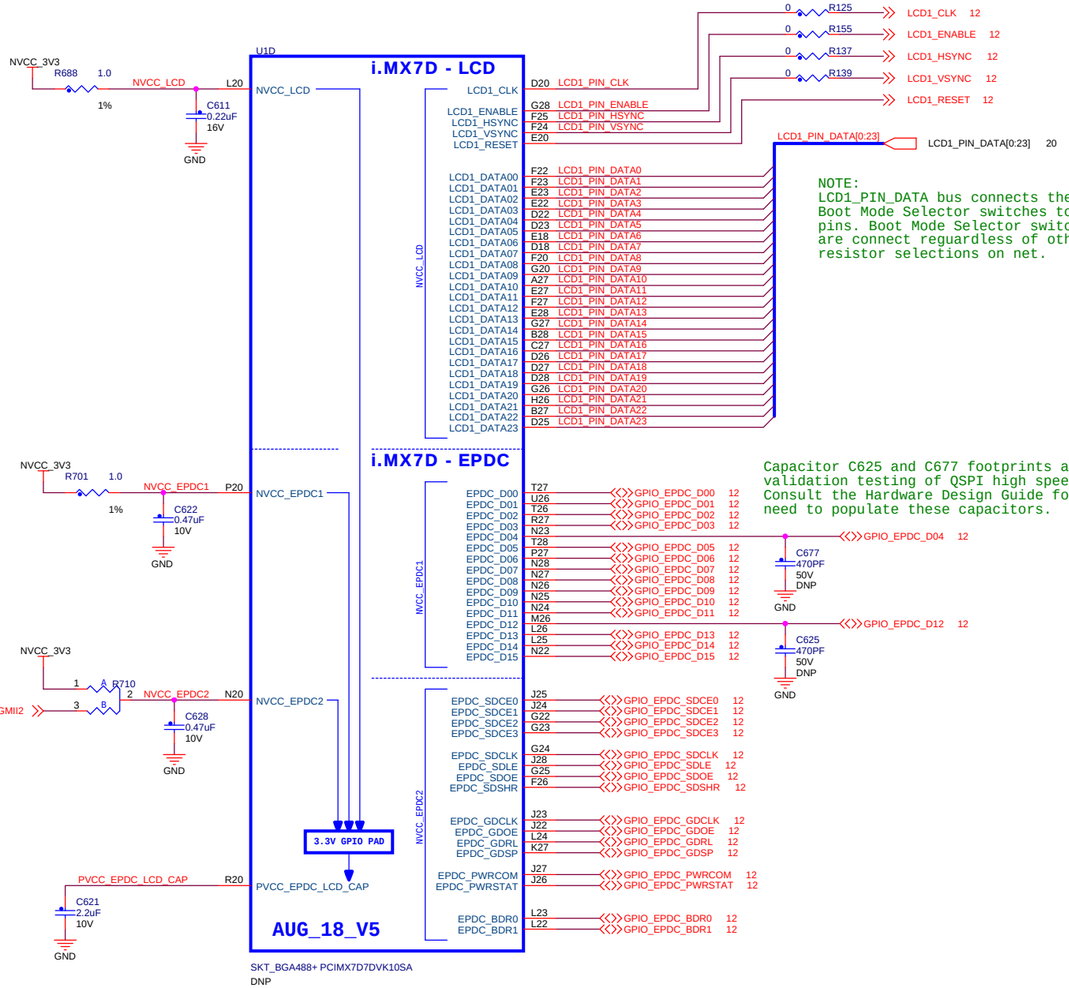
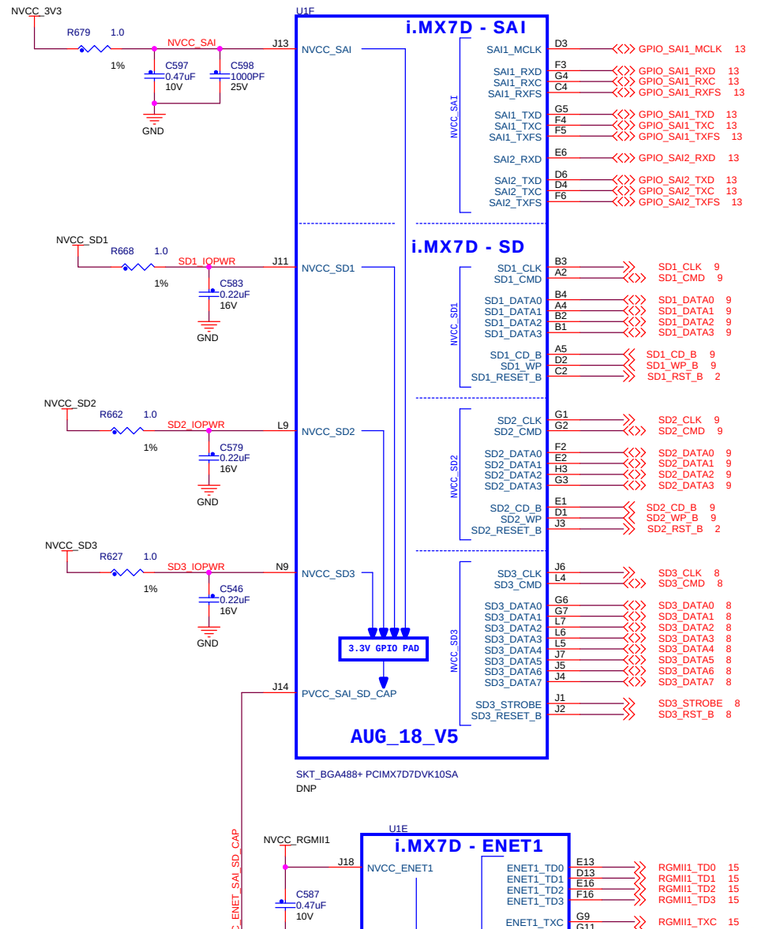
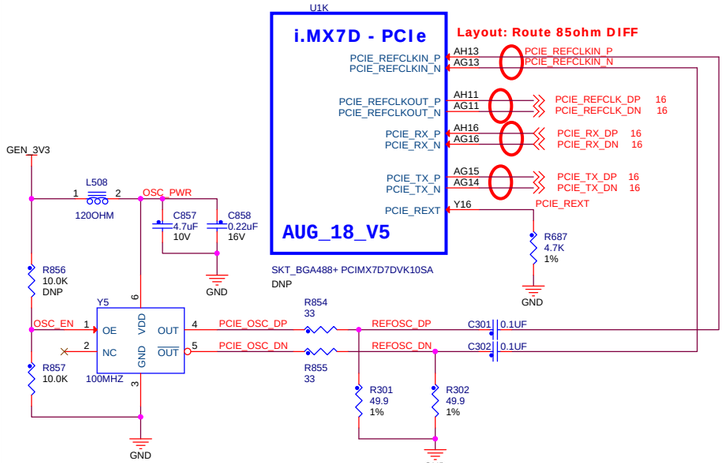
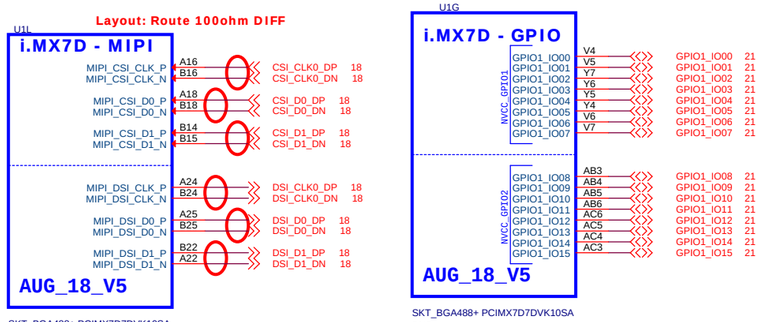
CPU SIGNALS - 2

NOTE:
Unless otherwise noted, all 3-way resistors will be populated in the "A" position with 0 Ohm resistors.









NOTE:
Power supply pins for NVCC_GPIO1 and NVCC_GPIO2 are included on CPU power page. These two supplies also work with the Low Power supply pins.

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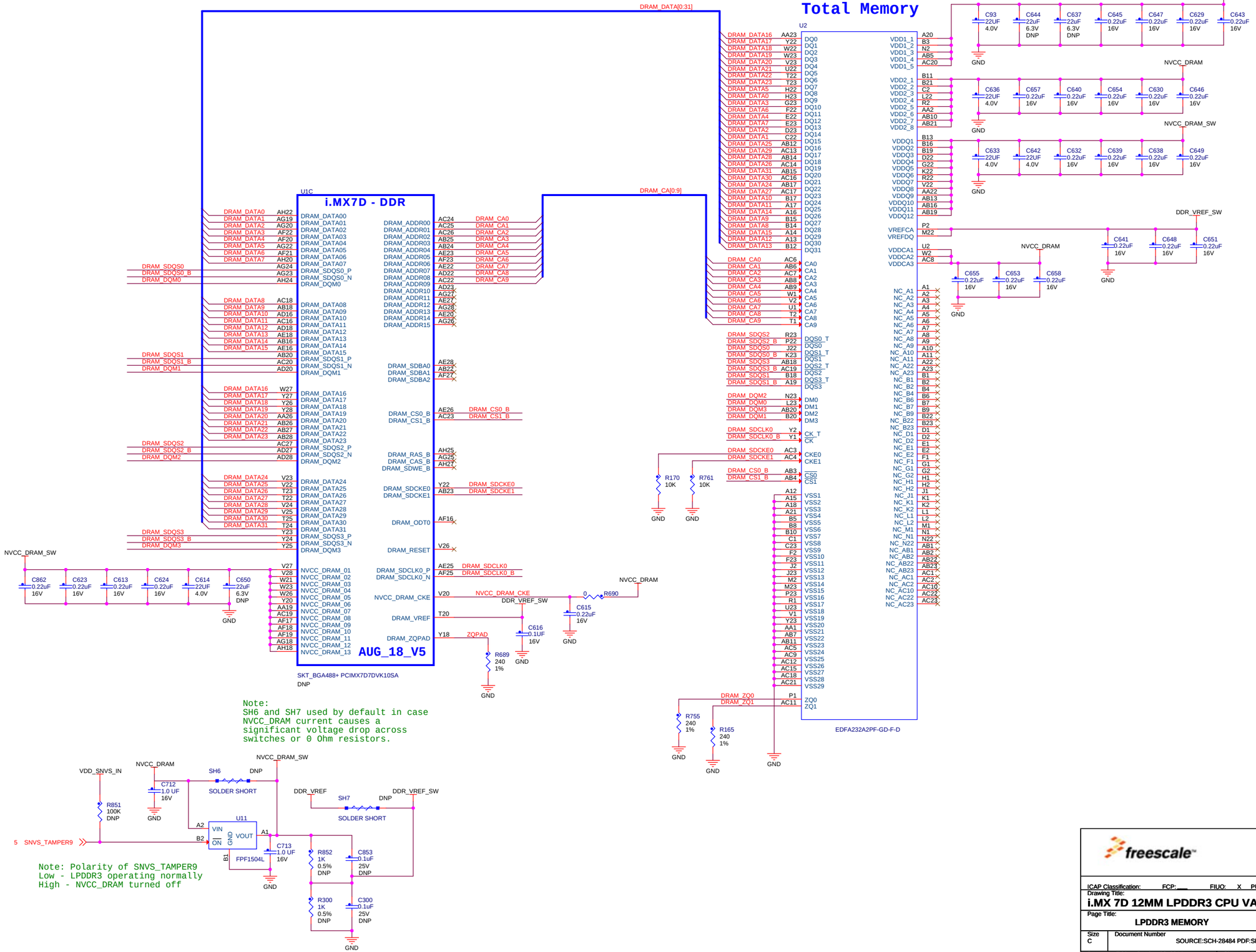
LPDDR3 MEMORY

2GB Total Memory



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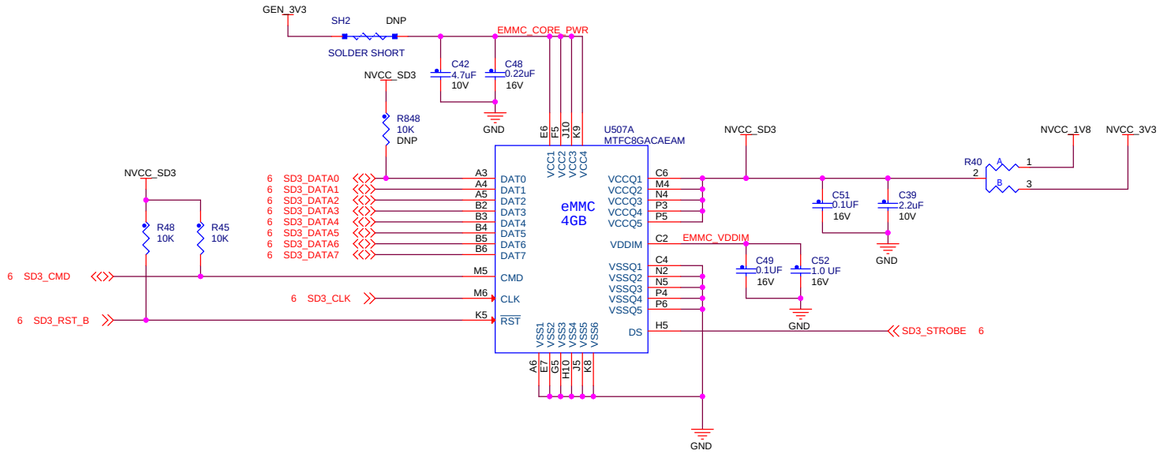
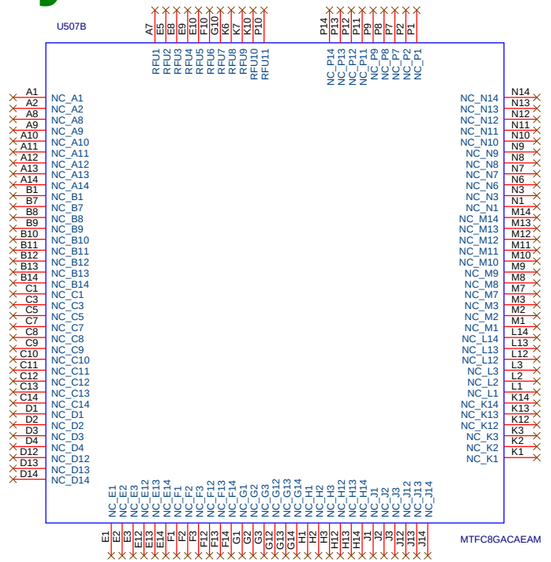
Label = eMMC Memory





QSPI

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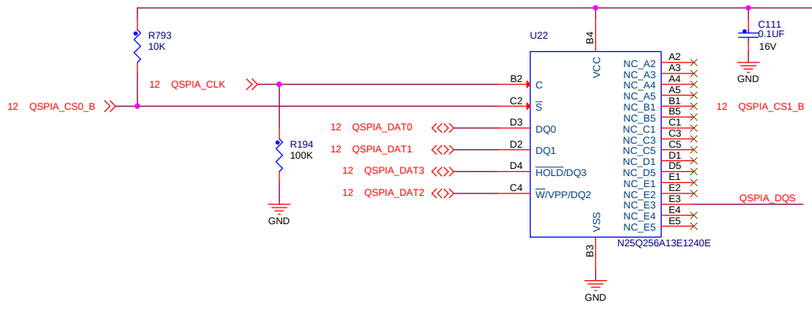

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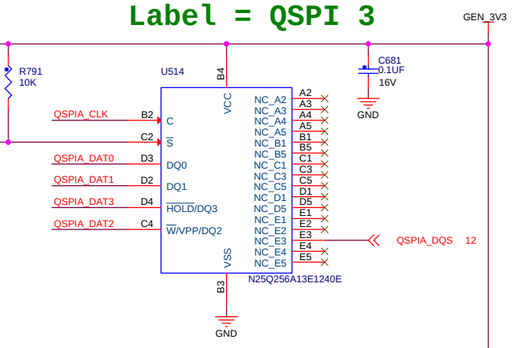

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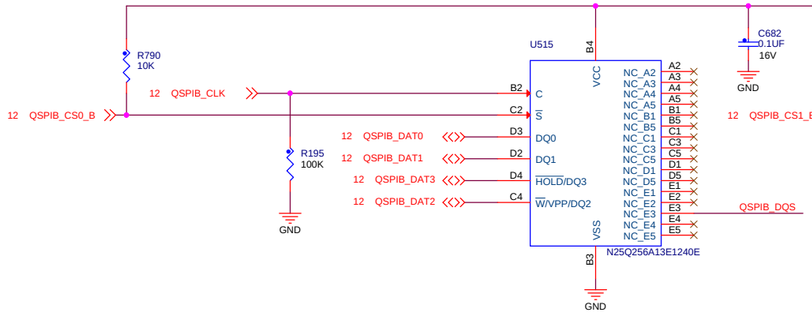

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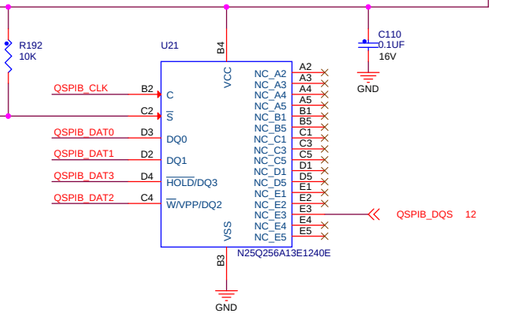

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QSPI, EMMC

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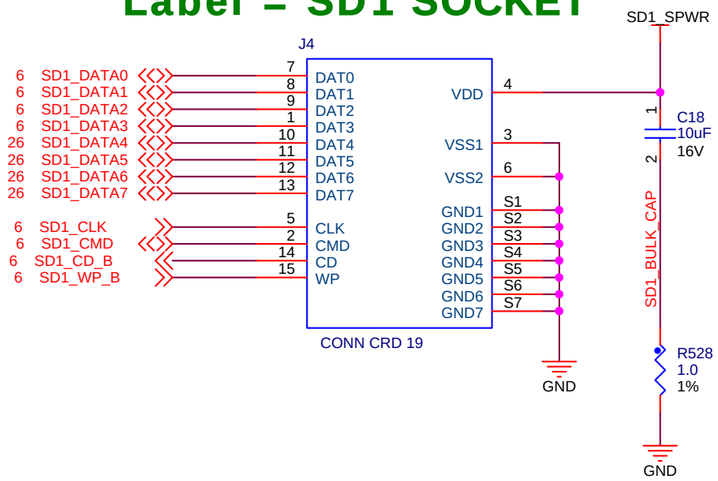
USDHC

Label = SD1 SOCKET



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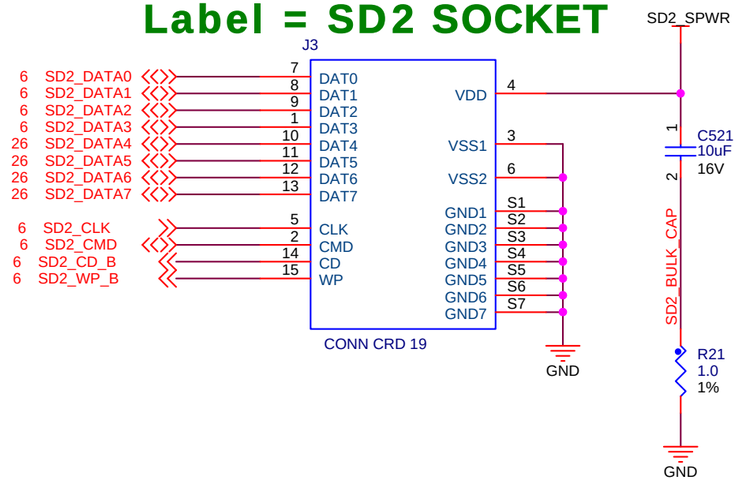
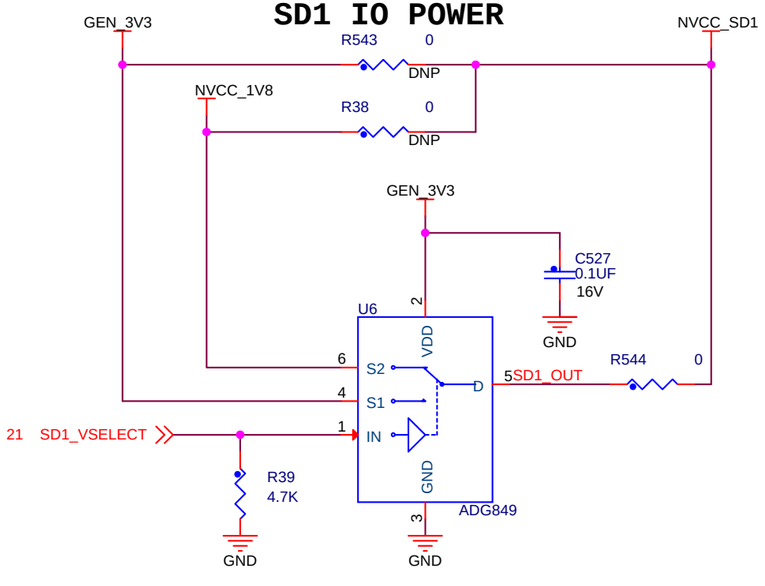


SD1 IO POWER



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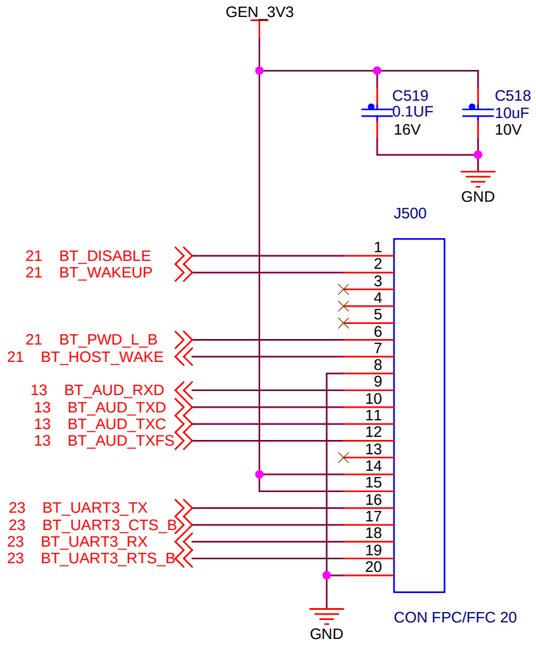
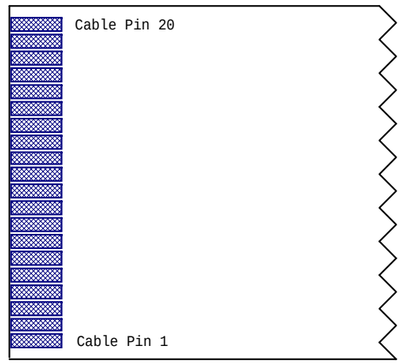
BLUETOOTH CABLE CONNECTOR

Label = BLUETOOTH



Layout NOTE:
BT Cable connector aligns with SDA card socket.
Add silk screen label:
"BT CABLE CONNECTOR"



NOTE:
Pin 1 of the cable connector on the Smart Device board is opposite Pin 20 of the WIFI/BT module. For the FFC to lie flat, the pin order number needs to be reversed on the schematics.

NOTE:
The AUX SDIO CARD SOCKET and the BLUETOOTH CABLE CONNECTOR have been designed and tested specifically for use with the WIFI/BT combo card SX-SDCAN-2830BT Developed and sold by Silex Technolgy. The developer may need to consult the datasheet of other WIFI solutions for compatibility with this card socket.

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BLUETOOTH

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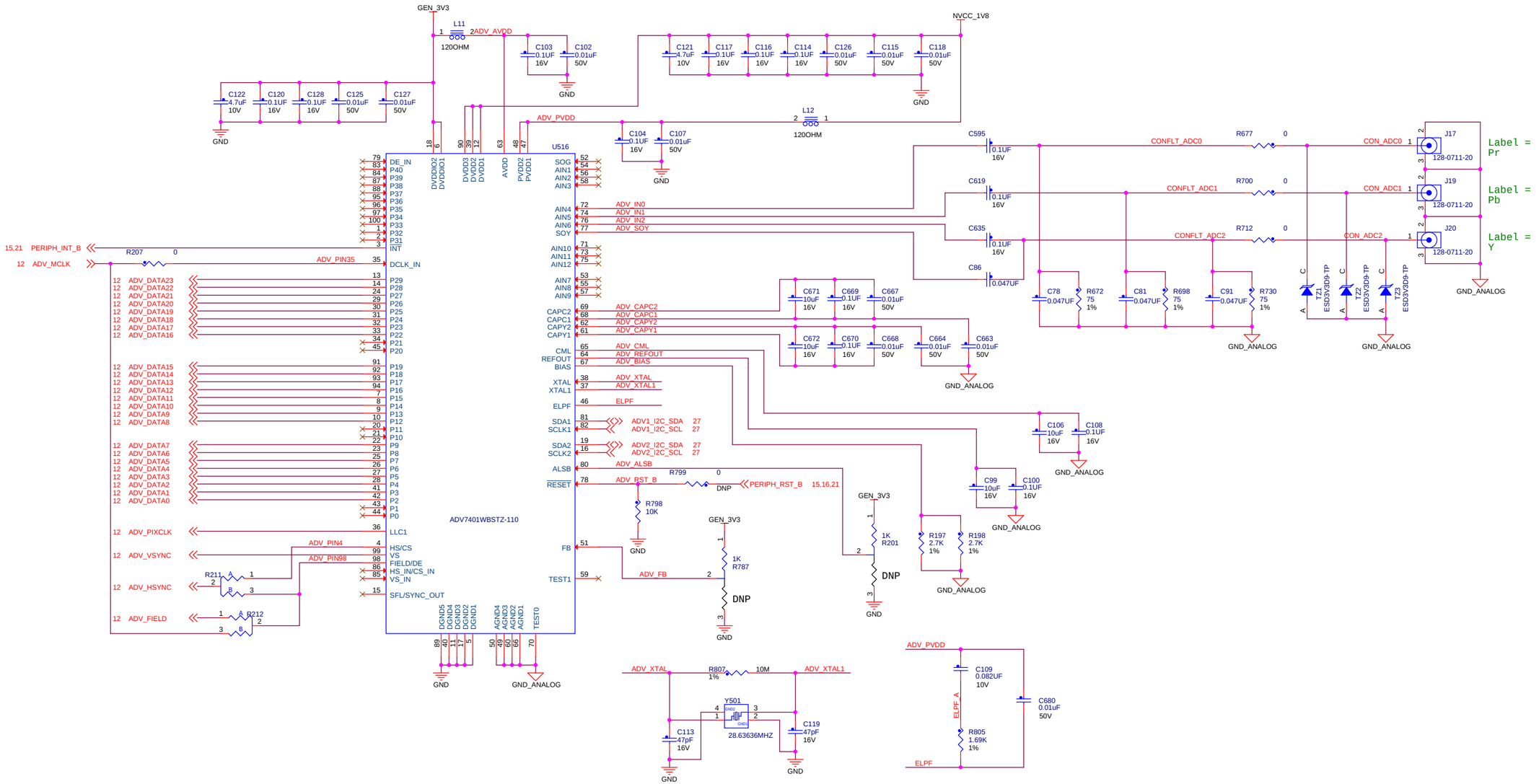
CSI

NOTE:
Unless otherwise noted, all 3-way resistors will be populated in the "A" position with 0 Ohm resistors.



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CSI

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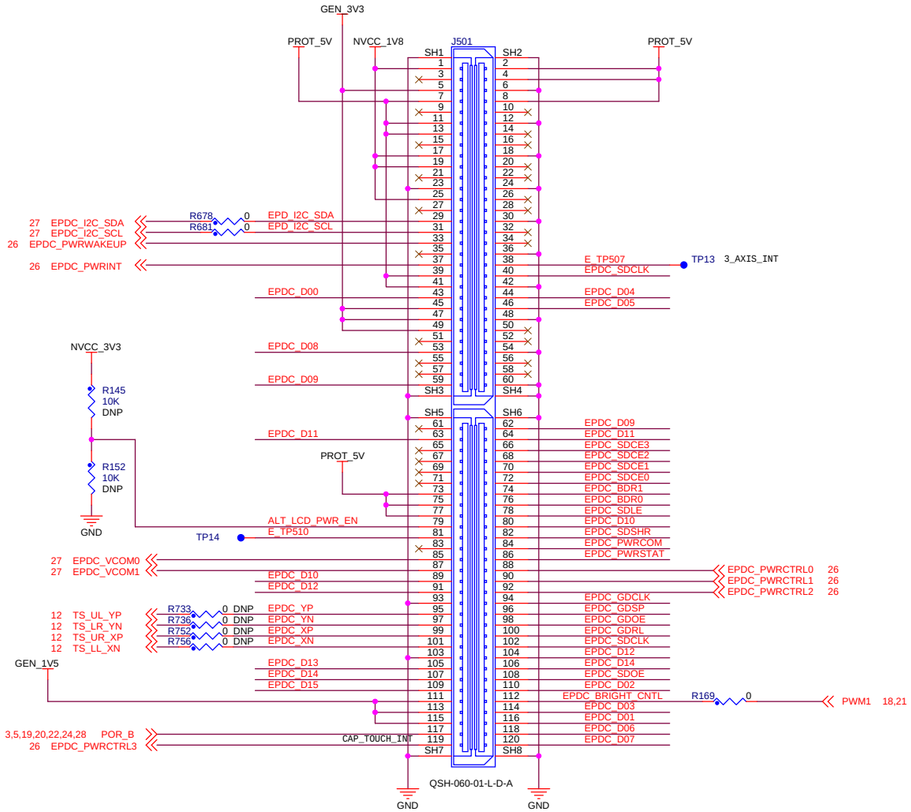
Label = EPDC HDR



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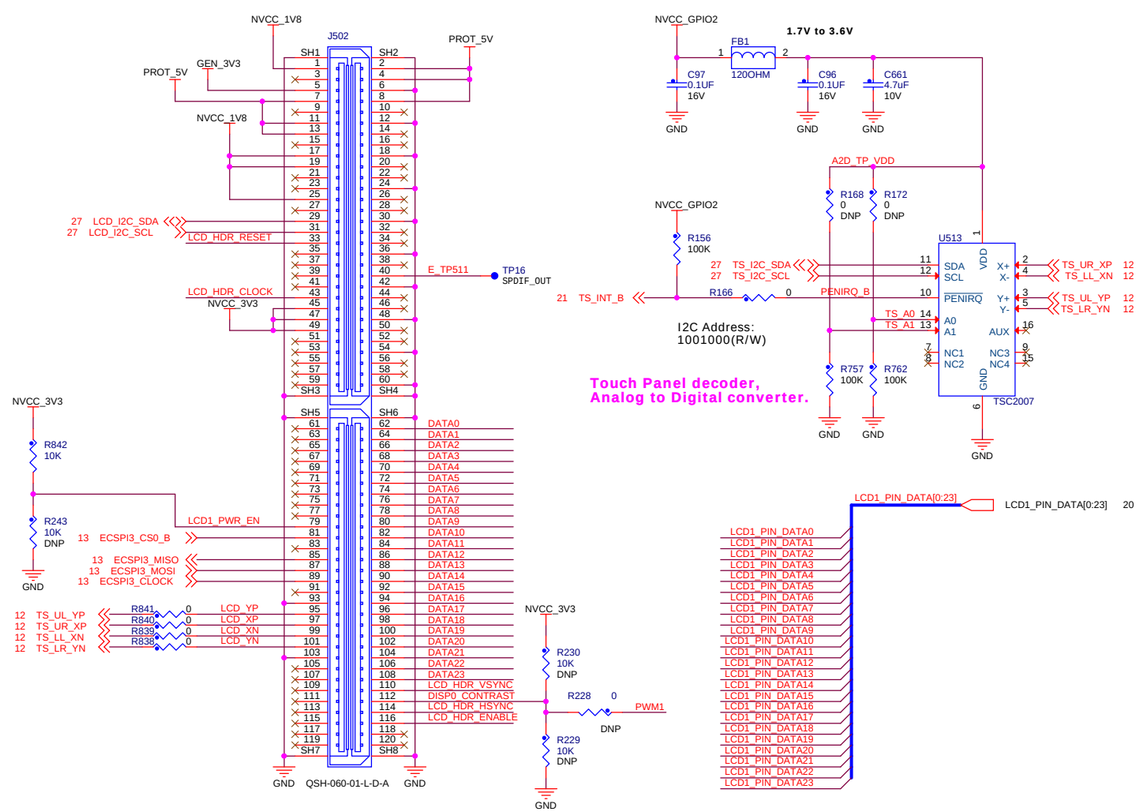
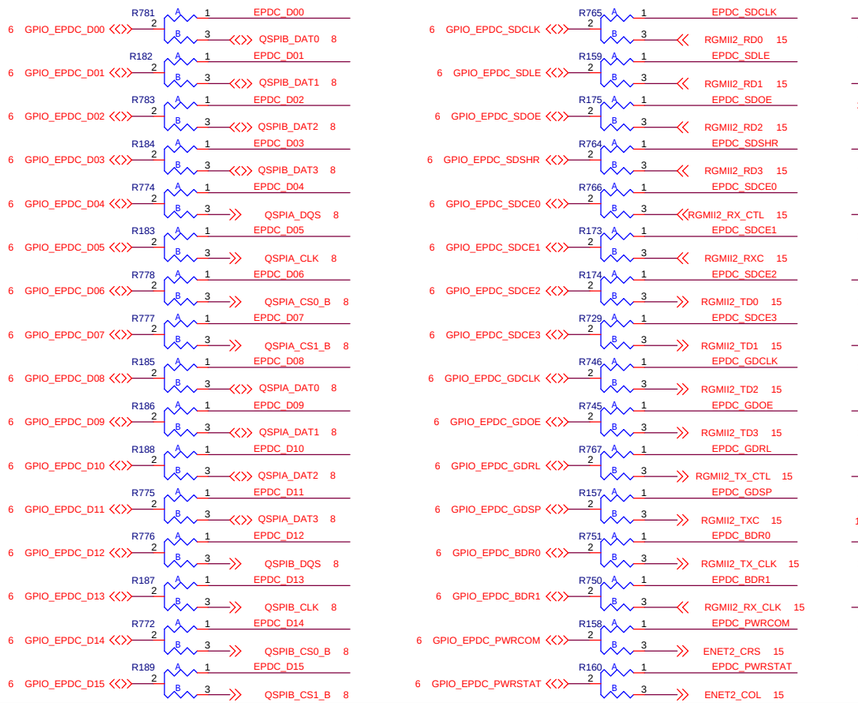
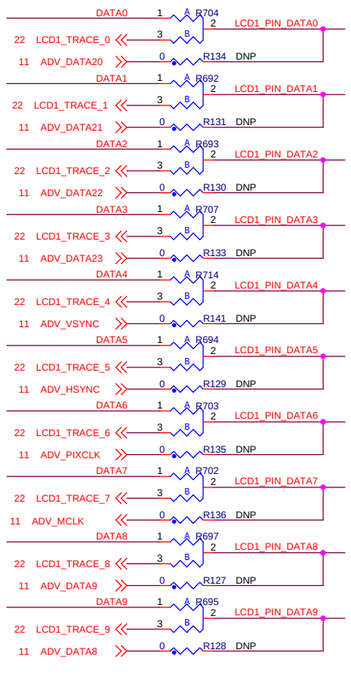
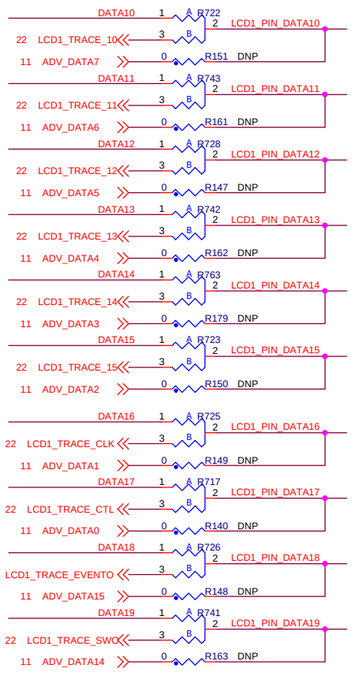
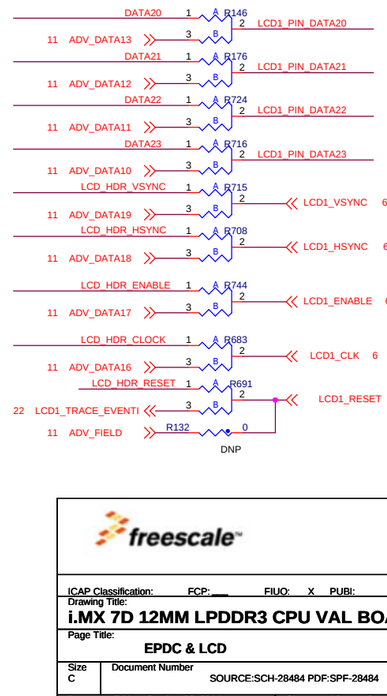


Powered from GPIO2 to allow stylus touch
on screen to wake processor out of deep sleep mode.









freescale

ICAP Classification: FCP: ___ FIUO: X PUBI:

Drawing Title:
i.MX 7D 12MM LPDDR3 CPU VAL BOARD

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EPDC & LCD

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AUDIO

NOTE:
Unless otherwise noted, all 3-way resistors will be populated in the "A" position.

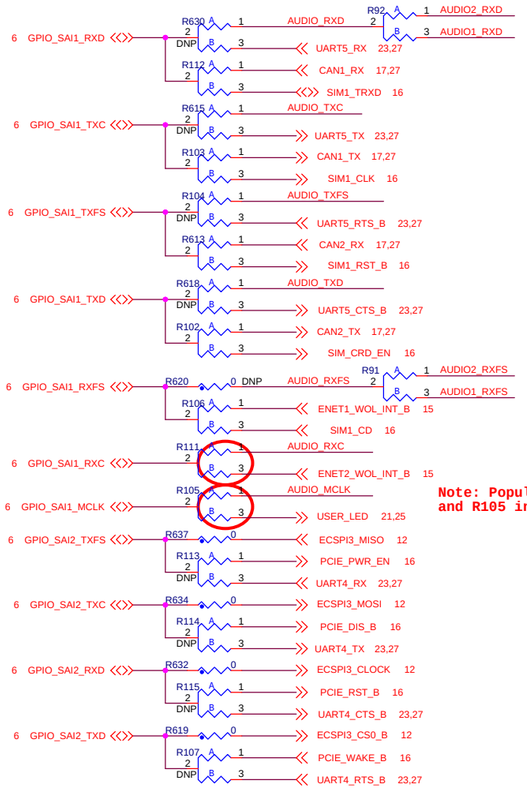
ENGR00334274: SAI1 signals have been changed from supporting Audio CODEC by default to supporting CAN1/2 and GPIO functionality due to signal logic mismatch. Error will be corrected in Rev B,

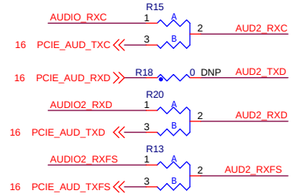
Logic: 1V8

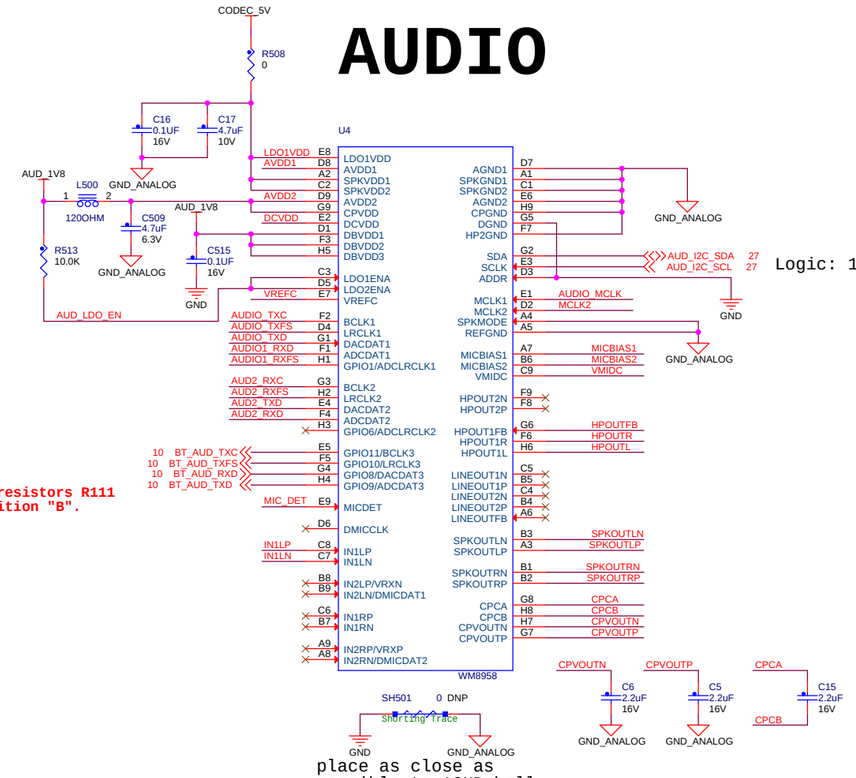
Note: Populate resistors R111 and R105 in position "B".

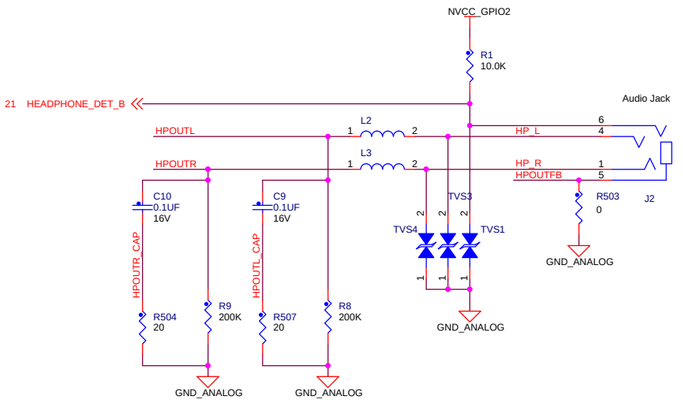
R509 and R516 are added to allow audio opertion if CODEC_PWR_EN GPIO is disabled.

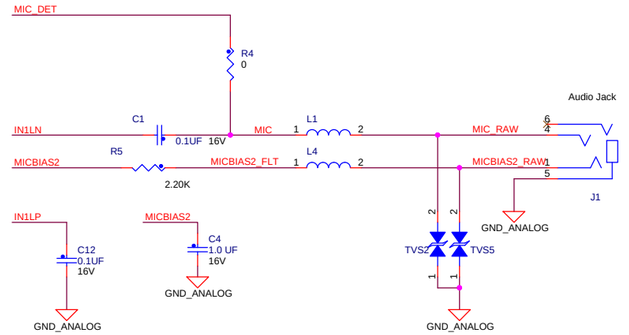
place as close as possible to AGND ball

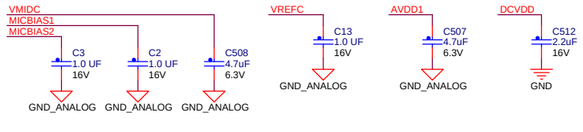


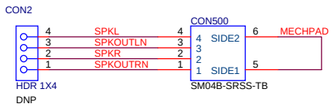


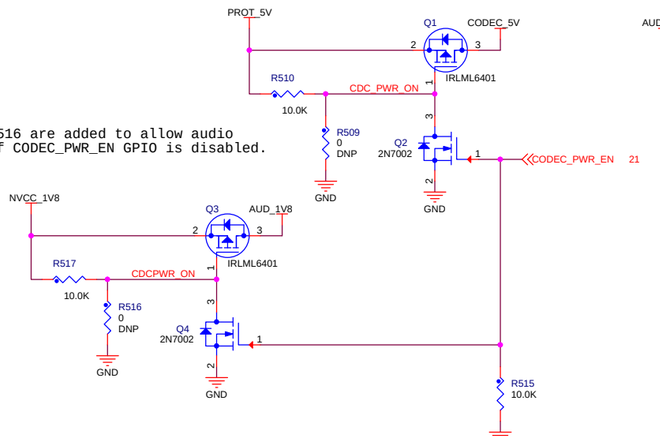


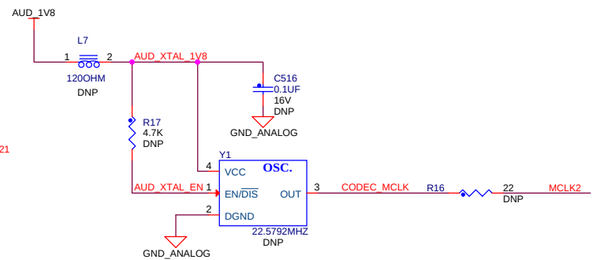












freescale

ICAP Classification: FCP: ___ FIUO: X PUBI:

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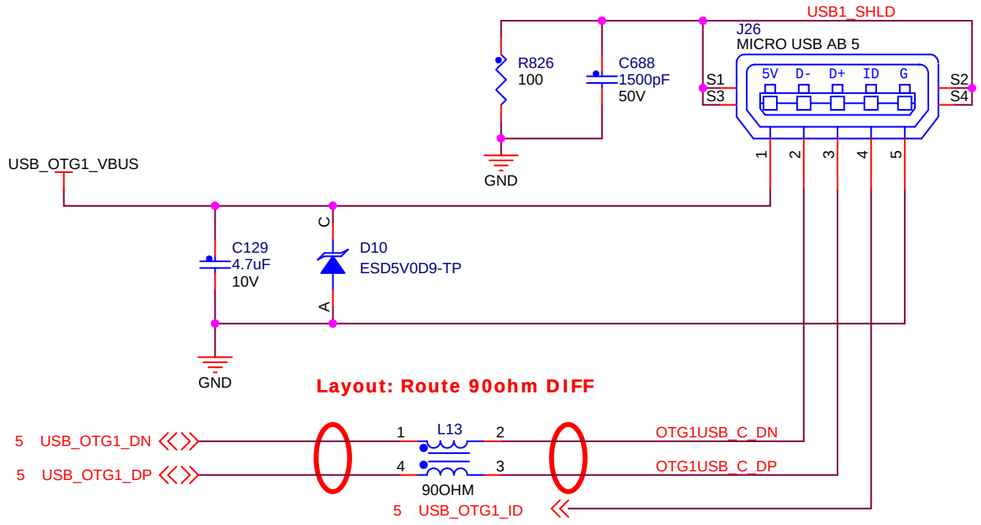
USB

Label = OTG1 USB

USB1 Boot/Debug

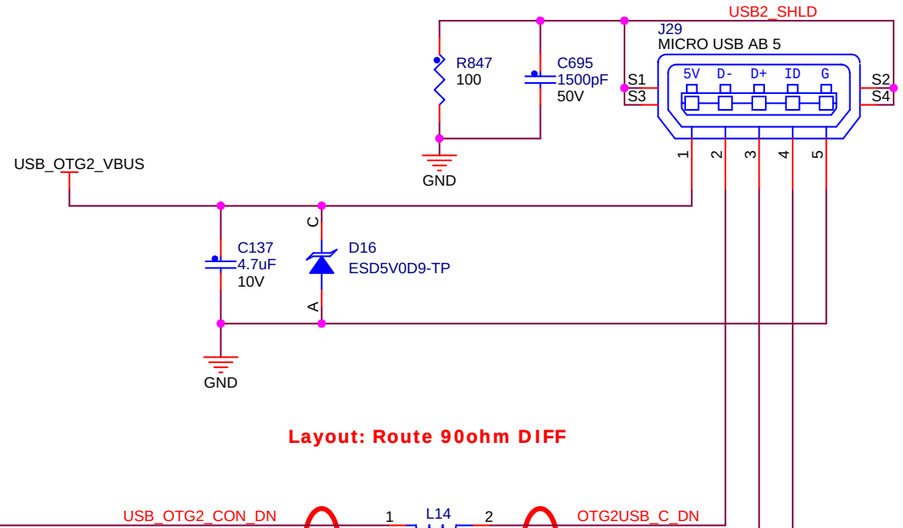
Micro USB-AB Receptacle

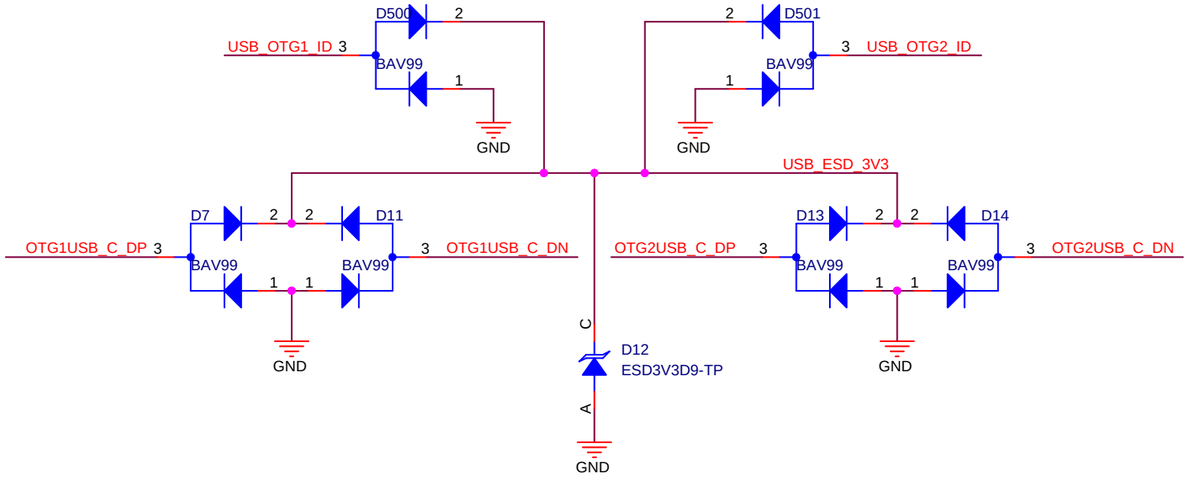


Label = OTG2 USB

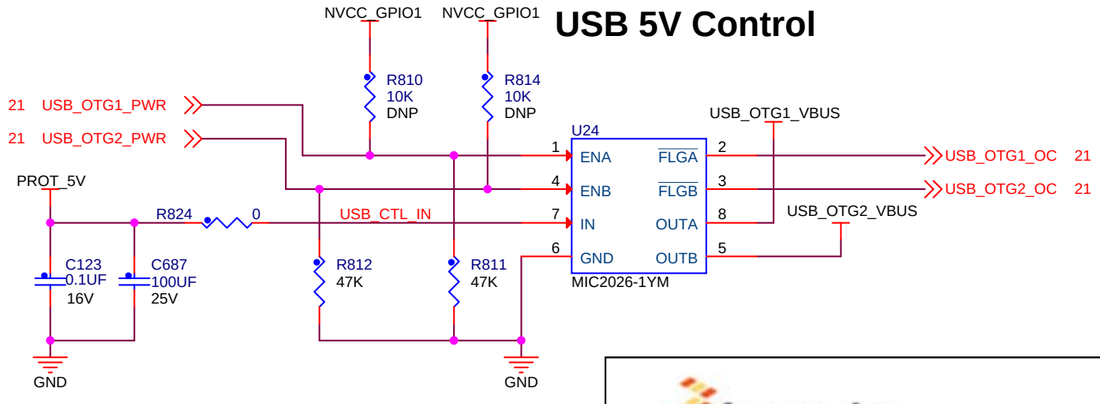
USB2

Micro USB-AB Receptacle





USB 5V Control



NOTE:
USB Superpisory IC supplies a minimum of
500 mA continuous current each channel.

NOTE:
R811 and R812 are populated to ensure supervisory
chip is disabled if power to the PMIC is removed.

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i.MX 7D 12MM LPDDR3 CPU VAL BOARD

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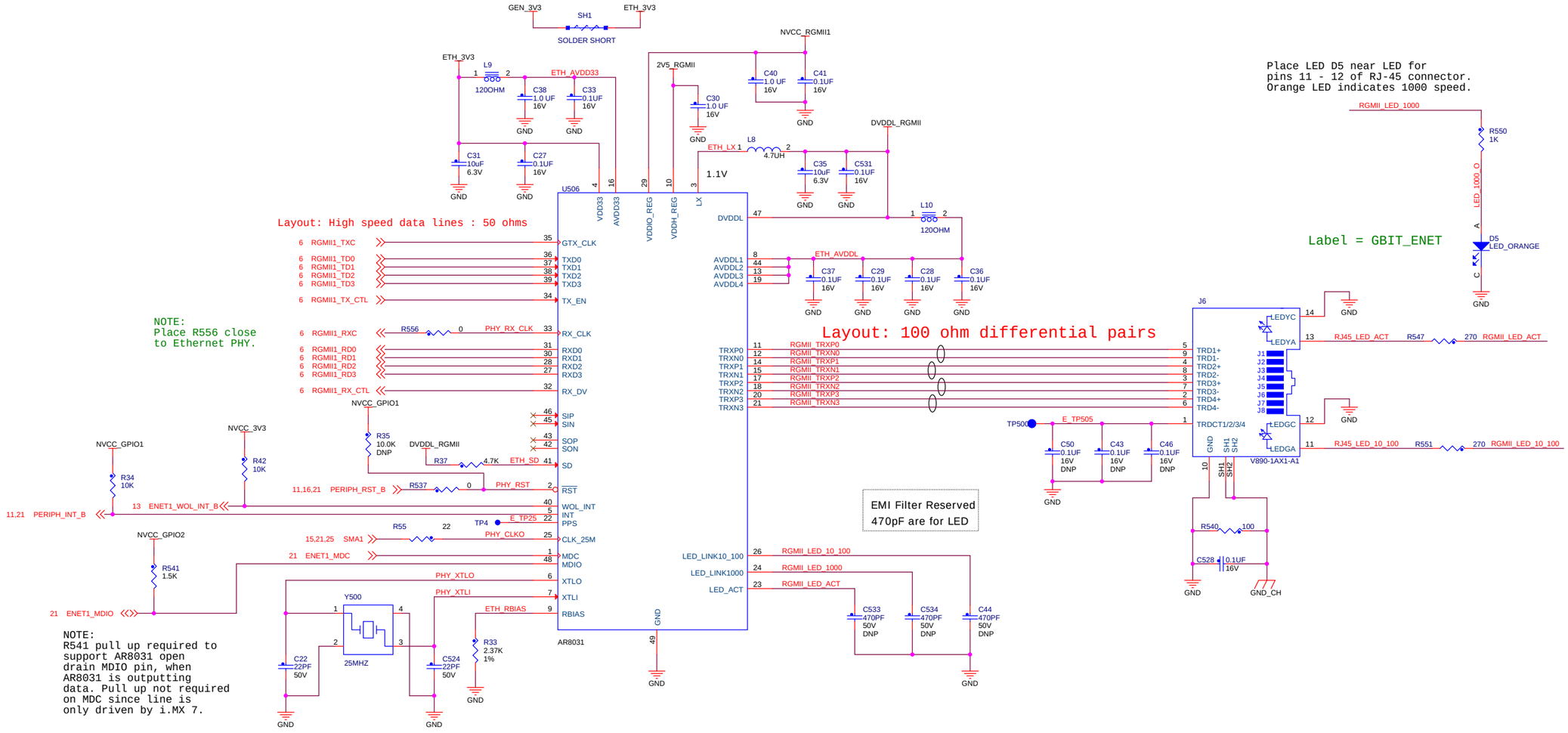
ETHERNET



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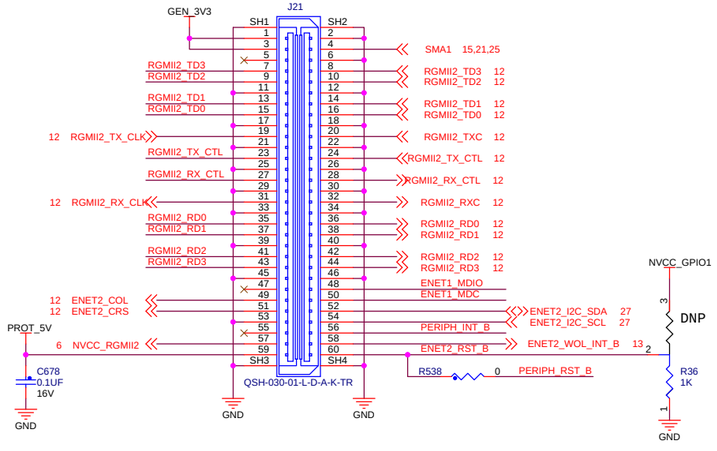
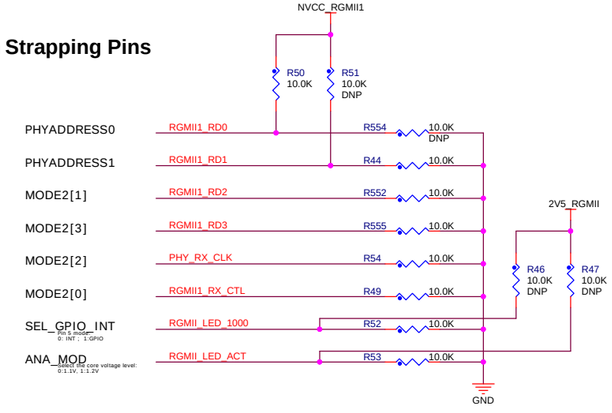


Power-on Strapping Pins



MODE2[3:0]

(Default assemble: 0000)
1100 BaseT, RMII1;
1101 BaseT, RMII2;
1110 100X, RGMII, 75OHMS;
1111 100X, TRANS, 75OHMS;
0000 BaseT, RGMII;
0001 BaseT, SGMII;
0010 1000X, RGMII, 50OHMS;
0011 1000X, RMII, 75OHMS;
0100 1000X, TRANS, 50OHMS;
0101 1000X, TRANS, 75OHMS;
0110 100X, RGMII, 50OHMS;
0111 100X, TRANS, 50OHMS;
Others Reserved

NOTE:
Unless otherwise noted, all
3-way resistors will be
populated in the "A"
position.

freescale

ICAP Classification:	FCP: ___ FIUO: X PUBI:
Drawing Title:	i.MX 7D 12MM LPDDR3 CPU VAL BOARD
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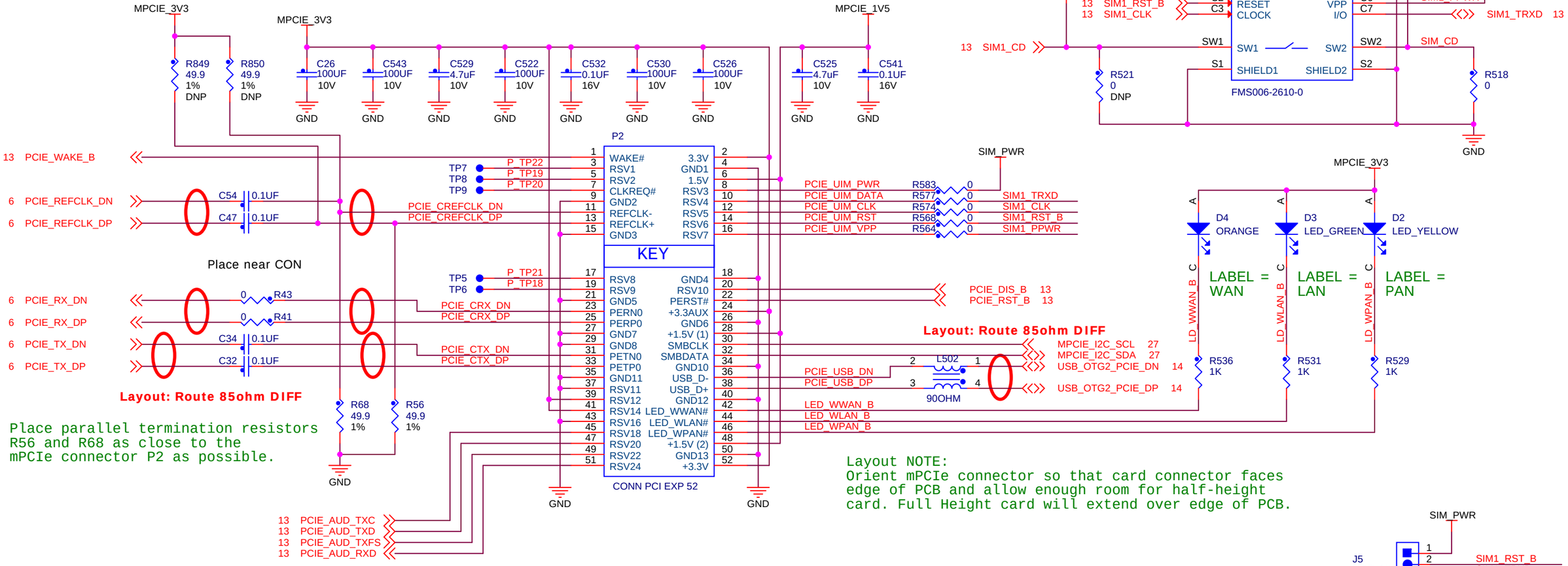
LABEL - MPCIE CONN

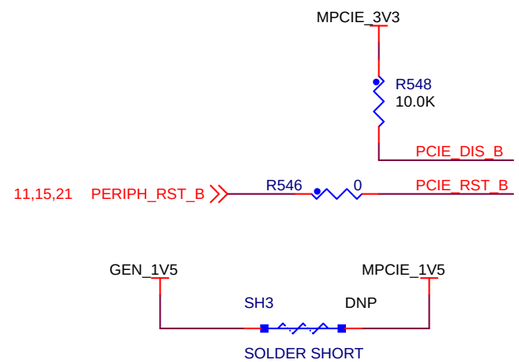
Note:
Pull up resistors R849 and R850 added in case output is HSCL levels and needs to be pulled up.

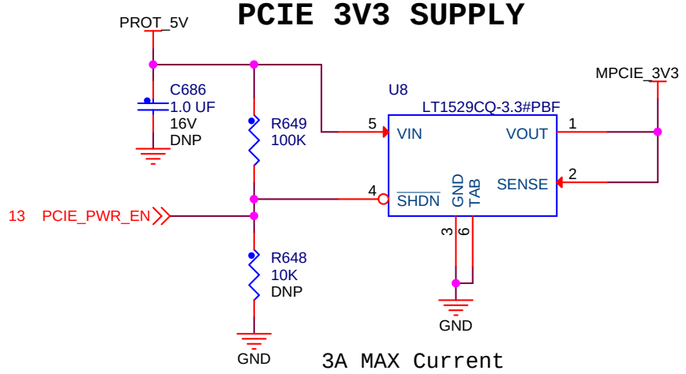


Place parallel termination resistors R56 and R68 as close to the mPCIe connector P2 as possible.

PCIE 3V3 SUPPLY

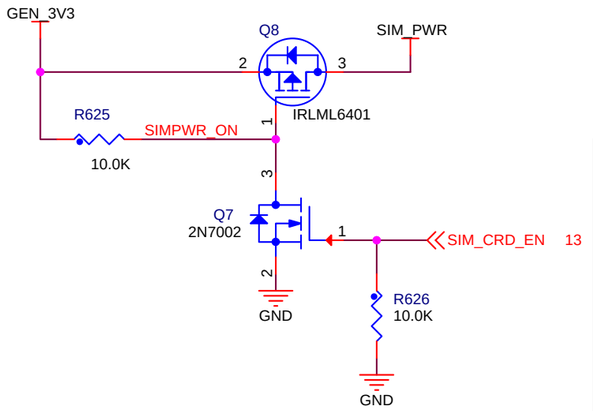
R546, R548 and R649 are populated by default to allow PCIE operation without required GPIO control pins connected.

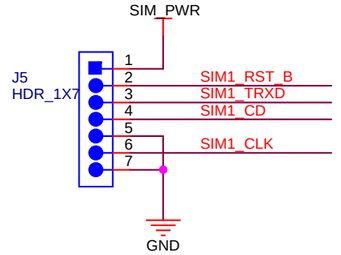




3A MAX Current

No minimum current required for regulation.





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ICAP Classification:	FCP:___ FIUO: __X PUBI:	
Drawing Title:	i.MX 7D 12MM LPDDR3 CPU VAL BOARD	
Page Title:	MPCIE	
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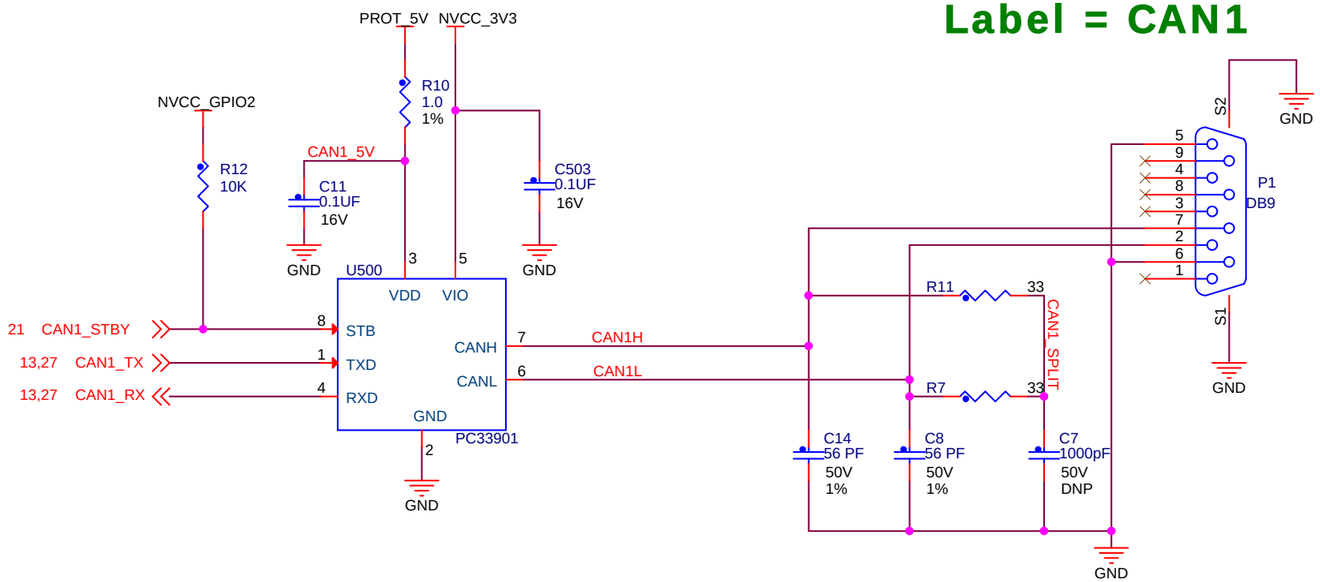
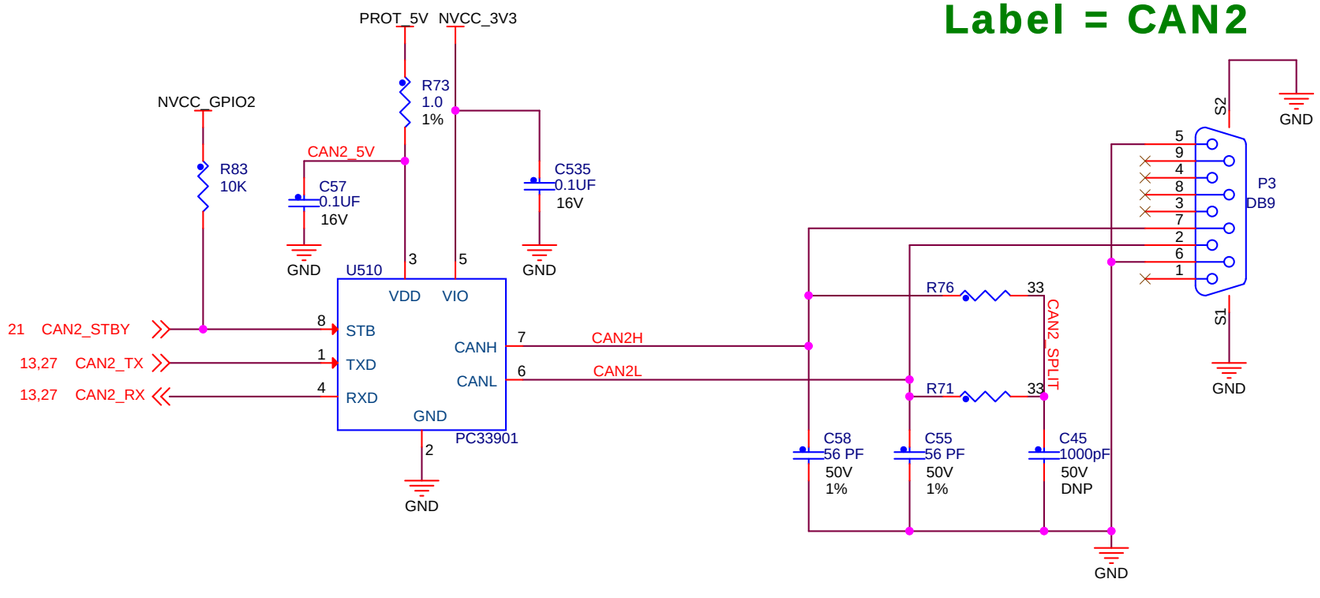
CAN





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CAN

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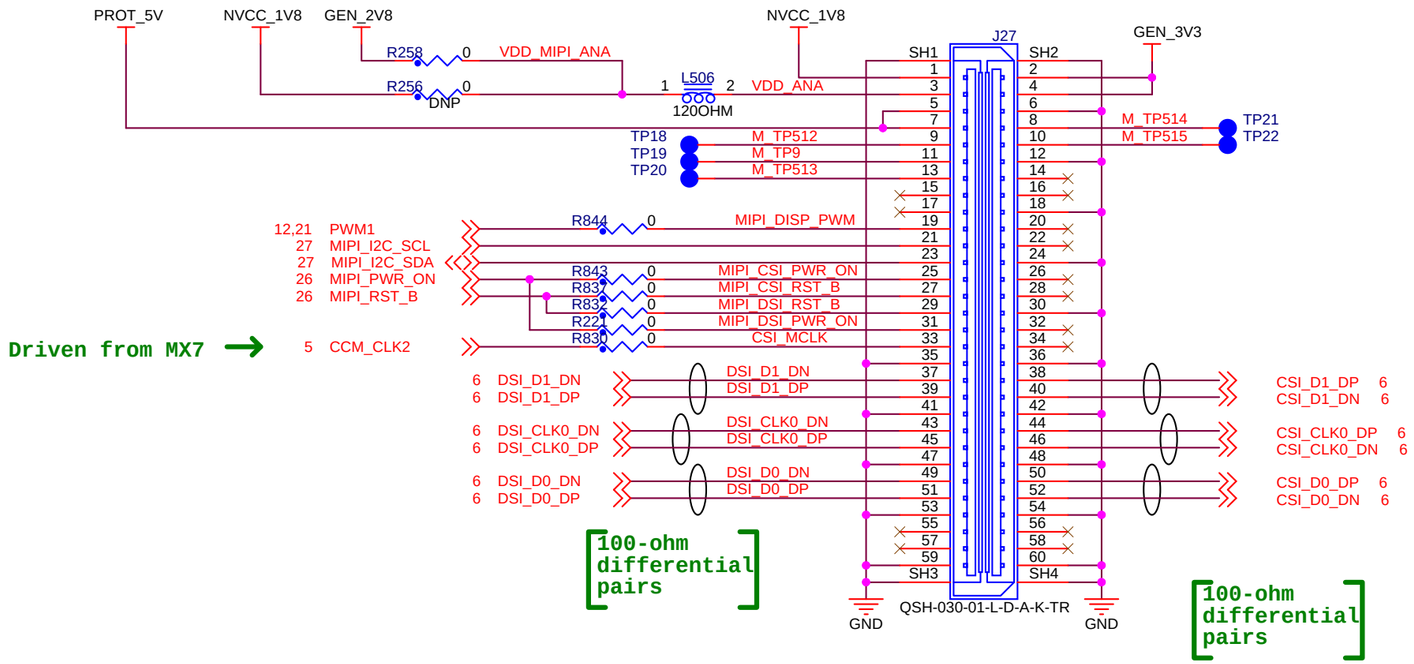
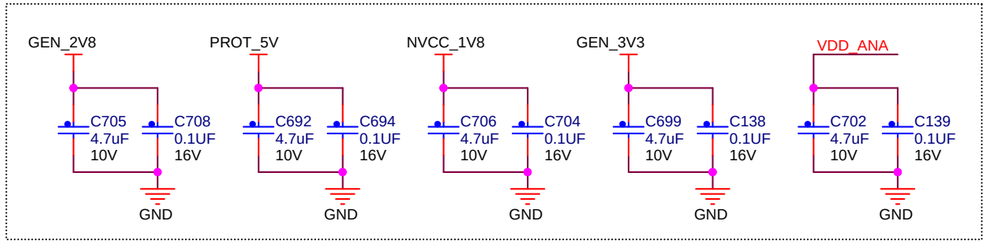
LABEL = MIPI HDR



Analog Devices ADV7280 SD video decoder card may be used with cable. Contact ADI for more information.



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ICAP Classification: FCP:___ FIUO: X PUBI:

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MIPI

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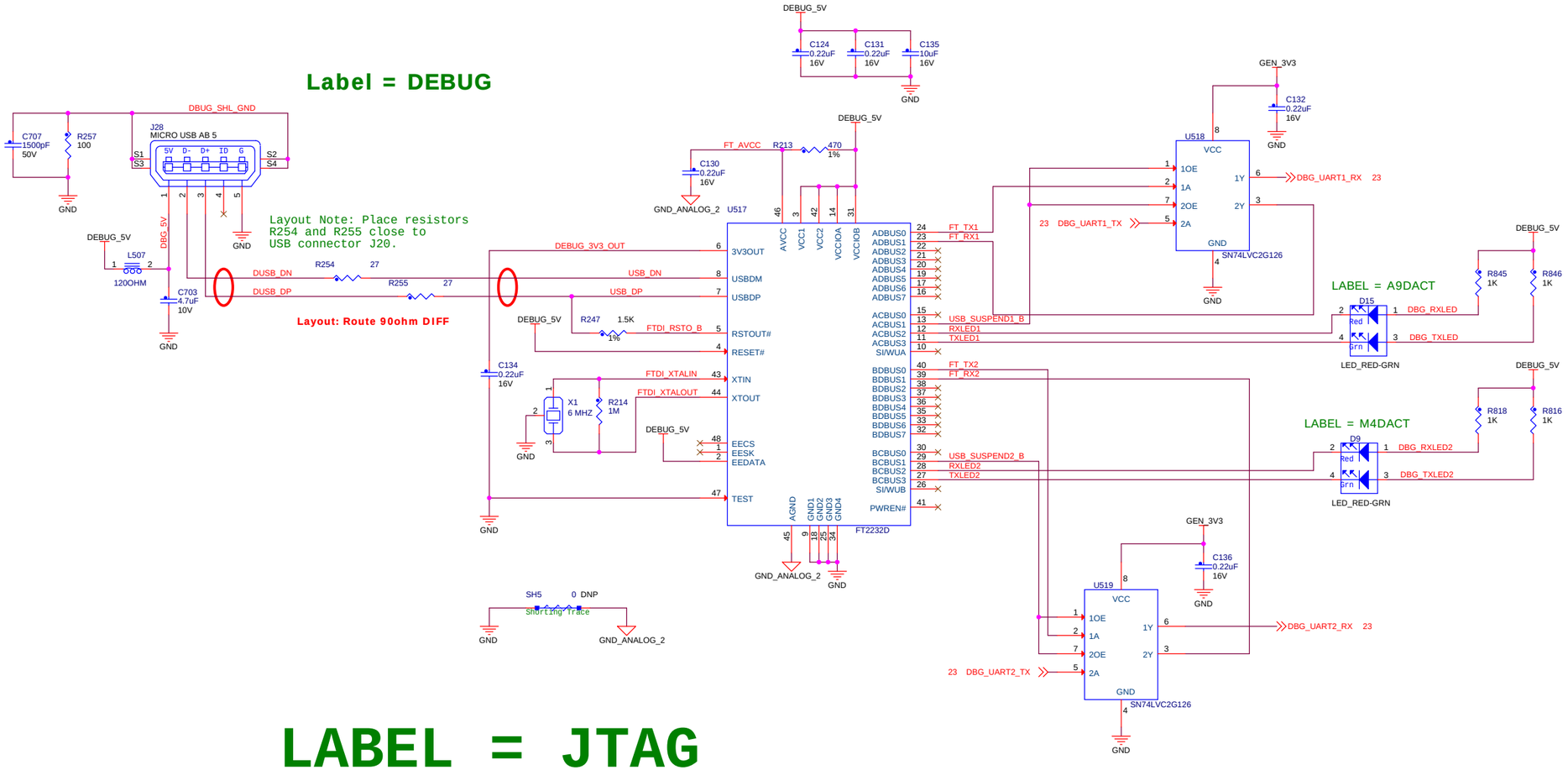
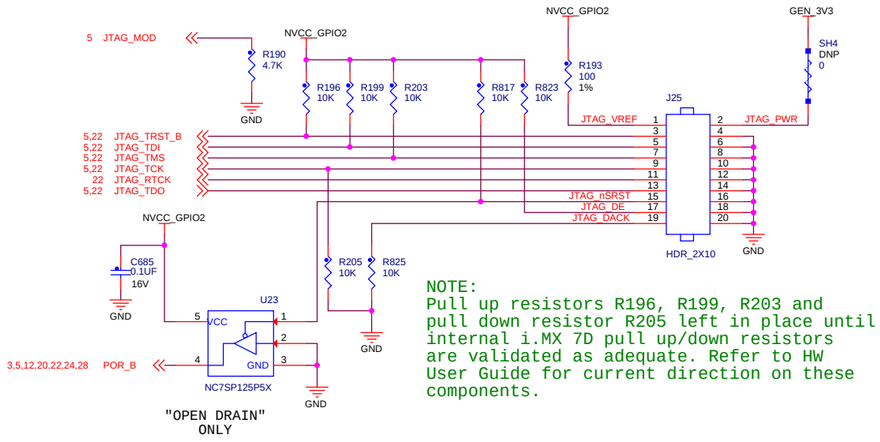
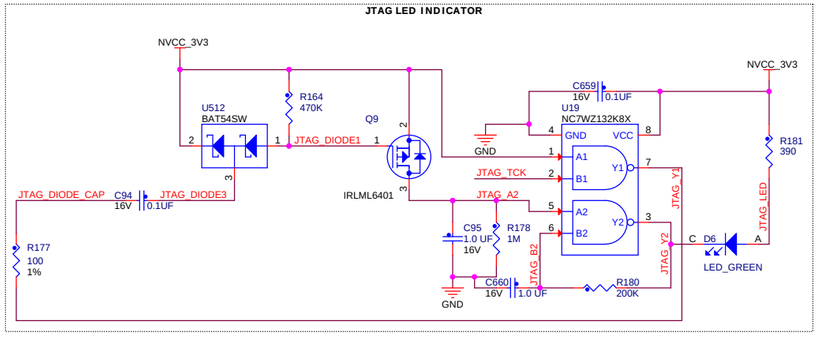
DEBUG UART TO USB CONVERSION

Label = DEBUG



LABEL = JTAG





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ICAP Classification: FCP: ___ FIUO: X PUBI:

Drawing Title: **i.MX 7D 12MM LPDDR3 CPU VAL BOARD**

Page Title: **JTAG & DEBUG**

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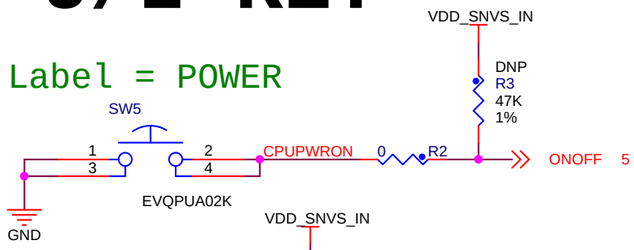
U/I KEY

Label = POWER



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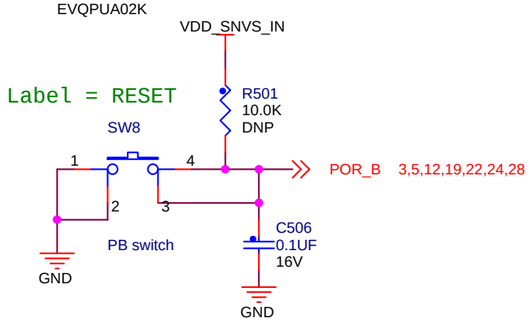

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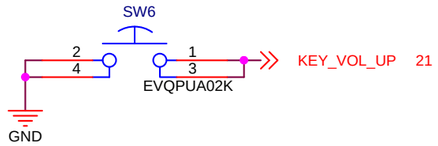

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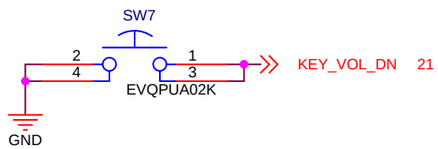
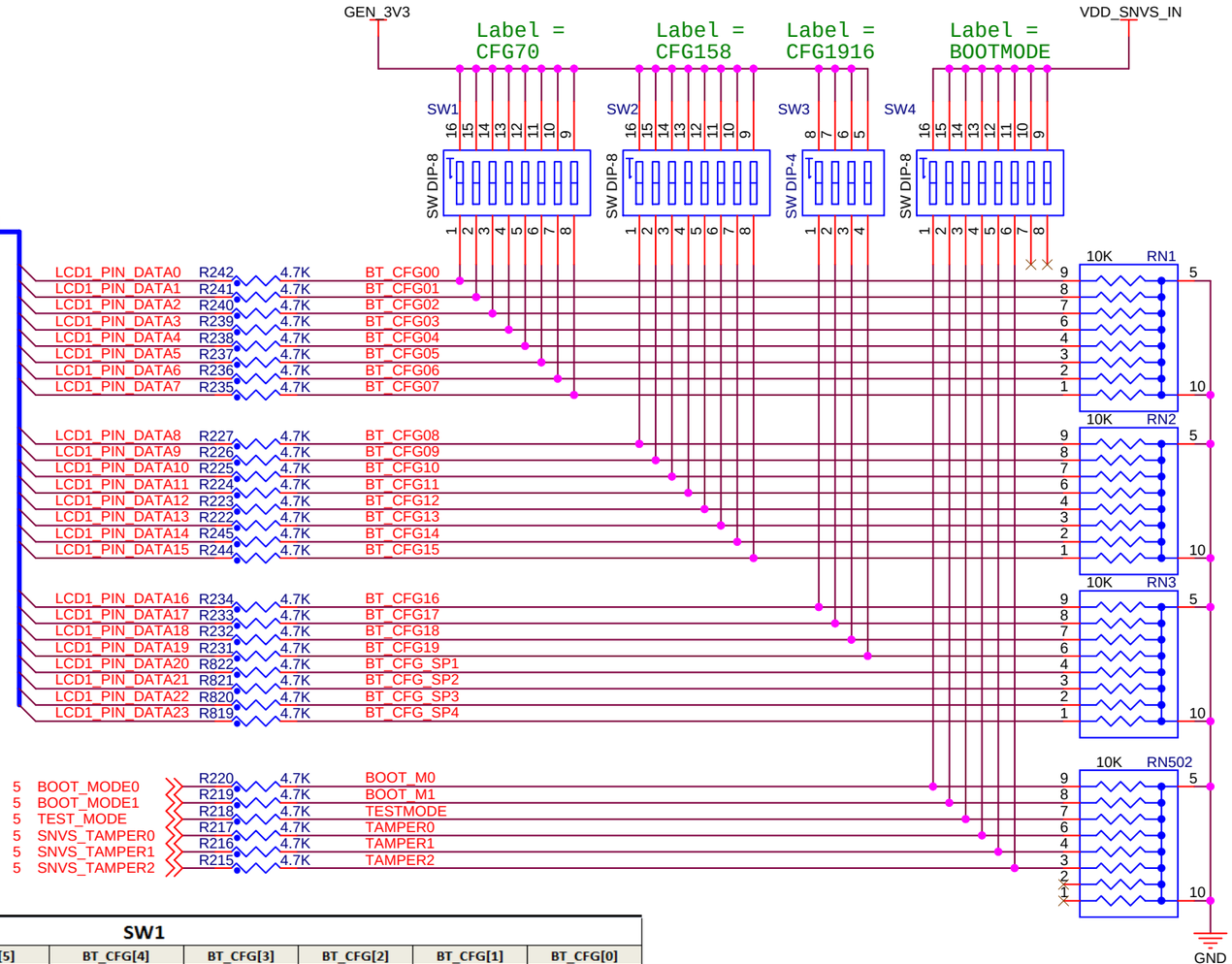


BOOT

Boot Configuration Select

Switch mapping with the configuration options is described on the Notes page of the schematics.

6,12 LCD1_PIN_DATA[0:23]



SW3			
BT_CFG[19]	**BT_CFG[18]**	**BT_CFG[17]**	**BT_CFG[16]**
Infinit-Loop (Debug USE only) 0 - Disable 1- Enable	Boot Frequencies (ARM/DDR) 0 - 792 / 533 MHz 1 - 396/ 266 MHz	Recovery Boot Enable '0' - Disabled '1' - Enabled	BT_MMU_DISABLE '0' - Enabled '1' - Disabled

SW4					
BOOT_MODE0	**BOOT_MODE1**	**TEST_MODE**	**SNVS_TAMPER0**	**SNVS_TAMPER1**	**SNVS_TAMPER2**
Boot Mode 00 - Boot From Fuses 01 - Serial Downloader 10 - Internal Boot 11 - Reserved		Processor Test Mode '0' - Disabled '1' - Enabled	Tamper Signal 0 '0' - No Detect '1' - Tamper Detect	Tamper Signal 1 '0' - No Detect '1' - Tamper Detect	Tamper Signal 2 '0' - No Detect '1' - Tamper Detect

SW2								SW1							
BT_CFG[15]	**BT_CFG[14]**	**BT_CFG[13]**	**BT_CFG[12]**	**BT_CFG[11]**	**BT_CFG[10]**	**BT_CFG[9]**	**BT_CFG[8]**	**BT_CFG[7]**	**BT_CFG[6]**	**BT_CFG[5]**	**BT_CFG[4]**	**BT_CFG[3]**	**BT_CFG[2]**	**BT_CFG[1]**	**BT_CFG[0]**
0001 - SD/eSD				Port Select: 00 - eSDHC1 01 - eSDHC2 10 - eSDHC3		Power Cycle Enable '0' - No power cycle '1' - Enabled via	SD Loopback Clock Source Sel(for SDR50 and SDR104 only) '0' - through SD pad '1' - direct	Fast Boot: 0 - Regular 1 - Fast Boot	Reserved	Reserved	Bus Width: 0 - 1-bit 1 - 4-bit	Speed 000 - Normal/SDR12 001 - High/SDR25 010 - SDR50 011 - SDR104 101 - Reserved for DDR50 Others - Reserved			Reserved
0010 - MMC/eMMC								Bus Width: 000 - 1-bit 001 - 4-bit 010 - 8-bit 101 - 4-bit DDR (MMC 4.4) 110 - 8-bit DDR (MMC 4.4) Else - reserved.				Speed 00 - Normal 01 - High 10 - Reserved for HS200 11 - Reserved		USDHC1 IO VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	USDHC2 IO VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V
0100 - QSPI				QSPI Instance 0 - QuadSPI0 1 - Reserved	SDR SMP: "000" : Default "001-111"			**HSPHS: Half Speed Phase Selection** 0 : select sampling at non-inverted clock 1: select sampling at inverted clock	**HSDLY: Half Speed Delay selection** 0 : one clock delay 1: two clock delay	**FSPHS: Full Speed Phase Selection** 0 : select sampling at non-inverted clock 1: select sampling at inverted clock	**FSDLY: Full Speed Delay selection** 0 : one clock delay 1: two clock delay	Reserved	Reserved	Reserved	Reserved

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BOOT

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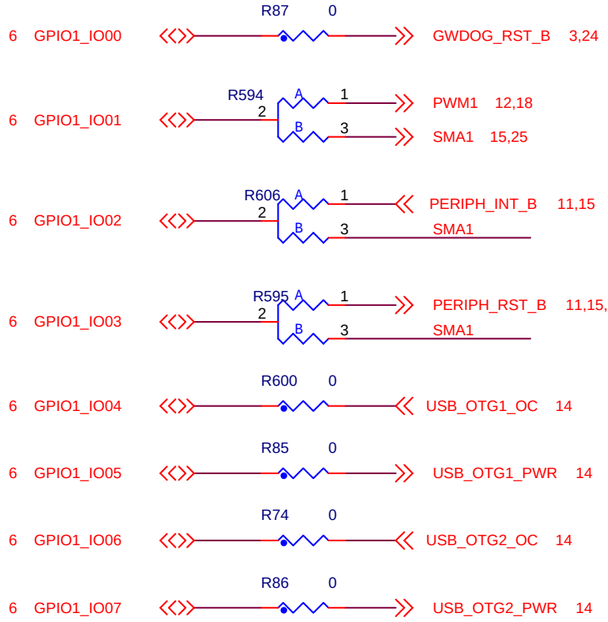
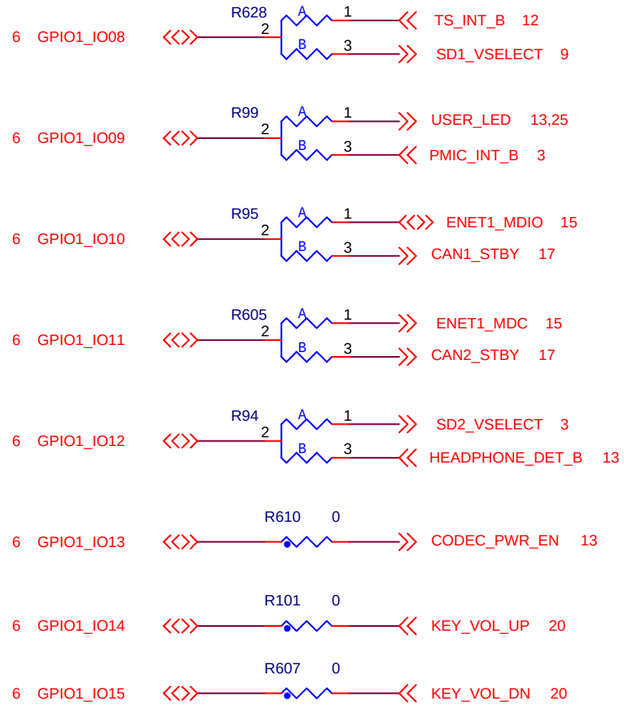
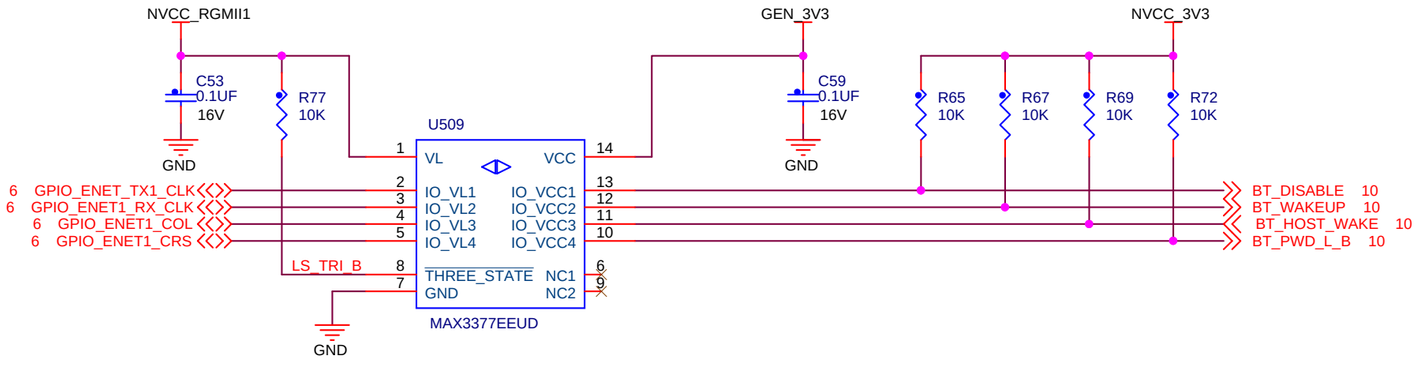
GPIO







NOTE:
Unless otherwise noted, all 3-way resistors will be populated in the "A" position with 0 Ohm resistors.

Note:
U509 is Level Shifter to bring GPIO signals from NVCC_ENET1 up to 3.3V levels.

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ICAP Classification: FCP:___ FIUO: X PUBI:

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GPIO

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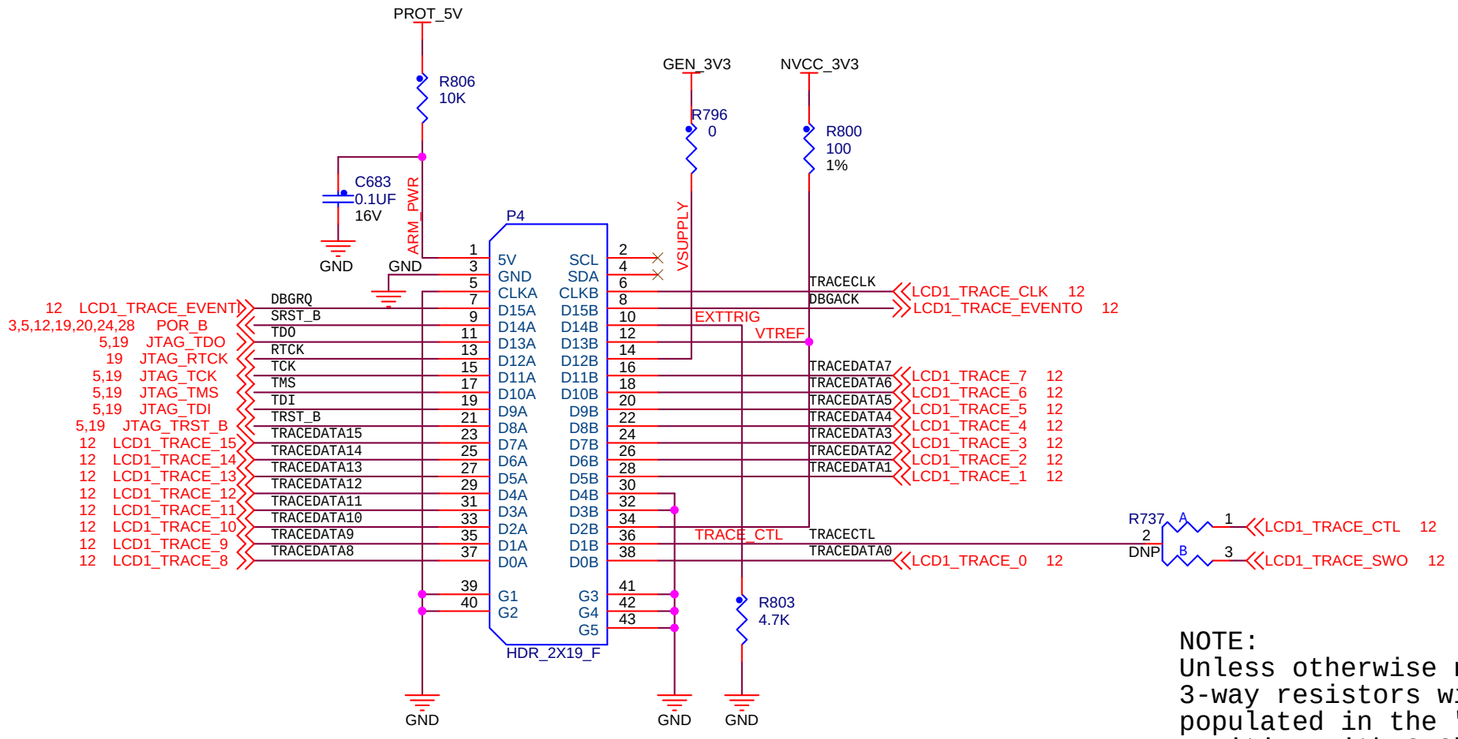
LABEL = ARMTRACE



LAYOUT NOTE:
ARM Trace connector traces need to be less than 1 inch in length. Place P4 as close to processor as possible.

NOTE:
Unless otherwise noted, all 3-way resistors will be populated in the "A" position with 0 Ohm resistors.

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ICAP Classification: FCP:___ FIUO: _X_ PUBI:

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ARM TRACE

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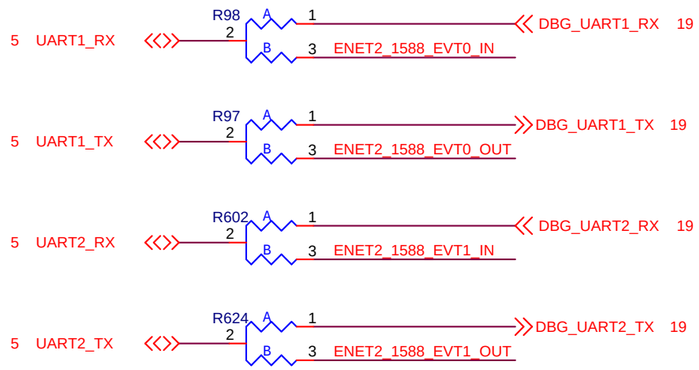
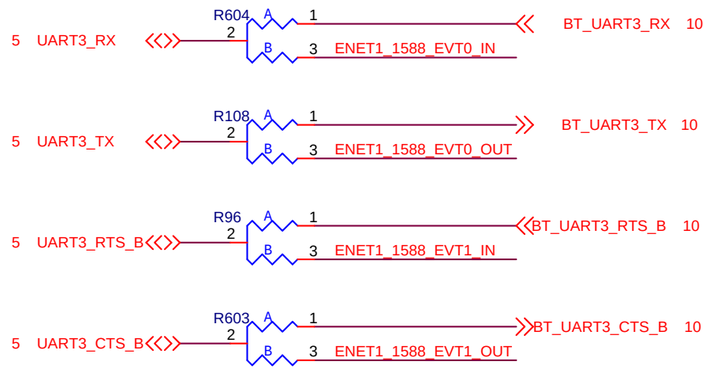
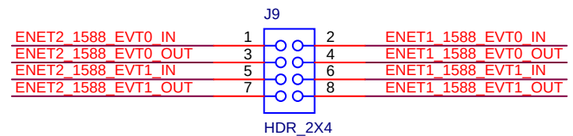
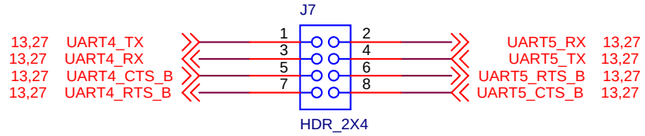
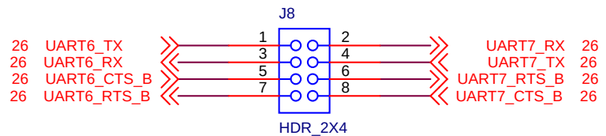
UART











NOTE:
Unless otherwise noted, all 3-way resistors will be populated in the "A" position with 0 Ohm resistors.

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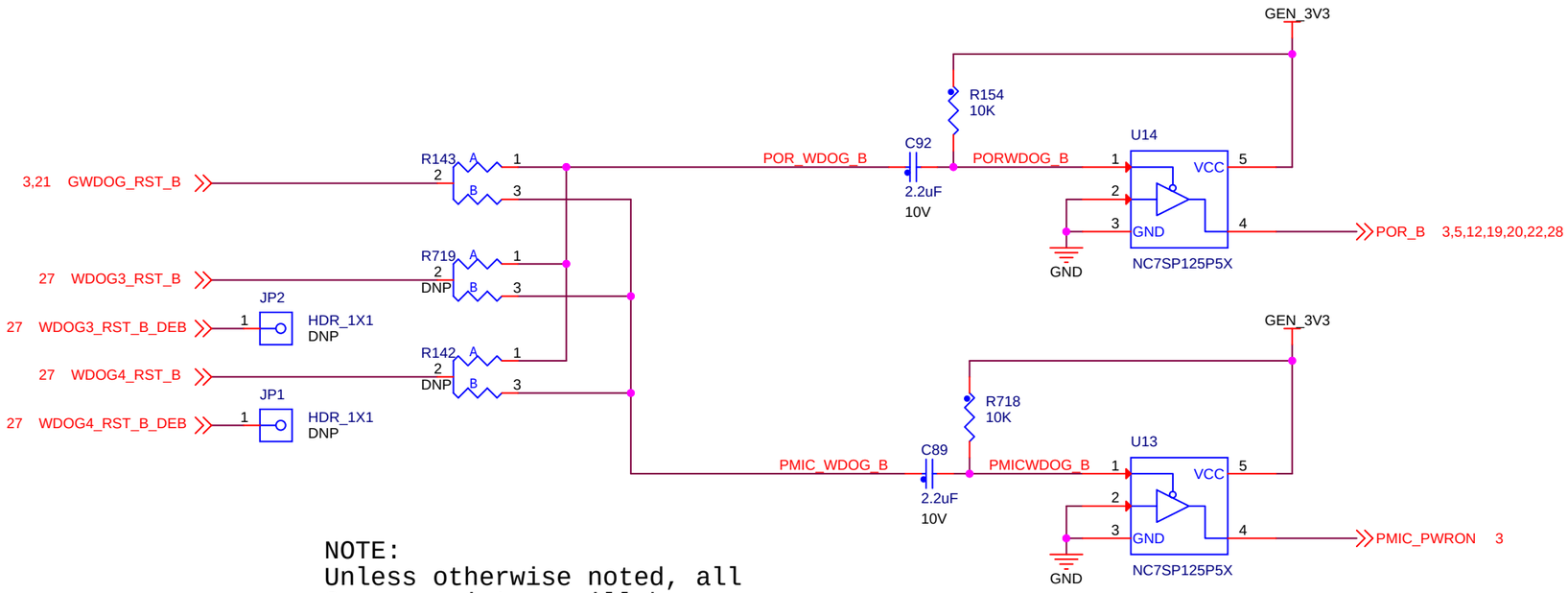
WDOG

WATCH DOG TIMER BUFFERS:
Capacitors C89 and C92 act as Blocking Capacitors.
When circuit is initialized, WDOG pin are held high and
keep buffers turned off. When WDOG engages, pins go
low and cause buffers to turn on and initiate a reset signal.
In a power down reset, WDOG does not return high until
power is turned back on. Capacitors allows OE signal on
buffer to return high after a short period regardless of
whether WDOG pin is powered or not.



NOTE:
Unless otherwise noted, all
3-way resistors will be
populated in the "A"
position with 0 Ohm
resistors.

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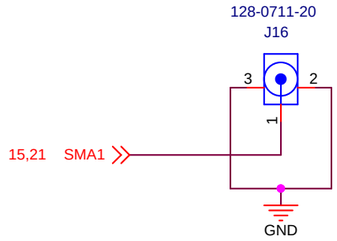
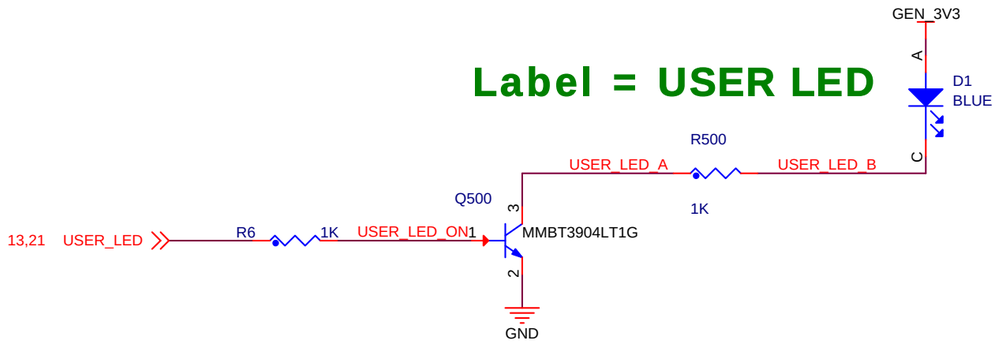
CLOCK_OUT

Label = ACLKO



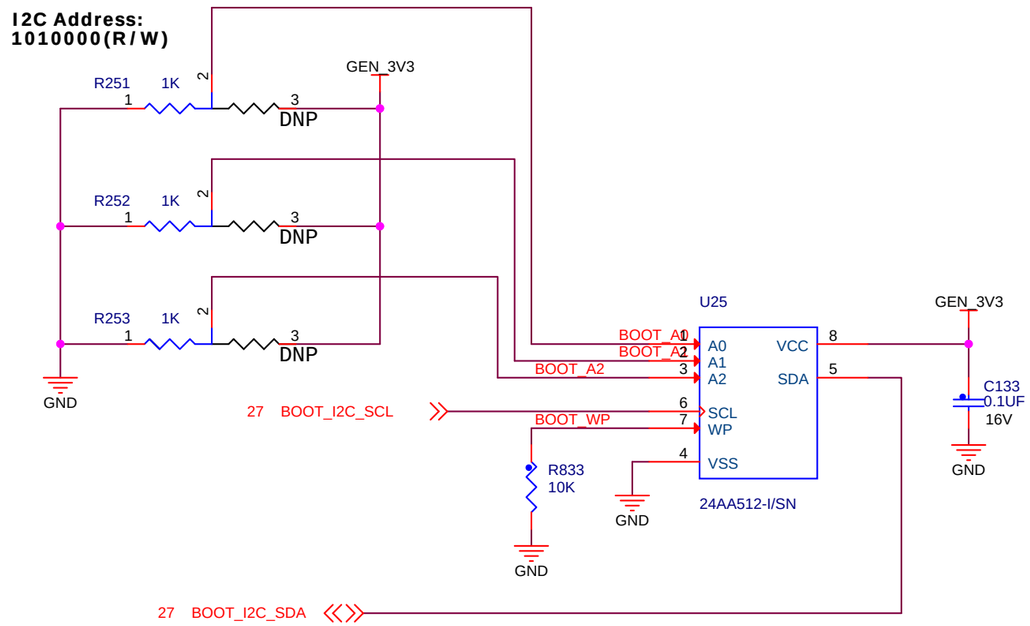
USER LED

Label = USER LED



Configuration I2C EEPROM

(For testing only)



NOTE:
Default XY program loading is across pins 1-2.

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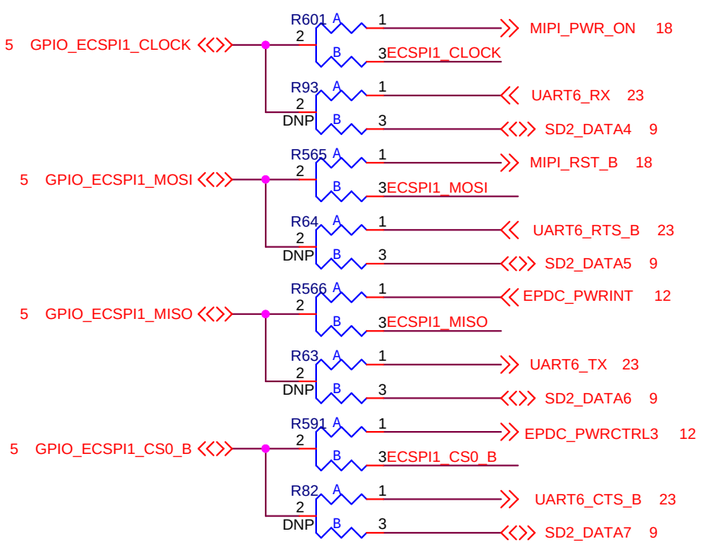
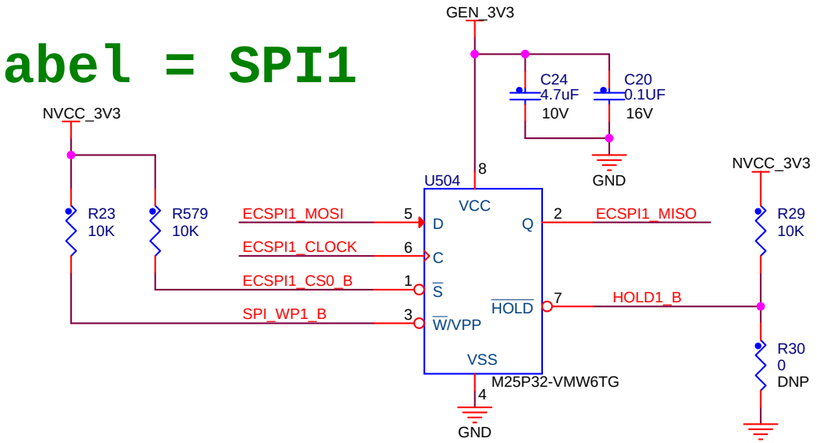
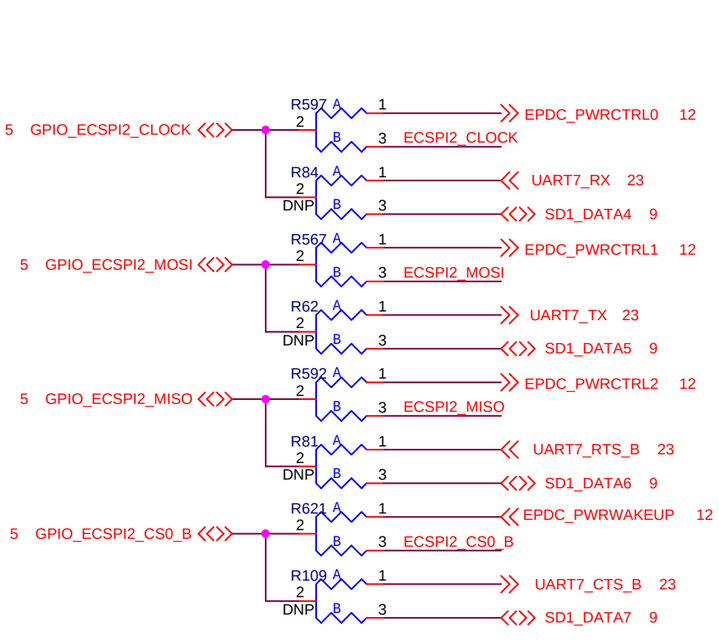
ECSPI

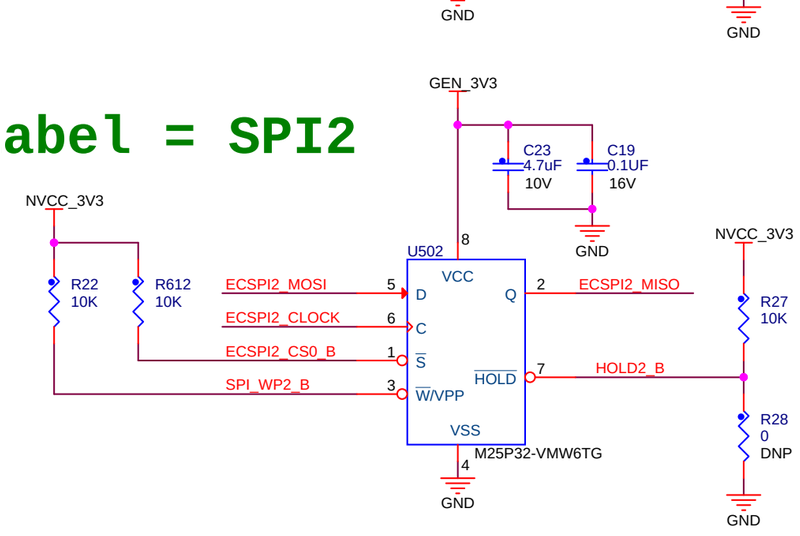
Label = SPI1





Label = SPI2





NOTE:
Unless otherwise noted, all 3-way resistors will be populated in the "A" position with 0 Ohm resistors.

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I2C

I2C1 BUS

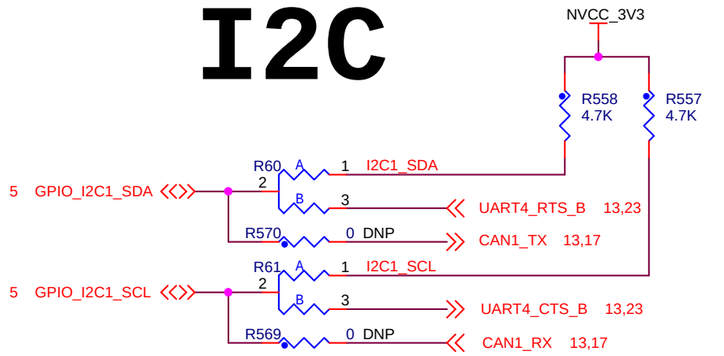
Peripheral	Speed (kpbs)	8-Bit Write Addressses	Default Write Address
PMIC	400	0x10 to 0x1E	0x10
EEPROM	400	0x10 to 0x37	0x30
ADV7401	400	0x21, 0x23	0x23

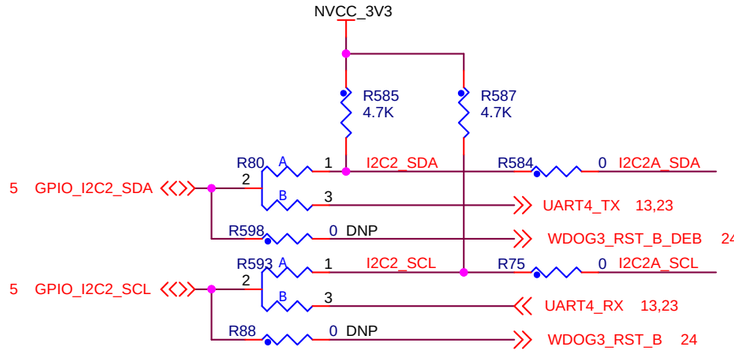
I2C2 BUS

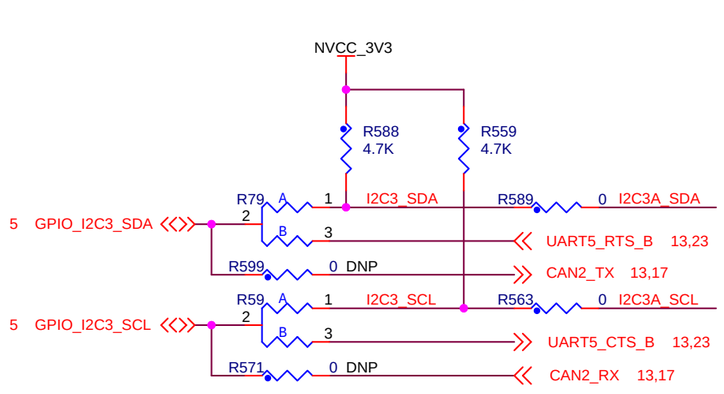
Peripheral	Speed (kpbs)	8-Bit Write Addressses	Default Write Address
ADV7401	400	0x40 to 0x42	0x10
i.MX28 LCD	400	0x68 to 0x6B	0x6B
MIPI OV5640	400	0x3C	0x3C
MIPI Touchscreen	400	0x48 to 0x4B	0x4B

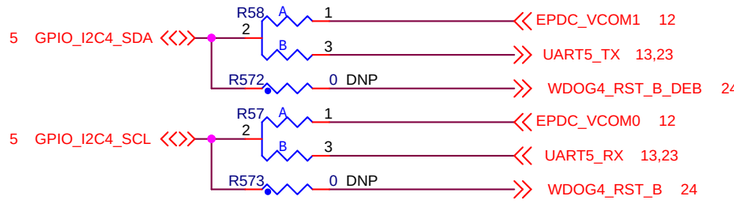
I2C3 BUS

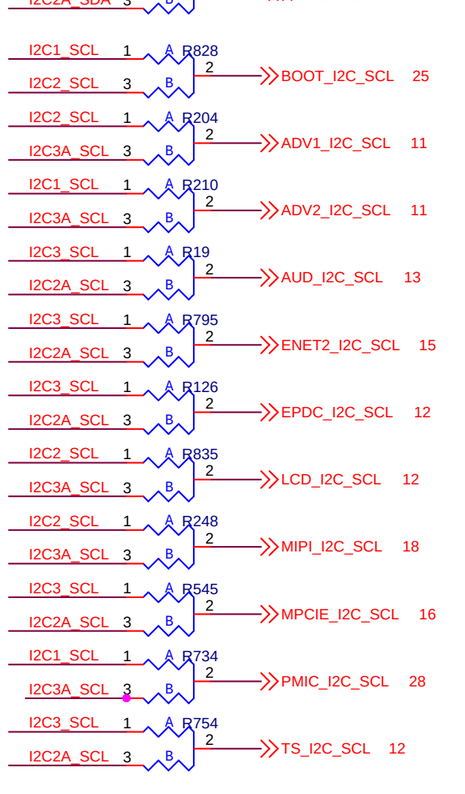
Peripheral	Speed (kpbs)	8-Bit Write Addressses	Default Write Address
ADV7401	400	0x40 to 0x42	0x10
i.MX28 LCD	400	0x68 to 0x6B	0x6B
MIPI OV5640	400	0x3C	0x3C
mPCIe MODULE	TBD	TBD	TBD
ENET2 DC	TBD	TBD	TBD











NOTE:
Unless otherwise noted, all 3-way resistors will be populated in the "A" position with 0 Ohm resistors.

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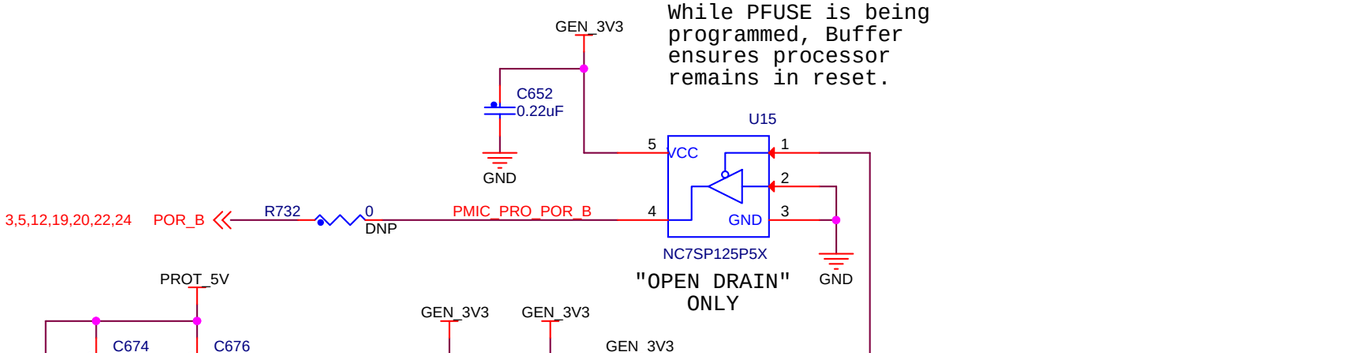
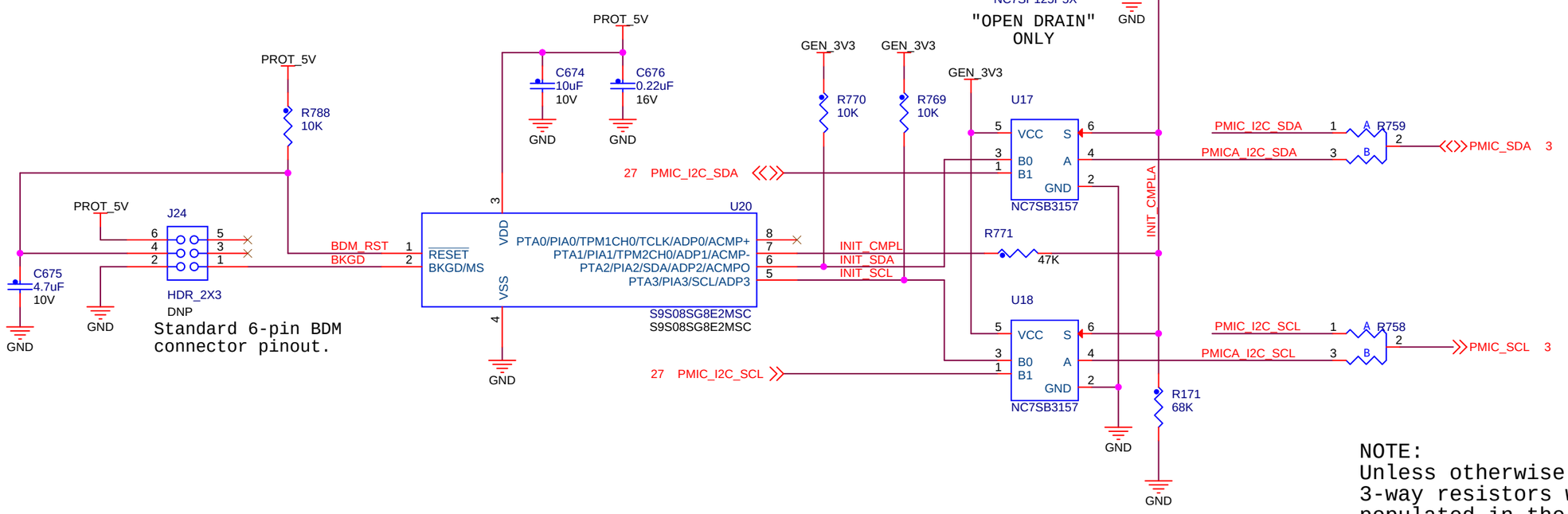
PMIC PROGRAMMING

While PFUSE is being programmed, Buffer ensures processor remains in reset.





NOTE:
Unless otherwise noted, all 3-way resistors will be populated in the "A" position with 0 Ohm resistors.

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PMIC PROGRAMMING

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PIN MUX TABLE

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HISTORY OF TEMPORARY DEVIATIONS

CLEARQUEST ISSUES

REV:	CHANGE:	REFERENCE DEFECT NUMBER:
A1	Audio CODEC is configured for SAI signals and I2C signals at a TTL level of 1.8V. The signal levels coming from the Processor are set for TTL of 3.3V. Therefore, SAI1 signals are being set by default to CAN1/2 and GPIO functionality.	ENGR00334274

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