FETIMX6UL

Schematics DevBoard

Table of Content

Revision History

Rev. Code	Date	By	Description
A	2015-02-28	Javen	1 Revision A release
B	2015-05-04	Javen	

1. Unless Otherwise Specified:

   All resistors are in ohms, 10%, 1/8 Watt,0603
   All capacitors are in uF, 20%, 50V,0603
   All voltages are DC
   All polarized capacitors are aluminum electrolytic

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

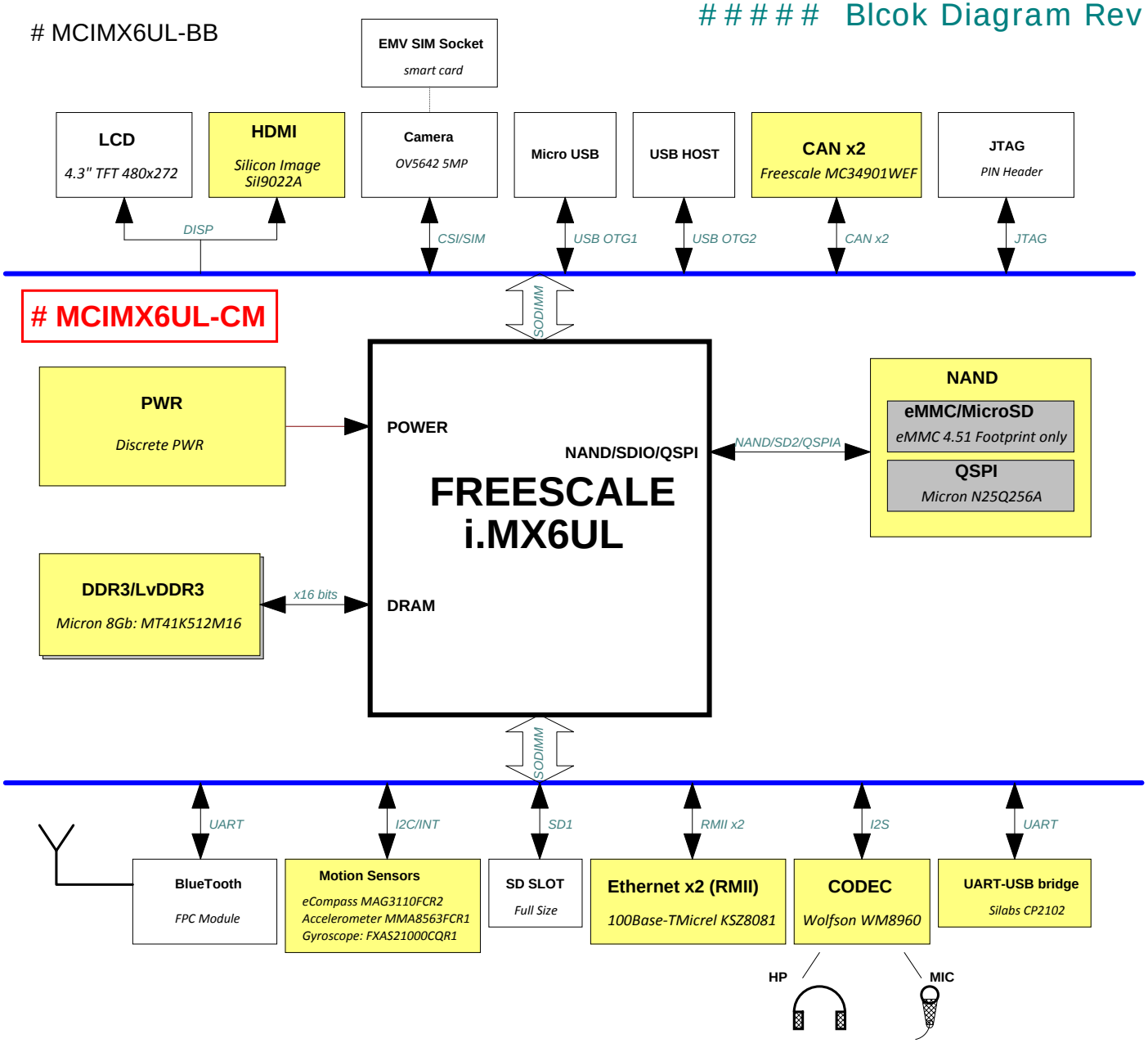
4. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

i.MX6UL EVK Block Diagram

Blcok Diagram Rev 1.0

MPN: MCIMX6UL-BB Agile No: 28616
MPN: MCIMX6UL-CM Agile No: 28617



i.MX6UL EVK PWR TREE

WALL Adapter: 5V/3A

OVP

VSYS
5V/3A

MCIMX6UL-BB

Always ON
LDO
RICHTEK RT9169
3.3V/100mA Iq = 4uA
VDD_SNVS_IN

PMIC_ON_REQ
DC/DC BUCK
MPS MP2144
3.3V/2A Iq=40uA
VDD_HIGH_IN
DCDC_3V3

DCDC_3V3_PG
DC/DC BUCK
MPS MP2159
1.275V/1A Iq=40uA
VDDARM_IN

DCDC_3V3_PG
DC/DC BUCK
MPS MP2159
1.35V/1A Iq=40uA
VDD_MEM1V5

1.8V for eMMC HS200 mode
LDO
RICHTEK RT9169
1.8V/100mA Iq = 4uA

DCDC_3V3
HIGH PSRR LDO
RICHTEK RT9193
3.3V/300mA
VLDO_3V3

DCDC_3V3_PG
LDO
UNION UM1750S
1.8V/3.3V/300mA
NVCC_SD (3.3V/1.8V)

1.8V for CSI;
1.8V/3.3V for SIM
DCDC_3V3
LDO
UNION UM1750S
2.8V/300mA
NVCC_CSI (1.8V/3.3V)

USB_OTGx_PWR
LOAD SW
USB_OTG_VBUS
USB_HOST_VBUS

VDD_SNVS_IN
276uA
LDO_SNVS
VDD_SNVS_CAP

LDO_1P1
NVCC_PLL

VDD_HIGH_IN
125mA
LDO_2P5
VDD_HIGH_CAP

NVCC_GPIO/NVCC_ENET/NVCC_LCDIF
NVCC_DRAM_2P5

VDD_SOC_IN
900mA
LDO_ARM_SOC
VDD_ARM_CAP
VDD_SOC_CAP

NVCC_DRAM
50mA
NVCC_NAND

FSL i.MX6UL CPU

VDDA_ADC_3P3
35mA

NVCC_SD

NVCC_CSI

50mA
USB_OTG1_VBUS
USB_OTG2_VBUS
LDO_USB
VDD_USB_CAP

LvDDR3
Micron: MT41K512M16

RGB LCD
TianMa TFT
VLCD_3V3
3.3V/23mA
5S2P
16V/25mA
BACKLIGHT
RICHTEK RT9293B
BLT_PWM

HDMI
SILICON IMAGE Sil9022A
VHDMI_3V3
3.3V/10mA
VLDO_1V2
1.2V/69.2mA
LDO
RICHTEK RT9169

Audio Codec
WM8960
VSPK_5V
5V/511mA
VAUD_3V3
3.3V/62.58mA

SENSOR
eCompass/
G-sensor/Gyroscope
VSENSOR_3V3
3.3V/6.9mA

CAN
FSL MC34901WEF
CAN_VIO_3V3
3.3V/1mA
CAN_VDD_5V
5V/65mA

Ethernet x2
Micrel KSZ8081RNB
VENET_3V3
3.3V/48.7mA
LOAD SW

Camera/EMV SIM
CSI B2B CN
DVDD1V5
AVDD_2V8
LDO
UNION UM1750S
1.5V/300mA

DCDC_3V3
3.3V/200mA
eMMC 4GB
Micron MTFC8GLCDM

NVCC_NAND
3.3V/1.8V

DCDC_3V3
3.3V/20mA
QSPI
Micron N25Q256

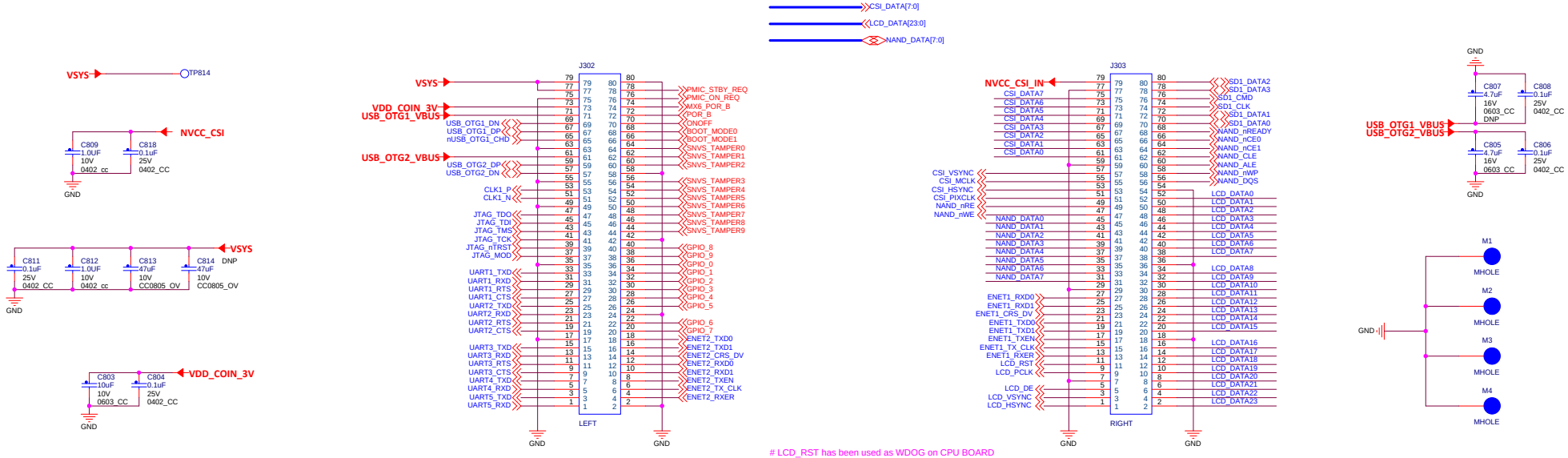
DCDC_3V3
3.3V/50mA
NAND
Micron MT29F32G08

MCIMX6UL-CM

USB_OTG_VBUS
USB OTG

USB_HOST_VBUS
USB HOST

SD1_nRST/POR_B
LOAD SW
SD Socket
BT MOD


VSYS
TP814
NVCC_CSI
C809
1.0UF
10V
0402_cc
C818
0.1uF
25V
0402_CC
GND
C811
0.1uF
25V
0402_CC
C812
1.0UF
10V
0402_cc
C813
47uF
10V
CC0805_OV
C814
47uF
10V
CC0805_OV
DNP
VSYS
GND
C803
10uF
10V
0603_CC
C804
0.1uF
25V
0402_CC
VDD_COIN_3V
GND
J302
VSYS
VDD_COIN_3V
USB_OTG1_VBUS
USB_OTG1_DN
USB_OTG1_DP
nUSB_OTG1_CHD
USB_OTG2_VBUS
USB_OTG2_DP
USB_OTG2_DN
CLK1_P
CLK1_N
JTAG_TDO
JTAG_TDI
JTAG_TMS
JTAG_TCK
JTAG_nTRST
JTAG_MOD
UART1_TXD
UART1_RXD
UART1_RTS
UART1_CTS
UART2_TXD
UART2_RXD
UART2_RTS
UART2_CTS
UART3_TXD
UART3_RXD
UART3_RTS
UART3_CTS
UART4_TXD
UART4_RXD
UART5_TXD
UART5_RXD
PMIC_STBY_REQ
PMIC_ON_REQ
MX6_POR_B
POR_B
ONOFF
BOOT_MODE0
BOOT_MODE1
SNVS_TAMPER0
SNVS_TAMPER1
SNVS_TAMPER2
SNVS_TAMPER3
SNVS_TAMPER4
SNVS_TAMPER5
SNVS_TAMPER6
SNVS_TAMPER7
SNVS_TAMPER8
SNVS_TAMPER9
GPIO_8
GPIO_9
GPIO_0
GPIO_1
GPIO_2
GPIO_3
GPIO_4
GPIO_5
GPIO_6
GPIO_7
ENET2_TXD0
ENET2_TXD1
ENET2_CRS_DV
ENET2_RXD0
ENET2_RXD1
ENET2_TXEN
ENET2_TX_CLK
ENET2_RXER
LEFT
GND
GND
CSI_DATA[7:0]
LCD_DATA[23:0]
NAND_DATA[7:0]
J303
NVCC_CSI_IN
CSI_DATA7
CSI_DATA6
CSI_DATA5
CSI_DATA4
CSI_DATA3
CSI_DATA2
CSI_DATA1
CSI_DATA0
CSI_VSYNC
CSI_MCLK
CSI_HSYNC
CSI_PIXCLK
NAND_nRE
NAND_nWE
NAND_DATA0
NAND_DATA1
NAND_DATA2
NAND_DATA3
NAND_DATA4
NAND_DATA5
NAND_DATA6
NAND_DATA7
ENET1_RXD0
ENET1_RXD1
ENET1_CRS_DV
ENET1_TXD0
ENET1_TXD1
ENET1_TXEN
ENET1_TX_CLK
ENET1_RXER
LCD_RST
LCD_PCLK
LCD_DE
LCD_VSYNC
LCD_HSYNC
SD1_DATA2
SD1_DATA3
SD1_CMD
SD1_CLK
SD1_DATA1
SD1_DATA0
NAND_nRREADY
NAND_nCE0
NAND_nCE1
NAND_CLE
NAND_ALE
NAND_nWP
NAND_DQS
LCD_DATA0
LCD_DATA1
LCD_DATA2
LCD_DATA3
LCD_DATA4
LCD_DATA5
LCD_DATA6
LCD_DATA7
LCD_DATA8
LCD_DATA9
LCD_DATA10
LCD_DATA11
LCD_DATA12
LCD_DATA13
LCD_DATA14
LCD_DATA15
LCD_DATA16
LCD_DATA17
LCD_DATA18
LCD_DATA19
LCD_DATA20
LCD_DATA21
LCD_DATA22
LCD_DATA23
RIGHT
GND
GND
LCD_RST has been used as WDOG on CPU BOARD
GND
C807
4.7uF
16V
0603_CC
DNP
C808
0.1uF
25V
0402_CC
USB_OTG1_VBUS
USB_OTG2_VBUS
C805
4.7uF
16V
0603_CC
C806
0.1uF
25V
0402_CC
GND
M1
MHOLE
M2
MHOLE
M3
MHOLE
M4
MHOLE
GND

i.MX6UL PWR

Power Rail	MIN	TYP	MAX	CURR
VDD_SNVS_IN	2.4	3	3.6	276uA
VDD_HIGH_IN	2.8	3	3.6	125mA
VDD_ARM_IN	0.9	1.275	1.5	400mA
VDD_SOC_IN	0.9	1.275	1.5	500mA
NVCC_DRAM	1.425	1.5	1.575	50mA
	1.283	1.35	1.45	
	1.14	1.2	1.3	
NVCC_xxx	1.65	1.8/2.5/3.3	3.6	
VDDA_ADC_3P3	3	3.3	3.6	
USB_OTG1_VBUS	4.4	5	5.25	50mA
USB_OTG2_VBUS				

DCDC_3V3 — R732 0 RC0603_OV — NVCC_3V3 → VDD_HIGH_IN, NVCC_LCDIF, NVCC_GPIO, NVCC_ENET, NVCC_UART

DCDC_3V3 / VLDO_1V8 — R701 0, R702 0 DNP → NVCC_NAND

1.8V for eMMC HS200 mode

DCDC_3V3 / VLDO_1V8 / NVCC_CSI_IN — R703 0 DNP, R704 0 DNP, R760 0, R759 0 DNP → NVCC_CSI

CSI default 2.8V from the base board

DCDC_3V3 / VLDO_3V3 — R705 0 DNP, R709 0 → VDDA_ADC_3P3

DCDC_3V3 — R731 0 DNP → NVCC_SD

Install the R731,Remove U707 if no requirement for SD3.0 of SD1

SNVS

LED1 — DCDC_3V3 — R765 100R — GND — LED0603_RED

LED2 — DCDC_3V3 — R766 100R — SNVS_TAMPER5 — LED0603_BLUE

VSYS — C701 10uF 10V 0603_CC, C708 0.1uF 25V 0402_CC — U701 RT9169-33GVL (VIN, VOUT, GND) — C709 4.7uF 6.3V 0402_CC, C710 0.1uF 25V 0402_CC — TP701 — VDD_SNVS_3V3

3.3V/100mA Iq = 4μA

ARM/SOC

2.5V to 6V — VSYS — C702 10uF 10V 0603_CC, C704 10uF 10V 0603_CC, C703 0.1uF 25V 0402_CC — U702 MP2159GJ (VIN, SW, OUT, FB, EN, PG, PGND, AGND) — L702 1uH — # 1.35V/1.05V/1.225V — TP702 — VDD_ARM_SOC_IN

Current 1A
I_Quiescent : 17μA

DCDC_3V3_PG — R710 10K — C707 0.1uF 25V 0402_CC

Vfb=0.6V / +-3%

Vo=Vfb*(R1+R2)/R2 = Vfb(1+R1/R2)

R1/R2 = (Vo-Vfb)/Vfb

1.4V: R1/R2 = 213K/160K
1.3V: R1/R2 = 186.7K/160K
0.925V: R1/R2 = 86.7K/160K

R706 215K, R707 147K, R708 1.5M, C705 22UF 6.3V 0603_CC, C706 0.1uF 25V 0402_CC, R737 51, R729 0 RC0805_OV

Q701 RYU002N05, Q702 2SK3018, Q707 2SK3018

DISCHG_EN — DNP C745 1000pF 50V 0402_CC

1.035M OHM 225K OHM PD (100K) — GPIO_DVFS, PMIC_STBY_REQ

R713 160K 1%, R714 100K DNP, R715 100K

PMIC_STBY_REQ = 0, GPIO_DVFS = 0, output is 1.4V (1.375V + 25mV)
PMIC_STBY_REQ = 0, GPIO_DVFS = 1, output is 1.3V (1.275V + 25mV) <Default>
PMIC_STBY_REQ = 1, GPIO_DVFS = 0, output is 0.925V (0.9V + 25mV)

Important: GPIO_DVFS / PMIC_STBY_REQ should be PULL DN when system reboot to ensure the VDD_ARM_SOC_IN voltage is not effected by DVFS

VDDHIGH / NVCC_xxx

由于不由核心板给底板供电，将MP2144，换为MP2159

2.5V-to-5.5V — VSYS — C711 10uF 10V 0603_CC, C712 10uF 10V 0603_CC, C713 0.1uF 25V 0402_CC, R716 100K DNP — U703 MP2159GJ (VIN, SW, OUT, FB, EN, PG, PGND, AGND) — L701 1uH — TP705 — R730 0 RC0805_OV — VDD_SNVS_3V3

Current 2A
I_Quiescent : 40μA
DCDC_3V3

PMIC_ON_REQ — R733 10K — C737 0.22UF 10V 0402_cc

R717 180K 1%, R718 40.2K 1%

R1/R2 = 9/2

PG pin is pulled up to VIN by the internal resistor 500K OHM

R758 0 DNP — D706 RB521S-30 — R726 0 — DCDC_3V3_PG — R727 0 DNP — C743 DNP 1000pF 50V 0402_CC, C744 DNP 1000pF 50V 0402_CC

R735 100K, DISCHG_EN, R740 10K, Q705 2SK3018, Q704 2SK3018, C736 0.1uF 25V 0402_CC, R734 51

Reset Button — MX6_POR_B — R757 100 — D702 RB521S-30 — C739 1000pF 0402_CC

U708 MAX811R (GND, VCC, RESET, MR) — C740 0.1uF 25V 0402_CC — VDD_SNVS_3V3

GPIO/WDOG PWR OFF->ON — nWDOG — C738 1.0UF 10V 0402_cc — D705 RB521S-30 — R755 1M

复位电压是2.63V，OD输出

DCDC_3V3 — # Stitching CAP for Layout — C741 0.1uF 25V 0402_CC, C742 0.1uF 25V 0402_CC

ADC High PSRR

VSYS — U704 RT9193 (VIN, VOUT, EN, GND, BP) — C716 10uF 10V 0603_CC, C717 0.1uF 25V 0402_CC, C720 0.022UF 16V 0402_CC, C718 4.7uF 6.3V 0402_CC, C719 0.1uF 25V 0402_CC — TP704 — VLDO_3V3

DCDC_3V3_PG — C747 DNP 1000pF 50V 0402_CC

1.8V PWR

RSV for eMMC HS200

DCDC_3V3 — D701 DNP RB521S-30 — U705 RT9169-18GVL (VIN, VOUT, GND) — C721 4.7uF 6.3V 0402_CC, C722 0.1uF 25V 0402_CC, C723 4.7uF 6.3V 0402_CC, C724 0.1uF 25V 0402_CC — TP707 — VLDO_1V8

1.8V/200mA Iq = 1.2μA

LvDDR3

2.5V to 6V — VSYS — C725 10uF 10V 0603_CC, C729 10uF 10V 0603_CC, C726 0.1uF 25V 0402_CC — U706 MP2159GJ (VIN, SW, OUT, FB, EN, PG, PGND, AGND) — L703 1uH — TP708 — R728 0 RC0805_OV — DRAM_1V35

Current 1A
I_Quiescent : 17μA

DCDC_3V3_PG — R722 10K — C735 0.1uF 25V 0402_CC

R719 200K 1%, R723 160K 1%

R1/R2 = 0.75/0.6

C727 22UF 6.3V 0603_CC, C728 0.1uF 25V 0402_CC, R736 51

DISCHG_EN — DNP C746 1000pF 50V 0402_CC — Q706 2SK3018

Update to MP2159

PG pin is pulled up to VIN by the internal resistor 550K OHM

NVCC_SD <SD3,0>

VSYS — U707 UM1750S-00 (IN, OUT, SHDN, FB, GND) — C730 10uF 10V 0603_CC, C731 0.1uF 25V 0402_CC — Vfb=1V — TP709 — NVCC_SD

1.8V/3.3V
Default: 3.3V

R720 464K, R721 243K, 330K, R724 200K 1%, 160K, R725 100K

Q703 2SK3018 — SD1_VSELECT

DCDC_3V3_PG

C732 4.7uF 6.3V 0402_CC, C733 0.1uF 25V 0402_CC

R1/R2 = (Vo-Vfb)/Vfb

FB = 0.8V — # 1.8V: R1/R2 = 1/0.8 : 200K/160K
3.3V: R1/R2 = 2.5/0.8 : 500K/160K
FB = 1.0V — # 1.8V: R1/R2 = 0.8/ 1: 160K/200K
3.3V: R1/R2 = 2.3/1 : 464K/200K

FUSE MAP

<Default: QSPI BOOT>

TYPE	BOOT_CFG1[7]	BOOT_CFG1[6]	BOOT_CFG1[5]	BOOT_CFG1[4]	BOOT_CFG1[3]	BOOT_CFG1[2]	BOOT_CFG1[1]	BOOT_CFG1[0]
	0/1	0/1	0/1	1	0	0	0	0
QSPI	0	0	0	1	Reserved	DDRSMP: "000" - Default "001-111"		
WEIM	0	0	0	0	Memory Type: 0 - NOR Flash 1 - OneNAND	Reserved	Reserved	Reserved
Serial-ROM	0	0	1	1	Reserved	Reserved	Reserved	Reserved
SD/eSD	0	1	0	Fast Boot: 0 - Regular 1 - Fast Boot	SD/SDXC Speed 00 - Normal/SDR12 01 - High/SDR25 10 - SDR50 11 - SDR104		SD Power Cycle Enable '0' - No power cycle '1' - Enabled via USDHC_RST pad (uSDHC3 & 4 only)	SD Loopback Clock Source Sel (for SDR50 and SDR104 only) '0' - through SD pad '1' - direct
MMC/eMMC	0	1	1	Fast Boot: 0 - Regular 1 - Fast Boot	SD/MMC Speed 0 - High! 1 - Normal	Fast Boot Acknowledge Disable: 0 - Boot Ack Enabled 1 - Boot Ack Disabled	SD Power Cycle Enable '0' - No power cycle '1' - Enabled via USDHC_RST pad (uSDHC3 & 4 only)	SD Loopback Clock Source Sel (for SDR50 and SDR104 only) '0' - through SD pad '1' - direct
NAND	1	BT_TOGGLEMODE	Pages In Block: 00 - 128 01 - 64 10 - 32 11 - 256		Nand Number Of Devices: 00 - 1 01 - 2 10 - 4 11 - Reserved		Nand_Row_address_bytes: 0 - 3 1 - 2 10 - 4 11 - 5	

TYPE	BOOT_CFG2[7]	BOOT_CFG2[6]	BOOT_CFG2[5]	BOOT_CFG2[4]	BOOT_CFG2[3]	BOOT_CFG2[2]	BOOT_CFG2[1]	BOOT_CFG2[0]
	0	0	0	0	1	0	0	0
QSPI	Reserved	HSPHS: Half Speed Phase Selection '0' - select sampling at non-inverted clock '1' - select sampling at inverted clock	HSDLY: Half Speed Delay selection '0' - one clock delay '1' - Two clock delay	FSPHS: Full Speed Phase Selection '0' - select sampling at non-inverted clock '1' - select sampling at inverted clock	FSDLY: Full Speed Delay selection '0' - one clock delay '1' - two clock delay	Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reserved	Reserved
WEIM	Muxing Scheme: 00 - A/D16(W Default in external boot) 01 - A+DH 10 - A+DL 11- Reserved		OneNand Page Size: 00 - 1KB 01 - 2KB 10 - 4KB 11 - Reserved		Reserved	Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reserved	Reserved
Serial-ROM	Reserved	Reserved	Reserved	Reserved	Reserved	Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reserved	Reserved
SD/eSD	SD Calibration Step '000' - 1 TBD		Bus Width: 0 - 1-bit 1 - 4-bit		Port Select: 00 - eSDHC1 01 - eSDHC2 10 - Reserved 11- Reserved	Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	SDIO VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	Reserved
MMC/eMMC	Bus Width: 000 - 1-bit 001 - 4-bit 010 - 8-bit 101 - 4-bit DDR (MMC 4.4) 110 - 8-bit DDR (MMC 4.4) Else - reserved				Port Select: 00 - eSDHC1 01 - eSDHC2 10 - Reserved 11- Reserved	Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	SDIO VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	Reserved
NAND	Toggle Mode 120MHz Extended Delay, Read Latency: '000' - 16 GPMICLK cycles '001' - 5 GPMICLK cycles '010' - 7 GPMICLK cycles '011' - 9 GPMICLK cycles '100' - 4 GPMICLK cycles '101' - 6 GPMICLK cycles '110' - 8 GPMICLK cycles '111' - 7 GPMICLK cycles				BOOT_SEARCH_COUNT: 00- 2 01- 3 10- 4 11- 8	Boot Frequencies (ARM/DDR) 0 - 500 / 400 MHz 1 - 250 / 200 MHz	Reset Time '0' - 12ms '1' - 32ms (LBA Nand)	Reserved

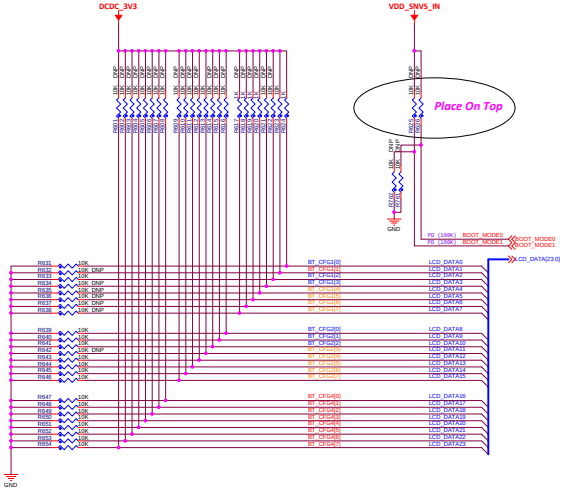
TYPE	BOOT_CFG4[7]	BOOT_CFG4[6]	BOOT_CFG4[5]	BOOT_CFG4[4]	BOOT_CFG4[3]	BOOT_CFG4[2]	BOOT_CFG4[1]	BOOT_CFG4[0]
QSPI	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
WEIM	Reserved	EEPROM Recovery Enable '0' - Disabled '1' - Enabled Fuse is Reserved for 'Serial-ROM' Boot mode	eCSPI chip select: 00 - ECSPIx_SS0 (default) 01 - ECSPIx_SS1 10 - ECSPIx_SS2 11 - ECSPIx_SS3		eCSPI Addressing: 0 - 2-bytes(16-bit) 1 - 3-bytes(24-bit)	Port Select: 000 - eCSPI1 001 - eCSPI2 010 - eCSPI3 011 - eCSPI4 100 - Reserved 101 - Reserved 110 - Reserved 111 - Reserved		
Serial-ROM	Reserved	EEPROM Recovery Enable '0' - Disabled '1' - Enabled Fuse is Reserved for 'Serial-ROM' Boot mode	eCSPI chip select: 00 - ECSPIx_SS0 (default) 01 - ECSPIx_SS1 10 - ECSPIx_SS2 11 - ECSPIx_SS3		eCSPI Addressing: 0 - 2-bytes(16-bit) 1 - 3-bytes(24-bit)	Port Select: 000 - eCSPI1 001 - eCSPI2 010 - eCSPI3 011 - eCSPI4 100 - Reserved 101 - Reserved 110 - Reserved 111 - Reserved		
SD/eSD	Reserved	EEPROM Recovery Enable '0' - Disabled '1' - Enabled Fuse is Reserved for 'Serial-ROM' Boot mode	eCSPI chip select: 00 - ECSPIx_SS0 (default) 01 - ECSPIx_SS1 10 - ECSPIx_SS2 11 - ECSPIx_SS3		eCSPI Addressing: 0 - 2-bytes(16-bit) 1 - 3-bytes(24-bit)	Port Select: 000 - eCSPI1 001 - eCSPI2 010 - eCSPI3 011 - eCSPI4 100 - Reserved 101 - Reserved 110 - Reserved 111 - Reserved		
MMC/eMMC	Reserved	EEPROM Recovery Enable '0' - Disabled '1' - Enabled Fuse is Reserved for 'Serial-ROM' Boot mode	eCSPI chip select: 00 - ECSPIx_SS0 (default) 01 - ECSPIx_SS1 10 - ECSPIx_SS2 11 - ECSPIx_SS3		eCSPI Addressing: 0 - 2-bytes(16-bit) 1 - 3-bytes(24-bit)	Port Select: 000 - eCSPI1 001 - eCSPI2 010 - eCSPI3 011 - eCSPI4 100 - Reserved 101 - Reserved 110 - Reserved 111 - Reserved		
NAND	Reserved	EEPROM Recovery Enable '0' - Disabled '1' - Enabled Fuse is Reserved for 'Serial-ROM' Boot mode	eCSPI chip select: 00 - ECSPIx_SS0 (default) 01 - ECSPIx_SS1 10 - ECSPIx_SS2 11 - ECSPIx_SS3		eCSPI Addressing: 0 - 2-bytes(16-bit) 1 - 3-bytes(24-bit)	Port Select: 000 - eCSPI1 001 - eCSPI2 010 - eCSPI3 011 - eCSPI4 100 - Reserved 101 - Reserved 110 - Reserved 111 - Reserved		

NAND MT29F32G08CBACA

1 page = (4K + 224 bytes)
1 block = (4K + 224) bytes x 256 pages
= 1,081,344 (1024) bytes
1 plane = (1024K + 56K) bytes x 2048 blocks
= 17.180Mb
1 LUN = 17.180Mb x 2 planes
= 34.360Mb

Boot Configuration

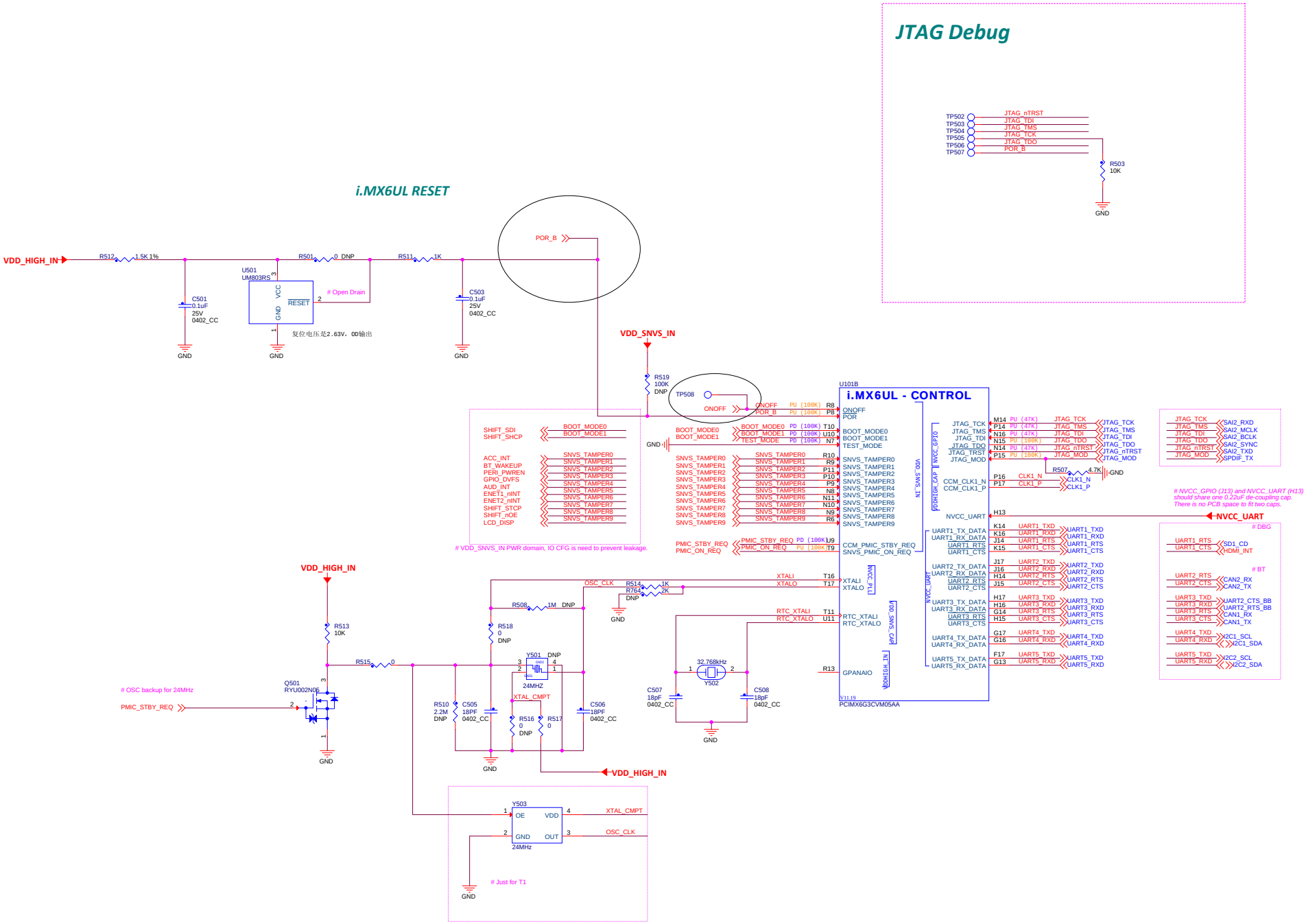
BMODE[1:0]	BOOT TYPE
00	Boot From Fuses
01	Serial Downloader
10	Internal Boot (Development)
11	Reserved



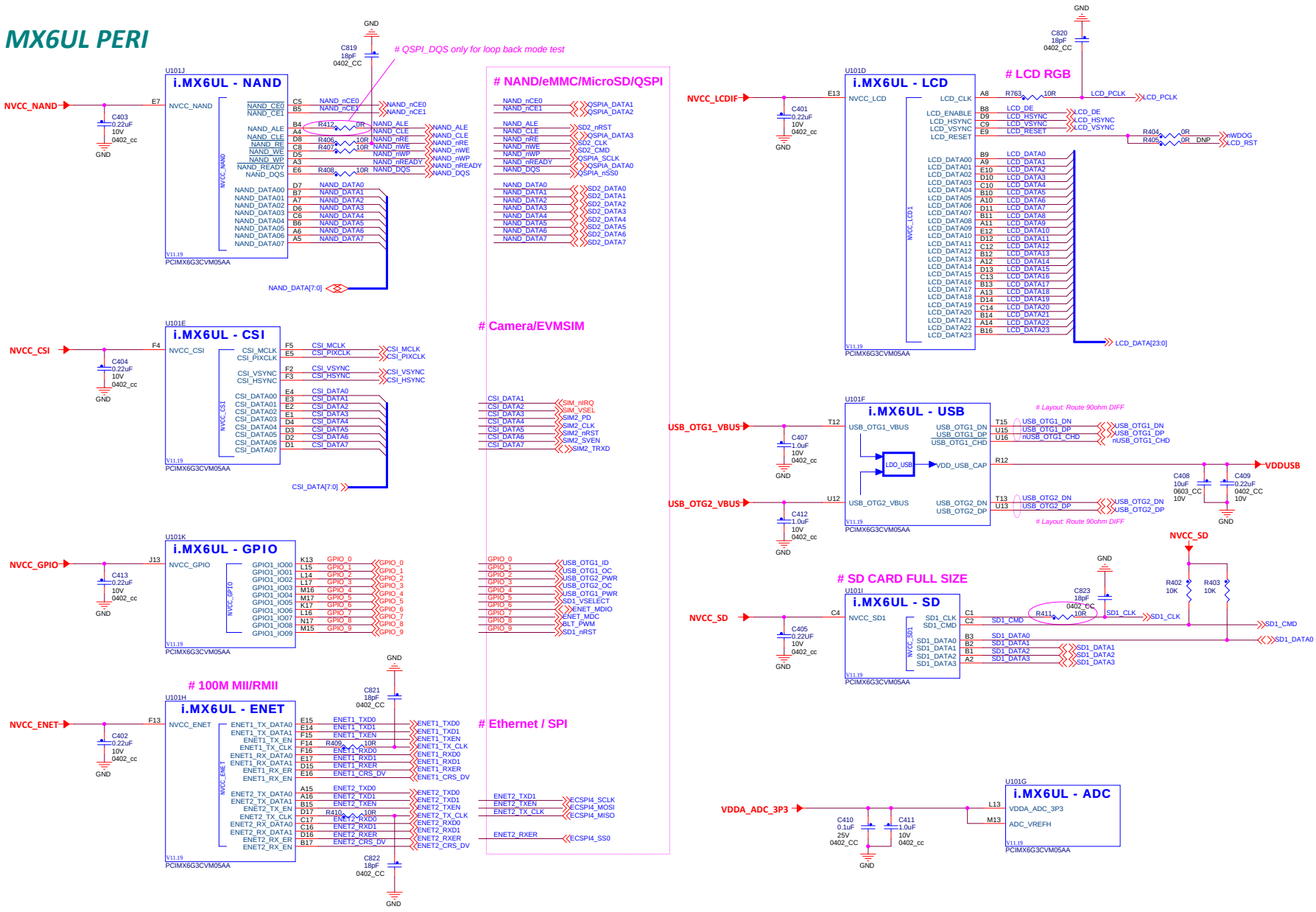
FOR WEIM BOOT	FOR Serial-ROM BOOT	FOR SD/eSD BOOT						
0x460[7:0]	Reserved	Reserved	FORCE_COLD_BOOT (Reflected in SBMR2)	BT_FUSE_SEL	DIR_BT_DIS	Reserved	SEC_CONFIG[1]	Reserved
0x460[15:8]	Reserved (DDR3 config options)							
0x460[23:16]	JTAG_SMODE[1:0]		WDOG_ENABLE '0' - Disabled '1' - Enabled	SJC_DISABLE	Reserved	Reserved	Reserved	Reserved
0x460[31:24]	Reserved	Reserved	Reserved	TZASC_ENABLE	JTAG_HEO	KTE	Reserved	DLL_ENABLE 0 - Disable DLL for SDrMMC 1 - Enable DLL for SDrMMC
0x470[7:0]	Dis Override 0 - Dis Slave Mode for SD/MMC 1 - Dis Override Mode for SD/MMC	SD1_KST_POLARITY_SELECT 0 - Reset active low 1 - Reset active high	SD2 Voltage Selection: 0 - 3.3V 1 - 1.8V	Reserved	Disable SDMMC Manufacture Mode 0 - Enable 1 - Disable	L1 I-Cache DISABLE	BT_MMU _DISABLE	Override SD PAD Settings (using PAD_SETTINGS value)
0x470[15:8]	SD2_RST_POLARITY_SELECT 0 - Reset active low 1 - Reset active high	eMMC 4.4 RESET TO PAD 0114 STATE	Override HYS bit for SD/MMC pads	USDHC_PAD_PULL_DOWN 0 - no action 1 - pull down	ENABLE_EMMC_22K_PULLUP 0 - 47K pullup 1 - 22K pullup	ADD_DS_SET_GPR1_16 0 - Set 1 - Do not set	USDHC_IOMUX_SION_BIT_ ENABLE 0 - Disable 1 - Enable	USDHC_IOMUX_SRE Enable 0 - Disable 1 - Enable
0x470[23:16]	Reserved	LPB_BOOT (Core / DDR- Bus) '00' - LPB Disable '01' - 1 GPIO (def freq) '10' - Div by2 '11' - Div by 4		BT_LPB_POLARITY (GPIO polarity) 0: Active High 1: Active Low	Reserved			
0x470[31:24]	Override Nand Pad settings (Use PAD_SETTINGS Value)	MMC_DLL_DLY[6:0]						
0x6D0[7:0]	RANDOMIZER_ENABLE	Reserved	PAD_SETTINGS[5:0]					

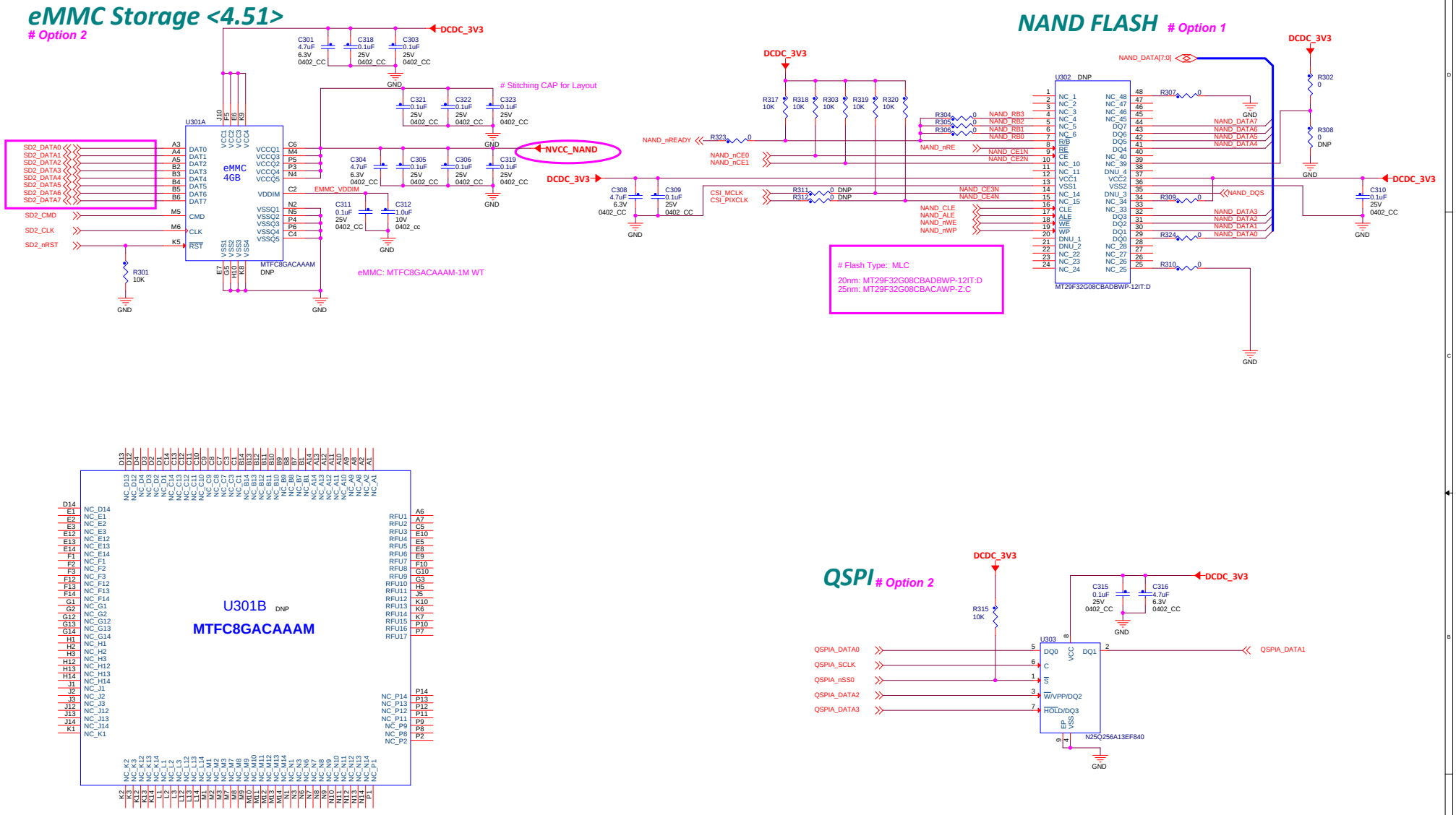
FOR NAND BOOT							
0x460[7:0]	Reserved	Reserved	FORCE_COLD_BOOT (Reflected in SBMR2)	BT_FUSE_SEL	DIR_BT_DIS	Reserved	SEC_CONFIG[1]	Reserved
0x460[15:8]	Reserved (DDR3 config options)							
0x460[23:16]	JTAG_SMODE[1:0]		WDOG_ENABLE '0' - Disabled '1' - Enabled	SJC_DISABLE	Reserved	Reserved	Reserved	Reserved
0x460[31:24]	Reserved	Reserved	Reserved	TZASC_ENABLE	JTAG_HEO	KTE	Reserved	DLL_ENABLE 0 - Disable DLL for SDrMMC 1 - Enable DLL for SDrMMC
0x470[7:0]	Dis Override 0 - Dis Slave Mode for SD/MMC 1 - Dis Override Mode for SD/MMC	SD1_KST_POLARITY_SELECT 0 - Reset active low 1 - Reset active high	SD2 Voltage Selection: 0 - 3.3V 1 - 1.8V	Reserved	Disable SDMMC Manufacture Mode 0 - Enable 1 - Disable	L1 I-Cache DISABLE	BT_MMU _DISABLE	Override SD PAD Settings (using PAD_SETTINGS value)
0x470[15:8]	SD2_RST_POLARITY_SELECT 0 - Reset active low 1 - Reset active high	eMMC 4.4 RESET TO PAD 0114 STATE	Override HYS bit for SD/MMC pads	USDHC_PAD_PULL_DOWN 0 - no action 1 - pull down	ENABLE_EMMC_22K_PULLUP 0 - 47K pullup 1 - 22K pullup	ADD_DS_SET_GPR1_16 0 - Set 1 - Do not set	USDHC_IOMUX_SION_BIT_ ENABLE 0 - Disable 1 - Enable	USDHC_IOMUX_SRE Enable 0 - Disable 1 - Enable
0x470[23:16]	Reserved	LPB_BOOT (Core / DDR- Bus) '00' - LPB Disable '01' - 1 GPIO (def freq) '10' - Div by2 '11' - Div by 4		BT_LPB_POLARITY (GPIO polarity) 0: Active High 1: Active Low	Reserved			
0x470[31:24]	Override Nand Pad settings (Use PAD_SETTINGS Value)	MMC_DLL_DLY[6:0]						
0x6D0[7:0]	RANDOMIZER_ENABLE	Reserved	PAD_SETTINGS[5:0]					
0x6D0[23:16]	NAND_READ_CMD_CODE1[7:0]							
0x6D0[31:24]	NAND_READ_CMD_CODE2[7:0]							

FOR QSPI BOOT							
0x460[7:0]	L2_HW_INVALIDATE _DISABLE	Reserved	FORCE_COLD_BOOT (Reflected in SBMR2)	BT_FUSE_SEL	DIR_BT_DIS	Reserved	SEC_CONFIG[1]	Reserved
0x460[15:8]	Reserved (DDR3 config options)							
0x460[23:16]	JTAG_SMODE[1:0]		WDOG_ENABLE '0' - Disabled '1' - Enabled	SJC_DISABLE	Reserved	Reserved	Reserved	Reserved
0x460[31:24]	Reserved	Reserved	Reserved	TZASC_ENABLE	JTAG_HEO	KTE	Reserved	DLL_ENABLE 0 - Disable DLL for SDrMMC 1 - Enable DLL for SDrMMC
0x470[7:0]	Not Used	Not Used	Not Used	Not Used	Reserved	L1 I-Cache DISABLE	BT_MMU _DISABLE	Reserved
0x470[15:8]	Reserved	Not Used	Reserved	ADD_DS_SET_GPR1_16 0 - Set 1 - Don't set	Reserved	Reserved	Not Used	Not Used
0x470[23:16]	Reserved	LPB_BOOT (Core / DDR- Bus) '00' - LPB Disable '01' - 1 GPIO (def freq) '10' - Div by2 '11' - Div by 4		BT_LPB_POLARITY (GPIO polarity) 0: Active High 1: Active Low	Reserved			
0x470[31:24]	Reserved	Reserved						

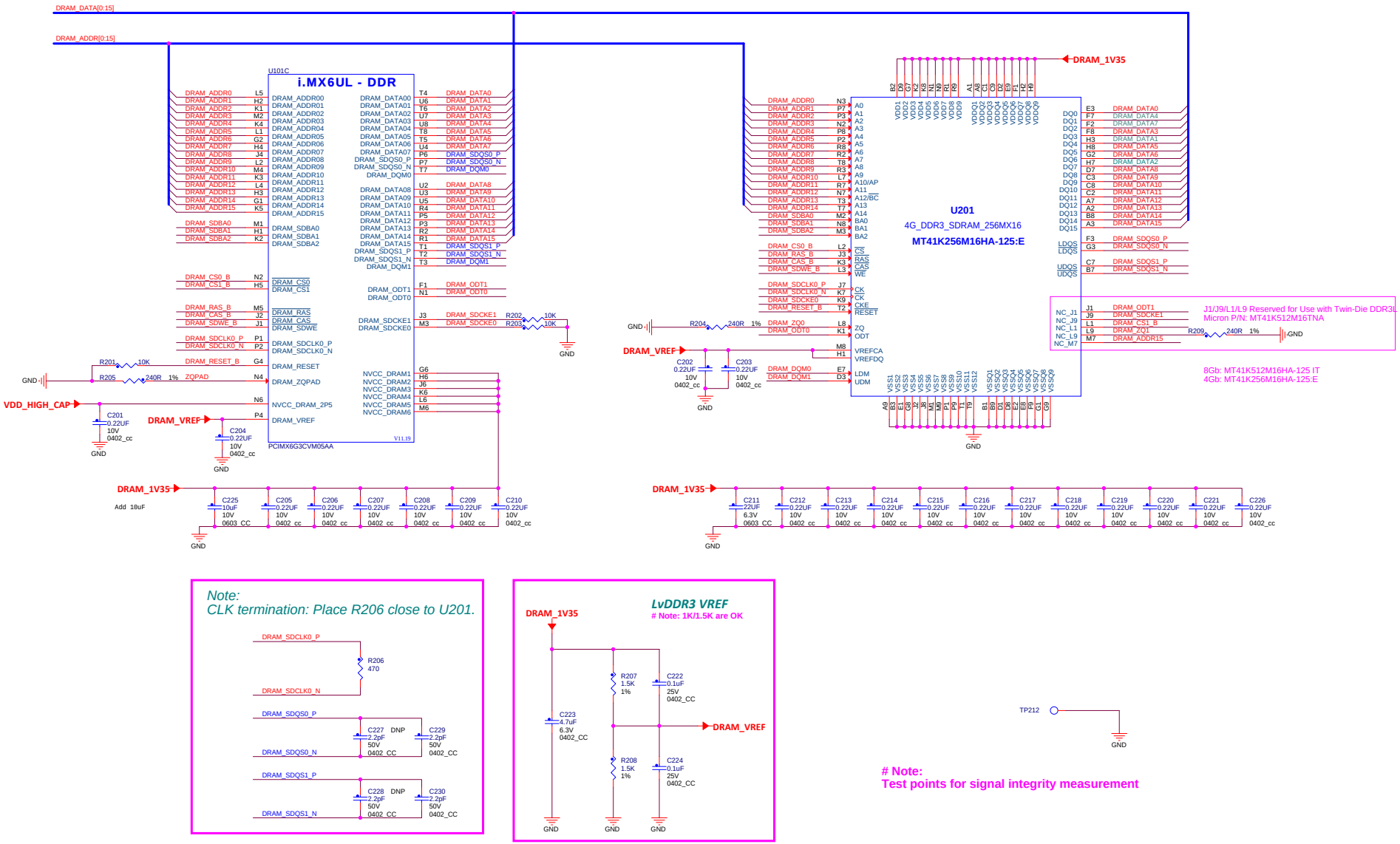

JTAG Debug
TP502
TP503
TP504
TP505
TP506
TP507
JTAG_nTRST
JTAG_TDI
JTAG_TMS
JTAG_TCK
JTAG_TDO
POR_B
R503
10K
GND
i.MX6UL RESET
VDD_HIGH_IN
R512
1.5K 1%
R501
0 DNP
R511
1K
POR_B
U501
UM803RS
VCC
GND
RESET
Open Drain
C501
0.1uF
25V
0402_CC
C503
0.1uF
25V
0402_CC
复位电压是2.63V，OD输出
VDD_SNVS_IN
R519
100K
DNP
TP508
ONOFF
U101B
i.MX6UL - CONTROL
BOOT_MODE0
BOOT_MODE1
TEST_MODE
SNVS_TAMPER0
SNVS_TAMPER1
SNVS_TAMPER2
SNVS_TAMPER3
SNVS_TAMPER4
SNVS_TAMPER5
SNVS_TAMPER6
SNVS_TAMPER7
SNVS_TAMPER8
SNVS_TAMPER9
SHIFT_SDI
SHIFT_SHCP
ACC_INT
BT_WAKEUP
PERI_PWREN
GPIO_DVFS
AUD_INT
ENET1_nINT
ENET2_nINT
SHIFT_STCP
SHIFT_nOE
LCD_DISP
VDD_SNVS_IN PWR domain, IO CFG is need to prevent leakage.
PMIC_STBY_REQ
PMIC_ON_REQ
CCM_PMIC_STBY_REQ
SNVS_PMIC_ON_REQ
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG_TRST
JTAG_MOD
CCM_CLK1_N
CCM_CLK1_P
R507
4.7K
NVCC_UART
UART1_TX_DATA
UART1_RX_DATA
UART1_RTS
UART1_CTS
UART2_TX_DATA
UART2_RX_DATA
UART2_RTS
UART2_CTS
UART3_TX_DATA
UART3_RX_DATA
UART3_RTS
UART3_CTS
UART4_TX_DATA
UART4_RX_DATA
UART5_TX_DATA
UART5_RX_DATA
NVCC_GPIO (J13) and NVCC_UART (H13) should share one 0.22uF de-coupling cap. There is no PCB space to fit two caps.
DBG
BT
SAI2_RXD
SAI2_MCLK
SAI2_BCLK
SAI2_SYNC
SAI2_TXD
SPDIF_TX
SD1_CD
HDMI_INT
CAN2_RX
CAN2_TX
UART2_RTS_BB
UART2_CTS_BB
CAN1_RX
CAN1_TX
I2C1_SCL
I2C1_SDA
I2C2_SCL
I2C2_SDA
VDD_HIGH_IN
R513
10K
R515
0
OSC_CLK
R514
1K
R764
2K
DNP
R508
1M DNP
R518
0
DNP
Y501 DNP
24MHZ
XTAL_CMPT
R510
2.2M
DNP
C505
18PF
0402_CC
R516
0
DNP
R517
0
C506
18PF
0402_CC
Q501
RYU002N06
OSC backup for 24MHz
PMIC_STBY_REQ
XTALI
XTALO
RTC_XTALI
RTC_XTALO
GPANAIO
32.768kHz
Y502
C507
18pF
0402_CC
C508
18pF
0402_CC
PCIMX6G3CVM05AA
Y503
OE
VDD
GND
OUT
24MHz
XTAL_CMPT
OSC_CLK
Just for T1

MX6UL PERI

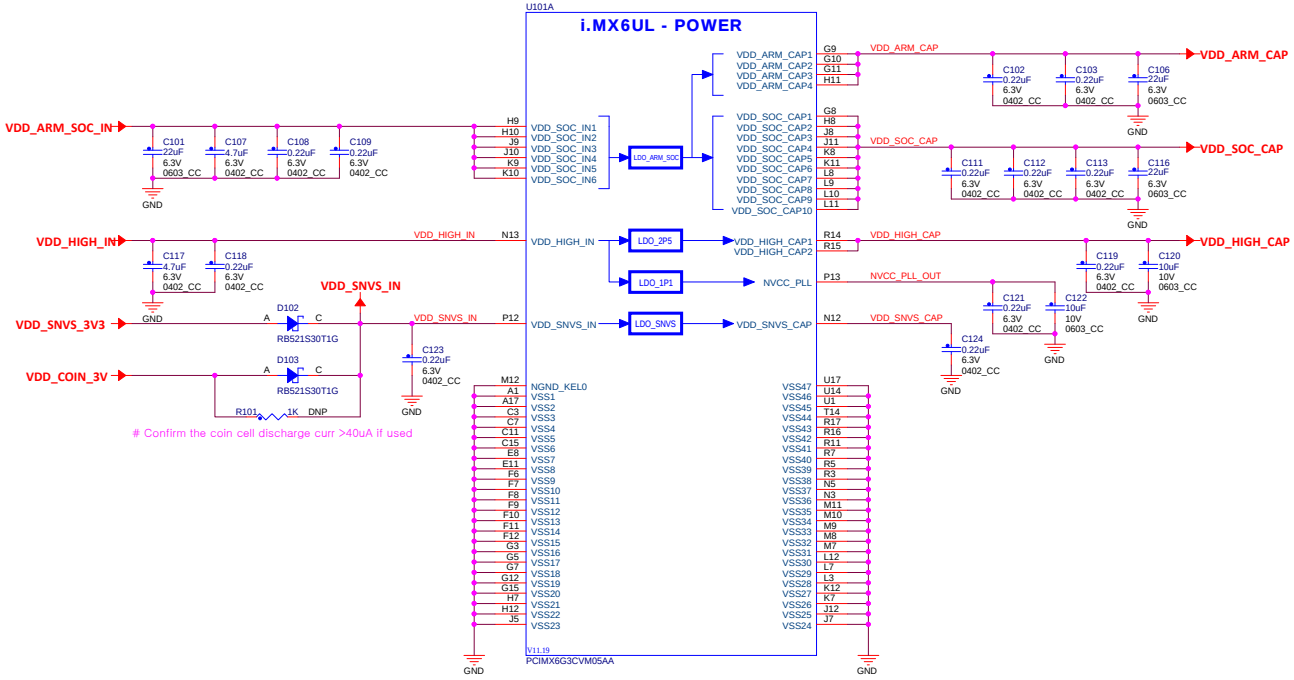

U101J
i.MX6UL - NAND
NVCC_NAND
C403 0.22uF 10V 0402_cc
C819 18pF 0402_CC
QSPI_DQS only for loop back mode test
NAND/eMMC/MicroSD/QSPI
U101E
i.MX6UL - CSI
NVCC_CSI
C404 0.22uF 10V 0402_cc
Camera/EVMSIM
U101K
i.MX6UL - GPIO
NVCC_GPIO
C413 0.22uF 10V 0402_cc
U101H
i.MX6UL - ENET
NVCC_ENET
C402 0.22uF 10V 0402_cc
100M MII/RMII
C821 18pF 0402_CC
C822 18pF 0402_CC
Ethernet / SPI
U101D
i.MX6UL - LCD
NVCC_LCDIF
C401 0.22uF 10V 0402_cc
LCD RGB
C820 18pF 0402_CC
U101F
i.MX6UL - USB
USB_OTG1_VBUS
USB_OTG2_VBUS
C407 1.0uF 10V 0402_cc
C412 1.0uF 10V 0402_cc
Layout: Route 90ohm DIFF
LDO_USB
VDD_USB_CAP
VDDUSB
C408 10uF 0603_CC 10V
C409 0.22uF 0402_CC 10V
U101I
i.MX6UL - SD
NVCC_SD
C405 0.22uF 10V 0402_cc
SD CARD FULL SIZE
C823 18pF 0402_CC
R402 10K
R403 10K
U101G
i.MX6UL - ADC
VDDA_ADC_3P3
C410 0.1uF 25V 0402_CC
C411 1.0uF 10V 0402_cc
ADC_VREFH
PCIMX6G3CVM05AA
GND


eMMC Storage <4.51>
Option 2
U301A
eMMC
4GB
MTFC8GACAAAM
DNP
eMMC: MTFC8GACAAAM-1M WT
Stitching CAP for Layout
DCDC_3V3
NVCC_NAND
EMMC_VDDIM
SD2_DATA0
SD2_DATA1
SD2_DATA2
SD2_DATA3
SD2_DATA4
SD2_DATA5
SD2_DATA6
SD2_DATA7
SD2_CMD
SD2_CLK
SD2_nRST
NAND FLASH
Option 1
U302 DNP
MT29F32G08CBADBWP-12IT:D
Flash Type: MLC
20nm: MT29F32G08CBADBWP-12IT:D
25nm: MT29F32G08CBACAWP-Z:C
NAND_DATA[7:0]
NAND_nREADY
NAND_nCE0
NAND_nCE1
NAND_nRE
NAND_CLE
NAND_ALE
NAND_nWE
NAND_nWP
NAND_DQS
CSI_MCLK
CSI_PIXCLK
U301B DNP
MTFC8GACAAAM
QSPI
Option 2
U303
N25Q256A13EF840
QSPIA_DATA0
QSPIA_SCLK
QSPIA_nSS0
QSPIA_DATA2
QSPIA_DATA3
QSPIA_DATA1

DDR3/LvDDR3


DRAM_DATA[0:15]
DRAM_ADDR[0:15]
U101C
i.MX6UL - DDR
PCIMX6G3CVM05AA
V11.19
U201
4G_DDR3_SDRAM_256MX16
MT41K256M16HA-125:E
DRAM_1V35
VDD_HIGH_CAP
DRAM_VREF
GND
J1/J9/L1/L9 Reserved for Use with Twin-Die DDR3L
Micron P/N: MT41K512M16TNA
8Gb: MT41K512M16HA-125 IT
4Gb: MT41K256M16HA-125:E
Note:
CLK termination: Place R206 close to U201.
LvDDR3 VREF
Note: 1K/1.5K are OK
TP212
Note:
Test points for signal integrity measurement

i.MX6UL PWR


U101A
i.MX6UL - POWER
VDD_ARM_SOC_IN
VDD_HIGH_IN
VDD_SNVS_3V3
VDD_COIN_3V
VDD_SNVS_IN
LDO_ARM_SOC
LDO_2P5
LDO_1P1
LDO_SNVS
VDD_ARM_CAP
VDD_SOC_CAP
VDD_HIGH_CAP
NVCC_PLL
VDD_SNVS_CAP
NVCC_PLL_OUT
D102
D103
RB521S30T1G
R101
1K
DNP
Confirm the coin cell discharge curr >40uA if used
GND
V11.19
PCIMX6G3CVM05AA

NOTE:

All pins using ~reset as harden :

PAD	Default State	Simulation Value
UART3_TX_DATA	Output Buffer(LOW) during reset --> Output keeper + Input enable after reset done	0 in real silicon
LCD_DATA00~LCD_DATA23	100K pull down + input enable during reset --> Output keeper + Input enable after reset done (this is boot option, we don't need change)	0 in real silicon

PAD	Default State	Signal Path	PAD Simulation Value
UART3_TX_DATA	Output Buffer(LOW) during reset --> Output keeper + Input enable after reset done	sjc.ipt_jta_active --> PAD	0 in real silicon
		(note : sjc.ipt_jta_active also connected to snvs_hp.sec_vio_in_1. This is security related, we don't plan to change it.)	ALT7

All pins using ~src.en_system_clk as harden :

PAD	Default State	Simulation Value
GPIO1_IO03	100K pull down + input enable during reset --> Output keeper + Input enable after reset done	0 in real silicon

PAD	Default State	Signal Path	PAD Simulation Value
GPIO1_IO03	100K pull down + input enable during reset --> Output keeper + Input enable after reset done	PAD --> ccmsrcmix. src_tester_ack	0 in real silicon
		This is the requirement of TE test	ALT7

All pins using snvs_hp.snvs_sec_vio_in_5_en as harden :

PAD	Default State	Simulation Value
CSI_PIXCLK	Output keeper + Input enable (snvs_sec_vio_in_5_en is 1'b0 in normal state, so harden is not triggerd in normal state). snvs_sec_vio_in_5_en is controlled by SNVS register. It can be disable or enable.	X (0 or 1 in real silicon)

i.MX6UL IOMUX

NAME	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	PAD DFU
TEST_MODE	tcu.TEST_MODE	tcu.TEST_MODE									100K PD
POR_B	src.POR_B	src.POR_B									100K PU
ONOFF	src.RESET_B	src.RESET_B									100K PU
SNVS_PMIC_ON_REQ	snvs_lp_wrapper.SNVS_WAKEUP_ALARM	snvs_lp_wrapper.PMIC_ON_REQ									100K PU
CCM_PMIC_STBY_REQ	ccm.PMIC_VSTBY_REQ	ccm.PMIC_VSTBY_REQ									100K PD
BOOT_MODE0	src.BOOT_MODE[0]	src.BOOT_MODE[0]					gpio5.IO[10]				100K PD
BOOT_MODE1	src.BOOT_MODE[1]	src.BOOT_MODE[1]					gpio5.IO[11]				100K PD
SNVS_TAMPER0	snvs_lp_wrapper.SNVS_TD1	snvs_lp_wrapper.TAMPER[0]					gpio5.IO[0]				Keeper
SNVS_TAMPER1	snvs_lp_wrapper.SNVS_TD1	snvs_lp_wrapper.TAMPER[1]					gpio5.IO[1]				Keeper
SNVS_TAMPER2	snvs_lp_wrapper.SNVS_TD1	snvs_lp_wrapper.TAMPER[2]					gpio5.IO[2]				Keeper
SNVS_TAMPER3	snvs_lp_wrapper.SNVS_TD1	snvs_lp_wrapper.TAMPER[3]					gpio5.IO[3]				Keeper
SNVS_TAMPER4	snvs_lp_wrapper.SNVS_TD1	snvs_lp_wrapper.TAMPER[4]					gpio5.IO[4]				Keeper
SNVS_TAMPER5	snvs_lp_wrapper.SNVS_TD1	snvs_lp_wrapper.TAMPER[5]					gpio5.IO[5]				Keeper
SNVS_TAMPER6	snvs_lp_wrapper.SNVS_TD1	snvs_lp_wrapper.TAMPER[6]					gpio5.IO[6]				Keeper
SNVS_TAMPER7	snvs_lp_wrapper.SNVS_TD1	snvs_lp_wrapper.TAMPER[7]					gpio5.IO[7]				Keeper
SNVS_TAMPER8	snvs_lp_wrapper.SNVS_TD1	snvs_lp_wrapper.TAMPER[8]					gpio5.IO[8]				Keeper
SNVS_TAMPER9	snvs_lp_wrapper.SNVS_TD1	snvs_lp_wrapper.TAMPER[9]					gpio5.IO[9]				Keeper
JTAG_MOD	sjc.MOD	sjc.MOD	gpt2.CLK	spdif.OUT	anatop.ENET_REF_CLK_25M	ccm.PMIC_RDY	gpio1.IO[10]	sdma.EXT_EVENT[0]			100K PU
JTAG_TMS	sjc.TMS	sjc.TMS	gpt2.CAPTURE1	sai2.MCLK	ccm.CLKO1	ccm.WAIT	gpio1.IO[11]	sdma.EXT_EVENT[1]		epit1.OUT	47K PU
JTAG_TDO	sjc.TDO	sjc.TDO	gpt2.CAPTURE2	sai2.TX_SYNC	ccm.CLKO2	ccm.STOP	gpio1.IO[12]	mqs.RIGHT		epit2.OUT	100K PU
JTAG_TDI	sjc.TDI	sjc.TDI	gpt2.COMPARE1	sai2.TX_BCLK	ccm.OUT0	pwm6.OUT	gpio1.IO[13]	mqs.LEFT		sim1.POWER_FAIL	47K PU
JTAG_TCK	sjc.TCK	sjc.TCK	gpt2.COMPARE2	sai2.RX_DATA	ccm.OUT1	pwm7.OUT	gpio1.IO[14]	osc32k.32K_OUT		sim2.POWER_FAIL	47K PU
JTAG_TRST_B	sjc.TRSTB	sjc.TRSTB	gpt2.COMPARE3	sai2.TX_DATA	ccm.OUT2	pwm8.OUT	gpio1.IO[15]	anatop.24M_OUT		caam_wrapper.RNG_OSC_OBS	47K PU
GPIO1_IO00	gpio1.IO[0]	i2c2.SCL	gpt1.CAPTURE1	anatop.OTG1_ID	anatop.ENET_REF_CLK1	mqs.RIGHT	gpio1.IO[0]	enet1.1588_EVENT0_IN	src.SYSTEM_RESET	wdog3.WDOG_B	Keeper
GPIO1_IO01	gpio1.IO[1]	i2c2.SDA	gpt1.COMPARE1	usb.OTG1_OC	anatop.ENET_REF_CLK2	mqs.LEFT	gpio1.IO[1]	enet1.1588_EVENT0_OUT	src.EARLY_RESET	wdog1.WDOG_B	Keeper
GPIO1_IO02	gpio1.IO[2]	i2c1.SCL	gpt1.COMPARE2	usb.OTG2_PWR	anatop.ENET_REF_CLK_25M	usdhc1.WP	gpio1.IO[2]	sdma.EXT_EVENT[0]	src.ANY_PU_RESET	uart1.TX	Keeper
GPIO1_IO03	gpio1.IO[3]	i2c1.SDA	gpt1.COMPARE3	usb.OTG2_OC	osc32k.32K_OUT	usdhc1.CD_B	gpio1.IO[3]	ccm.DI0_EXT_CLK	src.TESTER_ACK	uart1.RX	Keeper
GPIO1_IO04	gpio1.IO[4]	anatop.ENET_REF_CLK1	pwm3.OUT	usb.OTG1_PWR	anatop.24M_OUT	usdhc1.RESET_B	gpio1.IO[4]	enet2.1588_EVENT0_IN	ccm.PLL2_BYP	uart5.TX	Keeper
GPIO1_IO05	gpio1.IO[5]	anatop.ENET_REF_CLK2	pwm4.OUT	anatop.OTG2_ID	csi.FIELD	usdhc1.VSELECT	gpio1.IO[5]	enet2.1588_EVENT0_OUT	ccm.PLL3_BYP	uart5.RX	Keeper
GPIO1_IO06	gpio1.IO[6]	enet1.MDIO	enet2.MDIO	usb.OTG_PWR_WAKE	csi.MCLK	usdhc2.WP	gpio1.IO[6]	ccm.WAIT	ccm.REF_EN_B	uart1.CTS_B	Keeper
GPIO1_IO07	gpio1.IO[7]	enet1.MDC	enet2.MDC	usb.OTG_HOST_MODE	csi.PIXCLK	usdhc2.CD_B	gpio1.IO[7]	ccm.STOP	ecspi1.TESTER_TRIGGER	uart1.RTS_B	Keeper
GPIO1_IO08	gpio1.IO[8]	pwm1.OUT	wdog1.WDOG_B	spdif.OUT	csi.VSYNC	usdhc2.VSELECT	gpio1.IO[8]	ccm.PMIC_RDY	ecspi2.TESTER_TRIGGER	uart5.RTS_B	Keeper
GPIO1_IO09	gpio1.IO[9]	pwm2.OUT	global wdog	spdif.IN	csi.HSYNC	usdhc2.RESET_B	gpio1.IO[9]	usdhc1.RESET_B	ecspi3.TESTER_TRIGGER	uart5.CTS_B	Keeper
UART1_TXD	gpio1.IO[16]	uart1.TX	enet1.RDATA[2]	i2c3.SCL	csi.DATA[2]	gpt1.COMPARE1	gpio1.IO[16]	anatop.USBPHY1_TSTI_TX_LS_MODE	ecspi4.TESTER_TRIGGER	spdif.OUT	Keeper
UART1_RXD	gpio1.IO[17]	uart1.RX	enet1.RDATA[3]	i2c3.SDA	csi.DATA[3]	gpt1.CLK	gpio1.IO[17]	anatop.USBPHY1_TSTI_TX_HS_MODE	usdhc1.TESTER_TRIGGER	spdif.IN	Keeper
UART1_CTS	gpio1.IO[18]	uart1.CTS_B	enet1.RX_CLK	usdhc1.WP	csi.DATA[4]	enet2.1588_EVENT1_IN	gpio1.IO[18]	anatop.USBPHY1_TSTI_TX_DN	usdhc2.TESTER_TRIGGER	usdhc2.WP	Keeper
UART1_RTS	gpio1.IO[19]	uart1.RTS_B	enet1.TX_ER	usdhc1.CD_B	csi.DATA[5]	enet2.1588_EVENT1_OUT	gpio1.IO[19]	anatop.USBPHY1_TSTO_RX_SQUELCH	qspi.TESTER_TRIGGER	usdhc2.CD_B	Keeper
UART2_TXD	gpio1.IO[20]	uart2.TX	enet1.TDATA[2]	i2c4.SCL	csi.DATA[6]	gpt1.CAPTURE1	gpio1.IO[20]	anatop.USBPHY1_TSTO_RX_DISCON_DET	rawnand.TESTER_TRIGGER	ecspi3.SS0	Keeper
UART2_RXD	gpio1.IO[21]	uart2.RX	enet1.TDATA[3]	i2c4.SDA	csi.DATA[7]	gpt1.CAPTURE2	gpio1.IO[21]	anatop.USBPHY1_TSTO_RX_HS_RXD	sjc.DONE	ecspi3.SCLK	Keeper
UART2_CTS	gpio1.IO[22]	uart2.CTS_B	enet1.CRS	can2.TX	csi.DATA[8]	gpt1.COMPARE2	gpio1.IO[22]	anatop.USBPHY2_TSTO_RX_FS_RXD	sjc.DE_B	ecspi3.MOSI	Keeper
UART2_RTS	gpio1.IO[23]	uart2.RTS_B	enet1.COL	can2.RX	csi.DATA[9]	gpt1.COMPARE3	gpio1.IO[23]	anatop.USBPHY1_TSTO_RX_FS_RXD	sjc.FAIL	ecspi3.MISO	Keeper
UART3_TXD	gpio1.IO[24]	uart3.TX	enet2.RDATA[2]	sim1.PORT0_PD	csi.DATA[1]	uart2.CTS_B	gpio1.IO[24]	anatop.USBPHY1_TSTI_TX_DP	sjc.JTAG_ACT	anatop.OTG1_ID	Keeper
UART3_RXD	gpio1.IO[25]	uart3.RX	enet2.RDATA[3]	sim2.PORT0_PD	csi.DATA[0]	uart2.RTS_B	gpio1.IO[25]	anatop.USBPHY1_TSTI_TX_EN	sim_m.HADDR[0]	epit1.OUT	Keeper
UART3_CTS	gpio1.IO[26]	uart3.CTS_B	enet2.RX_CLK	can1.TX	csi.DATA[10]	enet1.1588_EVENT1_IN	gpio1.IO[26]	anatop.USBPHY1_TSTI_TX_HIZ	sim_m.HADDR[1]	epit2.OUT	Keeper
UART3_RTS	gpio1.IO[27]	uart3.RTS_B	enet2.TX_ER	can1.RX	csi.DATA[11]	enet1.1588_EVENT1_OUT	gpio1.IO[27]	anatop.USBPHY1_TSTO_RX_HS_RXD	sim_m.HADDR[2]	wdog1.WDOG_B	Keeper
UART4_TXD	gpio1.IO[28]	uart4.TX	enet2.TDATA[2]	i2c1.SCL	csi.DATA[12]	csu.CSU_ALARM_AUT[2]	gpio1.IO[28]	anatop.USBPHY1_TSTO_PLL_CLK20DIV	sim_m.HADDR[3]	ecspi2.SCLK	Keeper
UART4_RXD	gpio1.IO[29]	uart4.RX	enet2.TDATA[3]	i2c1.SDA	csi.DATA[13]	csu.CSU_ALARM_AUT[1]	gpio1.IO[29]	anatop.USBPHY2_TSTO_PLL_CLK20DIV	sim_m.HADDR[4]	ecspi2.SS0	Keeper
UART5_TXD	gpio1.IO[30]	uart5.TX	enet2.TX_ER	i2c2.SCL	csi.DATA[14]	csu.CSU_ALARM_AUT[0]	gpio1.IO[30]	anatop.USBPHY1_TSTO_RX_SQUELCH	sim_m.HADDR[5]	ecspi2.MOSI	Keeper
UART5_RXD	gpio1.IO[31]	uart5.RX	enet2.COL	i2c2.SDA	csi.DATA[15]	csu.CSU_INT_DEB	gpio1.IO[31]	anatop.USBPHY2_TSTO_RX_DISCON_DET	sim_m.HADDR[6]	ecspi2.MISO	Keeper
ENET1_RXD0	gpio2.IO[0]	enet1.RDATA[0]	uart4.RTS_B	pwm1.OUT	csi.DATA[16]	can1.TX	gpio2.IO[0]	kpp.ROW[0]	sim_m.HADDR[7]	usdhc1.LCTL	Keeper
ENET1_RXD1	gpio2.IO[1]	enet1.RDATA[1]	uart4.CTS_B	pwm2.OUT	csi.DATA[17]	can1.RX	gpio2.IO[1]	kpp.COL[0]	sim_m.HADDR[8]	usdhc2.LCTL	Keeper
ENET1_CRS_DV	gpio2.IO[2]	enet1.RX_EN	uart5.RTS_B	osc32k.32K_OUT	csi.DATA[18]	can2.TX	gpio2.IO[2]	kpp.ROW[1]	sim_m.HADDR[9]	usdhc1.VSELECT	Keeper
ENET1_TXD0	gpio2.IO[3]	enet1.TDATA[0]	uart5.CTS_B	anatop.24M_OUT	csi.DATA[19]	can2.RX	gpio2.IO[3]	kpp.COL[1]	sim_m.HADDR[10]	usdhc2.VSELECT	Keeper
ENET1_TXD1	gpio2.IO[4]	enet1.TDATA[1]	uart6.CTS_B	pwm5.OUT	csi.DATA[20]	enet2.MDIO	gpio2.IO[4]	kpp.ROW[2]	sim_m.HADDR[11]	wdog1.WDOG_RST_B_DEB	Keeper
ENET1_TXEN	gpio2.IO[5]	enet1.TX_EN	uart6.RTS_B	pwm6.OUT	csi.DATA[21]	enet2.MDC	gpio2.IO[5]	kpp.COL[2]	sim_m.HADDR[12]	wdog2.WDOG_RST_B_DEB	Keeper
ENET1_TXCLK	gpio2.IO[6]	enet1.TX_CLK	uart7.CTS_B	pwm7.OUT	csi.DATA[22]	anatop.ENET_REF_CLK1	gpio2.IO[6]	kpp.ROW[3]	sim_m.HADDR[13]	gpt1.CLK	Keeper
ENET1_RXER	gpio2.IO[7]	enet1.RX_ER	uart7.RTS_B	pwm8.OUT	csi.DATA[23]	weim.CRE	gpio2.IO[7]	kpp.COL[3]	sim_m.HADDR[14]	gpt1.CAPTURE2	Keeper
ENET2_RXD0	gpio2.IO[8]	enet2.RDATA[0]	uart6.TX	sim1.PORT0_TRXD	i2c3.SCL	enet1.MDIO	gpio2.IO[8]	kpp.ROW[4]	sim_m.HADDR[15]	usb.OTG1_PWR	Keeper
ENET2_RXD1	gpio2.IO[9]	enet2.RDATA[1]	uart6.RX	sim1.PORT0_CLK	i2c3.SDA	enet1.MDC	gpio2.IO[9]	kpp.COL[4]	sim_m.HADDR[16]	usb.OTG1_OC	Keeper
ENET2_CRS_DV	gpio2.IO[10]	enet2.RX_EN	uart7.TX	sim1.PORT0_RST_B	i2c4.SCL	weim.ADDR[26]	gpio2.IO[10]	kpp.ROW[5]	sim_m.HADDR[17]	anatop.ENET_REF_CLK_25M	Keeper
ENET2_TXD0	gpio2.IO[11]	enet2.TDATA[0]	uart7.RX	sim1.PORT0_SVEN	i2c4.SDA	weim.EB_B[2]	gpio2.IO[11]	kpp.COL[5]	sim_m.HADDR[18]	anatop.24M_OUT	Keeper
ENET2_TXD1	gpio2.IO[12]	enet2.TDATA[1]	uart8.TX	sim2.PORT0_TRXD	ecspi4.SCLK	weim.EB_B[3]	gpio2.IO[12]	kpp.ROW[6]	sim_m.HADDR[19]	usb.OTG2_PWR	Keeper
ENET2_TXEN	gpio2.IO[13]	enet2.TX_EN	uart8.RX	sim2.PORT0_CLK	ecspi4.MOSI	weim.ACLK_FREERUN	gpio2.IO[13]	kpp.COL[6]	sim_m.HADDR[20]	usb.OTG2_OC	Keeper
ENET2_TXCLK	gpio2.IO[14]	enet2.TX_CLK	uart8.CTS_B	sim2.PORT0_RST_B	ecspi4.MISO	anatop.ENET_REF_CLK2	gpio2.IO[14]	kpp.ROW[7]	sim_m.HADDR[21]	anatop.OTG2_ID	Keeper
ENET2_RXER	gpio2.IO[15]	enet2.RX_ER	uart8.RTS_B	sim2.PORT0_SVEN	ecspi4.SS0	weim.ADDR[25]	gpio2.IO[15]	kpp.COL[7]	sim_m.HADDR[22]	global wdog	Keeper
LCD_CLK	gpio3.IO[0]	lcdif.CLK	lcdif.WR_RWN	uart4.TX	sai3.MCLK	weim.CS2_B	gpio3.IO[0]	ocotp_ctrl_wrapper.FUSE_LATCHED	sim_m.HADDR[23]	wdog1.WDOG_RST_B_DEB	Keeper
LCD_ENABLE	gpio3.IO[1]	lcdif.ENABLE	lcdif.RD_E	uart4.RX	sai3.TX_SYNC	weim.CS3_B	gpio3.IO[1]	anatop.TESTI[0]	sim_m.HADDR[24]	ecspi2.RDY	Keeper
LCD_HSYNC	gpio3.IO[2]	lcdif.HSYNC	lcdif.RS	uart4.CTS_B	sai3.TX_BCLK	wdog3.WDOG_RST_B_DEB	gpio3.IO[2]	anatop.TESTI[1]	sim_m.HADDR[25]	ecspi2.SS1	Keeper
LCD_VSYNC	gpio3.IO[3]	lcdif.VSYNC	lcdif.BUSY	uart4.RTS_B	sai3.RX_DATA	wdog2.WDOG_B	gpio3.IO[3]	anatop.TESTI[2]	sim_m.HADDR[26]	ecspi2.SS2	Keeper
LCD_RESET	gpio3.IO[4]	lcdif.RESET	lcdif.CS	ca7_platform.EVENTI	sai3.TX_DATA	global wdog	gpio3.IO[4]	anatop.TESTI[3]	sim_m.HADDR[27]	ecspi2.SS3	Keeper
LCD_DATA00	gpio3.IO[5]	lcdif.DATA[0]	pwm1.OUT	ca7_platform.TRACE[0]	enet1.1588_EVENT2_IN	i2c3.SDA	gpio3.IO[5]	src.BT_CFG[0]	sim_m.HADDR[28]	sai1.MCLK	Keeper
LCD_DATA01	gpio3.IO[6]	lcdif.DATA[1]	pwm2.OUT	ca7_platform.TRACE[1]	enet1.1588_EVENT2_OUT	i2c3.SCL	gpio3.IO[6]	src.BT_CFG[1]	sim_m.HADDR[29]	sai1.TX_SYNC	Keeper
LCD_DATA02	gpio3.IO[7]	lcdif.DATA[2]	pwm3.OUT	ca7_platform.TRACE[2]	enet1.1588_EVENT3_IN	i2c4.SDA	gpio3.IO[7]	src.BT_CFG[2]	sim_m.HADDR[30]	sai1.TX_BCLK	Keeper
LCD_DATA03	gpio3.IO[8]	lcdif.DATA[3]	pwm4.OUT	ca7_platform.TRACE[3]	enet1.1588_EVENT3_OUT	i2c4.SCL	gpio3.IO[8]	src.BT_CFG[3]	sim_m.HADDR[31]	sai1.RX_DATA	Keeper
LCD_DATA04	gpio3.IO[9]	lcdif.DATA[4]	uart8.CTS_B	ca7_platform.TRACE[4]	enet2.1588_EVENT2_IN	sdma.PDB_CLK	gpio3.IO[9]	src.BT_CFG[4]	sim_m.HBURST[0]	sai1.TX_DATA	Keeper
LCD_DATA05	gpio3.IO[10]	lcdif.DATA[5]	uart8.RTS_B	ca7_platform.TRACE[5]	enet2.1588_EVENT2_OUT	spdif.OUT	gpio3.IO[10]	src.BT_CFG[5]	sim_m.HBURST[1]	ecspi1.SS1	Keeper
LCD_DATA06	gpio3.IO[11]	lcdif.DATA[6]	uart7.CTS_B	ca7_platform.TRACE[6]	enet2.1588_EVENT3_IN	spdif.LOCK	gpio3.IO[11]	src.BT_CFG[6]	sim_m.HBURST[2]	ecspi1.SS2	Keeper
LCD_DATA07	gpio3.IO[12]	lcdif.DATA[7]	uart7.RTS_B	ca7_platform.TRACE[7]	enet2.1588_EVENT3_OUT	spdif.EXT_CLK	gpio3.IO[12]	src.BT_CFG[7]	sim_m.HMASTLOCK	ecspi1.SS3	Keeper
LCD_DATA08	gpio3.IO[13]	lcdif.DATA[8]	spdif.IN	ca7_platform.TRACE[8]	csi.DATA[16]	weim.DATA[0]	gpio3.IO[13]	src.BT_CFG[8]	sim_m.HPROT[0]	can1.TX	Keeper
LCD_DATA09	gpio3.IO[14]	lcdif.DATA[9]	sai3.MCLK	ca7_platform.TRACE[9]	csi.DATA[17]	weim.DATA[1]	gpio3.IO[14]	src.BT_CFG[9]	sim_m.HPROT[1]	can1.RX	Keeper
LCD_DATA10	gpio3.IO[15]	lcdif.DATA[10]	sai3.RX_SYNC	ca7_platform.TRACE[10]	csi.DATA[18]	weim.DATA[2]	gpio3.IO[15]	src.BT_CFG[10]	sim_m.HPROT[2]	can2.TX	Keeper
LCD_DATA11	gpio3.IO[16]	lcdif.DATA[11]	sai3.RX_BCLK	ca7_platform.TRACE[11]	csi.DATA[19]	weim.DATA[3]	gpio3.IO[16]	src.BT_CFG[11]	sim_m.HPROT[3]	can2.RX	Keeper
LCD_DATA12	gpio3.IO[17]	lcdif.DATA[12]	sai3.TX_SYNC	ca7_platform.TRACE[12]	csi.DATA[20]	weim.DATA[4]	gpio3.IO[17]	src.BT_CFG[12]	sim_m.HREADYOUT	ecspi1.RDY	Keeper
LCD_DATA13	gpio3.IO[18]	lcdif.DATA[13]	sai3.TX_BCLK	ca7_platform.TRACE[13]	csi.DATA[21]	weim.DATA[5]	gpio3.IO[18]	src.BT_CFG[13]	sim_m.HRESP	usdhc2.RESET_B	Keeper
LCD_DATA14	gpio3.IO[19]	lcdif.DATA[14]	sai3.RX_DATA	ca7_platform.TRACE[14]	csi.DATA[22]	weim.DATA[6]	gpio3.IO[19]	src.BT_CFG[14]	sim_m.HSIZE[0]	usdhc2.DATA4	Keeper
LCD_DATA15	gpio3.IO[20]	lcdif.DATA[15]	sai3.TX_DATA	ca7_platform.TRACE[15]	csi.DATA[23]	weim.DATA[7]	gpio3.IO[20]	src.BT_CFG[15]	sim_m.HSIZE[1]	usdhc2.DATA5	Keeper
LCD_DATA16	gpio3.IO[21]	lcdif.DATA[16]	uart7.TX	ca7_platform.TRACE_CLK	csi.DATA[1]	weim.DATA[8]	gpio3.IO[21]	src.BT_CFG[24]	sim_m.HSIZE[2]	usdhc2.DATA6	Keeper
LCD_DATA17	gpio3.IO[22]	lcdif.DATA[17]	uart7.RX	ca7_platform.TRACE_CTL	csi.DATA[0]	weim.DATA[9]	gpio3.IO[22]	src.BT_CFG[25]	sim_m.HWRITE	usdhc2.DATA7	Keeper
LCD_DATA18	gpio3.IO[23]	lcdif.DATA[18]	pwm5.OUT	ca7_platform.EVENTO	csi.DATA[10]	weim.DATA[10]	gpio3.IO[23]	src.BT_CFG[26]	tpsmp.CLK	usdhc2.CMD	Keeper
LCD_DATA19	gpio3.IO[24]	lcdif.DATA[19]	pwm6.OUT	global wdog	csi.DATA[11]	weim.DATA[11]	gpio3.IO[24]	src.BT_CFG[27]	tpsmp.DATA_DIR	usdhc2.CLK	Keeper
LCD_DATA20	gpio3.IO[25]	lcdif.DATA[20]	uart8.TX	ecspi1.SCLK	csi.DATA[12]	weim.DATA[12]	gpio3.IO[25]	src.BT_CFG[28]	tpsmp.HTRANS[0]	usdhc2.DATA0	Keeper
LCD_DATA21	gpio3.IO[26]	lcdif.DATA[21]	uart8.RX	ecspi1.SS0	csi.DATA[13]	weim.DATA[13]	gpio3.IO[26]	src.BT_CFG[29]	tpsmp.HTRANS[1]	usdhc2.DATA1	Keeper
LCD_DATA22	gpio3.IO[27]	lcdif.DATA[22]	mqs.HIGHT	ecspi1.MOSI	csi.DATA[14]	weim.DATA[14]	gpio3.IO[27]	src.BT_CFG[30]	tpsmp.HDATA[0]	usdhc2.DATA2	Keeper
LCD_DATA23	gpio3.IO[28]	lcdif.DATA[23]	mqs.LEFT	ecspi1.MISO	csi.DATA[15]	weim.DATA[15]	gpio3.IO[28]	src.BT_CFG[31]	tpsmp.HDATA[1]	usdhc2.DATA3	Keeper
NAND_RE_B	gpio4.IO[0]	rawnand.RE_B	usdhc2.CLK	qspiB_SCLK	kpp.ROW[0]	weim.EB_B[1]	gpio4.IO[0]	anatop.TESTO[0]	tpsmp.HDATA[2]	ecspi3.SS2	Keeper
NAND_WE_B	gpio4.IO[1]	rawnand.WE_B	usdhc2.CMD	qspiB_SS0_B	kpp.COL[0]	weim.EB_B[1]	gpio4.IO[1]	anatop.TESTO[1]	tpsmp.HDATA[3]	ecspi3.SS3	Keeper
NAND_DATA00	gpio4.IO[2]	rawnand.DATA00	usdhc2.DATA0	qspiB_SS1_B	kpp.ROW[1]	weim.AD[8]	gpio4.IO[2]	anatop.TESTO[2]	tpsmp.HDATA[4]	ecspi4.RDY	Keeper
NAND_DATA01	gpio4.IO[3]	rawnand.DATA01	usdhc2.DATA1	qspiB_DQS	kpp.COL[1]	weim.AD[9]	gpio4.IO[3]	anatop.TESTO[3]	tpsmp.HDATA[5]	ecspi4.SS1	Keeper
NAND_DATA02	gpio4.IO[4]	rawnand.DATA02	usdhc2.DATA2	qspiB_DATA[0]	kpp.ROW[2]	weim.AD[10]	gpio4.IO[4]	anatop.TESTO[4]	tpsmp.HDATA[6]	ecspi4.SS2	Keeper
NAND_DATA03	gpio4.IO[5]	rawnand.DATA03	usdhc2.DATA3	qspiB_DATA[1]	kpp.COL[2]	weim.AD[11]	gpio4.IO[5]	anatop.TESTO[5]	tpsmp.HDATA[7]	ecspi4.SS3	Keeper
NAND_DATA04	gpio4.IO[6]	rawnand.DATA04	usdhc2.DATA4	qspiB_DATA[2]	ecspi4.SCLK	weim.AD[12]	gpio4.IO[6]	anatop.TESTO[6]	tpsmp.HDATA[8]	uart2.TX	Keeper
NAND_DATA05	gpio4.IO[7]	rawnand.DATA05	usdhc2.DATA5	qspiB_DATA[3]	ecspi4.MOSI	weim.AD[13]	gpio4.IO[7]	anatop.TESTO[7]	tpsmp.HDATA[9]	uart2.RX	Keeper
NAND_DATA06	gpio4.IO[8]	rawnand.DATA06	usdhc2.DATA6	sai2.RX_BCLK	ecspi4.MISO	weim.AD[14]	gpio4.IO[8]	anatop.TESTO[8]	tpsmp.HDATA[10]	uart2.CTS_B	Keeper
NAND_DATA07	gpio4.IO[9]	rawnand.DATA07	usdhc2.DATA7	qspiA_SS1_B	ecspi4.SS0	weim.AD[15]	gpio4.IO[9]	anatop.TESTO[9]	tpsmp.HDATA[11]	uart2.RTS_B	Keeper
NAND_ALE	gpio4.IO[10]	rawnand.ALE	usdhc1.RESET_B	qspiA_DQS	pwm3.OUT	weim.ADDR[17]	gpio4.IO[10]	anatop.TESTO[10]	tpsmp.HDATA[12]	ecspi3.SS1	Keeper
NAND_WP_B	gpio4.IO[11]	rawnand.WP_B	usdhc1.RESET_B	qspiA_SCLK	pwm4.OUT	weim.BCLK	gpio4.IO[11]	anatop.TESTO[11]	tpsmp.HDATA[13]	ecspi3.RDY	Keeper
NAND_READY_B	gpio4.IO[12]	rawnand.READY_B	usdhc1.DATA4	qspiA_DATA[0]	ecspi3.SS0	weim.CS1_B	gpio4.IO[12]	anatop.TESTO[12]	tpsmp.HDATA[14]	uart3.TX	Keeper
NAND_CE0_B	gpio4.IO[13]	rawnand.CE0_B	usdhc1.DATA5	qspiA_DATA[1]	ecspi3.SCLK	weim.DTACK_B	gpio4.IO[13]	anatop.TESTO[13]	tpsmp.HDATA[15]	uart3.RX	Keeper
NAND_CE1_B	gpio4.IO[14]	rawnand.CE1_B	usdhc1.DATA6	qspiA_DATA[2]	ecspi3.MOSI	weim.ADDR[18]	gpio4.IO[14]	anatop.TESTO[14]	tpsmp.HDATA[16]	uart3.CTS_B	Keeper
NAND_CLE	gpio4.IO[15]	rawnand.CLE	usdhc1.DATA7	qspiA_DATA[3]	ecspi3.MISO	weim.ADDR[16]	gpio4.IO[15]	anatop.TESTO[15]	tpsmp.HDATA[17]	uart3.RTS_B	Keeper
NAND_DQS	gpio4.IO[16]	rawnand.DQS	csi.FIELD	qspiA_SS0_B	pwm5.OUT	weim.WAIT	gpio4.IO[16]	sdma.EXT_EVENT[1]	tpsmp.HDATA[18]	spdif.EXT_CLK	Keeper
SD1_CMD	gpio2.IO[16]	usdhc1.CMD	gpt2.COMPARE1	sai2.RX_SYNC	spdif.OUT	weim.ADDR[19]	gpio2.IO[16]	sdma.EXT_EVENT[0]	tpsmp.HDATA[19]	usb.OTG1_PWR	Keeper
SD1_CLK	gpio2.IO[17]	usdhc1.CLK	gpt2.COMPARE2	sai2.MCLK	spdif.IN	weim.ADDR[20]	gpio2.IO[17]	ccm.OUT0	observe_mux.OUT[0]	usb.OTG1_OC	Keeper
SD1_DATA0	gpio2.IO[18]	usdhc1.DATA0	gpt2.COMPARE3	sai2.TX_SYNC	can1.TX	weim.ADDR[21]	gpio2.IO[18]	ccm.OUT1	observe_mux.OUT[1]	anatop.OTG1_ID	Keeper
SD1_DATA1	gpio2.IO[19]	usdhc1.DATA1	gpt2.CLK	sai2.TX_BCLK	can1.RX	weim.ADDR[22]	gpio2.IO[19]	ccm.OUT2	observe_mux.OUT[2]	usb.OTG2_PWR	Keeper
SD1_DATA2	gpio2.IO[20]	usdhc1.DATA2	gpt2.CAPTURE1	sai2.RX_DATA	can2.TX	weim.ADDR[23]	gpio2.IO[20]	ccm.CLKO1	observe_mux.OUT[3]	usb.OTG2_OC	Keeper
SD1_DATA3	gpio2.IO[21]	usdhc1.DATA3	gpt2.CAPTURE2	sai2.TX_DATA	can2.RX	weim.ADDR[24]	gpio2.IO[21]	ccm.CLKO2	observe_mux.OUT[4]	anatop.OTG2_ID	Keeper
CSI_MCLK	gpio4.IO[17]	csi.MCLK	usdhc2.CD_B	rawnand.CE2_B	i2c1.SDA	weim.CS0_B	gpio4.IO[17]	snvs_hp_wrapper.VIO_5_CTL	tpsmp.HDATA[20]	uart6.TX	Keeper
CSI_PIXCLK	gpio4.IO[18]	csi.PIXCLK	usdhc2.WP	rawnand.CE3_B	i2c1.SCL	weim.OE	gpio4.IO[18]	snvs_hp_wrapper.VIO_5	tpsmp.HDATA[21]	uart6.RX	Keeper
CSI_VSYNC	gpio4.IO[19]	csi.VSYNC	usdhc2.CLK	sim1.PORT1_CLK	i2c2.SDA	weim.RW	gpio4.IO[19]	pwm7.OUT	tpsmp.HDATA[22]	uart6.RTS_B	Keeper
CSI_HSYNC	gpio4.IO[20]	csi.HSYNC	usdhc2.CMD	sim1.PORT1_PD	i2c2.SCL	weim.LBA_B	gpio4.IO[20]	pwm8.OUT	tpsmp.HDATA[23]	uart6.CTS_B	Keeper
CSI_DATA00	gpio4.IO[21]	csi.DATA[2]	usdhc2.DATA0	sim1.PORT1_RST_B	ecspi2.SCLK	weim.AD[0]	gpio4.IO[21]	src.INT_BOOT	tpsmp.HDATA[24]	uart5.TX	Keeper
CSI_DATA01	gpio4.IO[22]	csi.DATA[3]	usdhc2.DATA1	sim1.PORT1_SVEN	ecspi2.SS0	weim.AD[1]	gpio4.IO[22]	sai1.MCLK	tpsmp.HDATA[25]	uart5.RX	Keeper
CSI_DATA02	gpio4.IO[23]	csi.DATA[4]	usdhc2.DATA2	sim1.PORT1_TRXD	ecspi2.MOSI	weim.AD[2]	gpio4.IO[23]	sai1.RX_SYNC	tpsmp.HDATA[26]	uart5.RTS_B	Keeper
CSI_DATA03	gpio4.IO[24]	csi.DATA[5]	usdhc2.DATA3	sim2.PORT1_PD	ecspi2.MISO	weim.AD[3]	gpio4.IO[24]	sai1.RX_BCLK	tpsmp.HDATA[27]	uart5.CTS_B	Keeper
CSI_DATA04	gpio4.IO[25]	csi.DATA[6]	usdhc2.DATA4	sim2.PORT1_CLK	ecspi2.SCLK	weim.AD[4]	gpio4.IO[25]	sai1.TX_SYNC	tpsmp.HDATA[28]	usdhc1.WP	Keeper
CSI_DATA05	gpio4.IO[26]	csi.DATA[7]	usdhc2.DATA5	sim2.PORT1_RST_B	ecspi1.SS0	weim.AD[5]	gpio4.IO[26]	sai1.TX_BCLK	tpsmp.HDATA[29]	usdhc1.CD_B	Keeper
CSI_DATA06	gpio4.IO[27]	csi.DATA[8]	usdhc2.DATA6	sim2.PORT1_SVEN	ecspi1.MOSI	weim.AD[6]	gpio4.IO[27]	sai1.RX_DATA	tpsmp.HDATA[30]	usdhc1.RESET_B	Keeper
CSI_DATA07	gpio4.IO[28]	csi.DATA[9]	usdhc2.DATA7	sim2.PORT1_TRXD	ecspi1.MISO	weim.AD[7]	gpio4.IO[28]	sai1.TX_DATA	tpsmp.HDATA[31]	usdhc1.VSELECT	Keeper