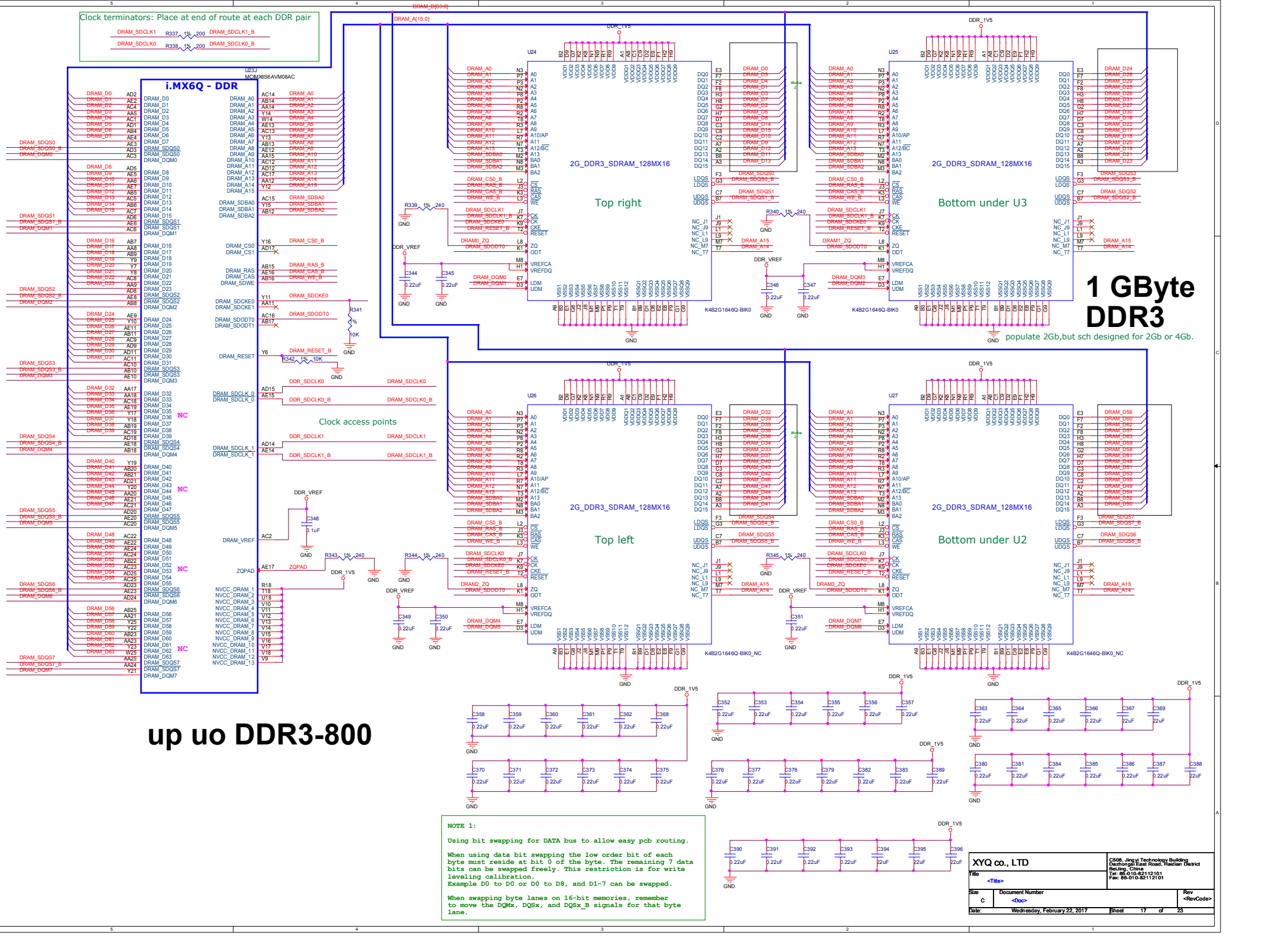
Clock terminators: Place at end of route at each DDR pair
DRAM_SDCLK1
R337 1% 200
DRAM_SDCLK1_B
DRAM_SDCLK0
R338 1% 200
DRAM_SDCLK0_B
i.MX6Q - DDR
U23J
MCIMX6S6AVM08AC
DRAM_D[63:0]
DRAM_A[15:0]
U24
U25
U26
U27
2G_DDR3_SDRAM_128MX16
Top right
Bottom under U3
Top left
Bottom under U2
K4B2G1646Q-BIK0
K4B2G1646Q-BIK0_NC
DDR_1V5
DDR_VREF
GND
Clock access points
1 GByte
DDR3
populate 2Gb,but sch designed for 2Gb or 4Gb.
up uo DDR3-800
NOTE 1:
Using bit swapping for DATA bus to allow easy pcb routing.
When using data bit swapping the low order bit of each byte must reside at bit 0 of the byte. The remaining 7 data bits can be swapped freely. This restriction is for write leveling calibration.
Example D0 to D0 or D0 to D8, and D1-7 can be swapped.
When swapping byte lanes on 16-bit memories, remember to move the DQMx, DQSx, and DQSx_B signals for that byte lane.
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