i.MX 6SoloX Applications Processors: Full Training Session

FTF-DES-F1131

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External Use

Agenda

- i.MX 6SoloX Introduction

  - Positioning Within i.MX 6 Series Portfolio

  - Target Markets and Use Cases

  - Device Options (Package, GPU, Use Profile)

  - Development Systems, Software and Tools Availability

- Technical Overview

  - Introduction to Heterogeneous Multicore Processing

  - The benefit and Features of New IP Blocks on i.MX 6SoloX

  - Low-power Architecture and Preliminary Results

  - Introduction to the Multi-Core Communication Library

Session Introduction

- This session introduces one of the newest member of the i.MX 6 series, the i.MX 6SoloX heterogeneous dual-core multimedia applications processor

  - Understand the target markets and benefits of the i.MX 6SoloX and how it is positioned within the i.MX 6 series portfolio.

  - With three different package offerings and four unique ball maps, learn how to select the device which is the best fit for your application.

  - Learn about the product availability, software, development systems, tools and timeframe for general market availability.

  - A detailed technical overview will be given on Cortex-A and Cortex-M heterogeneous multicore processing (HMP) and use cases, and the key differentiating features of the i.MX 6SoloX, including new IP and low-power modes available exclusively on the i.MX 6SoloX.

  - A detailed technical overview will be given of the Multi-Core Communication software.

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Session Objectives

- After completing this session you will be able to:
  - Identify the key features and positioning of the i.MX 6SoloX.
  - Determine the right package and device for your design.
  - Know your options for hardware and software development.
  - Understand the benefit of HMP and the new IP blocks and low-power design on i.MX 6SoloX.
  - Understand the basics of the Multi-Core Communications (MCC) library to realize operating environments between the A9 and M4 cores.

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i.MX Application Processors Core Values

Scalability
- CPU (single/dual/quad, asymmetric), GPU, IO
- Software: Linux, Android, QNX, Windows Embedded, RTOS
- Industry Leading Ecosystem and Partnerships

Integration
- Automotive/Industrial/Consumer peripheral sets
- Packaging to Meet Market Requirements
- Qualifications: AEC-Q100, JEDEC Industrial and Consumer

Trust
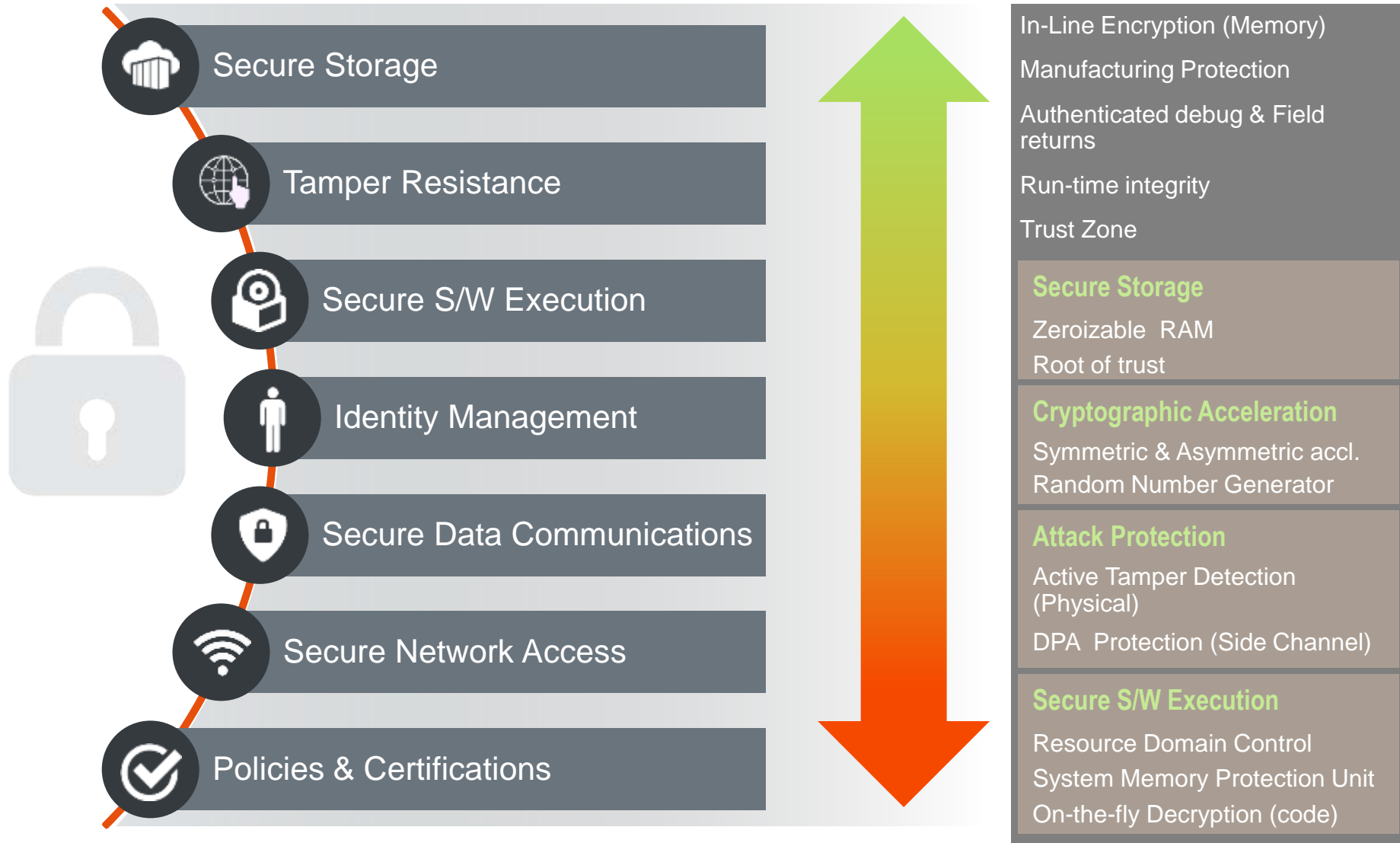- Longevity: Minimum of 10-15 years in all markets
- Consistency of Supply, Accessibility
- Quality, Robustness, Zero-defect methodology
- Security and Safety

Ease of Adoption
- Communities, Innovation, Support
- Design Collateral, Distribution
- System Solutions: SoC, Sensors, PMIC, IoT Comms, SBC

Product **Longevity**

RIoTboard

SolidRun

WaRP

WANDBOARD.ORG

UDOO

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Leadership Security – i.MX Hardware Enablement

Secure Storage

Tamper Resistance

Secure S/W Execution

Identity Management

Secure Data Communications

Secure Network Access

Policies & Certifications

In-Line Encryption (Memory)

Manufacturing Protection

Authenticated debug & Field returns

Run-time integrity

Trust Zone

Secure Storage

Zeroizable RAM

Root of trust

Cryptographic Acceleration

Symmetric & Asymmetric accl.
Random Number Generator

Attack Protection

Active Tamper Detection (Physical)

DPA Protection (Side Channel)

Secure S/W Execution

Resource Domain Control
System Memory Protection Unit
On-the-fly Decryption (code)

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i.MX 6SoloX

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i.MX 6 Series at a Glance

Red indicates change from column to the left

i.MX 6 UltraLite
- Single ARM® Cortex®-A7 up to 528 MHz
- 128 KB L2 cache, Neon, VFP, Trustzone
- X16 LPDDR2, DDR3/LV-DDR3
- 2X 10/100 Mb/s + IEEE 1588
- 2X 12-bit ADC (1 with resistance touch control)
- 10/100 Ethernet MAC

i.MX 6 SoloLite
- Single Cortex®-A9 up to 1.0 GHz
- 256 KB L2 cache, Neon, VFPvd16 Trustzone
- 2D graphics
- 32-bit DDR3 and LPDDR2 at 400 MHz
- Integrated EPD controller
- 10/100 Ethernet MAC

i.MX 6 SoloX
- Single Cortex®-A9 up to 1.0 GHz
- Single Cortex®-M4 up to 200 MHz
- 256 KB L2 cache, Neon, VFP, Trustzone
- 3D and 2D graphics
- 32-bit DDR3 and LPDDR2 at 400 MHz
- Dual Gigabit Ethernet MAC w/ hardware AVB support
- PCIe controller plus PHY
- LVDS controller plus PHY
- Analog camera interface
- 8-channel, 12-bit ADC
- MLB and FlexCAN controllers

i.MX 6 Solo
- Single Cortex®-A9 up to 1.0 GHz
- 512 KB L2 cache, Neon, VFPvd16 Trustzone
- 3D graphics with one shader
- 2D graphics
- 32-bit DDR3 and LPDDR2 at 400 MHz
- Gigabit Ethernet MAC
- Integrated EPD controller
- HDMIv1.4 controller plus PHY
- LVDS controller plus PHY
- PCIe controller plus PHY
- MLB and FlexCAN controllers

i.MX 6 DualLite
- Dual Cortex®-A9 up to 1.0 GHz
- 512 KB L2 cache, Neon, VFPvd16 Trustzone
- 3D graphics with one shader
- 2D graphics
- 64-bit DDR3 and 2-channel LPDDR2 at 400 MHz
- Gigabit Ethernet MAC
- Integrated EPD controller
- HDMIv1.4 controller plus PHY
- LVDS controller plus PHY
- PCIe controller plus PHY
- MLB and FlexCAN controllers

i.MX 6 Dual
- Dual Cortex®-A9 up to 1.2 GHz
- 1 MB L2 cache, Neon, VFPvd16 Trustzone
- 3D graphics with four shaders
- Two 2D graphics engines
- 64-bit DDR3 and 2-channel 32-bit LPDDR2 at 533 MHz
- Gigabit Ethernet MAC
- Integrated SATA-II
- HDMIv1.4 controller plus PHY
- LVDS controller plus PHY
- PCIe controller plus PHY
- MLB and FlexCAN controllers

i.MX 6 DualPlus
- Dual Cortex®-A9 up to 1.2 GHz
- 1 MB L2 cache, Neon, VFPvd16 Trustzone
- Enhanced 3D graphics with four shaders
- Enhanced Two 2D graphics engines
- Prefetch & Resolve Engine
- Gigabit Ethernet MAC
- Optimized 64-bit DDR3 and 2-channel 32-bit LPDDR2 at 533 MHz
- Integrated SATA-II
- HDMIv1.4 controller plus PHY
- LVDS controller plus PHY
- PCIe controller plus PHY
- MLB and FlexCAN controllers

i.MX 6 Quad
- Quad Cortex®-A9 up to 1.2 GHz
- 1 MB L2 cache, Neon, VFPvd16 Trustzone
- 3D graphics with four shaders
- Two 2D graphics engines
- 64-bit DDR3 and 2-channel 32-bit LPDDR2 at 533 MHz
- Gigabit Ethernet MAC
- Integrated SATA-II
- HDMIv1.4 controller plus PHY
- LVDS controller plus PHY
- PCIe controller plus PHY
- MLB and FlexCAN controllers

i.MX 6 QuadPlus
- Quad Cortex®-A9 up to 1.2 GHz
- 1 MB L2 cache, Neon, VFPvd16 Trustzone
- Enhanced 3D graphics with four shaders
- Enhanced Two 2D graphics engines
- Prefetch & Resolve Engine
- Gigabit Ethernet MAC
- Optimized 64-bit DDR3 and 2-channel 32-bit LPDDR2 at 533 MHz
- Integrated SATA-II
- HDMIv1.4 controller plus PHY
- LVDS controller plus PHY
- PCIe controller plus PHY
- MLB and FlexCAN controllers

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Consumer　Industrial　Automotive

i.MX 6SoloX Target Applications

Automotive

- Telematics
- Vehicle to vehicle connectivity
- Entry-level Infotainment

Smart Devices

- Health Care – patient monitoring, fitness equipment, wearables
- Factory, process and building automation (thermostats, gateways, surveillance, HMI)
- Handheld scanners and printers
- Home audio, appliances, VoIP
- Test and Measurement
- Transportation - industrial vehicle with control & HMI, e.g. tractor, train, ship, heavy equipment

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Market Challenge

- Growing number of embedded use cases require concurrent execution of <u>isolated and secure</u> software environments within the system

- Multiple software execution environments are needed for:
  - Real-time performance
  - System integrity and security
  - Power consumption
  - Fast boot

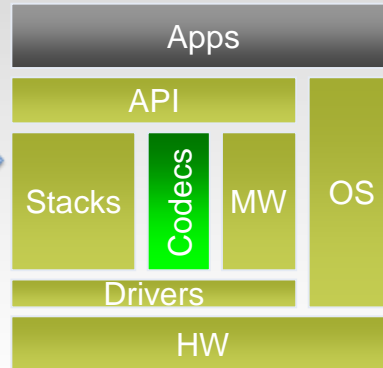OFFLOAD TASKS   OPTIMIZE POWER   INCREASE SECURITY

i.MX 6SoloX: Enablement

i.MX 6SoloX

Hardware Platform

SABRE SDB

- Richly featured development systems and accessories
- Ease of Use – BSP and demo images, development environment build demonstration, video tutorials, schematics and layout, documentation

Full hardware evaluation and development platforms

+ Software

- Mature, full-featured and and optimized BSPs for latest Linux and Android releases; MQX BSP for Cortex-M4 with multi-core communication (MCC) API
- Optimized audio codecs and code-signing tools to support on-chip security features

Complete software package to streamline software development

+ Ecosystem

- Hardware – Embedded Board Solutions (EBS)
- Tool chains
- Software – RTOS, OS, codecs, middleware/applications
- Design services
- System integrators
- Training

Technology alliances for building smarter, better connected solutions

www.freescale.com/imxcommunity

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Enabling Faster Time to Market

i.MX 6SoloX development tools are **Freescale designed** and **Freescale supported**

i.MX 6SoloX
SABRE SDB

- i.MX 6SoloX applications processor
  - 1GHz Cortex-A9 processor
  - 200MHz Cortex-M4 processor
  - 19x19 BGA, 0.8mm pitch
- OS: Linux and Android (Cortex-A9), MQX (Cortex-M4)
- 1GB total x16 DDR3-800
- Dual DDR Quad SPI
- Mini-PCIe
- 2x GbE PHYs and 2x Ethernet RJ45 connectors
- 1x Type A USB, 1x Micro-AB USB
- 1x CAN connector
- 3x Full-size SD slots (boot/storage/Wi-Fi)
- Stereo audio codec, microphone input
- Accessory boards (available separately): 10.1"
  capacitive multi-touch display (MCIMX-LVDS1), Wi-Fi
- Availability:
  - **Now**
  - **Part Number: MCIMX6SX-SDB**
  - **Price: $399**

i.MX 6SoloX SABRE for
Automotive Infotainment

- Available to Tier 1 automotive OEMs
- i.MX 6SoloX applications processor
  - 800MHz Cortex-A9 processor
  - 166MHz Cortex-M4 processor
  - 19x19 BGA, 0.8mm pitch
- OS: Linux and Android (Cortex-A9), MQX (Cortex-M4)
- 1GB total x16 DDR3-800
- Dual DDR Quad SPI
- 2x Ethernet connectors, mini/micro USB
- 2x Full-size SD slots (boot/storage/Wi-Fi)
- 2x CAN connectors, 1x MLB connector
- Analog video input
- 8ch audio codec, microphone input
- Support for terrestrial and satellite radio tuners, Wi-Fi, Bluetooth, GPS, cellular modem, iAP authentication modules, MOST vehicle networking, cameras and displays
- Accessory boards (available separately): 10.1" capacitive multi-touch display (MCIMX-LVDS1), Wi-Fi
- Available in Q32015

Preliminary, subject to change

i.MX 6SoloX: SABRE Board Key Features

Processor
- Freescale i.MX 6SoloX 19x19 package
  - Cortex-A9 CPU @1GHz
  - Cortex-M4 CPU @200MHz
- Freescale PF0200 Power Management IC

Memory
- 1 GB DDR3
- Footprint for Managed NAND (eMMC/eSD)
- 32MB x2 QuadSPI Flash
- SD/MMC socket

Display/Camera
- LVDS display connector
- Parallel LCD expansion connector
- Parallel camera connector

Wireless
- Via external module

Audio
- 3.5 mm audio stereo HP jack
- Board mounted microphone

  - Part Number: MCIMX6SX-SDB

Connectivity
- USB host connector
- Micro USB OTG connector
- 2x Ethernet (1Gbit) connector
- mPCIe connector
- 2x CAN (DB-9) using Freescale MC34901 CAN transceiver
- 12-bit ADC connector
- GPIO

Debug
- JTAG connector
- UART via USB

Sensors
- Freescale MMA8451 three-axis digital accelerometer
- Freescale MAG3110 three-axis digital magnetometer
- Ambient light sensor

Tools & OS Support
- Cortex-A9
  - Linux®
  - Android™
- Cortex-M4
  - MQX

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i.MX 6SoloX Technical Overview

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i.MX 6 SoloX Advantages

- **Heterogeneous architecture with smart system power**
  - Single Cortex-A9 paired with a Cortex-M4
    - Enables concurrent execution of multiple software environments to provide high performance with real time responsiveness, allowing for smart system power.
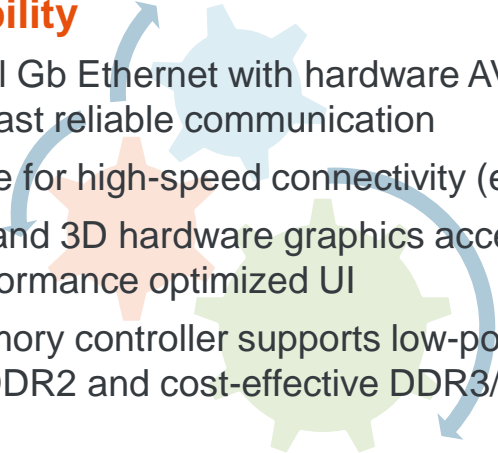
- **Optimized Power**
  - Maintain a system aware and power efficient state with complete shut down of the Cortex-A9 core, with the Cortex-M4 still active and performing low-level system monitoring tasks.

Energy
Efficient Solutions
by Freescale
™

- **Optimized integration for design flexibility**
  - Dual Gb Ethernet with hardware AVB support for fast reliable communication
  - PCIe for high-speed connectivity (e.g. Wi-Fi)
  - 2D and 3D hardware graphics acceleration for performance optimized UI
  - Memory controller supports low-power LPDDR2 and cost-effective DDR3/DDR3L

- **Secure solutions for optimized performance efficiency**
  - On-chip resource domain controller providing a centralized programming model to configure isolation and sharing of system resources.
  - Advanced security supporting high assurance (secure) boot, cryptographic cipher engines and random number generator.

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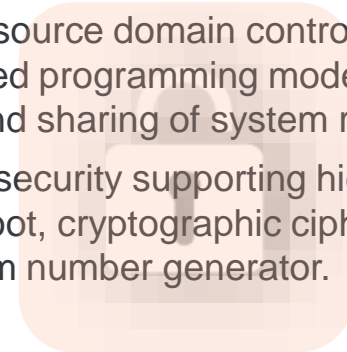
Package Options

14 x 14, 0.65p	17 x 17 NP, 0.8p	17 x 17 WP, 0.8p	19 x 19, 0.8p
Optimized for smallest form-factor designs	Optimized for lowest cost board design w/o PCIe	Optimized for lowest cost board design w PCIe	Full-featured package for HMI based designs
2D/3D GPU is optional	2D/3D GPU is optional	2D/3D GPU is optional	2D/3D GPU is standard
No PCIe	No PCIe	PCIe is standard	PCIe is standard
Parallel LCD interface	Parallel LCD interface	Parallel LCD interface	Parallel and LVDS interfaces
ADC is standard	ADC is standard	No ADC	ADC is standard
Automotive, industrial and consumer parts	Automotive, industrial and consumer parts	Automotive, industrial and consumer parts	Automotive, industrial and consumer parts

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i.MX 6SoloX 19x19

- Specifications:
  - CPU1: ARM Cortex-A9 at 800MHz-1GHz
  - CPU2: ARM Cortex-M4 at 166MHz-200MHz
  - Package: 19x19 VM, 0.8mm pitch MAPBGA
  - Device options: 6X4
- Key Features and Advantages
  - Cortex-A9 to run open OS or RTOS
  - Cortex-M4 for real-time response, system control / CAN messaging and low-power system monitoring
  - Support for 32-bit LPDDR2 and DDR3/DDR3L up to 400MHz (800MHz DDR)
  - Multiple boot sources include managed NAND, raw NAND, parallel NOR and dual DDR Quad SPI
  - Multimedia:
    - Vivante GC400T GPU supporting 27M Tri/s, 166M Pxl/s OpenGLES 2.x / OpenVG 1.x (6X3 only)
    - LVDS and parallel display interfaces up to WXGA
    - Video ADC (NTSC/PAL) plus 20-bit parallel CSI
    - Parallel LCD display interface up to WXGA
  - Connectivity:
    - USB HS Host + OTG with PHY, USB HSIC for Modem Interface
    - 2x Gb Ethernet with AVB
    - 1x PCIe 2.0 (x1 lane)
    - 2x FlexCAN / CAN FD, 1x MLB25/50 (automotive only)
    - 2x 8-ch 12-bit SAR ADC

Qual. Type	Temp. Range	6X4
Extended Commercial	-20C to +105C	Y
Industrial	-40C to +105C	Y
Automotive	-40C to +125C	Y

i.MX 6SoloX 19x19

System Control
- Secure JTAG
- PLL, Osc
- Clock & Reset
- Smart DMA
- IOMUX
- Timer x3
- PWM x8
- Watch Dog x3

Power Mgmt
- LDO
- Temp Monitor

ADC
- 8ch 12-bit ADC

Internal Memory
- ROM
- RAM

Security
- RNG
- TrustZone
- Ciphers
- Security Ctrl
- Secure RTC
- eFuses

CPU1 Platform
- Cortex-A9
- 32KB I-cache | 32KB D-cache
- NEON | PTM
- 256KB L2-cache

CPU2 Platform
- Cortex-M4, MPU, FPU
- 16KB I-cache | 16KB D-cache
- 64KB TCM

Graphics
- Graphics: OpenGL/ES 2.x, OpenVG 1.x (on 3D GPU)
- BitBLT, DirectFB / GAL

LCD Interfaces
- 24-bit RGB
- 1ch LVDS

Imaging Processing
- Resizing, Blending Inversion / Rotation

Camera Interfaces
- 20-bit Parallel RGB
- Analog NTSC

Connectivity
- MMC 4.4 / SD 3.0 x2
- MMC 4.4 / SDXC
- NAND (BCH60)
- UART x6
- I²C x4, SPI x5
- USB2 OTG & PHY USB2 Host & PHY
- USB2 HSIC Host
- 2x 1Gb Ethernet + IEEE1588 +AVB
- ESAI, I²S/SSI x5
- S/PDIF Tx/Rx
- ASRC
- 2 x FlexCAN/FD
- MLB25/50
- GPIO, Keypad
- 1x PCIe 2.0 (x1 lane)

External Memory
- 16-bit NOR
- 2x DDR Quad SPI
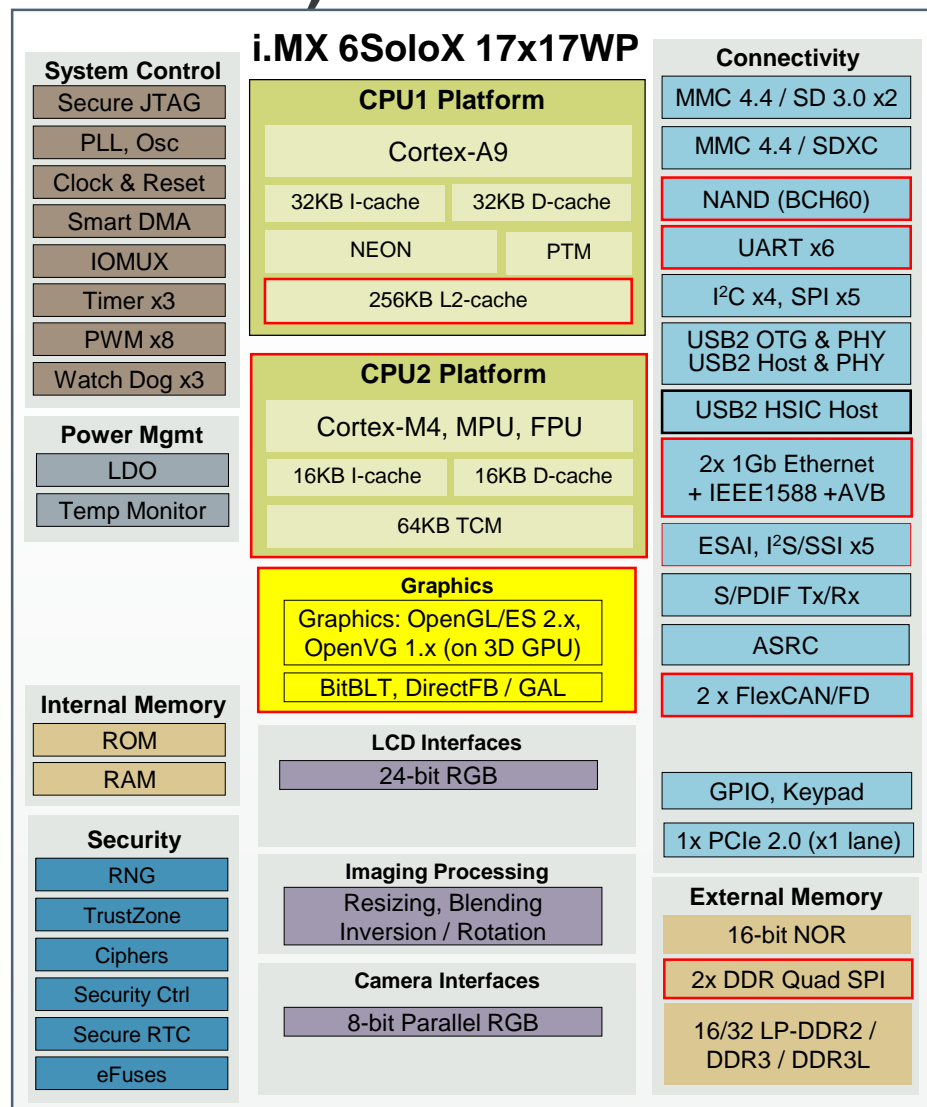- 16/32 LP-DDR2 / DDR3 / DDR3L

☐ Updated from i.MX 6Solo   ☐ 6X3 only   ☐ Auto only

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i.MX 6SoloX 17x17WP (WP = With PCIe)

- Specifications:
  - CPU1: ARM Cortex-A9 at 800MHz-1GHz
  - CPU2: ARM Cortex-M4 at 166MHz-200MHz
  - Package: 17x17 VN, 0.8mm pitch MAPBGA
  - Device options: 6X2 (no GPU), 6X3 (with GPU)
- Key Features and Advantages
  - Cortex-A9 to run open OS or RTOS
  - Cortex-M4 for real-time response, system control / CAN messaging and low-power system monitoring
  - Support for 32-bit LPDDR2 and DDR3/DDR3L up to 400MHz (800MHz DDR)
  - Multiple boot sources include managed NAND, raw NAND, parallel NOR and dual DDR Quad SPI
  - Multimedia:
    - Vivante GC400T GPU supporting 27M Tri/s, 166M Pxl/s OpenGLES 2.x / OpenVG 1.x (6X3 only)
    - Parallel LCD display interface up to WXGA
    - 8-bit CSI via RGMII2
  - Connectivity:
    - USB HS Host + OTG with PHY, USB HSIC for Modem Interface
    - 2x Gb Ethernet with AVB
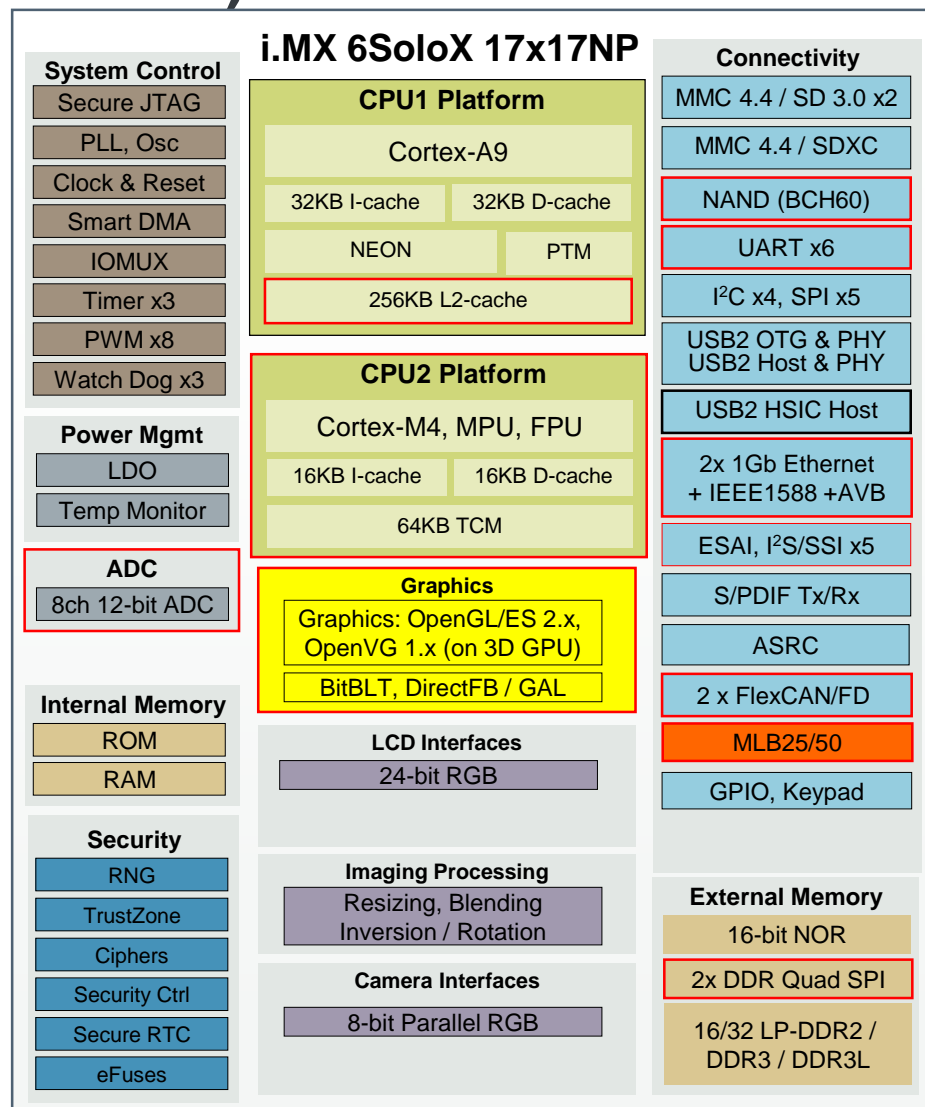   - 1x PCIe 2.0 (x1 lane)
    - 2x FlexCAN / CAN FD

Qual. Type	Temp. Range	6X2	6X3
Extended Commercial	-20C to +105C	Y	Y
Industrial	-40C to +105C	Y	Y

i.MX 6SoloX 17x17WP

System Control
- Secure JTAG
- PLL, Osc
- Clock & Reset
- Smart DMA
- IOMUX
- Timer x3
- PWM x8
- Watch Dog x3

Power Mgmt
- LDO
- Temp Monitor

Internal Memory
- ROM
- RAM

Security
- RNG
- TrustZone
- Ciphers
- Security Ctrl
- Secure RTC
- eFuses

CPU1 Platform
- Cortex-A9
- 32KB I-cache
- 32KB D-cache
- NEON
- PTM
- 256KB L2-cache

CPU2 Platform
- Cortex-M4, MPU, FPU
- 16KB I-cache
- 16KB D-cache
- 64KB TCM

Graphics
- Graphics: OpenGL/ES 2.x, OpenVG 1.x (on 3D GPU)
- BitBLT, DirectFB / GAL

LCD Interfaces
- 24-bit RGB

Imaging Processing
- Resizing, Blending Inversion / Rotation

Camera Interfaces
- 8-bit Parallel RGB

Connectivity
- MMC 4.4 / SD 3.0 x2
- MMC 4.4 / SDXC
- NAND (BCH60)
- UART x6
- I2C x4, SPI x5
- USB2 OTG & PHY USB2 Host & PHY
- USB2 HSIC Host
- 2x 1Gb Ethernet + IEEE1588 +AVB
- ESAI, I2S/SSI x5
- S/PDIF Tx/Rx
- ASRC
- 2 x FlexCAN/FD
- GPIO, Keypad
- 1x PCIe 2.0 (x1 lane)

External Memory
- 16-bit NOR
- 2x DDR Quad SPI
- 16/32 LP-DDR2 / DDR3 / DDR3L

Updated from i.MX 6Solo   6X3 only

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i.MX 6SoloX 17x17NP (NP = No PCIe)

- Specifications:
  - CPU1: ARM Cortex-A9 at 800MHz-1GHz
  - CPU2: ARM Cortex-M4 at 166MHz-200MHz
  - Package: 17x17 VO, 0.8mm pitch MAPBGA
  - Device options: 6X1 (no GPU), 6X3 (with GPU)
- Key Features and Advantages
  - Cortex-A9 to run open OS or RTOS
  - Cortex-M4 for real-time response, system control / CAN messaging and low-power system monitoring
  - Support for 32-bit LPDDR2 and DDR3/DDR3L up to 400MHz (800MHz DDR)
  - Multiple boot sources include managed NAND, raw NAND, parallel NOR and dual DDR Quad SPI
  - Multimedia:
    - Vivante GC400T GPU supporting 27M Tri/s, 166M Pxl/s OpenGLES 2.x / OpenVG 1.x (6X3 only)
    - Parallel LCD display interface up to WXGA
    - 8-bit CSI via RGMII2
  - Connectivity:
    - USB HS Host + OTG with PHY, USB HSIC for Modem Interface
    - 2x Gb Ethernet with AVB
    - 2x FlexCAN / CAN FD
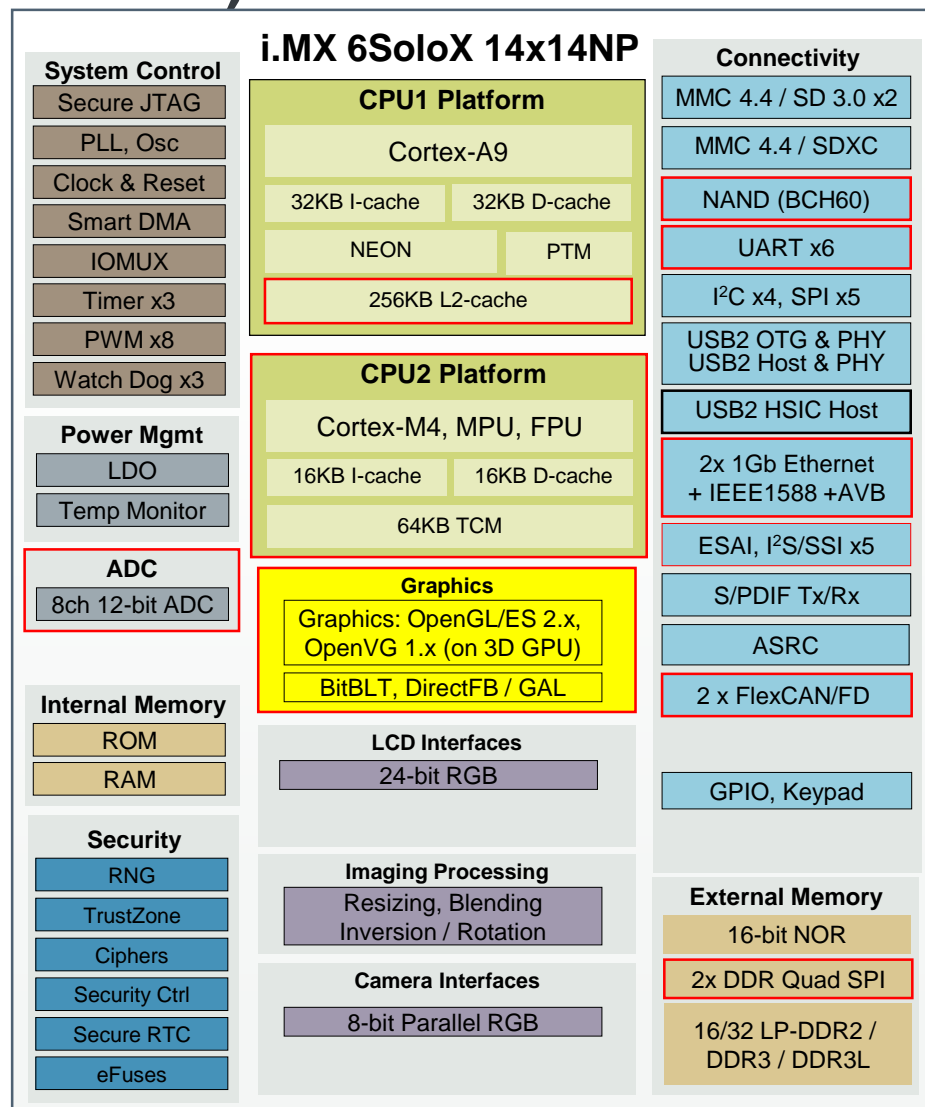   - 1x MLB25/50 (automotive only)
    - 2x 8-ch 12-bit SAR ADC

Qual. Type	Temp. Range	6X1	6X3
Extended Commercial	-20C to +105C	Y	Y
Industrial	-40C to +105C	Y	Y
Automotive	-40C to +125C	Y	n/a

i.MX 6SoloX 17x17NP

System Control
- Secure JTAG
- PLL, Osc
- Clock & Reset
- Smart DMA
- IOMUX
- Timer x3
- PWM x8
- Watch Dog x3

Power Mgmt
- LDO
- Temp Monitor

ADC
- 8ch 12-bit ADC

Internal Memory
- ROM
- RAM

Security
- RNG
- TrustZone
- Ciphers
- Security Ctrl
- Secure RTC
- eFuses

CPU1 Platform
- Cortex-A9
- 32KB I-cache | 32KB D-cache
- NEON | PTM
- 256KB L2-cache

CPU2 Platform
- Cortex-M4, MPU, FPU
- 16KB I-cache | 16KB D-cache
- 64KB TCM

Graphics
- Graphics: OpenGL/ES 2.x, OpenVG 1.x (on 3D GPU)
- BitBLT, DirectFB / GAL

LCD Interfaces
- 24-bit RGB

Imaging Processing
- Resizing, Blending Inversion / Rotation

Camera Interfaces
- 8-bit Parallel RGB

Connectivity
- MMC 4.4 / SD 3.0 x2
- MMC 4.4 / SDXC
- NAND (BCH60)
- UART x6
- I²C x4, SPI x5
- USB2 OTG & PHY USB2 Host & PHY
- USB2 HSIC Host
- 2x 1Gb Ethernet + IEEE1588 +AVB
- ESAI, I²S/SSI x5
- S/PDIF Tx/Rx
- ASRC
- 2 x FlexCAN/FD
- MLB25/50
- GPIO, Keypad

External Memory
- 16-bit NOR
- 2x DDR Quad SPI
- 16/32 LP-DDR2 / DDR3 / DDR3L

□ Updated from i.MX 6Solo ▉ 6X3 only ▉ Auto only

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i.MX 6SoloX 14x14NP (NP = No PCIe)

- Specifications:
  - CPU1: ARM Cortex-A9 at 1GHz
  - CPU2: ARM Cortex-M4 at 200MHz
  - Package: 14x14 VK, 0.65mm pitch MAPBGA
  - Device options: 6X1 (no GPU), 6X3 (with GPU)
- Key Features and Advantages
  - Cortex-A9 to run open OS or RTOS
  - Cortex-M4 for real-time response, system control / CAN messaging and low-power system monitoring
  - Support for 32-bit LPDDR2 and DDR3/DDR3L up to 400MHz (800MHz DDR)
  - Multiple boot sources include managed NAND, raw NAND, parallel NOR and dual DDR Quad SPI
  - Multimedia:
    - Vivante GC400T GPU supporting 27M Tri/s, 166M Pxl/s OpenGLES 2.x / OpenVG 1.x (6X3 only)
    - Parallel LCD display interface up to WXGA
    - 8-bit CSI via RGMII2
  - Connectivity:
    - USB HS Host + OTG with PHY, USB HSIC for Modem Interface
    - 2x Gb Ethernet with AVB
    - 2x FlexCAN / CAN FD
    - 2x 8-ch 12-bit SAR ADC

Qual. Type	Temp. Range	6X1	6X3
Extended Commercial	-20C to +105C	Y	Y

i.MX 6SoloX 14x14NP

System Control
- Secure JTAG
- PLL, Osc
- Clock & Reset
- Smart DMA
- IOMUX
- Timer x3
- PWM x8
- Watch Dog x3

Power Mgmt
- LDO
- Temp Monitor

ADC
- 8ch 12-bit ADC

Internal Memory
- ROM
- RAM

Security
- RNG
- TrustZone
- Ciphers
- Security Ctrl
- Secure RTC
- eFuses

CPU1 Platform
- Cortex-A9
- 32KB I-cache | 32KB D-cache
- NEON | PTM
- 256KB L2-cache

CPU2 Platform
- Cortex-M4, MPU, FPU
- 16KB I-cache | 16KB D-cache
- 64KB TCM

Graphics
- Graphics: OpenGL/ES 2.x, OpenVG 1.x (on 3D GPU)
- BitBLT, DirectFB / GAL

LCD Interfaces
- 24-bit RGB

Imaging Processing
- Resizing, Blending Inversion / Rotation

Camera Interfaces
- 8-bit Parallel RGB

Connectivity
- MMC 4.4 / SD 3.0 x2
- MMC 4.4 / SDXC
- NAND (BCH60)
- UART x6
- I²C x4, SPI x5
- USB2 OTG & PHY USB2 Host & PHY
- USB2 HSIC Host
- 2x 1Gb Ethernet + IEEE1588 +AVB
- ESAI, I²S/SSI x5
- S/PDIF Tx/Rx
- ASRC
- 2 x FlexCAN/FD
- GPIO, Keypad

External Memory
- 16-bit NOR
- 2x DDR Quad SPI
- 16/32 LP-DDR2 / DDR3 / DDR3L

☐ Updated from i.MX 6Solo   ☐ 6X3 only

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When to Choose i.MX 6SoloX vs. i.MX 6Solo/6SoloLite

Feature	i.MX 6SoloLite	i.MX 6SoloX	i.MX 6Solo
CPU1	1GHz Cortex-A9 (2400 DMIPS)	800MHz -1GHz Cortex-A9 (2400 DMIPS)	800MH-1GHz Cortex-A9 (2400 DMIPS)
CPU2	-	**166MHz-200MHz Cortex-M4 (208 DMIPS)**	-
On-chip memory	256KB L2 + **256KB SRAM**	256KB L2 + 128KB SRAM	**512KB L2** + 128KB SRAM
Serial Flash I/F	SPI	**Dual DDR QuadSPI**	SPI
Raw NAND Flash I/F	-	**8-bit NAND BCH60**	**8-bit NAND BCH40**
DRAM interface	32-bit LPDDR2/DDR3 @400MHz	32-bit LPDDR2/DDR3 @400MHz	32-bit LPDDR2/DDR3 @400MHz
Ethernet	1x 10/100	**2x Gb AVB**	1x Gb + 1588
PCIe	-	**1x PCIe 2.0 (x1 lane)** [*n/a on all packages]	**1x PCIe 2.0 (x1 lane)**
USB	1x USB OTG HS w/PHY 1x USB Host HS w/PHY 1x HSIC	1x USB OTG HS w/PHY 1x USB Host HS w/PHY 1x HSIC	1x USB OTG HS w/PHY 1x USB Host HS w/PHY **2x HSIC**
UART, SPI, I2C	5, 4, 4	**6**, 4, 4	5, 4, 4
SD/MMC interface	3x SD/MMC, 1x SDXC	3x SD/MMC, 1x SDXC	3x SD/MMC, 1x SDXC
12-bit ADC	-	**2x 12-bit SAR** [*n/a on all packages]	-
Camera Input	16-bit parallel	**20-bit parallel** [*n/a on all packages] **4x Composite** [*n/a on all packages]	20-bit parallel **1x MIPI CSI**
GPU 2D	**GC320 Composition (600Mpxl/s)** [*n/a on all devices]	via GPU 3D (300Mpxl/s) [*n/a on all devices]	**GC320 Composition (600Mpxl/s)** [*n/a on all devices]
GPU 3D	-	**GC400T Open GLES 2.0** [*n/a on all devices] **27M Tri/s, 133 Mpxl/s**	**GC880 Open GLES 2.0** [*n/a on all devices] **53M Tri/s, 266 Mpxl/s**
Video Decode	via Software	via Software	**1080p30 + D1**
Display interface	1x 24-bit RGB up to WXGA 1x EPDC	1x 24-bit RGB up to WXGA 1x LVDS [*n/a on all packages]	**2x 24-bit RGB up to WXGA** **1x LVDS, HDMI, MIPI DSI, EPDC**
Package	13x13, 0.5P	17 x17, 0.8P or 19x19, 0.8P	21 x 21, 0.8P
Qual. Tiers	Commercial	Commercial, Industrial, Automotive	Commercial, Industrial, Automotive
Availability	Now	Sampling – now (alpha) Production – 4Q14	Now

Multiple Execution Environments

Requisite for Multiple Software Execution Environments

- A growing number of embedded use cases require concurrent execution of <u>isolated</u> software environments within the system

- Motivation for multiple software execution environments:
  - Real-time performance
  - Power consumption
  - Fast boot
  - System integrity
  - System security
  - Leverage hardened or certified software solutions
  - Reuse of legacy software

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Multiple Execution Environments – Automotive Use Case

- Use case details:
  - Automotive infotainment unit
  - Based on rich OS
  - Connected to vehicle bus (CAN)
  - Connected to rear camera

Environment Requirement	Use Case Details
Fast boot	CAN bus response Activation of rear-view camera
System security	CAN bus access separated from rich OS
Leverage hardened/certified solutions	Certified CAN stack running in AUTOSAR-compliant environment
System integrity	Critical driver notifications available regardless of rich OS state

Multiple Execution Environments – Industrial Use Case

- Use case details:
  - Industrial control system
  - Rich OS for user interface
  - Battery power or constrained power supply

Environment Requirement	Use Case Details
Real-time performance	Connected to sensors/controls that require real-time response
Power consumption	Majority of active time spent aggregating data from sensors
Reuse of legacy software	Reuse legacy software from standalone MCU

Multiple Execution Environments – Consumer Use Case

- Use case details:
  - Portable consumer device
  - Based on rich OS
  - Battery power
  - Low-power Bluetooth low energy (BLE) connection

Environment Requirement	Use Case Details
Leverage certified solutions	Leverage BLE solution certified on standalone MCU
Power consumption	Majority of active time spent maintaining BLE connection and monitoring sensors

Multiple Execution Environment Solutions

Solution	Pros	Cons
Multi-chip System MCU/MPU connected to separate MCU	• Strict separation between execution environments	• Increased BOM • Cannot directly share resources between chips • Potential for high IPC overhead • Complicates power management
Virtualization	• No need for additional MCU • Allows more software environments than MCUs • Dynamic allocation of CPU bandwidth between software environments	• Performance impact • Real-time impact • Power impact • Para-virtualization requires significant software • Full virtualization requires significant hardware
Heterogeneous Multiprocessing (HMP)	• SoC resources can be efficiently shared and repurposed for new use cases • Integrated MCU reduces BOM • Potential to improve energy efficiency • Efficient interprocessor communication	• Shared resources require isolation/protection mechanisms or design changes to support multiple concurrent interfaces

i.MX HMP Architecture

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Heterogeneous Multiprocessing

- i.MX 6SoloX HMP Hardware Support
  - Shared Bus Topology
  - Resource Domain Controller (RDC)
  - Message Unit (MU)
  - SEMA4
  - Shared Memory
  - Exclusive Access Instructions
- Solution: Multi-Core Communication (MCC) Library

HMP Challenges – Synchronization and Communication

- Interprocessor Synchronization
  - Access to shared memory and peripherals must be synchronized
  - Development of cooperative software is more challenging than SMP systems due to separate development environments
  - Hardware support needed to enforce the development of cooperative software

- Interprocessor Communication
  - Robust and efficient interprocessor communication is needed

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HMP Challenges – Resource Partitioning and Protection

- Split bus topology
  - Provides immutable isolation of resources
  - Lacks flexibility to repartition the resources to adapt to new use cases
  - Resources such as memory may need to be duplicated

- Shared bus topology
  - Provides flexibility to repartition the resources for new use cases
  - Memory partitioning necessary to specify shared and isolated regions
  - Potential issues with isolation and protection of resources

Split Topology

Core0	Core1
Bus Fabric	Bus Fabric
Slave Device	Slave Device

Shared Topology

Core0	Core1
Bus Fabric	
Slave Device	Slave Device

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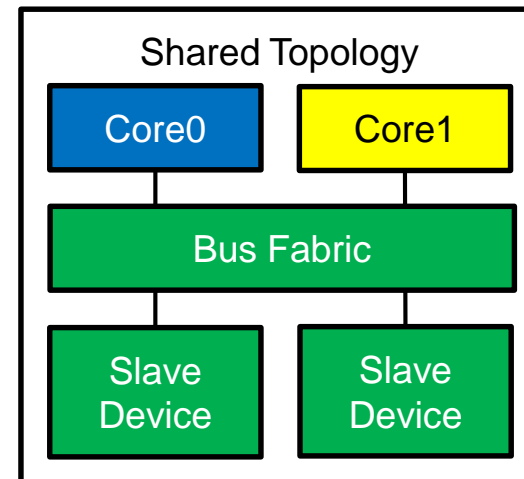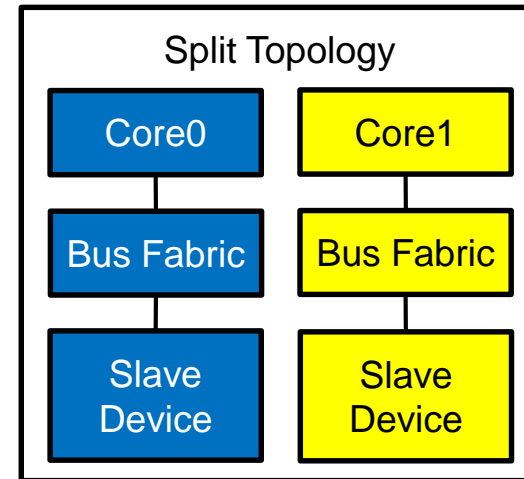
Resource Domains

- Use *resource domains* to partition the system
  - Masters are assigned to a resource domain
  - Slave access permissions are defined per resource domain
  - Memory region access permissions are defined per resource domain
- Sideband signals of bus fabrics carry resource domain ID
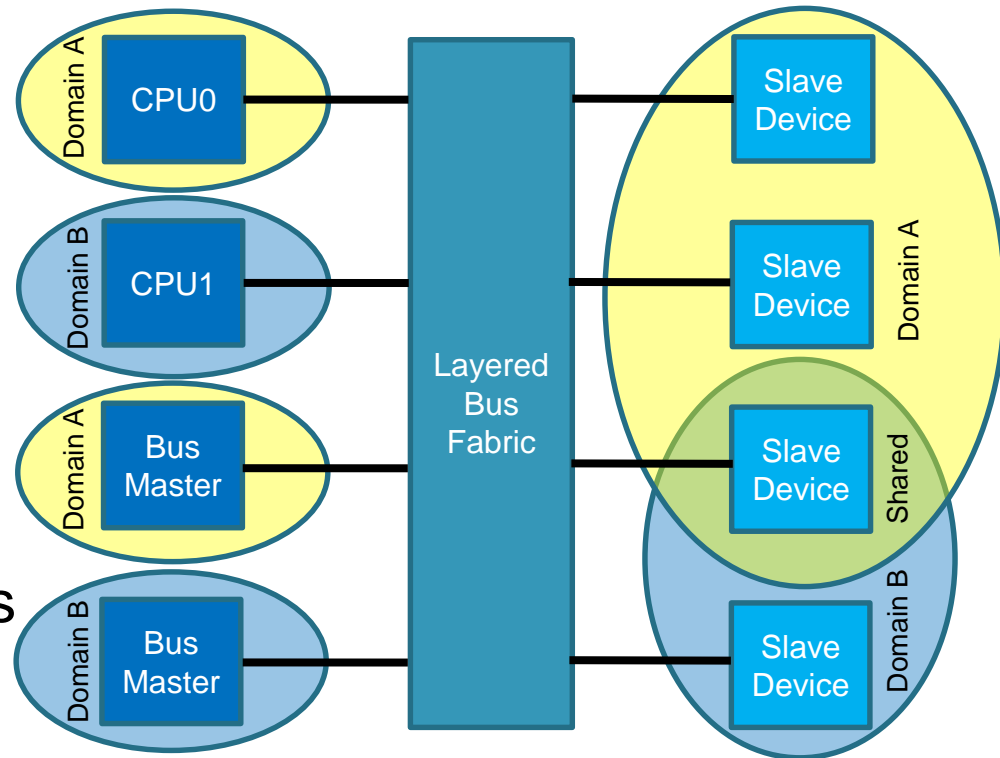
Resource Domain Controller (RDC)

- Resource Domain Controller (RDC) is a new module integrated into next-gen i.MX devices

- RDC provides a centralized programming model to configure isolation and sharing of system resources

- **Key RDC features:**
  - Assignment of master resources (CPUs and bus mastering peripherals) to a *resource domain*

  - Configuration of read/write access for slave peripherals based on *resource domain*

  - Partitioning of memory into regions that can have separate domain access controls

  - Configuration of read/write access for memory regions based on *resource domain*

  - Integral semaphore hardware enables cooperative software to safely access peripherals with access by multiple domains

  - Optional enforcement of semaphore usage to reject accesses by master resources that have not obtained the semaphore lock
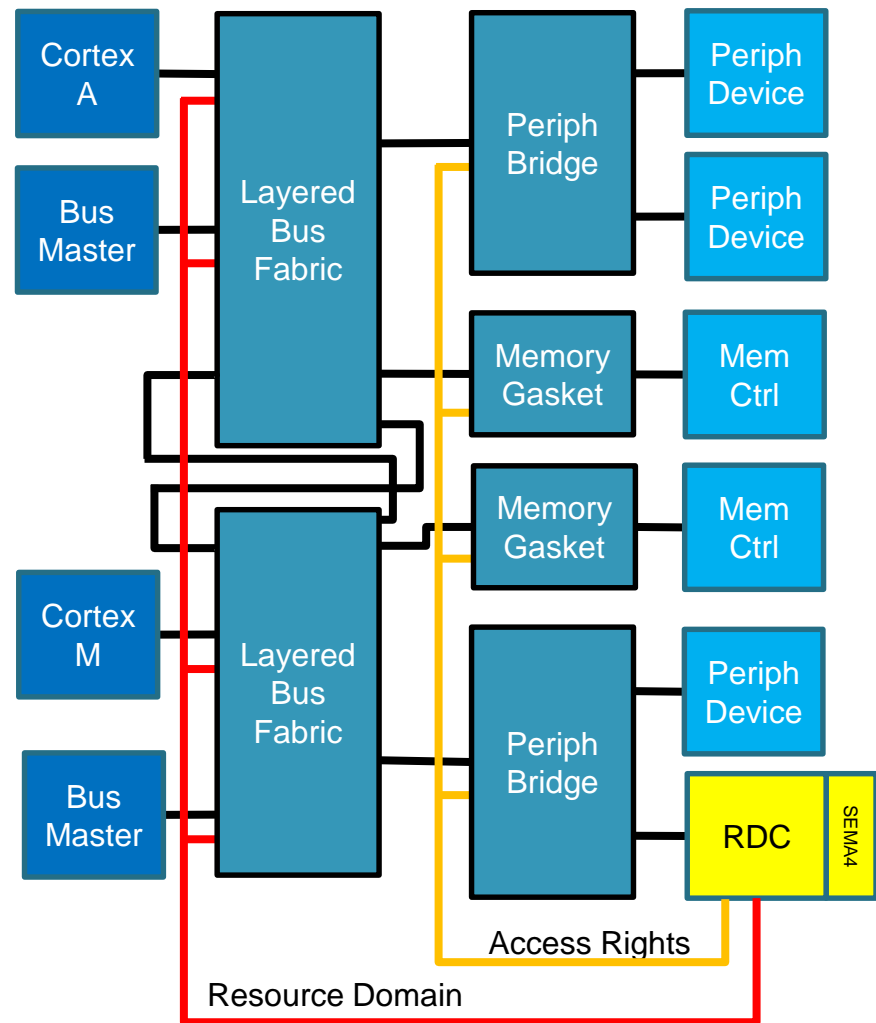
Memory Region Mapping

- Access permission are prioritized for overlapping regions. Lower order entries in the memory region table have precedence.

Memory/Port	Number of Regions	Region Resolution
MMCD	8	4 KB
QSPI	8	4 KB
WEIM	8	4 KB
PCIe	8	4 KB
OCRAM	5	32 B
OCRAM_S	5	32 B
OCRAM_L2	5	32 B

RDC Initialization

- RDC should be isolated to ensure that only a trustworthy master resource can configure the registers

- Recommended options for initialization of RDC:
    - Configure RDC during secure boot and lock configuration registers from further modification
    - Configure the RDC to accessible only from CA9 and use CSU to further restrict access to secure supervisor software (TrustZone)
    - Configure the RDC to be accessible only from trustworthy domain and use CSU to further restrict access to supervisor software

IPC Hardware Summary

Hardware	Features
Messaging Unit (MU)	Mailbox registers to send/receive messages Provided interprocessor interrupts
SEMA4	Hardware-based general-purpose semaphore module
Shared Memory	Bus topology allows shared memory RDC and CSU can provide memory protection/isolation
Exclusive Access	ARMv7-A and ARMv7-M defines exclusive access instructions (LDREX/STREX)

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Messaging Unit (MU)

- Proven IP from cellular baseband SoCs
- Messaging control by interrupts or polling
- 4 RX/TX registers on each side
- 12 interrupt requests (IRQs) per side
  - 4 RX register full IRQs
  - 4 TX register empty IRQs
  - 4 general-purpose IRQs
- 3 general-purpose flags per side

Processor A

Messaging Unit (MU)

Processor A side

TX / RX Registers

Status and Control Registers

Sync and Control Registers

Generate Interrupts

Processor B side

TX / RX Registers

Status and Control Registers

Sync and Control Registers

Generate Interrupts

Processor B

Processor A Peripheral Bus

Processor B Peripheral Bus

Interrupts to Processor A interrupt controller

Interrupts to Processor B interrupt controller

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Semaphore (SEMA4)

- Provides a hardware mechanism for cooperative software to safely share resources in HMP systems
- Module reused from Vybrid and Freescale automotive MCUs
- Separate module from RDC semaphore
- Supports 16 general-purpose hardware semaphores
- Semaphore can only be unlocked by locking processor
- Optional interrupt notification after failed lock attempt to indicate when semaphore is unlocked
- Software conventions still required to ensure only processor with semaphore lock can access shared resources

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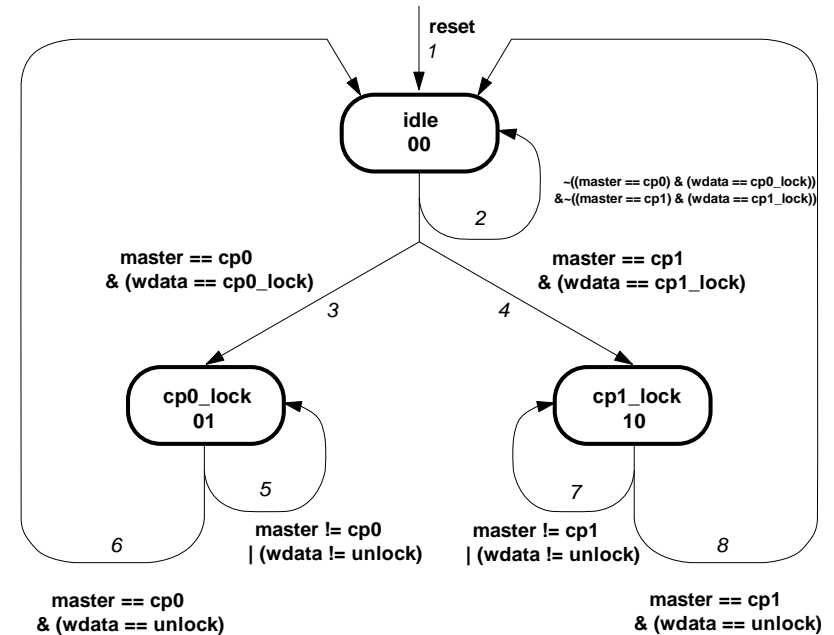
Shared Memory

- Shared bus topology allows sharing of internal/external memories
- RDC hardware can be used to partition each memory individually and restrict access based on resource domain

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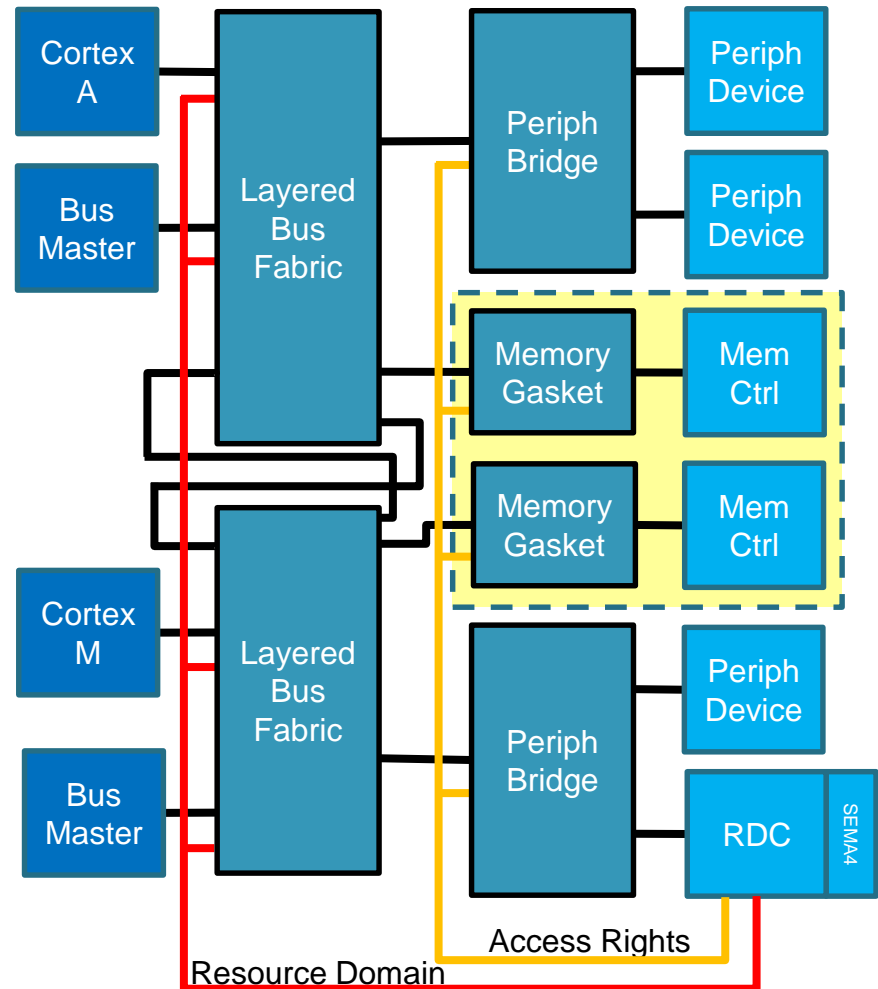
Exclusive Access

- Cortex-A (ARMv7-A) and Cortex-M (ARMv7-M) support exclusive access instructions (LDREX/STREX).

- Exclusive access bus signals generated by the CPUs are connected to monitors in the memory gaskets to support load/store exclusive instructions.

- Exclusive access is widely used for synchronization in SMP systems, but is applicable to HMP systems that have architectural support.

- For HMP systems, the memory referenced during exclusive accesses must be configured such that the access will occur at the *point of coherency* for the CPUs.

Power Domain Partitioning

- System resources are partitioned into multiple power domains
- Power domains with unused resources can be powered down under software control to save leakage
- Cortex-M and low-power peripherals are located in a separate low-leakage domain to enable low-power processing

High-Power CPU Domain

High-Power Peripheral Domain

Low-Power CPU and Peripheral Domain

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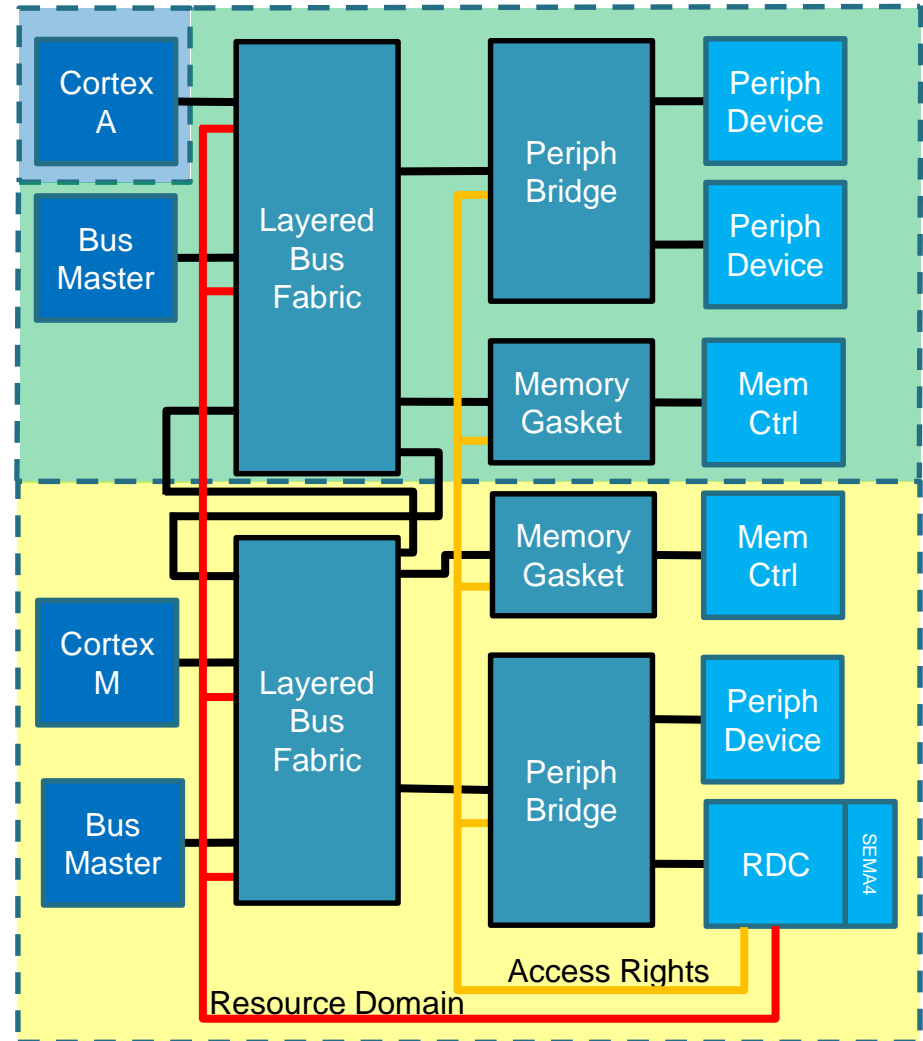
Cortex-M4 Enables New Low Power Modes

Low Power Modes*

- ■ Cortex-M4=Off
- ■ Cortex-M4=4MHz
- ■ Cortex-M4=24MHz
- ■ Cortex-M4=Max
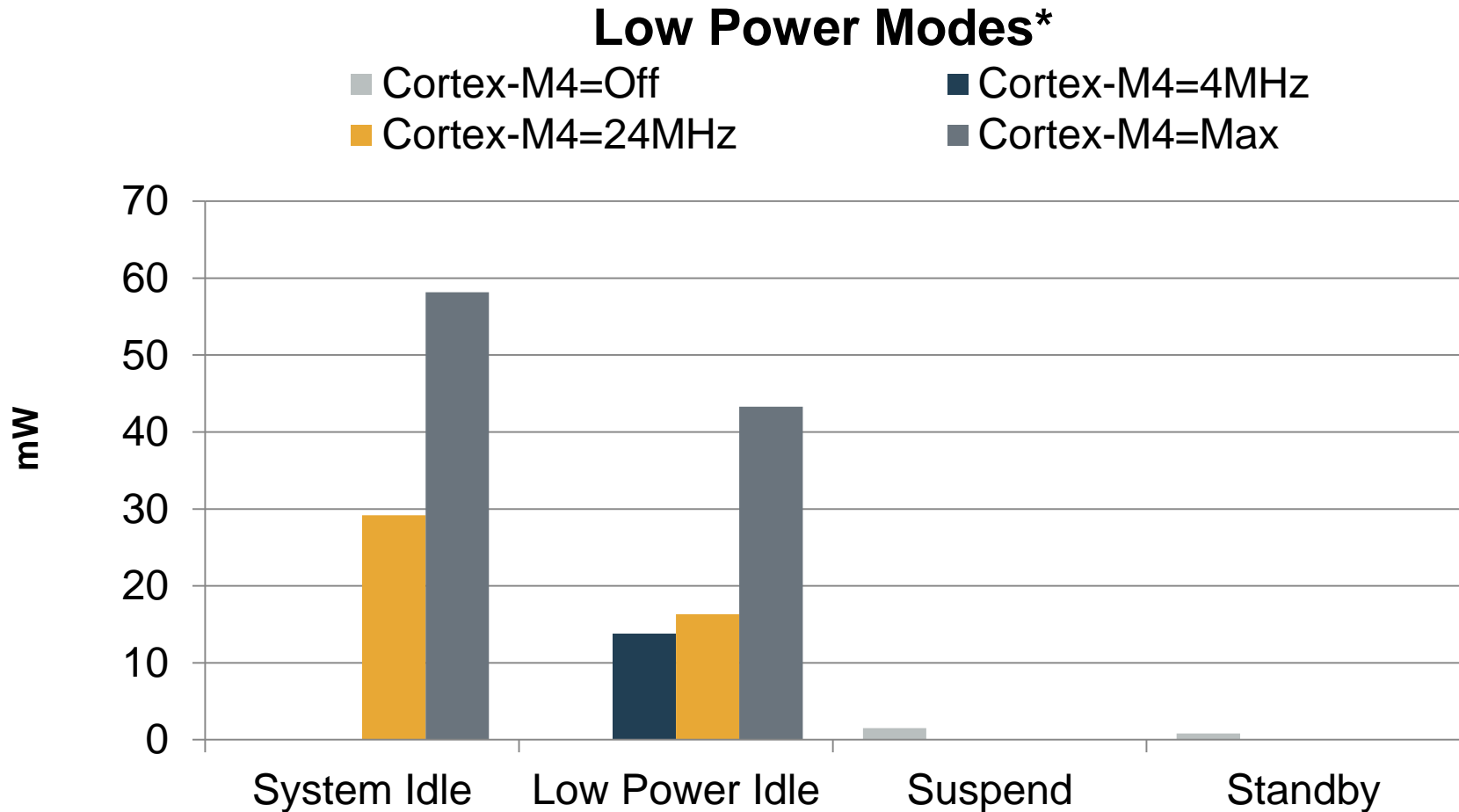
* Cortex-A9 is power gated in all low-power modes, Cortex-M4 is available for low-level processing

Summary of i.MX HMP Features

Feature	HMP Benefits
Integration of Cortex-A and Cortex-M processors	• Execute rich OS on Cortex-A and real-time software on Cortex-M • Cortex-M enhances low-power capability • Use Cortex-M to increase system integrity and security • Leverage proven Cortex-M software solutions
Shared Bus Topology	• Efficient use of system resources • Flexibility to adapt to new use cases
Resource Domain Controller	• Allows software to partition peripherals and memories into resource domains with assignable access permissions • Integrated hardware semaphore facilitates safe sharing of peripherals
Messaging Unit (MU)	Flexible interprocessor communication
Hardware Semaphore (SEMA4)	HMP synchronization to shared resources
Shared Memory	Efficient interprocessor communication
Power Domain Partitioning	Flexibility to enable low-power processing

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ARM Platform and Debug

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ARM Cortex M4 Platform

- CPU Complex:
  - Cortex-M4 processor @227 MHz, 208DMPIS
  - Single Precision FPU
  - MPU (Memory Protection Unit)
  - Supports 128 Interrupts
- Cache
  - 16KB I-Cache
  - 16KB D-Cache
  - 64KB TCM
  - Single cycle access
- TCM
  - 32KB TCM on system bus
  - 32KB TCM on code bus
  - Single cycle access
  - Can be initialized by A9 through its backdoor port.

Cortex M4 Platform

NVIC	CM4 CPU	FPU
FPB		DWT
AP	Bus Martix	ITM

SystemBus   CodeBus

RAM Array — TCMU — TCML — RAM Array

Data/Tag Array — SYS-$ — CODE-$ — Data/Tag Array

SysBIU CodeBIU

64-bit AHB System Bus   64-bit AHB Code Bus   Backdoor Port

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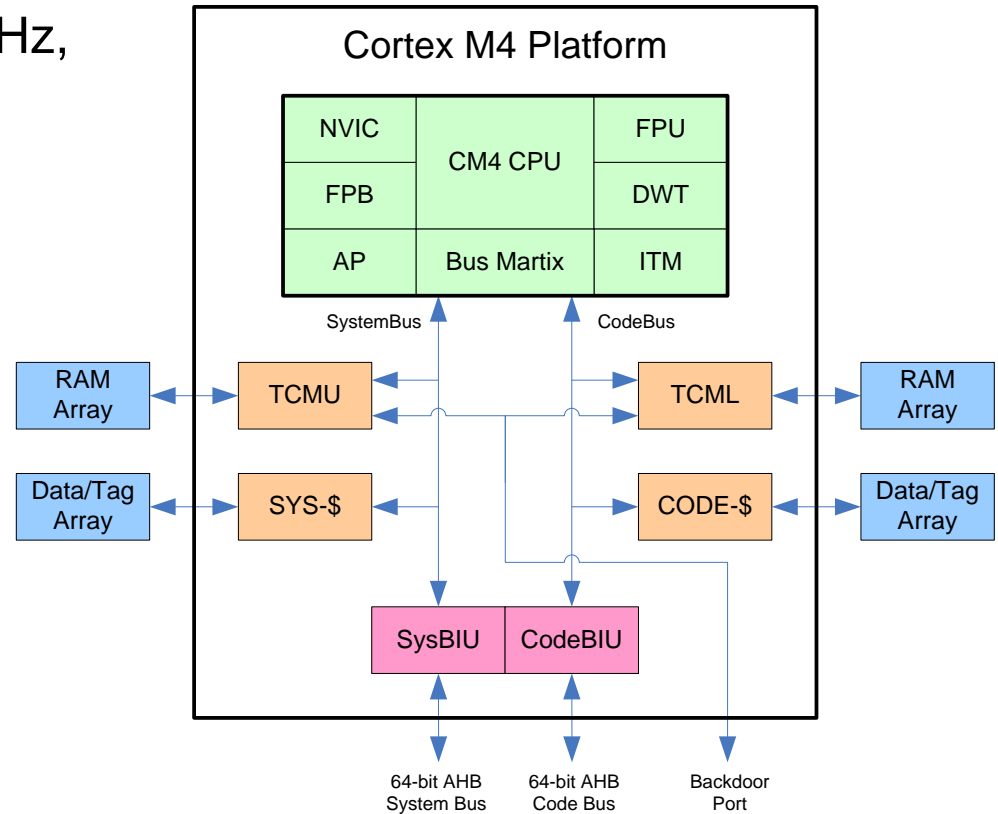
Debug Scheme

- Both A9 core and M4 core have their own DAP, all the resources in its platform will be accessed through its own DAP; (only CPU core is shown in the diagram below)

- Recommended toolchain is ARM DS-5

- JTAG Chain Configuration:
  - SJC, IR Length = 5, same as i.MX 6Solo;
  - SDMA, IR Length = 5, same as i.MX 6Solo;
  - DAP for A9, IR Length = 4, same as i.MX 6Solo;
  - DAP for M4, IR Length = 4, new in i.MX 6SoloX.

Memory

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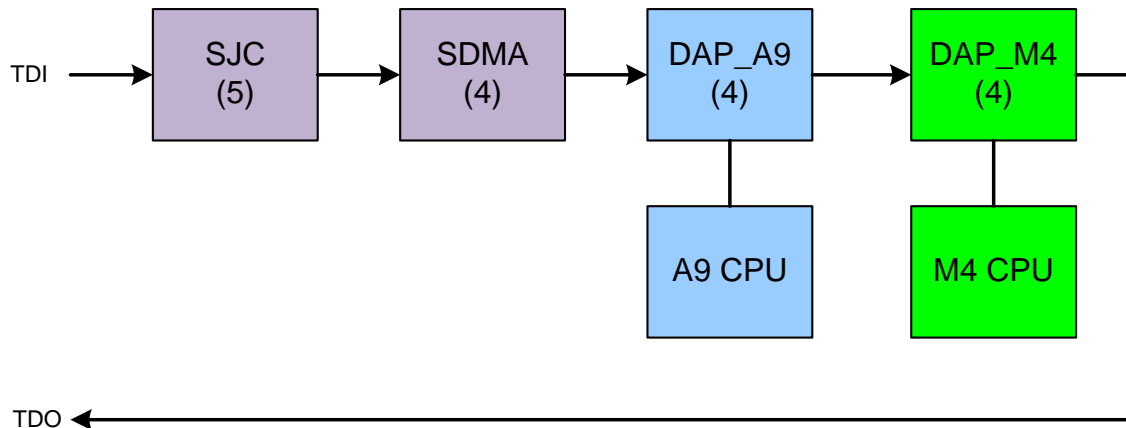
Internal Memory

- ROM 96KB
  - Used to store the boot ROM, including code for boot device support, HAB, etc;
- OCRAM 128KB
  - General purpose On-Chip RAM, has the shortest CPU access latency among all the internal memories;
- OCRAM_S 16KB
  - Smaller On-Chip RAM in always-on domain;
  - Mainly used by software to retain system state during low power mode;
- Secure RAM 32KB
  - 8x 4K RAM in CAAM module, used to store security information;
- TCM 64KB
  - Tight-Coupled Memory in ARM Cortex M4 platform;
  - Can be used as general purpose memory when M4 is not used;
- OCRAM_L2 256KB
  - L2 Cache memory in A9 platform, can be access as normal OCRAM;
  - The switching between L2 Cache Mode / OCRAM Mode is configured by a register in IOMUXC_GPR;
  - Boot ROM supports a boot option to use OCRAM_L2 as OCRAM to hold entire boot image.

All the internal memory can be accessed by both A9 CPU and M4 CPU. In some low power modes, while OCRAM and Secure RAM will be powered down, the OCRAM_L2, OCRAM_S and TCM will be able to retain their state.

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External Memory Interface

- DRAM
  - 32-bit / 16-bit DDR3/LPDDR2 @400MHz
- RawNAND
  - 8-bit NAND FLASH, up to 4 devices supported by 4 chip-selects and 1 ganged ready/busy;
  - ONFI 2.x complaint, synchronous clock rate of up to 100 MHz with data rate of up to 200 MB/s;
  - Support ONFI NAND for Micron and Hynix and Toggle NAND for Toshiba and Samsung.
  - BCH62 for ECC, up to 200MB/s.
- SD/eMMC x4
  - Conforms to the SD Host Controller Standard Specification version 3.0;
  - Compatible with the MMC System Specification version 4.4;
  - Card bus clock frequency up to 208 MHz;
  - Up to 4 controllers supported;
- Parallel NOR FLASH/SRAM
  - Support 8-bit/16-bit parallel NOR FLASH/SRAM;
  - Support both async mode and sync mode access;
- QSPI NOR FLASH
  - Supports industry Standard Single, Dual and Quad mode serial flashes;
  - Supports Double Data Rate (DDR) serial flash for high performance;
  - Maximum serial clock frequency 100MHz SDR Mode, 50MHz DDR Mode;
  - Dual channel architecture enables simultaneous access to two external flashes;
  - Two QSPI controllers are supported, both of them with dual channel capability

Multimedia

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3D & 2D Graphics – GC400T

- Single GPU with 2D & 3D capability
  - OpenGL ES 2.0 compliance, including extensions; OpenGL ES1.1; OpenVG1.1
  - IEEE 32-bit floating-point pipeline
  - Ultra-threaded, unified vertex and fragments shaders
  - BitBlt and StretchBlt
  - DirectFB hardware acceleration
  - ROP2, ROP3, ROP4 full alpha blending and transparency
  - Alpha blending includes Java 2 Porter-Duff compositing rules
  - 90, 180, 270 rotation on every primitive
  - YUV-to-RGB color space conversion
- Supported API
  - OpenGL ES 2.0
  - OpenGL ES 1.1
  - OpenVG 1.1
  - DirectFB
  - GDI/DirectDraw
- Performance Target
  - 3D: 17 MTri/s
  - 3D: 165 MPixel/s
  - 3D: 2.3 GFlops/s
  - 2D Fillrate: 200MPixel/s


Ultra-threaded Unified Shader

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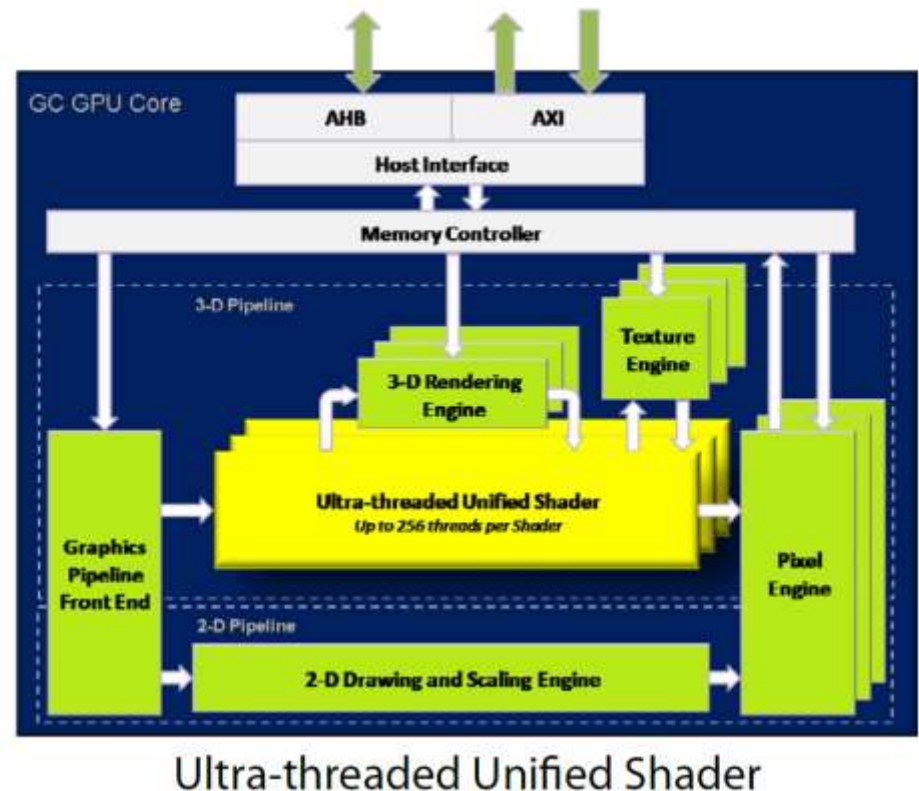
At A Glance: i.MX6 Dual / Solo, i.MX6 SoloX

	i.MX Dual/Solo	i.MX SoloX	Notes
3D GPU	GC 880	GC 400T	400T Can support 3D and 2D contexts simultaneously.
2D GPU	GC 320	(GC400T)	2 Layer 2D HW Composition Engine
Vector Graphics	GC 355	N/A	Full OpenVG Compliant (Font Rendering / SVG Accelerator.)
Video	1080p30FPS	None	Support up to H.264 / VP8 single stream
OpenCL	N/A	N/A	OpenCL support on A9 only w/ NEON

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Pixel Pipeline (PXP)
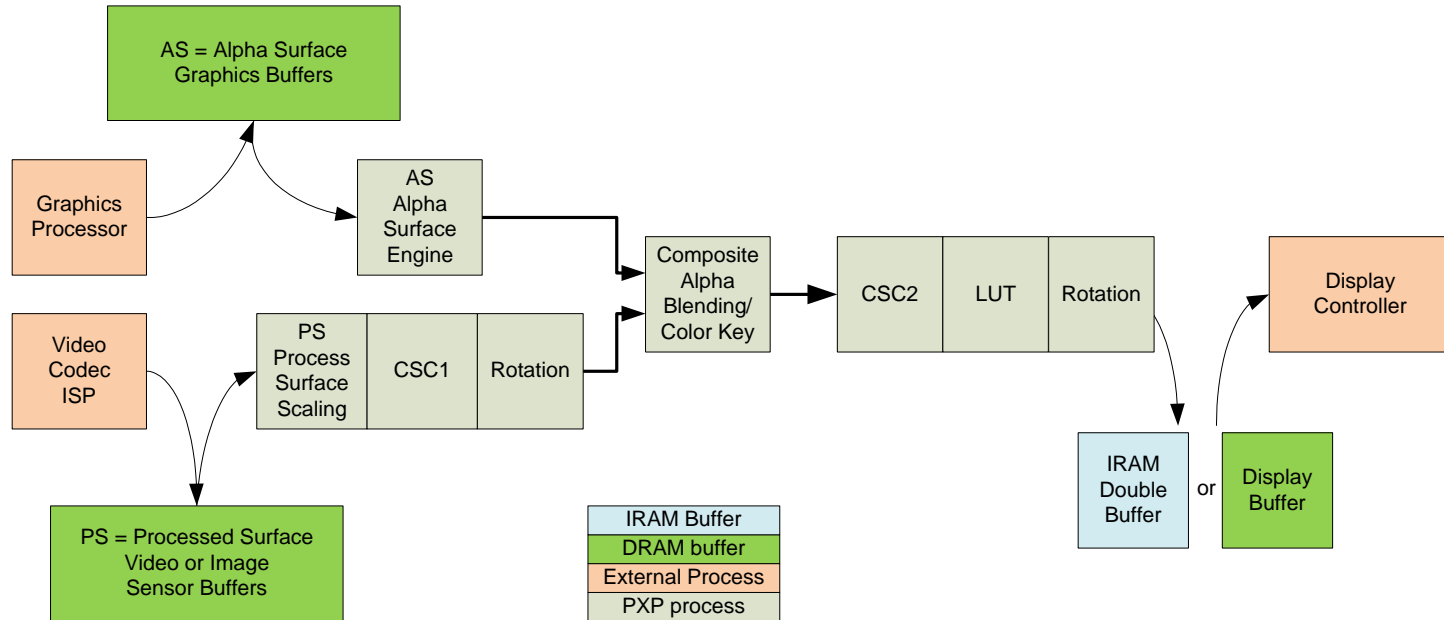
- High-efficiency image processing engine for video/display:
  - RGB/YUV scaling with bilinear filter;
  - 2-layer composite, support both global/embedded alpha, color key;
  - Color space conversion from YUV to RGB or RGB to YUV;
  - Single-pass processing for Resize, CSC, Overlay and Rotation;
  - Up to 200MPixel/s processing speed.
  - Support data pipeline mode with LCDIF to for DRAM bandwidth saving;

Camera & Display Interfaces
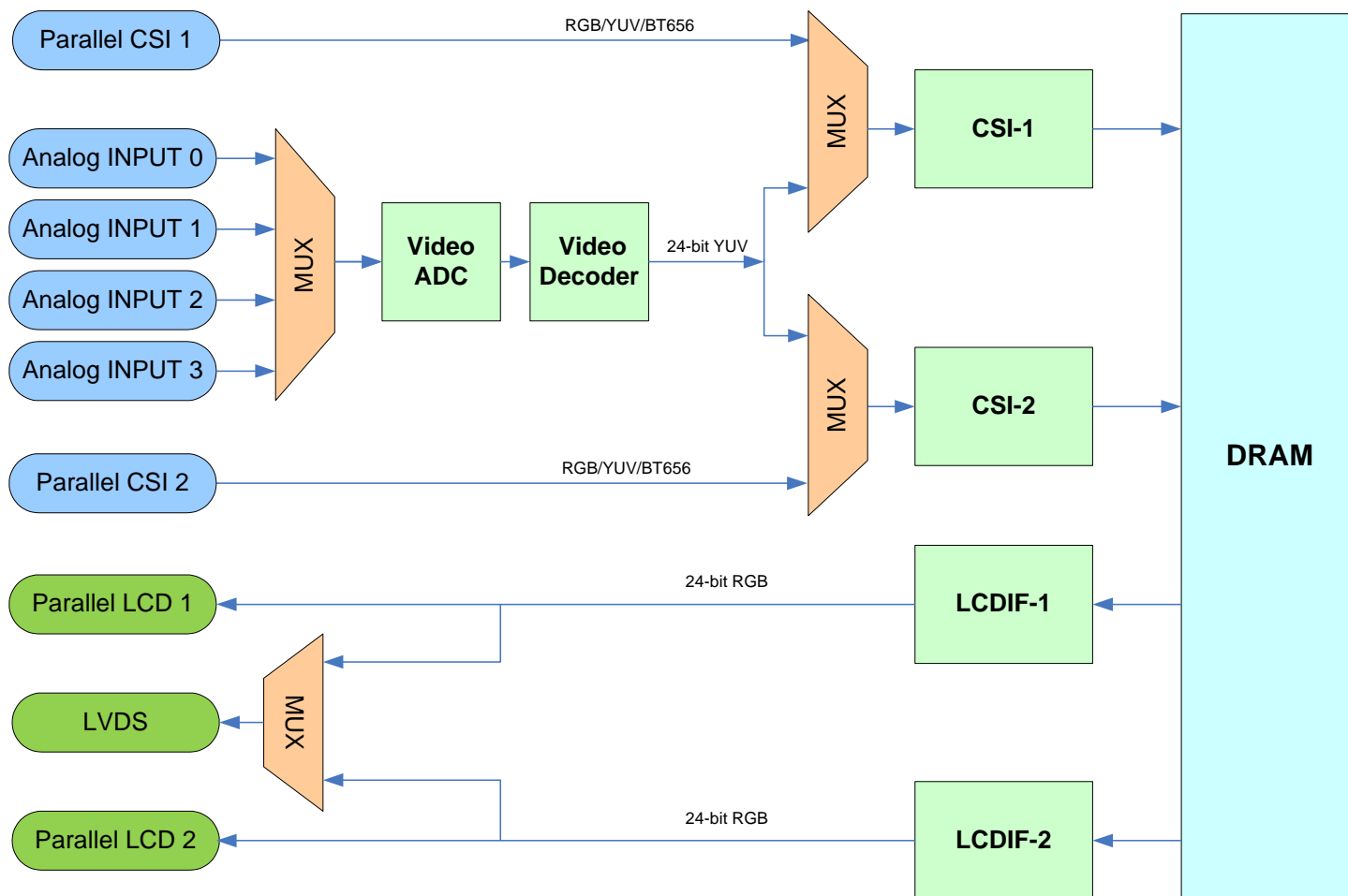
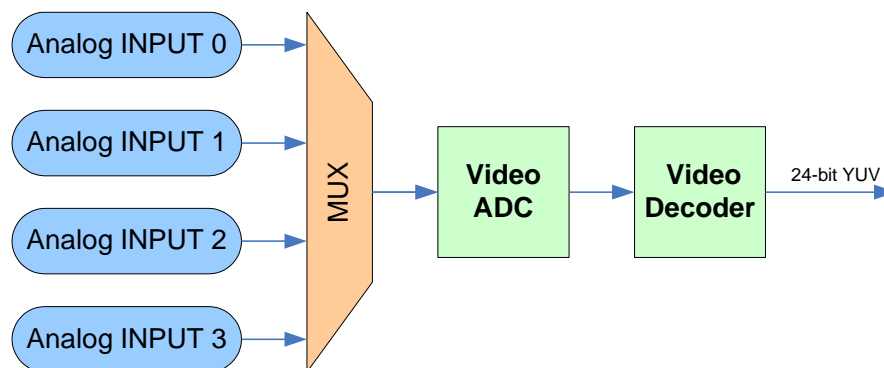* Total number of parallel CSI & parallel LCD are limited by the PINMUX
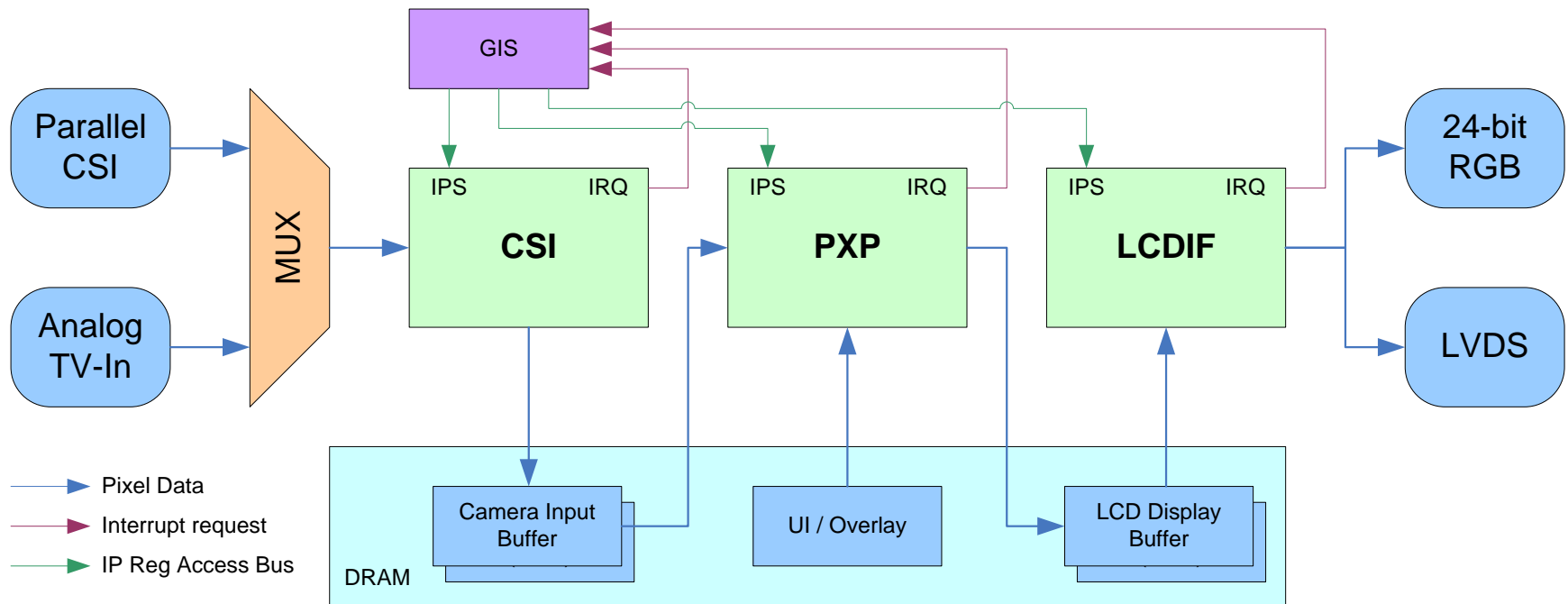
Video ADC and Video Decoder

- Video ADC
  - Support 4 CVBS analog TV input, one of them can be selected as the input source to the system;
  - Digitizes an analog video signal such as from an inexpensive analog camera
  - Internal voltage and current reference generator
  - 10-bit resolution (8 bit ENOB at 60 Msps)
  - Programmable anti-aliasing filter, gain, and clamp

- Video Decoder
  - Support both NTSC and PAL standards
  - Automatic standards detection
  - 2D adaptive comb filter
  - Luma passband is flat to >6MHz
  - Generate output in YUV 24-bit to CSI

| Analog INPUT 0 |
| Analog INPUT 1 | → | MUX | → | **Video ADC** | → | **Video Decoder** | → 24-bit YUV |
| Analog INPUT 2 |
| Analog INPUT 3 |

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Data Flow for Rearview Camera

- **CSI:** Camera input interface, receive input from digital CSI interface or analog TV-in, save the pixel data into DRAM.
- **PXP:** Pixel processing engine, support CSC/resize/overlay, read camera input buffer and generate frame buffer for LCD display.
- **LCDIF:** LCD interface, read frame buffer from DRAM and drive to 24-bit RGB interface or LVDS interface.
- **GIS:** General interrupt service module, manage frame buffer pointer for CSI/PXP/LCDIF based on the interrupt request signals.

- No CPU interrupt service is required, can be enabled before OS boot to meet fast rearview camera display requirement;
- PXP can read another UI / Overlay buffer and do alpha blending with the input to add graphics and text messages on the camera image.

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Data Flow for Video Pass Through
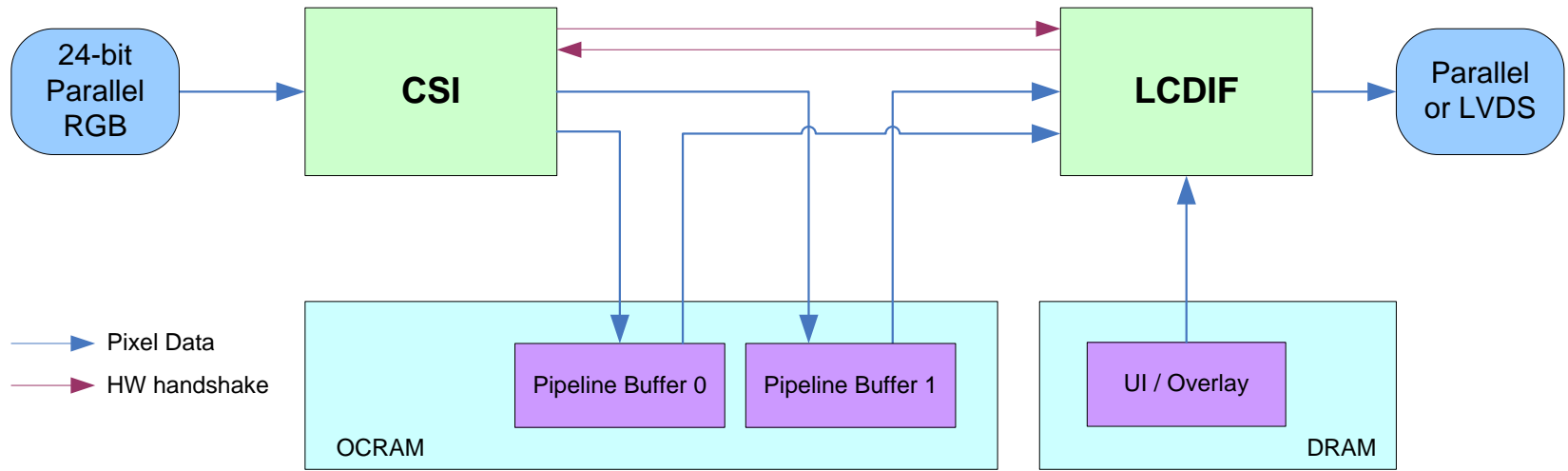
- Support 24-bit RGB parallel input from CSI interface
- Support 24-bit RGB parallel interface or LVDS interface
- No CPU interrupt service is required, fully HW handshake between CSI and LCDIF
- Use double pipeline buffer inside On-Chip RAM, no DRAM bandwidth cost
- Each pipeline buffer is only 8-line, the delay from input to output is only 8 lines time
- LCDIF can read another UI/Overlay buffer from DRAM, and do real-time alpha blending with the RGB input, both local alpha and global alpha are supported.

- Pipeline Buffer Size in OCRAM:
  - WVGA (800x480) = 50KB
  - WXGA (1280x768) = 80 KB

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Data Flow for Video Pass Through with Rearview Camera
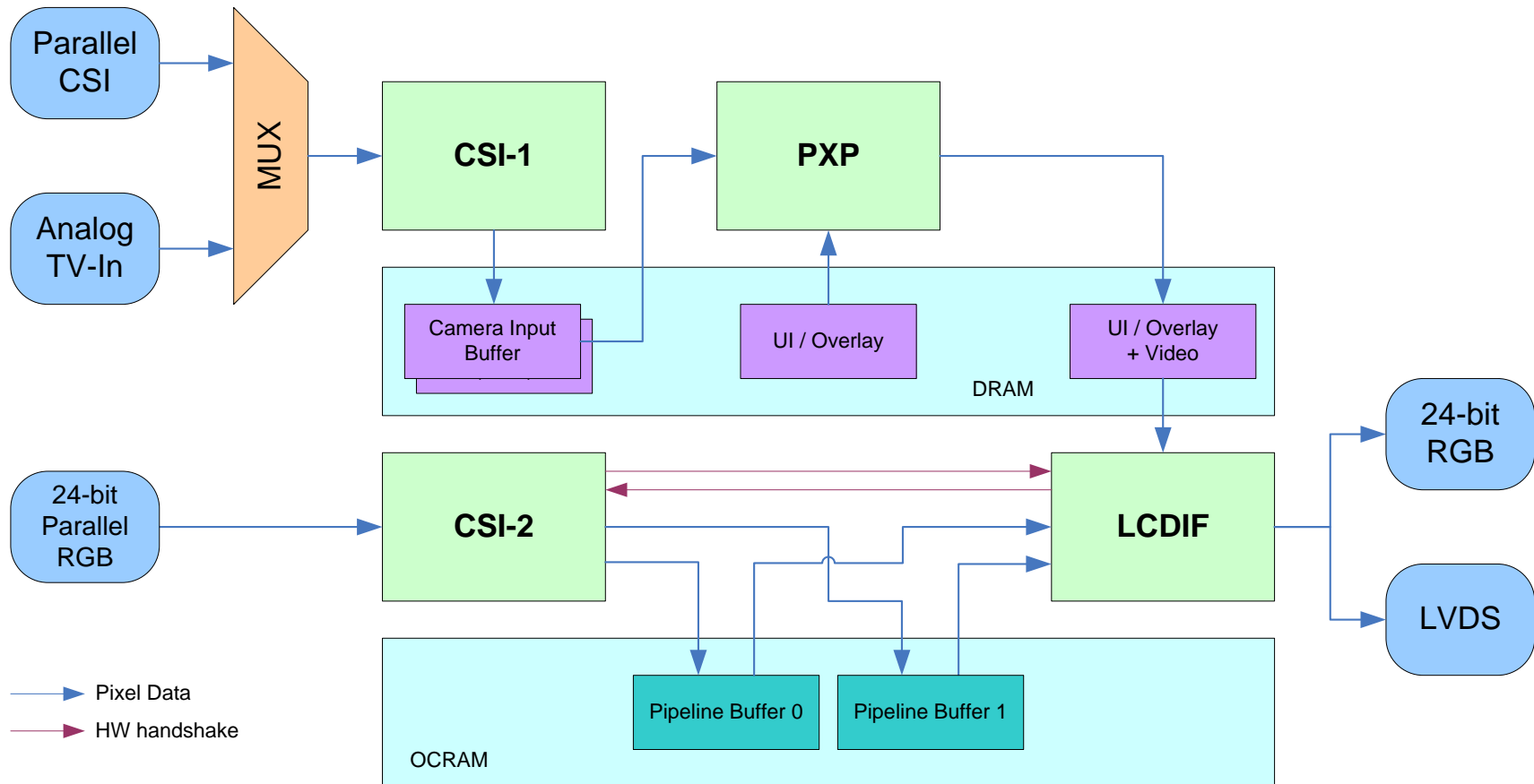
- Support video pass through function and rearview function simultaneously with two CSI input;
- Support combination of three layers, including camera in, video pass through input, and UI / overlay;
- No additional delay added compared to simple video pass through without camera;
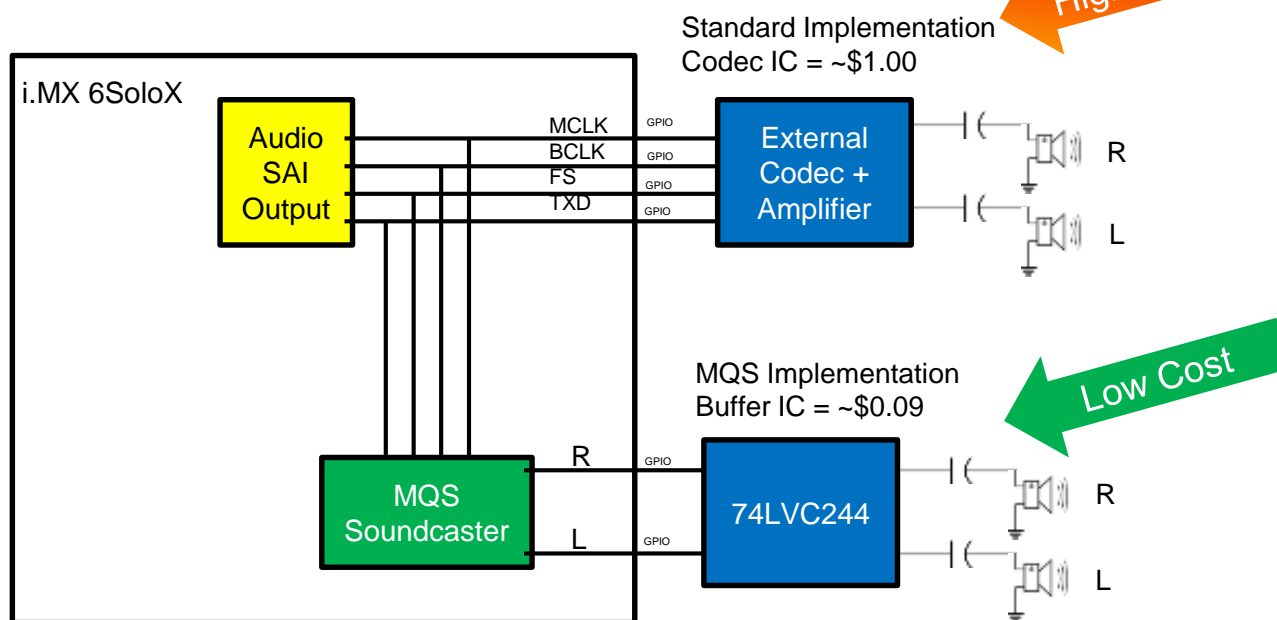
Audio Subsystem: Alignment with i.MX 6Solo

- i.MX 6SoloX retains the existing audio processing and connectivity capabilities available in the i.MX 6Solo family including:
  - 3x Synchronous Serial Interface (SSI) for I2S
  - 1x Enhanced Serial Audio Interface (ESAI) for multichannel audio
  - 1x Sony/Philips Digital Interface (SPDIF)
  - 1x Asynchronous Sample Rate Converter (ASRC)
  - 1x Digital Audio Multiplexer (AUDMUX)

- Module alignment allows portable audio driver code across the i.MX 6 series
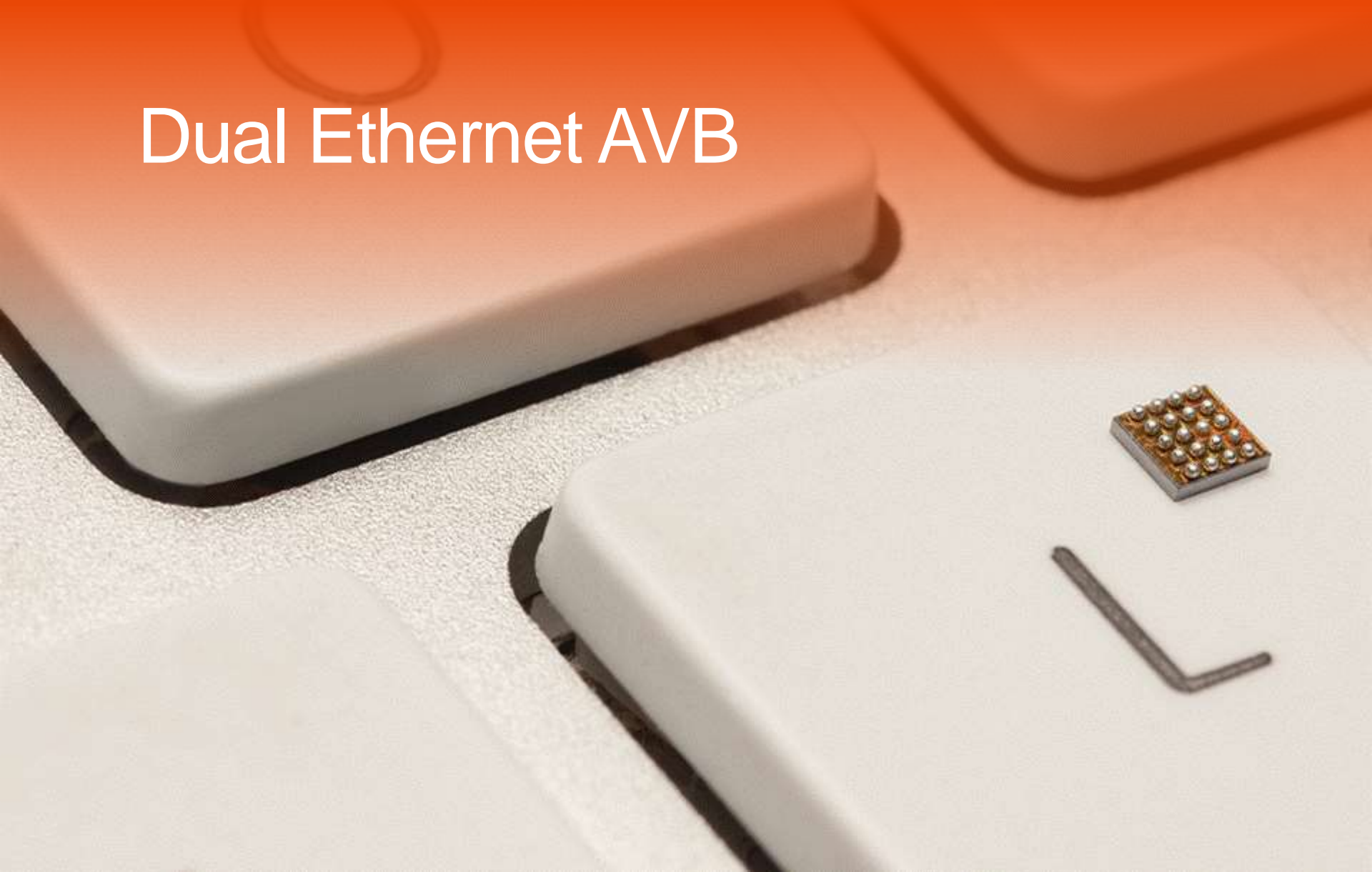
Audio Subsystem: New Features - SAI

- i.MX 6SoloX retains the existing audio processing and connectivity capabilities available in the i.MX 6Solo family including:
  - 3x Synchronous Serial Interface (SSI) for I2S
  - 1x Enhanced Serial Audio Interface (ESAI) for multichannel audio
  - 1x Sony/Philips Digital Interface (SPDIF)
  - 1x Asynchronous Sample Rate Converter (ASRC)
  - 1x Digital Audio Multiplexer (AUDMUX)

- Module alignment allows portable audio driver code across the i.MX 6 series

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Audio Subsystem: New Features - MQS

- MQS (Medium Quality Sound) module added
    - Hardware module converts I2S to PWM
    - No software overhead – completely hardware controlled
    - External buffer+capacitor converts PWM data to audio
    - Audio quality between tape and CD
    - Inexpensive solution for applications that require good-quality audio.
    - Can also drive some piezo speakers directly (without the external buffer) to provide greeting card quality sound

Standard Implementation
Codec IC = ~$1.00

High Fidelity

MQS Implementation
Buffer IC = ~$0.09

Low Cost

i.MX 6SoloX

Audio SAI Output

MCLK   GPIO
BCLK   GPIO
FS   GPIO
TXD   GPIO

External Codec + Amplifier

R
L

MQS Soundcaster
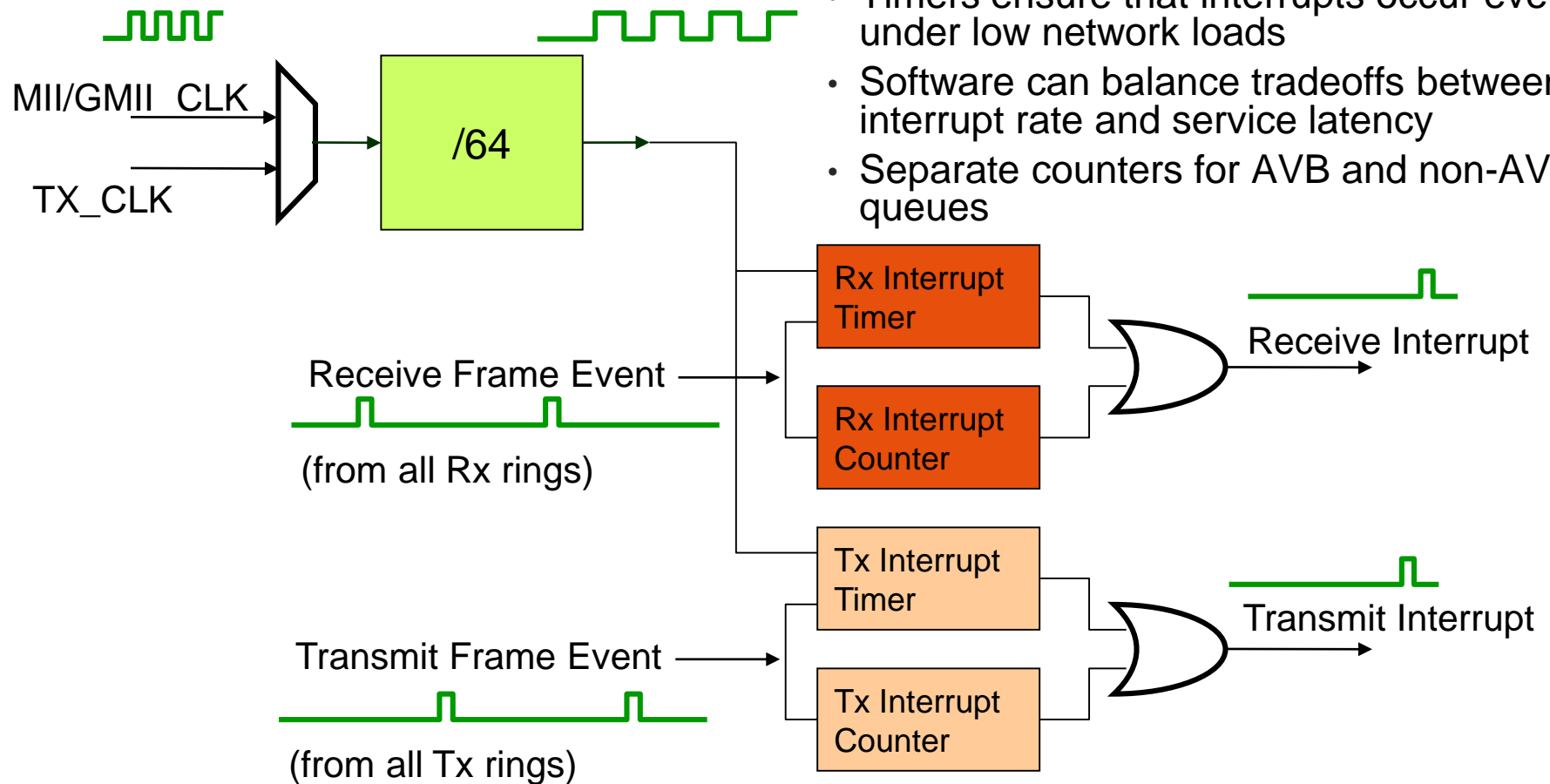
R   GPIO
L   GPIO

74LVC244

R
L

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Dual Ethernet AVB

Ethernet Feature Comparison

Feature	i.MX 6D/Q/DL/S	i.MX 6SoloX
General	1x 10/100/1000 Ethernet Controller	2x 10/100/1000 Ethernet Controllers
Bus Interface	Single 32-bit AHB Shared RX and TX interfaces Shared bus fabric priority control for RX & TX Priority configurable only for first level of bus fabric 1-2 outstanding transactions shared for RX & TX	Dual 64-bit AXI Separate interfaces for RX &TX Separate bus fabric priority control for RX & TX Separate bus fabric priority for each controller Priority configurable at all levels of bus fabric 4 outstanding transactions for RX &TX (8 total) Improved access timing for DMA engine
RX & TX FIFO Size	4K	8K
Unaligned buffers	Not supported, requires copy	Supported, no copy needed
Interrupt Coalescing	Not supported	Supported and configured separately for each queue
AVB	Must be supported using software	Hardware support for AVB AVB endpoint support for talker and listener Arbitration between AVB and best-effort traffic Credit-based traffic shaping provided by hardware Advanced launch control to assist traffic shaping

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Interrupt Coalescing

- Interrupt counters reduce interrupts to one per *N* frames
- Timers ensure that interrupts occur even under low network loads
- Software can balance tradeoffs between interrupt rate and service latency
- Separate counters for AVB and non-AVB queues

MII/GMII_CLK

TX_CLK

/64

Rx Interrupt Timer

Rx Interrupt Counter

Receive Frame Event

(from all Rx rings)

Receive Interrupt

Tx Interrupt Timer

Tx Interrupt Counter

Transmit Frame Event

(from all Tx rings)

Transmit Interrupt

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AVB Traffic Classes

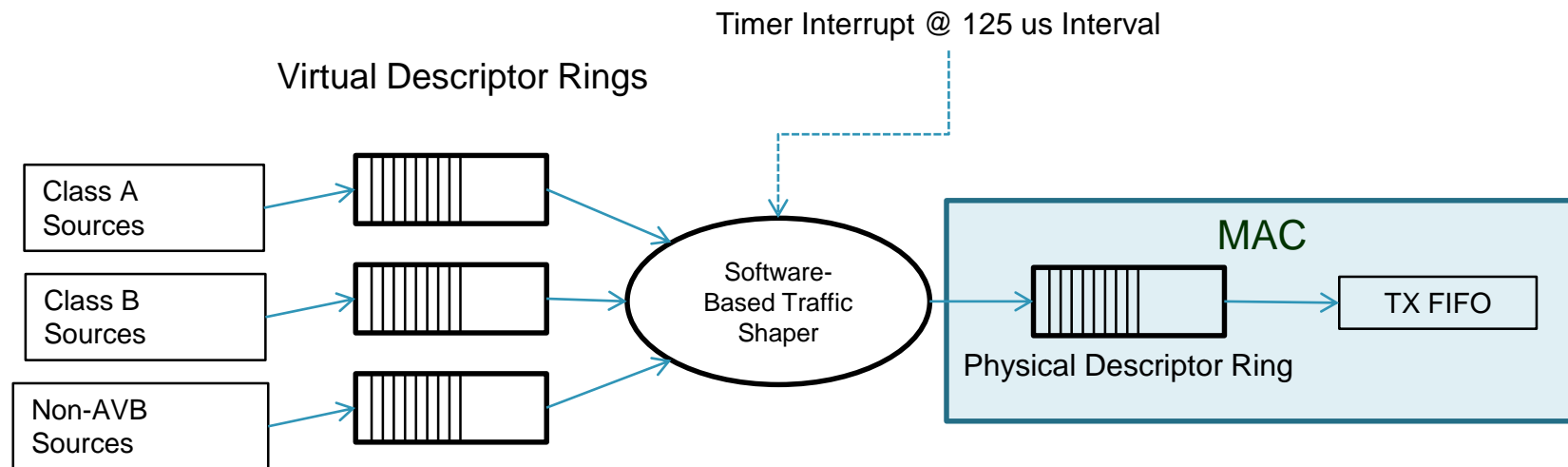| Class Type	Interval	Maximum Latency
Class A	125 us	2 ms over 7 hops
Class B	250 us	50 ms over 7 hops
Class C (definition in progress)	1000 us	TBD

- Class A/B have been defined to target professional A/V use cases

- For automotive use cases, some Class A/B parameters may not be practical

  - Automotive systems unlikely to have 7 hops between talker and listener (implies cascade of 7 Ethernet switches)

  - Potential for poor network efficiency using Class A

  Example: AVB talker sending audio (16-bit stereo @ 48 kHz) using Class A

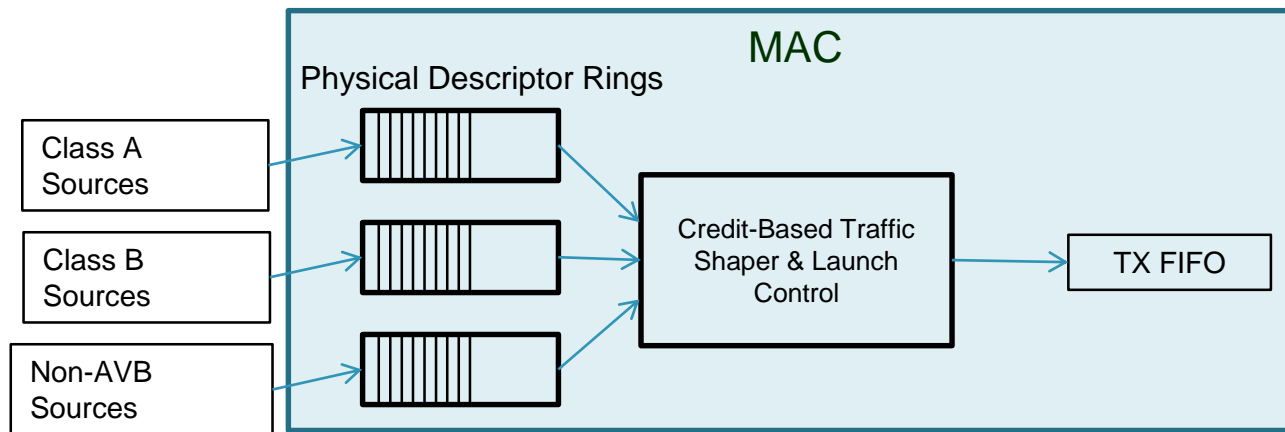 125 us Class A interval → 8 KHz TX rate → 6 samples (24 bytes) / interval

  64-byte Ethernet frame used to TX 24 bytes of audio data → poor network efficiency

AVB Traffic Shaping Using Software

Timer Interrupt @ 125 us Interval

Virtual Descriptor Rings

Class A Sources

Class B Sources

Non-AVB Sources

Software-Based Traffic Shaper
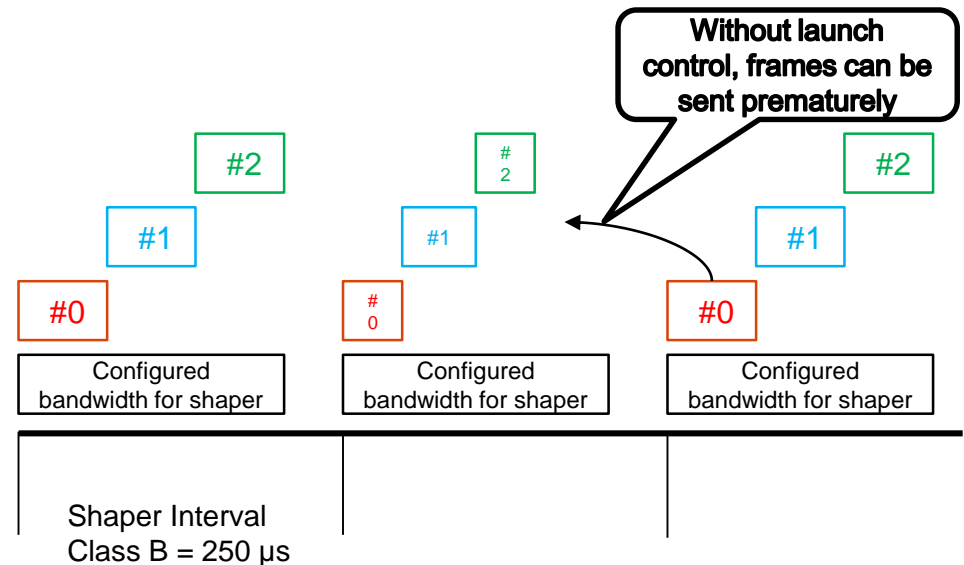
MAC

Physical Descriptor Ring

TX FIFO

- Virtual descriptor rings must be exposed since MAC has a single descriptor ring and cannot distinguish/prioritize AVB class traffic

- Software responsible for dequeueing descriptors from virtual descriptor rings and prioritizing them in the single physical descriptor ring

- Traffic shaping must be provided by software using a low-latency service routine running at 125 us interval (8000 interrupts/sec) to support Class A traffic

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AVB Traffic Shaping in i.MX6 SoloX

MAC

Physical Descriptor Rings

- Class A Sources
- Class B Sources
- Non-AVB Sources

Credit-Based Traffic Shaper & Launch Control

TX FIFO

- Real-time servicing from software not required

- Optional launch control support in hardware supports timestamp field in descriptor to prevent transmitting packets before the intended timeslot

- Launch control reduces the interrupt rate and latency requirements of software

Without launch control, frames can be sent prematurely

#2   #2   #2
#1   #1   #1
#0   #0   #0

Configured bandwidth for shaper | Configured bandwidth for shaper | Configured bandwidth for shaper

Shaper Interval
Class B = 250 µs

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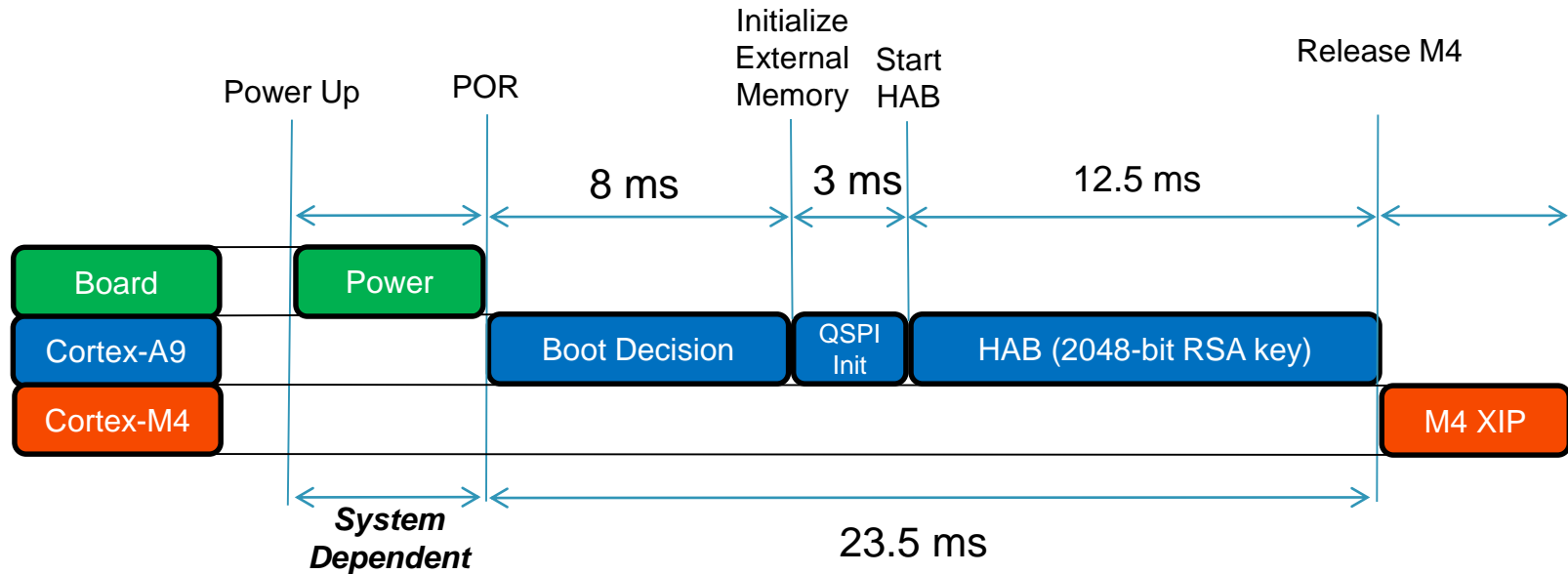# M4 Fast Boot

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M4 Boot Sequence

- i.MX 6SoloX always boots from Cortex A9 CPU.

- The M4 CPU stays in reset after chip reset.

- After A9 CPU boot, it will load M4 program into M4 TCM, then release the reset of M4 to enable it.

- Once enabled, the M4 can execute-in-place from QSPI/NOR or run from DRAM/OCRAM/TCM.

- If the system requires security boot, HAB can be used to validate the boot image before M4 is enabled.

i.MX 6SoloX Boot Estimates – QSPI XIP

- SDR QSPI at 66 MHz
- Cortex-M4 launched with small Cortex-A9 code copied to OCRAM

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Security

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i.MX 6 Series and i.MX 6SoloX Security HW Comparison

Feature	i.MX 6 Series	i.MX 6SoloX
Assurance Boot	Authenticated Boot + Encrypted boot (HABv4.1)	Same
Secure Storage	On-chip zeroizable 4x4kB Secure RAM Off-chip storage protected using unique HW master key (AES-256) (CAAM/SNVS)	**On-chip zeroizable 8x4kB Secure RAM** Remainder is the same
Cryptographic Accelerators	Symmetric: AES-128/256, DES, 3DES, ARC4 Hash & HMAC: MD5, SHA-1, SHA-224, SHA-256 HW Random Number Generator – follows NIST/BSI recommendations > 2015 (CAAM)	**+ Additional AES modes: CMAC, XCBC-MAC**
Secure Real Time Clock	SNVS	SNVS
Hardware Firewalls	External memory (TZASC) On-chip peripherals (CSU) On-Chip Memory (CAAM, OCRAM)	Same
Resource Domain Separation	None	**Separation between Cortex-A9 and Cortex-M4 peripherals and memory (RDC)**
Secure JTAG	Full or Controlled Disable (3 modes)	Same
Physical Tamper Detection	Tamper Input GPIO Tamper Response (SNVS)	Same
Device Configuration	Open, Closed, Field Return	Same
TrustZone Support	Peripheral DMA access control (CSU) Memory DMA access control (ARM TZASC) Interrupt separation (ARM GIC) Secure storage separation (CAAM) OCRAM protected region (OCRAM, CSU)	Same

i.MX 6 Series Secure Boot: HAB4 Features

Feature	HAB4	Comments
Software Image authentication	Yes	Yes
Super Root Key (public key)	Multiple, revocable	Fused Hash
Public key type	RSA-4096 (max)	128-bit security achieved with RSA-3072
Certificate format	X.509v3	Tools support
CMS (PKCS#1)	CMS (PKCS#1)	Tools support
Hash algorithm	SHA-256	NIST recommended
Image Encryption	Yes	
Wrapped key format	CAAM blob	Secret keys stored in secure RAM partition on i.MX 6Dual/Quad
Secret key type	AES-128/192/256	
Decryption algorithm	AES-CCM	Authenticated decryption
Device configuration commands	• Write value • Set/clear bitmask • Wait on bitmask	Provides flexible device configuration
Unlock commands	• Field Return fuse • Revocation fuses • Secure JTAG • CAAM/SNVS	Secure by default

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HAB Impact in Boot Time

- Two process in parallel RSA and SHA.
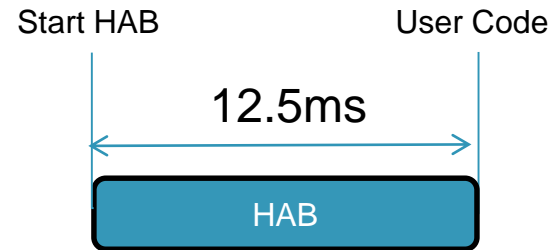
- For i.MX 6SoloX:
  - If initial image < ~1MB:
    - RSA is the bottleneck.
    - HAB time minimum = 12.5 ms.

  - If initial image > 1MB:
    - SHA is the bottleneck
    - HAB time depends on image size.
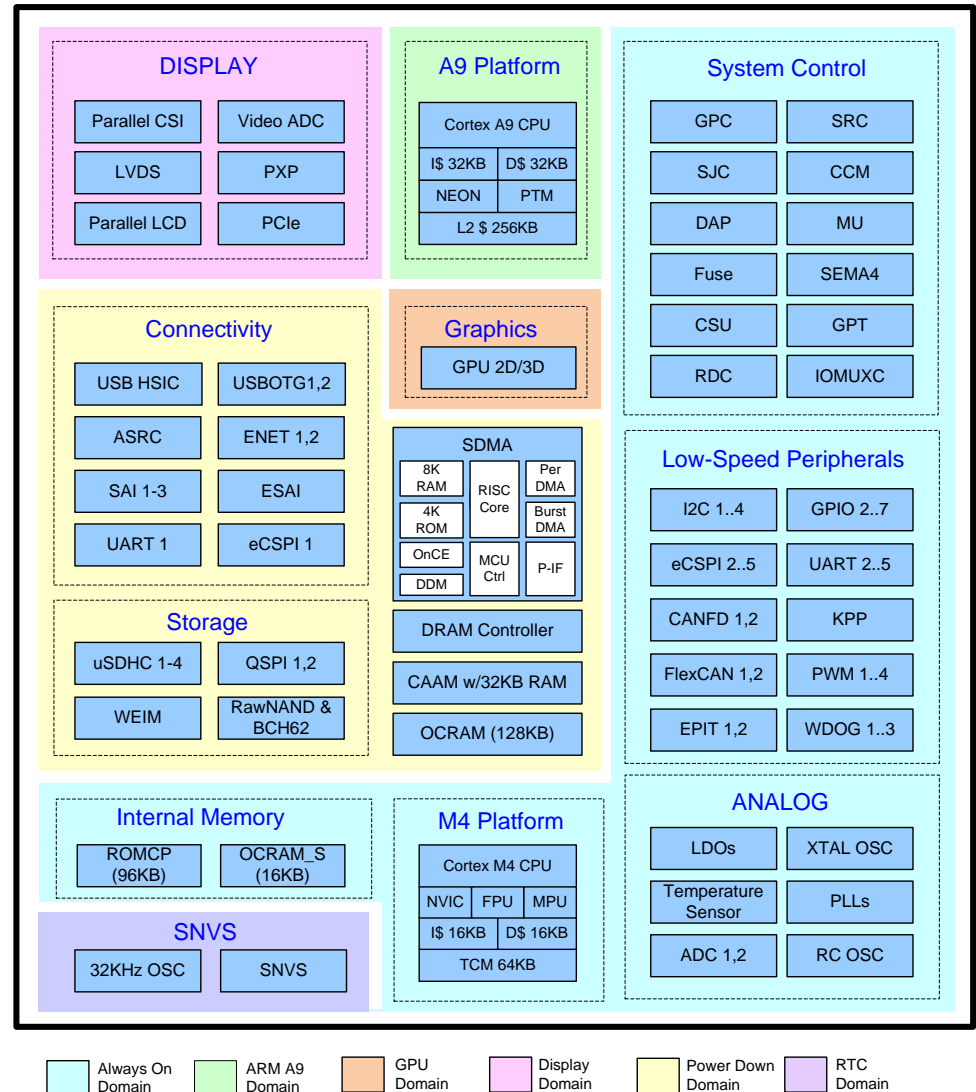
- For i.MX 6Quad, HAB time minimum was 25ms.

Start HAB   User Code

12.5ms

HAB

Low-Power Mode

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SoC Power Domains

- The SOC is divided into 6 power domains for flexible power gating. (not including analog domains)

- The following domains can be shut off independently:
- ARM Cortex A9
- GPU
- Display

- The Power Down domain can be off when A9, GPU and Display is off.

- The Always-On domain will always be on when VDD_SOC is active.

- When entering RTC mode, all the power domains can be off only except the SNVS domain.

DISPLAY	
Parallel CSI	Video ADC
LVDS	PXP
Parallel LCD	PCIe

A9 Platform	
Cortex A9 CPU	
I$ 32KB	D$ 32KB
NEON	PTM
L2 $ 256KB	

System Control	
GPC	SRC
SJC	CCM
DAP	MU
Fuse	SEMA4
CSU	GPT
RDC	IOMUXC

Connectivity	
USB HSIC	USBOTG1,2
ASRC	ENET 1,2
SAI 1-3	ESAI
UART 1	eCSPI 1

Graphics
GPU 2D/3D

SDMA: 8K RAM, RISC Core, Per DMA, 4K ROM, Burst DMA, OnCE, MCU Ctrl, P-IF, DDM

DRAM Controller

CAAM w/32KB RAM

OCRAM (128KB)

Low-Speed Peripherals	
I2C 1..4	GPIO 2..7
eCSPI 2..5	UART 2..5
CANFD 1,2	KPP
FlexCAN 1,2	PWM 1..4
EPIT 1,2	WDOG 1..3

Storage	
uSDHC 1-4	QSPI 1,2
WEIM	RawNAND & BCH62

Internal Memory	
ROMCP (96KB)	OCRAM_S (16KB)

M4 Platform	
Cortex M4 CPU	
NVIC	FPU	MPU
I$ 16KB	D$ 16KB
TCM 64KB	

ANALOG	
LDOs	XTAL OSC
Temperature Sensor	PLLs
ADC 1,2	RC OSC

SNVS	
32KHz OSC	SNVS

Legend: Always On Domain · ARM A9 Domain · GPU Domain · Display Domain · Power Down Domain · RTC Domain

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i.MX 6Series – Power Consumption Summary

i.MX 6Quad		i.MX 6Dual		i.MX 6DualLite		i.MX 6Solo		i.MX 6SoloX		i.MX 6SoloLite	
Sleep	3.8mW	Sleep	3.8mW	Sleep	3.9mW	Sleep	3.1mW	Sleep	1.8mW	Sleep	2.6mW
IDLE	227mW	IDLE	220mW*	IDLE	151mW	IDLE	143mW	IDLE	13mW	IDLE	14.5mW
Video	867mW	Video	867mW	Video	772mW	Video	695mW	Video	n/a	Video	n/a
3D	1.6W	3D	1.6W	3D	1.1W	3D	1.1W	3D	0.5W	3D	n/a
TypMax	3.8W	TypMax	n/a	TypMax	2.4W	TypMax	1.7W	TypMax	1.1W	TypMax	n/a

All results include power at the chip (cores, accelerators, peripherals, DDR I/O)

- **i.MX 6Dual cores are estimated on i.MX 6Quad by clock gating two cores**
- **Results are based on typical silicon @ 25C**

Case 1: Deep Sleep → lowest power mode available
Case 2: System IDLE mode → LCD off, system waiting on input
Case 3: 1080p30 video → Playback on 1080p TV, device LCD is off
Case 4: 3D Benchmark → Running 3DMobileMark ES 1.1 on device LCD
Case 5: "Typical" Max Power → heavy use case (1080p playback on TV, 3DMM06 on LCD, Dhrystone on all cores)

Scalable Performance and Power Consumption
'One Series fits all'

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Power Mode Details

	RUN	System IDLE	Low Power IDLE	SUSPEND
CCM LPM Mode	RUN	WAIT	WAIT	STOP
ARM Core	ON	Low-Freq Voltage	Power Down	Power Down
L1 Cache	ON	ON	Power Down	Power Down
L2 Cache	ON	ON	ON / Power Down	Power Down
SOC	Nominal Voltage	Nominal Voltage	Nominal Voltage	Standby Voltage
GPU	ON / Power Down	Power Down	Power Down	Power Down
DISPLAYMIX	ON / Power Down	Power Down	Power Down	Power Down
FASTMIX/MEGAMIX	ON	ON	ON / Power Down	ON / Power Down
M4	ON / Clock Gated	ON / Clock Gated	ON / Clock Gated	Always Clock Gated
PLL	ON as needed	ON as needed	Power Down	Power Down
XTAL	ON	ON	OFF	OFF
RC OSC	OFF	OFF	ON	OFF
DRAM	ON	Self-Refresh	Self-Refresh	Self-Refresh
DRAM IO Low Power	No	No	Yes	Yes
LDO ARM	ON	ON	Power Gate	Power Gate
LDO SOC	ON	ON	Digital Bypass	Digital Bypass
LDO2P5	ON	ON	OFF	OFF
LDO1P1	ON	ON	OFF	OFF
WEAK2P5	OFF	OFF	ON	OFF
WEAK1P1	OFF	OFF	ON	OFF
Bandgap	ON	ON	OFF	OFF
Low Power Bandgap	OFF	OFF	ON	OFF
MMDC clock	400MHz	24MHz	OFF	OFF
AHB clock	133MHz	24MHz	3MHz	OFF
IPG clock	66MHz	12MHz	1.5MHz	OFF
PER clock	66/24MHz	24MHz	1MHz	OFF
Module clocks	On as needed	On as needed	On as needed	OFF
GPIO wakeup	Yes	Yes	Yes	Yes
RTC wakeup	Yes	Yes	Yes	Yes
USB remote wakeup	Yes	Yes	Yes (requires megamix on)	Yes (requires megamix on and weak2p5 for HSIC)
Other wakeup source	Yes	Yes	Yes (megamix peripherals require megamix to be on)	No
Power Target	Varies	20-50mW	6-9mW	1-1.5mW

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* All power numbers are typical silicon at 25C

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i.MX 6SoloX: Software

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Leadership Software - i.MX Linux Enablement

- Silver Member of Linux Foundation
- AGL Working Group Bronze Member (in progress)

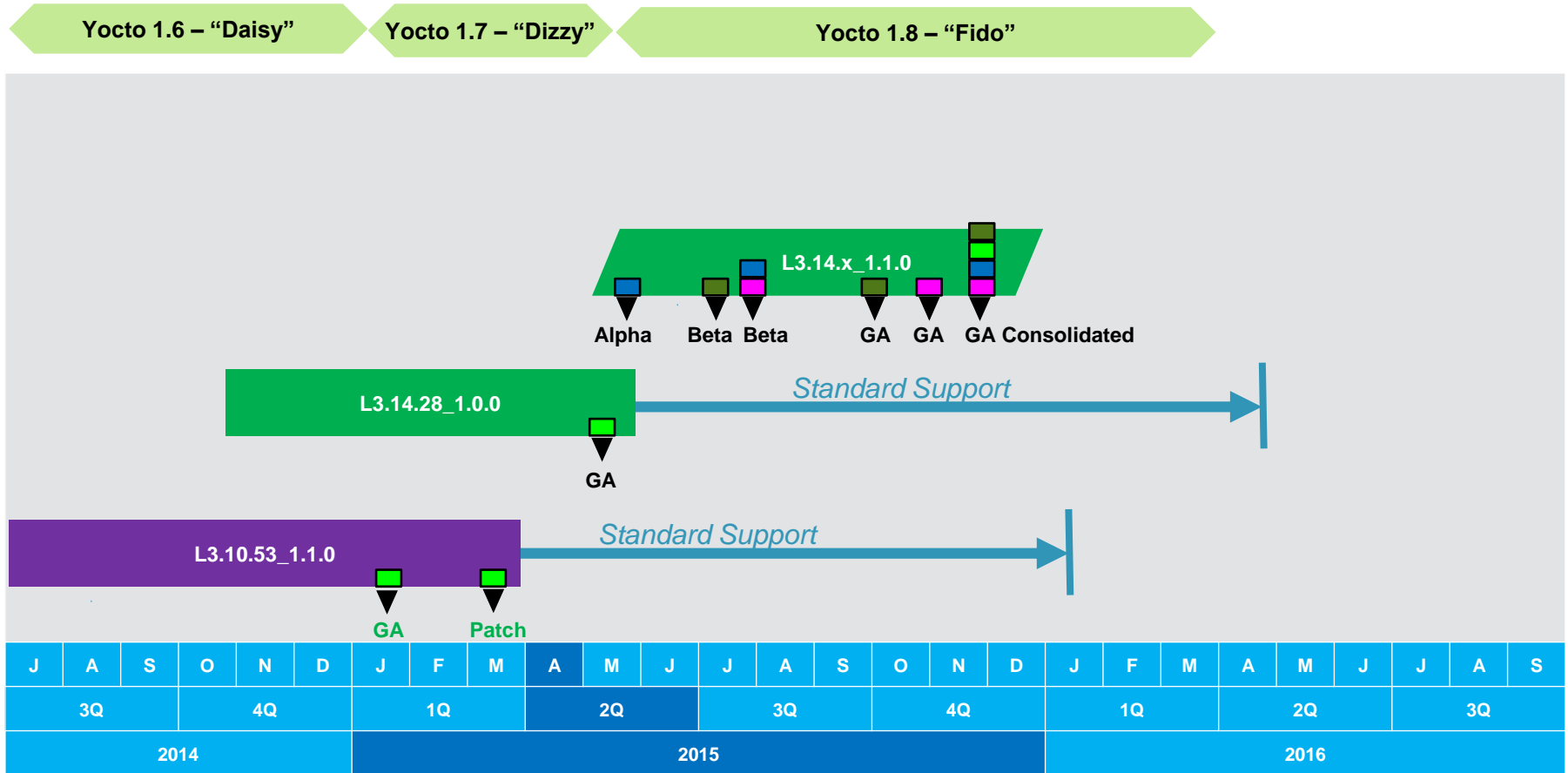**Over the past 15 years shipping i.MX application processors…**

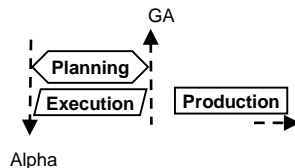i.MX 2   i.MX 3   i.MX 5   i.MX 6

← 39,000+ Linux Downloads →

Multiple i.MX 6 Series customer engagements are using GENIVI Solutions
Freescale has more compliant platforms than ANY semiconductor vendor
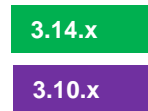*Reference: http://www.genivi.org/compliant-products*

Linux Release Plans

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GA – Support for 1 year
Alpha & Beta – Availability until next release

i.MX Android Leadership

Commitment: **9** Android OS versions released over past **7** years

Broad Acceptance: **Over 25,000 + Downloads** for i.MX BSP's to date

Fast Development: **~4 months** from development start to production release on multiple Android versions

Cross market robustness: **Automotive, Embedded/Industrial, Consumer**

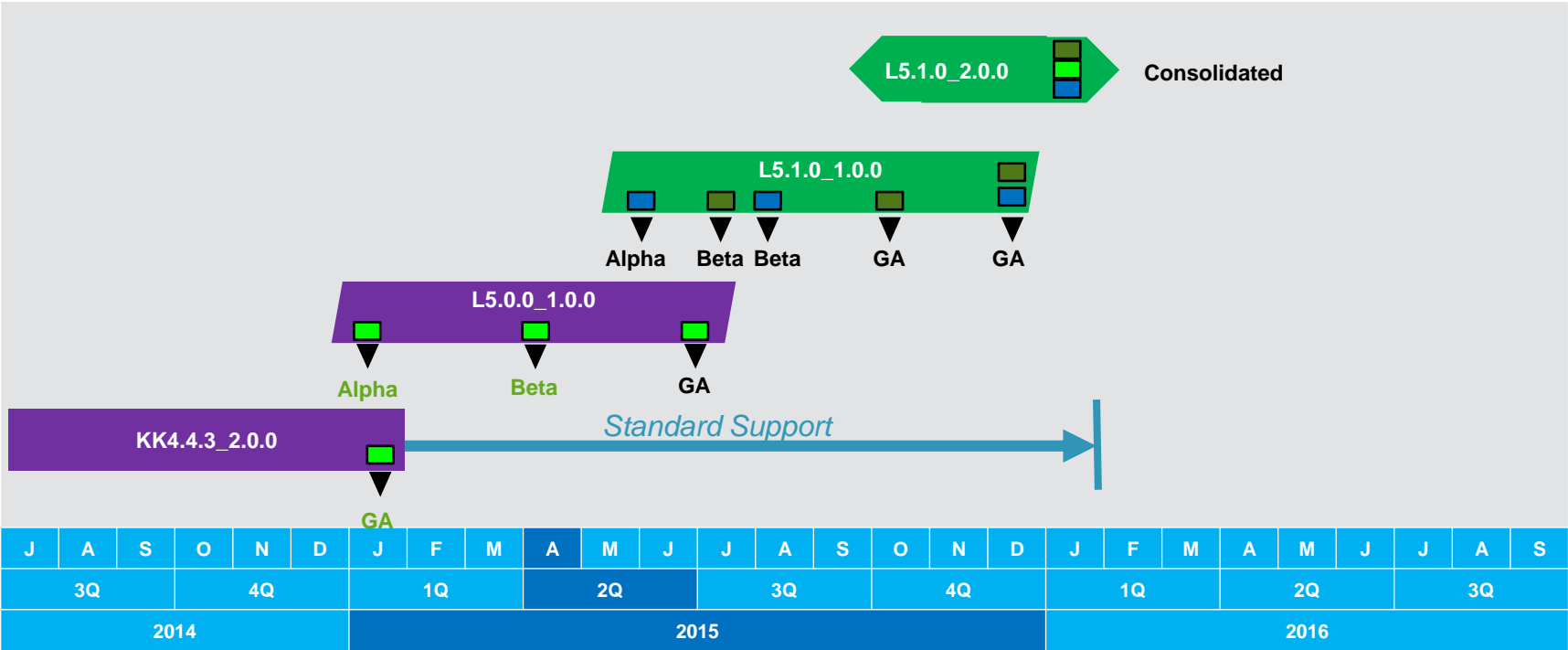**Continued support:** New OS releases for **2 years** after silicon production qual

Leadership: i.MX – only Android system shipping in a **top 5 OEM infotainment platform** today

| 2008 | 2009 | 2010 | 2011 | 2011 | 2012 | 2012 | 2013 | 2014 | 2015 |

i.MX 6 Series Software – Android Release Strategy

- **Support the latest Android OS releases across i.MX 6 series**
  - More information: http://www.android.com/whatsnew/

- **Support core functionality**
  - As defined in the relevant Android CDD and only if supported by the Freescale development platform
  - Core functionality is released in the standard BSP package
  - Extended functionality (e.g. multimedia extensions, Wi-Fi sink) is available for license – contact L2manager-android@freescale.com for further details

- **Freescale provides CTS results**
  - Android CTS (Compatibility Test Suite) is run on FSL development hardware
  - No guarantee is made regarding ability to pass CTS as not all features under test are supported on the FSL development platforms
  - The OEM is responsible for device level CTS pass/fail
  - i.MX 6SoloLite/6SoloX Notes:
    - No guarantee on CTS pass rate
    - No Miracast support (requires VPU)

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Android Release Plans

Lollipop 5.0

L5.1.0_2.0.0 — Consolidated

L5.1.0_1.0.0

Alpha   Beta   Beta   GA   GA

L5.0.0_1.0.0

Alpha   Beta   GA

KK4.4.3_2.0.0   *Standard Support*

GA

J	A	S	O	N	D	J	F	M	A	M	J	J	A	S	O	N	D	J	F	M	A	M	J	J	A	S
3Q			4Q			1Q			2Q			3Q			4Q			1Q			2Q			3Q		
2014						2015												2016								

Release Schedule

GA
Planning
Execution
Production
Alpha

Linux Kernel
3.10.x
3.14.x

Supported Platforms
■ i.MX 6QP/i.MX6DP
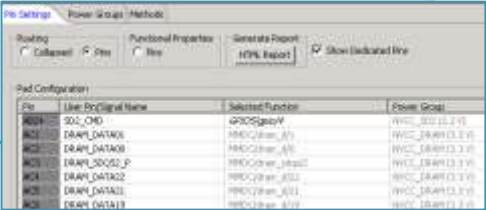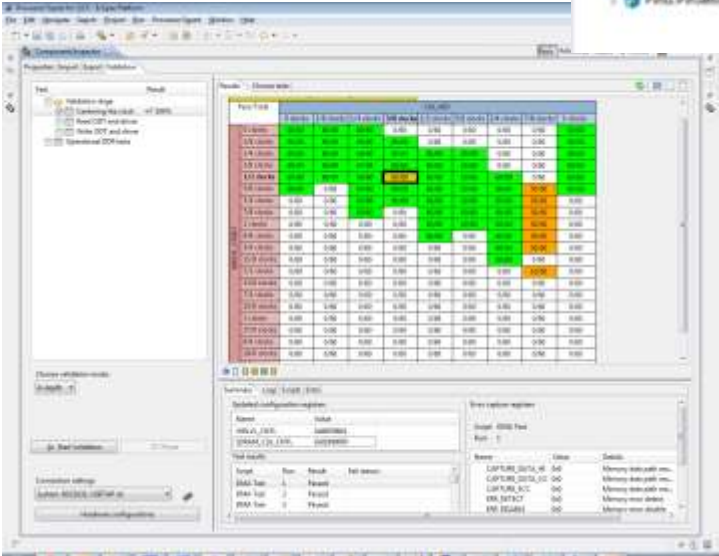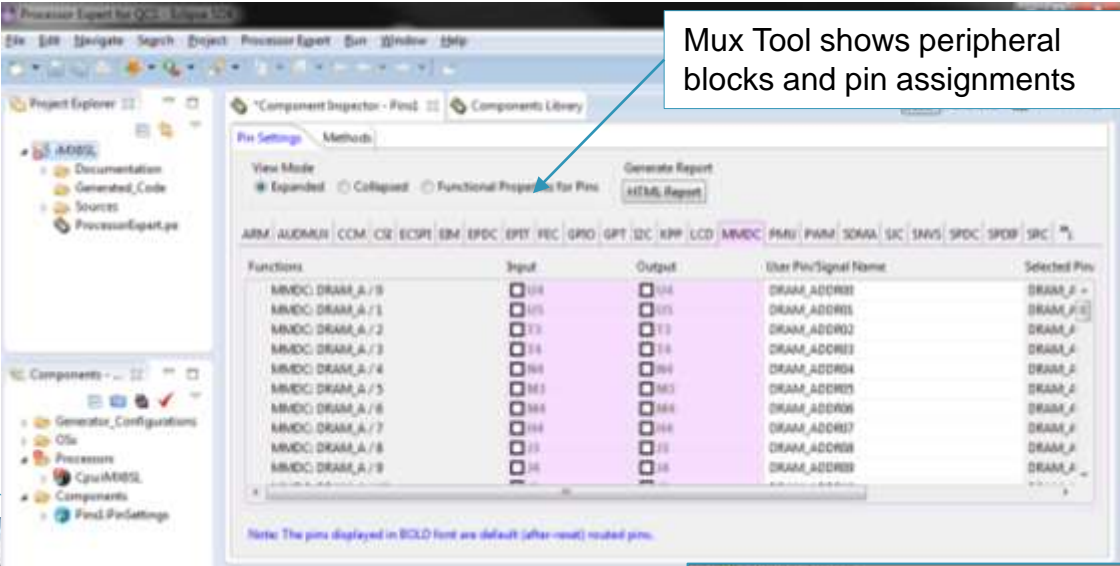■ i.MX 6Q, i.MX6 D, i.MX 6DL, i.MX 6S, i.MX 6Solox, i.MX 6SL
■ i.MX 7 SABRE SDB

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GA – Support for 1 year
Alpha & Beta – Availability until next release

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Processor Expert for i.MX 6SoloX
IOMUX tool configuration/validation

Define a configuration project →

Mux Tool shows peripheral blocks and pin assignments

Tools show up here

Supports i.MX Power Groupings

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Silicon, Tools and SW Available Now

The i.MX 6SoloX is a highly integrated multi-market applications processor designed to enable secure and connected homes and vehicles within the Internet of Things.

✓ **First device to market with ARM® Cortex®- A9 and Cortex-M4 cores**
Take advantage of heterogeneous processing and benefit from high performance with real time responsiveness, allowing for <u>smart system power</u>.

✓ **Security**
Design with confidence with the on-chip <u>resource domain controller </u>providing a centralized programming model to configure isolation and sharing of system resources

✓ **Optimized Integration**
Select the ideal integration for your application with the 17 unique device options, spanning <u>consumer, industrial, and automotive markets</u>.

✓ **Development Support**
Richly featured development systems with mature and optimized Linux and Android BSPs and MQX BSP for Cortex-M4.

Multi-Core Communication Library

Multi-Core Communication (MCC) Library

- Software mechanism for communication between heterogeneous cores that takes advantage of hardware synchronization and communication features
- Lightweight and fast
- Scalable from bare metal to Linux
- Uses shared RAM, interrupts, hardware semaphores
- Configurable at build time
  - Buffer sizes
  - Number of buffers
  - Maximum number of endpoints
- API calls are simple send/receive between endpoints
- Variable timeouts

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Endpoints

- Endpoints are receive buffer queues in shared RAM
- Addressed by a triplet of

Element	Description
Core	On the i.MX 6SoloX the A9 is core 0 and the M4 is core 1.
Node	Current implementations select a single node for the Linux MCC TTY driver and one for MQX tasks. This is not a design limitation of MCC.
Port	an arbitrary value up to a configurable maximum (though zero is reserved)

- Endpoints are part of a user's system design — there is no discovery protocol.
- Similar to Internet Protocol (IP) which addresses endpoints by an IP address, a protocol (e.g. TCP, UDP) and a port number

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Buffer Management

- Data transfers occur in fixed size buffers located in shared RAM.
- All buffers in the pool are allocated during initialization.
- Only one buffer pool is shared by all cores.
- Send / Receive
  - Copy data to user buffer or
  - Get a pointer to the buffer in shared RAM (user responsible for freeing shared buffer)
  - May wait for a timeout, return immediately or block.

Shared RAM

- Shared RAM contains
  - Buffers for transferring data between endpoints
  - Internal buffer management data structures
- Shared RAM configuration
  - Maximum number of endpoints (default: 5)
  - Number of data buffers (default: 10)
  - Fixed size of every data buffer (default: 1024)
- Access to shared RAM protected by hardware semaphores

Interrupts

- Core interrupts occur when
    - Buffer queued for an endpoint on the interrupted core
    - Buffer freed by the interrupting core
- One signal queue per core
- Signal in the queue indicates type of interrupt (buffer queued or freed)
- Maximum number of outstanding signals configurable at build time

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MCC API

- Initialization, version control
  - `mcc_initialize()`
  - `mcc_destroy()`
  - `mcc_get_info()` to compare version compatibility between MCC on each core
- Data transfer — `_nocopy()` availability configurable at build-time
  - `mcc_recv()`
  - `mcc_recv_nocopy()`
  - `mcc_send()`
  - `mcc_send_nocopy()`
- Buffer management for `_nocopy()` data transfers
  - `mcc_get_buffer()`
  - `mcc_free_buffer()`
- Status
  - `mcc_msgs_available()` for this core only

MCC Status

- MCC is officially released, version 002.000
  - Linux L3.10.53_1.1.0_GA and L3.14.28_1.0.0_iMX6SX_BUNDLE
  - MQX 4.1.0 GA for i.MX 6SoloX
- Released under a BSD-like license (dual BSD/GPL on Linux)
- Demos have been available incorporating Linux, MQX and MCC
  - Ping Pong Demo
  - i.MX 6SoloX Power Demo shown at FTF

MCC Alternative: Linux rpmsg

- rpmsg is the Remote Processor Messaging framework implemented in the Linux kernel.
- API provides facilities to send messages and register a device driver with `probe()`, `remove()` and receive `callback()` functions.
- Uses "addresses" similar in concept to MCC endpoints but implemented as 32-bit unsigned integers. Addresses identify which driver's receive handler should be invoked.
- Each device is a communication "channel" which incorporates both a source and a destination rpmsg address.
- rpmsg implements an "endpoint" structure
  - Not like MCC endpoints
  - Contains rpmsg address + internal implementation structures
  - Only needed for complex drivers requiring more than one channel
  - The `probe()` function creates an endpoint, typically the only one needed.
- rpmsg has not been implemented in MQX – independent implementations seen in FreeRTOS

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MCC Implementations

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MCC in Linux Kernel-Space

- The raw MCC API is provided in kernel-space.
- Linux porting layer in arch/arm/mach-imx/mcc_linux.c
- Shared parameters
  - Memory buffers are located in DDR RAM (0xbff0_0000)
  - Buffer size is configured as 1024 bytes but effectively limited by the driver to 1000 due to a stack frame maximum of 1024. Keep this in mind when writing your Cortex-M4 driver.
  - Receive buffer count: 10
  - Endpoints: 5, but the implementation effectively limits this to two – one for each core.
- Buffer management and Cortex-M4 interrupts are handled by the imx-mu driver.
- SEMA4 semaphores are implemented in the imx-sema4 driver.
- mcc_send() and mcc_recv() calls are blocked by Linux wait queues when buffers are unavailable.
- Demo "ping pong" driver available in kernel-space.

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MCC in Linux User-Space

- imx6sx-mcc-tty driver available in kernel configuration in menuconfig's Device Drivers → Character devices.
  - Enable the IMX SEMA4 driver (CONFIG_IMX_SEMA4).
  - Disable IMX MCC test driver (this is the "ping pong" demo from the previous page).
  - Enable IMX PTY for MCC interface (CONFIG_IMX_MCC_TTY).
- Implements /dev/ttyMCC, character device major 5, minor 3
- The driver is an intermediate layer between MCC message passing and the standard Linux TTY driver.
  - Simple character stream like any other TTY
  - Termios line discipline
    - Watch out for echo settings that might confuse your Cortex-M4 side
    - MCC message block composition might not work the way you think.

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MCC in MQX

- MCC was initially developed in MQX on the VFxxx Controller platform
  - Similar to i.MX 6SoloX: Cortex-A5 + Cortex-M4
  - MQX using MCC ran on both cores initially, expanded to Linux on the Cortex-A5
- Buffers, message queues, etc. handled in MQX porting layer
- The MCC API is provided directly in MQX
- Interrupt vs. polling of MCC message handling is left to the user to implement.
  - Blocking, non-blocking or blocking with a timeout available in mcc_send/_recv() calls.

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Summary Slide

With the knowledge from this session, you should be able to:

- Identify if the i.MX 6SoloX is the right fit for your project.

- Determine the right package and device for your design.

- Be aware of the options for hardware and software development.

- Understand the benefits of HMP, new IP blocks and low-power design on the i.MX 6SoloX.

- Understand the basics of the Multi-Core Communications (MCC) library to allow for co-existing operating environments and shared resources between the A9 and M4 cores.

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Freescale i.MX 6SoloX Information Links

[i.MX 6SoloX Product Page](#)

[i.MX 6SoloX Documentation](#)

[i.MX 6SoloX Parts Ordering](#)

[www.imxcommunity.com](#)

[i.MX 6 Development Tools](#)

Q&A

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www.Freescale.com