How to run DDR stress test in hab_closed board

Maggie Jiang

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SECURE CONNECTIONS FOR A SMARTER WORLD

Background

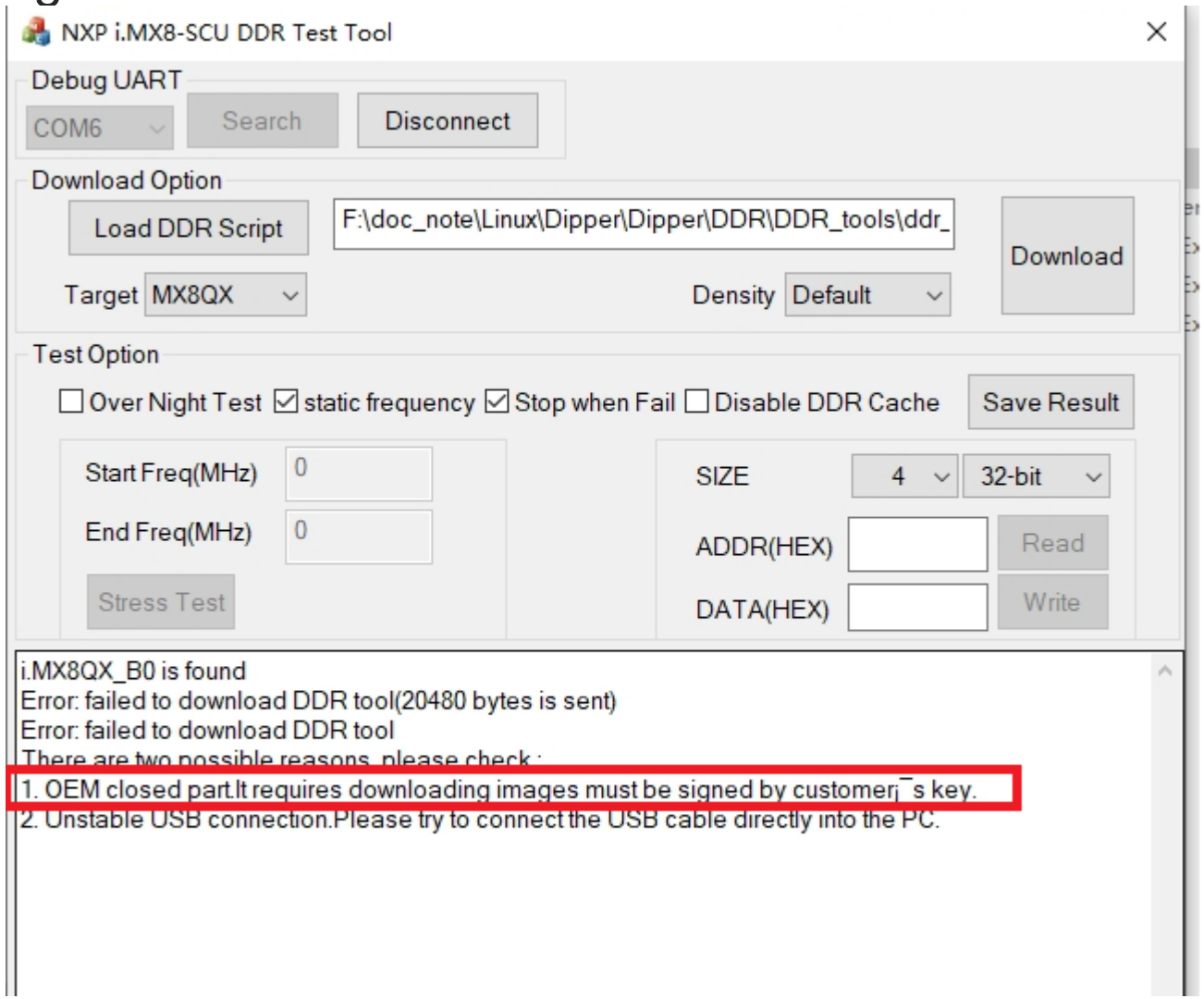
- Platform: i.MX8QXP (i.MX8QM is similar)
- Customer requirement:

  The i.MX8QXP board already burn fuse and do hab_closed. Then customer need to replace DDR type, or debug returned board.

  So they need to run DDR stress test in hab_closed board.

FAILED WHEN USING GUI VERSION DDR STRESS TEST

- It have following error when do DDR stress test



GUI VERSION DDR STRESS TEST

- So the question is : How to sign image when doing DDR stress test?
- Answer is: Our released GUI version DDR stress test doesn't support signed image.
- The reason is:

  When do DDR stress test, customer input DDR script file, so it combine customer input DDR script file and scfw together dynamically:

  DDR script file: MX8QXP_C0_B0_LPDDR4_RPA_1.2GHz_v14.ds

  Scfw: mx8_ddr_stress_test_ER14\bin\mx8qxb0_scfw_download.bin

  So it have no way to sign the whole scfw image and run in hab_closed board.
- The solution is:

 using command line version DDR stress test and sign flash.bin when using command line version DDR stress test

CUSTOMER BOARD DDR SCFW

- When compile SCFW, the procedure is same with default SCFW compile and set customer DDR script:
- i.MX8QXP MEK board:

  make qx B=mek R=B0

  It use scfw_export_mx8qx_b0/platform/board/mx8qx_mek/dcd/imx8qx_dcd_1.2GHz.cfg by default
- Customer board:

make qx B=mek R=B0 DDR_CON=customer_ddr_script

then it will use customer_ddr_script.cfg file under scfw_export_mx8qx_b0/platform/board/mx8qx_mek/dcd

- It produce scfw_tcm.bin under imx-scfw-porting-kit-1.7.0/src/scfw_export_mx8qx_b0/build_mx8qx_b0

COMMAND LINE VERSION DDR STRESS TEST FLASH.BIN

- DDR stress test firmware is mx8qx_ddr_stress_test.bin, which can get from FAE for tested version.
- Then put this file into imx-mkimage/iMX8QX

  There is also mx8qxc0-ahab-container.img and scfw_tcm.bin under iMX8QX.

Then produce flash.bin using following command:

make SOC=iMX8QX REV=C0 flash_ddrstress

Why add flash_ddrstress parameter, in imx-mkimage/iMX8QX/scripts/test.mak, it list:

flash_ddrstress flash_b0_ddrstress: $(MKIMG) $(AHAB_IMG) scfw_tcm.bin mx8qxb0_ddr_stress_test.bin

./$(MKIMG) -soc QX -rev B0 -append $(AHAB_IMG) -c -flags 0x00800000 -scfw scfw_tcm.bin -ap mx8qxb0_ddr_stress_test.bin a35 0x00100000 -out flash.bin

LOG OUTPUT

- When run: make SOC=iMX8QX REV=C0 flash_ddrstress
- The log is following, it means it use following three files to combine flash.bin:
- ./../mkimage_imx8 -soc QX -rev B0 -append mx8qxc0-ahab-container.img -c -flags 0x00800000 -scfw scfw_tcm.bin -ap mx8qxb0_ddr_stress_test.bin a35 0x00100000 -out flash.bin

  CST: CONTAINER 0 offset: 0x400

  CST: CONTAINER 0: Signature Block: offset is at 0x590

  DONE.

  Note: Please copy image to offset: IVT_OFFSET + IMAGE_OFFSET

COMPARE FLASH.BIN

- Normal flash.bin include:

✓ SECO firmware(mx8qxc0-ahab-container.img)

✓ SCFW(scfw_tcm.bin)

✓ Uboot image(u-boot.bin)

✓ ATF(bl31.bin)

- command line version DDR stress test flash.bin:

✓SECO firmware(mx8qxc0-ahab-container.img)

✓SCFW(scfw_tcm.bin)

✓ DDR stress test firmware(mx8qx_ddr_stress_test.bin)

So it doesn’t include uboot，and use ddr stress test firmware instead.

SIGN DDR STRESS TEST VERSION FLASH.BIN

1.Check SOC=iMX8QX REV=C0 flash_ddrstress log output:

……

- CST: CONTAINER 0 offset: 0x400
- CST: CONTAINER 0: Signature Block: offset is at 0x590

……

2.Modify csf_boot_image.txt :

- # Offsets = Container header Signature block (printed out by mkimage)
- Offsets   = 0x400   0x590

3. Sign flash.bin using following command:

- ./cst -o flash-signed.bin -i csf-flash-ddr-test.txt

BURN DDR STRESS TEST VERSION FLASH.BIN INTO EMMC

- Burn non-singed flash.bin into normal board:
  uuu -b emmc flash-normal.bin flash.bin

- Burn singed flash.bin into hab_closed board:
  uuu -b emmc flash-normal.bin flash-signed.bin

✓flash-normal.bin : It is normal flash.bin which include uboot.
✓flash.bin: It is DDR stress test version flash.bin which is non-signed.
✓flash-signed.bin: It is DDR stress test version flash.bin which is signed.
We use normal flash.bin to burn DDR stress test version flash.bin

BOOT UP BOARD

- It have following log, instead of normal uboot log, then press “Y”

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  - MMU and cache setup complete

--Clock Rates (current clock rates)--
  - Cortex-A35 clock rate: 1200MHz
  - DRC controller0 and DDR PHY clock rate: 600000000Hz, 1200000000Hz

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        DDR configuration
DDR type is LPDDR4
Data width: 32, bank num: 8
Row size: 16, col size: 10
Two chip selects are used
Number of DDR controllers used on the SoC: 1
Density per chip select:   1536MB
Density per controller is: 3072MB
Total density detected on the board is: 3072MB

Command Bus Training was executed
No DDR data training errors detected for DDRC0
=========================================

Would you like to run the DDR Stress test?
```

CHOOSE DDR SIZE

- Choose DDR size

```
DDR type is LPDDR4
Data width: 32, bank num: 8
Row size: 16, col size: 10
Two chip selects are used
Number of DDR controllers used on the SoC: 1
Density per chip select:   1536MB
Density per controller is: 3072MB
Total density detected on the board is: 3072MB

Command Bus Training was executed
No DDR data training errors detected for DDRC0
=============================================

Would you like to run the DDR Stress test?


Please select the desired DDR density to test. Enter:
 '1' for 8GB;   '2' for 6GB;   '3' for 4GB;
 '4' for 3GB    '5' for 2GB;   '6' for 1GB;
 '7' for 512MB; '8' for 256MB; '9' for 128MB; 'a' for 64MB;
 'b' for 32MB;  'c' for 16MB;  'd' for 8MB;   'e' for 4MB;
 'f' for 2MB
  Or hit 'x' to test all of the detected density
```

RUN DDR STRESS TEST

- Input start/end frequency, then start DDR stress test

```
NOTE: The start freq must be within +/-50MHz of the current frequency.
(current DDR frequency - 50MHz) < start freq < current DDR frequency
1200
  The actual start frequency is: 1200 MHz

Enter desired END freq in MHz, then hit enter.
Make sure this is equal to or greater than start freq
The actual frequency will be rounded down to the nearest 12MHz per PLL programmi
ng.
1200
  The actual end frequency is: 1200 MHz

Do you want to run DDR Stress Test for simple loop or infintely (till failure)?
Type '0' for simple loop. Type '1' for infinte test


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  --Running DDR test on region 1--
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t0.1: data is addr test
....
```

SECURE CONNECTIONS
FOR A SMARTER WORLD