mx8_ddr_stress_test without UI

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Case Description

i.MX8/i.MX8X/i.MX8DXL has ddr stress test tool. It is a window UI program.

In some cases, i.MX devices is security closed. Need signed image to run.

Such as unit fail field return analyze, switch new ddr part on existing board.

Solution

Make a ddr stress test “flash.bin” and send test command directly through uart.

Generate ddr stress test flash.bin

Copy ddr_stress_test.bin from mx8_ddr_stress_test to imx-mkimage

Use **flash_ddrstress** rule to generate the flash.bin

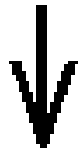
i.MX8X:
make SOC=iMX8QX flash_ddrstress REV=C0

i.MX8DXL:
make SOC=iMX8DXL flash_ddrstress V2X=NO

i.MX8QM:
make SOC=iMX8QM flash_b0_ca72_ddrstress

uart command sequence

initial ddr stress test



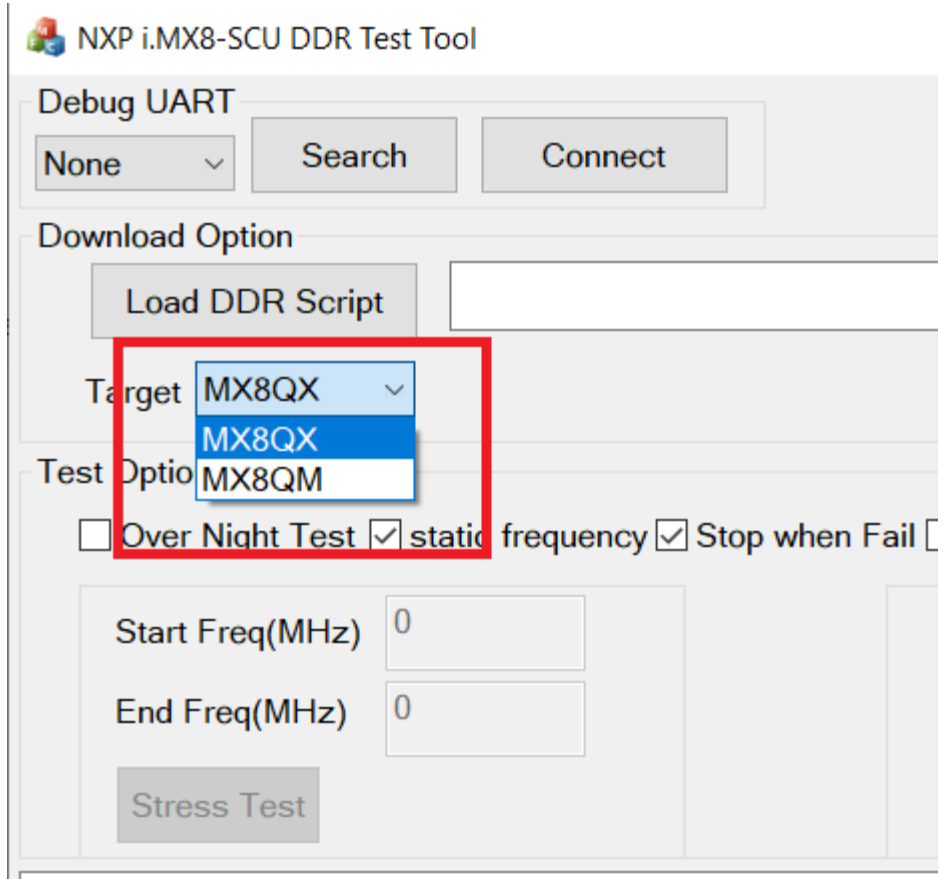
start ddr stress test

uart command code

target :

81 for i.MX8X
81/86 i.MX8DXL er15pre uses 81 and er15.1 uses 86
80 for i.MX8QM

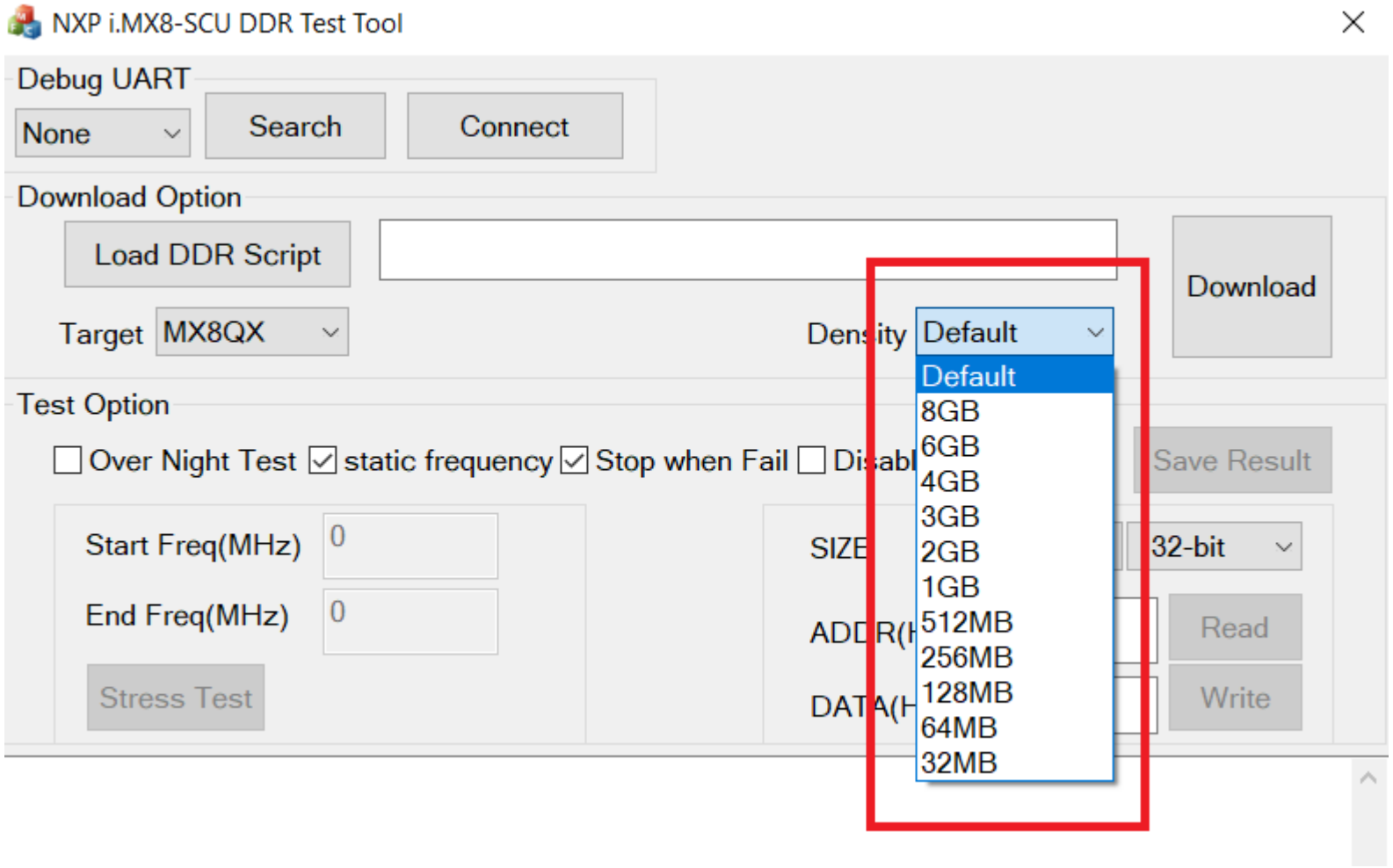
Ex:
81 00 00 00 00 is i.MX8X and i.MX8DXL initialization.



uart command code

initial ddr stress test :

81 00 00 00 00 default
81 20 00 00 00 8G
81 18 00 00 00 6G
81 10 00 00 00 4G
81 08 00 00 00 2G
81 04 00 00 00 1G
81 02 00 00 00 512M
81 01 00 00 00 256M
81 00 80 00 00 128M
81 00 40 00 00 64M
81 00 20 00 00 32M

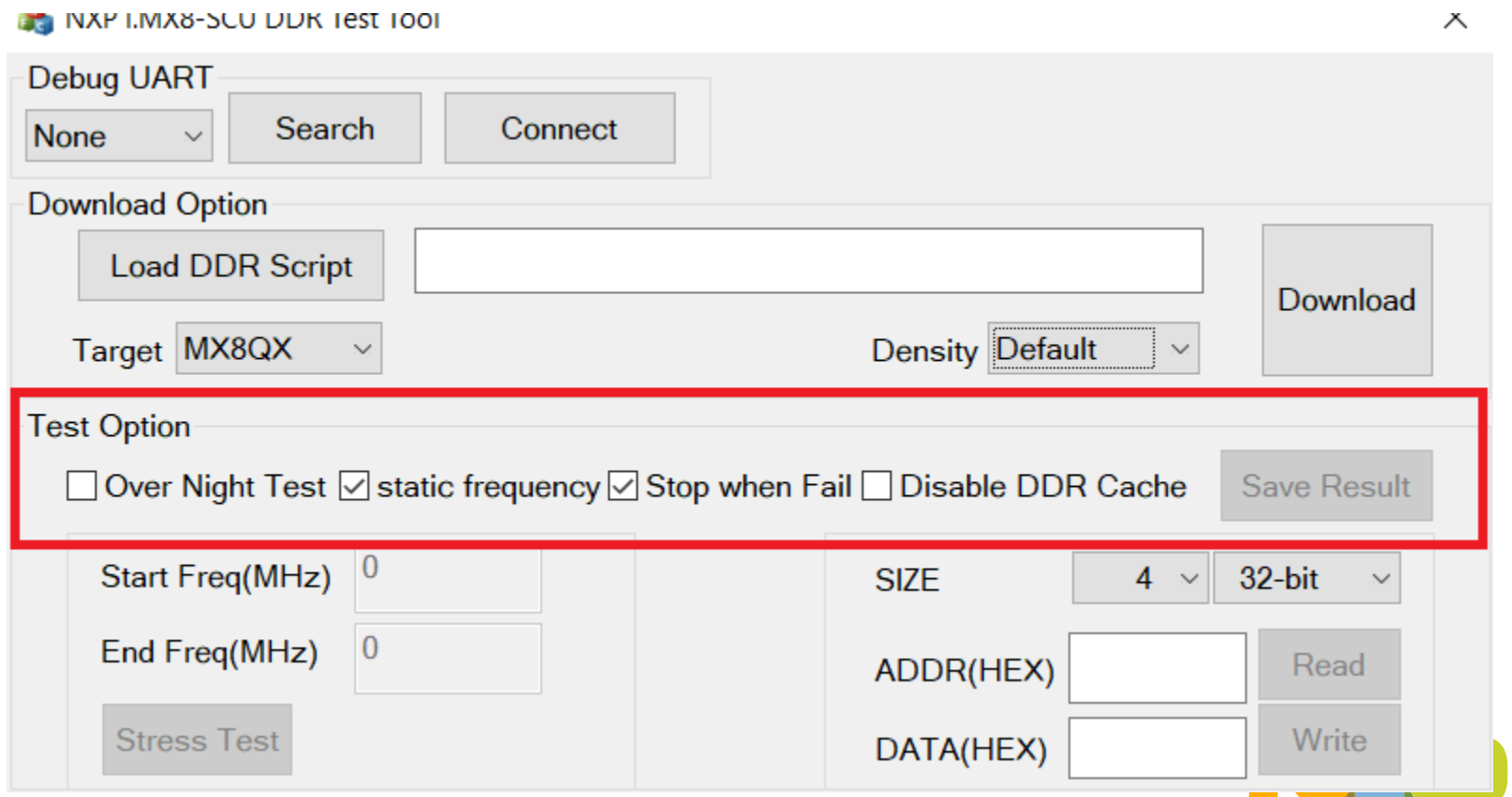


uart command code

start ddr stress test

02 08 **|** Start Freq(MHz)**|**End Freq(MHz)**|**Over Night Test**|**stop when fail**|**disable ddr cache**|**static frequency

All the below field in 16 bit
Start Freq(MHz)
End Freq(MHz)
Over Night Test
stop when fail
disable ddr cache
static frequency



uart command code(Cont.)

start ddr stress test

02 08 | Start Freq(MHz)|End Freq(MHz)|Over Night Test|stop when fail|disable ddr cache|static frequency

Start Freq(MHz) : 16bit ex: 04 7e 1150
End Freq(MHz) : 16bit ex: 04 b0 1200

Over Night Test: 0 --- no Over Night Test, 1 --- Over Night Test
stop when fail : 0 --- stop when fail, aa --- no stop when fail
disable ddr cache : 0 --- enable ddr cache, aa --- disable ddr cache
static frequency : 0 --- set in Start Freq(MHz) and End Freq(MHz) field, aa --- static frequency

02 08 00 00 00 00 01 00 00 aa --- Over Night Test, stop when fail, enable ddr cache, static frequency
02 08 04 7e 04 b0 00 00 aa 00 --- start 1150M, end 1200M,not over night, Disable DDR cache, no static freq

Test

HW: i.MX8QXP MEK + Base Board
SW: lf-5.10.52-2.1.0 + mx8qxb0_ddr_stress_test.bin from mx8_ddr_stress_test_ER14
UART tool: SerialTool
https://github.com/Skiars/SerialTool

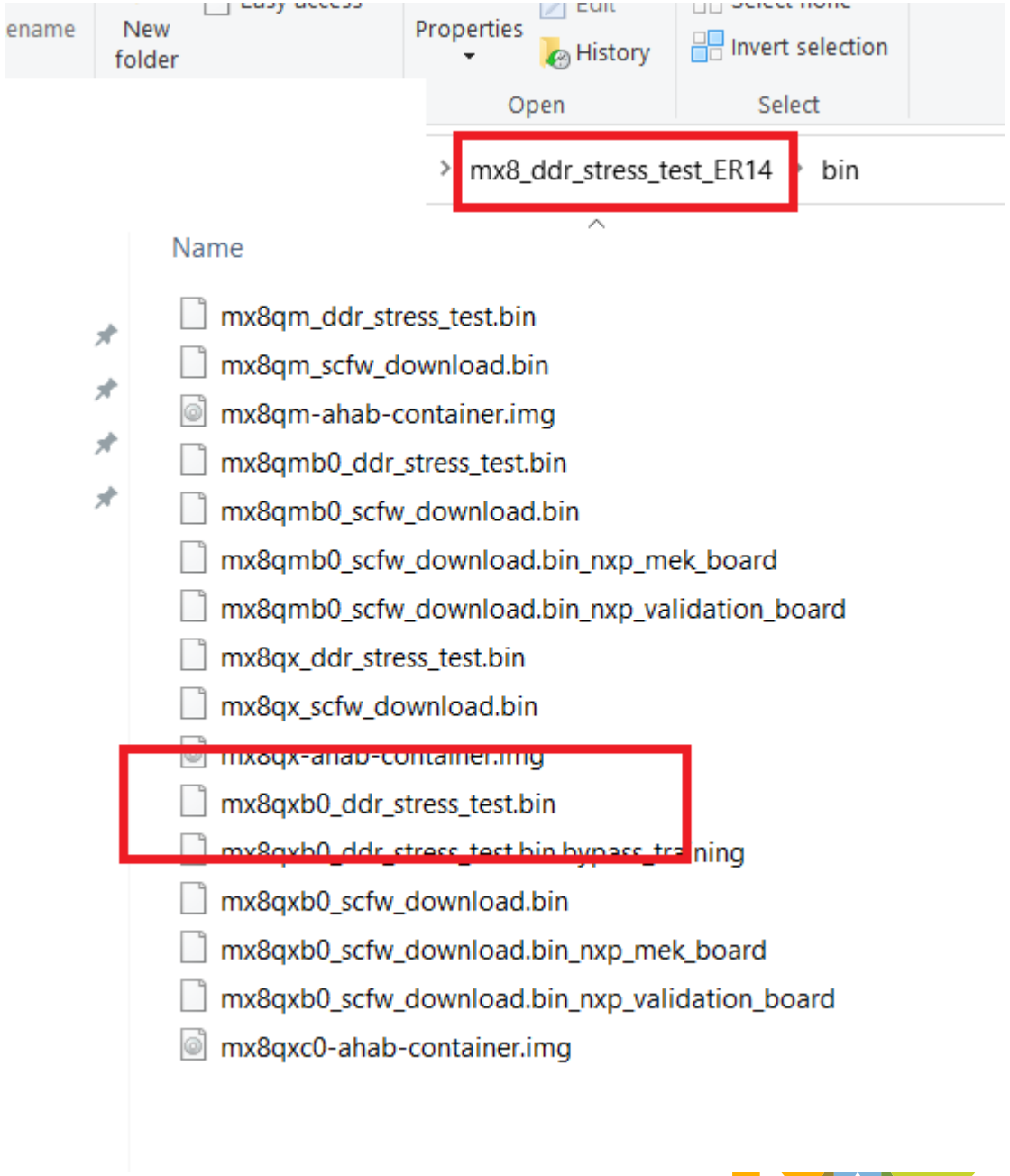
Test(cont.)

Build:

make SOC=iMX8QX flash_ddrstress REV=C0

flash.bin is the ddr stress test flash.bin

imx-mkimage/iMX8QX/
|-- bl31.bin ->
|-- **flash.bin**
|-- mkimage_fit_atf.sh
|-- mx8qxb0_ddr_stress_test.bin
|-- mx8qxc0-ahab-container.img
|-- scfw_tcm.bin



Test(cont.)

ddr stress test:

1. connect uart and usb port
2. uuu flash.bin(imx8qxpc0_er14.bin-flash_ddrstress)
3. send 81 00 00 00 00 to initial the ddr stress test
4. send 02 08 00 00 00 00 00 00 00 aa to start the stress test
   or sent 02 08 00 00 00 00 01 00 00 aa to start Over Night Test

   Note: Please add space between every 8bit hex value for the SerialTool
   81 00 00 00 00
   81[sp]00[sp] 00[sp] 00[sp] 00

Test(cont.)

change the uart port:
The following patch is to change to uart2 from uart0.
Details, please read the ddr stress test tool guide.

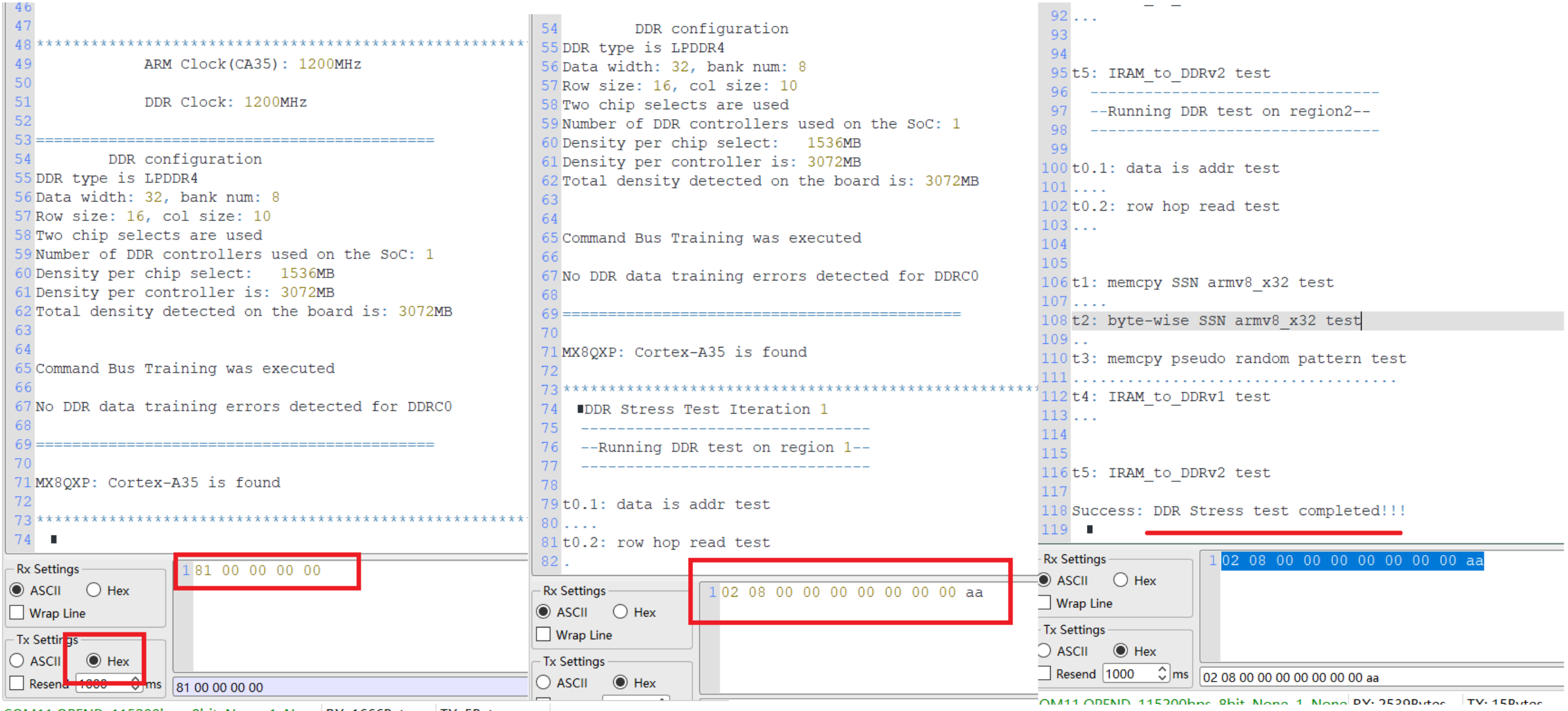
The uart2 is on base board.

```
--- lf-5.10.52-2.1.0/scfw/platform/board/mx8qx_mek/dcd/imx8qx_dcd_1.2GHz.cfg.orig       2022-02-14
16:41:25.340682187 +0800
+++ lf-5.10.52-2.1.0/scfw/platform/board/mx8qx_mek/dcd/imx8qx_dcd_1.2GHz.cfg    2022-02-14
16:41:44.124507479 +0800
@@ -360,6 +360,9 @@ DATA 4   DDR_PHY_DQSDR0_0  0x20188005
 DATA 4   DDR_PHY_DQSDR1_0  0xA8AA0000
 DATA 4   DDR_PHY_DQSDR2_0  0x00070200

+//Change ddr stress test uart
+DATA 4  DDR_PHY_BISTUDPR_0  2
+
 //Enable QCHAN HWidle
 DATA 4   0x41c80504  0x400
```

Test(cont.)

snapshot:



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