i.MX6D/Q/S Core Board User Guide

V0.1, 09/20/2012

Revision History:

Rev. Number	date	Changes
V0.1	09/20/2012	Initialization

Contents

1.1 About This Document.

These documents describe the function of i.MX6 core board and debug board, and will guide customer to use this board for their product developing.

1.1.1 Audience

This guide is intended to be used by board-level product designers and product software developers. This guide assumes that the reader has a background in computer engineering and/or software engineering and understands concepts of digital system design, microprocessor architecture, Input / Output (I/O) devices and industry standard communication and device interface protocols.

1.1.2 Objective

Some customers want to speed up their product development, and they want to focus on software development only. This Core board can help customer on this. Customers only need to focus on their external device drivers and application, no need to care about minimal system. It will shorten the time to market.

1.2 Core Board introduction

For customer, they need to design a main board using 2 layers or 4 layers according to their system requirement.

1.2.1 Core Board overview

-- 8 layers

-- Board Size: 1000(mm) x750(mm)

-- Two 2x40 pins connectors, total PINOUT numbers are 160

-- The pitch of connector is 2mm

-- Debug Board Connector

-- Power Connector

-- Boot Source Connector

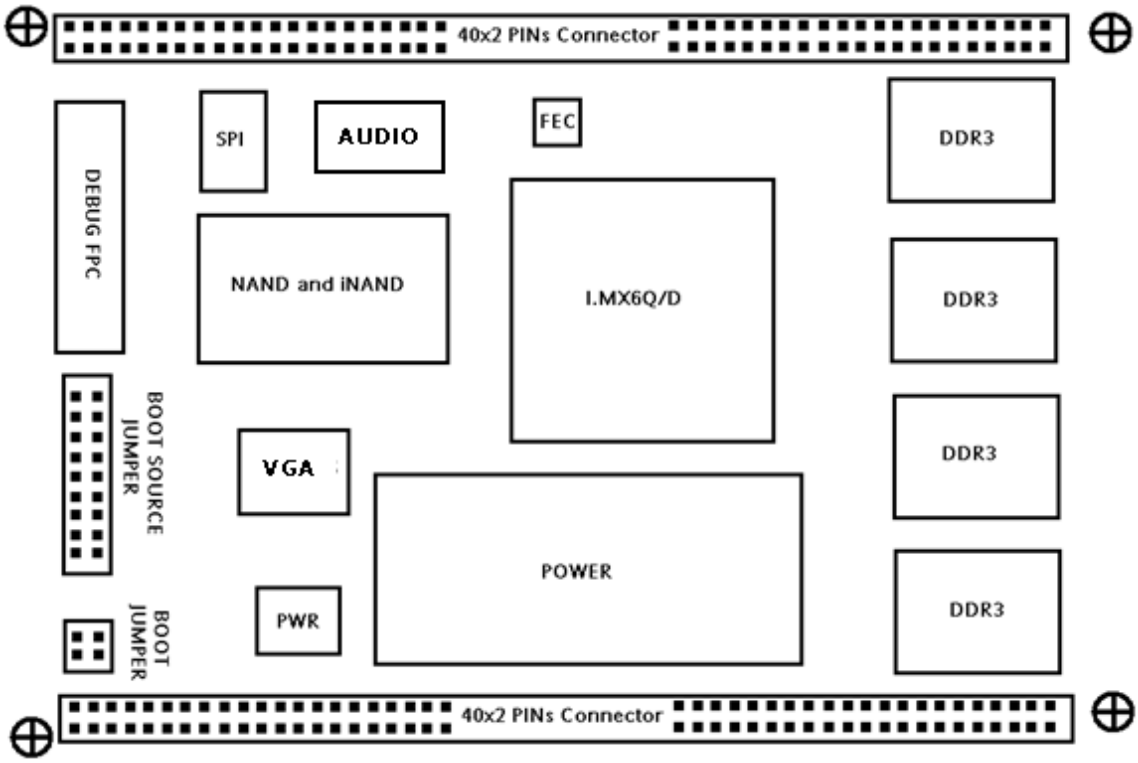
-- Boot mode Connector

-- 4 Fixing holes

-- LED indicate for Power, run mode indicated

1.2.2 Board Layout

For Board layout, we place all components with BGA package in top layer, and place resistors can capacitance on bottom side. It's easy for manufacturer.And it could save the BOM cost.



1.2.3 Support Features

Features	Comments
i.MX6S/D/Q/L	Support i.MX6D/Q with 64 bit DDR3, i.MX6S with 32bit
DDR3	Up to 2GB
Power	Discrete Power
LVDS	2 LVDS port with 4 pairs and one clock
HDMI	HDMI 1.4a
TVOUT	VGA output with 1080P resolution
FEC	10/100M Ethernet with FEC
Boot Source	SPI-NOR ,SD1/SD2/SD3, NAND,SATA
Audio Codec	Analog L/R output
MIC IN	Yes
USB OTG	OTG support
USB HOST	1 USB HOST Port
I2C	3 I2C port
SPI	1 SPI port with 2 chip select
CAN	1 CAN BUS

DUAL-CHANNEL LVDS	Yes, need to MUX with I2C and UART
CSI	1 CSI port with 8 bit data bus width
GPIO	7 GPIO
Debug UART	Yes
APP UART	4 application UART
JTAG	Support JTAG debug via Debug board.
SATA	Yes
PCIE	Yes
I2S	1 Port
SPDIF TX	Yes
SDHC	2 Port SDHC, 1port supports 4bit, another supports 8bit.
PWM	1
CLK Out	2
NAND	Yes

1.2.4 Boot Source definition

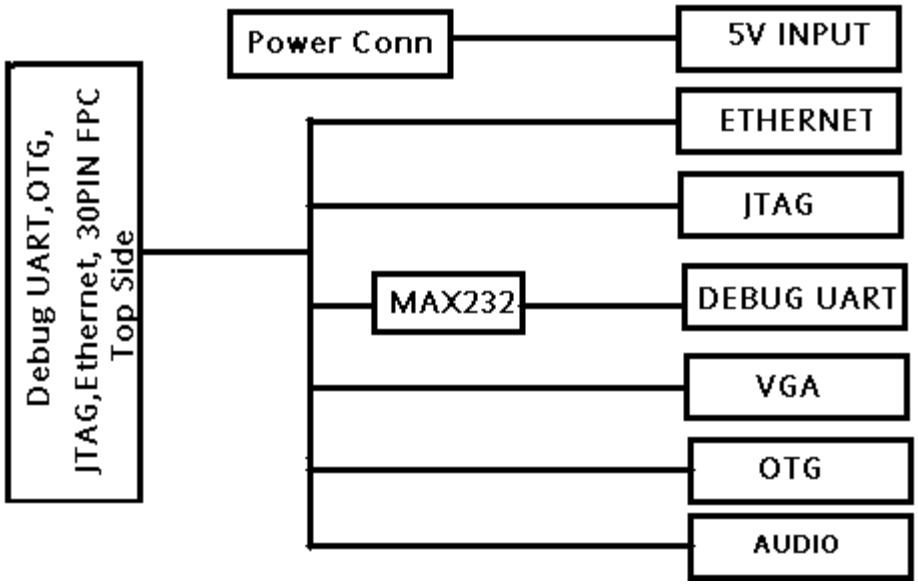
PIN#	NAME	SPI-NOR	SD1@4Bit	SD3@8bit	eMMC@SD4	NAND	SATA
1-2	BOOT_CFG1[7]	0	0	0	0	1	0
3-4	BOOT_CFG1[6]	0	1	1	1	0	0
5-6	BOOT_CFG1[5]	1	0	1	1	0	1
7-8	BOOT_CFG1[4]	1	0	0	0	0	0
9-10	BOOT_CFG2[6]	0	0	1	1	0	0
11-12	BOOT_CFG2[5]	0	1	0	0	0	0
13-14	BOOT_CFG2[4]	0	0	1	1	0	0
15-16	BOOT_CFG2[3]	0	0	0	1	0	0

1.2.5 Boot Mode

Boot Mode	MODE1	MODE0
Fuses	0	0
Serial	0	1
Straps	1	0
Reserved	1	1

1.2.6 Debug Board

There is a 40 PIN FPC connector on Core board; we could connect core board to debug board via 40 PINs FPC.



With debug board, customer can do basic evaluation for MX6x Core board. Following features can be support on debug Board.

Module Name	Function
Debug UART	To print debug info
JTAG	DDR Stress test
VGA	Display port up to 1080P
OTG	Image update
Power	5V Input
Ethernet	NFS, Streaming playback
AUDIO	Support Head Phone and MIC Phone

1.2.7 Connector Spec

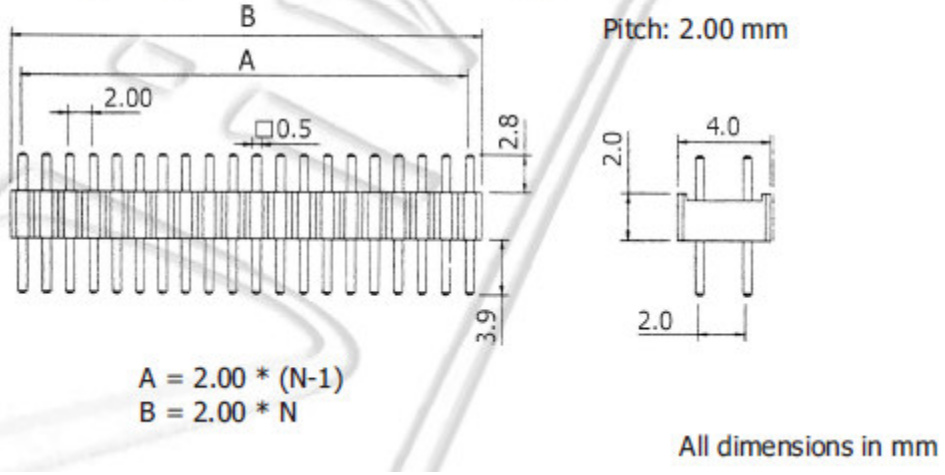
Ninigi DATASHEET

ZL303-2X SERIES 2.00 MM (0.079") PIN HEADER DUAL ROW

Specification:

1) To +105° Current Rate: 3 A
2) Dielectric Withstanding Voltage: 500 VAC
3) Insulation Resistance: 5000 MΩ
4) Temperature: -55°C ~ 105°C
5) Insulator: Thermoplastic (UL94V-0)
6) Contact: Copper Alloy

Series No.	No. of Contact (N)	Contact Plating
ZL303-2X20P-T	2 x 20	Tin
ZL303-2X20P	2 x 20	Gold
ZL303-2X40P-T	2 x 40	Tin
ZL303-2X40P	2 x 40	Gold



1.3 Core Board PINOUT definition(J5)

PIN#	Module	Sub Module	PIN Name	Direction	Voltage(V)
1	**POWER**	**5V**	5V_INPUT	INPUT	5
2			5V_INPUT	INPUT	5
3			5V_INPUT	INPUT	5
4			5V_INPUT	INPUT	5
5		**GND**	GND	N/A	0
6			GND	N/A	0
7			GND	N/A	0
8			GND	N/A	0
9		**3.3V**	3V3	OUTPUT	3.3
10			3V3	OUTPUT	3.3
11			GND	N/A	0
12			GND	N/A	0
13		**1.8V**	1V8	OUTPUT	1.8
14			1V8	OUTPUT	1.8
15	**SDHC**	**SDHC1**	SD1_CMD	I/O	3.3
16			SD1_CLK	OUTPUT	3.3
17			SD1_DATA0	I/O	3.3
18			SD1_DATA1	I/O	3.3
19			SD1_DATA2	I/O	3.3
20			SD1_DATA3	I/O	3.3
21			SD1_CD#	INPUT	3.3
22			SD1_WP	INPUT	3.3
23			GND	N/A	0
24			GND	N/A	0
25		**SDHC3**	SD3_CMD	I/O	3.3
26			SD3_CLK	OUTPUT	3.3
27			SD3_DATA0	I/O	3.3

28			SD3_DATA1	I/O	3.3
29			SD3_DATA2	I/O	3.3
30			SD3_DATA3	I/O	3.3
31			SD3_DATA4	I/O	3.3
32			SD3_DATA5	I/O	3.3
33			SD3_DATA6	I/O	3.3
34			SD3_DATA7	I/O	3.3
35			SD3_CD#	INPUT	3.3
36			SD3_WP	INPUT	3.3
37	**Digital Audio**	**I2S**	AUD4_RXC	INPUT	3.3
38			AUD4_RXFS	INPUT	3.3
39			AUD4_RXD	INPUT	3.3
40			AUD4_TXFS	OUTPUT	3.3
41			AUD4_TXD	OUTPUT	3.3
42			AUD4_TXC	OUTPUT	3.3
43			GND	N/A	0
44			I2S_MCLK	INPUT	3.3
45	**CSPI**	**SPI2**	CSPI2_SSS1	OUTPUT	3.3
46			CSPI2_SCLK	OUTPUT	3.3
47			CSPI2_SSS0	OUTPUT	3.3
48			CSPI2_MISO	INPUT	3.3
49			CSPI2_MOSI	OUTPUT	3.3
50	**RESET**	**RESET**	SYS_POR#	INPUT	3.3
51	**FEC**	**LED**	FEC_LED1	OUTPUT	3.3
52			FEC_LED2	OUTPUT	3.3
53	**APP UART**	**UART2**	UART2_TXD	OUTPUT	3.3
54			UART2_RXD	INPUT	3.3
55		**UART3**	UART3_TXD	OUTPUT	3.3
56			UART3_RXD	INPUT	3.3
57	**TVOUT**	**VGA**	VGA_BLUE	OUTPUT	3.3
58			VGA_GREEN	OUTPUT	3.3
59			VGA_RED	OUTPUT	3.3
60			GND	N/A	0
61			VGA_HSYNC	OUTPUT	5
62			VGA_VSYNC	OUTPUT	5
63			DDC_SDA	I/O	5
64			DDC_SCL	I/O	5
65			5V_VGA	OUTPUT	5
66			GND	N/A	0
67	**Analog AUDIO**	**MIC phone**	AGND	N/A	0
68			MIC	INPUT	N/A
69		**Headphone**	HP_L	OUTPUT	N/A
70			HP_R	OUTPUT	N/A
71	**I2C**	**I2C2**	I2C2_SDA	I/O	3.3
72			I2C2_SCL	I/O	3.3
73	**Debug UART**	**UART1**	UART1_TXD	OUTPUT	3.3
74			UART1_RXD	INPUT	3.3
75	**ETHERNET**	**FEC**	FEC_TX+	OUTPUT	3.3
76			FEC_TX-	OUTPUT	3.3
77			FEC_RX+	INPUT	3.3

78			FEC_RX-	INPUT	3.3
79			FEC_PWR	OUTPUT	3.3
80			GND	N/A	0

1.4 Core Board PINOUT definition(J6)

PIN#	Module	Sub Module	PIN Name	Direction	Voltage(V)
1	**SATA**	**SATA**	SATA_RXP	INPUT	2.5
2			SATA_RXM	INPUT	2.5
3			SATA_TXM	INPUT	2.5
4			SATA_TXP	INPUT	2.5
5			GND	N/A	0
6	**USB**	**OTG**	GND	N/A	0
7			USB5V_OTG	INPUT	5
8			USBOTG_DN	I/O	5
9			USBOTG_DP	I/O	5
10			GND	N/A	0
11			USBOTG_OC	INPUT	5
12			USBOTG_PWR	OUTPUT	5
13		**USB HOST**	USB5V	INPUT	5
14			USB_H1_DN	I/O	5
15			USB_H1_DP	I/O	5
16			GND	N/A	0
17			USB_HUB_RST#	OUTPUT	3.3
18			USB5V_PWR	OUTPUT	5
19	**PCIE**	**PCIE**	PCIE_RXM	INPUT	3.3
20			PCIE_RXP	INPUT	3.3
21			PCIE_TXM	OUTPUT	3.3
22			PCIE_TXP	OUTPUT	3.3
23			PCIE_CLK_N	OUTPUT	3.3
24			PCIE_CLK_P	OUTPUT	3.3
25			GND	N/A	0
26			GND	N/A	0
27	**APP UART**	**UART4**	UART4_TXD	OUTPUT	3.3
28			UART4_RXD	INPUT	3.3
29		**UART5**	UART5_TXD	OUTPUT	3.3
30			UART5_RXD	INPUT	3.3
31	**I2C**	**I2C3**	I2C3_SDA	I/O	3.3
32			I2C3_SCL	I/O	3.3
33	**GPIO**	**GPIO7**	GP7_11	I/O	3.3
34			GP7_13	I/O	3.3
35		**GPIO4**	GP4_14	I/O	3.3
36			GP4_15	I/O	3.3
37	**DISPLAY**	**HDMI**	GND	N/A	0
38			GND	N/A	0
39			HDMI_CLKM	OUTPUT	3.3
40			HDMI_CLKP	OUTPUT	3.3
41			HDMI_D0M	OUTPUT	3.3
42			HDMI_D0P	OUTPUT	3.3
43			HDMI_D1M	OUTPUT	3.3
44			HDMI_D1P	OUTPUT	3.3

45			HDMI_D2M	OUTPUT	3.3
46			HDMI_D2P	OUTPUT	3.3
47			HDMI_HPD	INPUT	3.3
48			HDMI_DDCCEC	INPUT	3.3
49	**CAMERA**	**CSI0**	CSI0_PIXCLK	OUTPUT	3.3
50			CSI0_HSYNC	OUTPUT	3.3
51			CSI0_ENABLE	OUTPUT	3.3
52			CSI0_VSYNC	OUTPUT	3.3
53			CSI0_DAT12	I/O	3.3
54			CSI0_DAT13	I/O	3.3
55			CSI0_DAT14	I/O	3.3
56			CSI0_DAT15	I/O	3.3
57			CSI0_DAT16	I/O	3.3
58			CSI0_DAT17	I/O	3.3
59			CSI0_DAT18	I/O	3.3
60			CSI0_DAT19	I/O	3.3
61	**I2C**	**I2C1**	I2C1_SDA	I/O	3.3
62			I2C1_SCL	I/O	3.3
63			GND	N/A	0
64	**LVDS**	**LVDS0**	GND	N/A	0
65			LVDS0_TX0_N	OUTPUT	3.3
66			LVDS0_TX0_P	OUTPUT	3.3
67			LVDS0_TX1_N	OUTPUT	3.3
68			LVDS0_TX1_P	OUTPUT	3.3
69			LVDS0_TX2_N	OUTPUT	3.3
70			LVDS0_TX2_P	OUTPUT	3.3
71			LVDS0_CLK_N	OUTPUT	3.3
72			LVDS0_CLK_P	OUTPUT	3.3
73			LVDS0_TX3_N	OUTPUT	3.3
74			LVDS0_TX3_P	OUTPUT	3.3
75	**PWM**	**PWM2**	PWM2	OUTPUT	3.3
76	**SPDIF**	**SPDIF**	SPDIF_OUT1	OUTPUT	3.3
77	**CLK OUT**	**CLKO1**	CLKO1	OUTPUT	3.3
78		**CLKO2**	CLKO2	OUTPUT	3.3
79	**CAN BUS**	**CAN1**	CAN1_TX	OUTPUT	3.3
80			CAN1_RX	INPUT	3.3

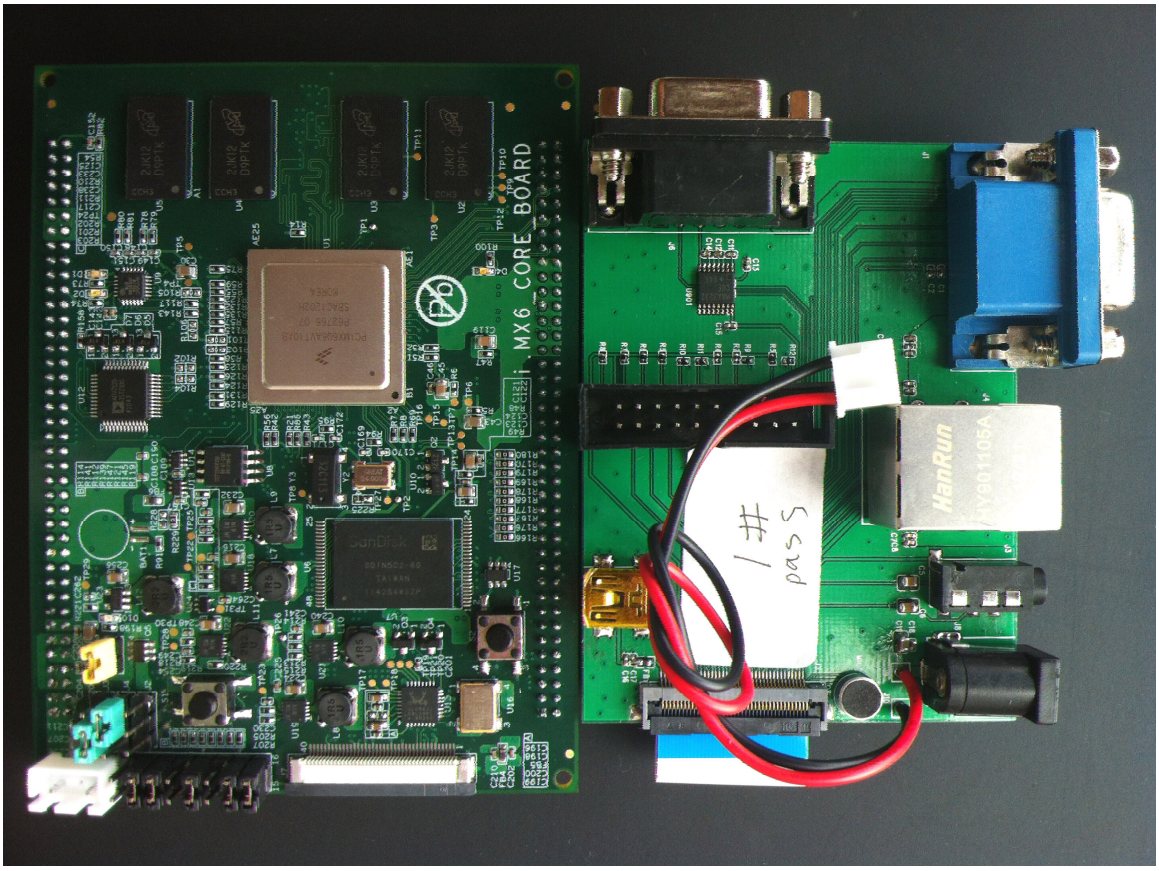
1.5 Debug Connector PINOUT definition(J7)

PIN#	Module	PIN Name	Direction	Voltage(V)
1	**OTG**	USB5V_OTG	INPUT	5
2		GND	N/A	0
3		USBOTG_DN	I/O	5
4		USBOTG_DP	I/O	5
5		GND	N/A	0
6	**JTAG**	VCC_JTAG	N/A	3.3
7		JTAG_TRSTB	INPUT	3.3

8		JTAG_TDI	I/O	3.3
9		JTAG_TMS	I/O	3.3
10		JTAG_TCK	I/O	3.3
11		JTAG_TDO	I/O	3.3
12		JTAG_MOD	I/O	3.3
13		JTAG_RST#	INPUT	3.3
14		GND	N/A	0
15	**POWER**	3V3	OUTPUT	3.3
16	**Debug UART**	UART1_TXD	OUTPUT	3.3
17		UART1_RXD	INPUT	3.3
18	**VGA**	5V_VGA	N/A	5
19		DDC_SCL	I/O	5
20		DDC_SDA	I/O	5
21		VGA_VSYNC	OUTPUT	5
22		VGA_HSYNC	OUTPUT	5
23		GND	N/A	0
24		VGA_RED	OUTPUT	5
25		GND	N/A	0
26		VGA_GREEN	OUTPUT	5
27		GND	N/A	0
28		VGA_BLUE	OUTPUT	5
29		GND	N/A	0
30	**FEC**	FEC_TX+	OUTPUT	3.3
31		FEC_TX-	OUTPUT	3.3
32		GND	N/A	0
33		FEC_RX+	INPUT	3.3
34		FEC_RX-	INPUT	3.3
35		GND	N/A	0
36		FEC_PWR	N/A	3.3
37	**AUDIO**	AGND	N/A	0
38		MIC	INPUT	3.3
39		HP_L	OUTPUT	3.3
40		HP_R	OUTPUT	3.3

1.6 How to 2nd LVDS or Dual-Channel LVDS

This Board can support 2nd LVDS interface, it needs to MUX with I2C and UART function.



勤为技术有限公司
QINWEI TECHNOLOGY CO., LIMITED
中国深圳南山科技园中区深南花园C座28B室邮编：518057
Rm 28B, C Bldg., Shennan Garden, Hi-Tech Park, Nanshan, Shenzhen 518057, P.R. China
电话/Tel: +86 755 2697 8597
传真/Fax: +86 755 2695 5058
网站/Website: http://www.qwtek.com
技术支持： steven@qwtek.com +86 186 6580 9652
Technical Support: steven@qwtek.com +86 186 6580 9652
市场联络： horsepower@qwtek.com +86 159 1990 0820
Marketing Contact: horsepower@qwtek.com +86 159 1990 0820