Agilent Technologies

PCI Express Test Report

Overall Result: PASS

Test Configuration Details	
Device Description	
Device ID	Device 1
Preset Type	None
Test Session Details	
Infiniium SW Version	04.20.0008
Infiniium Model Number	DSO91304A
Infiniium Serial Number	MY50140158
Application SW Version	3.34
Debug Mode Used	No
Last Test Date	2015-01-28 13:44:03 UTC +02:00

Summary of Results

Test Statistics	
Failed	0
Passed	16
Total	16

Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	System Board Tx, Unit Interval (PCIE 2.0, 5.0 GT/s)	200.0110 ps	40.8 %	199.9400 ps <= VALUE <= 200.0600 ps
✓	0	1	System Board Tx, Template Tests (PCIE 2.0, 5.0 GT/s)	Pass	100.0 %	Pass/Fail
✓	0	1	System Board Tx, Peak Differential Output Voltage (Transition) (PCIE 2.0, 5.0 GT/s)	467.8 mV	18.6 %	300.0 mV <= VALUE <= 1.2000 V
✓	0	1	System Board Tx, Peak Differential Output Voltage (Non Transition)(PCIE 2.0, 5.0 GT/s)	923.2 mV	30.8 %	300.0 mV <= VALUE <= 1.2000 V
✓	0	1	System Board Tx, Eye-Width with crosstalk (PCIE 2.0, 5.0 GT/s)	133.56 ps	40.6 %	VALUE >= 95.00 ps
✓	0	1	System Board Tx, RMS Random Jitter with crosstalk (PCIE 2.0, 5.0 GT/s)	3.006 ps	93.7 %	VALUE <= 48.000 ps
✓	0	1	System Board Tx, Maximum Deterministic Jitter with crosstalk (PCIE 2.0, 5.0 GT/s)	24.148 ps	57.6 %	VALUE <= 57.000 ps
✓	0	1	System Board Tx, Total Jitter at BER-12 with crosstalk (PCIE 2.0, 5.0 GT/s)	66.443 ps	36.7 %	VALUE <= 105.000 ps
✓	0	1	System Board Tx, Eye-Width without crosstalk (PCIE 2.0, 5.0 GT/s)	133.56 ps	23.7 %	VALUE >= 108.00 ps
✓	0	1	System Board Tx, RMS Random Jitter without crosstalk (PCIE 2.0, 5.0 GT/s)	3.006 ps	93.7 %	VALUE <= 48.000 ps
✓	0	1	System Board Tx, Maximum Deterministic Jitter without crosstalk (PCIE 2.0, 5.0 GT/s)	24.148 ps	45.1 %	VALUE <= 44.000 ps
✓	0	1	System Board Tx, Total Jitter at BER-12 without crosstalk (PCIE 2.0, 5.0 GT/s)	66.443 ps	27.8 %	VALUE <= 92.000 ps
✓	0	1	Reference Clock, High frequency > 1.5MHz RMS Jitter (Common Clk) (PCIE 2.0, 5.0 GT/s)	1.77 ps	42.9 %	VALUE <= 3.10 ps
✓	0	1	Reference Clock, Low frequency 10kHz - 1.5MHz RMS Jitter (Common Clk) (PCIE 2.0, 5.0 GT/s)	480 fs	84.0 %	VALUE <= 3.00 ps
✓	0	1	Reference Clock, High frequency > 1.5MHz RMS Jitter (Data Clk) (PCIE 2.0, 5.0 GT/s)	2.05 ps	48.8 %	VALUE <= 4.00 ps
✓	0	1	Reference Clock, Low frequency 10kHz - 1.5MHz RMS Jitter (Data Clk) (PCIE 2.0, 5.0 GT/s)	460 fs	93.9 %	VALUE <= 7.50 ps

Report Detail

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✓System Board Tx, Unit Interval (PCIE 2.0, 5.0 GT/s)

Reference: This test is not required. It is informative only.

Test Summary: Pass | Test Description: | A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered TX UI is reported here. The UI range is NOT specified for this test point. It is provided here as informative data only.

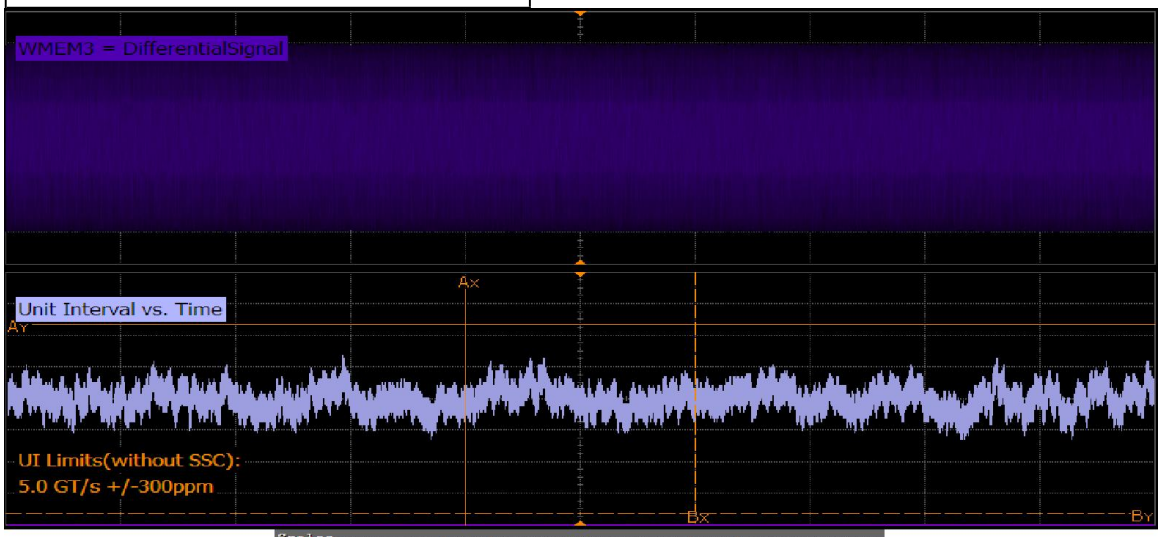
Pass Limits: [199.9400 ps to 200.0600 ps] **Mean UI (ps)** 200.0110 ps

Result Details

Data Lane	(no value)	**Note:**	Non-SSC Limits Used: 5.0 GT/s +/-300ppm	**#3500 UI Blocks Measured**	1.596401 M		
Min UI	199.9870 ps	**Max UI**	200.0400 ps	**Mean UI**	200.0110 ps	**Worst Case Data Rate**	4.999000199960 Gbits/sec
Mean Data Rate	4.999725015124 Gbits/sec	**Connection Type**	Chan 1(D+),3(D-),2(Clk+),4(Clk-) - Direct Connect				

Trial 1

Trial 1: Mean Data Rate



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✓System Board Tx, Template Tests (PCIE 2.0, 5.0 GT/s)

Reference: PCI Express CEM Specification, Rev 2.0, Section 4.7.6, Figure 4-12

Test Summary: Pass | Test Description: System boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in table 4-15 of section 4.7.6 of the PCI Express Card Electromechanical (CEM) Specification, Rev 2.0, as measured after the connector with an ideal load.

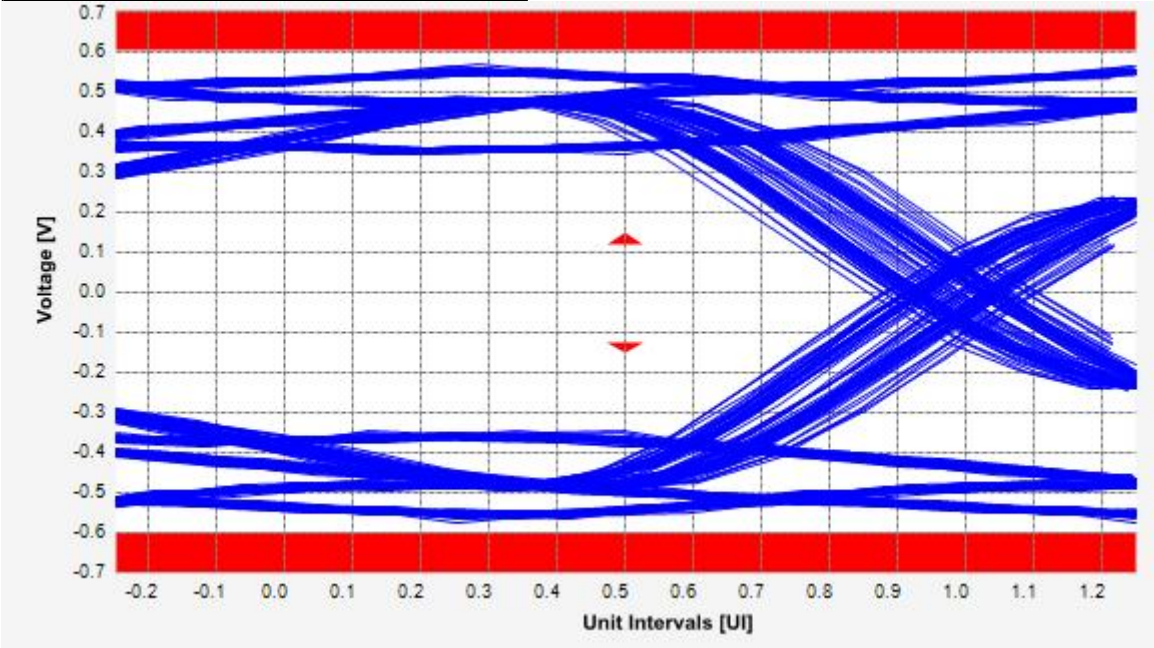
Pass Limits: Pass/Fail | **Total # Failures** Pass

Result Details

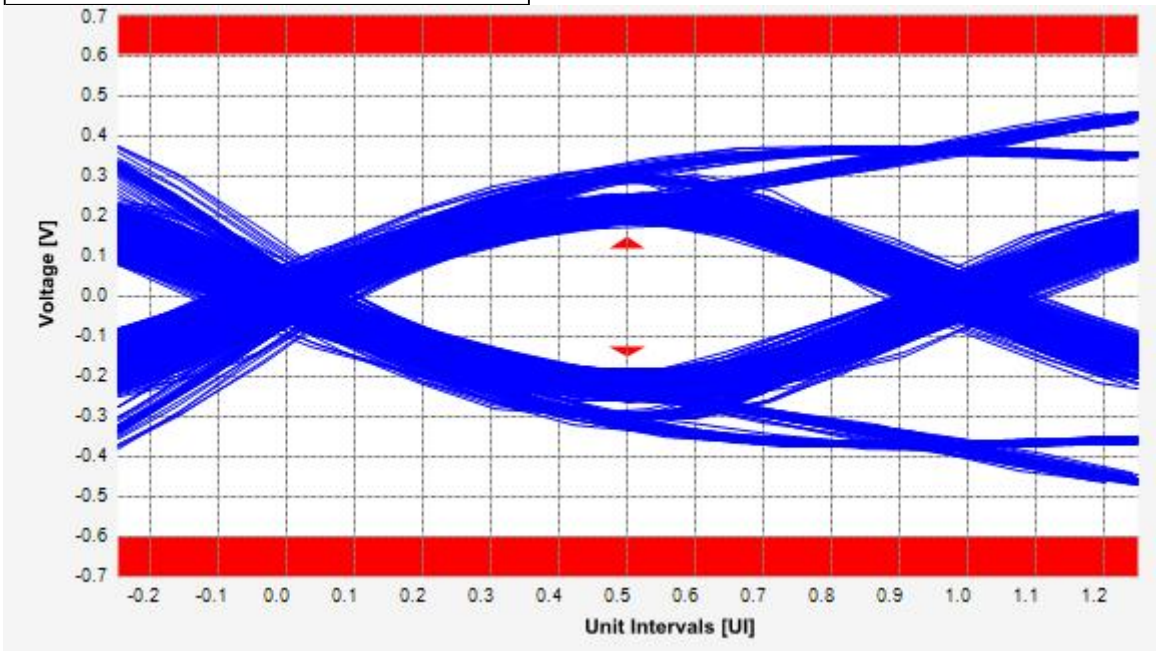
Total #UI Measured	1.600000000 M	**Non-Transition Failures**	0.000	**Transition Failures**	0.000
Non-Transition Eye Diagram	(See image)	**Transition Eye Diagram**	(See image)	**Data Lane**	(no value)
Sample Rate (GSa/s)	40.0				

Trial 1

Trial 1: Non-Transition Eye Diagram



Trial 1: Transition Eye Diagram



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✓System Board Tx, Peak Differential Output Voltage (Transition)(PCIE 2.0, 5.0 GT/s)

Reference: PCI Express CEM Specification, Rev 2.0, Section 4.7.6, Table 4-15

Test Summary: Pass | Test Description: | This test verifies that the Differential Peak Differential Output Voltage is within the allowed range.

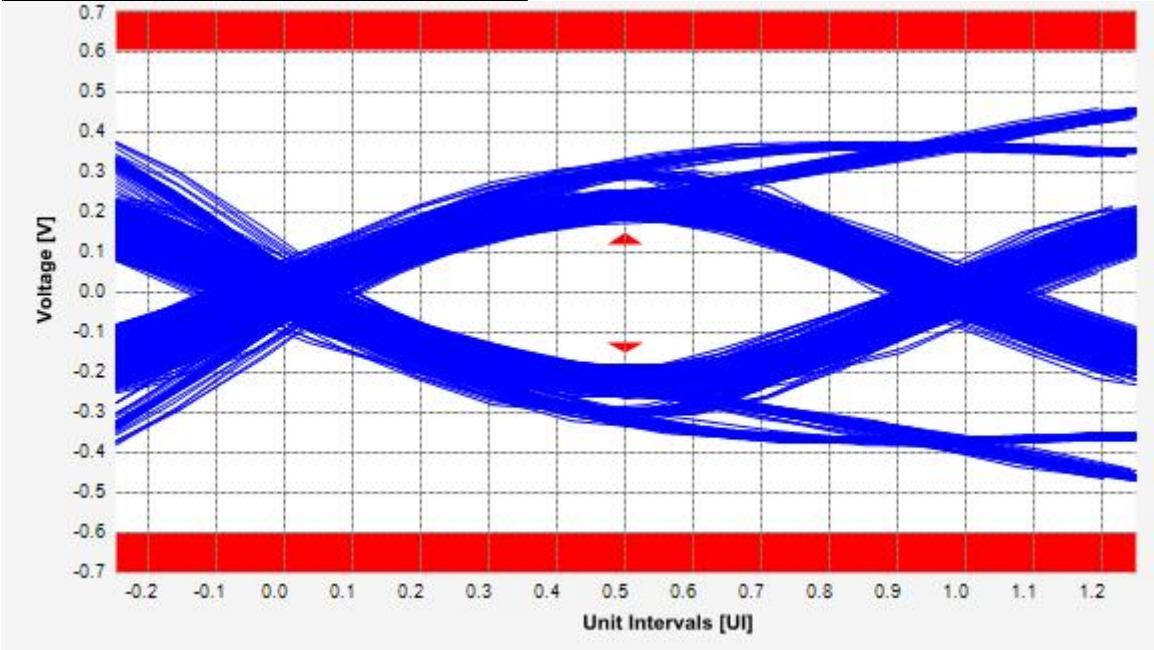
Pass Limits: [300.0 mV to 1.2000 V] **PeakVoltage** 467.8 mV

Result Details

Total #UI Measured	1.600000000 M	**Largest Transition Amplitude (Outer eye)**	798.9 mV		
Smallest Transition Amplitude (Inner eye)	348.0 mV	**Data Lane**	(no value)	**Transition Eye Diagram**	(See image)
Connection Type	Chan 1(D+),3(D-),2(Clk+),4(Clk-) - Direct Connect				

Trial 1

Trial 1: Transition Eye Diagram



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✓System Board Tx, Peak Differential Output Voltage (Non Transition)(PCIE 2.0, 5.0 GT/s)

Reference: PCI Express CEM Specification, Rev 2.0, Section 4.7.6, Table 4-15

Test Summary: Pass | Test Description: This test verifies that the Differential Peak Differential Output Voltage is within the allowed range.

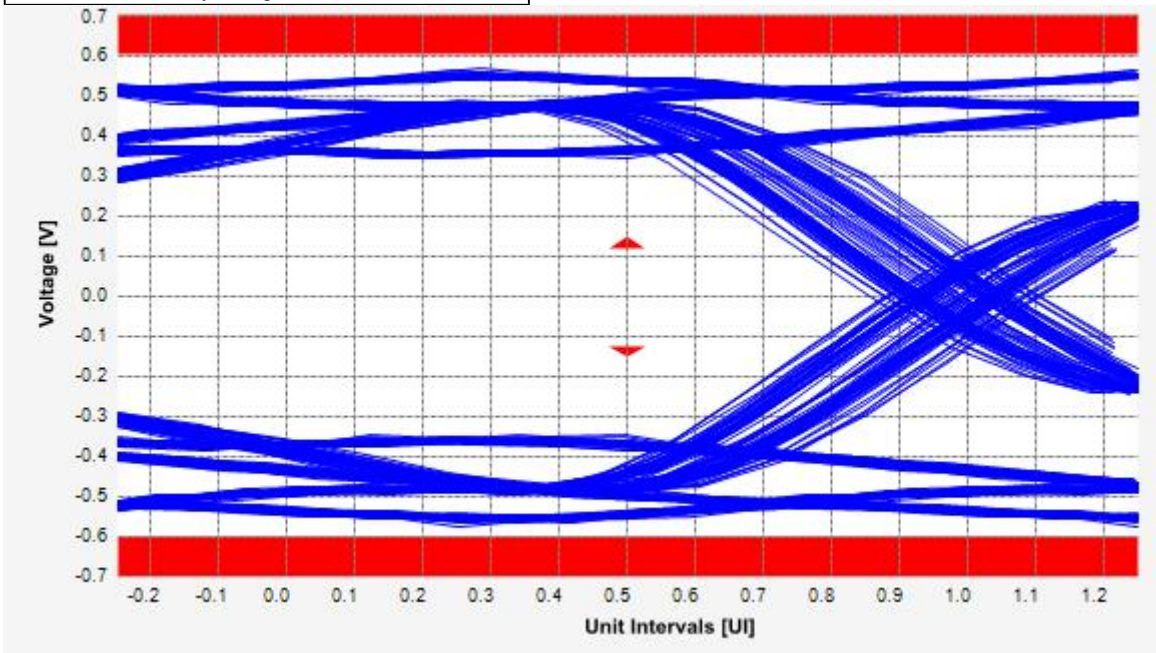
Pass Limits: [300.0 mV to 1.2000 V] **PeakVoltage** 923.2 mV

Result Details

Total #UI Measured	1.600000000 M	**Largest Non Transition Amplitude (Outer eye)**	1.1439 V
Smallest Non Transition Amplitude (Inner eye)	691.5 mV	**Data Lane**	(no value)
Transition Eye Diagram	(See image)	**Connection Type**	Chan 1(D+),3(D-),2(Clk+),4(Clk-) - Direct Connect

Trial 1

Trial 1: Transition Eye Diagram



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✓System Board Tx, Eye-Width with crosstalk (PCIE 2.0, 5.0 GT/s)

Reference: PCI Express CEM Specification, Rev 2.0, Section 4.7.6, Table 4-15

Test Summary: Pass | Test Description: | This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].

Pass Limits: >= 95.00 ps | **Eye-Width** 133.56 ps

Result Details

Total #UI Measured 1.600000000 M | **TJ at BER-12** 66.443 ps

Worst Filter Info PLL Damping Factor = 0.54, PLL Frequency = 16000000Hz | **Worst Transport Delay** 3.0 ns

Data Lane (no value) | **Connection Type** Chan 1(D+),3(D-),2(Clk+),4(Clk-) - Direct Connect

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✓System Board Tx, RMS Random Jitter with crosstalk (PCIE 2.0, 5.0 GT/s)

Reference: This test is not required. It is informative only.

Test Summary: Pass | Test Description: | The RJ(rms) range is NOT specified for this test point. It is provided here as informative data only.

Pass Limits: <= 48.000 ps | **Rj_rms** 3.006 ps

Result Details

Total #UI Measured 1.600000000 M | **Worst Filter Info** PLL Damping Factor = 0.54, PLL Frequency = 16000000Hz

Worst Transport Delay 3.0 ns | **Data Lane** (no value) | **Sample Rate (GSa/s)** 40.0

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✓System Board Tx, Maximum Deterministic Jitter with crosstalk (PCIE 2.0, 5.0 GT/s)

Reference: PCI Express CEM Specification, Rev 2.0, Section 4.7.7, Table 4-16

Test Summary: Pass | Test Description: | System boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in table 4-16 of section 4.7.6 of the PCI Express Card Electromechanical (CEM) Specification, Rev 2.0, as measured after the connector with an ideal load.

Pass Limits: <= 57.000 ps | **Dj_dd** 24.148 ps

Result Details

Total #UI Measured 1.600000000 M | **Worst Filter Info** PLL Damping Factor = 0.54, PLL Frequency = 16000000Hz

Worst Transport Delay 3.0 ns | **Data Lane** (no value) | **Sample Rate (GSa/s)** 40.0

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✓System Board Tx, Total Jitter at BER-12 with crosstalk (PCIE 2.0, 5.0 GT/s)

Reference: PCI Express CEM Specification, Rev 2.0, Section 4.7.2, Table 4-16

Test Summary: Pass | Test Description: | System boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in table 4-16 of section 4.7.6 of the PCI Express Card Electromechanical (CEM) Specification, Rev 2.0, as measured after the connector with an ideal load.

Pass Limits: <= 105.000 ps | **Tj at BER 10E-12** 66.443 ps

Result Details

Total #UI Measured 1.600000000 M | **Worst Filter Info** PLL Damping Factor = 0.54, PLL Frequency = 16000000Hz

Worst Transport Delay 3.0 ns | **Data Lane** (no value) | **Sample Rate (GSa/s)** 40.0

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✓System Board Tx, Eye-Width without crosstalk (PCIE 2.0, 5.0 GT/s)

Reference: PCI Express CEM Specification, Rev 2.0, Section 4.7.6, Table 4-15

Test Summary: Pass | Test Description: | This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].

Pass Limits: >= 108.00 ps | **Eye-Width** 133.56 ps

Result Details

Total #UI Measured 1.600000000 M | **TJ at BER-12** 66.443 ps

Worst Filter Info PLL Damping Factor = 0.54, PLL Frequency = 16000000Hz | **Worst Transport Delay** 3.0 ns

Data Lane	(no value)	Connection Type	Chan 1(D+),3(D-),2(Clk+),4(Clk-) - Direct Connect

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✓System Board Tx, RMS Random Jitter without crosstalk (PCIE 2.0, 5.0 GT/s)

Reference: This test is not required. It is informative only.

Test Summary: Pass | Test Description: | The RJ(rms) range is NOT specified for this test point. It is provided here as informative data only.

Pass Limits:	<= 48.000 ps	Rj_rms	3.006 ps

Result Details

Total #UI Measured	1.600000000 M	Worst Filter Info	PLL Damping Factor = 0.54, PLL Frequency = 16000000Hz
Worst Transport Delay	3.0 ns	Data Lane	(no value)
Sample Rate (GSa/s)	40.0		

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✓System Board Tx, Maximum Deterministic Jitter without crosstalk (PCIE 2.0, 5.0 GT/s)

Reference: PCI Express CEM Specification, Rev 2.0, Section 4.7.6, Table 4-16

Test Summary: Pass | Test Description: | System boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in table 4-16 of section 4.7.6 of the PCI Express Card Electromechanical (CEM) Specification, Rev 2.0, as measured after the connector with an ideal load.

Pass Limits:	<= 44.000 ps	Dj_dd	24.148 ps

Result Details

Total #UI Measured	1.600000000 M	Worst Filter Info	PLL Damping Factor = 0.54, PLL Frequency = 16000000Hz
Worst Transport Delay	3.0 ns	Data Lane	(no value)
Sample Rate (GSa/s)	40.0		

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✓System Board Tx, Total Jitter at BER-12 without crosstalk (PCIE 2.0, 5.0 GT/s)

Reference: PCI Express CEM Specification, Rev 2.0, Section 4.7.2, Table 4-16

Test Summary: Pass | Test Description: | System boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in table 4-16 of section 4.7.6 of the PCI Express Card Electromechanical (CEM) Specification, Rev 2.0, as measured after the connector with an ideal load.

Pass Limits:	<= 92.000 ps	Tj at BER 10-12	66.443 ps

Result Details

Total #UI Measured	1.600000000 M	Worst Filter Info	PLL Damping Factor = 0.54, PLL Frequency = 16000000Hz
Worst Transport Delay	3.0 ns	Data Lane	(no value)
Sample Rate (GSa/s)	40.0		

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✓Reference Clock, High frequency > 1.5MHz RMS Jitter (Common Clk) (PCIE 2.0, 5.0 GT/s)

Reference: PCI Express Base Specification, Rev 3.0, Section 4.3.7.3.3, Table 4-31

Test Summary: Pass | Test Description: | This test verifies that the reference clock TREFCLK-HF-RMS is less than the maximum allowed value.

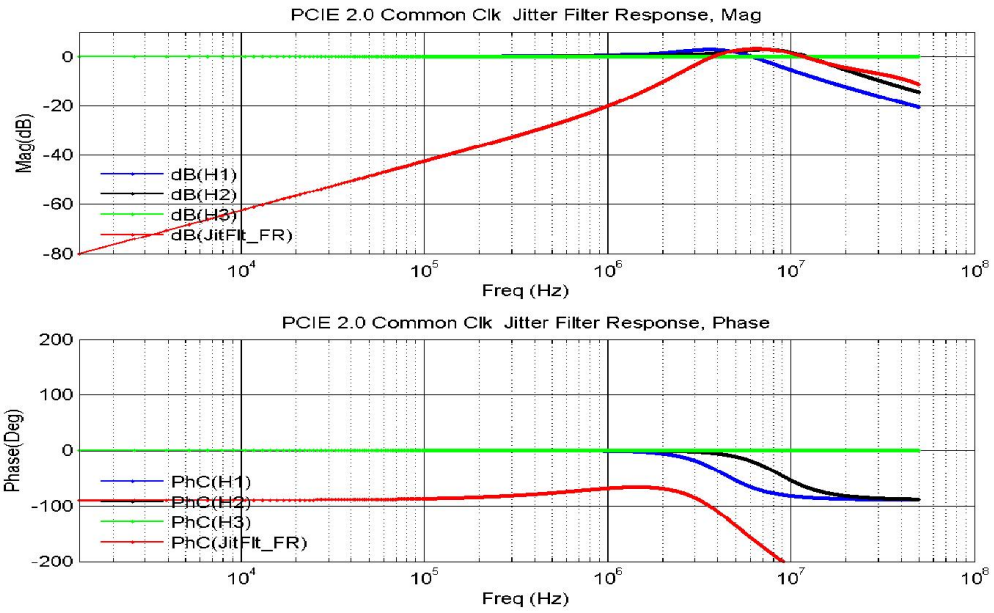
Pass Limits:	<= 3.10 ps	Reference Clock RMS Jitter (TREFCLK-HF-RMS)	1.77 ps

Result Details

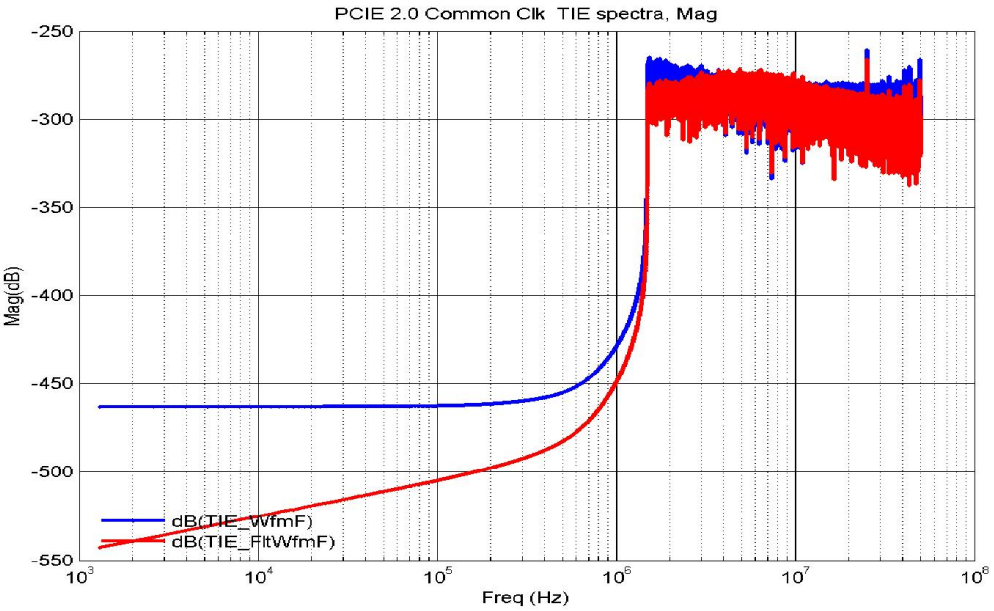
Ref Clock Filter Response	(See image)	Ref Clock TIE Spectra	(See image)	Ref Clock TIE Waveforms	(See image)
Transfer Function	H1: 8MHz, 3.0dB peaking | H2: 16MHz, 3.0dB peaking	Num UIs Processed	95.446 kCycles		
RefClkJit (p-p) filtered	14.48 ps	RefClkJit (rms) filtered	1.77 ps	Connection Type	Chan 2,4 - Direct Connect

Trial 1

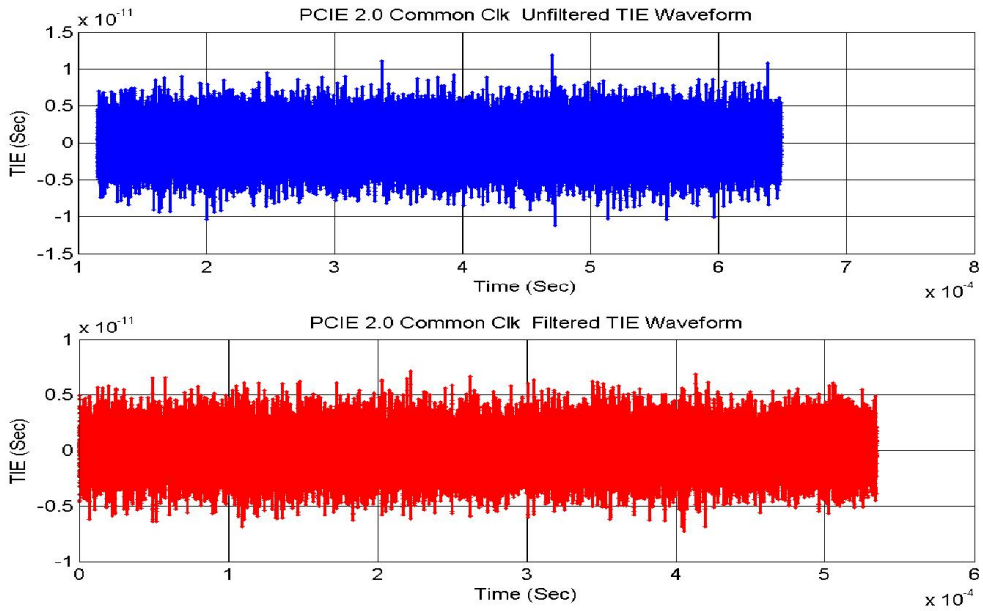
Trial 1: Ref Clock Filter Response



Trial 1: Ref Clock TIE Spectra



Trial 1: Ref Clock TIE Waveforms



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✓Reference Clock, Low frequency 10kHz - 1.5MHz RMS Jitter (Common Clk) (PCIE 2.0, 5.0 GT/s)

Reference: PCI Express Base Specification, Rev 3.0, Section 4.3.7.3.3, Table 4-31

Test Summary: Pass | Test Description: This test verifies that the reference clock TREFCLK-LF-RMS is less than the maximum allowed value.

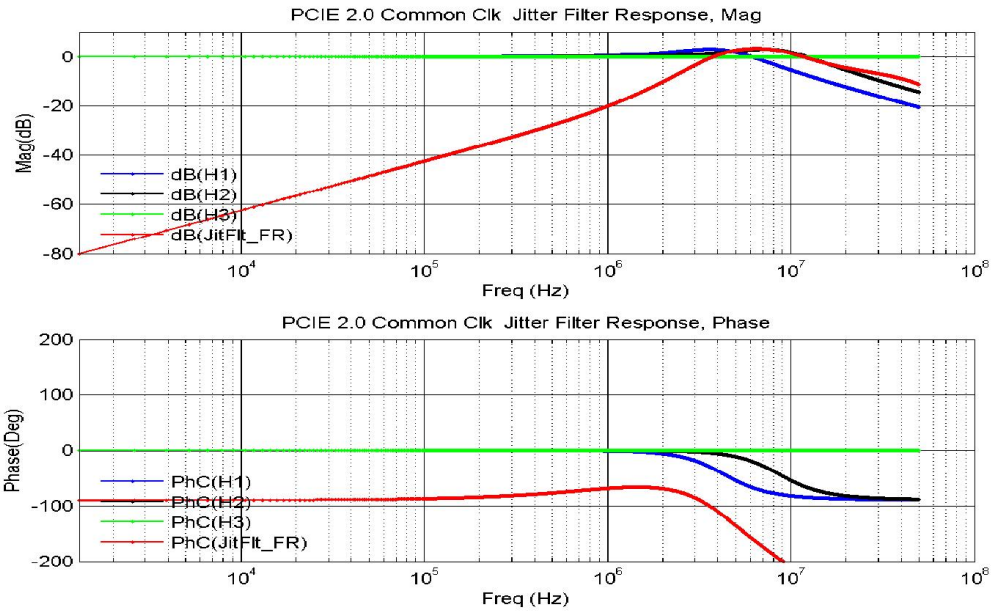
Pass Limits: <= 3.00 ps | **Reference Clock RMS Jitter (TREFCLK-LF-RMS)** 480 fs

Result Details

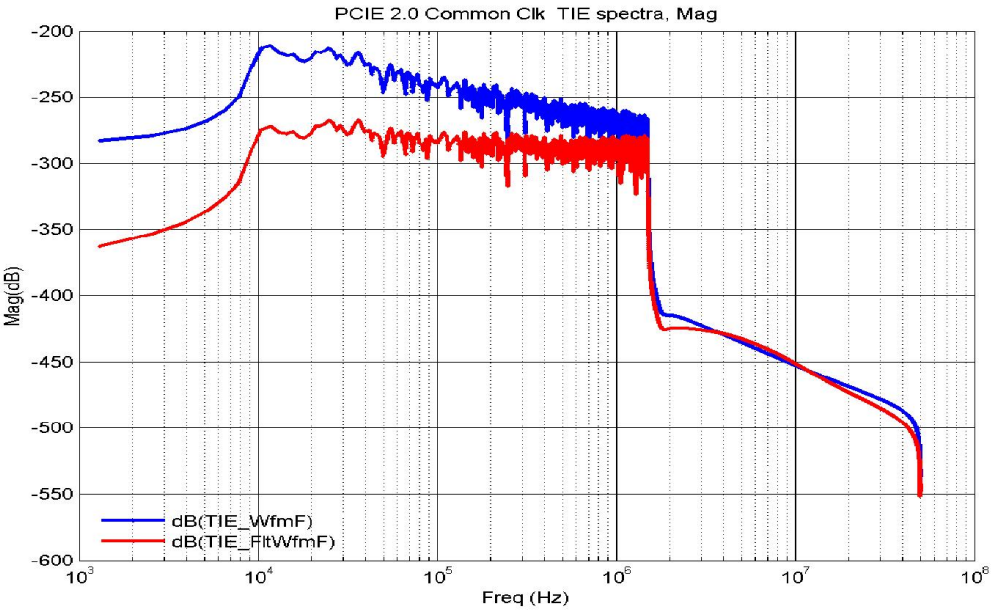
Ref Clock Filter Response	(See image)	**Ref Clock TIE Spectra**	(See image)	**Ref Clock TIE Waveforms**	(See image)
Transfer Function	H1: 8MHz, 3.0dB peaking | H2: 16MHz, 3.0dB peaking	**Num UIs Processed**	95.446 kCycles		
RefClkJit (p-p) filtered	3.74 ps	**RefClkJit (rms) filtered**	480 fs	**Connection Type**	Chan 2,4 - Direct Connect

Trial 1

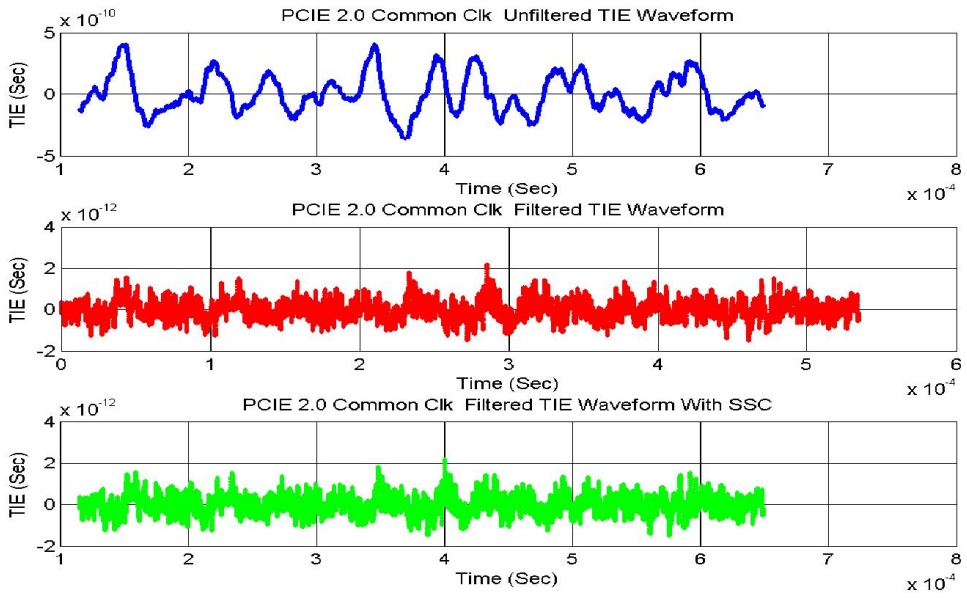
Trial 1: Ref Clock Filter Response



Trial 1: Ref Clock TIE Spectra



Trial 1: Ref Clock TIE Waveforms



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✓ Reference Clock, High frequency > 1.5MHz RMS Jitter (Data Clk) (PCIE 2.0, 5.0 GT/s)

Reference: PCI Express Base Specification, Rev 3.0, Section 4.3.7.3.5, Table 4-33

Test Summary: Pass | Test Description: This test verifies that the reference clock TREFCLK-HF-RMS is less than the maximum allowed value.

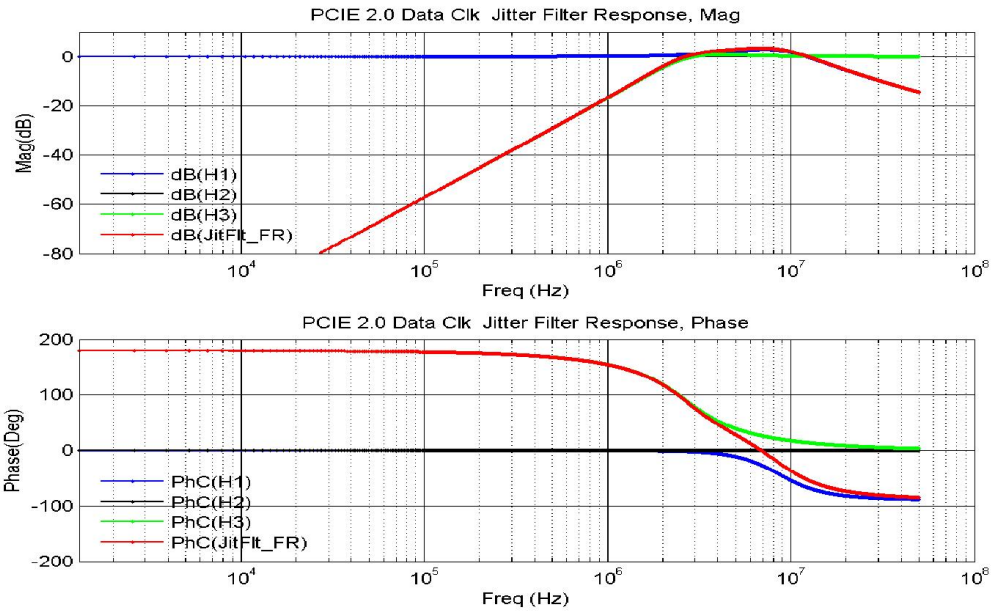
Pass Limits: <= 4.00 ps | **Reference Clock RMS Jitter (TREFCLK-HF-RMS)** 2.05 ps

Result Details

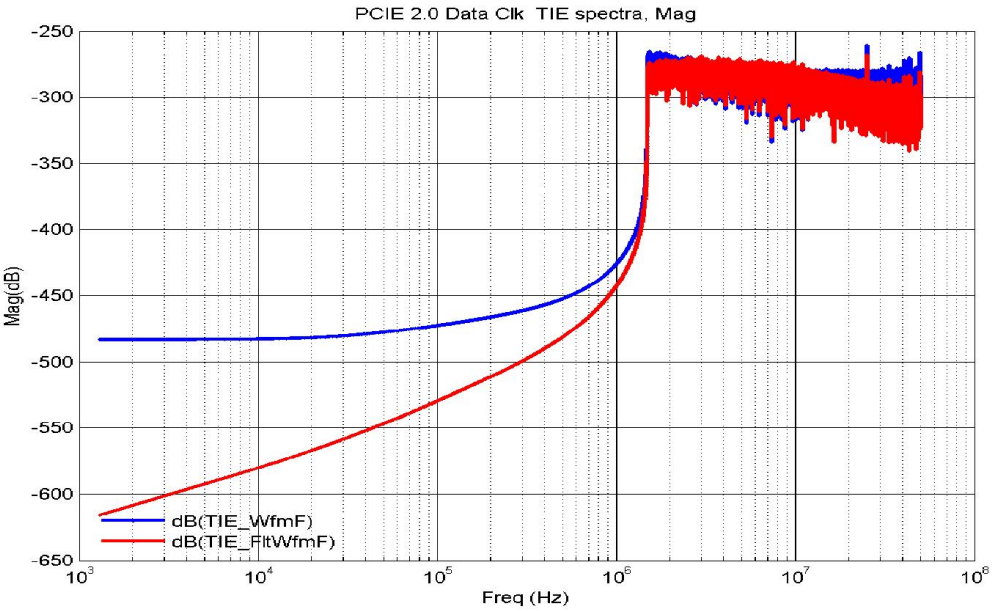
Ref Clock Filter Response	(See image)	**Ref Clock TIE Spectra**	(See image)	**Ref Clock TIE Waveforms**	(See image)
Num UIs Processed	95.446 kCycles	**RefClkJit (p-p) filtered**	16.70 ps	**RefClkJit (rms) filtered**	2.05 ps
Connection Type	Chan 2,4 - Direct Connect				

Trial 1

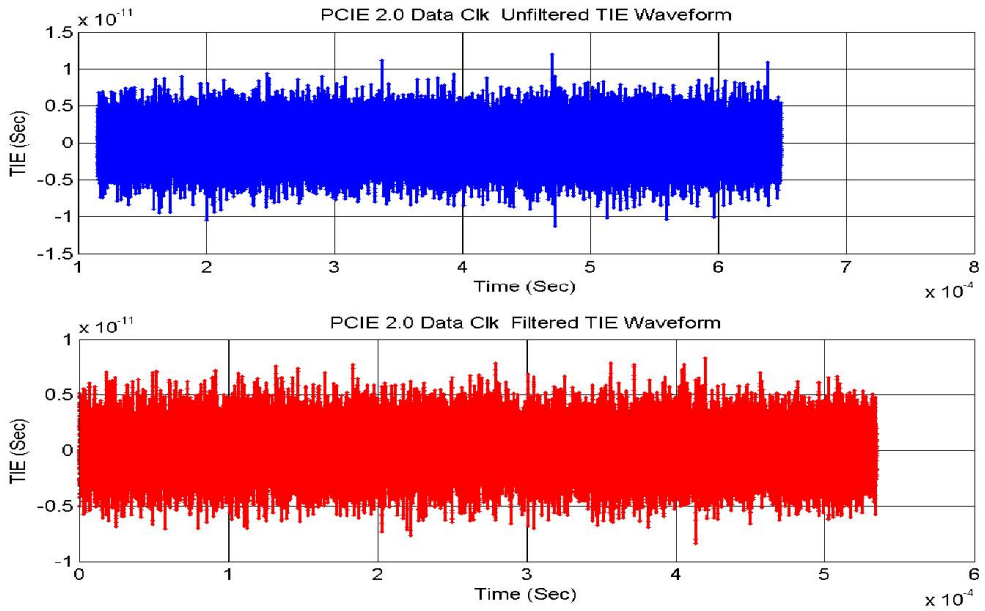
Trial 1: Ref Clock Filter Response



Trial 1: Ref Clock TIE Spectra



Trial 1: Ref Clock TIE Waveforms



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✓ Reference Clock, Low frequency 10kHz - 1.5MHz RMS Jitter (Data Clk) (PCIE 2.0, 5.0 GT/s)

Reference: PCI Express Base Specification, Rev 3.0, Section 4.3.7.3.5, Table 4-33

Test Summary: Pass | Test Description: | This test verifies that the RMS reference clock phase jitter at a bit error rate of 10E-6 is less than the maximum allowed value.

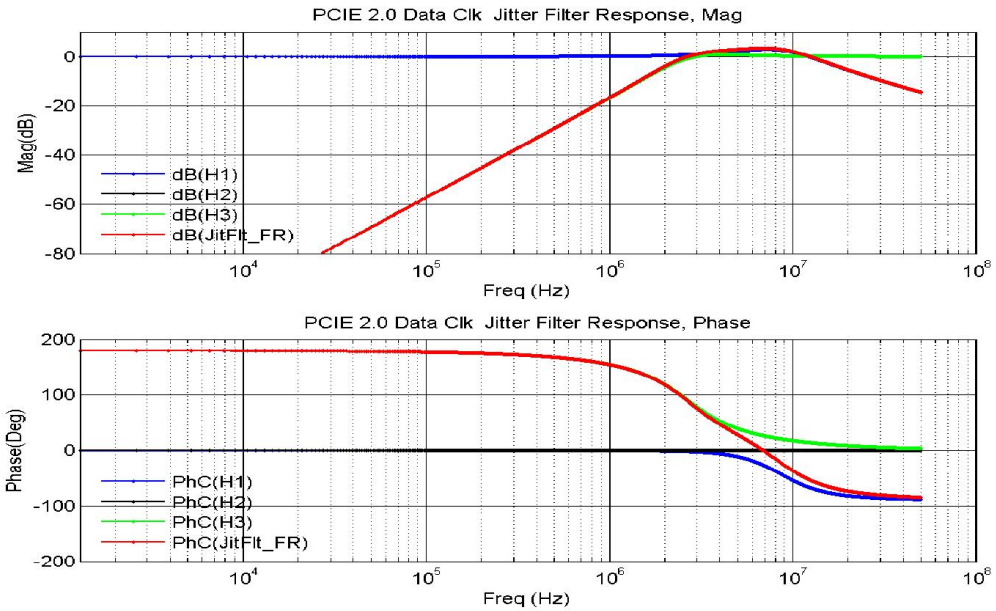
Pass Limits: <= 7.50 ps | **Reference Clock RMS Jitter (TREFCLK-LF-RMS)** 460 fs

Result Details

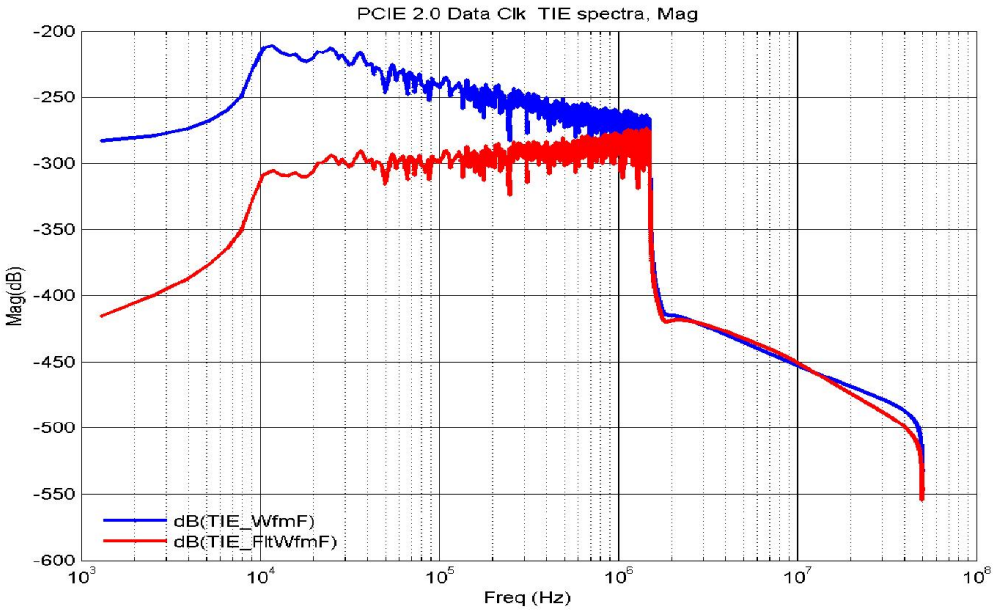
Ref Clock Filter Response (See image)	**Ref Clock TIE Spectra** (See image)	**Ref Clock TIE Waveforms** (See image)
Num UIs Processed 95.446 kCycles	**RefClkJit (p-p) filtered** 3.46 ps	**RefClkJit (rms) filtered** 460 fs
Connection Type Chan 2,4 - Direct Connect		

Trial 1

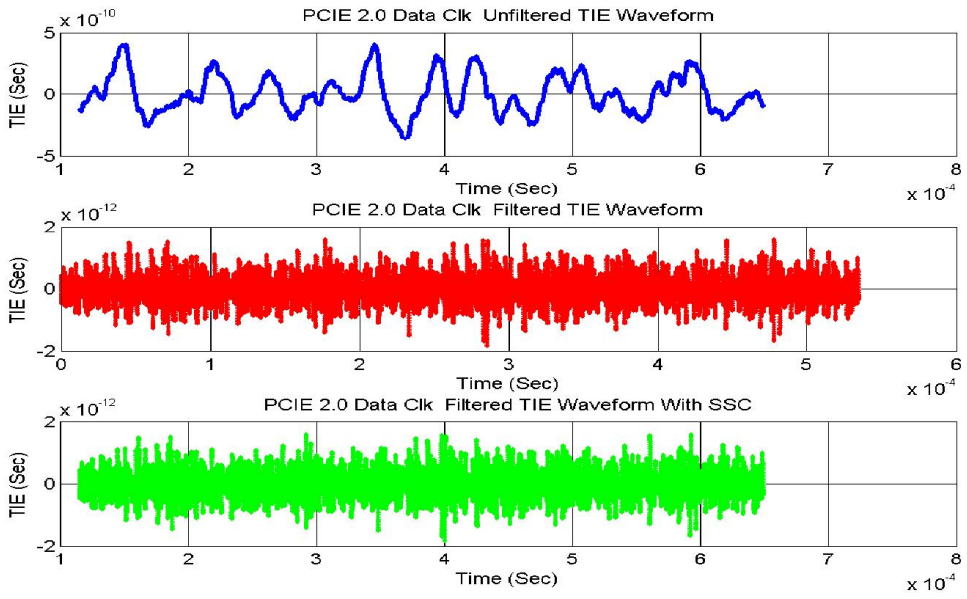
Trial 1: Ref Clock Filter Response



Trial 1: Ref Clock TIE Spectra



Trial 1: Ref Clock TIE Waveforms



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