Agilent Technologies

PCI Express Test Report

Overall Result: PASS

Test Configuration Details	
Device Description	
Device ID	Device 1
Preset Type	None
Test Session Details	
Infiniium SW Version	04.20.0008
Infiniium Model Number	DSO91304A
Infiniium Serial Number	MY50140158
Application SW Version	3.34
Debug Mode Used	No
Last Test Date	2015-01-08 09:47:29 UTC +02:00

Summary of Results

Test Statistics	
Failed	0
Passed	17
Total	17

Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	System Board Tx, Unit Interval (PCIE 1.1)	400.0710 ps	20.4 %	399.8800 ps <= VALUE <= 400.1200 ps
✓	0	1	System Board Tx, Template Tests (PCIE 1.1)	Pass	100.0 %	Pass/Fail
✓	0	1	System Board Tx, Median to Max Jitter (PCIE 1.1)	22.92 ps	70.2 %	VALUE <= 77.00 ps
✓	0	1	System Board Tx, Eye-Width (PCIE 1.1)	343.42 ps	39.6 %	VALUE >= 246.00 ps
✓	0	1	System Board Tx, Peak Differential Output Voltage (Transition)(PCIE 1.1)	706.8 mV	46.7 %	274.0 mV <= VALUE <= 1.2000 V
✓	0	1	System Board Tx, Peak Differential Output Voltage (NonTransition)(PCIE 1.1)	1.0594 V	14.8 %	253.0 mV <= VALUE <= 1.2000 V
✓	0	1	Reference Clock, Phase Jitter (PCIE 1.1)	25.24 ps	70.7 %	VALUE <= 86.00 ps
✓	0	1	Reference Clock, Rising Edge Rate (PCIE 1.1)	1.60 V/ns	29.4 %	600 mV/ns <= VALUE <= 4.00 V/ns
✓	0	1	Reference Clock, Falling Edge Rate (PCIE 1.1)	1.56 V/ns	28.2 %	600 mV/ns <= VALUE <= 4.00 V/ns
✓	0	1	Reference Clock, Differential Input High Voltage (PCIE 1.1)	410 mV	173.3 %	VALUE >= 150 mV
✓	0	1	Reference Clock, Differential Input Low Voltage (PCIE 1.1)	-410 mV	173.3 %	VALUE <= -150 mV
✓	0	1	Reference Clock, Average Clock Period (PCIE 1.1)	53 ppm	41.2 %	-300 ppm <= VALUE <= 300 ppm
✓	0	1	Reference Clock, Duty Cycle (PCIE 1.1)	49.9 %	49.5 %	40.0 % <= VALUE <= 60.0 %
✓	0	1	Reference Clock, Variation of VCross (PCIE 1.1)	34.4 mV	75.4 %	VALUE <= 140.0 mV
✓	0	1	Reference Clock, Absolute Max Input Voltage (PCIE 1.1)	407.1 mV	64.6 %	VALUE <= 1.1500 V
✓	0	1	Reference Clock, Absolute Min Input Voltage (PCIE 1.1)	-12.4 mV	95.9 %	VALUE >= -300.0 mV
✓	0	1	Reference Clock, Rise-Fall Matching (PCIE 1.1)	16.90 %	15.5 %	VALUE <= 20.00 %

Report Detail

Next

System Board Tx, Unit Interval (PCIE 1.1)

Reference: This test is not required. It is informative only.

Test Summary: Pass

Test Description: A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The worst case recovered TX UI is reported here. The UI range is NOT specified for this test point. It is provided here as informative data only.

Pass Limits: [399.8800 ps to 400.1200 ps] **Worst Case UI (ps)** 400.0710 ps

Result Details

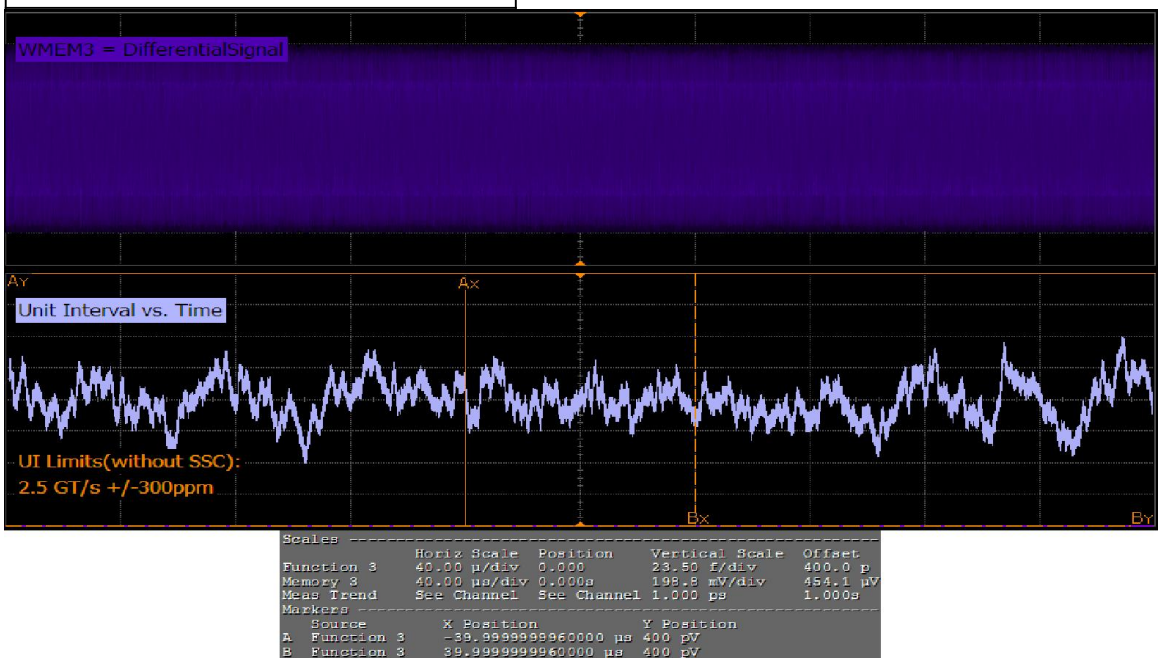
Data Lane (no value) **Note:** Non-SSC Limits Used: 2.5 GT/s +/-300ppm **#3500 UI Blocks Measured** 996.440 k

Min UI 399.9770 ps **Max UI** 400.0710 ps **Mean UI** 400.0240 ps **Worst Case Data Rate** 2.499556328752 Gbits/sec

Mean Data Rate 2.499850008999 Gbits/sec **Connection Type** Chan 1,3 - 2 Single Ended Probes

Trial 1

Trial 1: Mean Data Rate



Scales				
	Horiz Scale	Position	Vertical Scale	Offset
Function 3	40.00 µ/div	0.000	23.50 f/div	400.0 p
Memory 3	40.00 µs/div	0.000s	198.8 mV/div	454.1 µV
Meas Trend	See Channel	See Channel	1.000 ps	1.000s

Markers			
	Source	X Position	Y Position
A	Function 3	-39.999999960000 µs	400 pV
B	Function 3	39.999999960000 µs	400 pV

Top Previous Next

System Board Tx, Template Tests (PCIE 1.1)

Reference: PCI Express CEM Specification, Rev 1.1, Section 4.7.3, Figure 4-10

Test Summary: Pass

Test Description: System boards must meet the System Board Transmitter Path Compliance Eye Requirements specified in table 4-8 of section 4.7.3 of the PCI Express Card Electromechanical (CEM) Specification, Rev 1.1, as measured after the connector with an ideal load.

Pass Limits: Pass/Fail **Total # Failures** Pass

Result Details

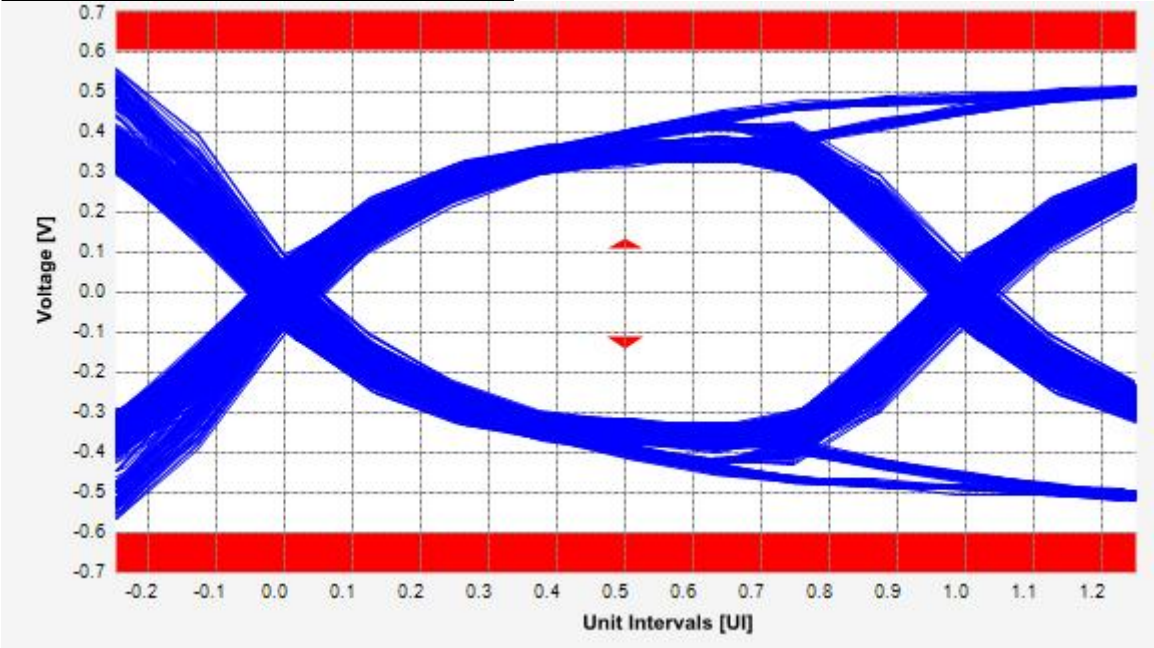
Transition Eye Diagram (See image) **Transition Failures** 0.000 **Non-Transition Eye Diagram** (See image)

Non-Transition Failures 0.000 **Total #UI Measured** 1.000000000 M **Reference Clock** Clean **Data Lane** (no value)

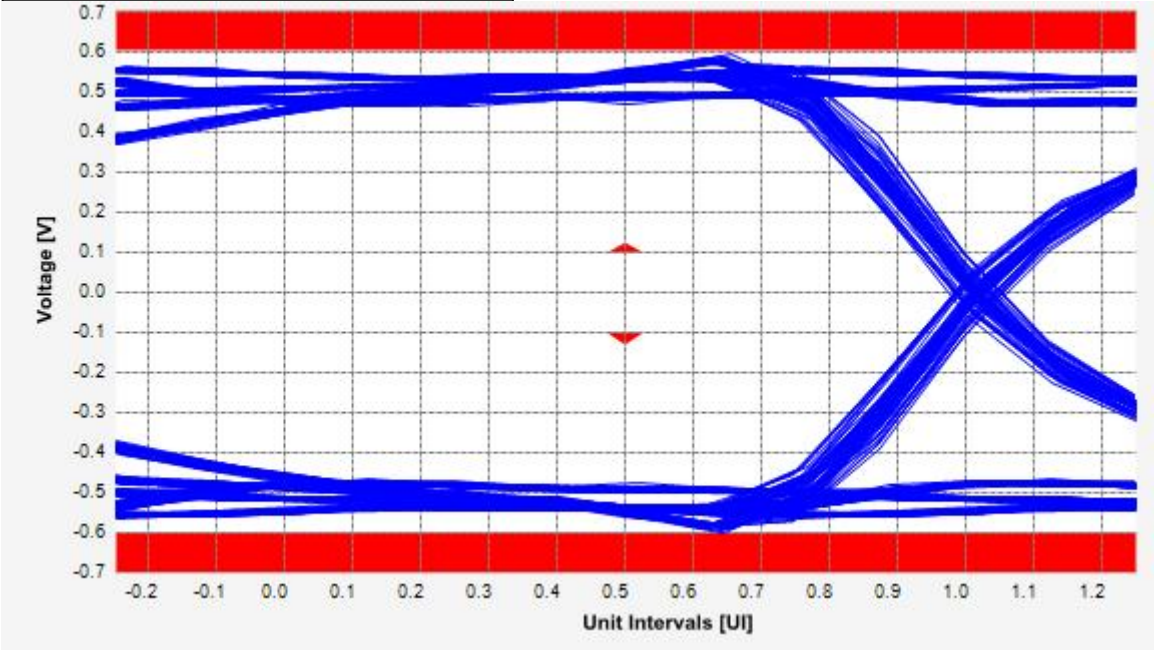
Requested Sample Rate (GSa/s) 20.0

Trial 1

Trial 1: Transition Eye Diagram



Trial 1: Non-Transition Eye Diagram



Top Previous Next

✓ System Board Tx, Median to Max Jitter (PCIE 1.1)

Reference: PCI Express CEM Specification, Rev 1.1, Table 4-9

Test Summary: Pass

Test Description: | This test measures the maximum time between the jitter median and maximum deviation from the median.

Pass Limits: <= 77.00 ps | **Median-to-Max Jitter** 22.92 ps

Result Details

Data Lane (no value) | **Connection Type** Chan 1,3 - 2 Single Ended Probes

Top Previous Next

✓ System Board Tx, Eye-Width (PCIE 1.1)

Reference: PCI Express CEM Specification, Rev 1.1, Table 4-9

Test Summary: Pass | Test Description: | This test measures the eye-width of the compliance eye. The eye-width is computed as the [mean unit interval] - [peak-to-peak jitter].

Pass Limits: >= 246.00 ps | **Eye-Width** 343.42 ps

Result Details

Data Lane (no value) | **Connection Type** Chan 1,3 - 2 Single Ended Probes

Top Previous Next

System Board Tx, Peak Differential Output Voltage (Transition)(PCIE 1.1)

Reference: PCI Express CEM Specification, Rev 1.1, Table 4-9

Test Summary: Pass | Test Description: | This test verifies that the Differential Peak Differential Output Voltage for transition bits is within the allowed range.

Pass Limits: [274.0 mV to 1.2000 V] | **PeakVoltage** 706.8 mV

Result Details

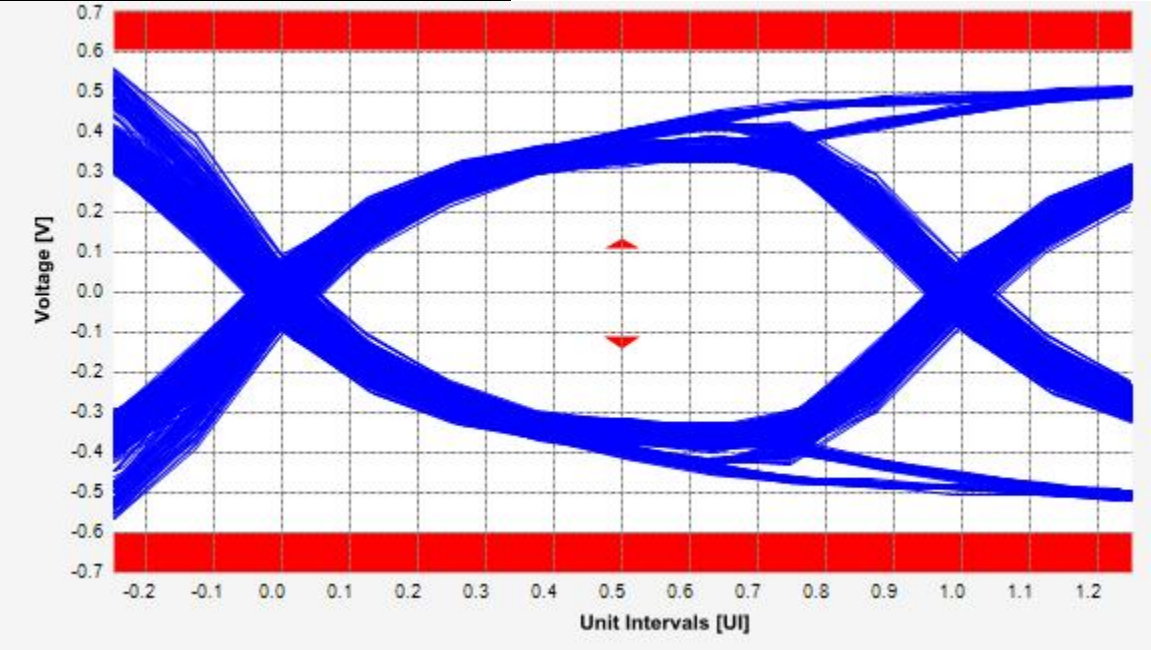
Total #UI Measured 1.000000000 M | **Largest Transition Amplitude (Outer eye)** 999.6 mV

Smallest Transition Amplitude (Inner eye) 627.3 mV | **Data Lane** (no value) | **Transition Eye Diagram** (See image)

Connection Type Chan 1,3 - 2 Single Ended Probes

Trial 1

Trial 1: Transition Eye Diagram



Top Previous Next

System Board Tx, Peak Differential Output Voltage (NonTransition)(PCIE 1.1)

Reference: PCI Express CEM Specification, Rev 1.1, Table 4-9

Test Summary: Pass | Test Description: | This test verifies that the Differential Peak Differential Output Voltage for non transition bits is within the allowed range.

Pass Limits: [253.0 mV to 1.2000 V] | **PeakVoltage** 1.0594 V

Result Details

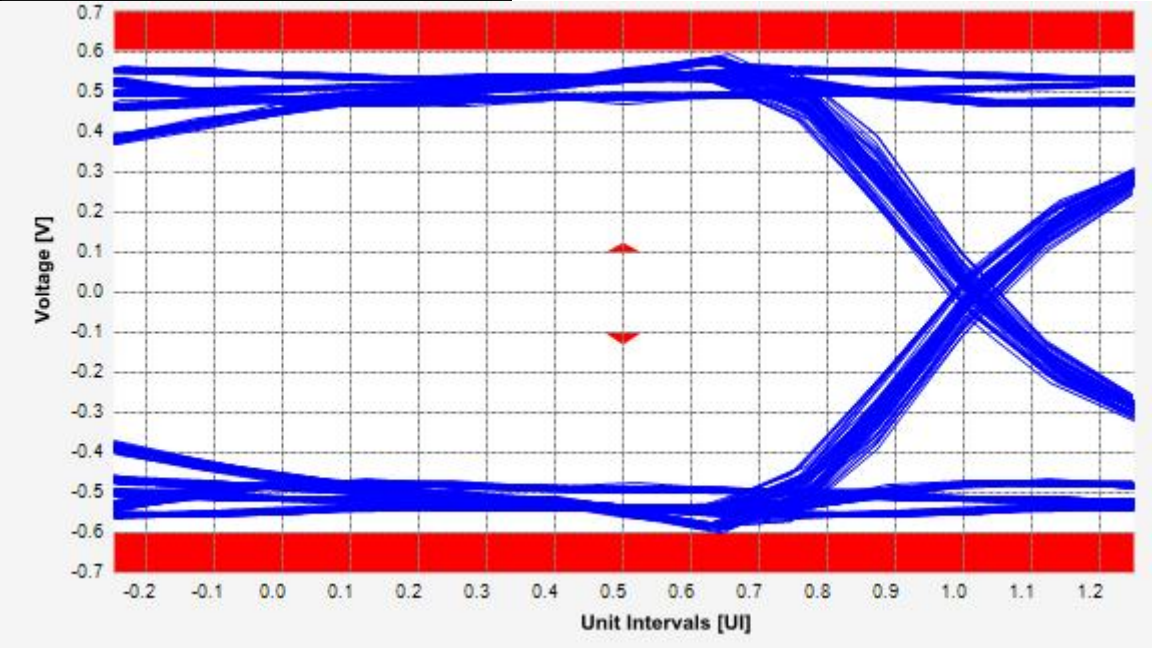
Total #UI Measured 1.000000000 M | **Largest Non Transition Amplitude (Outer eye)** 1.1933 V

Smallest Non Transition Amplitude (Inner eye) 947.6 mV | **Data Lane** (no value) | **Non-Transition Eye Diagram** (See image)

Connection Type Chan 1,3 - 2 Single Ended Probes

Trial 1

Trial 1: Non-Transition Eye Diagram



Top Previous Next

✓ Reference Clock, Phase Jitter (PCIE 1.1)

Reference: PCI Express CEM Specification, Rev 1.1, Section 2.1.4, Table 2-2

Test Summary: Pass | Test Description: | This test verifies that the magnitude of the peak-peak reference clock phase jitter at a bit error rate of 10E-6 is less than the maximum allowed value.

Pass Limits: <= 86.00 ps | **Reference Clock Phase Jitter** 25.24 ps

Result Details

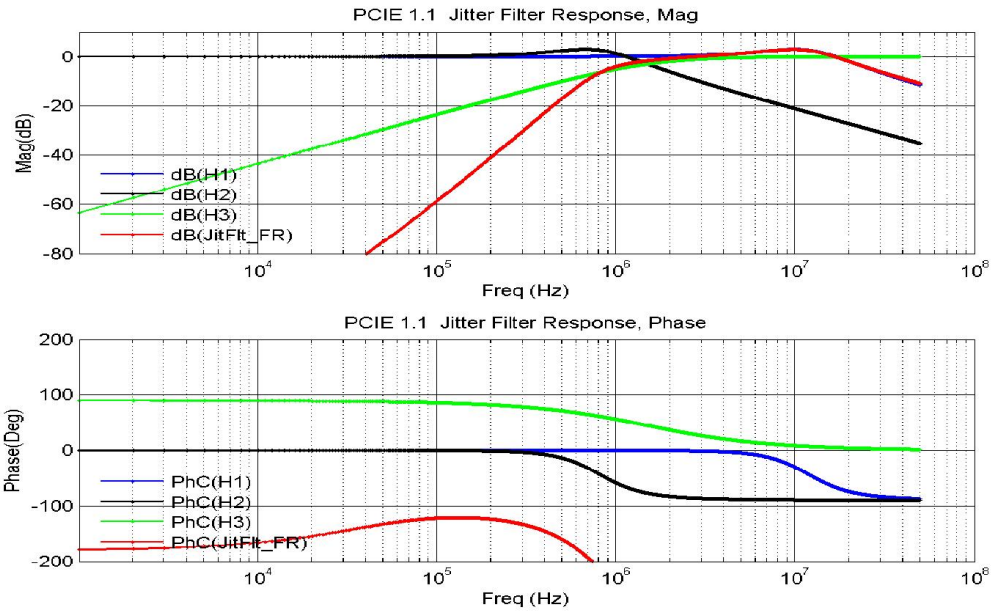
Ref Clock Filter Response (See image) | **Ref Clock TIE Spectra** (See image) | **Ref Clock TIE Waveforms** (See image)

Num UIs Processed 98.860 kCycles | **RefClkJit (p-p) filtered** 25.24 ps | **RefClkJit (rms) filtered** 2.82 ps

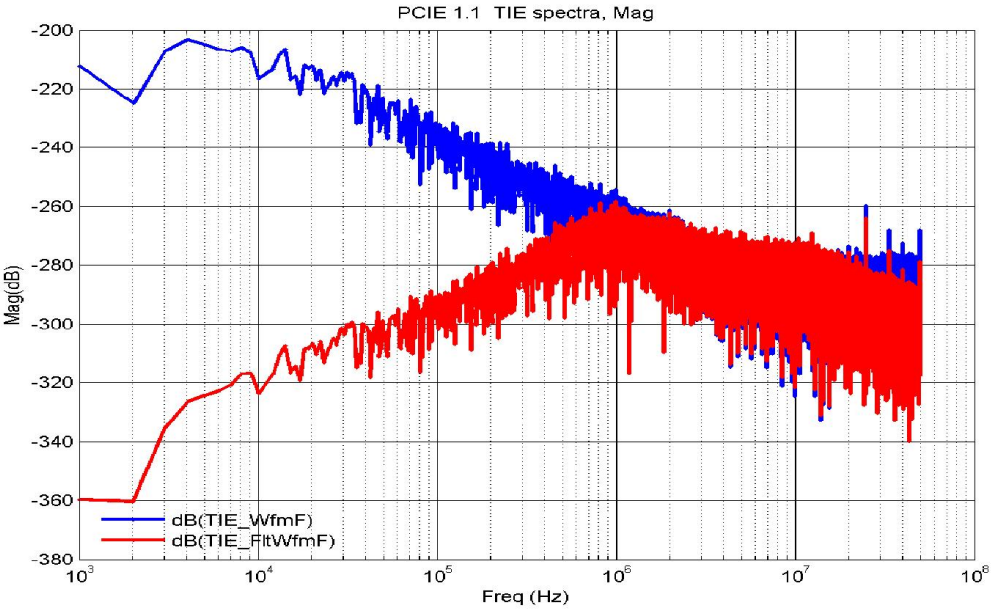
Connection Type Chan 2,4 - Direct Connect

Trial 1

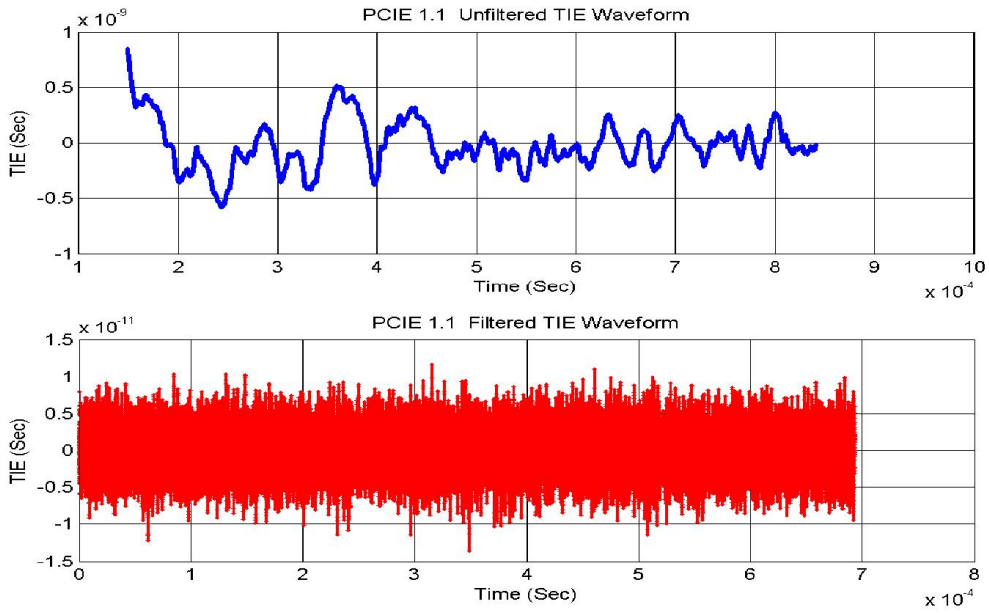
Trial 1: Ref Clock Filter Response



Trial 1: Ref Clock TIE Spectra



Trial 1: Ref Clock TIE Waveforms



Top Previous Next

Reference Clock, Rising Edge Rate (PCIE 1.1)

Reference: PCI Express CEM Specification, Rev 1.1, Section 2.1.3, Table 2-1

Test Summary: Pass

Test Description: | This test verifies that the rising edge rate of the waveform is within the allowed range. The value is measured from -150mV to +150mV on the differential waveform and the measurement window is centered on the differential zero crossing.

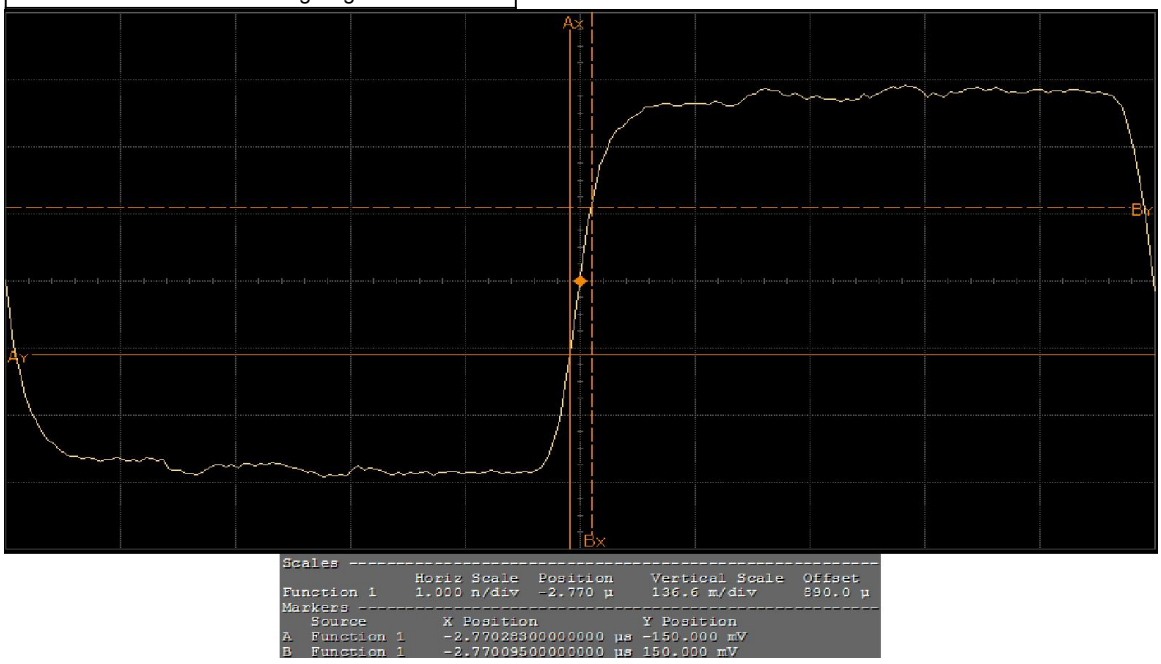
Pass Limits: [600 mV/ns to 4.00 V/ns] **Reference Clock Rising Edge Rate** 1.60 V/ns

Result Details

Connection Type Chan 2,4 - Direct Connect

Trial 1

Trial 1: Reference Clock Rising Edge Rate



Top Previous Next

Reference Clock, Falling Edge Rate (PCIE 1.1)

Reference: PCI Express CEM Specification, Rev 1.1, Section 2.1.3, Table 2-1

Test Summary: Pass

Test Description: | This test verifies that the falling edge rate of the waveform is within the allowed range. The value is measured from -150mV to +150mV on the differential waveform and the measurement window is centered on the differential zero crossing.

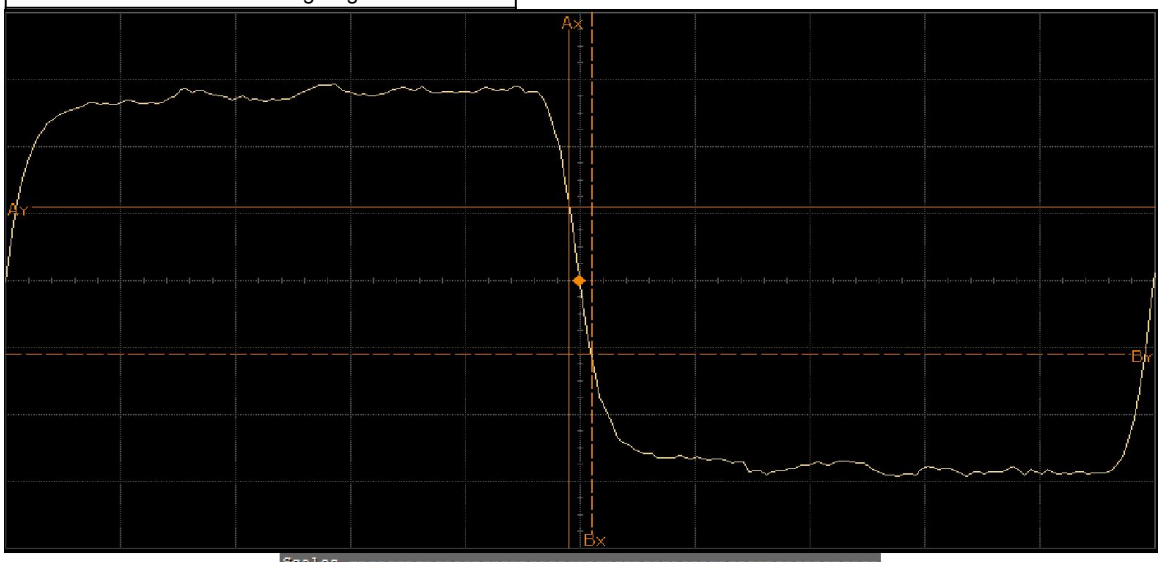
Pass Limits: [600 mV/ns to 4.00 V/ns] **Reference Clock Falling Edge Rate** 1.56 V/ns

Result Details

Connection Type Chan 2,4 - Direct Connect

Trial 1

Trial 1: Reference Clock Falling Edge Rate



Scales

	Horiz Scale	Position	Vertical Scale	Offset
Function 1	1.000 n/div	12.14 µ	136.6 m/div	890.0 µ

Markers

	Source	X Position	Y Position
A	Function 1	12.1358600000000 µs	150.000 mV
B	Function 1	12.1360520000000 µs	-150.000 mV

Top Previous Next

Reference Clock, Differential Input High Voltage (PCIE 1.1)

Reference: PCI Express CEM Specification, Rev 1.1, Section 2.1.3, Table 2-1

Test Summary: Pass

Test Description: | This test verifies that the high voltage of the reference clock differential waveform is greater than the minimum allowed value.

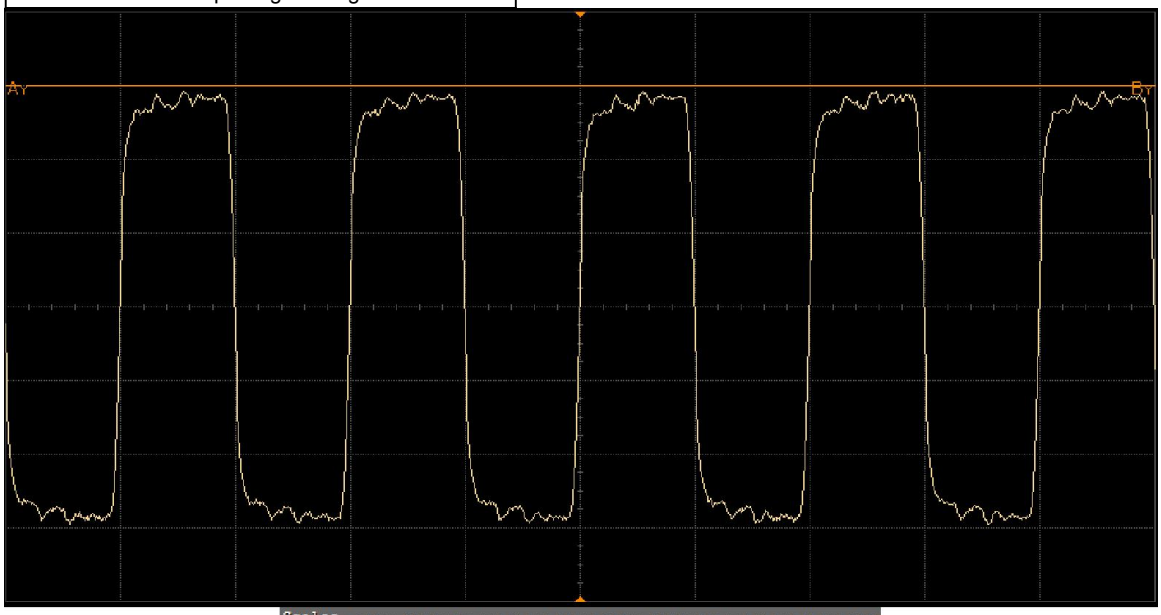
Pass Limits: >= 150 mV **RefClk Diff Input High Voltage** 410 mV

Result Details

Connection Type Chan 2,4 - Direct Connect

Trial 1

Trial 1: RefClk Diff Input High Voltage



Top Previous Next

Reference Clock, Differential Input Low Voltage (PCIE 1.1)

Reference: PCI Express CEM Specification, Rev 1.1, Section 2.1.3, Table 2-1

Test Summary: Pass

Test Description: | This test verifies that the low voltage of the reference clock differential waveform is less than the maximum allowed value.

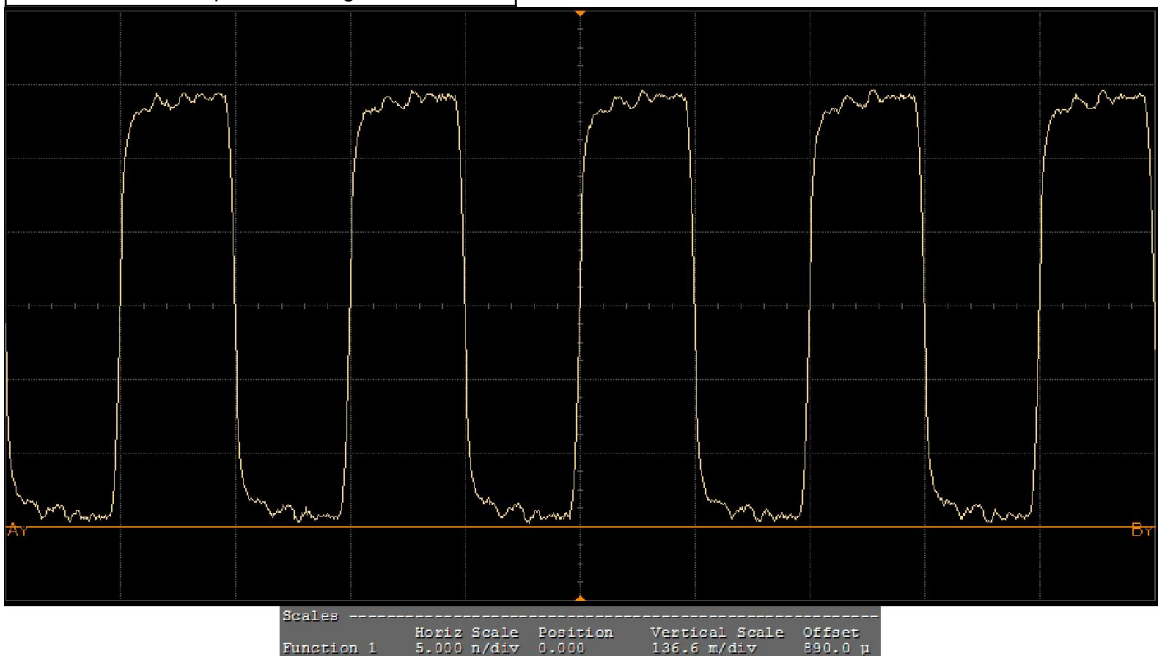
Pass Limits: <= -150 mV **RefClk Diff Input Low Voltage** -410 mV

Result Details

Connection Type Chan 2,4 - Direct Connect

Trial 1

Trial 1: RefClk Diff Input Low Voltage



Top Previous Next

Reference Clock, Average Clock Period (PCIE 1.1)

Reference: PCI Express CEM Specification, Rev 1.1, Section 2.1.3, Table 2-1

Test Summary: Pass

Test Description: | The average clock period accuracy of the differential waveform is measured in PPM (parts per million) where 1 PPM equals 100Hz. A requirement of +/- 300 PPM applies to systems that do NOT employ SSC or that use a common clock source. For systems employing SSC there is an additional 2500 PPM nominal shift in the maximum period resulting in a maximum average period specification of +2800 PPM.

Pass Limits: [-300 ppm to 300 ppm] **RefClk Average Clock Period** 53 ppm

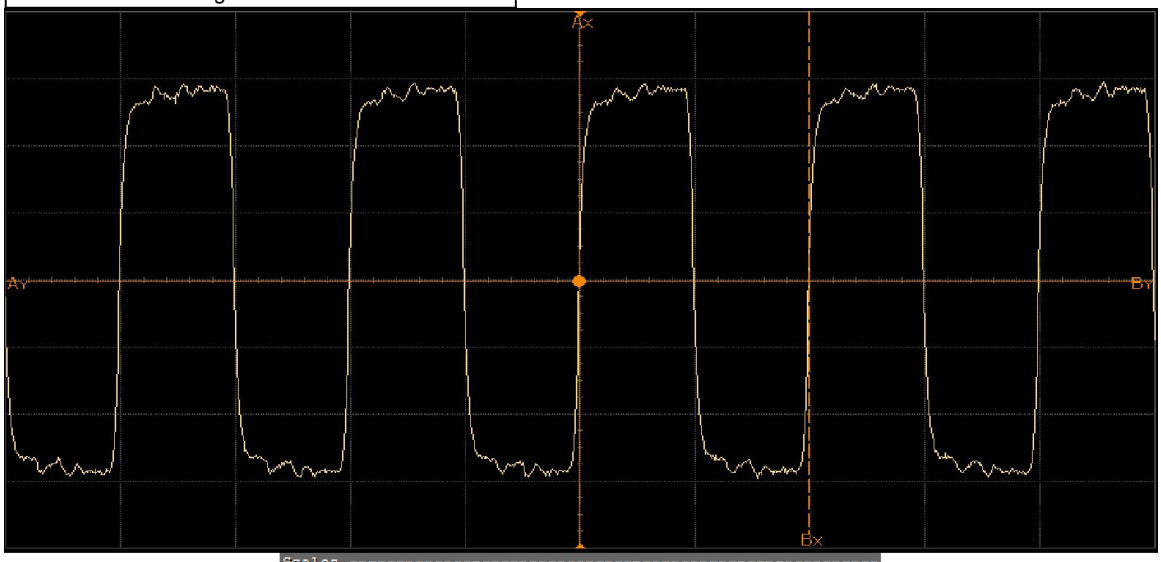
Result Details

Average Clock Frequency 99.994658500000 MHz **Average Clock Period** 10.00053480 ns

Note: Non-SSC Limits Used: 100MHz +/-300ppm **Connection Type** Chan 2,4 - Direct Connect

Trial 1

Trial 1: RefClk Average Clock Period



Scales

	Horiz Scale	Position	Vertical Scale	Offset
Function 1	5.000 n/div	0.000	136.6 m/div	890.0 µ

Markers

	Source	X Position	Y Position
A	Function 1	-47.0000000000000 ps	-829 µV
B	Function 1	9.95200000000000 ns	-829 µV

Top Previous Next

Reference Clock, Duty Cycle (PCIE 1.1)

Reference: PCI Express CEM Specification, Rev 1.1, Section 2.1.3, Table 2-1

Test Summary: Pass

Test Description: | This test verifies that the duty cycle of the reference clock differential waveform is within the allowed range.

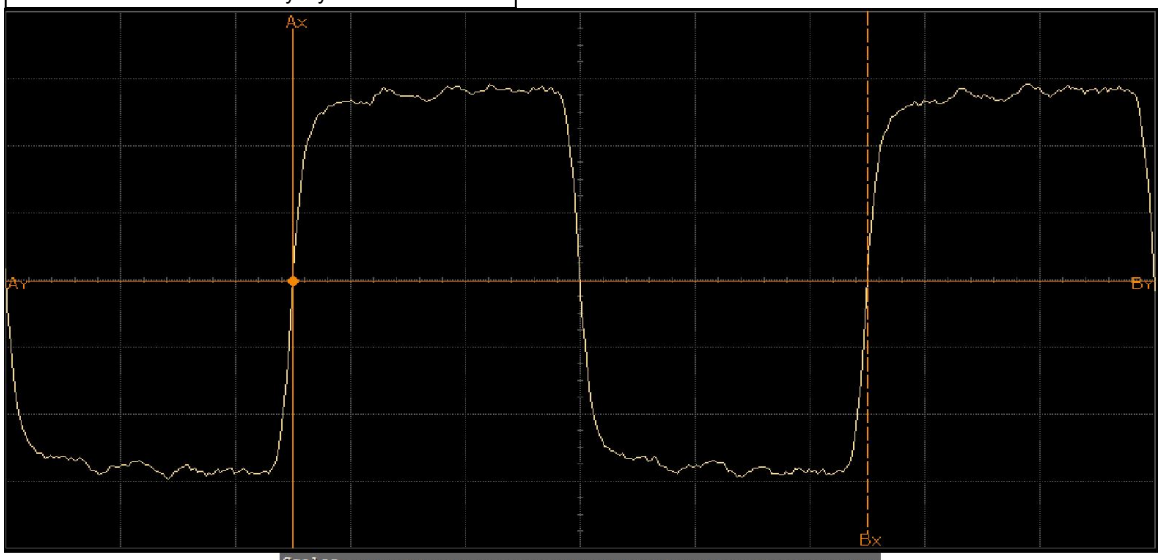
Pass Limits: [40.0 % to 60.0 %] **Reference Clock Duty Cycle** 49.9 %

Result Details

Duty Cycle Mean 50.0 % **Duty Cycle Min** 49.9 % **Duty Cycle Max** 50.1 % **Connection Type** Chan 2,4 - Direct Connect

Trial 1

Trial 1: Reference Clock Duty Cycle



Top Previous Next

✓ Reference Clock, Variation of VCross (PCIE 1.1)

Reference: PCI Express CEM Specification, Rev 1.1, Section 2.1.3, Table 2-1

Test Summary: Pass | Test Description: | This test verifies that the variation of VCross over all rising clock edges is within the allowed range.

Pass Limits: <= 140.0 mV | **VCross Delta** 34.4 mV

Result Details

Rising Edge VCross Max 177.0 mV | **Rising Edge VCross Min** 142.6 mV | **Connection Type** Chan 2,4 - Direct Connect

Top Previous Next

✓ Reference Clock, Absolute Max Input Voltage (PCIE 1.1)

Reference: PCI Express CEM Specification, Rev 1.1, Section 2.1.3, Table 2-1

Test Summary: Pass | Test Description: | This test verifies that the absolute maximum input voltage of the reference clock is within the allowed range.

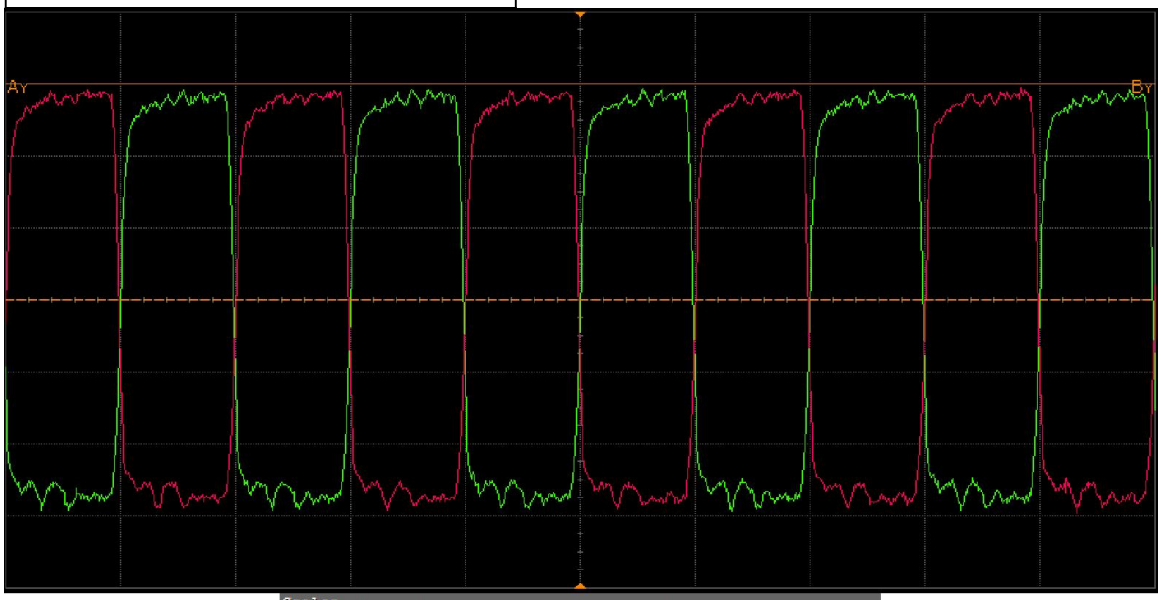
Pass Limits: <= 1.1500 V | **VMAX** 407.1 mV

Result Details

REFCLK+ VMax 407.1 mV | **REFCLK- VMin** 406.6 mV | **Connection Type** Chan 2,4 - Direct Connect

Trial 1

Trial 1: VMAX



Top Previous Next

✓ Reference Clock, Absolute Min Input Voltage (PCIE 1.1)

Reference: PCI Express CEM Specification, Rev 1.1, Section 2.1.3, Table 2-1

Test Summary: Pass | Test Description: | This test verifies that the absolute minimum input voltage of the reference clock is within the allowed range.

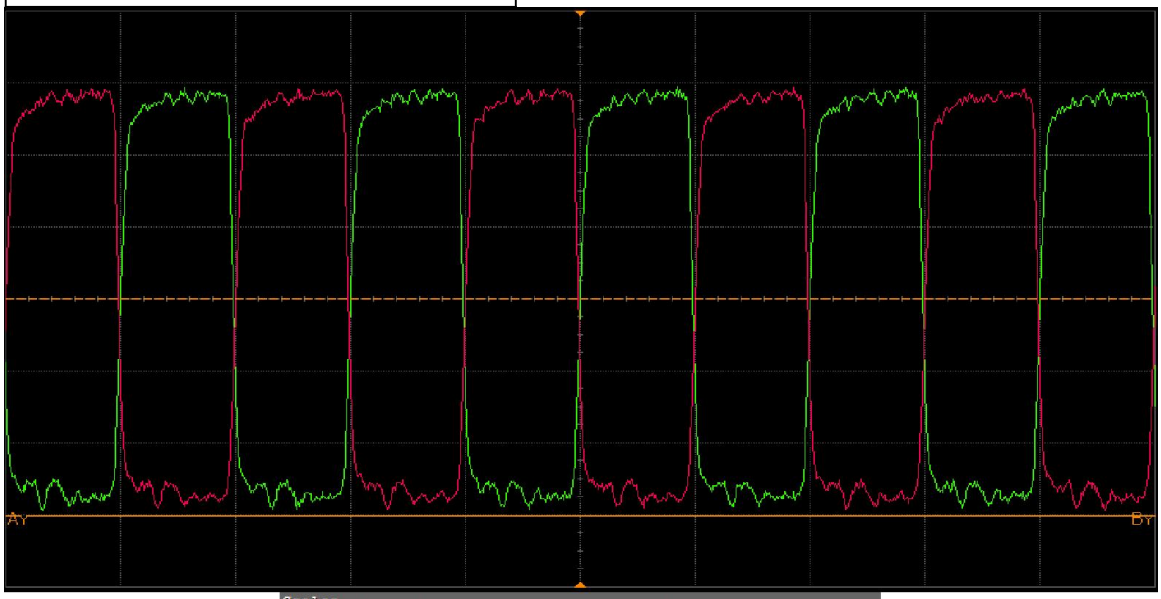
Pass Limits: >= -300.0 mV | **VMIN** -12.4 mV

Result Details

REFCLK+ VMin -12.4 mV | **REFCLK- VMin** -11.6 mV | **Connection Type** Chan 2,4 - Direct Connect

Trial 1

Trial 1: VMIN



Top Previous Next

✓ Reference Clock, Rise-Fall Matching (PCIE 1.1)

Reference: PCI Express CEM Specification, Rev 1.1, Section 2.1.3, Table 2-1

Test Summary: Pass

Test Description: | This test verifies that the rising edge rate (REFCLK+) to falling edge rate (REFCLK-) matching is within the allowed range.

Pass Limits: <= 20.00 %

Rise-Fall Matching 16.90 %

Result Details

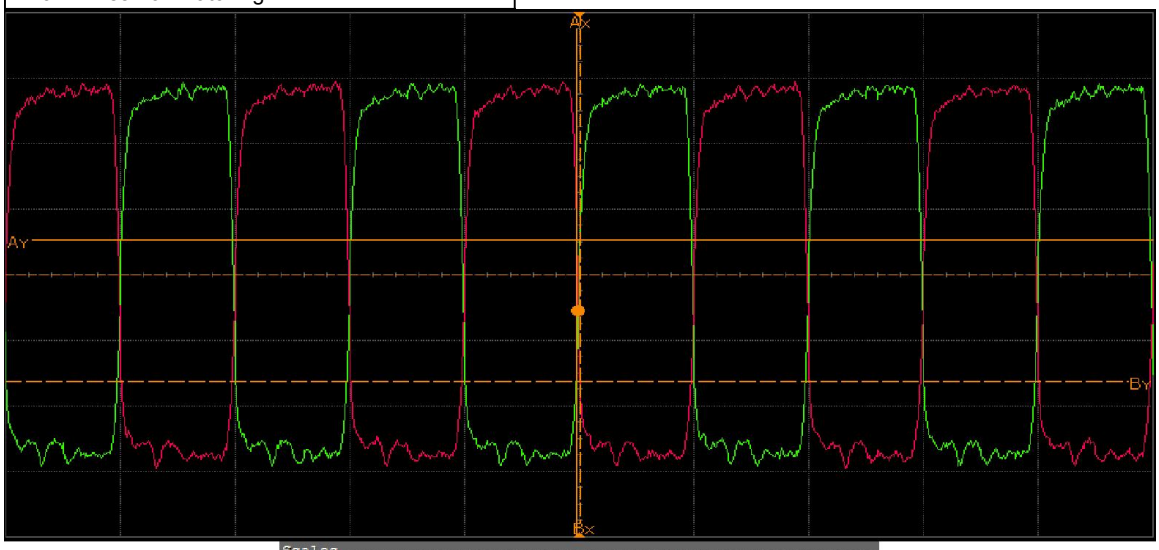
REFCLK+ Rise time 197.9 ps

REFCLK- Fall time 164.4 ps

Connection Type Chan 2,4 - Direct Connect

Trial 1

Trial 1: Rise-Fall Matching



Scales

	Horiz Scale	Position	Vertical Scale	Offset
Channel 2	5.000 ns/div	0.000s	69.60 mV/div	197.6 mV
Channel 4	5.000 ns/div	0.000s	69.50 mV/div	198.0 mV

Markers

	Source	X Position	Y Position
A	Channel 4	-115.000000000000 ps	234.761 mV
B	Channel 4	50.0000000000000 ps	84.761 mV

Top Previous