FTF 2016
TECHNOLOGY FORUM

LEVERAGING NXP RESOURCES TO AID IN PRODUCT DEVELOPMENT

FTF-DES-N1993

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AGENDA

- System Architecture
- Board Requirements
- Component Selection
- Schematic Design
- Layout
- DFM/DFA/DFT
- Fabrication and Assembly
- Test
- Software Integration
- Regulatory Compliance

System Architecture – Requirements

Product definition:

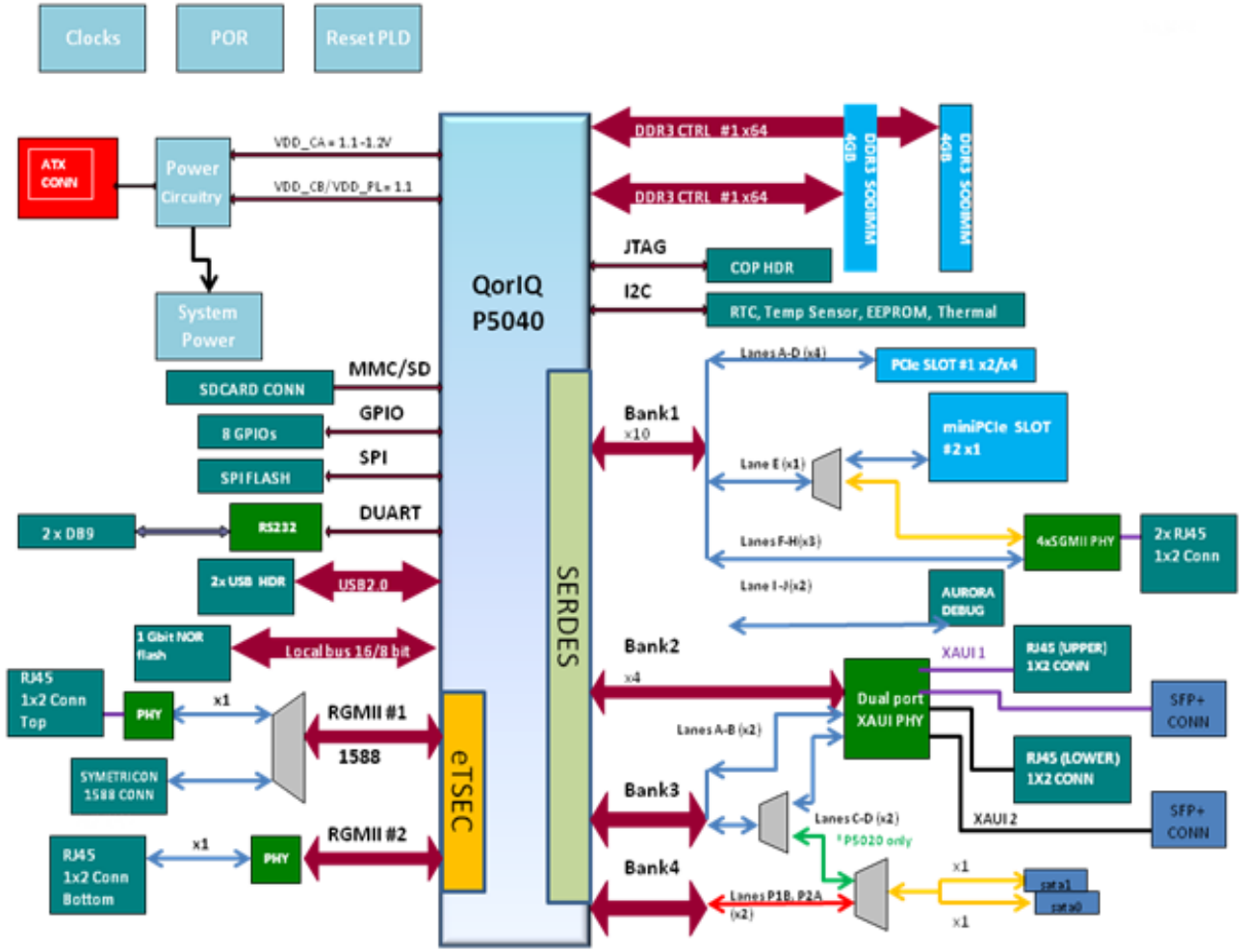
- What are you going to build
- Who is your market
- What is your cost target
- What is your schedule
- Features and functions
- Look and feel
- Marketing requirements, system and board level
- Customer feedback
- Lessons learned from previous products
- Required documentation and software
- Required resources to complete each aspect of the project

System Architecture – Enclosure and System BOM

- Board form factor can be microATX, miniATX, ATX, or customized depending on budgetary cost. Less expensive if the chassis is off-the-shelf in mass quantity, however chassis lifecycle can affect customization, and regulatory compliance.
- Form factor of the enclosure can be ATX standard or rack-mount i.e., 1U, 2U, custom, etc.
- FCC/CE, EMI, safety testing and thermal considerations for the chassis, board, and IO access
- Testing for reliability, ESD, Drop Test, and Heat Chamber
- System BOM includes power supply, cables, add-in cards, mechanical components, marketing collateral, software, and documentation

System Architecture – Functional Block Diagram

- Technical Spec and Functional Block Diagram
- The requirements are specified in a technical document that describes the functions supported by the system
- Functional Block Diagram illustrates the components for each function
- Example Block Diagram



Board Requirements – Design, Layout, and Debug Tools

- There are many tool flows that are used throughout the industry, but NXP generally uses the following:
  - Schematics: Cadence Design Entry CIS
  - Signal integrity simulation: Cadence Sigrity, Mentor HyperLynx
  - FPGA simulation and capture tools: ModelSim, HDLDesigner, Synplify, Vendor specific tools
  - Layout: Cadence Allegro
  - Design for Manufacturing/Assembly validation: Valor
  - Mechanical 3D modeling: SolidWorks
  - Run Control/Board Access: USBTap, OSBDM, JTAG
  - Software Debug: CodeWarrior, KDS, Linux SDK

Board Requirements – Industry Standards

- Functional features integrated with our state-of-the art processors and MCUs support many industry standards to provide our customers with mass market pricing and the latest technologies
- Examples:
  - DDR1/2/3, LPDDR2, Jedec.org
  - PCIe1/2 (pci.org), XAUI, SGMII, RMII, RGMII
  - USB1.0/2.0, ULPI
  - SATA 1.0/2.0
  - PICMG (picmg.org)
  - I2C, I2S, SDHC, MMC, SPI
  - CAN, LIN, UART, UTOPIA, HDLC

Component Selection

- **Performance** – Part must provide needed function and performance
- **Availability** – It doesn't matter how good the part is if you can't get it in time or in sufficient quantities. Obtain quotes early in the schematic cycle to identify long lead and expensive parts, thus allowing you to make changes on the part selection before layout.
- **Regional** – Buy parts in the region where you will be using them. This will help avoid lead-time and MOQ problems. Consider production assembly location when choosing parts for prototypes.
- **Quality & Counterfeit Parts:**
  - Buy direct from manufacturers or from distributors
  - Most vendors will not honor warranties on parts obtained from brokers
  - Parts from distributors are much less likely to be counterfeit
- **Cost** – The last criteria (the cost doesn't matter if the part doesn't meet the above requirements)
- **Selection Tools** – Use vendor selection guides to narrow your choices

Board Requirements – Power Budget and Power Supply

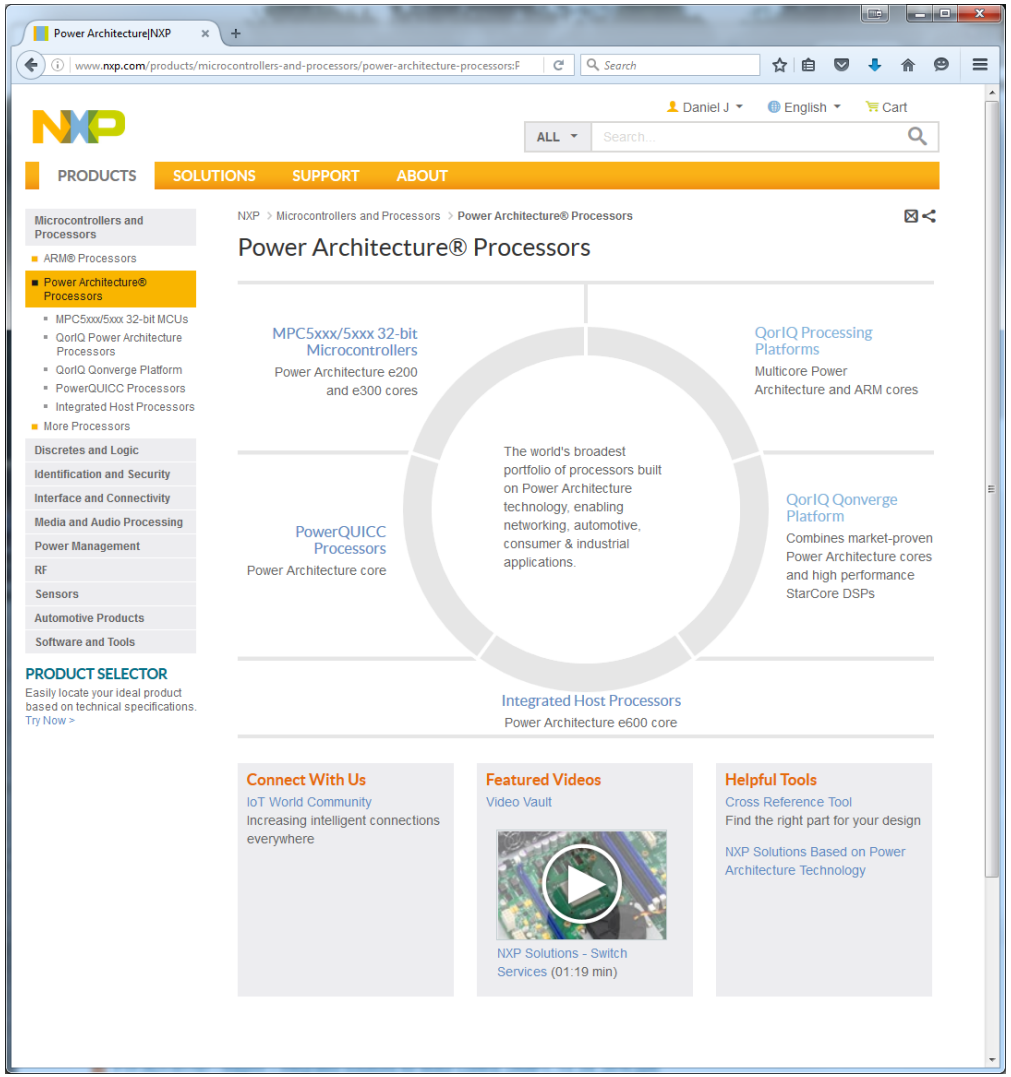
- Sum up all current usage for each voltage rail i.e., 2A@3.3v, etc., then determine what power supply to use in order to provide total power (Wattage) for all voltage rails.
- Power supply selection is also based on form factor of the enclosure such as ATX, 1U, 2U, 3U, 4U rack, custom, and so on.

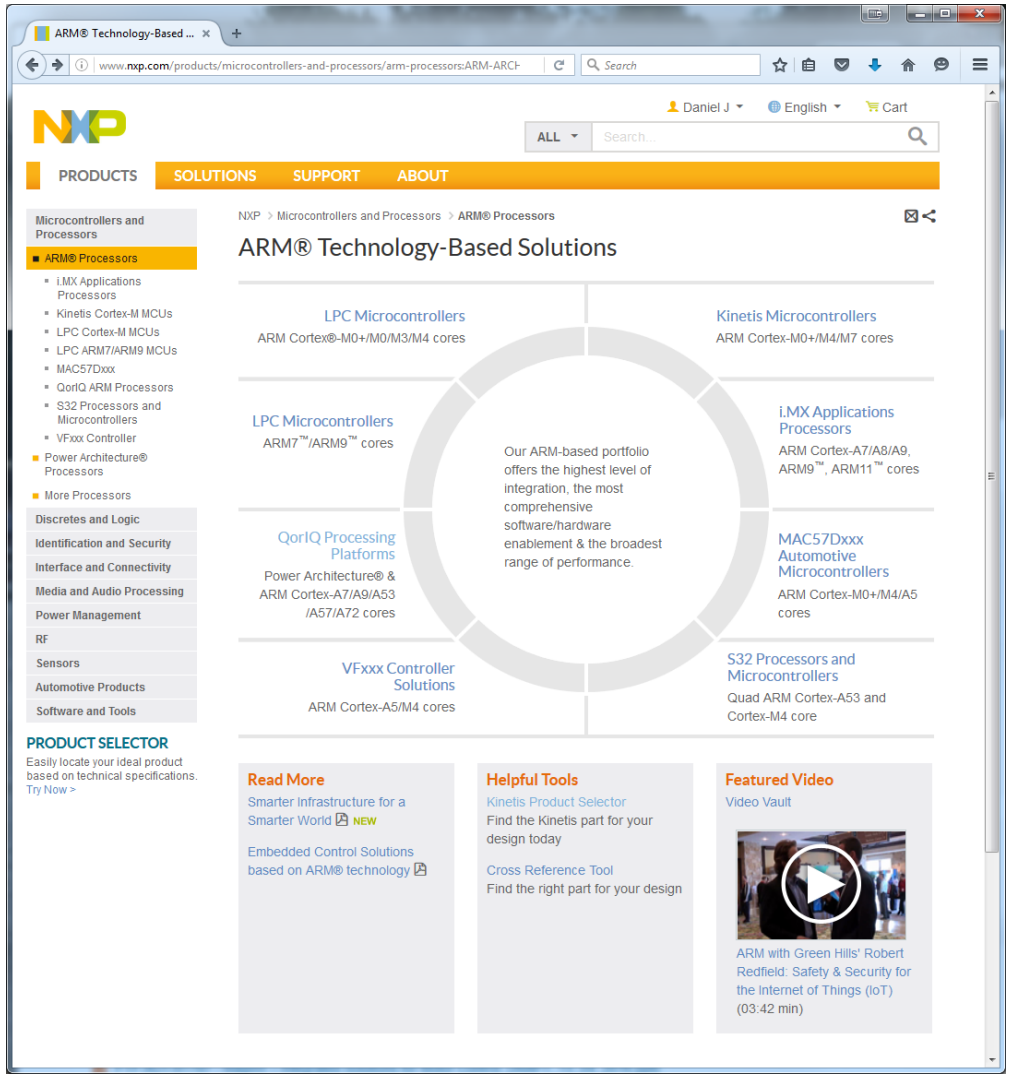
	0.9V	+1.0V	+1.1V	+1.2V	+1.8V	+2.5V	+1.8VH	+2.5VH	+3.3VH	+3.3V	+5.0V	+12V	-12V	+5V Stand-By	Power
Model: Antec SL450	(amps)	(amps)	(amps)	(amps)	(amps)	(amps)	(amps)	(amps)	(amps)	(amps)	(amps)	(amps)	(amps)	(amps)	(watts)
PCI SPEC Power Supply															
+3.3V (7.6 Amps max)										6.151515					20.3
+5.0V (5 Amps max)											0				0
+12V (0.5 Amps max)												1.5983			19.179
-12V (0.1 Amp max)													0		0
+5V Stand-By (2 Amps max)														1.5	7.5
													Supply	Total	46.979

Component Selection – Processor

- Choosing the right processor can be a daunting task, the following considerations should be taken:
  - Features
  - Power/Voltage
  - Temperature
  - Frequency
  - Pin Count/Package Type/Package Size
  - Memory Type/Size
- PowerQUICC and QorIQ Processor Selector Guide:
  - http://cache.nxp.com/files/32bit/doc/brochure/PWRARCHQIQSG.pdf
- ARM® Technology-Based Solutions:
  - http://www.nxp.com/products/microcontrollers-and-processors/arm-processors:ARM-ARCHITECTURE

Processors and Solutions





Component Selection – FPGA Considerations

- FPGA/CPLD vendors can provide help with selection
  - Features
  - Number of IO pins
  - Voltage tolerance
  - Speed
  - Ease of tools for debug and simulation

Schematic Design – Design Flow

- Block Diagram – break design into functional parts, one function per sheet, put primary functions near the front (e.g. main MCU/MPU)
- Reuse sections of previous designs – they are already proven and lower risk
- Central Library to promote component reuse and reduce costs
- Schematic is used to create a net list and to teach someone else the design, avoid air-wires, and include sheet to sheet cross references
- BOM Optimization – avoid same values in different sizes
- Check your design with a design checklist (helps to not forget something)
- NXP OrCAD symbols and Allegro footprints are available at:
  - http://www.nxp.com/webapp/parametricSelector.sp?#/breadcrumb_anchor
  - On orderable part numbers, select “Package/Quality”

Schematic Design – Design Checklist

- Logic – check voltage, buffering, timing, polarities
- Signal Integrity – are signals (especially clocks) properly terminated
- Pull-ups for open collector/drain
- Standard I/O properly connected and correct gender (e.g. DB9)
- Verify DNP properties and ensure schematic will netlist
- Validate bulk and decoupling caps and power sequencing
- Verify ratings on all components – especially R, L, C, diodes
- Use a standard format for all power nets (VDDxx, VSSxx or P5V, P3V3, N1V5, etc.)
- Test points for production test – include ground test points and probe loops
- Check DRC file for: Pin Conflicts, Net Aliases, Nets shorted to ground, Floating inputs, and Single node nets
- Hand check net-list – helps to find nets with the same name

Schematic Design – Layout Considerations

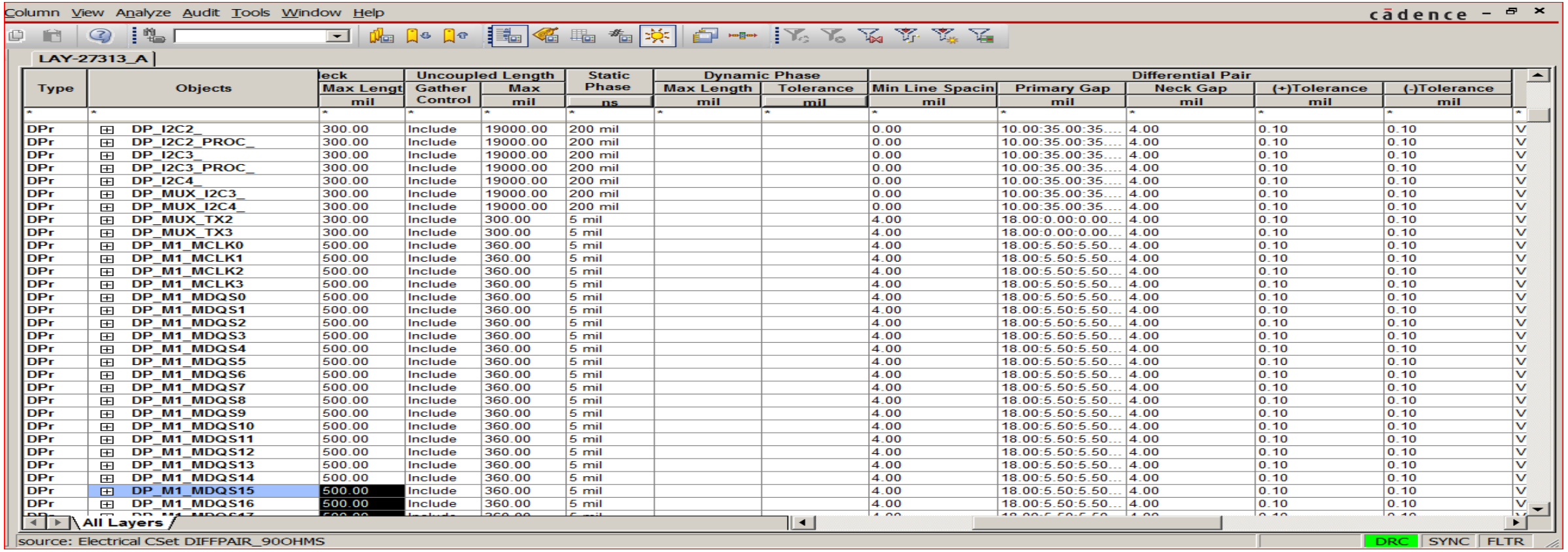
- NXP provides many layout application notes including industry standards such as PCIexpress and DDR, NXP.com→ Support → Documentation Library → Application Notes
- Other component vendors are good sources of layout guidelines, for circuits such as memories and power
- Mechanical – size, board thickness, stack-up, height restrictions (both top and bottom of the board)
- Fabrication – copper thickness, RoHS material, finish platings
- Power distribution and reference planes
  - List all power and ground nets
  - Specify reference planes and split planes (no routing across splits in reference planes without coupling caps between planes next to the line)

Schematic Design – Layout Considerations, Continued

- Analog isolation (physical isolation, split planes or moat and drawbridge)
- Placement of critical parts (a diagram is helpful) – caps and termination resistors near related parts, I/F with other boards, crystals next to ICs and R and C near crystals
- Impedance requirements
- Routing requirements of clocks, diff pairs, and other sensitive signals can be put into Allegro constraint manager
  - Max Parallel Rules
  - Differential routing – impedance, delta lengths, max total lengths
- Silkscreen text on components
- Manufacturing and production test-point requirements (spacing, power, etc.)

Layout – Constraint Manager

Cadence real time constraint manager on all CAD design files



Type	Objects	leck Max Lengt mil	Uncoupled Length Gather Control	Uncoupled Length Max mil	Static Phase ns	Dynamic Phase Max Length mil	Dynamic Phase Tolerance mil	Differential Pair Min Line Spacin mil	Differential Pair Primary Gap mil	Differential Pair Neck Gap mil	Differential Pair (+)Tolerance mil	Differential Pair (-)Tolerance mil
DPr	DP_I2C2_	300.00	Include	19000.00	200 mil			0.00	10.00:35.00:35....	4.00	0.10	0.10
DPr	DP_I2C2_PROC_	300.00	Include	19000.00	200 mil			0.00	10.00:35.00:35....	4.00	0.10	0.10
DPr	DP_I2C3_	300.00	Include	19000.00	200 mil			0.00	10.00:35.00:35....	4.00	0.10	0.10
DPr	DP_I2C3_PROC_	300.00	Include	19000.00	200 mil			0.00	10.00:35.00:35....	4.00	0.10	0.10
DPr	DP_I2C4_	300.00	Include	19000.00	200 mil			0.00	10.00:35.00:35....	4.00	0.10	0.10
DPr	DP_MUX_I2C3_	300.00	Include	19000.00	200 mil			0.00	10.00:35.00:35....	4.00	0.10	0.10
DPr	DP_MUX_I2C4_	300.00	Include	19000.00	200 mil			0.00	10.00:35.00:35....	4.00	0.10	0.10
DPr	DP_MUX_TX2	300.00	Include	300.00	5 mil			4.00	18.00:0.00:0.00...	4.00	0.10	0.10
DPr	DP_MUX_TX3	300.00	Include	300.00	5 mil			4.00	18.00:0.00:0.00...	4.00	0.10	0.10
DPr	DP_M1_MCLK0	500.00	Include	360.00	5 mil			4.00	18.00:5.50:5.50...	4.00	0.10	0.10
DPr	DP_M1_MCLK1	500.00	Include	360.00	5 mil			4.00	18.00:5.50:5.50...	4.00	0.10	0.10
DPr	DP_M1_MCLK2	500.00	Include	360.00	5 mil			4.00	18.00:5.50:5.50...	4.00	0.10	0.10
DPr	DP_M1_MCLK3	500.00	Include	360.00	5 mil			4.00	18.00:5.50:5.50...	4.00	0.10	0.10
DPr	DP_M1_MDQS0	500.00	Include	360.00	5 mil			4.00	18.00:5.50:5.50...	4.00	0.10	0.10
DPr	DP_M1_MDQS1	500.00	Include	360.00	5 mil			4.00	18.00:5.50:5.50...	4.00	0.10	0.10
DPr	DP_M1_MDQS2	500.00	Include	360.00	5 mil			4.00	18.00:5.50:5.50...	4.00	0.10	0.10
DPr	DP_M1_MDQS3	500.00	Include	360.00	5 mil			4.00	18.00:5.50:5.50...	4.00	0.10	0.10
DPr	DP_M1_MDQS4	500.00	Include	360.00	5 mil			4.00	18.00:5.50:5.50...	4.00	0.10	0.10
DPr	DP_M1_MDQS5	500.00	Include	360.00	5 mil			4.00	18.00:5.50:5.50...	4.00	0.10	0.10
DPr	DP_M1_MDQS6	500.00	Include	360.00	5 mil			4.00	18.00:5.50:5.50...	4.00	0.10	0.10
DPr	DP_M1_MDQS7	500.00	Include	360.00	5 mil			4.00	18.00:5.50:5.50...	4.00	0.10	0.10
DPr	DP_M1_MDQS8	500.00	Include	360.00	5 mil			4.00	18.00:5.50:5.50...	4.00	0.10	0.10
DPr	DP_M1_MDQS9	500.00	Include	360.00	5 mil			4.00	18.00:5.50:5.50...	4.00	0.10	0.10
DPr	DP_M1_MDQS10	500.00	Include	360.00	5 mil			4.00	18.00:5.50:5.50...	4.00	0.10	0.10
DPr	DP_M1_MDQS11	500.00	Include	360.00	5 mil			4.00	18.00:5.50:5.50...	4.00	0.10	0.10
DPr	DP_M1_MDQS12	500.00	Include	360.00	5 mil			4.00	18.00:5.50:5.50...	4.00	0.10	0.10
DPr	DP_M1_MDQS13	500.00	Include	360.00	5 mil			4.00	18.00:5.50:5.50...	4.00	0.10	0.10
DPr	DP_M1_MDQS14	500.00	Include	360.00	5 mil			4.00	18.00:5.50:5.50...	4.00	0.10	0.10
DPr	DP_M1_MDQS15	500.00	Include	360.00	5 mil			4.00	18.00:5.50:5.50...	4.00	0.10	0.10
DPr	DP_M1_MDQS16	500.00	Include	360.00	5 mil			4.00	18.00:5.50:5.50...	4.00	0.10	0.10

Layout – Stackup Definition

- Desired layer count
- Balanced layer count, signal layers vs. planes
- Thickness
- Controlled impedance
- Signal to plane reference
- Board frequency, Ground return paths
- Material type – Tg, Dk, CTE

Layout – Example 8 Layer Stack-up

SIG

GND

SIG

PWR

GND

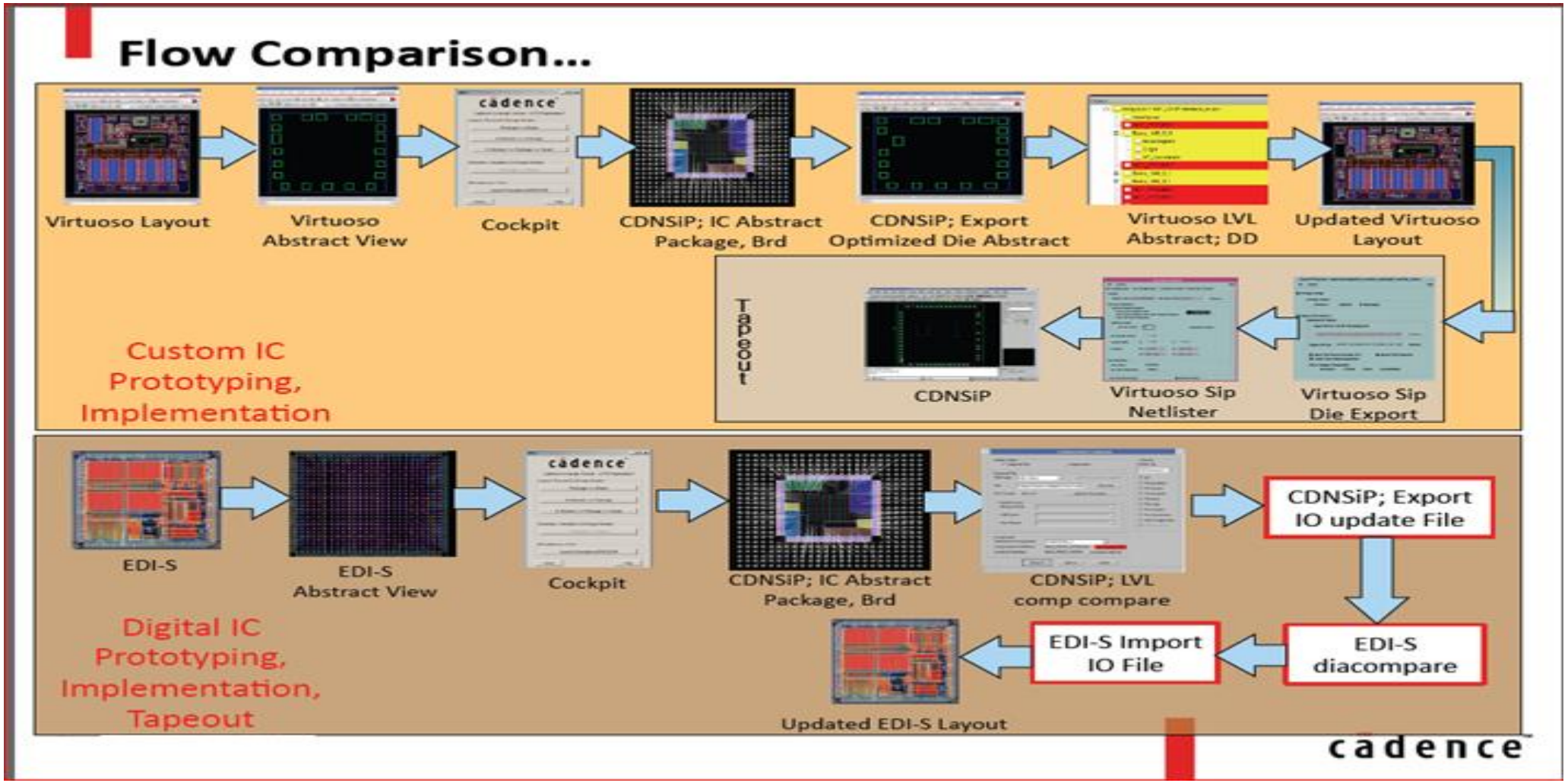
SIG

GND

SIG

- Power Bus Switching Noise will be on the order of a few milivolts
- E-Field and H-Field spread will be at or near zero
- Impedance control on inner layers will be extremely tight and consistent
- CrossTalk on inner layers will be extremely low
- Due to tight field coupling, risk of EMI problems are very low, however boards could be more expensive

Layout – Co-Design BGA Ball-Map optimization



Design for Manufacturing / Assembly (DFM/DFA)

Design for Manufacturing is the engineering art of designing products in such a way that they are easy to manufacture.

DFM

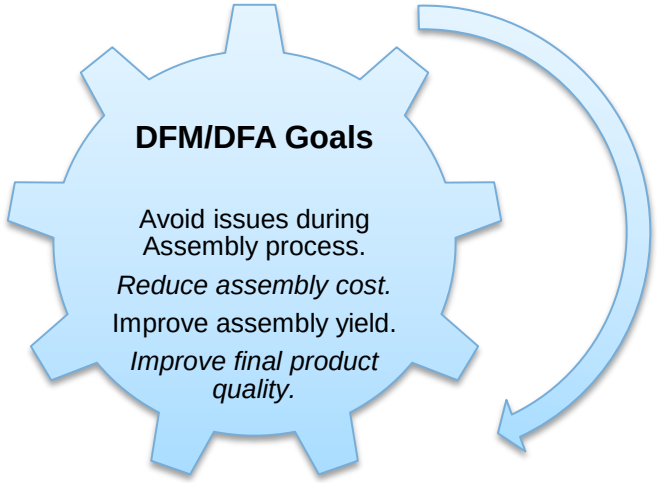
Analysis to define tolerances, rules and manufacturing checks related to the PCB fabrication process.

(Performed only to PCB without components)

DFA

Boards are analyzed with ease of assembly in mind.

(Performed to PCB plus components)



Keep it Simple… The more manufacturing processes are involved the more complex and expensive it gets.

Design for Manufacturing (DFM), Assembly (DFA), and Test (DFT)

- Schematic review
- JTAG, single chain or multiples to match wiggler/software capabilities
- Output Enables pulled up / down through a resistor
- Clock driver disables – can tester override onboard clocks, buffers
- Layout/Placement Review – Heavy parts and BGAs on one side
- Examine the physical attributes of the board as it is designed to work within the system: cable access and connectors and heat sinks competing with other physical attributes
- Consideration of Flying Probe or ICT / MDA and Functional Test
- Tools to automate the DFA/DFM process such as Valor
- Does it boot by itself or require external help: this impacts manufacturing cost and closely ties the software integration to hardware design/accessibility
- Pre-programmed vs. inline-programmed devices
- Time vs. inventory costs with multiple programmed parts

Fabrication and Assembly

- Domestic vs. International fabrication:
  - Materials availability and Leadtime
  - Real Cost: PCB+parts+labor+shipping+rework+ECOs
  - Comparable regional part sources
  - Customs and regulations
- Component technology, cost versus requirements
- Understanding supplier capabilities and strengths
  - Will they need to outsource any necessary operations
- Will the manufacturer drop ship to your customers
- Packaging for retail shelves versus direct delivery to your customer

Test

- Test automation: costs, benefits, subjective judgments of “OK” versus a program-defined / measured PASS/FAIL
- UnderTesting: samples only or 100%
- OverTesting: measurement changes though a product lifecycle, tolerances, clock/volt/temp margining
- Cost Benefit Analysis: Flying Probe / MDA / ICT / FT / no test; or a logical, layered combination of the above
- Fixtured test versus HMU versus fixtureless
- Shift-Left failure detection: early cost avoidance versus process hits, later test means more value has been added by the process but the device is more complete

Software Integration

- Drop in box software packages versus pre-installed software
- Build to order or single configuration
- Customer expectation modeling => OOBE/OBA
  - Does OBA feed into your manufacturing or design process
- Ensure address mapping validated with the software team during the schematic phase
- Breaking the seal at the customer
  - Does the unit boot into a demo mode
  - A complete operating environment
  - Or is the unit ready for customer code installation at initial power-up

Regulatory Compliance

- Know product destination countries and product use to understand compliance and testing
- Customer Expectations / Options
  - Pre-certified for integration by customers
  - Will certify by customers after integration
- Self certification
  - In-house lab and expertise (cost versus convenience)
  - External Agency Support
- Pre-scan before formal (co$tly) testing
- Design for Safety (High Voltages) / Emissions / Susceptibility
- Unintentional versus Intentional Emitter
- Some countries have additional requirements for certain items such as batteries and PSE certification for power supplies in Japan

SECURE CONNECTIONS
FOR A SMARTER WORLD

ATTRIBUTION STATEMENT