FTF 2016
TECHNOLOGY FORUM

HIGH-SPEED SERDES MODELING FOR THE PCB AND SYSTEM ENVIRONMENT

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FTF-DES-N1855
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AGENDA

- SERDES Features
- IBIS-AMI Background
- Tool for SERDES Validation: QCVS
- Basic TX EQ and RX EQ Simulations
- Channel Analysis and Printed Circuit Board Considerations
- IBIS-AMI Simulation Examples

SERDES FEATURES

Highlights

- Higher Speed SerDes busses operate with a closed eye at the pin of the Receiver in some cases
  - RX EQ will help open the eye
  - But RX EQ is producing a signal that is not seen at the pin
    - How to model what is happening inside the die to offset the losses in the channel and the closed eye that they produce?

- IBIS-AMI modeling finer details
  - IBIS-AMI models proprietary on-die RX EQ
  - TX EQ effects with RX EQ

- SERDES-based tool for viewing RX after EQ
  - Jitter Scope tool
  - TX pattern generation helpful, too

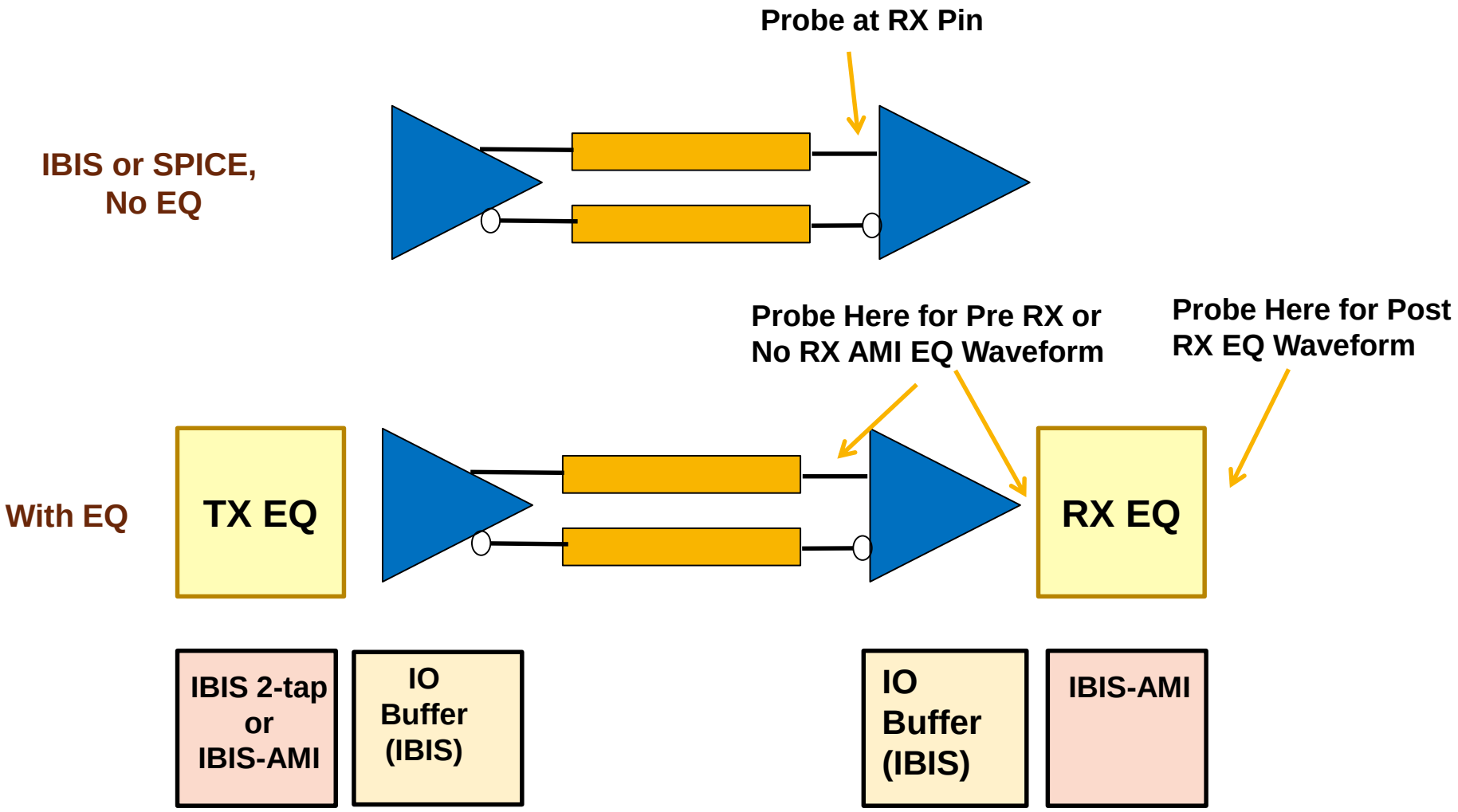
- PCB Design at 10Gbps
  - Every detail matters in complex channels
  - Manage Return Loss

IBIS-AMI BACKGROUND

IBIS-AMI Model Sections

- IBIS-AMI model
  - Top level is “.ibs” file, like standard IBIS
    - Has pin listing, signal to model name mapping, diff pair listing, etc.
    - Uses standard analog modeling for driver impedance, capacitive loading, edge rates, etc.
      - “analog IBIS”
  - Parameter file – “.ami” file
    - Text file that is readable by user
    - Sets values to be used in DLL model file
  - DLL
    - Where algorithms are modeled in AMI language
    - Compiled to protect the proprietary TX and RX model information
    - IBIS >= 5.1 compliant allows it to run in multiple tools

Pre- and Post-RX EQ Waveform Probing Locations



Digital Networking IBIS and IBIS-AMI Models Overview

- Slower Speed SERDES (<= 3.125 Gbps)
  - Uses IBIS
  - Does not require IBIS-AMI, since no RX EQ
  - Uses TX EQ only
    - TX EQ modeled using driver schedule
      - Add/subtracts model data to produce de-emphasis
      - Only one model per bit period

- Higher Speed SERDES (>= 5 Gbps)
  - Uses IBIS-AMI
  - First IBIS-AMI model was for 5-6 Gbps applications
    - Also used for slower speed protocols using that IP
  - Second IBIS-AMI model was for 10 Gbps applications
    - Also, used for slower speed protocols using that IP
      - Models SGMII at 1.25 Gbps up to the 10.3125 Gbps protocols

- FSL IBIS-AMI model is released/controlled through NDA

TX IBIS-AMI MODEL BACKGROUND

SerDes IBIS-AMI Model

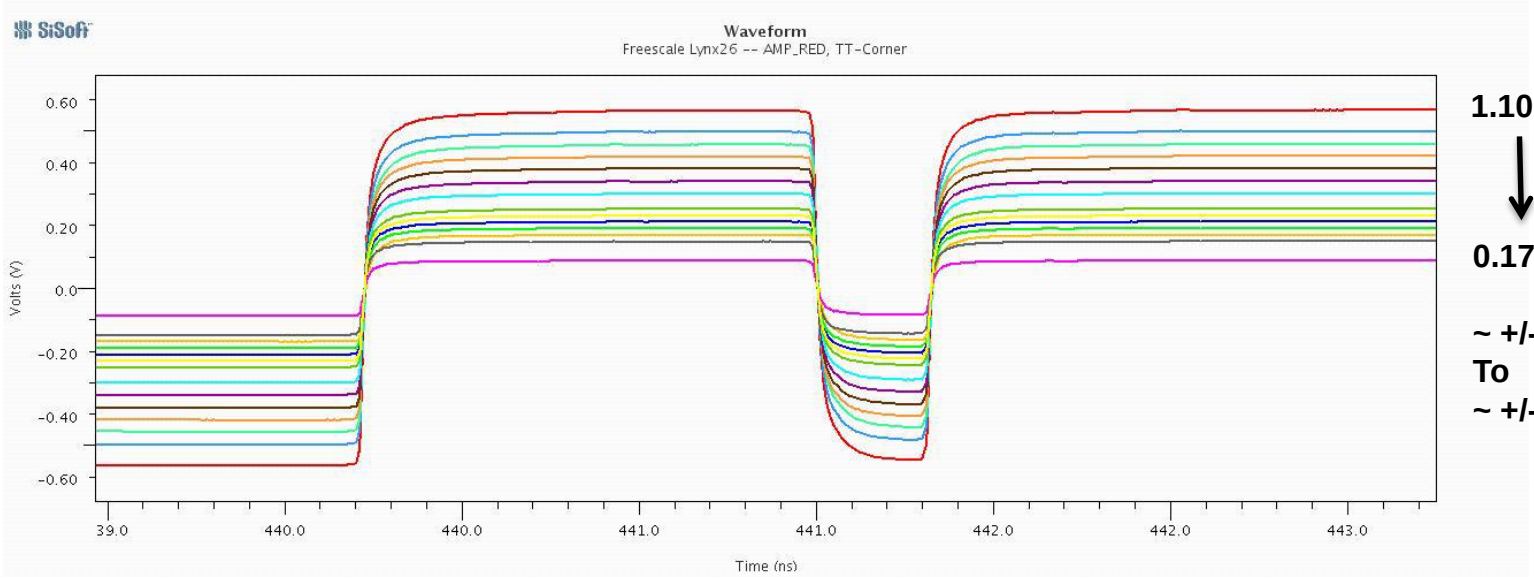
- TX Model includes EQ (TEQ_TYPE)
  - No Tap
  - 2-Tap
  - 3-Tap or 4-Tap
- TX Model includes Amplitude Adjustment (AMP_RED)
  - Matches to protocol
- TX Model: De-emphasis levels (RATIO_PST1Q)
  - Ranges from: 0 to 2-3x
- RX Model: Includes Adaptive EQ
  - May have ability to communicate with TX (Backchannel)

TX EQ – AMP_RED: Adjust Swing of TX Signal

AMI Model:

```
(AMP_RED     (List 32 0 1 3 2 6 7 16 17 19 18 22 23 31)(Usage In)(Type Integer)(Default 0)
                  (Labels "10 0000 (d32): 1.100 X Full Swing" "00 0000 (d0): 1.000 X Full Swing"
                          "00 0001 (d1): 0.917 X Full Swing"  "00 0011 (d3): 0.840 X Full Swing"
                          "00 0010 (d2): 0.752 X Full Swing"  "00 0110 (d6): 0.667 X Full Swing"
                          "00 0111 (d7): 0.585 X Full Swing"  "01 0000 (d16): 0.500 X Full Swing"
                          "01 0001 (d17): 0.458 X Full Swing" "01 0011 (d19): 0.420 X Full Swing"
                          "01 0010 (d18): 0.376 X Full Swing" "01 0110 (d22): 0.333 X Full Swing"
                          "01 0111 (d23): 0.292 X Full Swing" "01 1111 (d31): 0.170 X Full Swing")
```

(Description "**Transmitter Output Amplitude Control**"))



1.100X

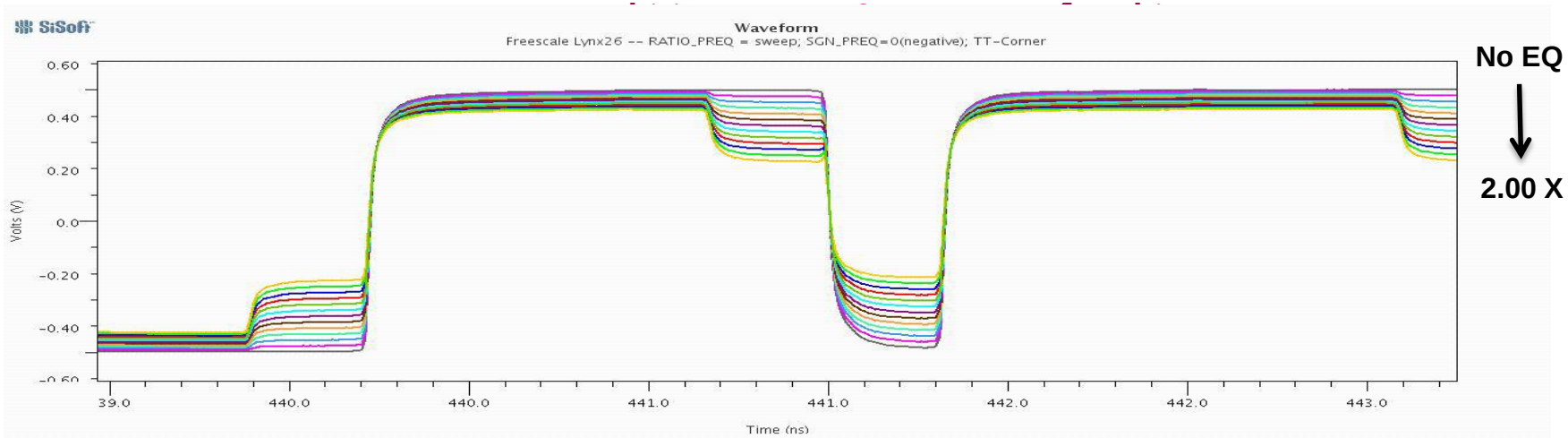
↓

0.170X

~ +/- 550 mV
To
~ +/- 85 mV

SerDes TX: Pre-Cursor in AMI Model

```
AMI_Model:
(RATIO_PREQ  (List 0 1 2 3 4 5 6 7 8 9 10 11 12)(Usage In)(Type Integer)(Default 0)
                  (Labels "0000 (d0): No equalization" "0001 (d1): 1.04 X relative amplitude"
                          "0010 (d2): 1.09 X relative amplitude"  "0011 (d3): 1.14 X relative amplitude"
                          "0100 (d4): 1.20 X relative amplitude"  "0101 (d5): 1.26 X relative amplitude"
                          "0110 (d6): 1.33 X relative amplitude"  "0111 (d7): 1.40 X relative amplitude"
                          "1000 (d8): 1.50 X relative amplitude"  "1001 (d9): 1.60 X relative amplitude"
                          "1010 (d10): 1.71 X relative amplitude" "1011 (d11): 1.84 X relative amplitude"
                          "1100 (d12): 2.00 X relative amplitude")
                  (Description "Transmitter Pre-Cursor Control"))
 (SGN_PREQ    (List 0 1)(Usage In)(Type Integer)(Default 1)
                  (Labels "0 = Negative"  "1 = Positive")
```



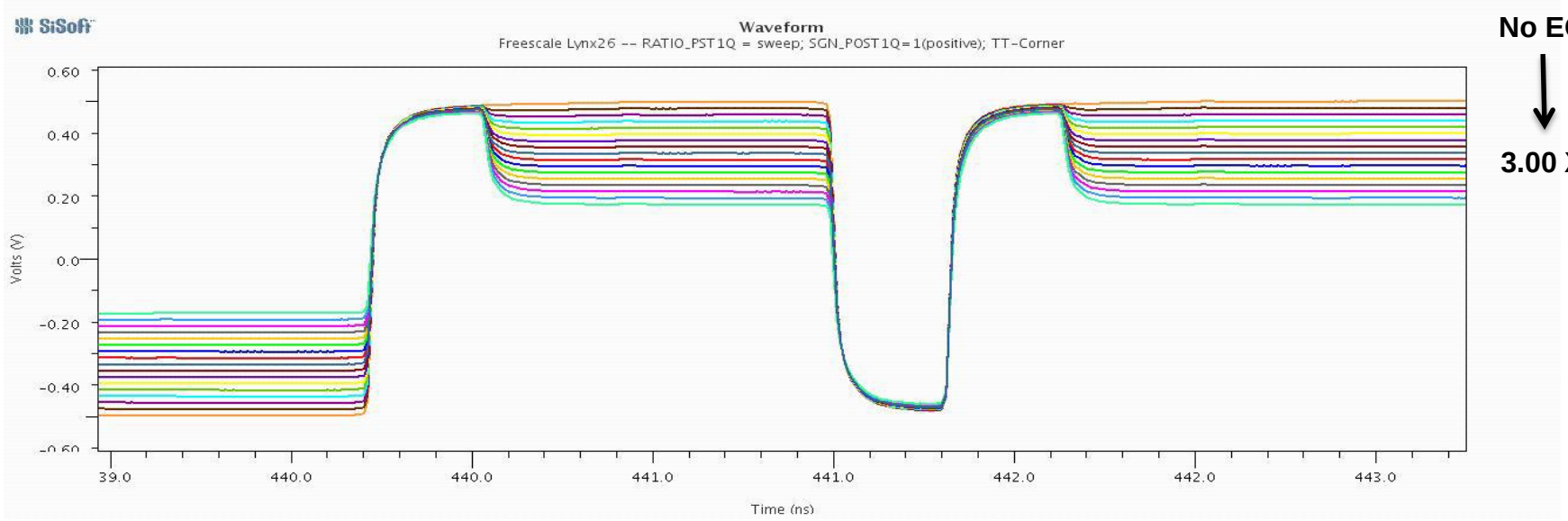
No EQ

↓

2.00 X

SerDes TX: Post-Cursor in AMI Model

```
AMI Model:
    (RATIO_PST1Q (List 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16)(Usage In)(Type Integer)(Default 12)
                 (Labels "0 0000 (d0): No equalization"            "0 0001 (d1): 1.04 X relative amplitude"
                         "0 0010 (d2): 1.09 X relative amplitude"  "0 0011 (d3): 1.14 X relative amplitude"
                         "0 0100 (d4): 1.20 X relative amplitude"  "0 0101 (d5): 1.26 X relative amplitude"
                         "0 0110 (d6): 1.33 X relative amplitude"  "0 0111 (d7): 1.40 X relative amplitude"
                         "0 1000 (d8): 1.50 X relative amplitude"  "0 1001 (d9): 1.60 X relative amplitude"
                         "0 1010 (d10): 1.71 X relative amplitude" "0 1011 (d11): 1.84 X relative amplitude"
                         "0 1100 (d12): 2.00 X relative amplitude" "0 1101 (d13): 2.18 X relative amplitude"
                         "0 1110 (d14): 2.40 X relative amplitude" "0 1111 (d15): 2.66 X relative amplitude"
                         "1 0000 (d16): 3.00 X relative amplitude")
                 (Description "Transmitter Post-Cursor Control"))
```



No EQ

↓

3.00 X

SerDes TX: Post-Cursor → Translate Ratio into dB PCI Express Calls for -3.5 dB and -6.0 dB Levels (1.5x and 2.0x)

```
AMI Model:
   (RATIO_PST1Q (List 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16)(Usage In)(Type
   Integer)(Default 12)
                (Labels
"0 0000 (d0): No equalization"
"0 0001 (d1):  1.04 X relative amplitude"
"0 0010 (d2):  1.09 X relative amplitude"
"0 0011 (d3):  1.14 X relative amplitude"
"0 0100 (d4):  1.20 X relative amplitude"
"0 0101 (d5):  1.26 X relative amplitude"
"0 0110 (d6):  1.33 X relative amplitude"
"0 0111 (d7):  1.40 X relative amplitude"
"0 1000 (d8):  1.50 X relative amplitude"
"0 1001 (d9):  1.60 X relative amplitude"
"0 1010 (d10): 1.71 X relative amplitude"
"0 1011 (d11): 1.84 X relative amplitude"
"0 1100 (d12): 2.00 X relative amplitude"
"0 1101 (d13): 2.18 X relative amplitude"
"0 1110 (d14): 2.40 X relative amplitude"
"0 1111 (d15): 2.66 X relative amplitude"
"1 0000 (d16): 3.00 X relative amplitude")
```

Relative Amplitude	dB
No EQ	0.0
1.04:1	-0.3
1.09:1	-0.7
1.14:1	-1.1
1.20:1	-1.6
1.26:1	-2.0
1.33:1	-2.5
1.40:1	-2.9
1.50:1	***-3.5***
1.60:1	-4.1
1.71:1	-4.7
1.84:1	-5.3
2.00:1	***-6.0***
2.18:1	-6.8
2.40:1	-7.6
2.66:1	-8.5
3.00:1	-9.5

RX IBIS-AMI MODEL BACKGROUND

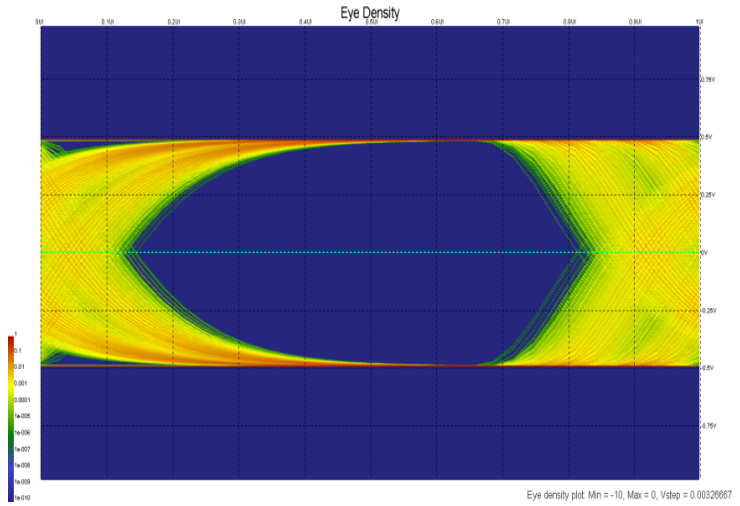
Simulate to Optimize RX EQ

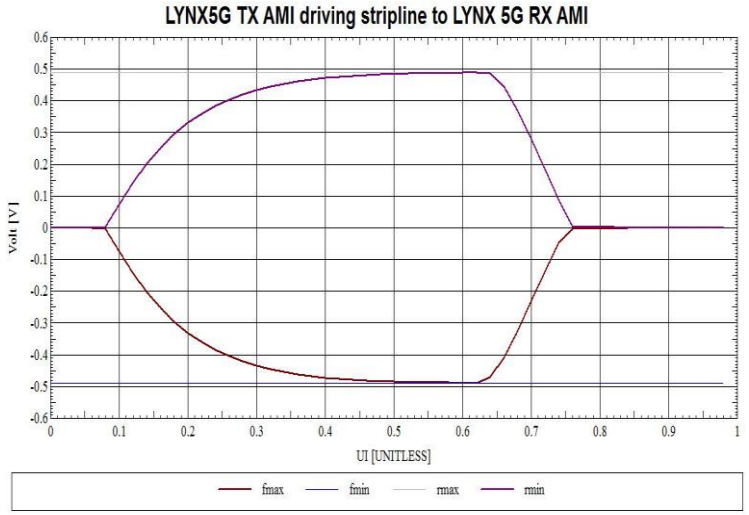
- RX EQ
  - Simulation to provide visibility at Post RX EQ
  - Typically where data eye recovery takes place

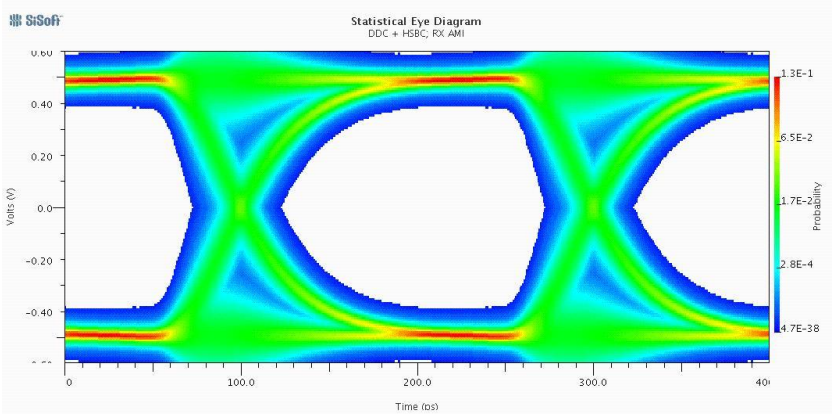
  - Often Adaptive
    - May have overrides
    - Freescale is adaptive (finds best values for its RX EQ parameters)

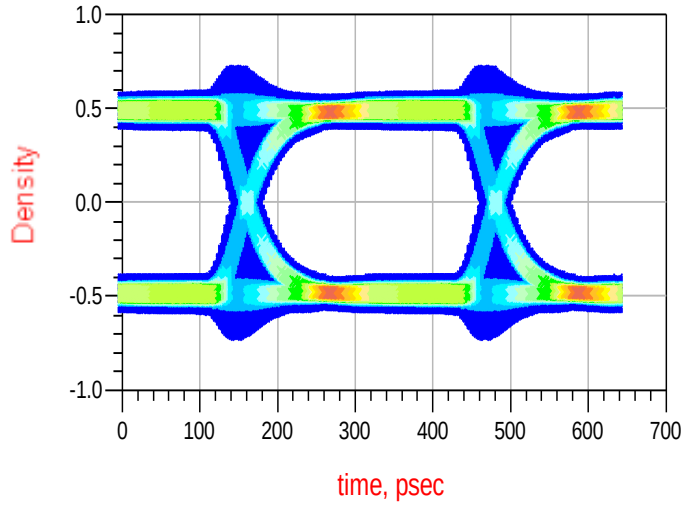
  - Instructive to look at data eye before/after RX EQ in some cases

Comment: 5G IBIS-AMI Post RX EQ

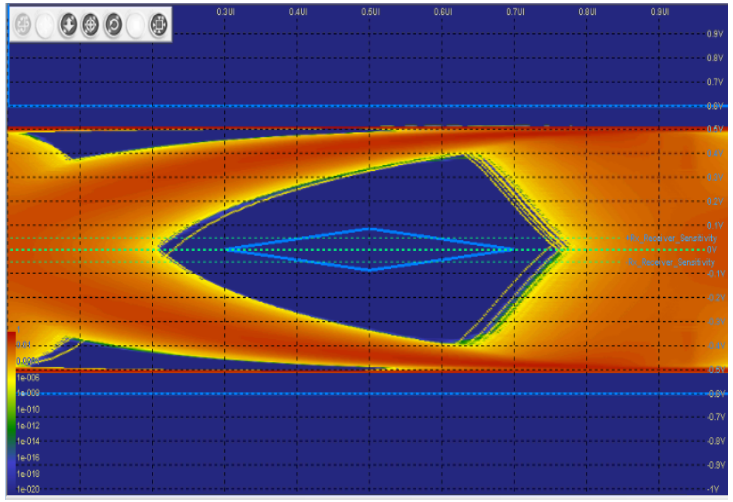


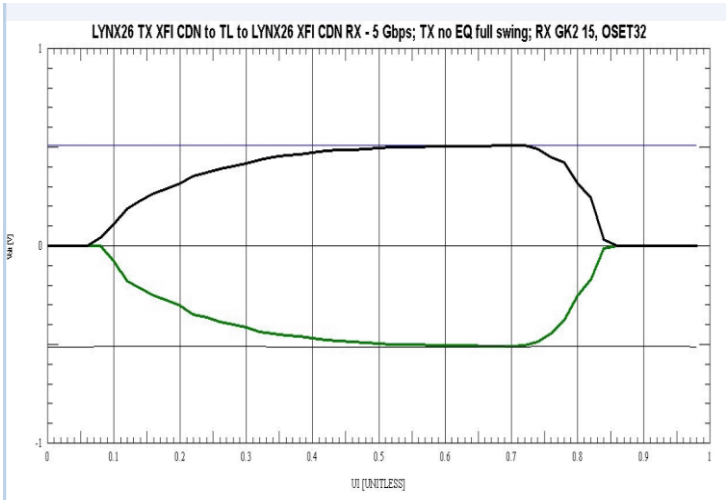


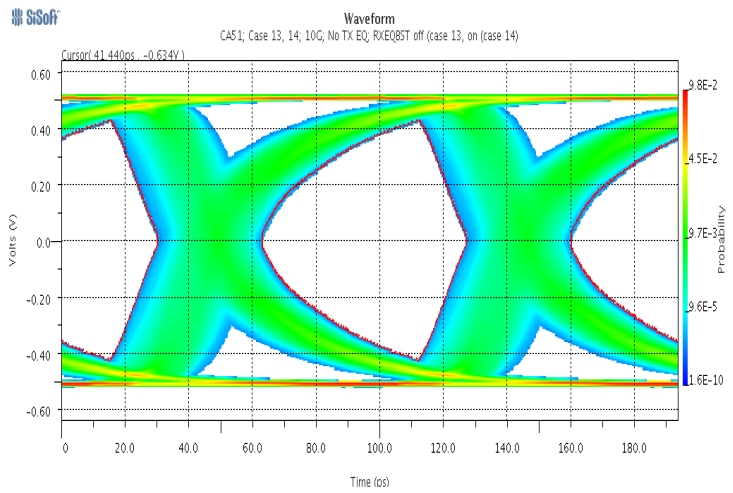


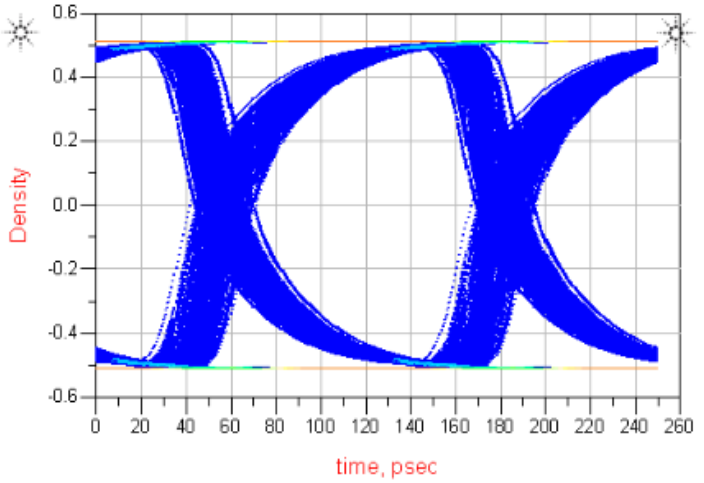


Comment: 10G IBIS-AMI Post RX EQ









SerDes IBIS-AMI Correlation

- 95+% Figure of Merit between SiSoft Simulation Freescale Internal SPICE simulation

5Gbps on left

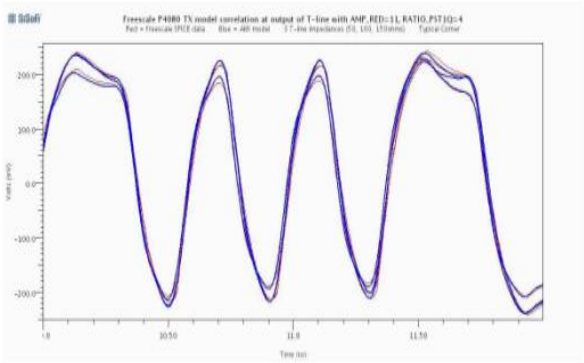


Figure 18: TX waveform at Load; Amplitude=11, Equalization=4, TT-PVT Corner

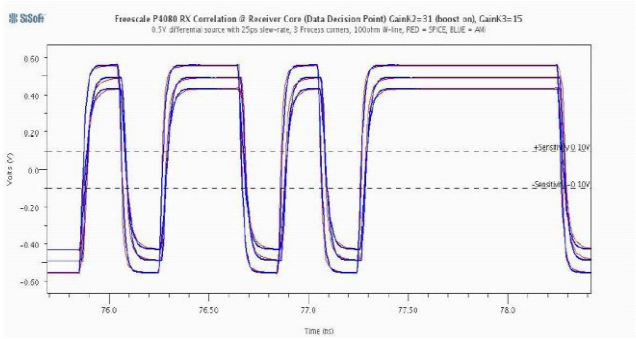


Figure 55: IBIS-AMI correlation, 500mV input swing w/ 25ps rise-time, K2=31, K3=15

10Gbps on right

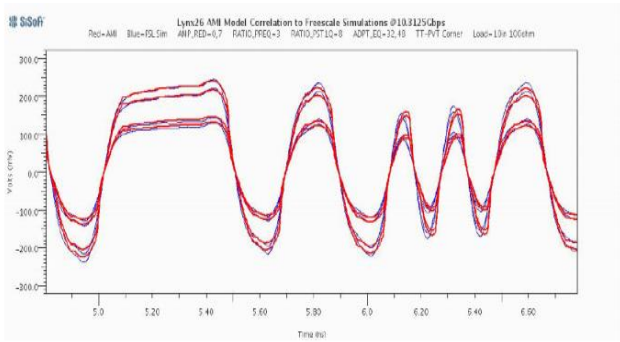


Figure 20: TX waveform at load: 10.3125Gbps; AMP_RED=0,7; RATIO_PREQ=3; RATIO_PST1Q=8; ADPT_EQ=32,48; 100ohm etch; TT-PVT Corner

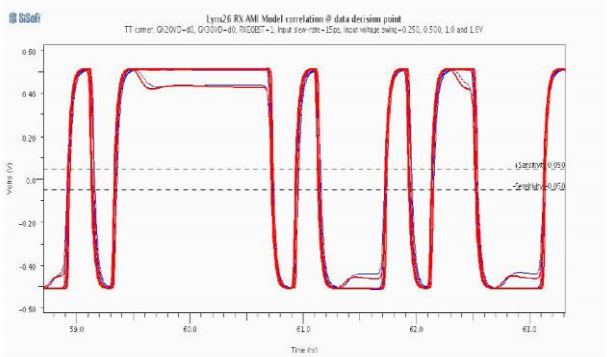


Figure 41: Waveform at RX Core; GK2=d0; GK3=d0; BST=1; Slew=15ps; TT-PVT corner

TOOL FOR SERDES VALIDATION: QCVS

Special Focus on Jitter Scope Tool

QCVS SerDes Documents: User's Guide and App Note (AN5119)

QorIQ Configuration and Validation Suite SerDes Tool User Guide

Document Number: QCVSSerDesUG
Rev. 4.2, 04/2015

Freescale Semiconductor
Application Note

Document Number: AN5119
Rev. 2, 01/2016

SerDes Configuration and Validation Tool Companion

Contents

1 Introduction

This application note is a companion document to the SerDes Configuration & Validation Tool User Guide. It is provided to assist those engineers wishing to use the Tx Equalization, Built-In Self Test (BIST), and Jitter Scope test features of the QCVS SerDes validation tool. The 10 G SerDes block is the basis for describing the technical topics. The 10 G SerDes is in the T4240, B4860, T2080, P5040, and T1xx QorIQ multicore processors families.

The fundamental blocks of a SerDes are a transmitter and a receiver. The transmitter serializes the parallel data, performs transmit equalization, and sends serial differential pair signals to the output pad and then across the channel (the path between the transmitter and receiver, that is, electrical components, printed circuit board, traces, cables, and so on) to the receiver. The receiver collects the serial data, extracts a clock from the data, de-serializes the data, and performs equalization if necessary.

The Freescale 10 G SerDes implements both transmit equalization and receive equalization. Transmit and receive equalization is provided to compensate for lossy channels. An example is to take a single pulse (1 bit) and send it through a lossy channel. It starts out as a definite single pulse, but, by traversing the channel, it develops "tails" on either side of the received pulse, as shown in the following figure.

QCVS User's Guide: SerDes Validation

Chapter 3
SerDes Validation

After a SerDes configuration has been created in terms of protocol/speed, lane receive and transmit, and PLL allocation, the question is whether that configuration will perform reliably under the intended type of traffic. For that, the SerDes validation capability comes into the picture.

The validation relies on SerDes hardware block built-in, programmable test capabilities that are used to verify the block under different traffic conditions. The validation programs the built-in testing capabilities, and then runs a series of tests. The results of the tests are displayed in a format that enables you to make a decision on whether or not the SerDes configuration is reliable. If the answer is no, then you need to adjust the SerDes configuration and run the validation again, until the reliable SerDes configuration is determined.

The added value of validation feature is:

- Easy programmability of SerDes built-in test capabilities
- One click run of the validation test, which includes applying SerDes configuration to the target, programming the test block, and collecting and aggregating the results
- A quick synthesis of the tests results in industry standard interpretations, such as data eye diagram or recovered data stream diagram

Effective Reporting
Programming to adjust parameters
Data Eye and Data Stream
- Like in AMI simulations

QCVS User's Guide: Jitter Scope

3.2.3 Jitter scope scenario

The Jitter scope scenario displays the results of the SerDes configuration validation as a diagram (data eye diagram or recovered data stream diagram).

In the Digital Loopback and External Loopback modes, the pattern is generated by the SerDes block. In case of the External mode, you can send any pattern, as long as it matches the selected length.

The figure below shows how the Jitter scope scenario works.

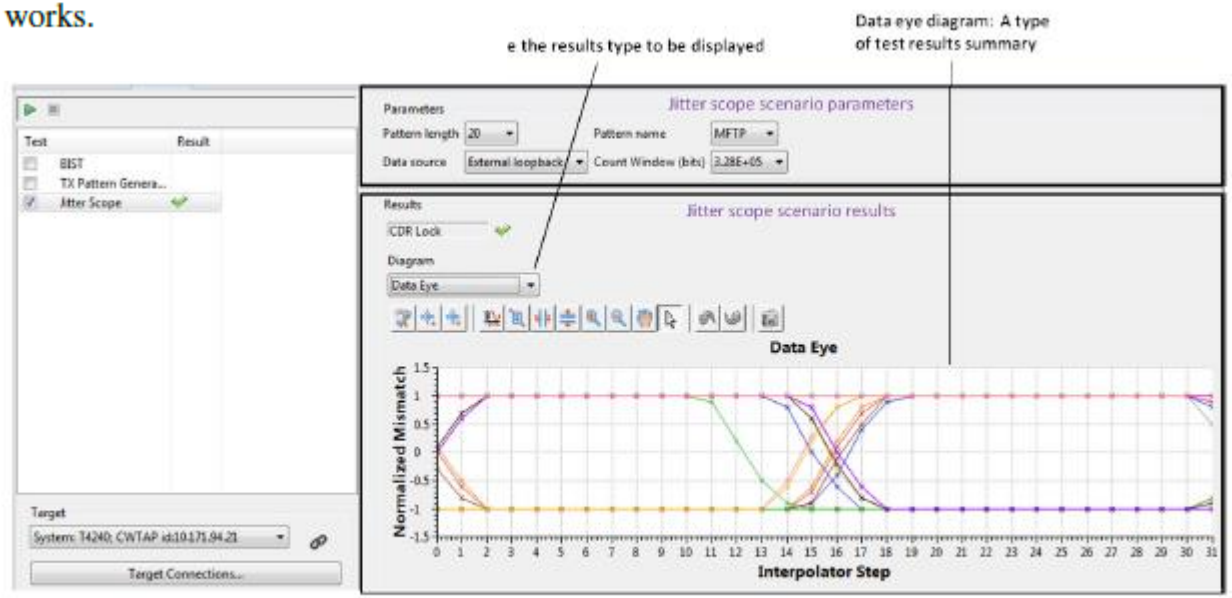


Figure 3-4. Jitter scope scenario

BASIC TX EQ AND RX EQ SIMULATIONS

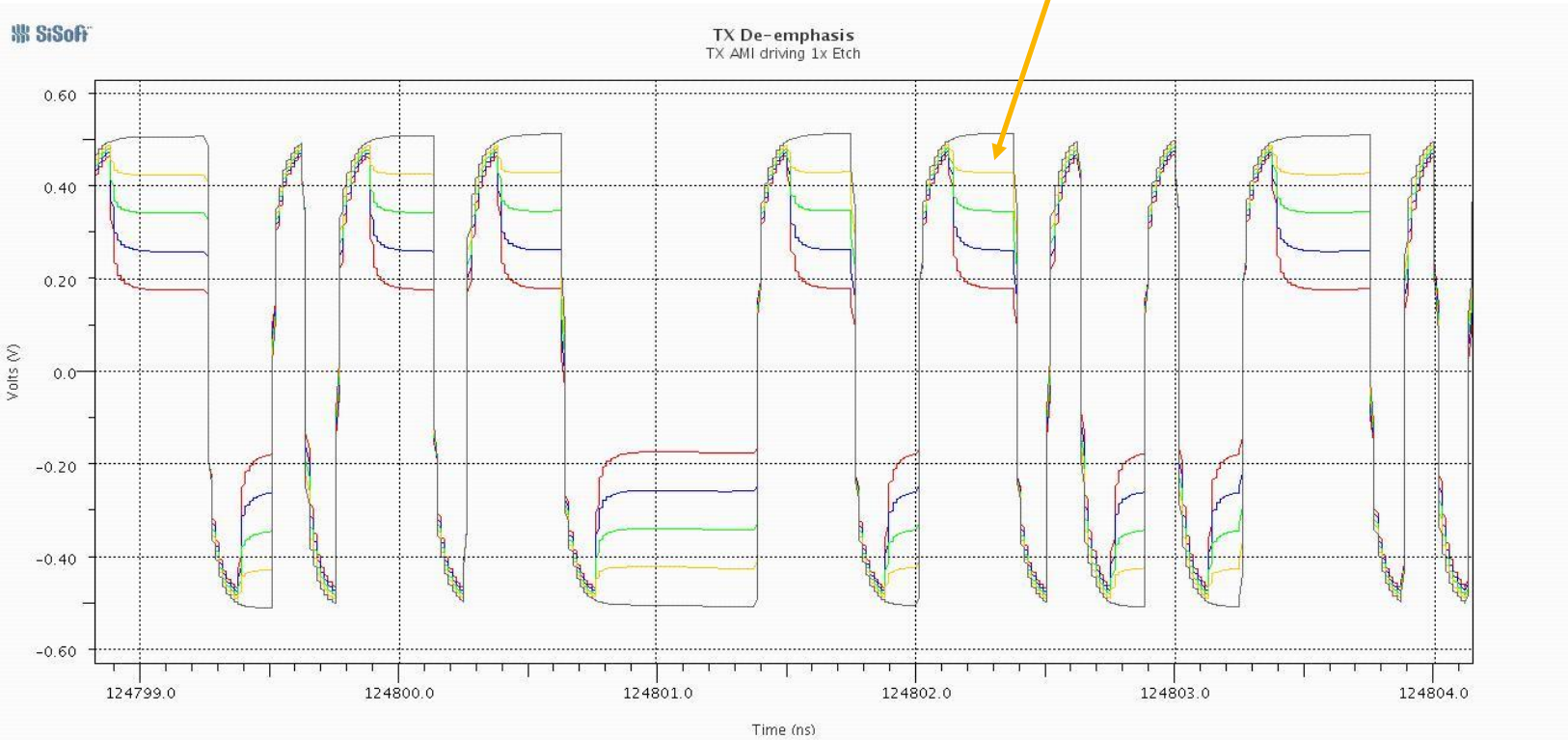
Show how SERDES TX and RX EQ works

TX EQ SIMULATIONS

Examine de-emphasis levels
Compare 1.5x and 2.0x de-emphasis waveforms

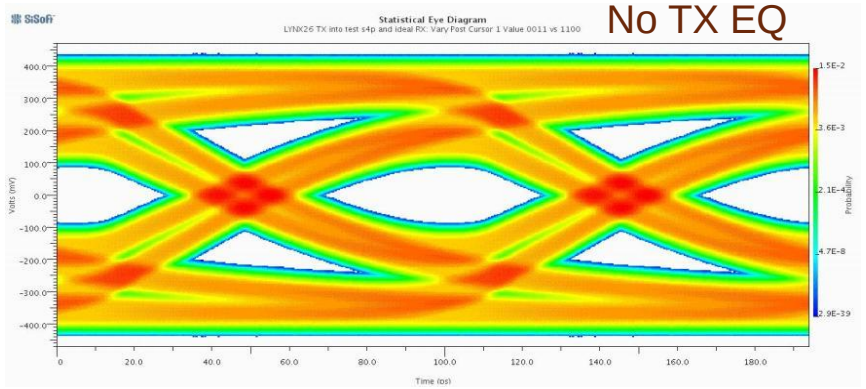
10G TX Driving 1x Etch Length @ 8G – TX AMI Only

- Compare Voltage vs. Time De-Emphasis Plots at TX
  - See how de-emphasis levels change non-transition bits (1x – 2.5x)

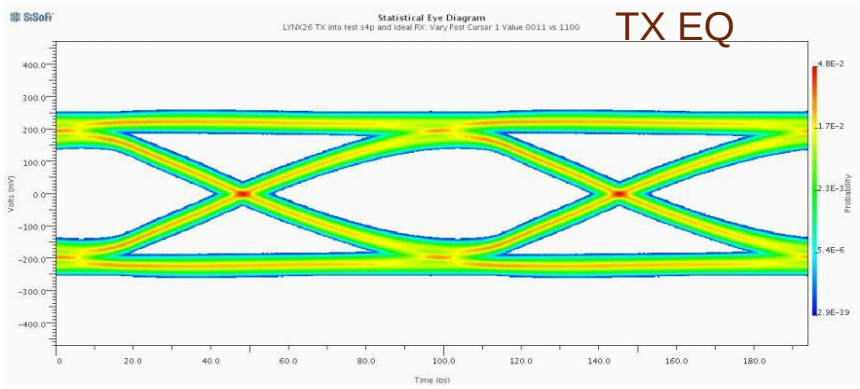


SerDes 10G TX IBIS-AMI: No TX EQ vs. TX EQ

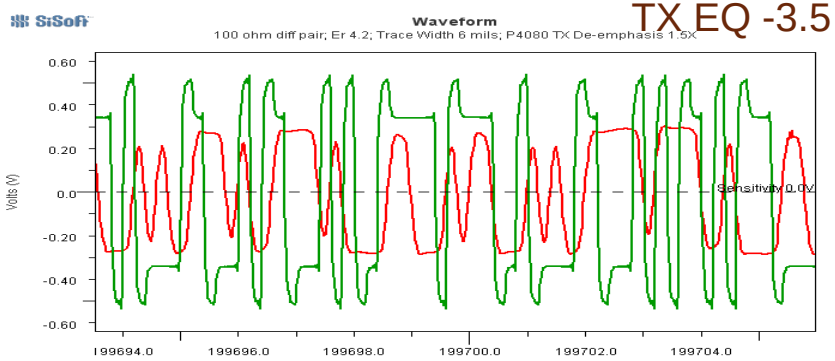
No TX EQ



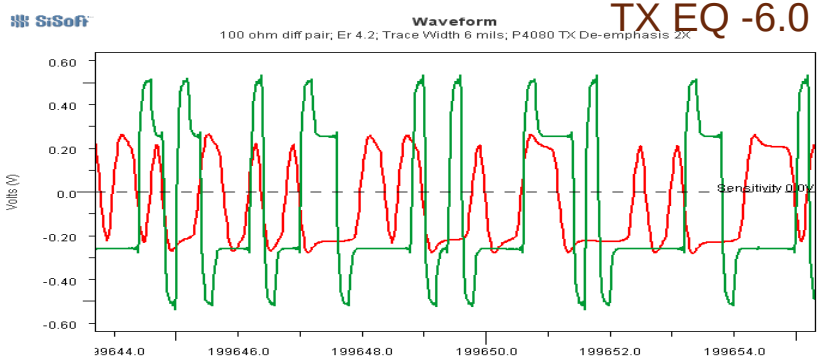
TX EQ



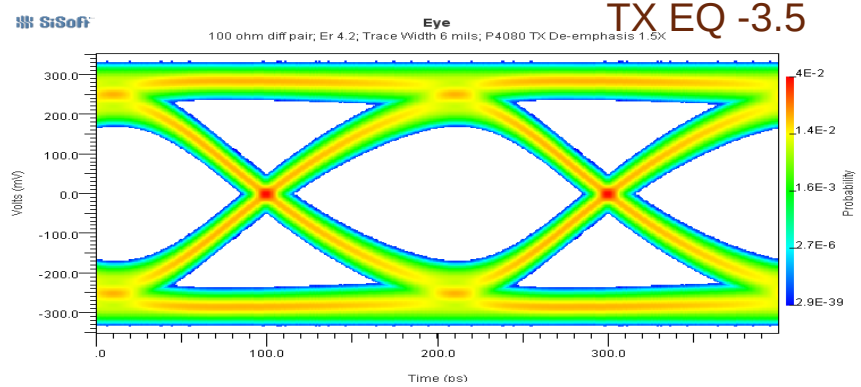
TX EQ -3.5



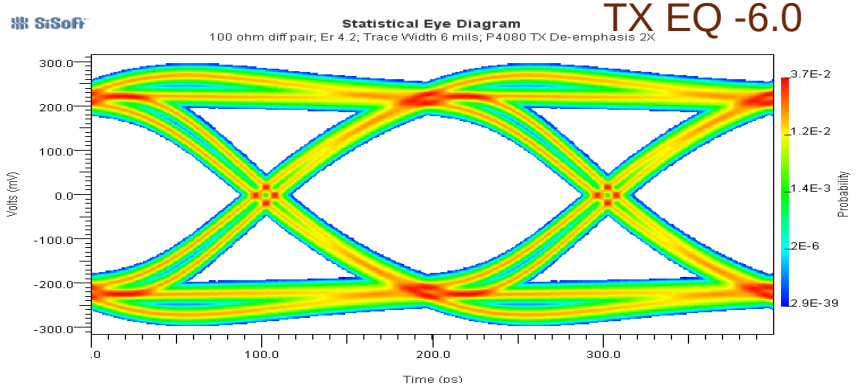
TX EQ -6.0



TX EQ -3.5

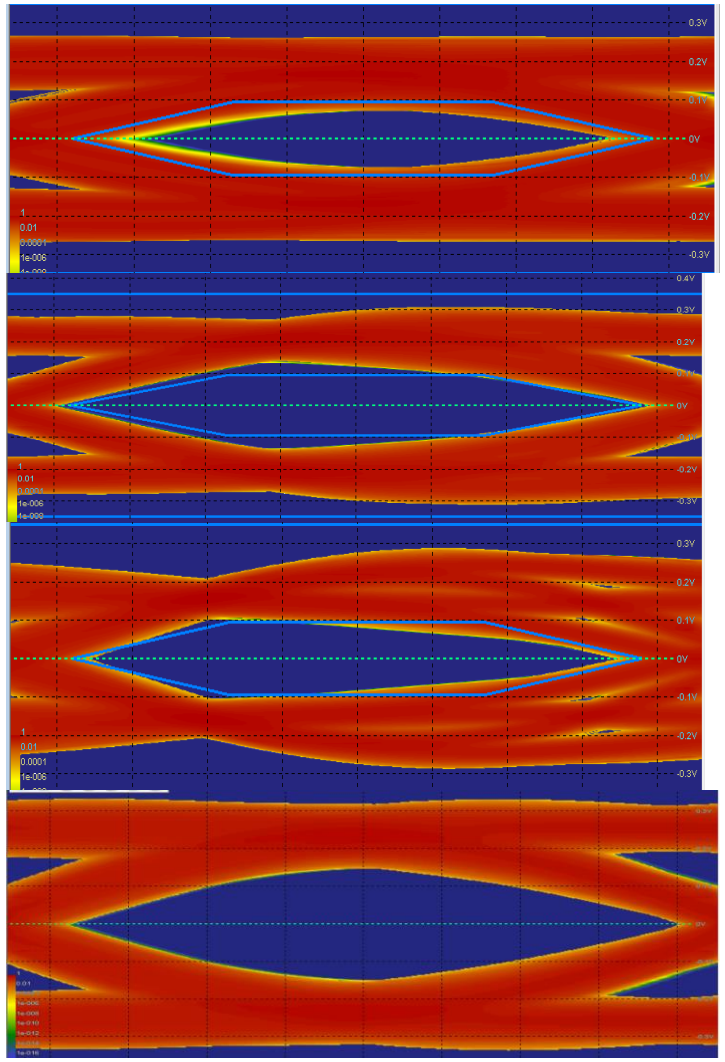


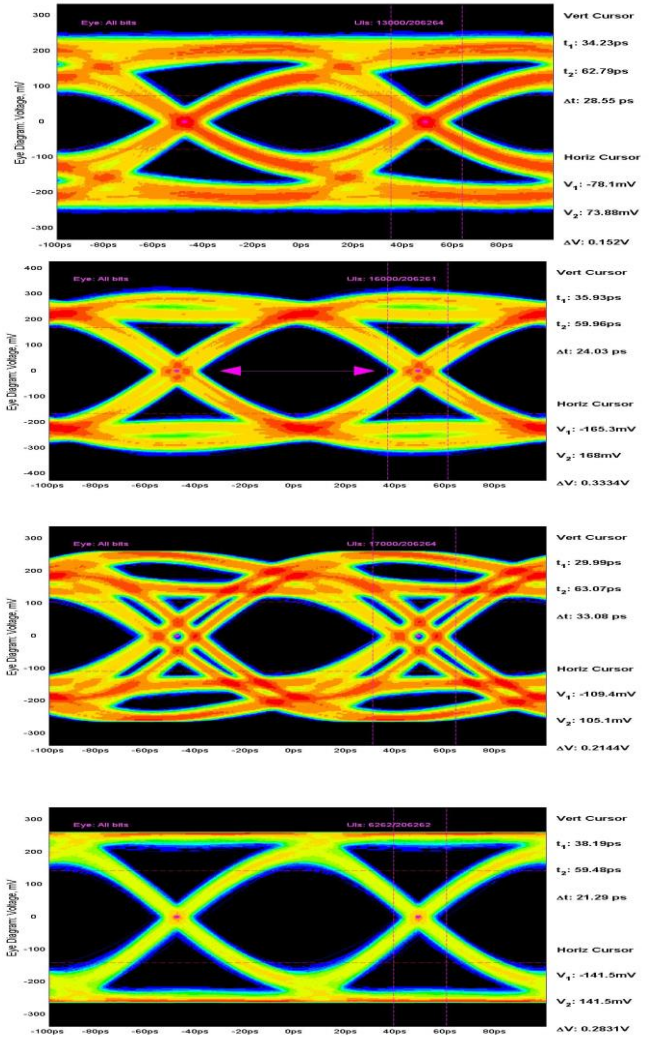
TX EQ -6.0



T4240 QDS-XFI: XFI1 TX Channel

Default XFI,
Reduced Swing vs
Full Swing; Vary TX
EQ 2.0x, 3.0x, 1.6x

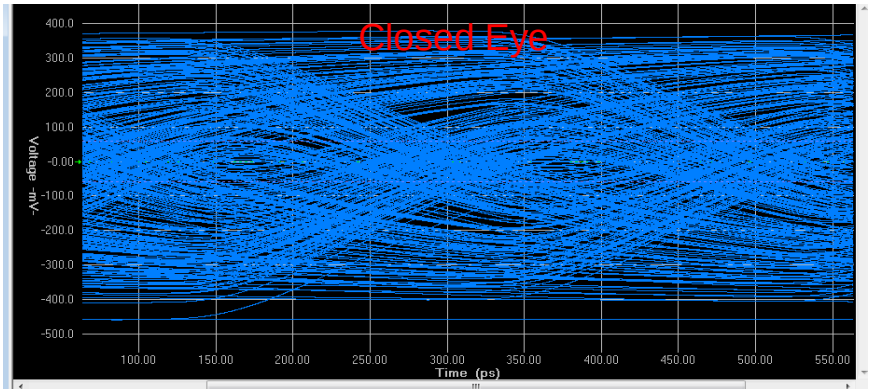


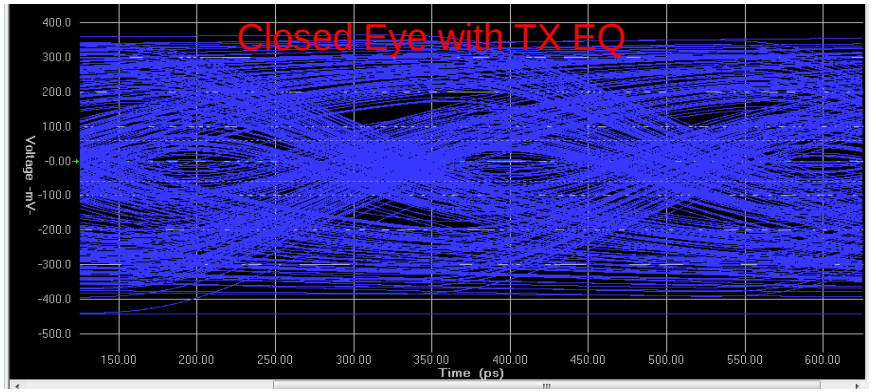


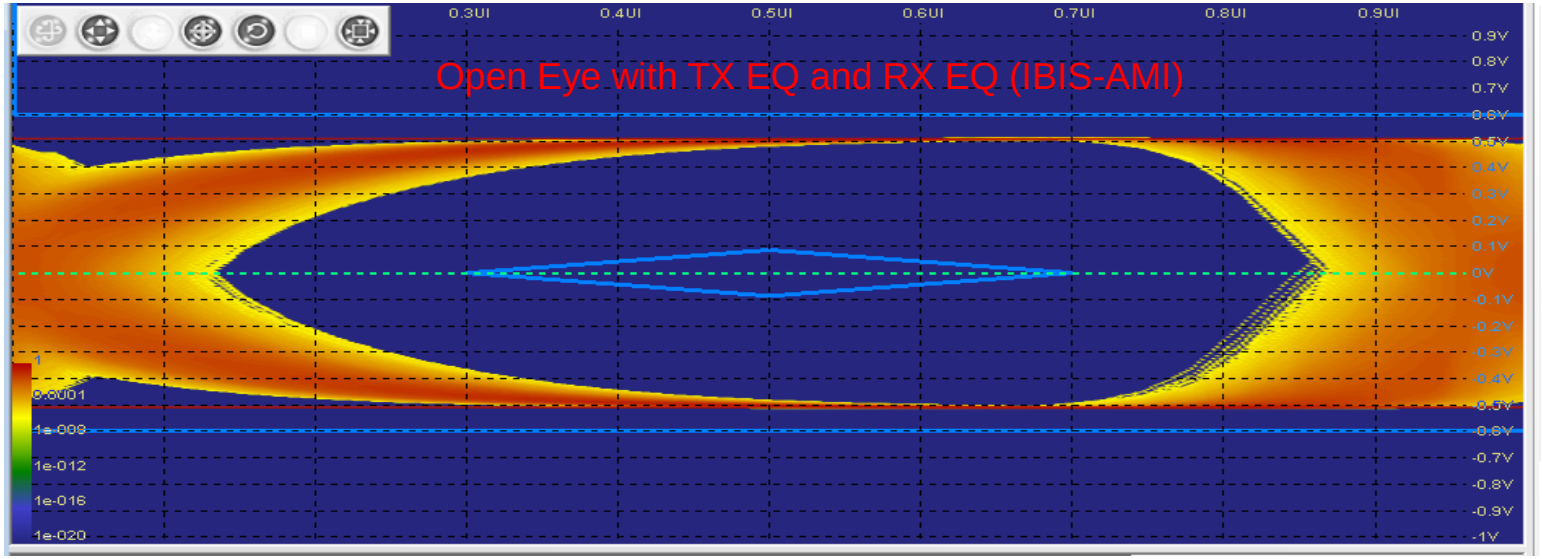
RX EQ SIMULATIONS

Examine how specific RX EQ settings change waveforms
More pronounced at greater frequency of operation

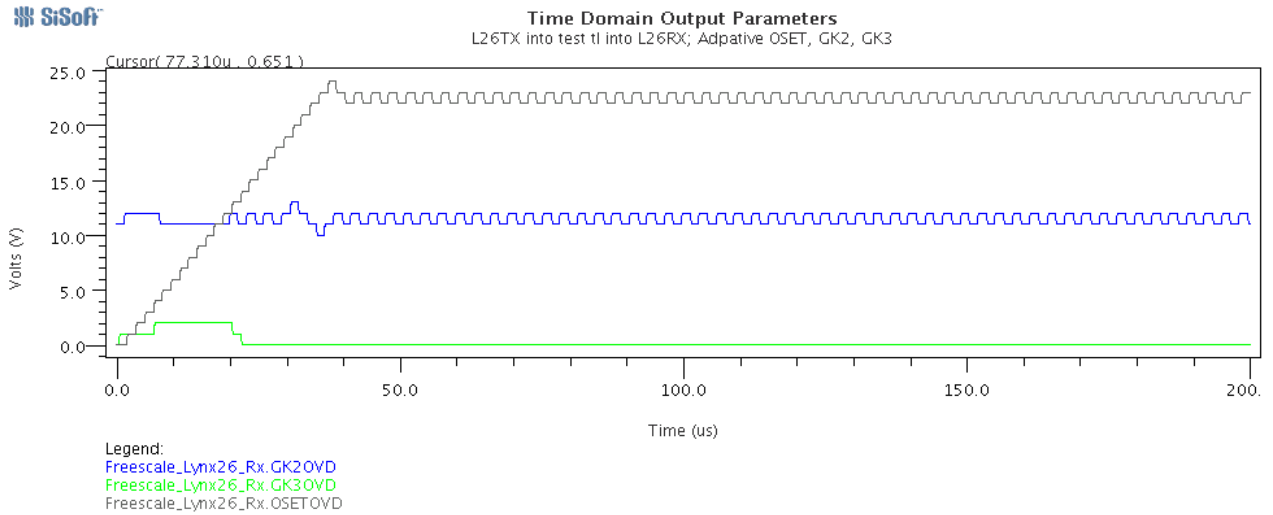
Big Improvement: Add RX EQ – Show TX EQ Eye vs. RX EQ Eye

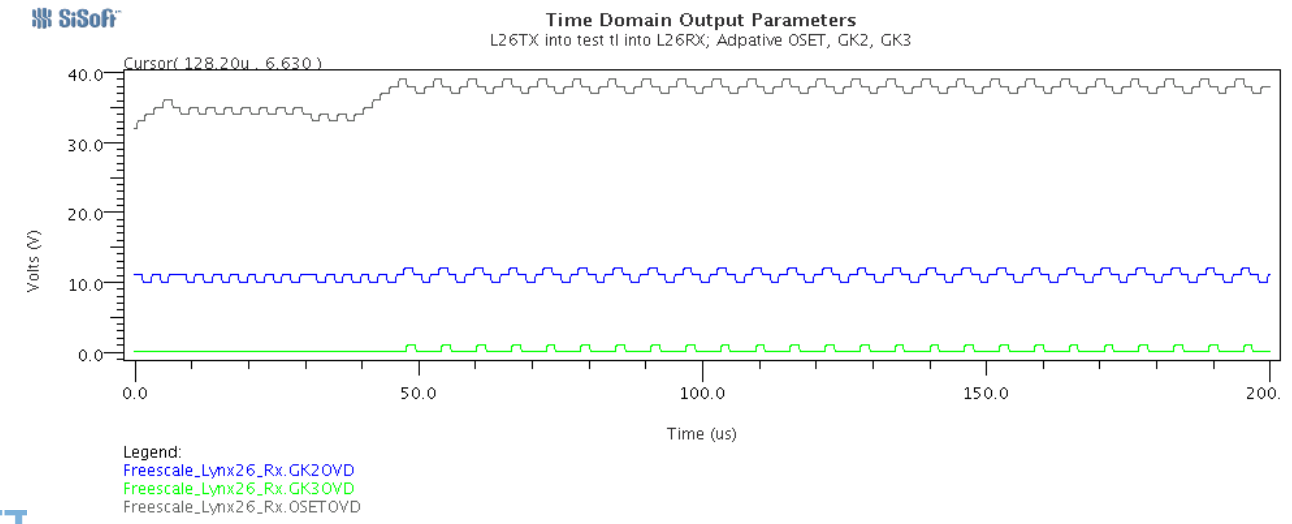






RX EQ Parameters: Watch them Adapt to Find Settings

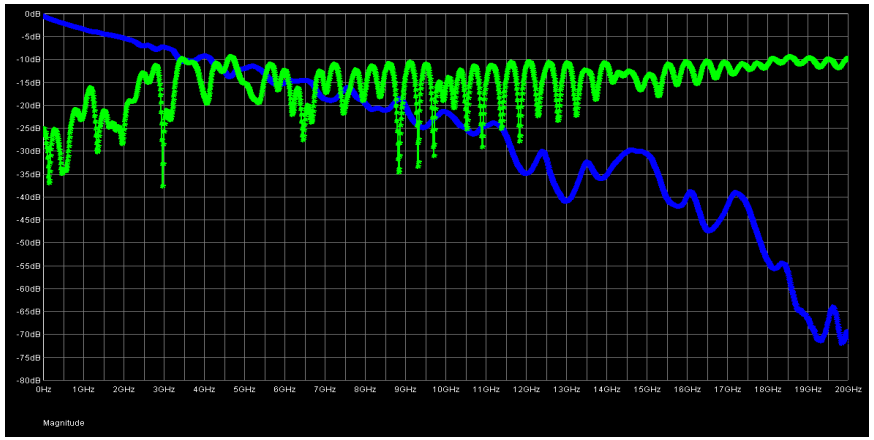




CHANNEL ANALYSIS AND PRINTED CIRCUIT BOARD CONSIDERATIONS

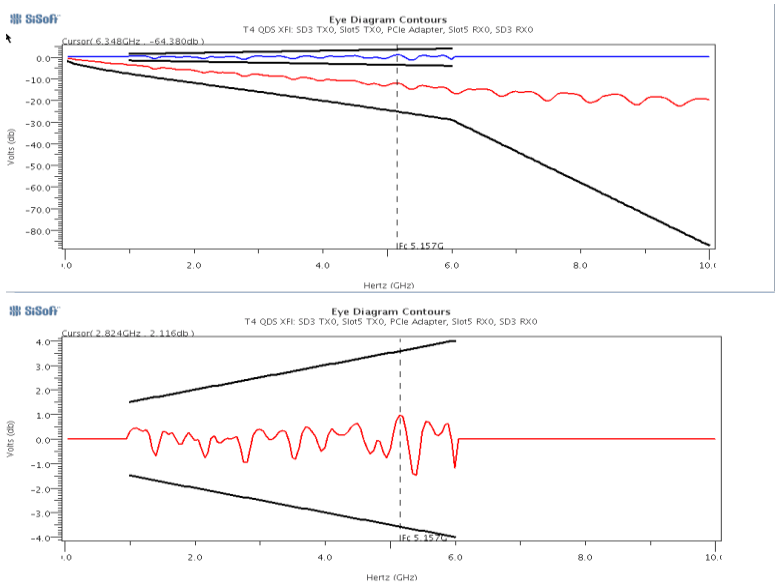
PCB Trace Losses

- PCB Interconnect losses due to traces can be seen in S-Parameter data
- Insertion Loss (S12, S21)
  - The PCB dielectric materials and traces have losses that increase with the frequency of the signal. As the SerDes bus speeds increase, the PCB losses become a larger factor in signal degradation
- Return Loss (S11, S22)
  - Signal losses are also caused by mismatches in impedance. Impedance mismatches occur in packages, PCB traces, vias, connectors, and sockets



Example of Using S-parameter Plots for Channel Review

- IEEE's 10G Base-KR specification is one example of a SERDES protocol providing guidelines for the channel based on S-parameter data



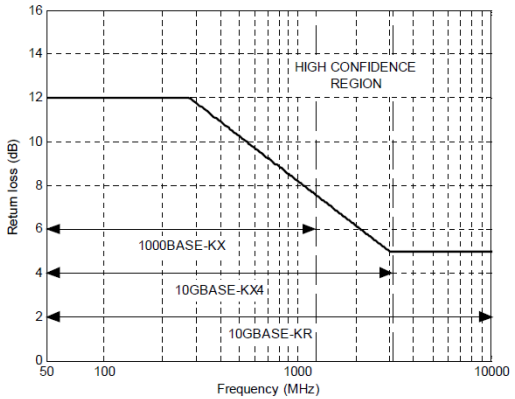


Figure 69B–7—Return loss limit

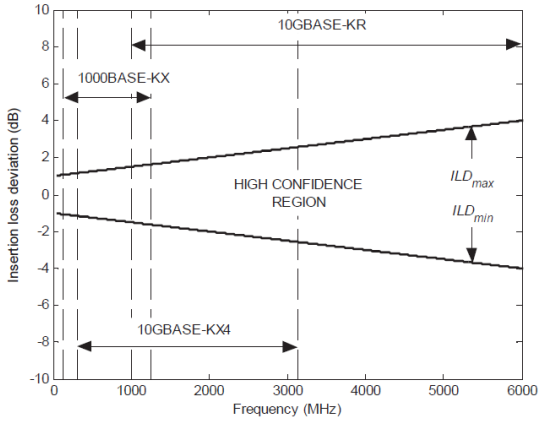


Figure 69B–6—Insertion loss deviation limits

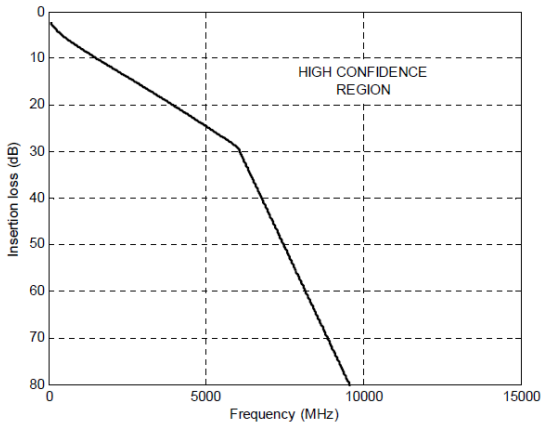
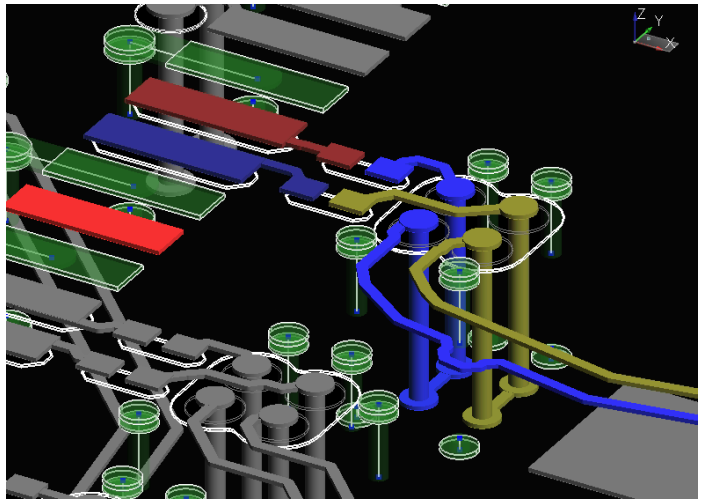


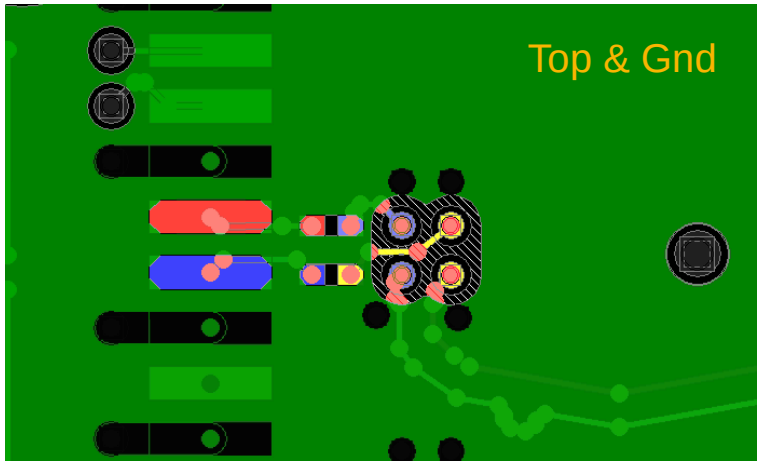
Figure 69B–5—Insertion loss limit for 10GBASE-KR

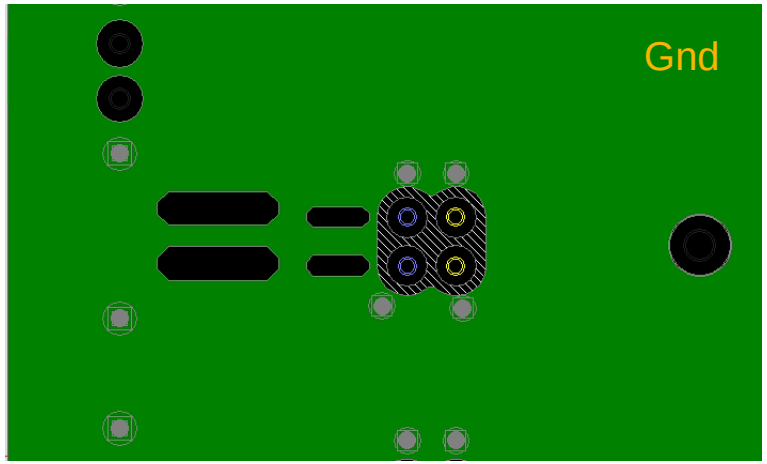
PCB LAYOUT – FINER DETAILS

Pads: Connector, AC Cap, Device

- Consider cutting out plane under pad
  - AC cap pads
  - Connector pads
  - BGA pads
  - Pads are cut out to ~match pad width
    - Reduces capacitance & reduces impedance discontinuity

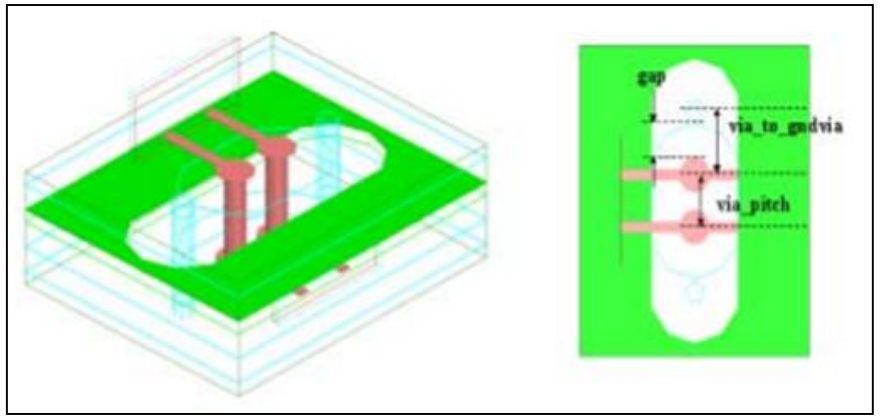


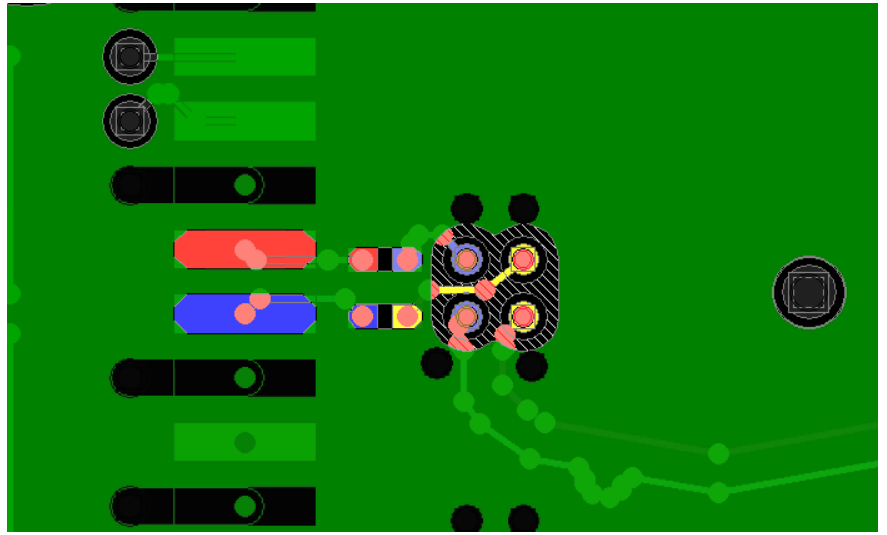




PCB Vias

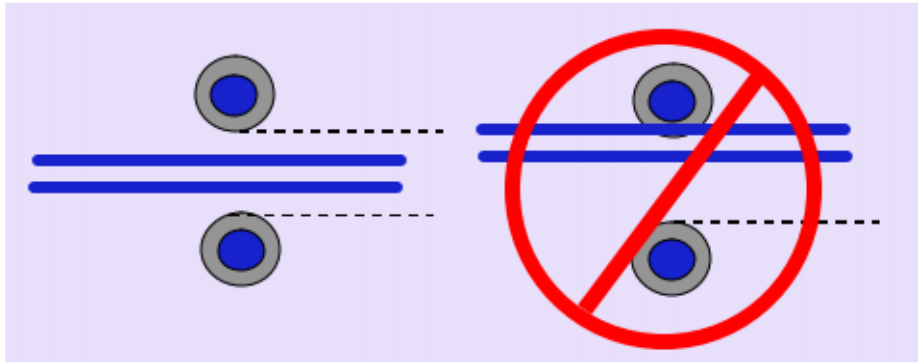
- PCB Vias (diff pair) often will be <100 ohms
  - ~100 mil PCB, 10 mil drill, ~40 mil pitch
- Consider creating larger antipad for planes in the stackup to reduce capacitance and raise impedance
- Diff pair Vias from board with antipad cutouts shown
- Work with PCB Fab House to use best drill size
  - Small drill usually raises via impedance
  - Small drill size may be more costly
- Remove unused pads on vias

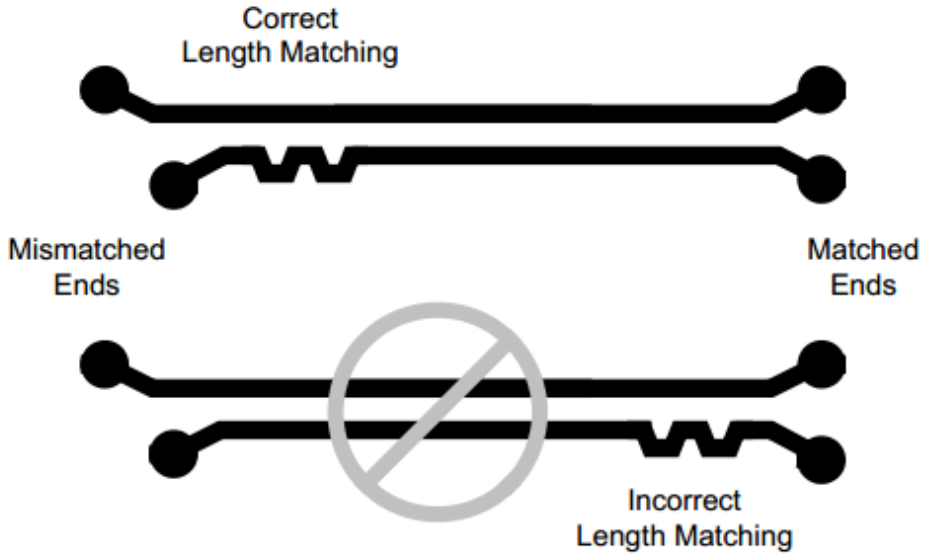


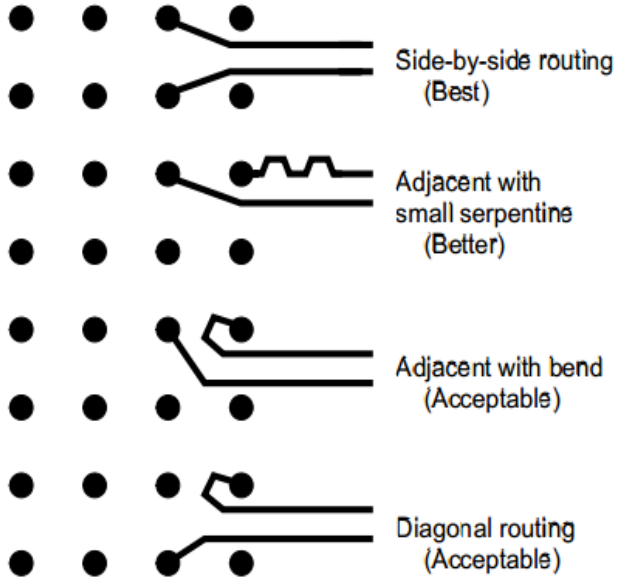


More Finer Details for PCB SERDES Routing

- Route over solid Ground plane
  - Be careful for pad cutouts, antipads
  - BGA Area may need special attention
- Try to match serpentine routing mismatch closer to source

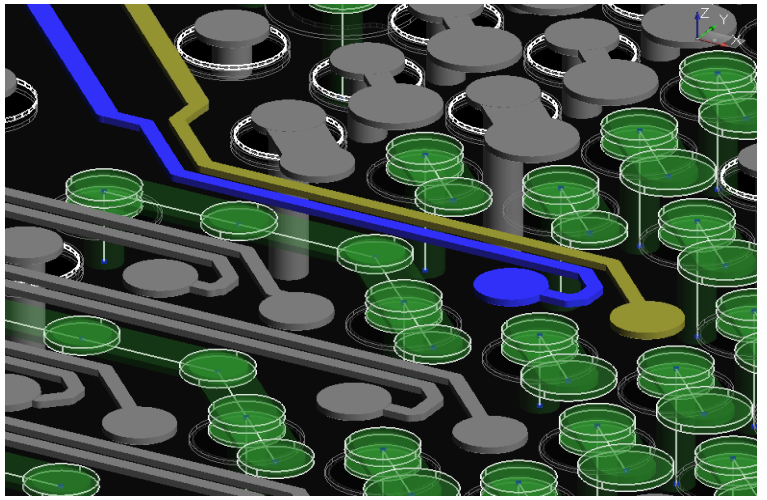


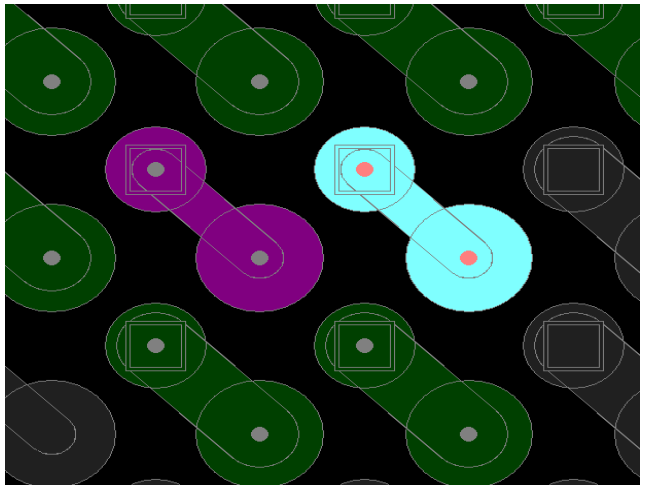


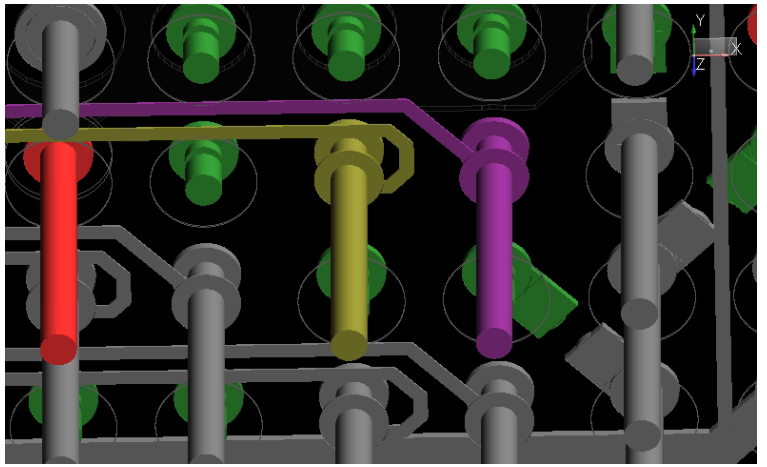


BGA Breakout

- Breakout on which layer?
  - Top Layer
  - Bottom Layer
  - Internal Layers
    - Via Stubs due to internal layer choice?
    - Stripline with short via stub
    - Stripline with micro via or back drilled via
  - Trace Width Management
    - Neckdowns? Dual Track Routing?
    - Dog Bones, Via in Pad?







BGA Breakout Options

- Dogbone Route to offset pads and provide more area and channels into BGA
- Examine how deep are SERDES diff pairs to break out
- Often can be 9 rows deep
  - Will be difficult to break out or route on top or bottom layers with pads intact
- Manage Neckdowns carefully
- Consider backdrilling of vias
  - Scheme shown below is from Altera AN

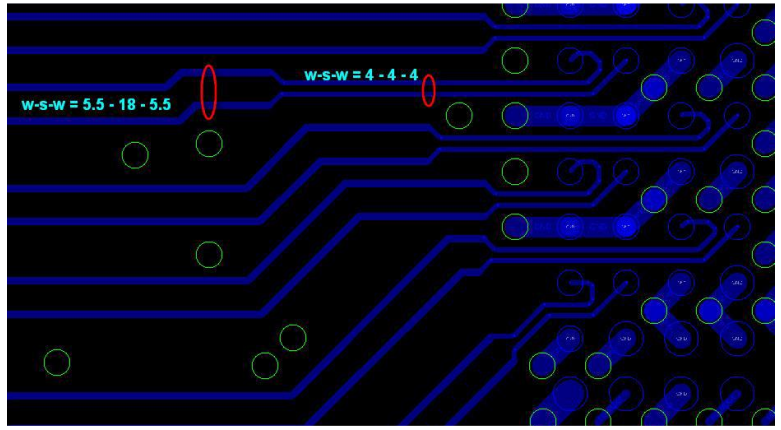


Figure 4. Optimum Layer Assignment for Effective Backdrill

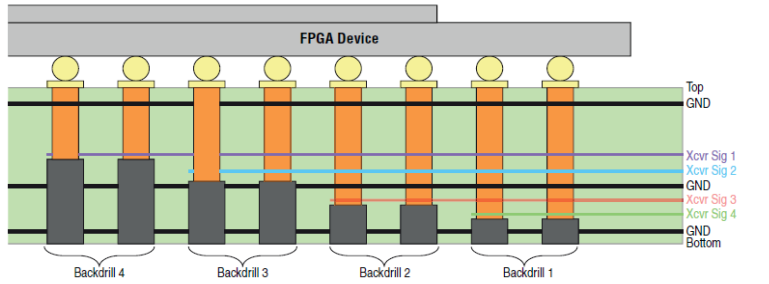


Figure 5. Poor Layer Assignment Limits Backdrill Effectiveness

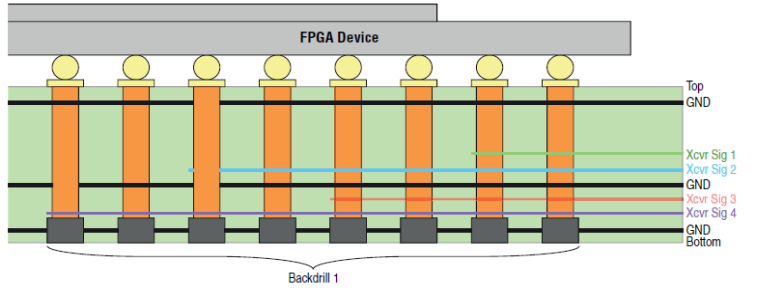
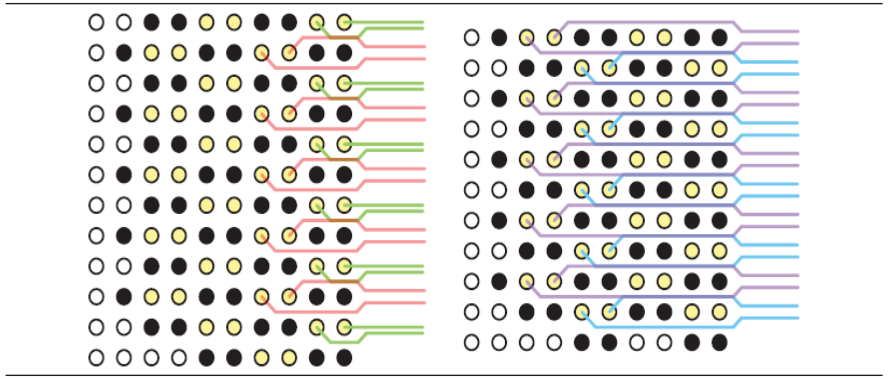
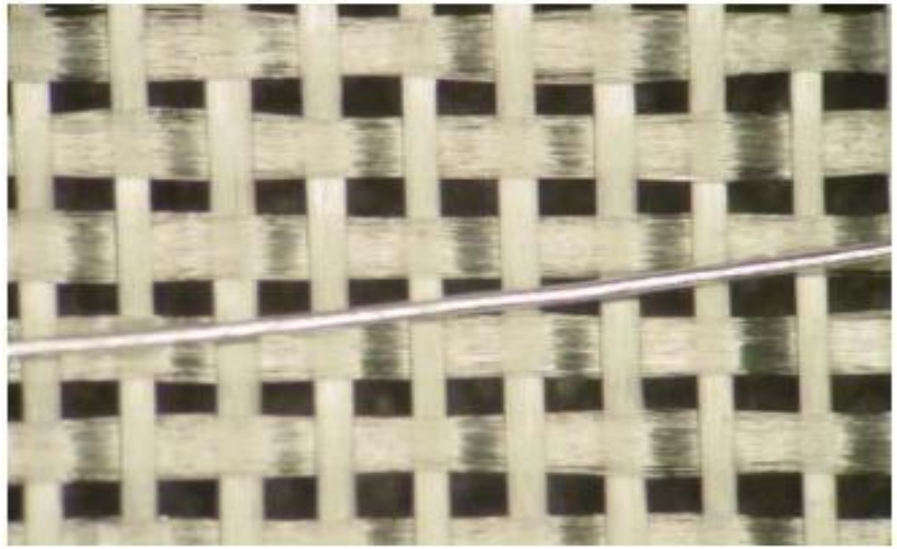


Figure 3. Single Trace Breakout Layer Usage



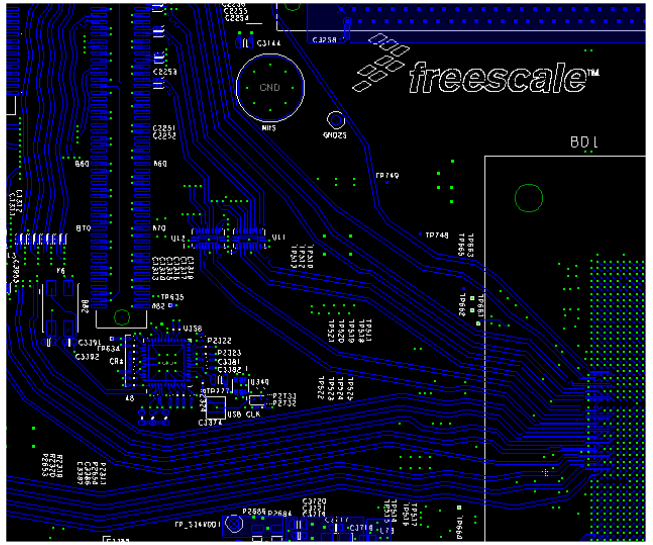
Fiber Weave Effects

- Be careful about routing high speed signals, like SERDES diff pairs, on 90 degree angles so that the traces line up with the fibers in the PCB materials
  - This could lead to one signal of the diff pair having a different effective dielectric constant than the other, which then will create skew between the two signals in the diff pair
- Consider using materials with a tighter, flatter weave so that effects are minimized.
- Route at offset, oblique angle to avoid the weave lining up with a signal in the diff pair.



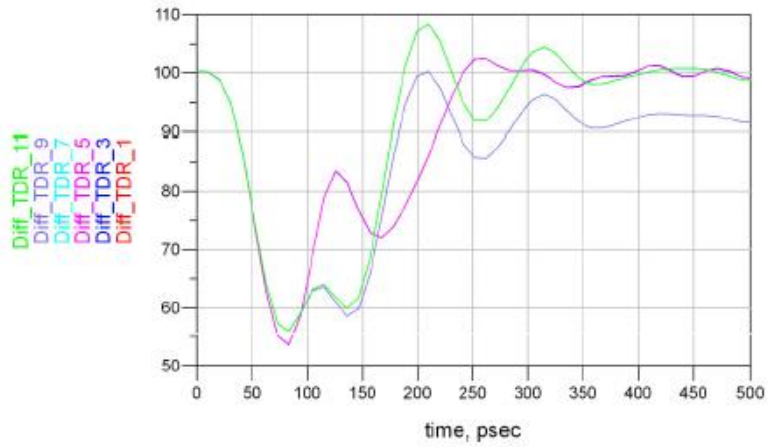
PCB Material Improvements

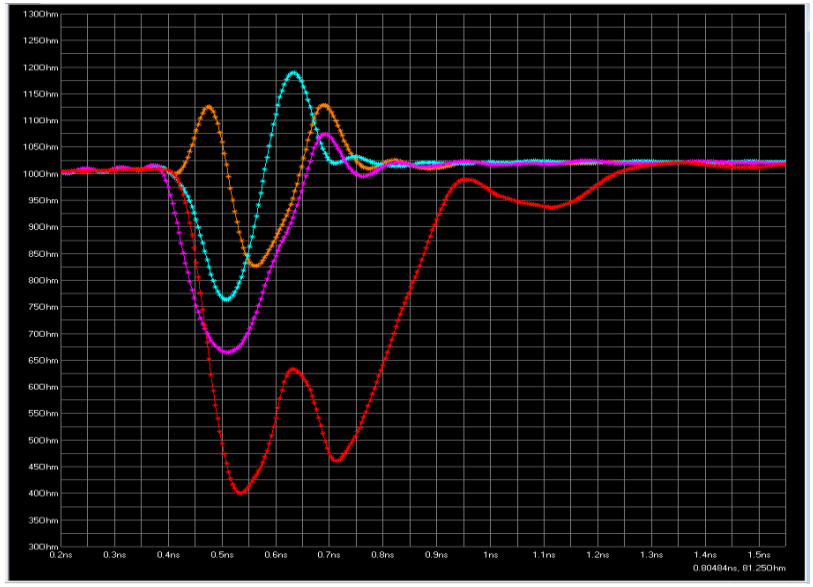
- **Oblique routing (avoids alignment with fiberglass weave)**
- **"this study shows worst-case skew variation of up to 60 ps for 4" of trace"** *("Impact of PCB Laminate Weave on the Electrical Performance of Differential Signalling at Multi-Gigabit Data Rates", DesignCon 2005)*



Connectors

- Connectors may not have as much impedance control as we would like for higher speeds
- Need to consider the PCB pad, pin, via design that is associated with the connector
- For fast edge rate TDR's, can see solder size effect in some cases
- Pay attention to TDR edge rate values in SERDES protocol specs





Checklist

Layout and Routing Guidelines based on 8Gbps rules

- AC coupling caps placed symmetrically? Near one end of the channel?
- AC coupling caps located near TX end when connector is implemented in system
- TX and RX data and REFCLKs routed as diff pairs
- Diff pairs routed symmetrically?
- No stubs anywhere in the diff pair routing
- No routing over plane splits or anti-pads
- Oblique routing used for diff pairs
- Diff pair (P-N) matching to within 10 mils for TX and RX data diff pairs
- Diff pair (P-N) matching to within 5 mil for REFCLK diff pairs
- Max length of all diff pairs on add-in card < 4 inches
- Diff pair length matching near the location of mismatch; within guidelines for sectional jogs?
- Lane-to-lane skew within tolerance
- Serpentine bends within guideline (no sharp angles)
- Breakout routing of diff pairs per guideline; avoid dog-bone in BGA area
- Neckdown of trace width / spacing in breakout areas per guideline; care with impedance matching
- Differential vias:
  - thru-hole vs. microvia choice; each meets aspect ratio requirements
  - Four or fewer vias in TX channel
  - Two or fewer vias in RX channel
  - Use smallest via possible; pads removed from via on internal layers
  - Increase via pair anti-pad to match impedance
  - Add GND stitching vias near diff pair vias
  - Back-drill thru-hole differential vias to remove stubs
- Cutout GND underneath pads of components in differential pairs
- Remove all reference planes underneath edge fingers of add-in cards
- Add-in card comply with mechanical form factor dimensions

PCB CHARACTERISTICS – QUICK OVERVIEW

Summary Data on PCB Trace Width and Materials

- Trace Width affects the loss of the SERDES channel
  - Narrower traces produce more loss due to skin effect (Increases at Square Root of Frequency)

    - Trace width: Use wider traces (may be limited due to board thickness requirements)
    - (+) Improves skin-effect loss
    - (+) No increase in material cost
    - (-) Uses more routing area
    - (-) Increases PCB thickness to maintain impedance targets

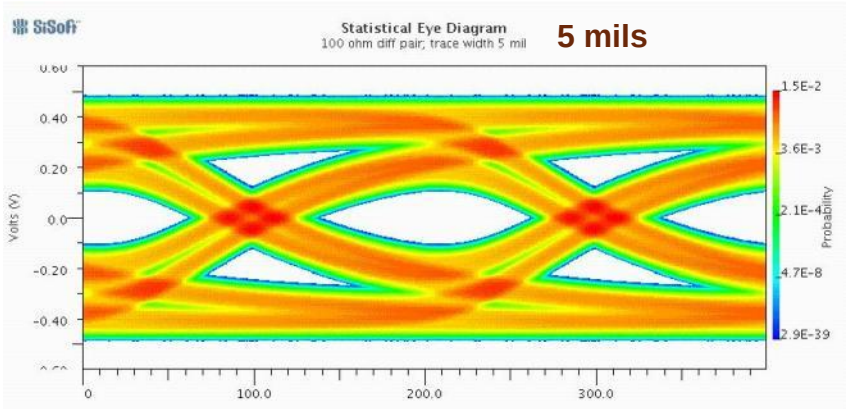
- Higher loss tangent values → greater loss in the SERDES Channel (Increases Proportionally to Frequency)

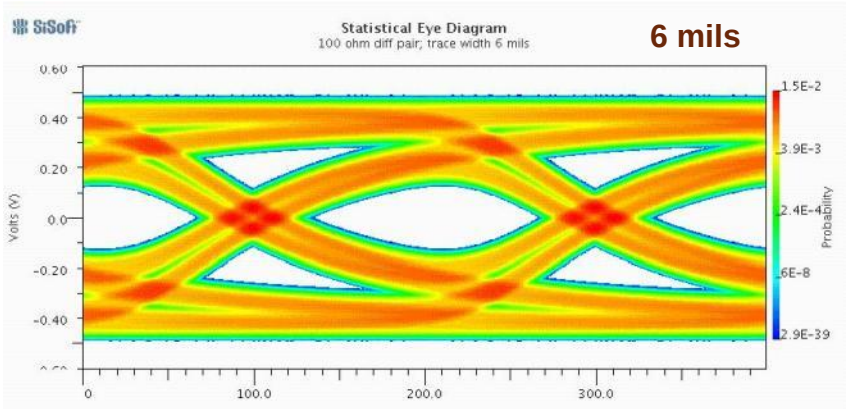
- PCB materials: Use “high-speed” FR4
  - (+) Lower loss tangent ➔ lowers dielectric loss (Loss tangent can be cut in half with modified FR4 materials)

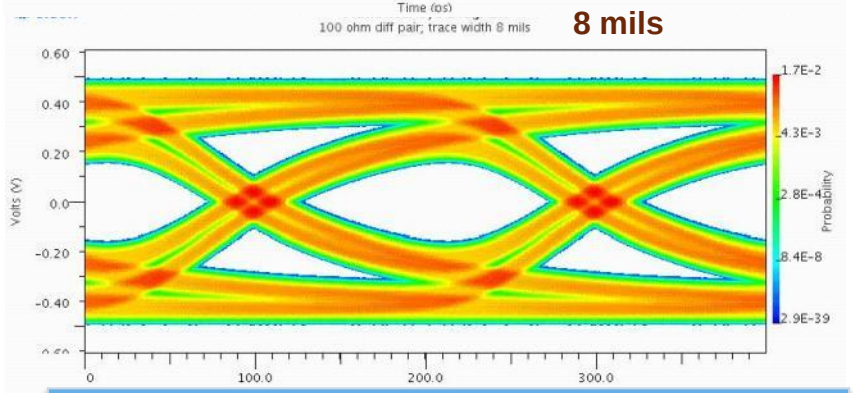
- Use “smooth” copper
  - (+) Lower conductor loss
  - (-) Caution! Peel strength is reduced

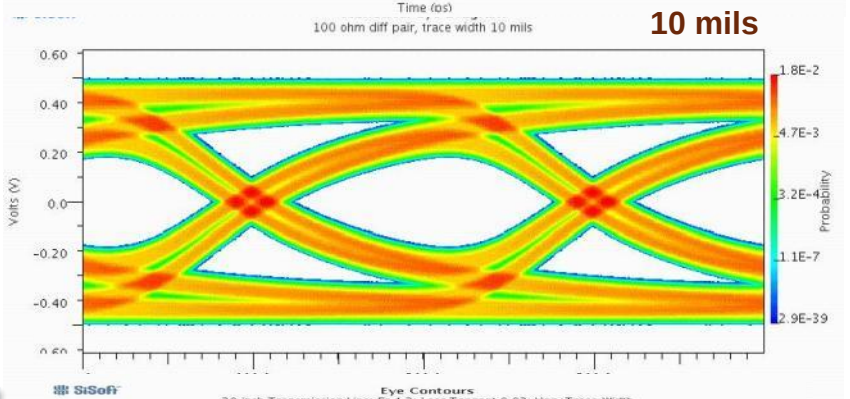
- *** → May benefit from use of TX and RX EQ to offset trace losses

PCB Trace Width Results No EQ: Compare

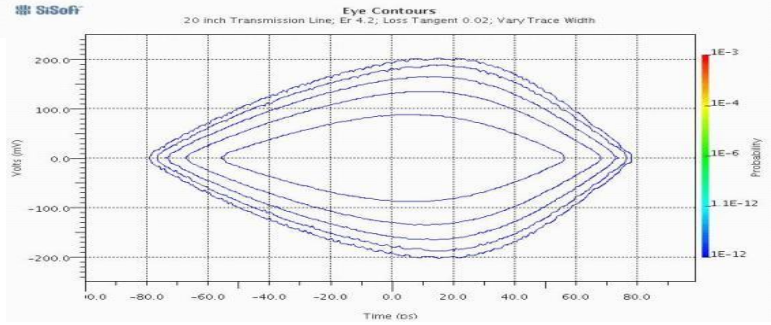




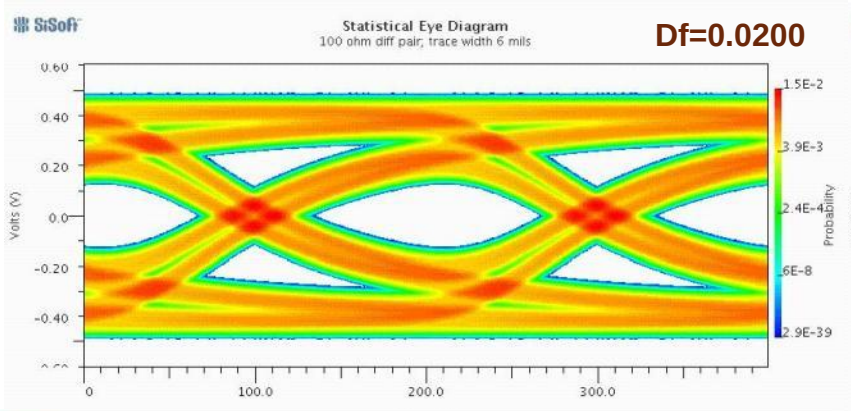


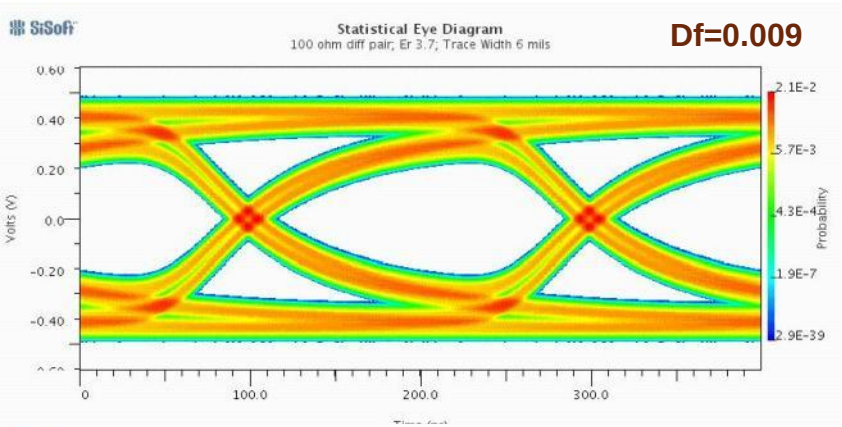


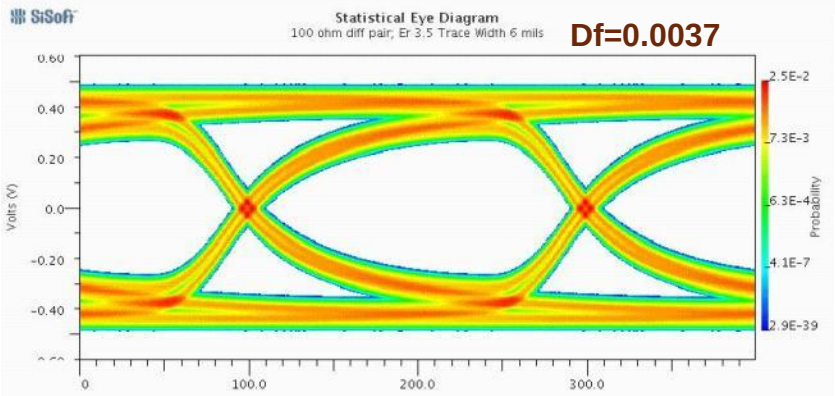
Trace Width (mils)	Eye Ht (mV)	Eye Width (ps)
4	173.7	113.3
6	261.6	136.7
8	317.9	148.4
10	360.8	154.7
12	380.9	158.6

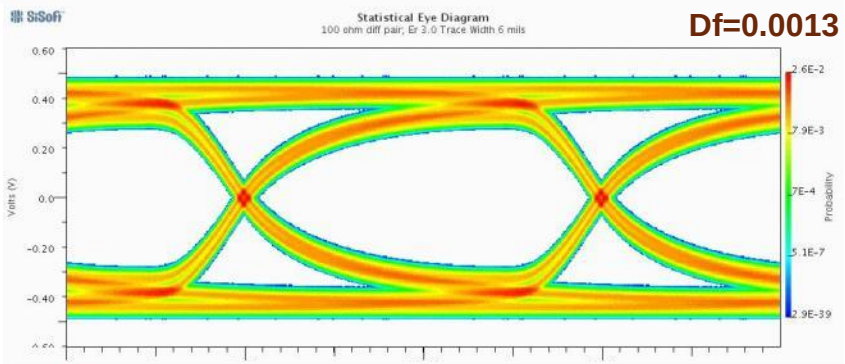


PCB Materials Results: Compare

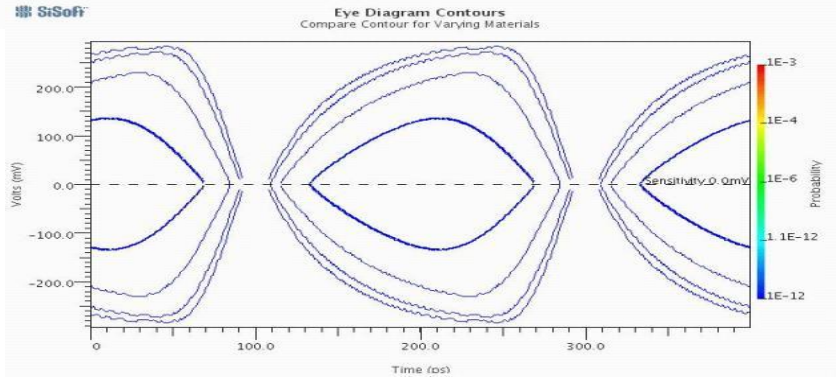








Material	Eye Ht (mV)	Eye Width (ps)
Er 4.2, 0.0200	261.6	136.7
Er 3.7, 0.0090	414.7	170.3
Er 3.5, 0.0037	506.0	182.8
Er 3.0, 0.0013	536.9	185.9



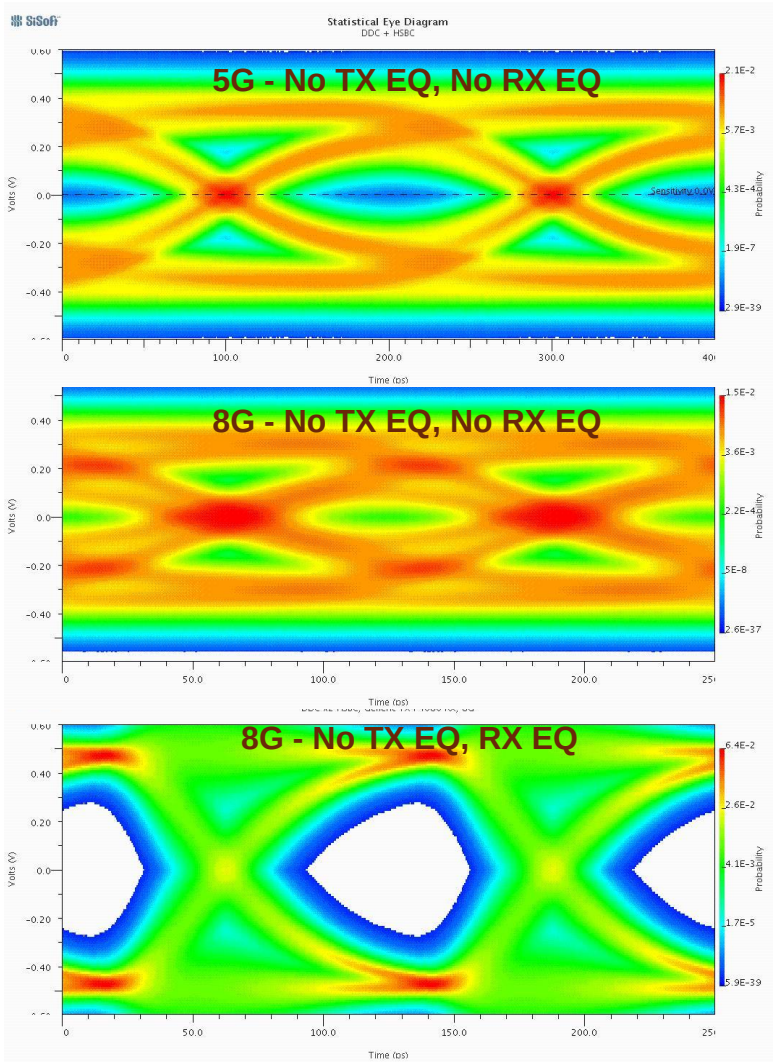
IBIS-AMI SIMULATION EXAMPLES

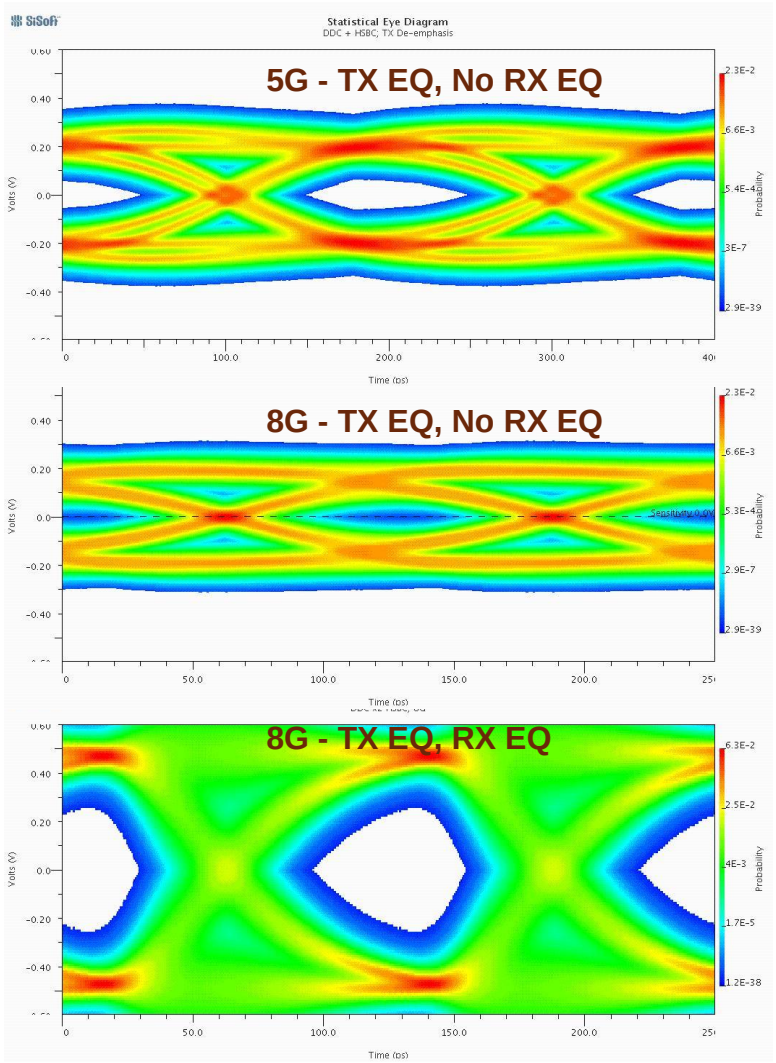
Show TX EQ and RX EQ in AMI simulations
Sweep TX EQ to work best with RX EQ

Channel Simulations with AMI Models

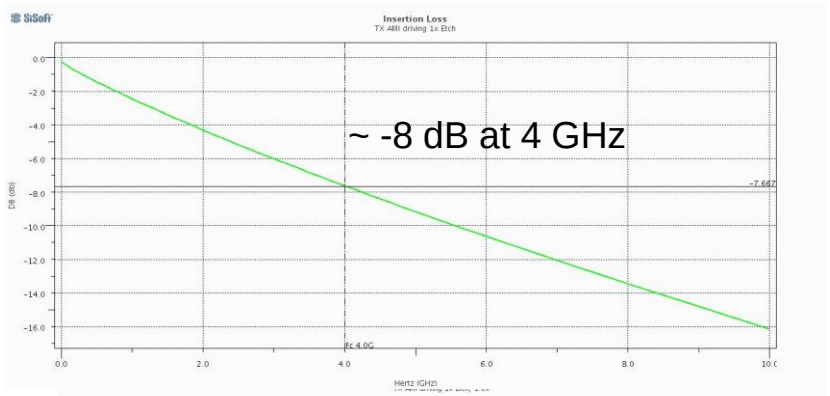
- Show TX EQ helps but does not open eye
  - RX EQ opens eye
- Show how TX EQ and RX EQ work together
  - RX EQ may work better with TX EQ set differently (than if TX EQ alone was present)
    - Less TX EQ de-emphasis helps RX EQ
- Longer channel, more insertion loss shows more of a challenge
  - TX EQ does not open eye
  - RX EQ needed to open eye
    - More TX EQ de-emphasis helps RX EQ
- Best EQ settings change with Frequency in some cases

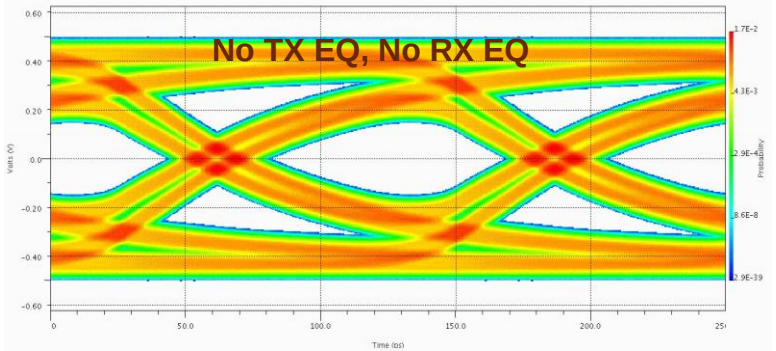
Compare TX and RX EQ Options @ 5G, 8G: TX EQ + RX EQ

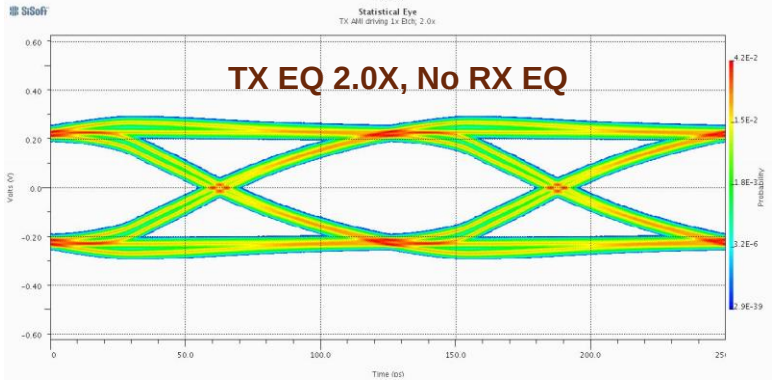


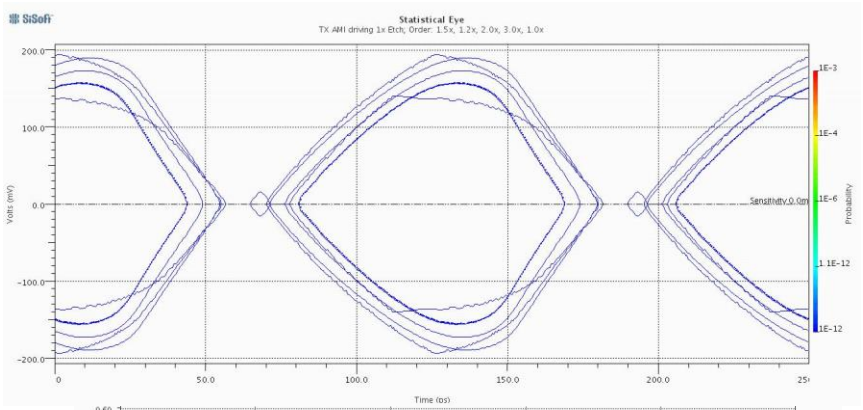


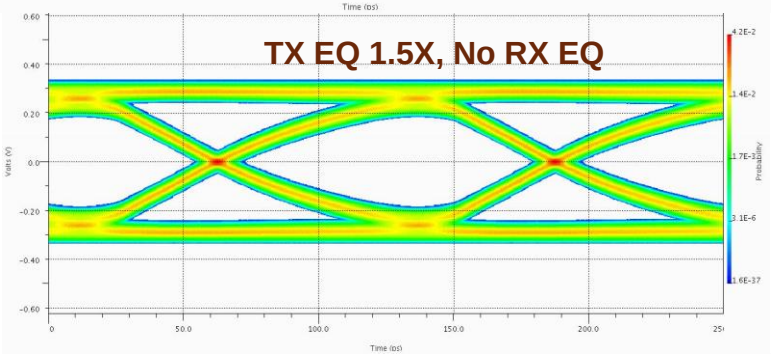
Compare TX EQ at 8G: Eye Density (TX EQ alone still works)

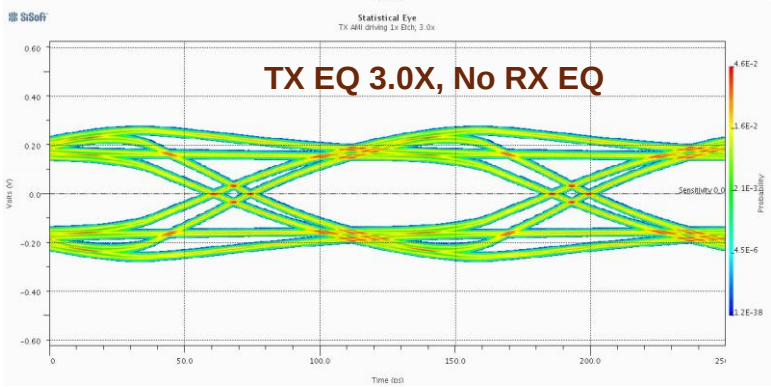




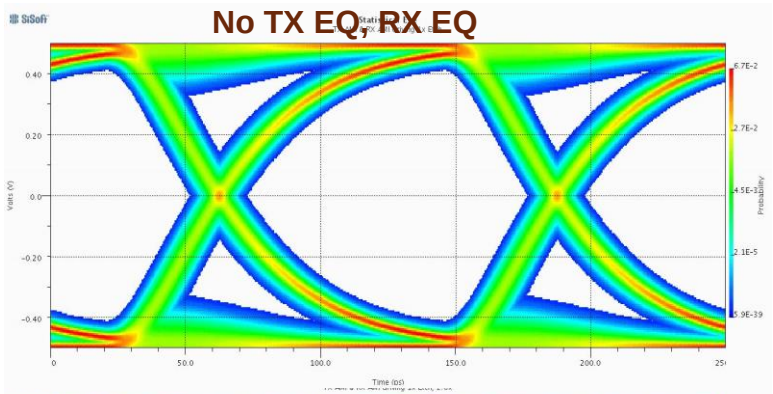


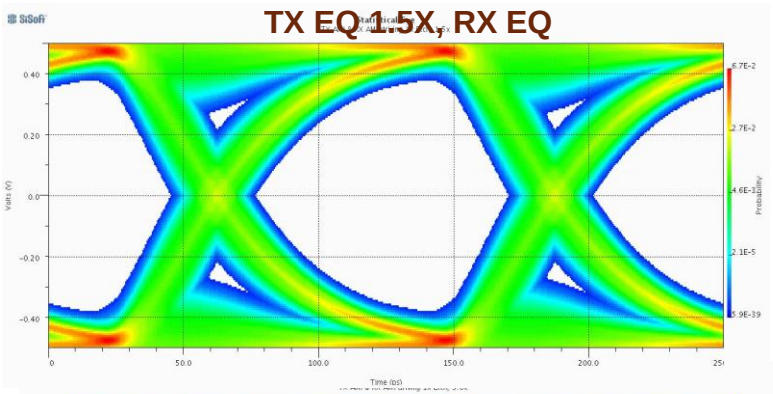


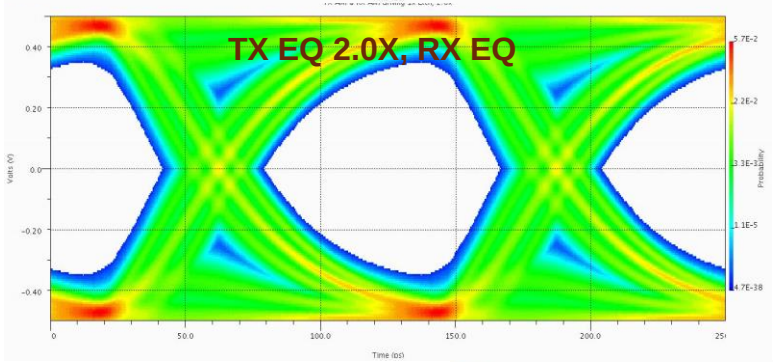


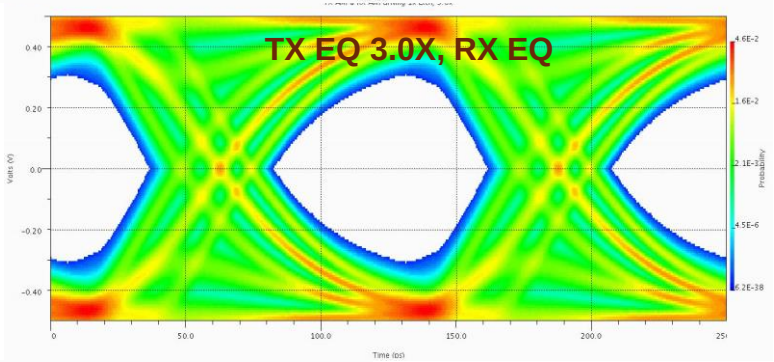


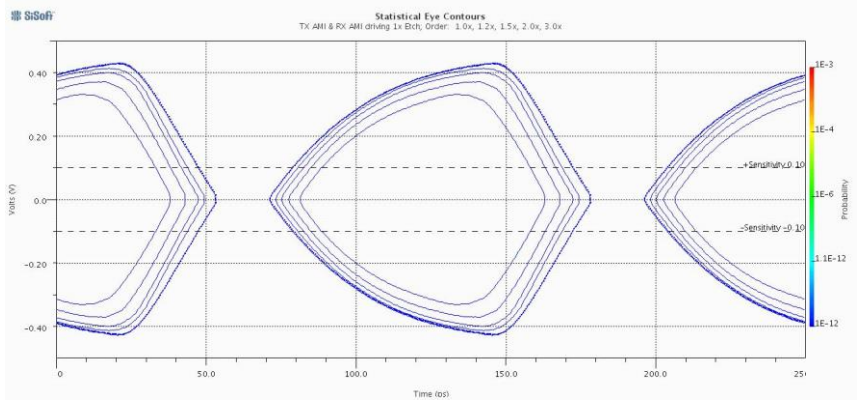
Compare TX EQ + RX EQ at 8G: Eye Density (Less TX EQ is best)



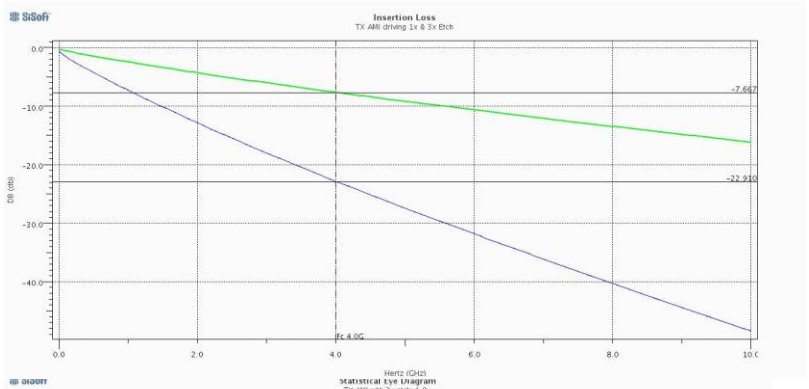




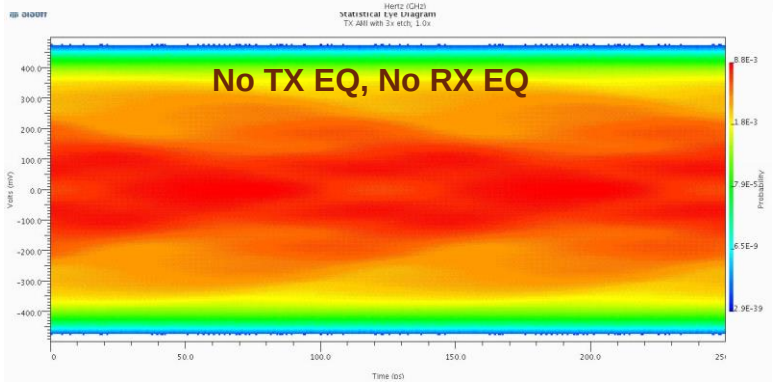


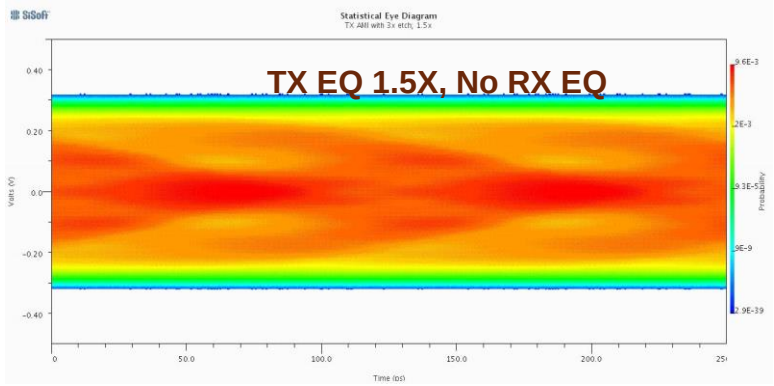


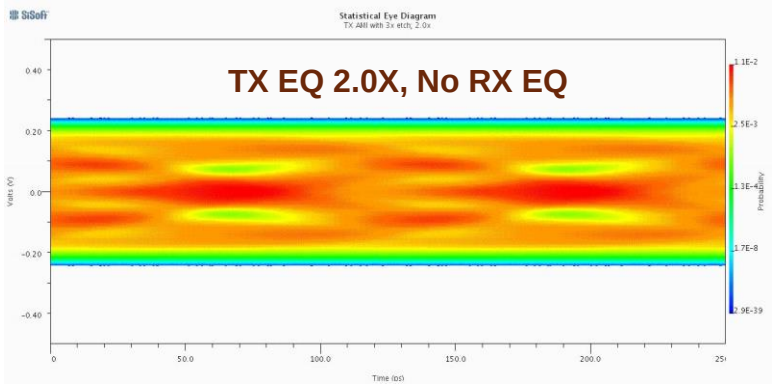
3x Loss from Prior Channel: Compare TX EQ at 8G: Eye Density

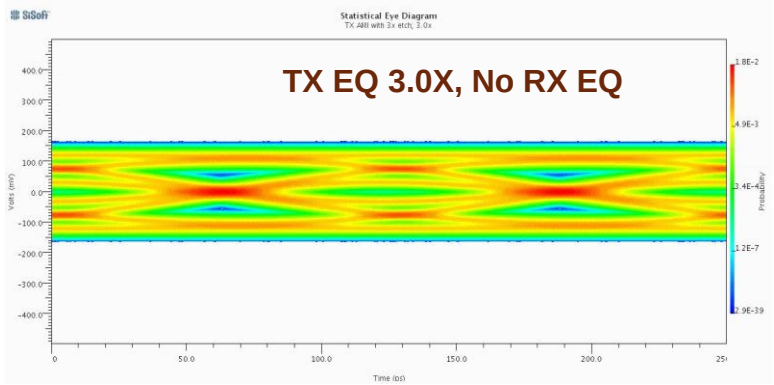


(Compared to Prior Channel Insertion Loss ~3x More Loss)

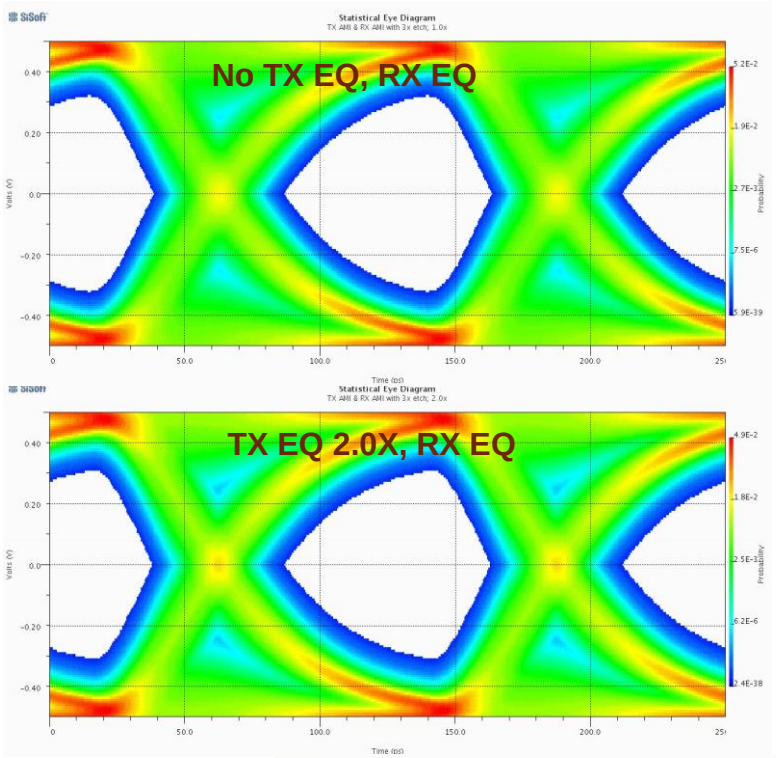


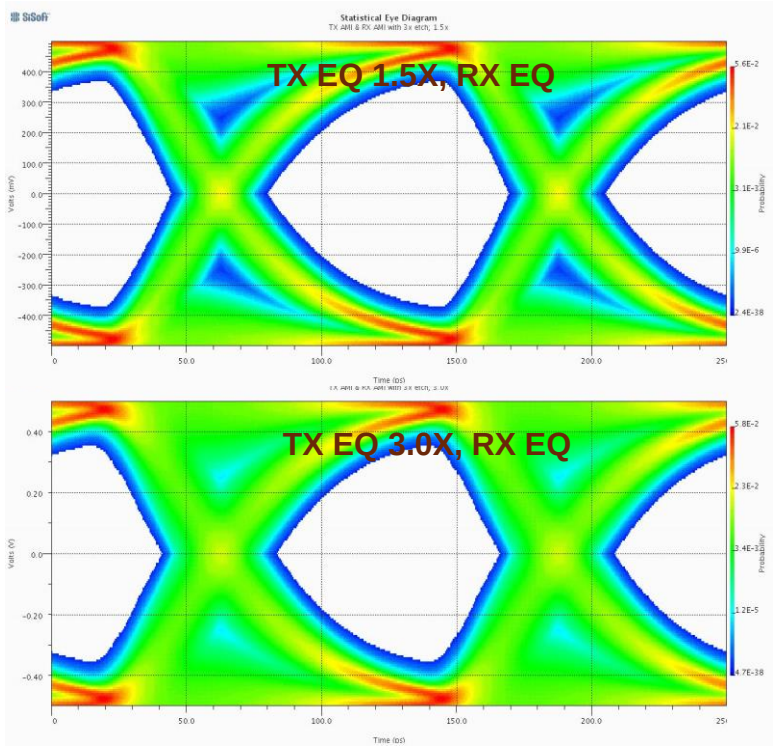


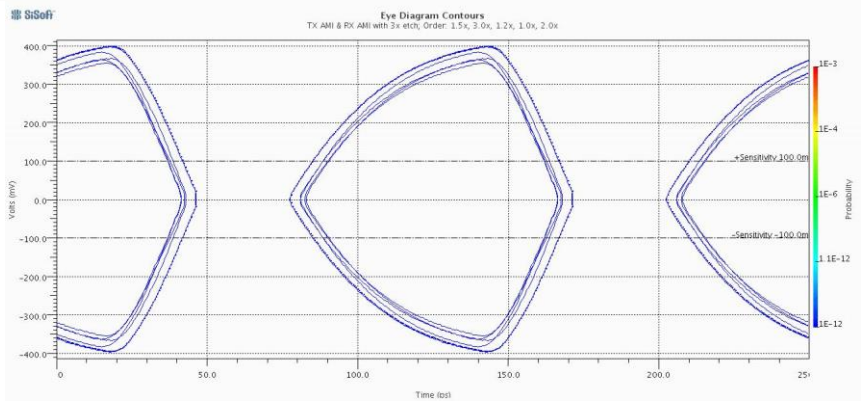




3x Loss from Prior Channel: Compare TX EQ + RX EQ at 8G: Eye Density







Summary of Eye Height and Eye Width from TX EQ Sweep: Left is 1X Etch Length; Right is 3X Etch Length

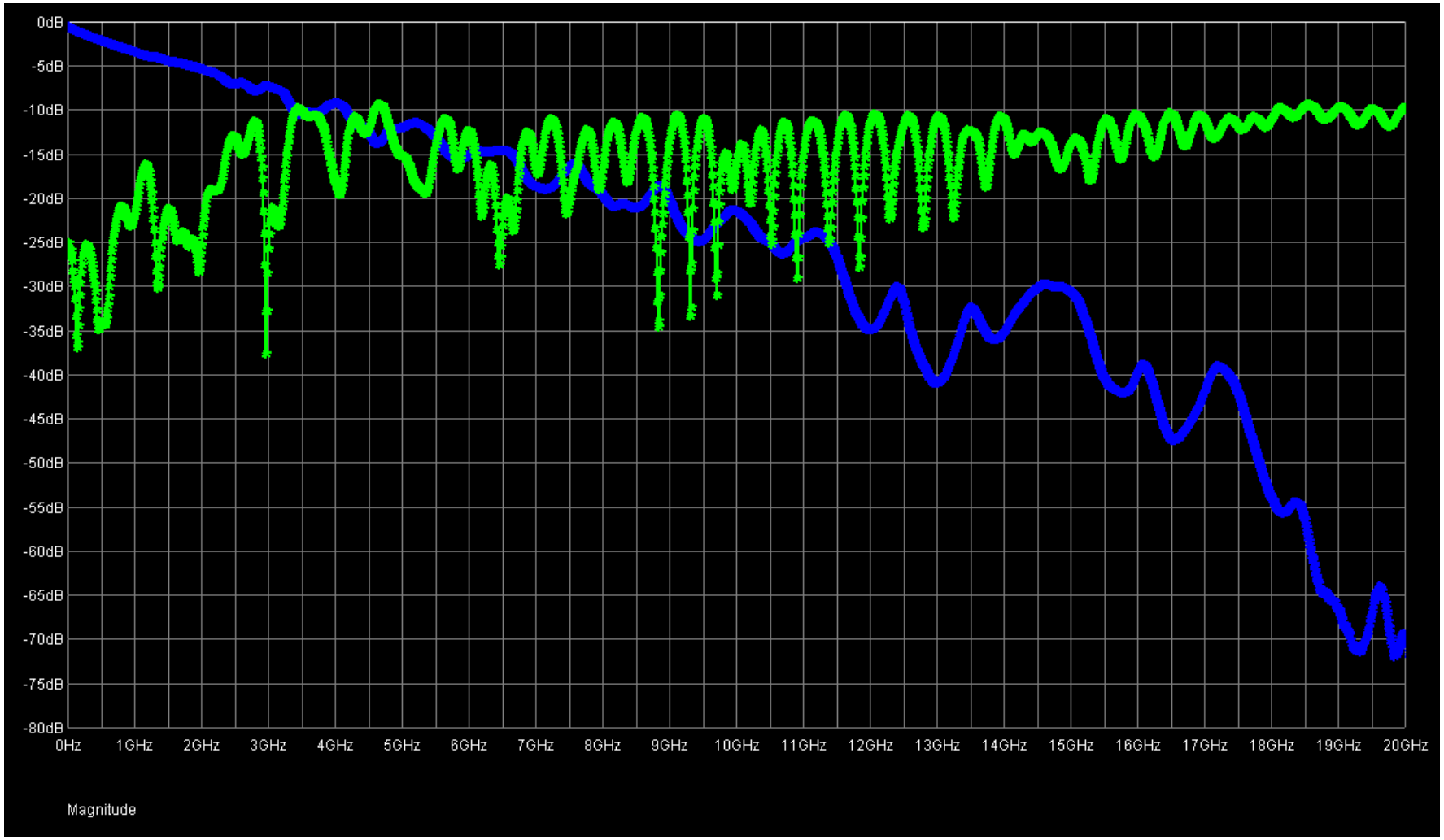
Left is 1X Etch Length

TX EQ	RX AMI	Eye Height (V)	Eye Width (ps)
0	No	0.300	88.9
1.2x	No	0.330	98.6
1.5x	No	0.360	109.4
2.0x	***No***	***0.385***	***110.8***
3.0x	No	0.273	104.5
0	***Yes***	***0.782***	***107.9***
1.2x	Yes	0.767	102.1
1.5x	Yes	0.742	98.1
2.0x	Yes	0.694	91.3
3.0x	Yes	0.628	82.5

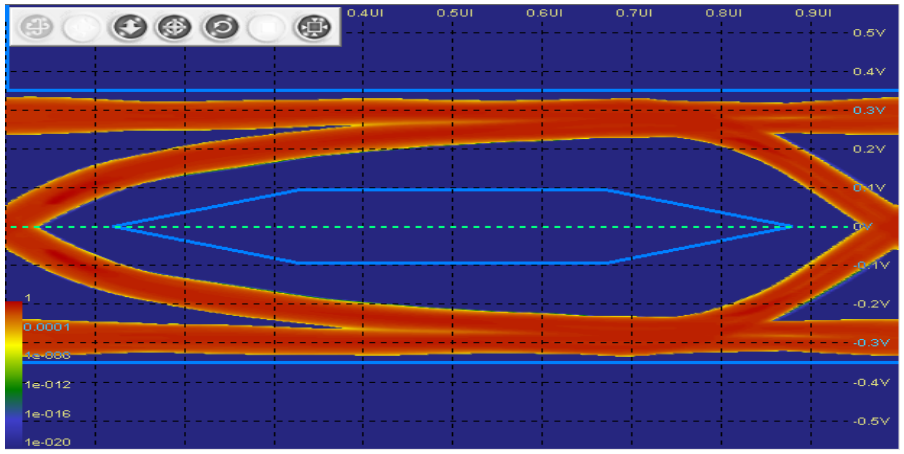
Right is 3X Etch Length

TX EQ	RX AMI	Eye Height (V)	Eye Width (ps)
0	No	0	0
1.2x	No	0	0
1.5x	No	0	0
2.0x	No	0	0
3.0x	No	0	0
0	Yes	0.658	84.5
1.2x	Yes	0.661	87.9
1.5x	***Yes***	***0.721***	***94.7***
2.0x	Yes	0.640	84.9
3.0x	Yes	0.699	87.4

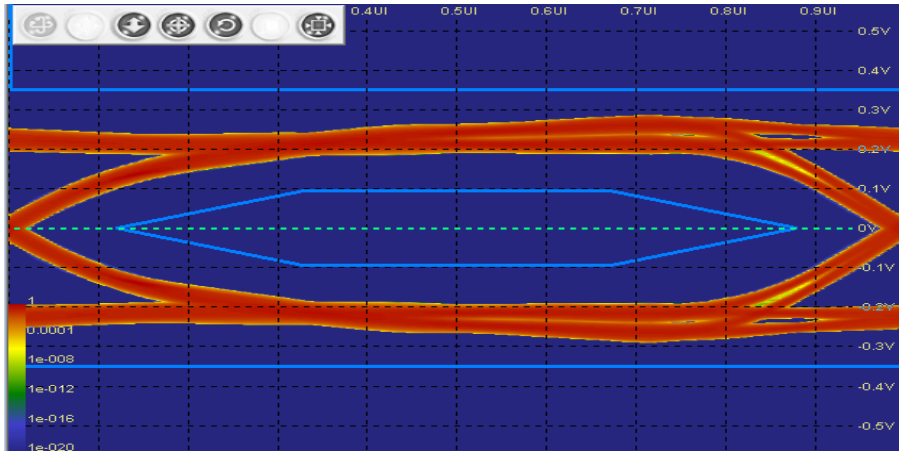
Channel Insertion Loss, Return Loss (add SDD21 values)



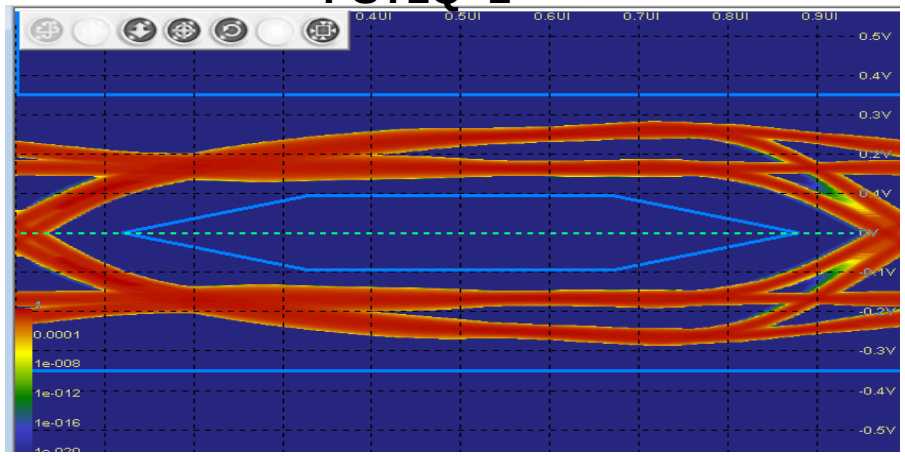
TX EQ: 2.5 Gbps; Vary PST1Q: 1, 8, 12, 16
Minimal TX EQ Good



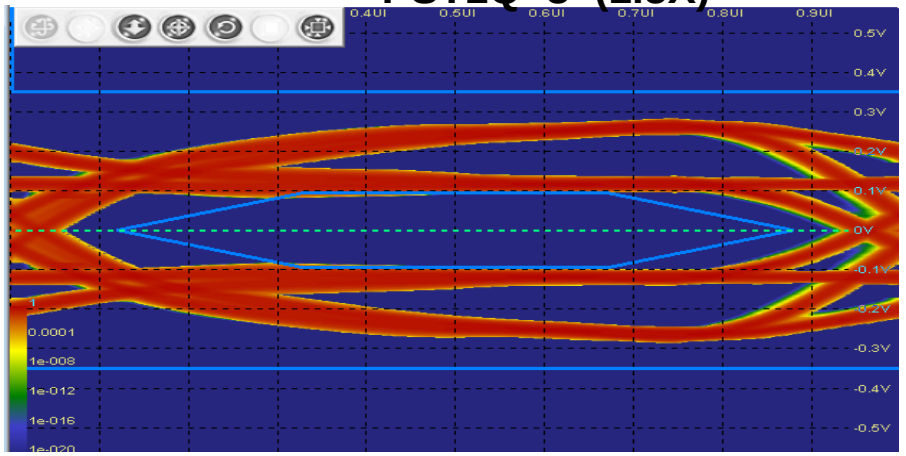
PST1Q=1



PST1Q=8 (1.5X)

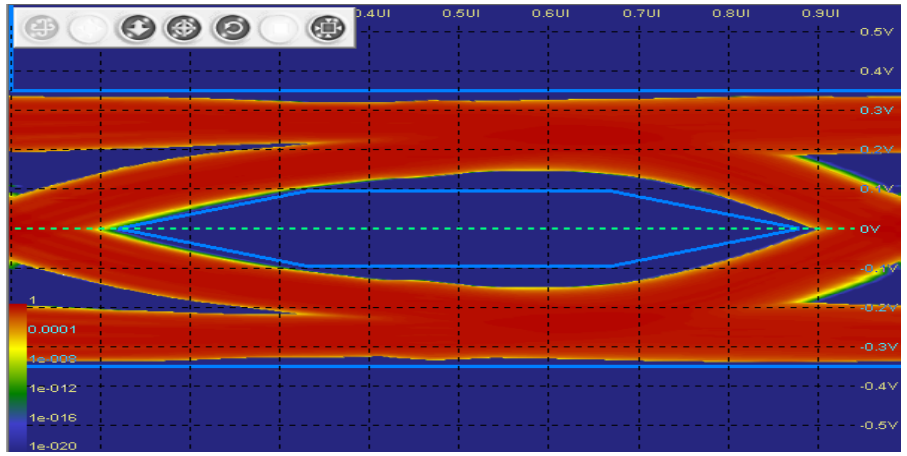


PST1Q=12 (2.0X)

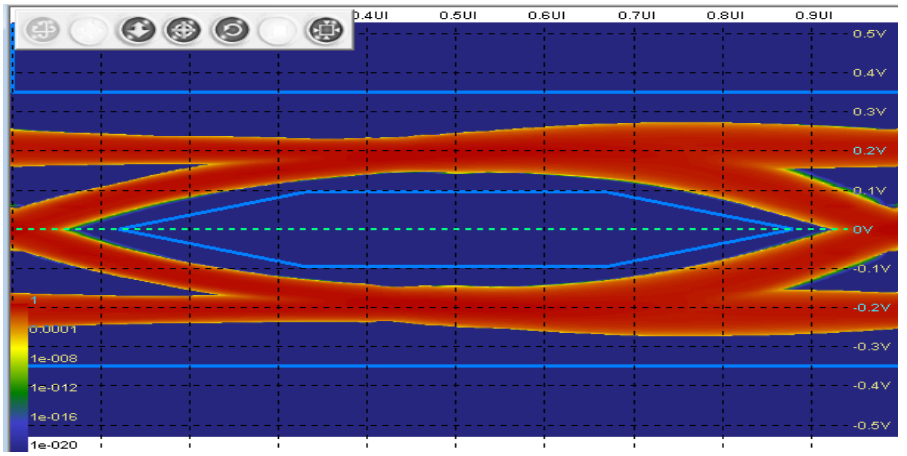


PST1Q=16 (3.0X)

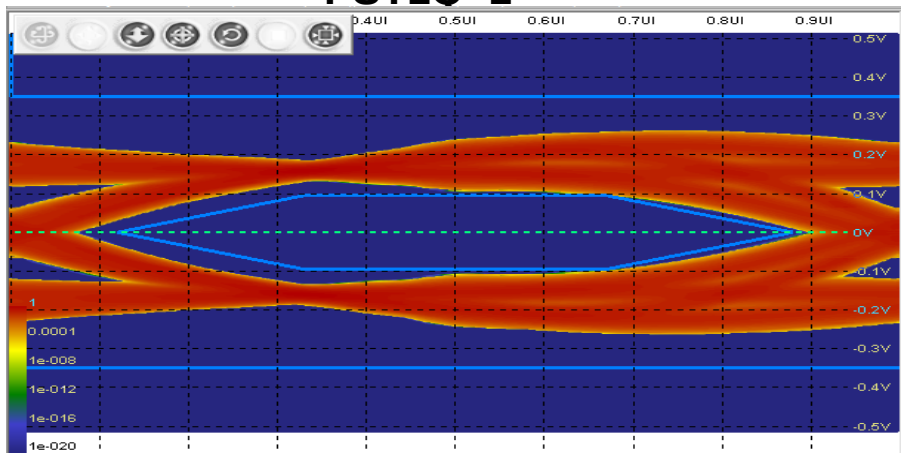
TX EQ: 5.0 Gbps; Vary PST1Q: 1, 8, 12, 16
Minimal to Moderate TX EQ Good



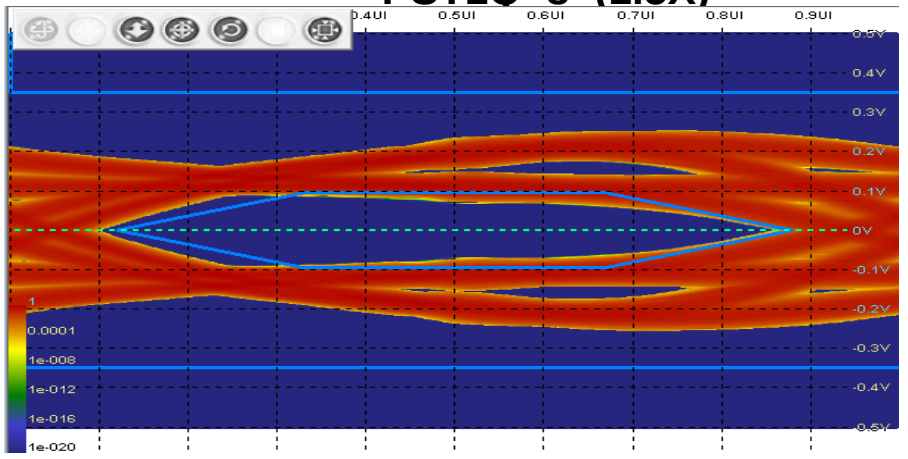
PST1Q=1



PST1Q=8 (1.5X)

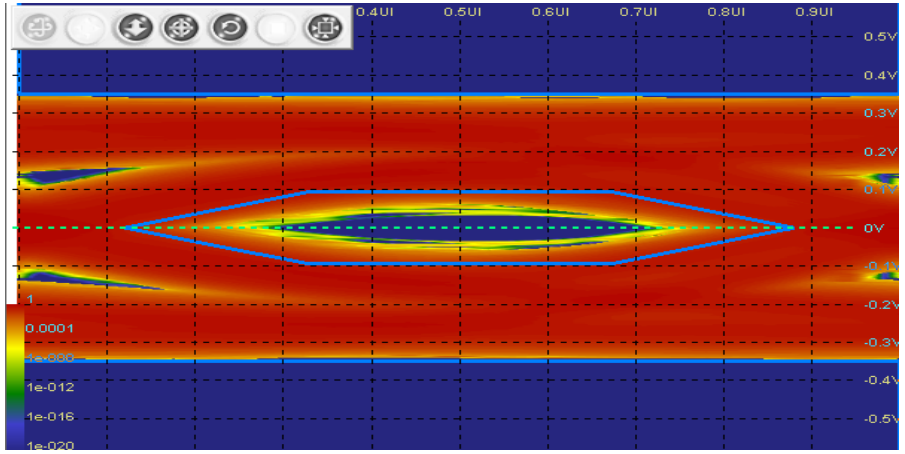


PST1Q=12 (2.0X)

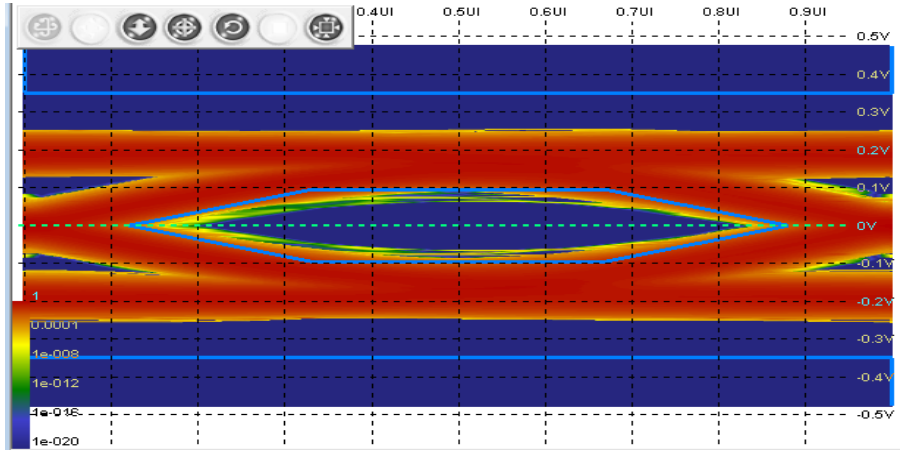


PST1Q=16 (3.0X)

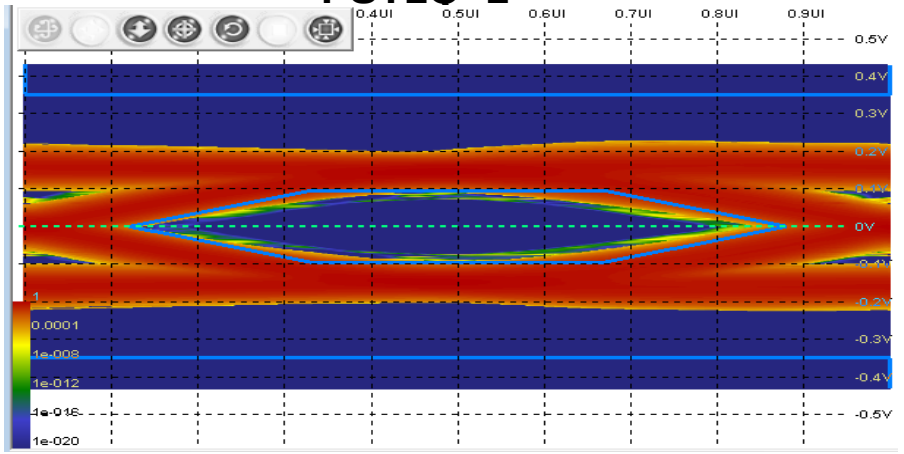
TX EQ: 8.0 Gbps; Vary PST1Q: 1, 8, 12, 16
Best TX EQ Not Same for All Speeds; Stronger TX EQ Helps



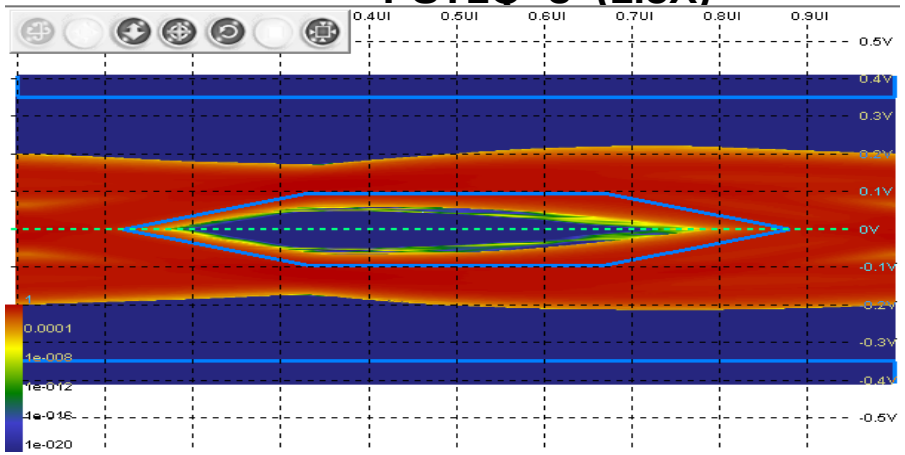
PST1Q=1



PST1Q=8 (1.5X)

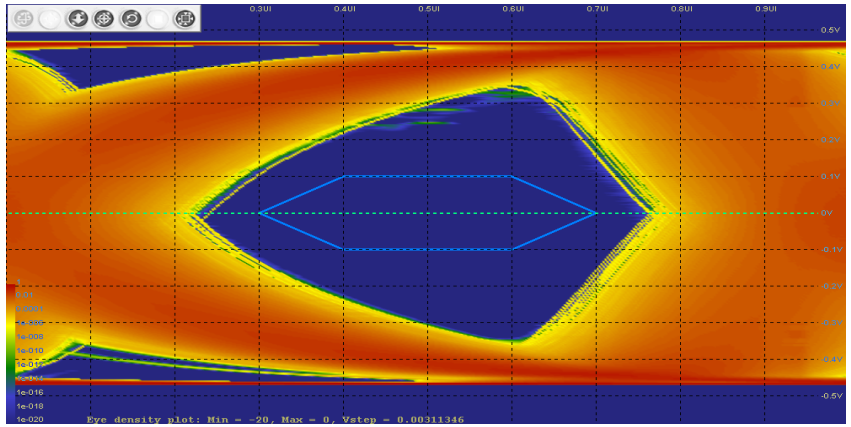


PST1Q=12 (2.0X)

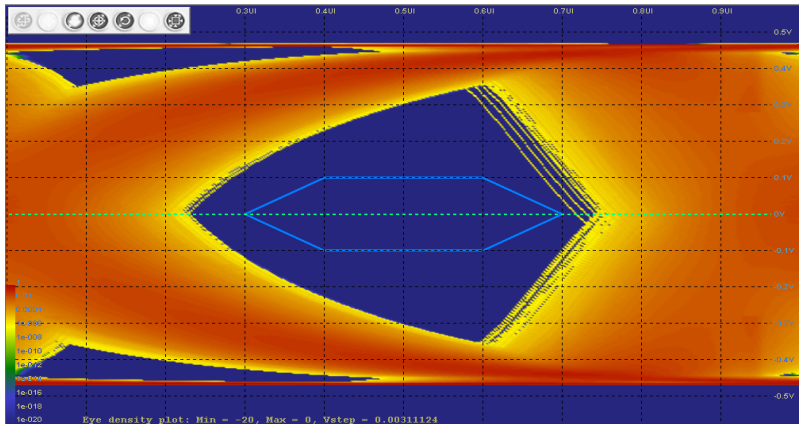


PST1Q=16 (3.0X)

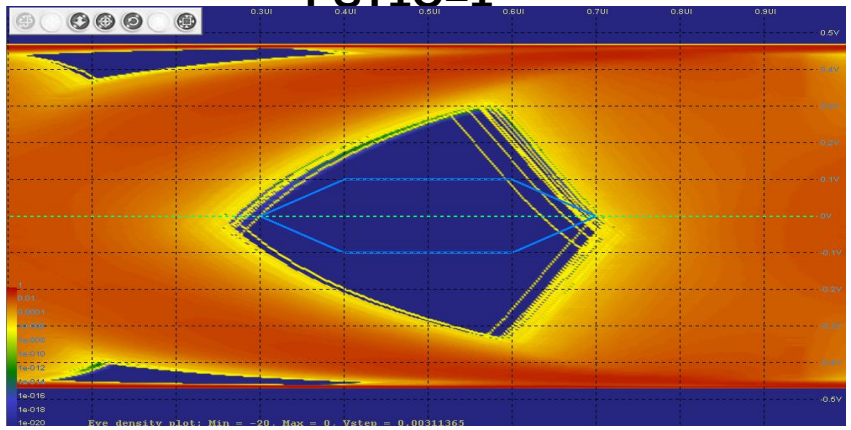
TX EQ + RX EQ: 8 Gbps; Vary PST1Q: 1, 8, 12, 16
Best TX EQ without RX EQ May Not Be Best for with RX EQ (RX EQ Dependent)



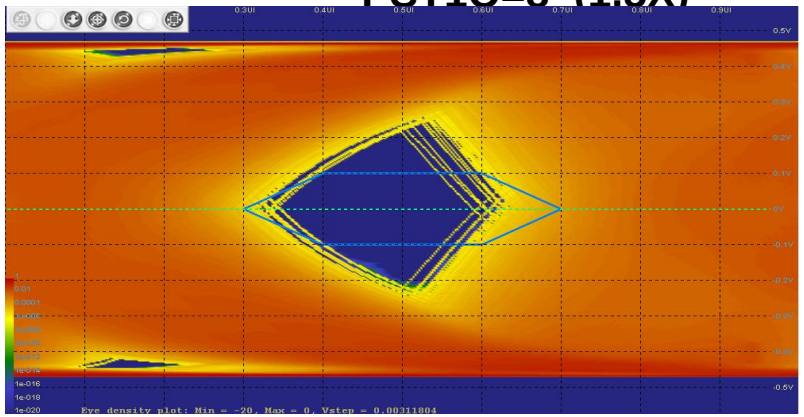
PST1Q=1



PST1Q=8 (1.5X)



PST1Q=12 (2.0X)



PST1Q=16 (3.0X)

Summary of IBIS-AMI Benefits and PCB Design Challenges

- AMI good for modeling TX and RX Equalization
  - TX EQ: 2 tap, 3 tap, 4 tap TX EQ
  - RX EQ:
    - Proprietary Circuits can be modeled: AMI Model can be tailored specifically for a device's design
    - Adaptive EQ is good feature

- TX EQ and RX EQ can be significant tools for improving SerDes channel response
  - May permit design using lower cost materials and narrower traces
    - Translates to << $$ and << board space

- Now have QCVS tool for SERDES Validation
  - Generate TX Patterns; Look at Jitter Scope On Die Eye

- PCB design at > 5 Gbps
  - Need to pay attention to the fine details
  - Be careful about assuming a prior working 5 Gbps design will work at 8-10 Gbps
  - Simulate and analyze in advance before laying out the PCB
  - Validate with QCVS after the board is built

Application Notes Related to SERDES TX and RX

- AN5119, SerDes Configuration and Validation Tool Companion
- AN4311, SerDes Reference Clock Interfacing and HSSI Measurements Recommendations.
- AN4996, PCI Express® Endpoint Design Guide (NDA required)
- AN4990, Enabling CPRI on BSC9132QDS

QUESTIONS AND ANSWERS

Thanks!

References

- *Ambiguous Influences Affecting Insertion Loss of Microwave Printed Circuit Boards*, Rogers Corp.
- NXP App Note, AN4996, *PCI Express® Endpoint Design Guide. (NDA)*
- NXP AN5119, *SerDes Configuration and Validation Tool Companion*.
- Altera Application Note AN-651-1.0: *PCB Breakout Routing for High-Density Serial Channel Designs Beyond 10 Gbps.*
- Agilent Signal Integrity Analysis Series Application Notes, 2007.
- *Finding Elusive Problems In High Speed Serial Data Links*, Howard Williams, LeCroy, 2013.
- *PCIe® 2.0 Signal Integrity Considerations (Fiberweave Effect),* Jeff Loyer, 2007.
- *Board Design Guidelines for PCI Express Architecture*, Zale Schoenborn, PCI Express Electrical WG, 2004.

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