FTF 2016
TECHNOLOGY FORUM

NXP LPC MICROCONTROLLERS

MAXIMIZING ENERGY EFFICIENCY IN ALWAYS-ON APPLICATIONS

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TECHNOLOGY AND BUSINESS DEVELOPMENT
FTF-DES-N1967
MAY 17, 2016

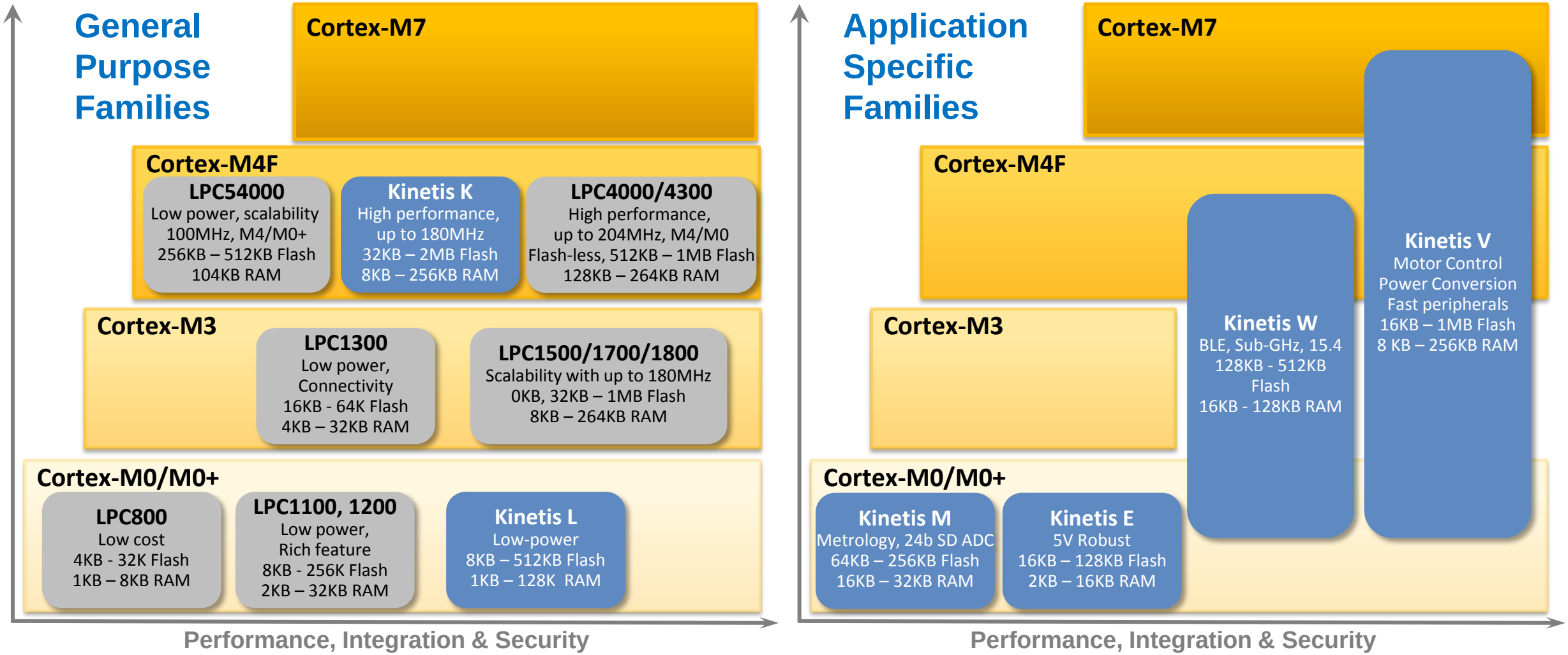
AGENDA

- LPC Microcontroller Portfolio Overview
- Leveraging Low Power Design Techniques
- What is next ?

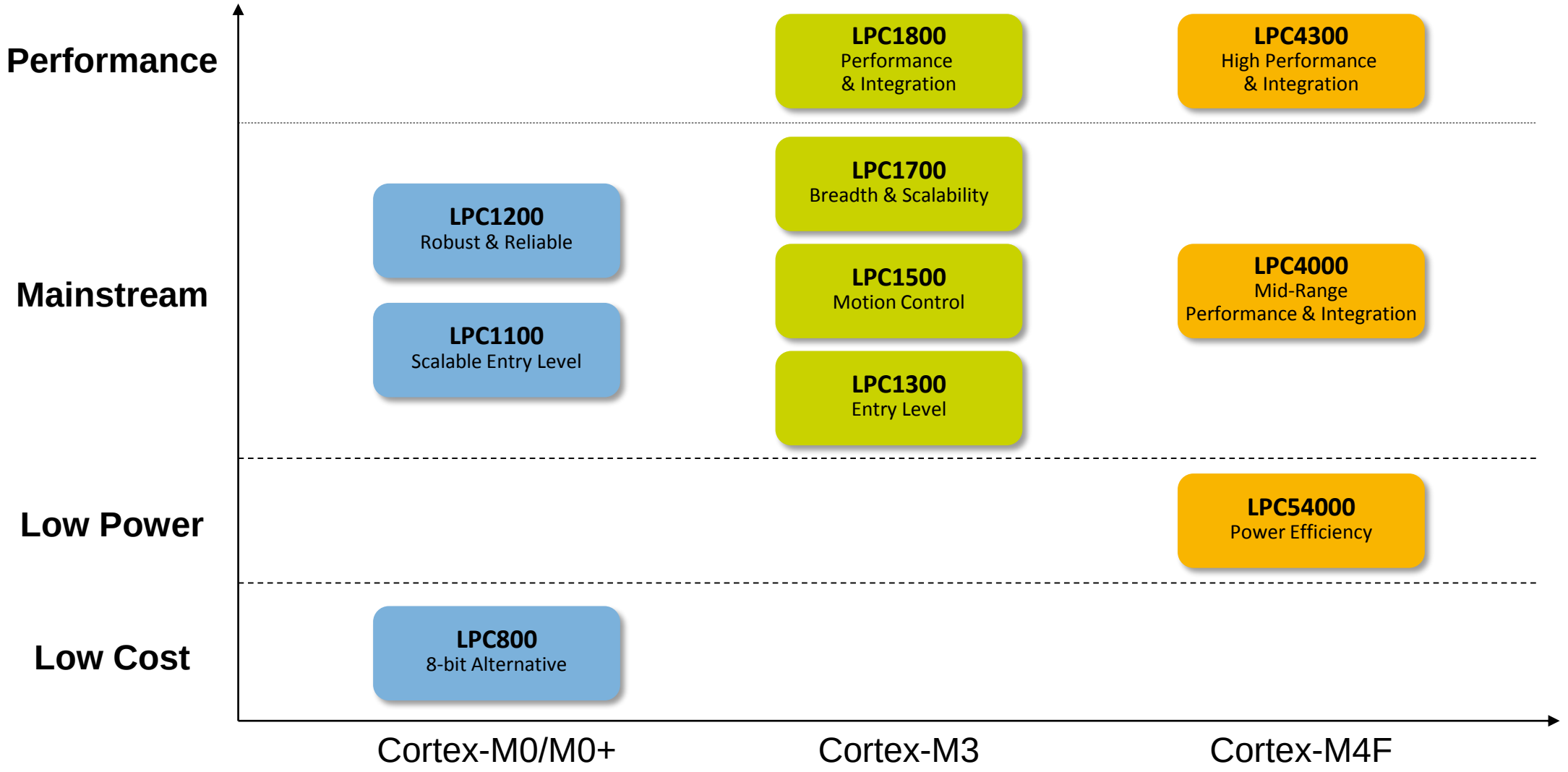
LPC MICROCONTROLLER PORTFOLIO OVERVIEW

NXP'S Breadth in Microcontrollers

Kinetis + LPC = Broad Portfolio of Microcontroller Families



Continuity in the LPC Cortex-M Microcontroller Portfolio



Introducing LPC54000 Series of Power Efficient Microcontrollers

LPC5410x

entry level

Cortex-M4F at 100 MHz
1.62 V to 3.6 V
256-512 KB Flash
104 KB RAM

Two product families
Optional coprocessor

LPC5411x

mass market appeal

Cortex-M4F at 100 MHz
1.62 V to 3.6 V
128-256 KB Flash
96-192 KB RAM
FRO, FS USB, DMIC

Two product families
Optional coprocessor

LPC542xx

extended memory & added security

Cortex-M4F at 100 MHz
1.62 V to 3.6 V
512-704 KB Flash
256-320 KB RAM
FRO, FS USB, DMIC

Three product families
Optional coprocessor,
Optional security

LPC546xx

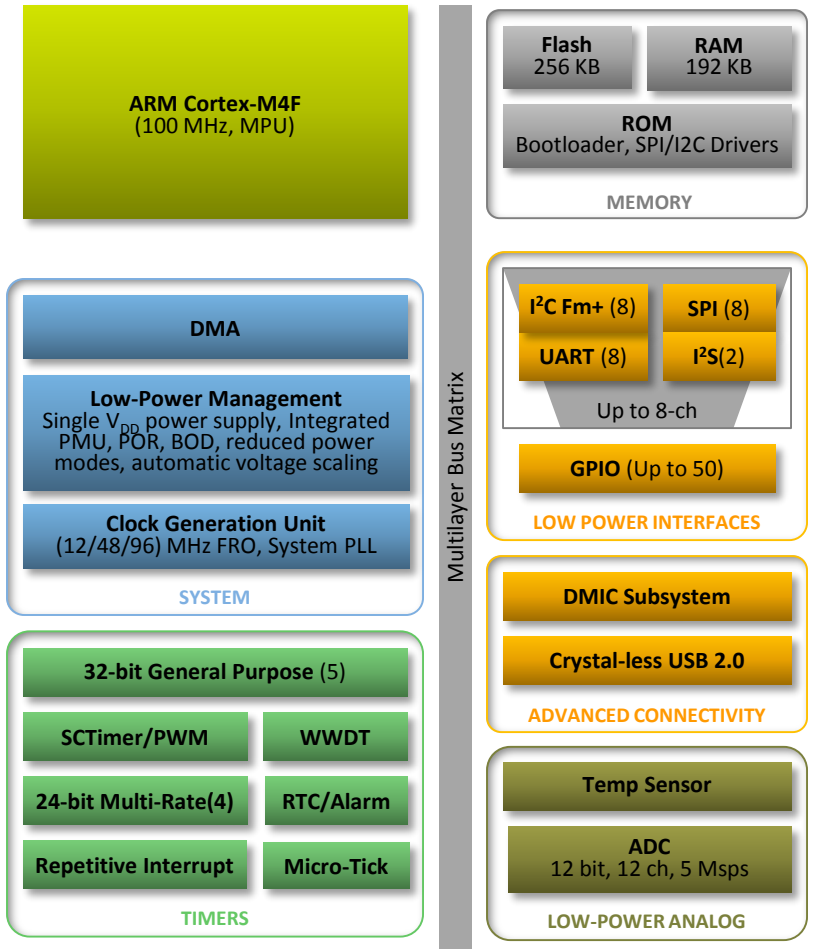
added performance & integration

Cortex-M4F at 180 MHz
1.62 V to 3.6 V
256-512 KB Flash
136-200 KB RAM
FRO, FS/HS USB, DMIC

Six product families,
Optional TFT-LCD Controller,
Ethernet, CAN FD,
& Security

LPC54113: 100MHz Cortex-M4F with 256 KB Flash

Block diagram and key features



CPU

- **100MHz Cortex-M4F**

Memory

- 256 KB Flash, **192 KB RAM**

Interfaces for connectivity & sensors

- Stereo DMIC subsystem
  - (PDM, decimator, HW VAD)
- **8 SPI, 8 I2C, 8 UART, 2 I²S channels.**
  Max 8 channels
- **Crystal-less FS USB**
- Power-efficient **5.0 Msps, 12-bit ADC**: full-spec performance (1.62 to 3.6V, -40 to 105 °C)

Clocks & timers

- **12/48/96 MHz FRO**, 100 kHz-1.5MHz WDOG OSC, 32 Xtal OSC, external clock input
- Basic & advanced timers including SCTimer/PWM
- Asynchronous peripheral bus

Packages

- LQFP64 (10 x 10 mm)
- WLCSP49 (3.45 x 3.45 mm)

Other

- Operating voltage: 1.62 to 3.6V
- Temperature range: -40 to 105 °C

Availability

LPC5411x Silicon
LPCXpresso 54114 (OM13089)
LPC54114 Audio & Voice Recognition Kit (OM13090)

Limited Early Access Samples **NOW**
Market Announcement **Embedded World**
Full Market Launch **May 30, 2016**
(WLCSP MP Jul-2016)

Target Applications

Consumer / Wearable / Personal Health Mgmt

- Wearables, fitness monitoring, home healthcare, and patient monitoring

Gaming / Entertainment

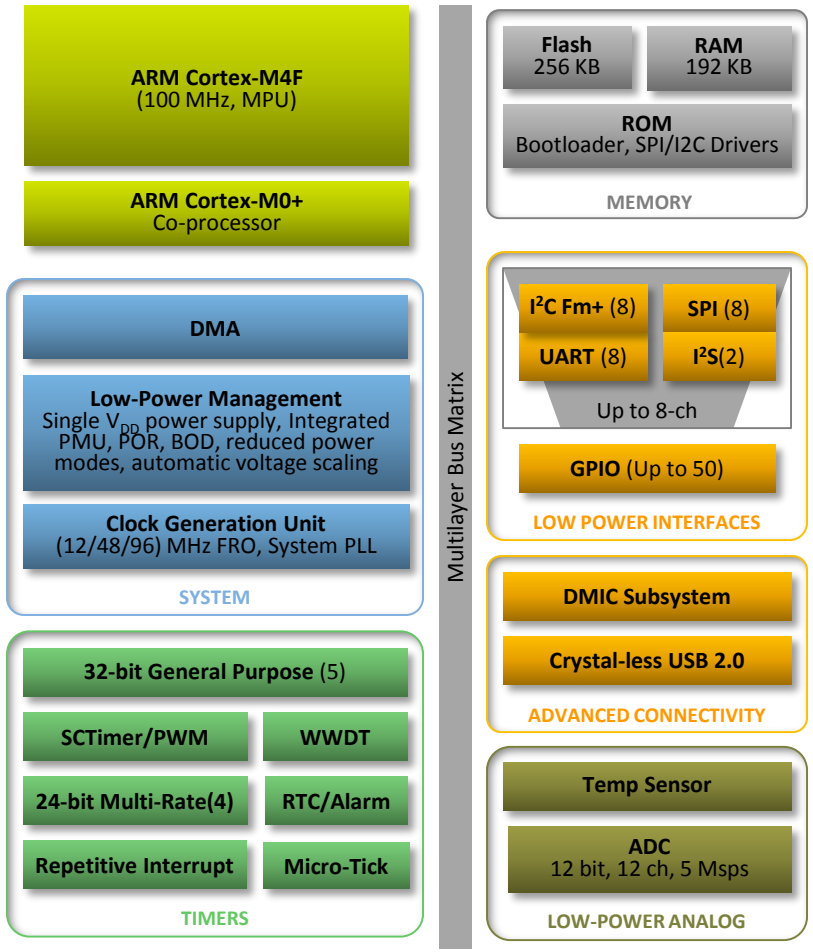
- Console / user motion control and orientation, voice and sound activation, general toys

Home / Building Automation & Control

- Access and lighting control, HVAC and smart thermostats, fire, safety and security
- UI with voice and sound activation

LPC54114: 100MHz Cortex-M4F/M0+ with 256 KB Flash

Block diagram and key features



CPU

- **100MHz Cortex-M4F**
- **Cortex-M0+ Co-processor**

Memory

- 256 KB Flash, **192 KB RAM**

Interfaces for connectivity & sensors

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LPC5411x Target Application
Always-on battery operated device

Low Active Currents for Always-On Processing

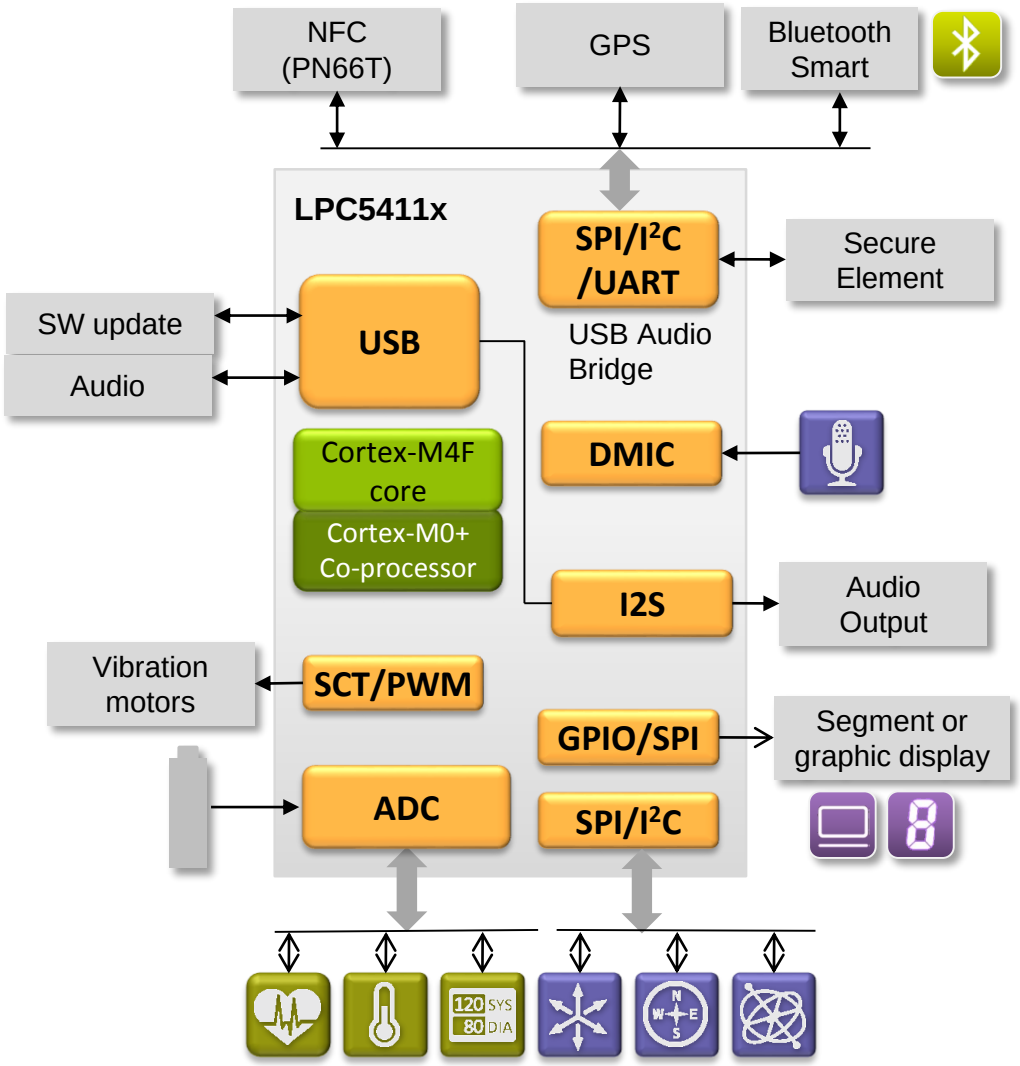
- ARM® Cortex® **M4F <85 µA/MHz** (from RAM at 48MHz)
- ARM® Cortex® **M0+ <65 µA/MHz** (from RAM at 48MHz)
- **7 uA (64kB SRAM retention)** with **19us wake-up**
- Optional co-processor for sensor interfacing, data aggregation and system task management

Optimized integration, including on-chip digital microphone (DMIC) subsystem

- Maximize battery life through ultra-low power sound detection, voice recognition and activation
- **12-bit, 5 Mbps ADC** for high-precision analog sensor interface, full spec over voltage range: 1.62 to 3.6V
- **Accurate, Low-power FRO Supporting Crystal-less FS USB**

Optimal serial interfaces and peripherals for your application

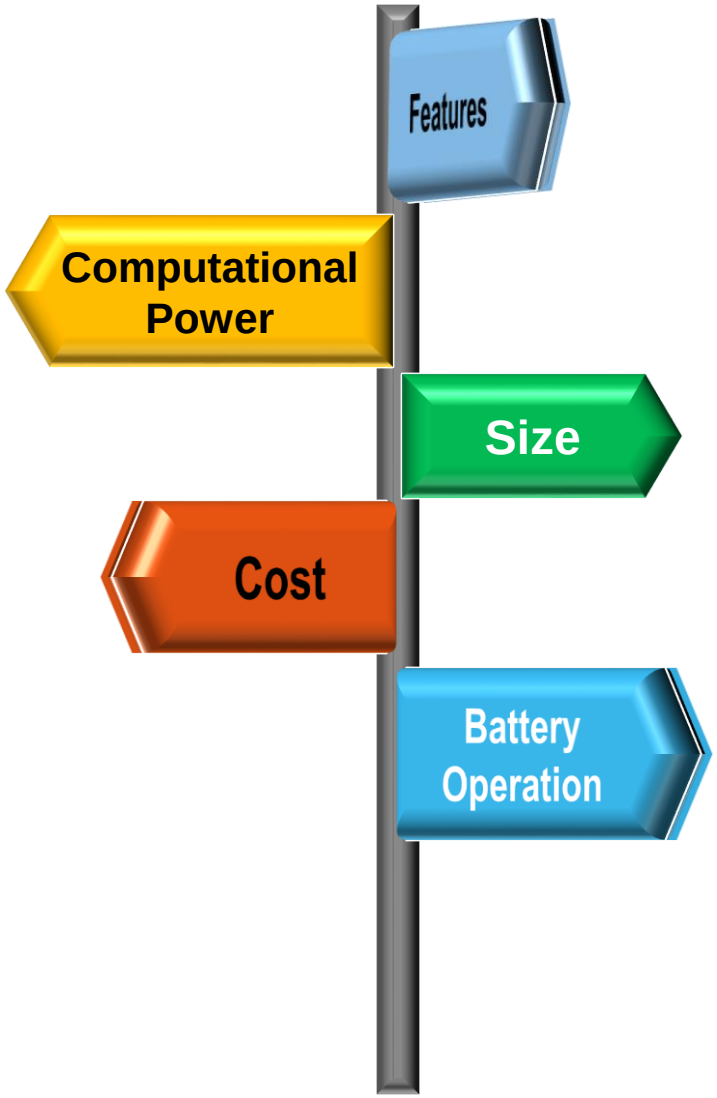
- **Select up to any eight of our FlexComm peripherals**
  - up to 8x SPI, 8x I²C, 8x UART, and 2x I²S
- Up to 48 GPIOs



** Target Dates, Features, Specs Subject to Change*

LEVERAGING LOW POWER DESIGN TECHNIQUES

Low Power: Is It More Than Just an Industry Buzzword?

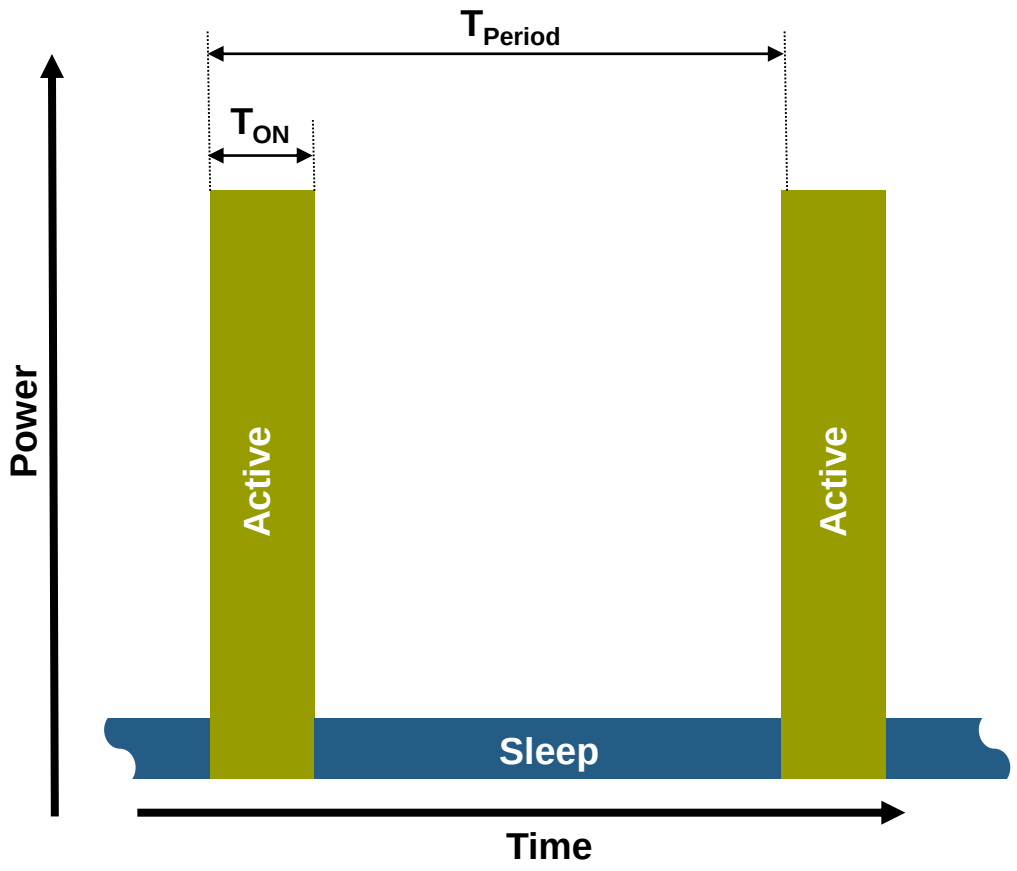


1. Everybody wants “lower power” …
   … but it can mean different things depending on the application

2. The IC / system implementation and choices can be different depending on the desired optimization point

3. There are a lot of “engineering benchmark” and number fights in the industry …

Typical Application for a Microcontroller

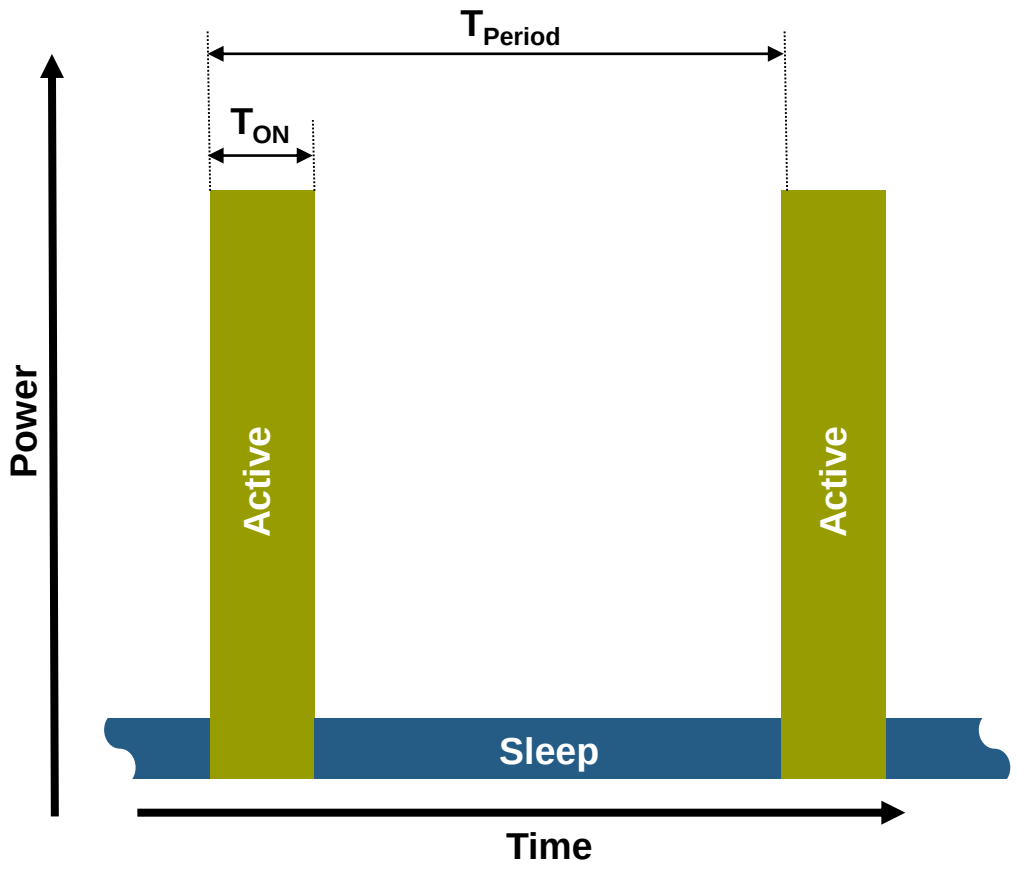


"Duty Cycle" is the ratio of "Active" time (T_{ON}) over the period (T_{period})

Instantaneous power consumption is important
→The device cannot demand more volt-amps which are available from the energy source

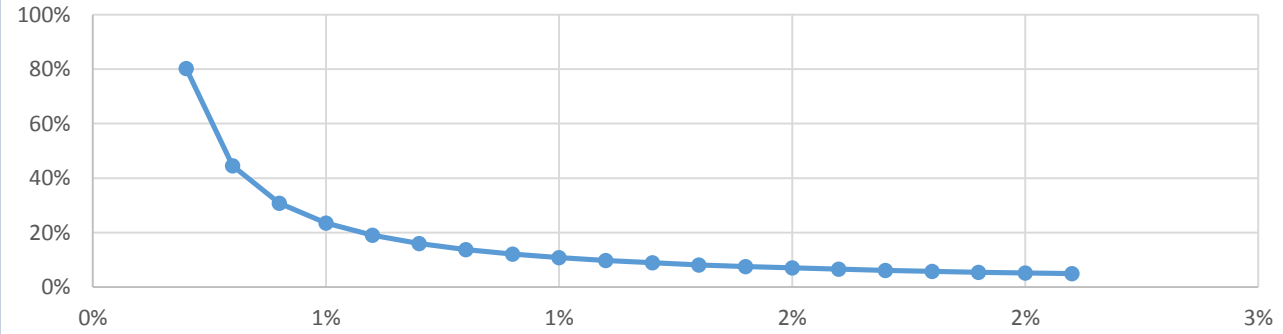
But even more important is the energy consumption (energy is the integration of power over time – the area under power curve)
→Energy consumption determines the battery life

Why Do I Need to Understand the Power Profile of My Application?



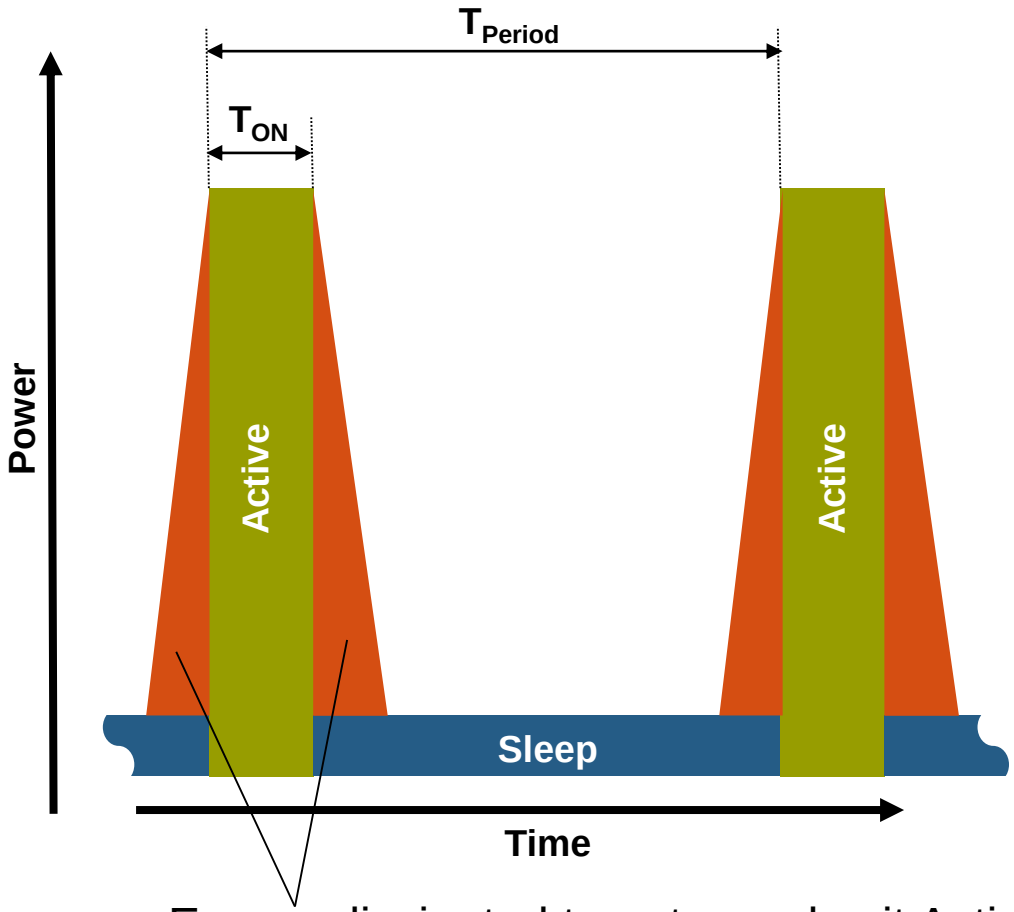
Example:

- 1uA leakage
- 85uA/MHz
- 48MHz operation in active mode



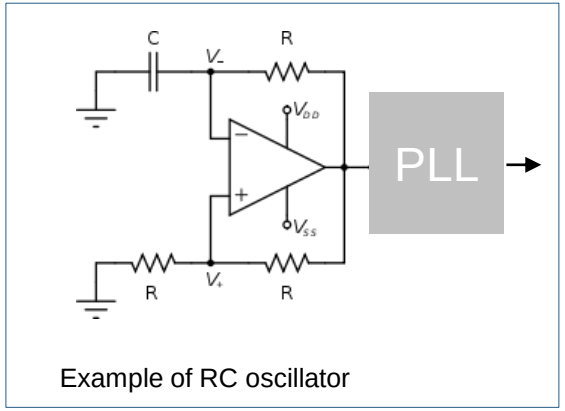
1. Depending on Duty Cycle, the overall energy consumption can be dominated either by the sleep or active power consumption
2. Even with 99.9% duty cycle, Energy consumption in Active Mode is 4x Energy in Sleep Mode

Multiple Areas to Optimize: Wakeup Time



Energy dissipated to enter and exit Active Mode → reducing this time is critical

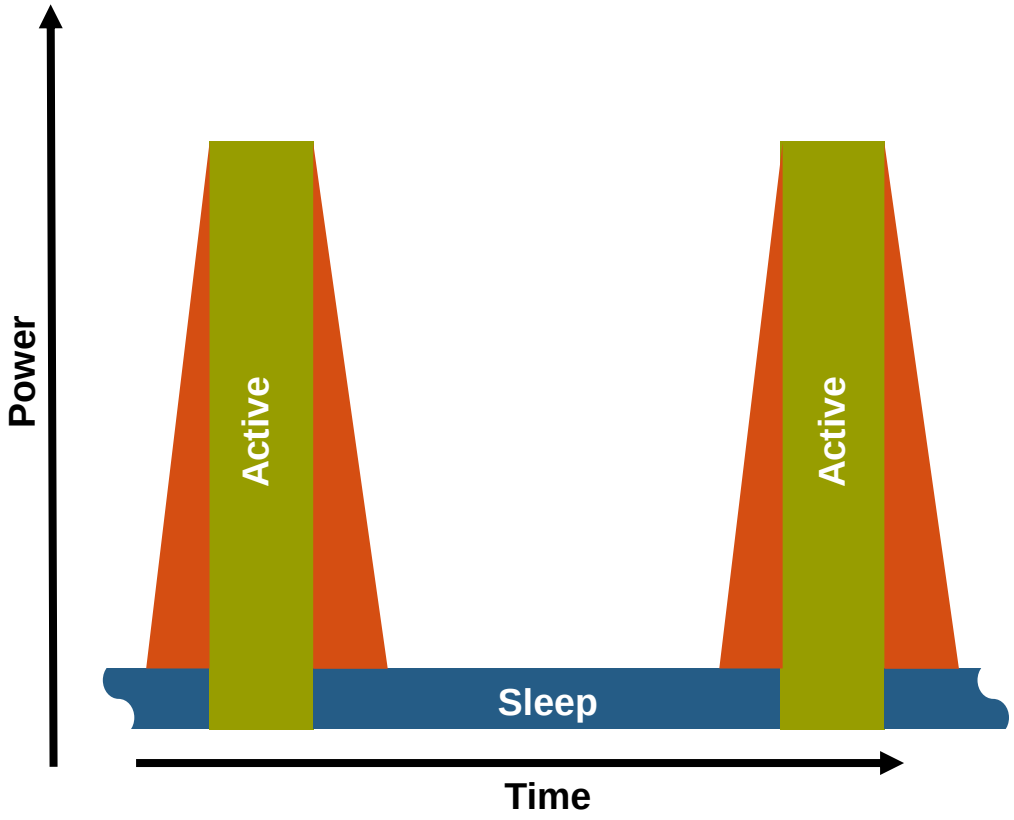
IRC + PLL



FRO

X10 reduction in wakeup time

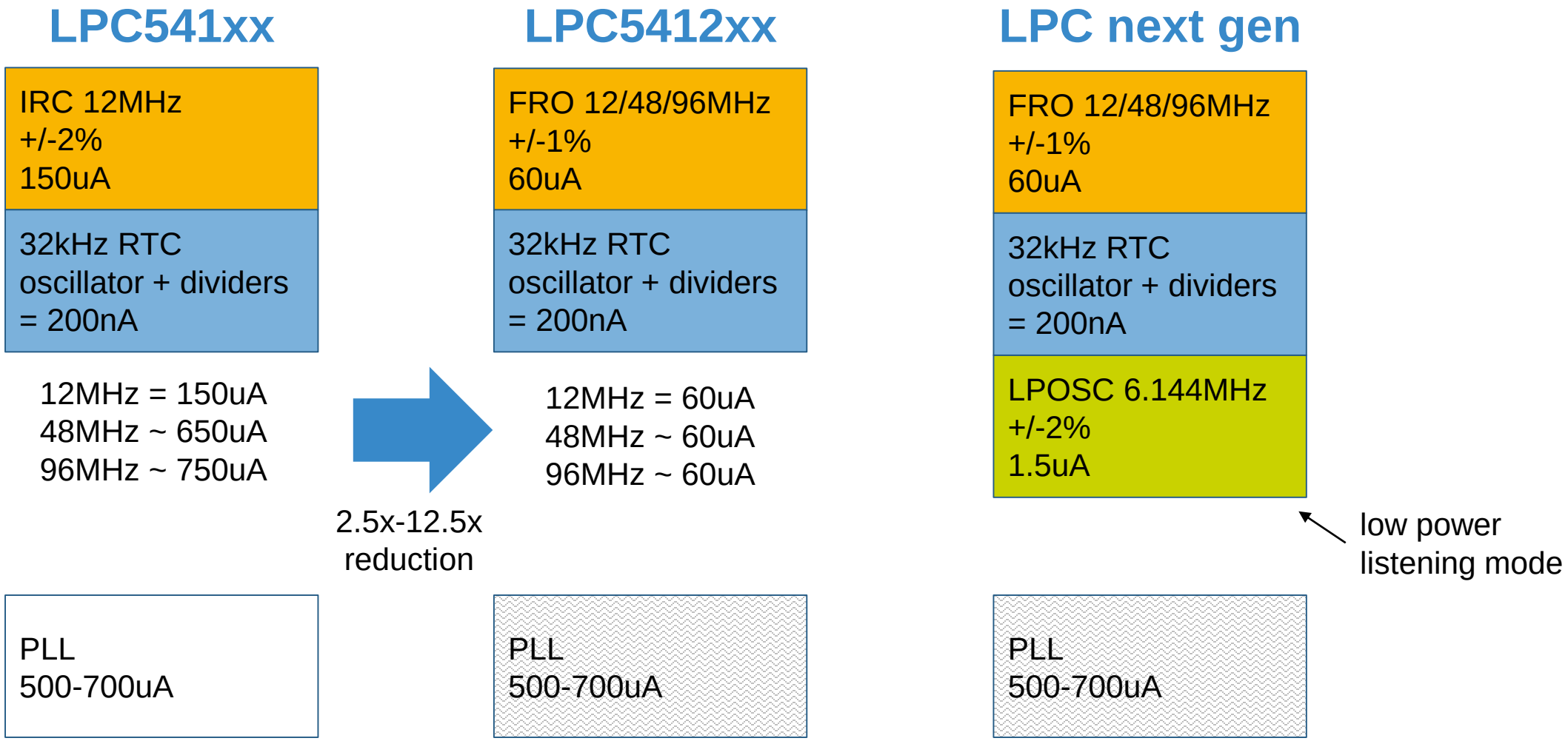
Multiple Areas to Optimize: Active and Sleep Mode Optimizations



(Some of the) techniques to reduce power consumptions in Active Sleep Mode

- Clock Generation
- (Auto) Clock Gating
- Low Power Voltage Regulator
- Low power oscillator
- Ultra Low Power Voltage Regulator
- Source Biased RAM
- …

Clock Generation

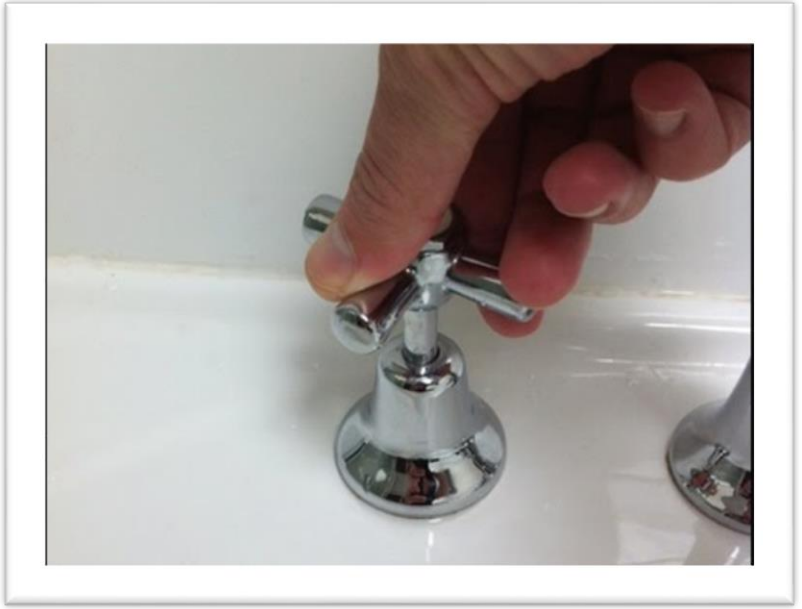


What is Clock Gating?

- **Clock Gating** is a technique used in synchronous circuits for reducing dynamic power consumption, by adding logic to a circuit to prune the clock tree
- It disables portions of the circuitry so that the flip-flops to avoid unnecessary switch states
- Clock gating works by taking the enable conditions attached to registers, and uses them to gate the clocks
- Mote that the clock gating logic will change the clock tree structure, since the clock gating logic will sit in the clock tree
- Clock gating logic can be added into a design in a variety of ways:
  - Coded into the RTL as enable conditions that can be automatically translated into clock gating logic by synthesis tools (fine grain clock gating)
  - Inserted into the design manually by the RTL designers (typically as module level clock gating) by instantiating library specific ICG (Integrated Clock Gating) cells to gate the clocks of specific modules or registers
  - Semi-automatically inserted into the RTL by automated clock gating tools

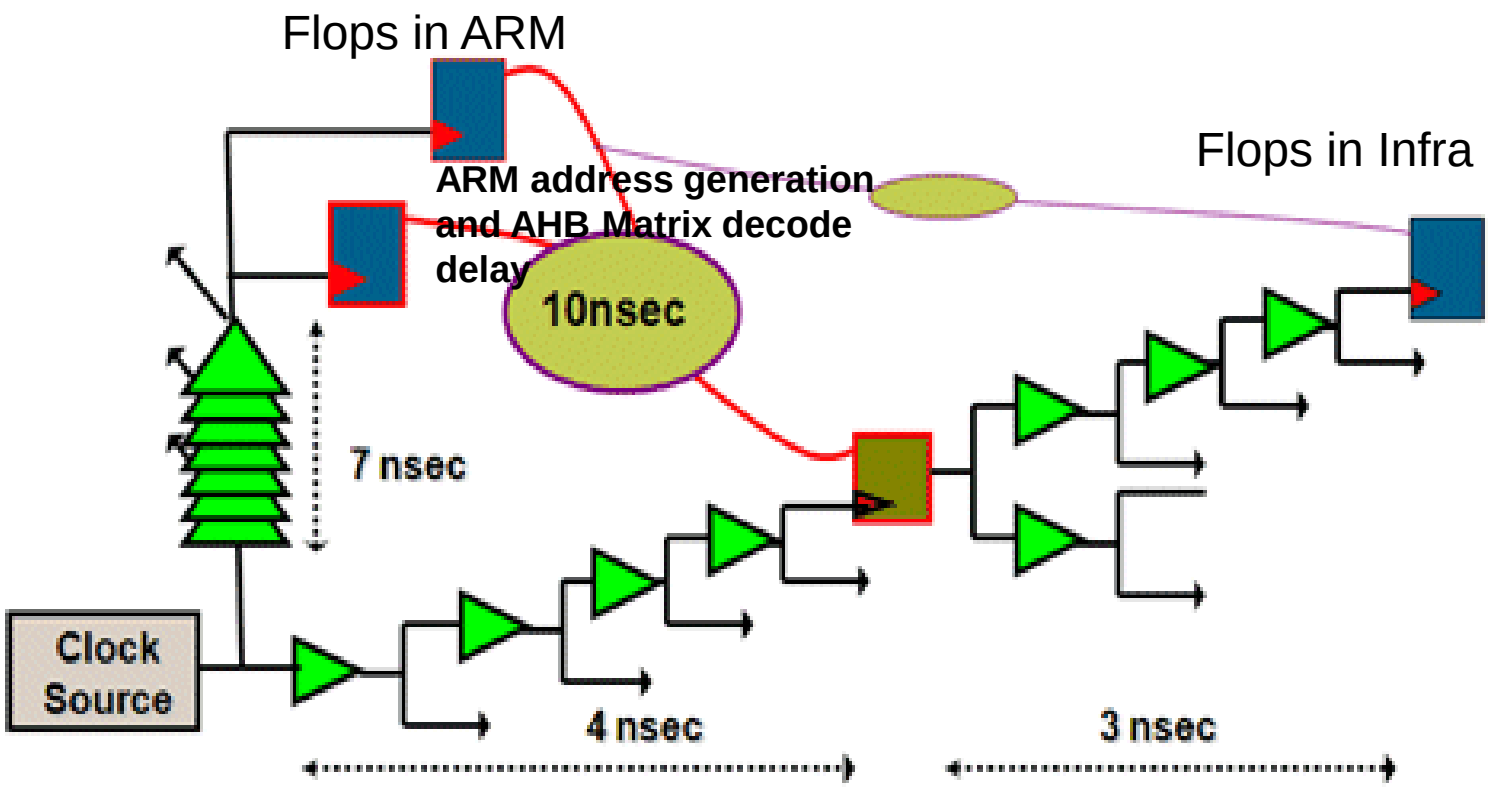
Software Controlled Clock Gating

- The most basic form of dynamic power control is achieved by '**enable**' registers for clock trees
- Software only turns on clocks to **blocks it needs**
- This method for clock control is **common for peripheral clock branch enable**
- Software cannot control the clock enable for the chip's **infra-structure blocks**. That is blocks such as:
  - Bridges
  - Bus fabrics
  - RAM/ROM/FLASH controller
  - Chip's main Clock Gating (e.g. in low power mode)



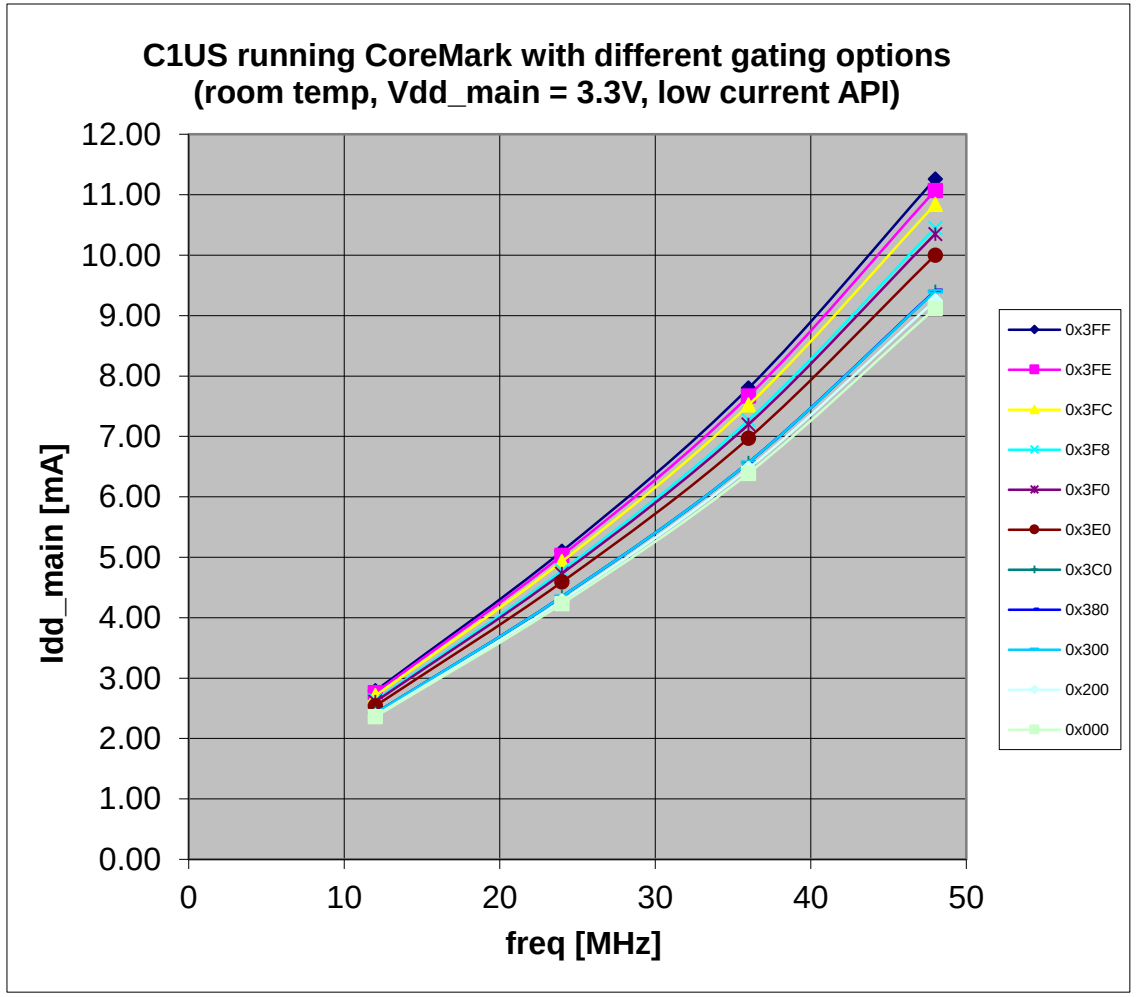
Auto Clock Gating

- Auto-clockgating needs to be able **dynamically** decide when a clock should be turned on/off for a logic cloud
- Can use **bus 'SEL'** –
- Turn OFF clock when block not accessed



Making a live decision can limit circuit speed, in this case to 13ns!!

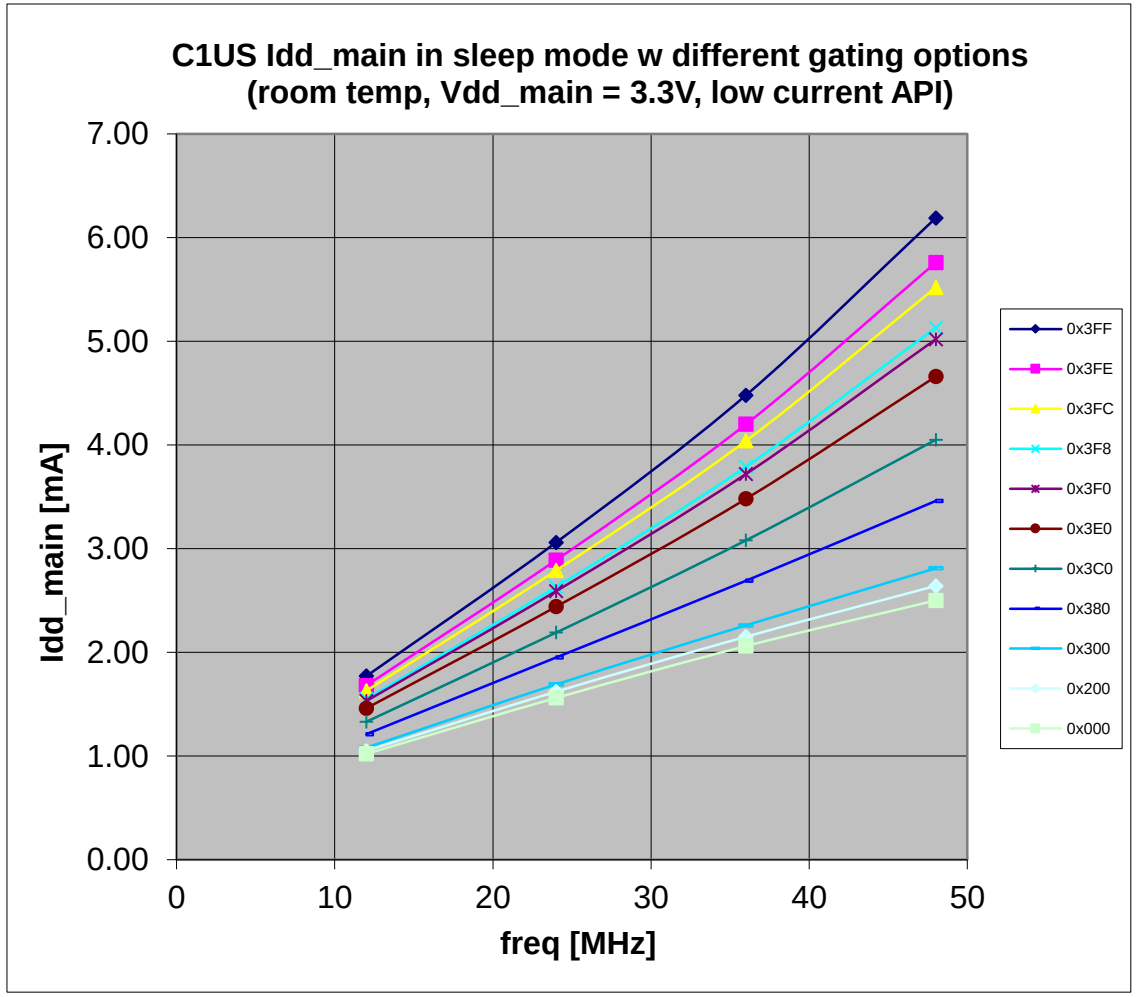
C1US Auto Clock Gating Results Dynamic Power



Clock gating control bits
('0' to enable auto gating)

0 – RAM0
1 – ROM0
2 – RAM1
3 – ROM1
4 – RAM2
5 – FLASH VPB
6 – FLASH AHB
7 – AHB MATRIX
8 – AHB2VPB BRIDGE
9 – SYCON REGBANK

C1US Sleep Figures with Auto Clock Gating



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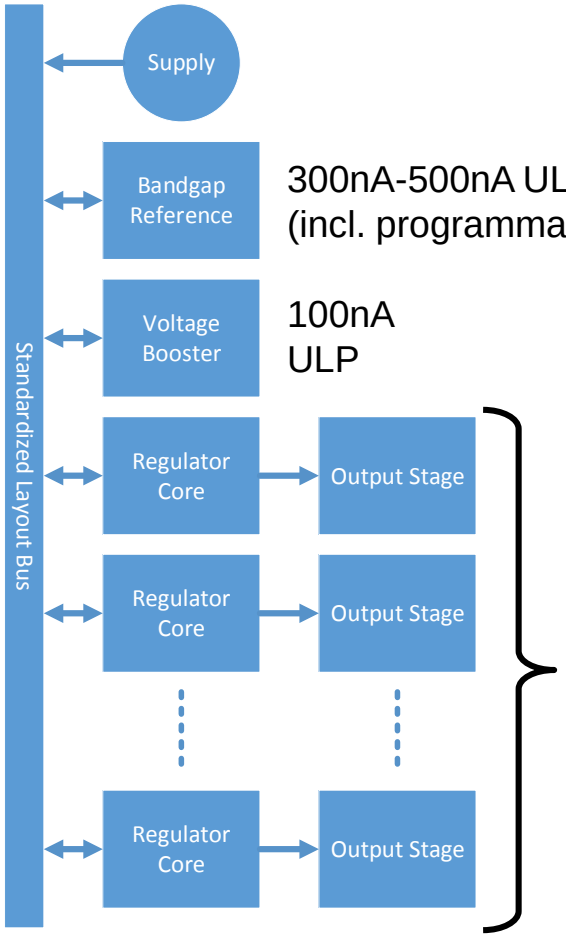
Low Power Regulator:

Supporting a large number of internal supplies for optimum voltage scaling

$$P = f_{clk} a C_{tot} V_{DD}^2 + V_{DD} I_{SC}(V_{DD}) + V_{DD} I_{leakage}(V_{DD})$$

- Use minimum V_{DD} for given task
- Support large number of power domains to allow each task to be completed with minimum power.
- Separately scale voltages to different chip functions (RAM, SB-RAM, ROM, FLASH, CORE, IO, retention domains, analog, RF)
- A power architecture that achieves this flexibility with minimal overhead (area, power) is required
- Supporting a large number of supply domains without the need to add capacitance for stabilization (stable, very fast response time, yet very low power)

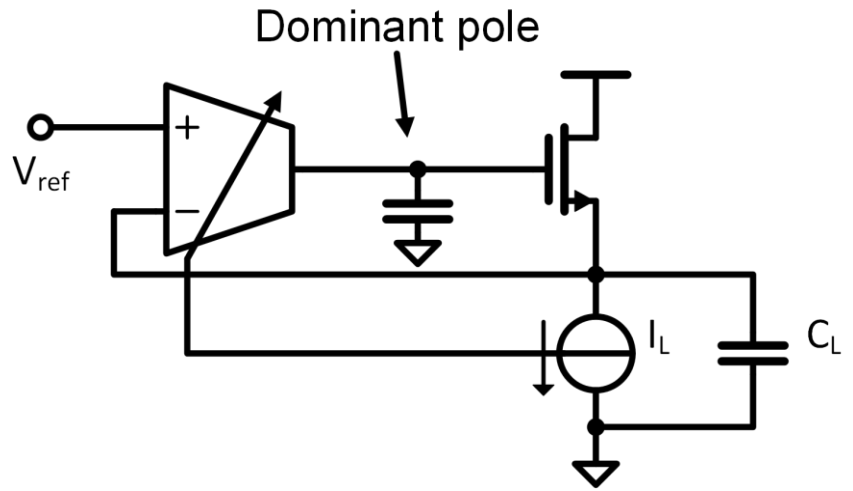
Modular LDO Concept



300nA-500nA ULP
(incl. programmable output)

100nA
ULP

- Modularity to support many voltage domains
- Power consumption will not increase with number of stages
- DVS via software or hardware feedback (PVT) possible
- Fine granularity
- Voltage follower mode (Analog input) to support ATE



- NMOS type regulator → small Zout even at higher frequencies
- Requires charge pump (can be very low power)
- Current feedback loop ensures good load regulation
- Current feedback bias → dominant pole moves with output pole
- High speed clamps → load cap can be small (no extra decap)

Specification of Low Power LDO Design

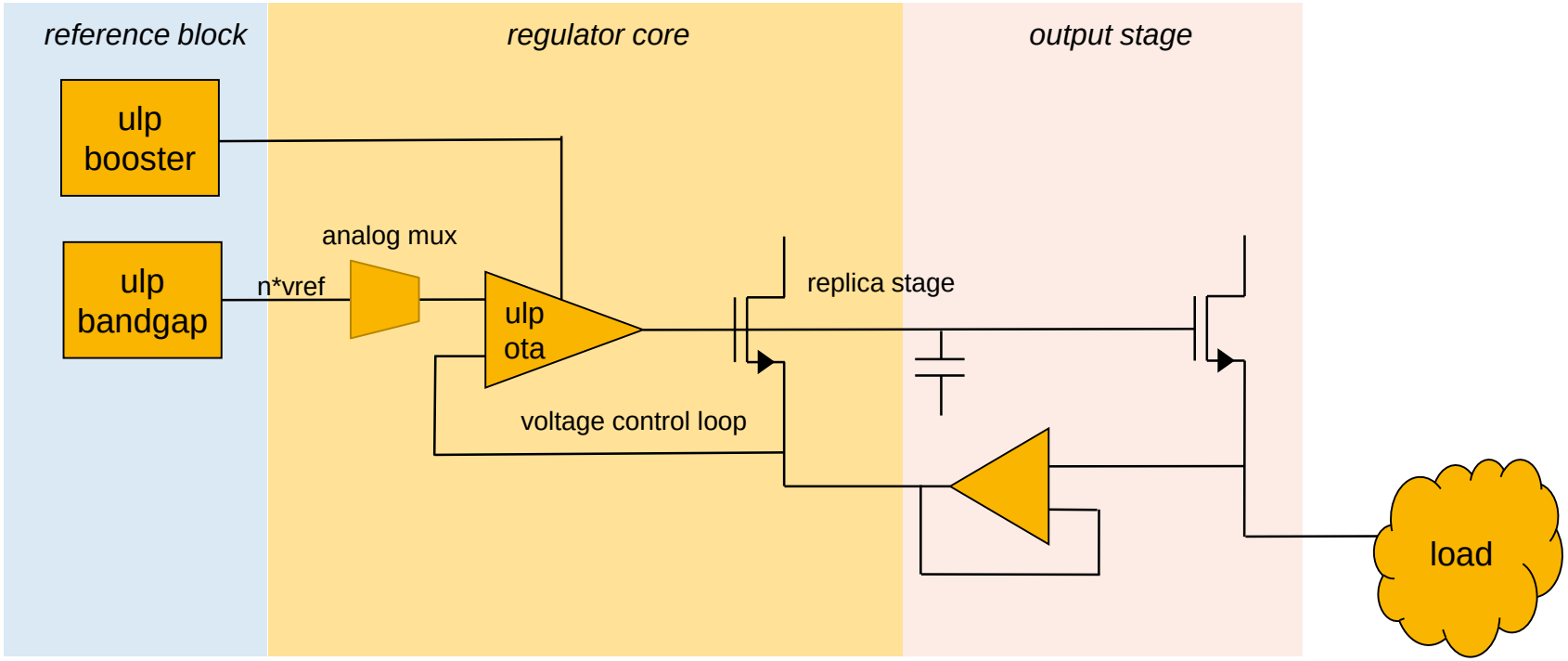
Static specs

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Vdda	Unregulated DC input voltage		1.5		3.6	V
Vout	Output range		0.65		1.40	V
Vout_step	Output step size			50		mV
Vout_acc	Output accuracy	Including bandgap, regular mode	-5%		5%	
Vout_acc_lp	Output accuracy	Including bandgap, low-power mode	-10%		10%	
Vout_acc	Output accuracy	Excluding bandgap	-2%		2%	
IQ	Quiescent current	Disabled, at 27˚C, no load			5	nA
IQ	Quiescent current	Low-power, at 27˚C, no load			100	nA
IQ	Quiescent current	Regular (per slice)			50	uA
Imax	Maximum load current	200mA output stage (magellan version)			200	mA
Vclamp_h[1]	Voltage at which high-side clamp activates	Relative to Vout		+100		mV
Vlcamp_l[1]	Voltage at which low-side clamp activates	Relative to Vout		-100		mV

Dynamic specs

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Tstart	Startup time	Vout within 5% settled		10u	25	us
Cload-max	Max load capacitance	25mA output stage	5			nF
Islope	Load step slope	25mA output stage Iload>100µA, regular power mode, ΔVout<10%			10	mA/µs
PSRR	Power supply rejection ratio		20			dB

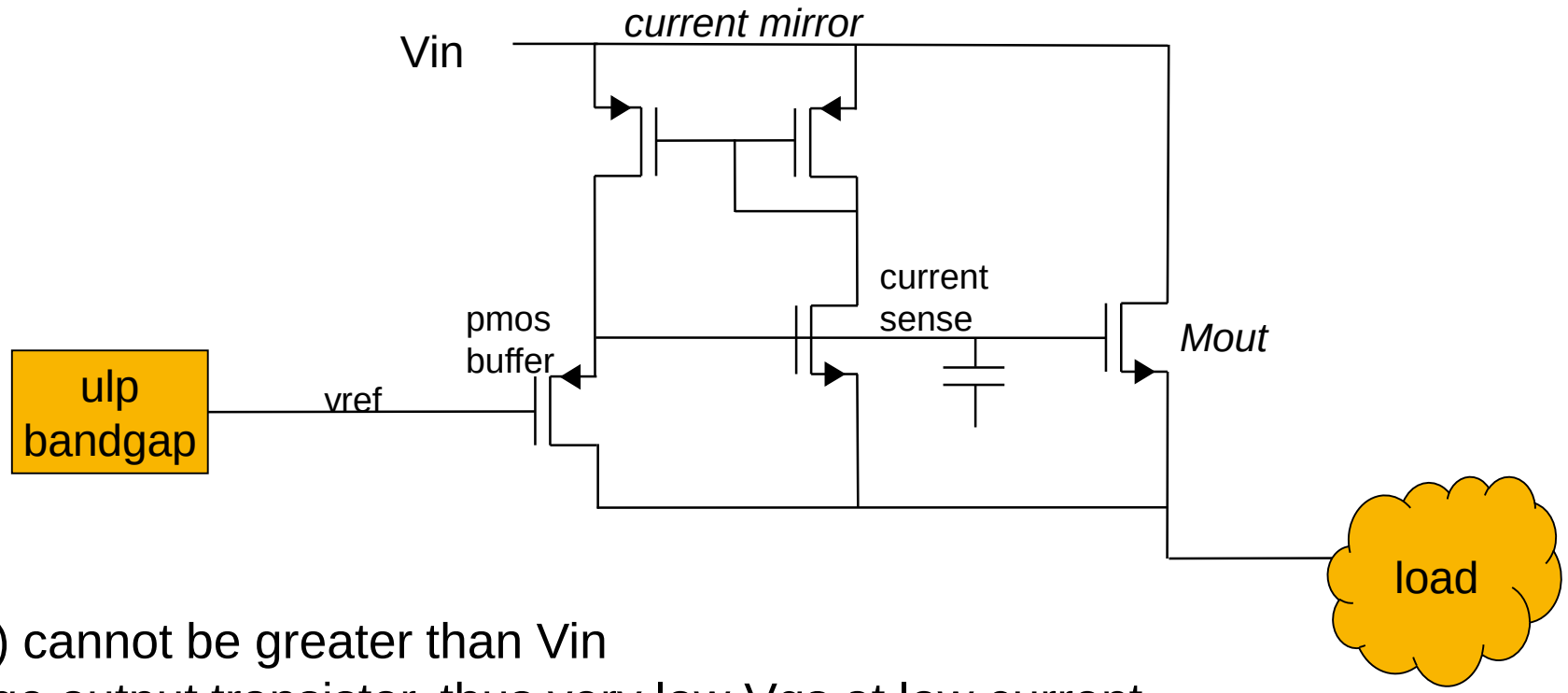
Modular LDO Output Stage Concept



New regulator output stage

- Fully programmable (vref ladder)
- Adaptively biased
- Uses separate bandgap booster in ULP mode to save power

Ultra-low Ireg LDO (LP mode regulation)

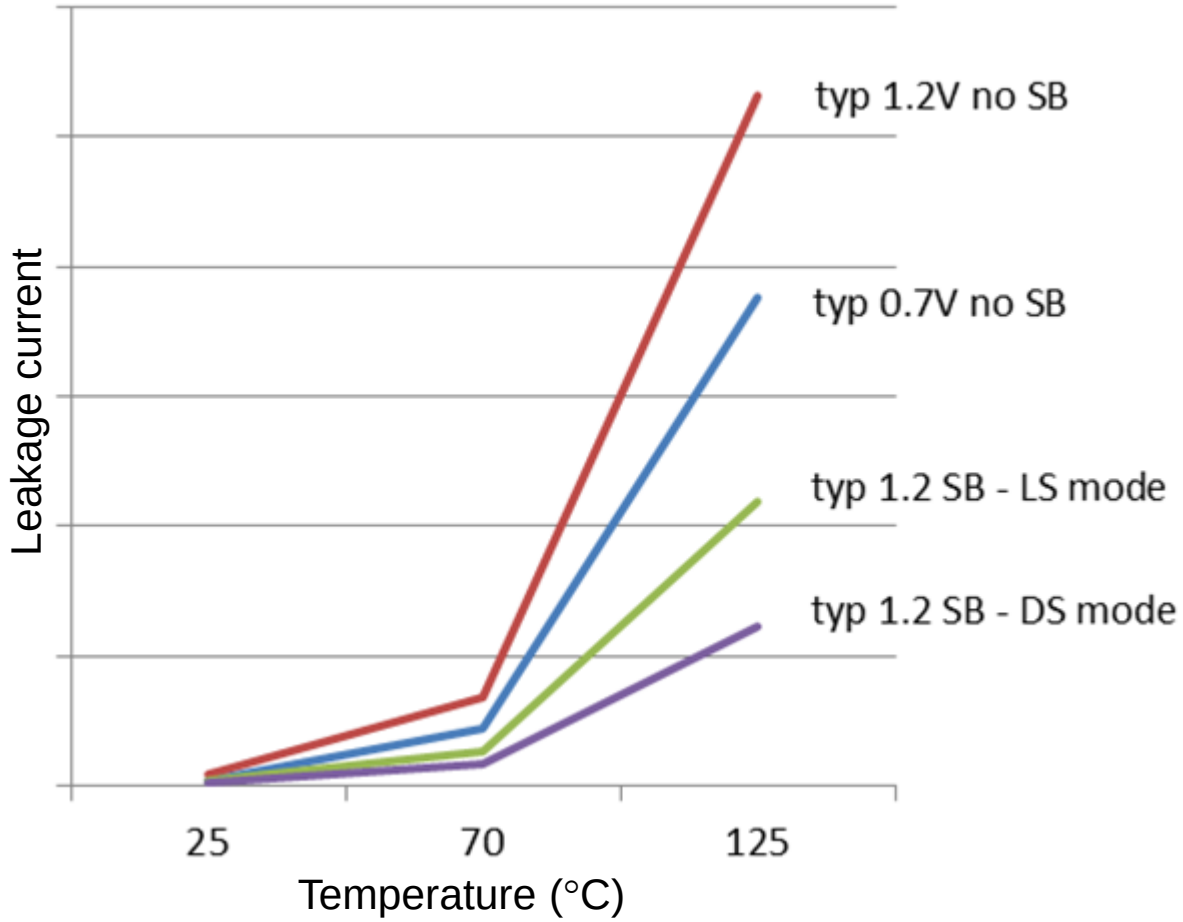


Vg (Mout) cannot be greater than Vin
Same large output transistor, thus very low Vgs at low current

All current is recycled to the output (Near perfect current efficiency LDO) Ireg = 300nA (current for Bandgap)

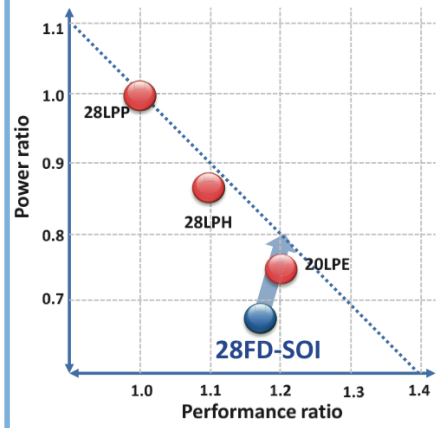
Source Biased RAM to Reduce Leakage

- The source biasing scheme raises the ground voltage of the memory cell in the standby mode to achieve a large reduction in the leakage current
- Implementations:
  - Light sleep mode (Source biasing for Matrix)
  - Deep sleep mode (periphery shutdown + Source biasing for Matrix)



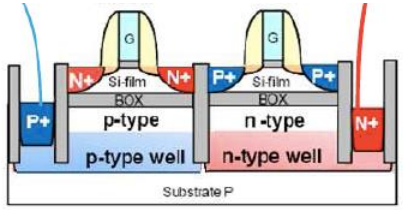
WHAT IS NEXT?

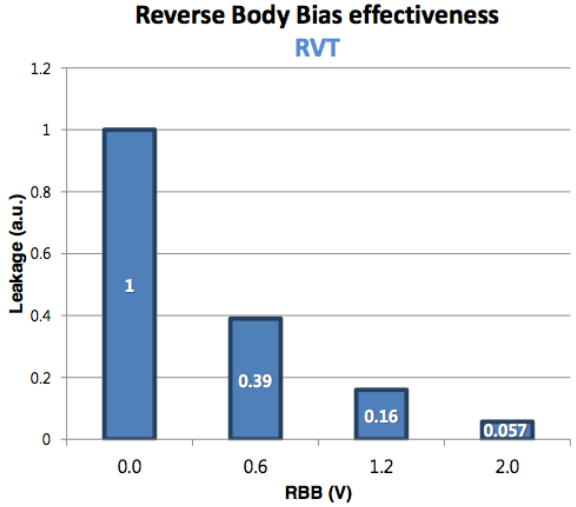
28nm FD-SOI as the Next Technology Node



	28LPP	28 FD-SOI[1)]	28LPH	20LPE
Performance @Same Leakage	1	**1.18**	1.08	1.20
Power @Same Speed	1	**0.67**	0.87	0.75
Area	1	**1**	1.04	0.70

- Tailored to the ULP family
  - Lower voltage operation
  - Range from <.7 volts to 1.1 volts
- Low power with on-demand performance
- Advanced process without double patterning to keep cost low



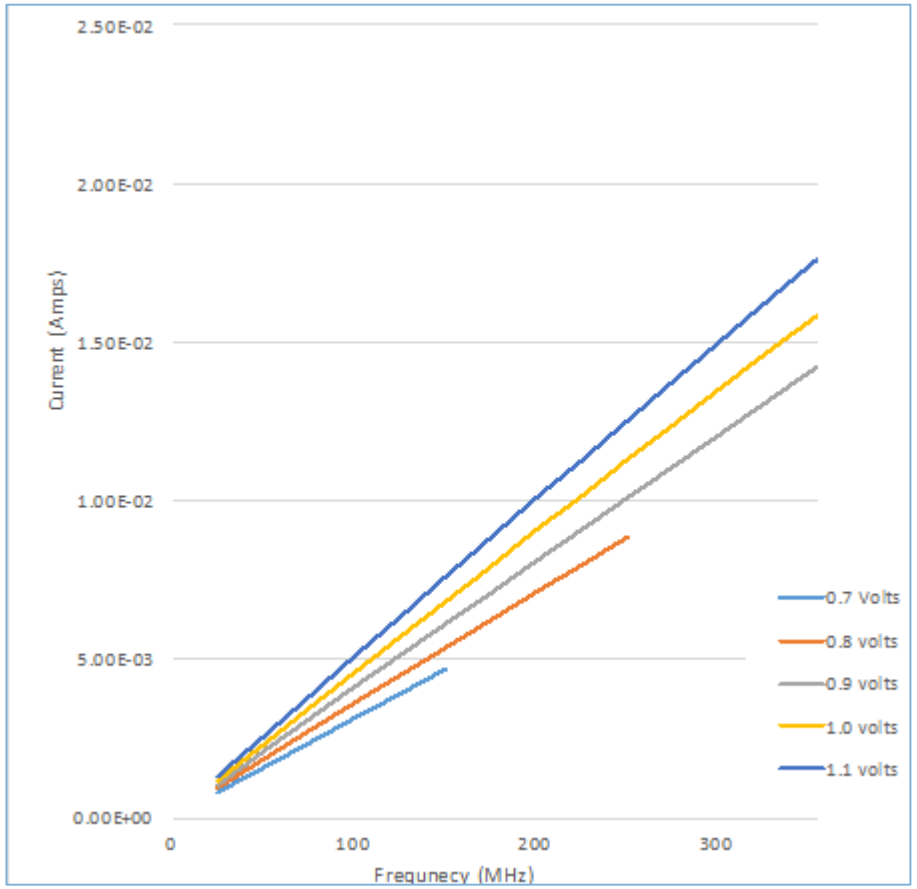


Much lower leakage than 28LPP

- More than an order of magnitude better using RBB
- RBB not limited by body diodes

Unparalleled Low Power Performance…but It Will Take Some Time

Cortex-M4 performance: test chip results (Q1-16)



- <10uA/MHz @ 300MHz with DCDC
- Wakeup time from deep sleep to 100MHz in <5us
- Deep Sleep with 256k byte SRAM retained: 2.4uW
- Active mode (core and memory) consumption @ 300MHz <10uW

SECURE CONNECTIONS
FOR A SMARTER WORLD

ATTRIBUTION STATEMENT