FTF 2016
TECHNOLOGY FORUM

HARDWARE DESIGN GUIDE FOR AUTOMOTIVE PROCESSORS

FTF-AUT-N1809

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PUBLIC USE

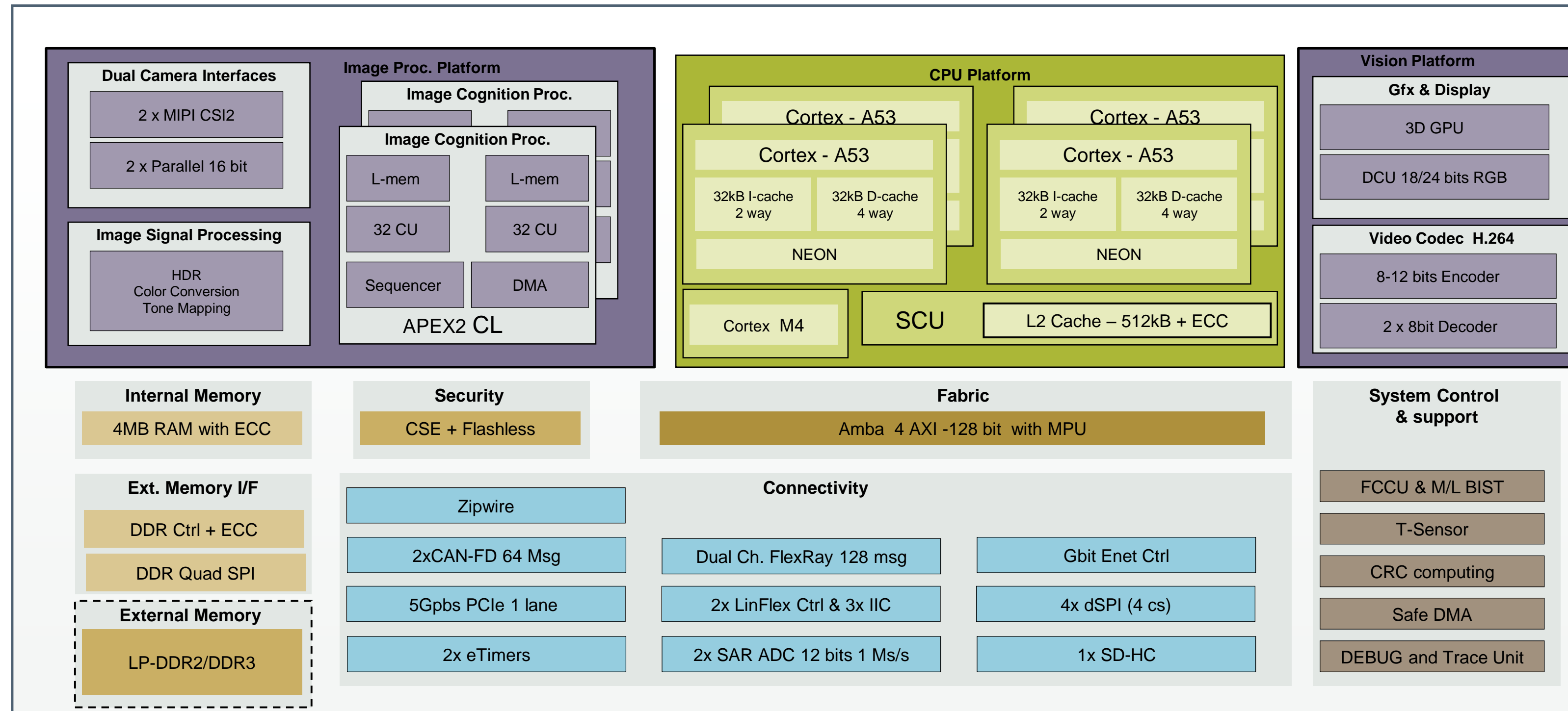
AGENDA

- The S32V234 Processor
- Memory Architecture and Booting
- Camera Connectivity
- Display Connectivity
- Communications Interfaces
- Power Supply Design
- Multiplexing and Configurable Supplies
- Package Considerations

S32V234

- Vision processing MPU
  - multiple ARM® Cortex®-A53 CPUs and one Cortex-M4 CPU
  - many dedicated modules and processors for acceleration of vision processing tasks
  - Developed according to ISO 26262 with an integrated safety concept
- Automotive applications include front view, surround view and Data Fusion systems
  - Scalable
- Includes leading edge camera vision modules like APEX2, ISP, and GPU
- Full enablement environment
  - OS, Libraries/SDK & application examples

S32V234 Block Diagram



Specifications:

- **CPU1-4:** ARM Cortex-A53 @1GHz, L1/L2 cache with ECC & Neon
- **CPU5:** Cortex -M4 for IO control with I/D Cache and ECC
- **ICP:** 2 x APEX2 CL (MIMD APU-64 CU each) at 400MHz
- **GPU:** GC3000 from Vivante
- **Package:** 17x17**FC-BGA**
- **Temp Range (Ta):** -40 to 105°C, 125 °C Tj, AEC-Q100 Grade 2
- **Main Supply:** 3.3V IO and 0.94V Core - external PMU + DDR rails

Key Features:

- **F. Safety:** developed as per ISO26262 with target ASILB
- **SW Enablement:** OpenCL Tools for ICP, GPU, NEON.
- **Video Codec:** H.264 Encoder (8-12 bit) + Decoder (8 bit)
- **DRAM:** External LPDDR2 & DDR3 supported
- **Security:** SHE (almost) compliant Crypto Security Engine
- **Surround 3D**: 3D unified architecture. 19/38Gflops at 600MHz
- **Video dist. Network**: 2X Mipi CIS2 – 4 Virtual channels each
- **Connectivity**: Gbit Etehrnet, PCIe, FD-Can & Flexray

S32V234 Block Detailed Diagram

MEMORY ARCHITECTURE AND BOOTING

Memory Architecture

- No NVM on chip
  - (fuses provide configuration setting)
- NAND, NOR and removable storage supported
- “Custom” SRAM on chip
- 2 x SDRAM interfaces for application use
- 130 – 150 pins used to connect memory in a typical application
- Important to get memory configuration right or performance suffers

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S32V234 Block Detailed Diagram

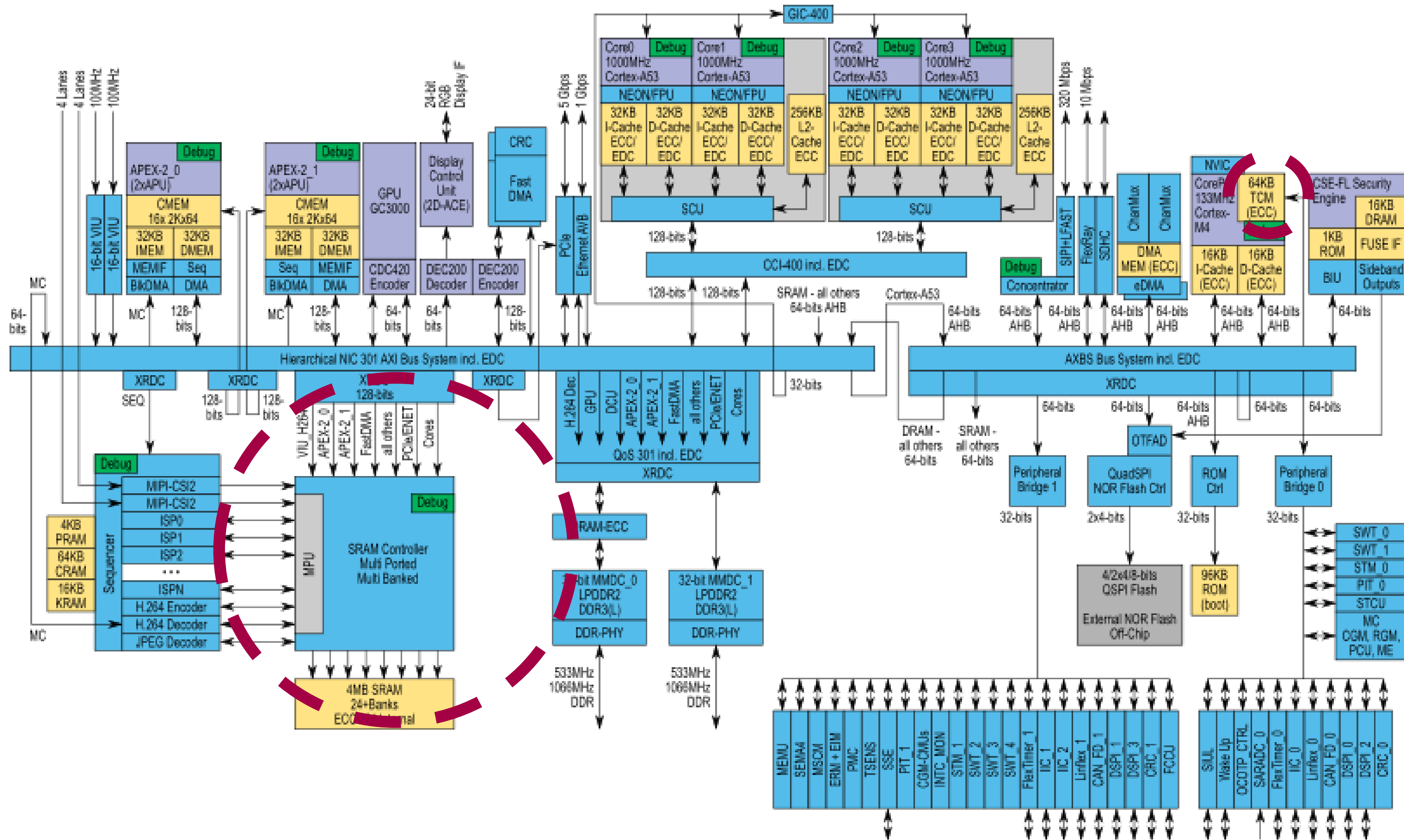
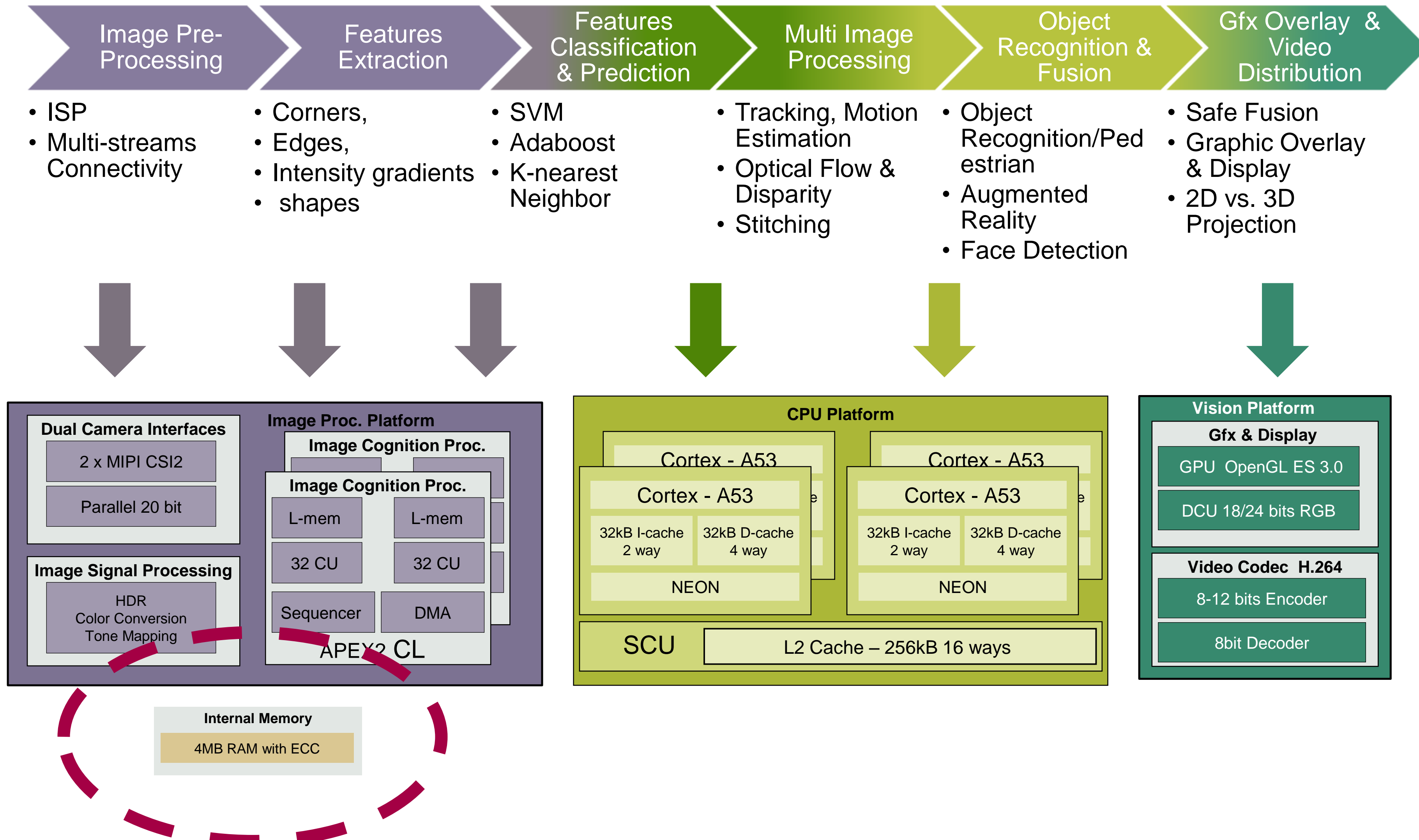
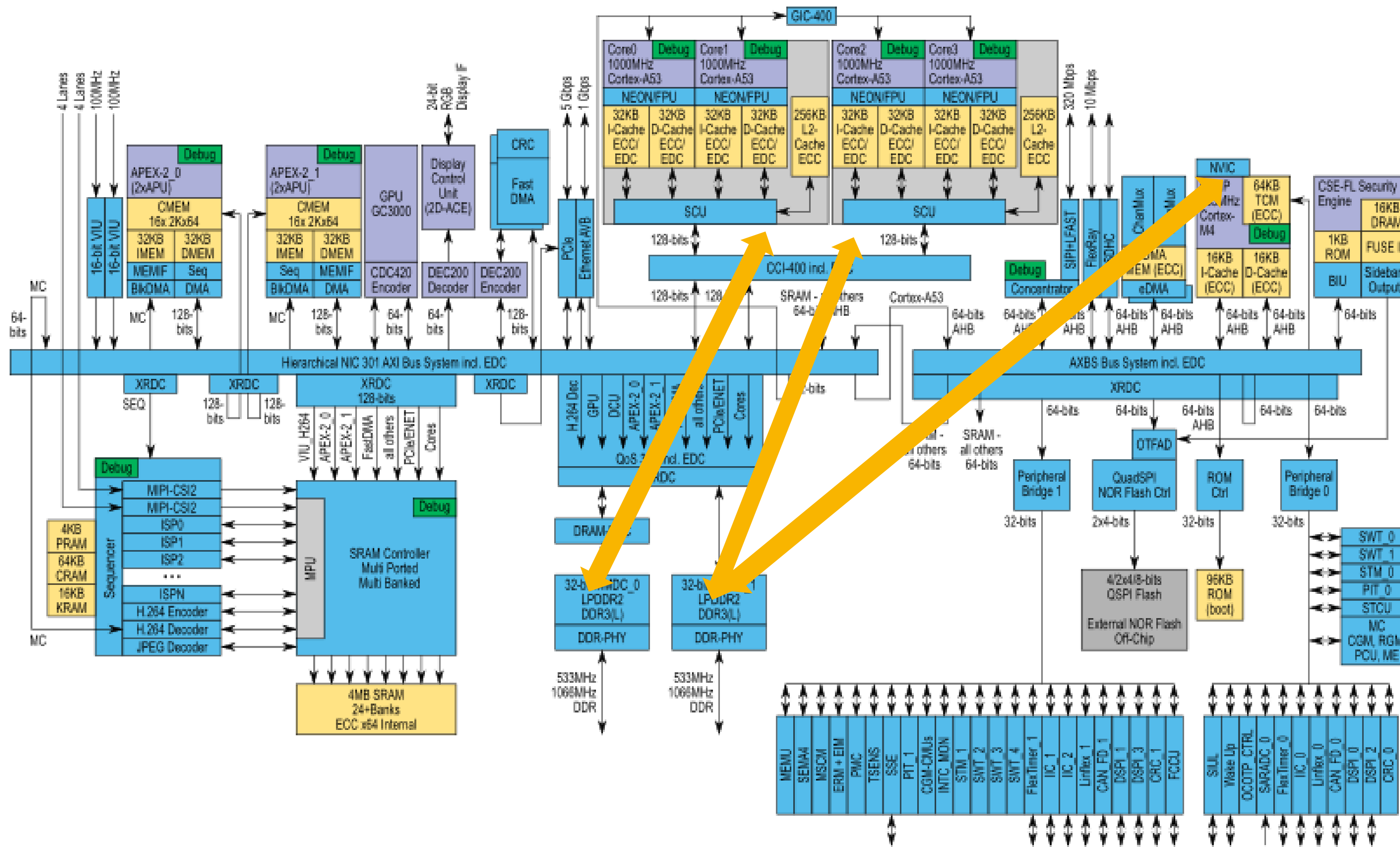


Image Processing & Data Fusion Application Flow



S32V234 Program Memories



S32V234 Data Flow

External NAND flash

S32V234 Program Memories

Choice of memories:

One DRAM or two?

NAND or NOR?

DRAM Interfaces

- There are two independent DRAM interfaces on the S32V234
- Each supports DDR3, DDR3L and LPDDR2 at 533 MHz with a 32-bit data bus
  - Total bandwidth is 8 GBytes/s
    - 2 modules x 4 bytes x 2 edges x 533 MT/s
  - Each has a 1 GB memory space
    - In upper slot the Cortex M4 can only access 512 MB
- DDR3(L) comes in 16-bit wide devices so four are required to fill both DRAM slots
- LPDDR2 has 32-bit wide devices available
- Both technologies have significant optimisations over DDR2 for embedded applications

A Note on DRAM Timing Specification

- There are two different ways of defining timing in the JEDEC specification
  - AC timing and derating values
  - Board simulations require the correct values to be used
- NXP provides only the derating timing in our data sheet
  - Choose matching spec from memory supplier
  - See JEDEC spec for explanatory notes
- This timing relies on a prior calibration being performed to locate the DQS in the middle of DQ window

SDRAM Layout Guidance from Data Sheet

- DDR3 Layout
- Clock, address and Commands
  - Route with 50Ω controlled impedance and differential pair (CLK) with 100Ω controlled impedance
  - Use Fly by topology in case of multiple memory components
  - Terminated to VTT with 50Ω
  - To be referenced with Power, not Ground
  - Address/Cmd to be routed within 66 mils with respect to CLK and to be matched from controller to memory; memory to memory as well
  - All traces to be routed in internal layers
  - Preference is to use only two layers for routing this group
  - Limit the via number to less than three
- Data/Strobe
  - Route with 50Ω controlled impedance and differential pair (DQS strobe) with 100Ω controlled impedance
  - Data to be routed within 33 mils with respect to respective strobe
  - To be referenced with Ground
  - All traces to be routed in internal layers
  - Strictly to be routed in only two layers
  - Avoid more than two vias

- LPDDR2 Layout
- Clock and commands
  - Route with 50Ω controlled impedance and differential pair (CLK) with 100Ω controlled impedance
  - To be referenced with Power, not Ground
  - Command to be routed within 66 mils with respect to CLK and to be matched from controller to memory
  - All traces to be routed in internal layers and delay should be less than 150 ps
  - Preference is to use only two layers for routing this group
  - Limit the via number to less than three
- Data/Strobe
  - Route with 50Ω controlled impedance and differential pair (DQS strobe) with100Ω controlled impedance
  - Data to be routed within 33 mils with respect to respective strobe
  - To be referenced with Ground
  - All traces to be routed in internal layers and delay should be less than 150 ps
  - Strictly to be routed in only two layers
  - Avoid more than two vias

NVM Memories

- The S32V234 provides support for three different standard NVM interfaces
  - SD card
  - eMMC
  - QuadSPI
- Typically SD and eMMC use NAND flash and QuadSPI uses NOR
  - Picking the correct storage option can optimise application performance
- Typically NVM used during booting and for data storage

Summary from Wikipedia

Attribute	NAND	NOR
Main Application	File Storage	Code execution
Storage capacity	High	Low
Cost per bit	Better	
Active Power	Better	
Standby Power		Better
Write Speed	Good	
Read Speed		Good

SD and eMMC

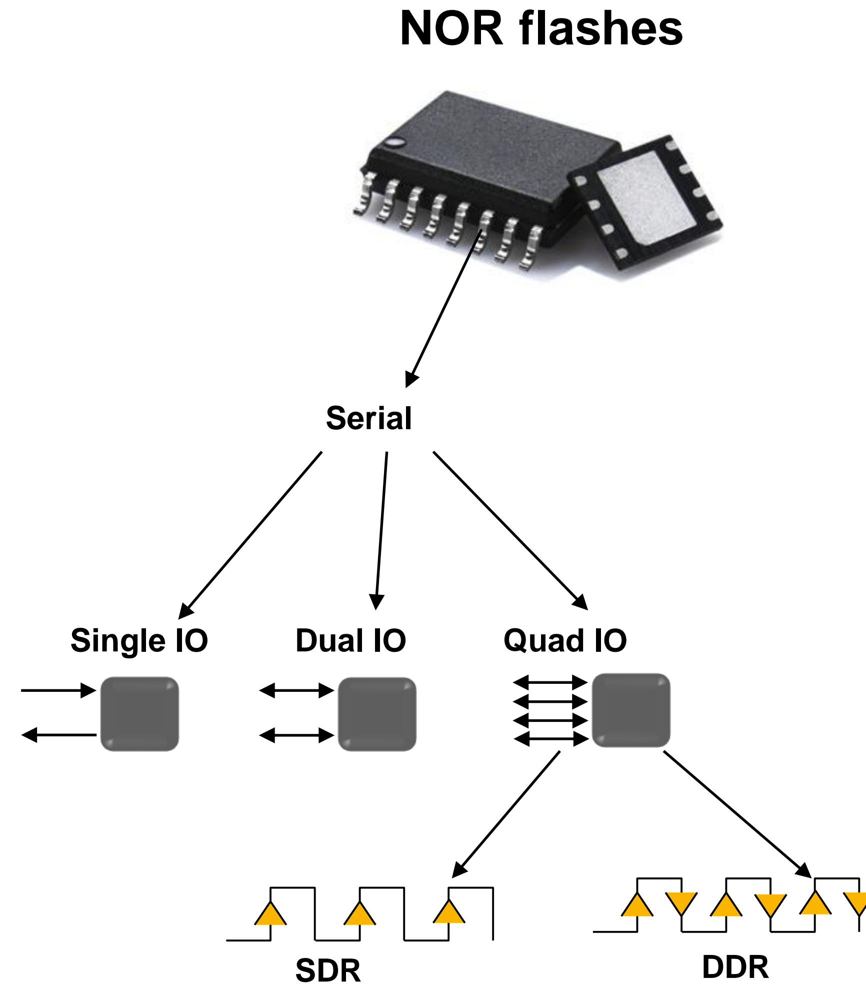
- Two different but related standards supported on same uSDHC module
- Embedded Multi-Media Card (eMMC)
  - 8 data + 3 control pins
  - 3.3V supply with optional 1.8V I/O
  - 52 Mhz clock with DDR and 8-bit interface gives peak 104 MB/s transfer
    - Flash speed will typically limit reads to ~90 MB/s and writes to ~40 MB/s
- Secure Digital (SD) card
  - Derived from MMC spec
  - 4 data + 2 control
  - Support for 1.8V operation (auto-switching)
  - 50 MHz clock with DDR and 4-bit interface gives peak 50 MB/s transfer

SD and eMMC NAND

- Very large memory sizes available
  - Good for mass storage at low cost
- Same disadvantages as other NAND flash technologies
  - Not memory mapped
    - Typically block read and write supported
    - No XiP
  - Bit errors can occur due to read disturb
    - Both SLC and MLC NAND flashes suffer from bit flips
    - ECC is a must for NAND flash

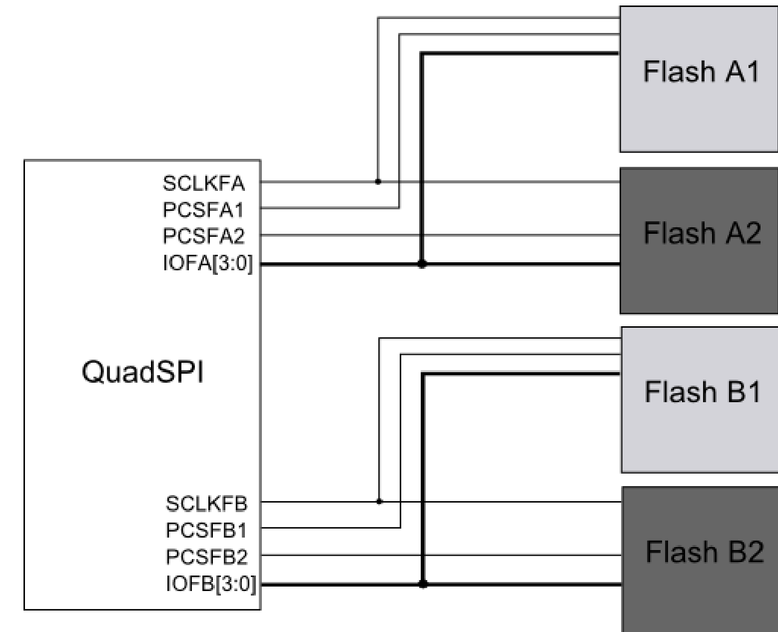
Serial Flashes

- Serial Quad flashes offer multiple advantages over other flash:
  - High bandwidth and low protocol overhead
  - Available in auto qual grade
  - Interface and implementation enables Execute-in-Place (XiP) applications.
  - Available as KGD for SiP (System-in-Package)
  - Available now from multiple vendors
- Stability of NOR over NAND



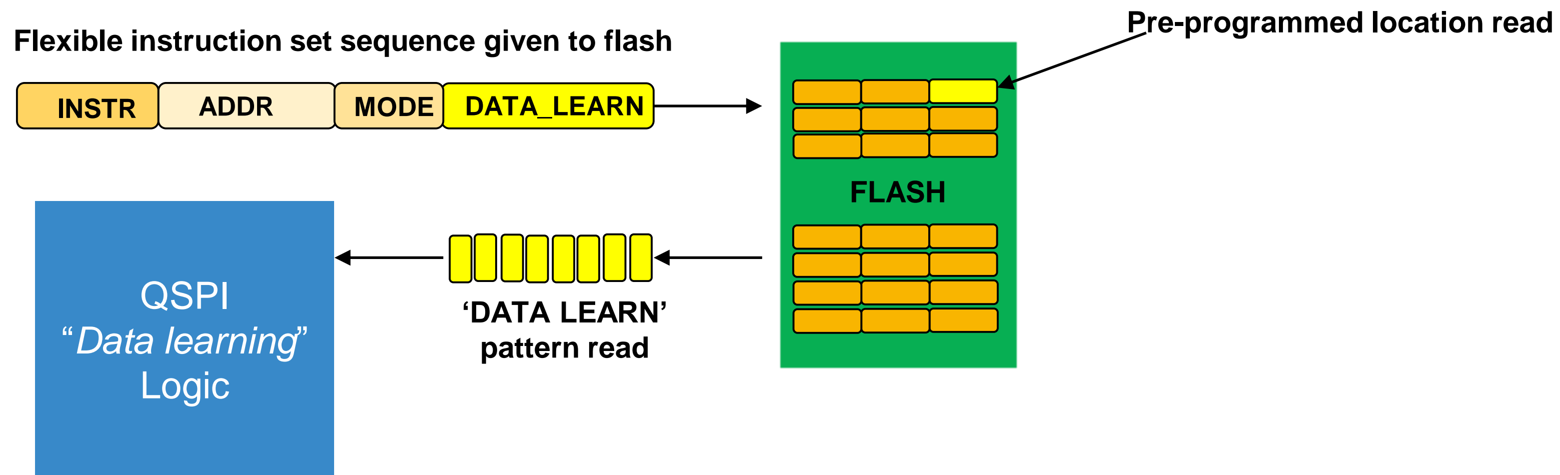
QuadSPI Parallel Access Mode

- This mode allows two identical serial flash devices to be connected and accessed in parallel forming one (virtual) flash memory with doubled readout bandwidth
- Parallel Flash Mode is valid only for commands related to data read from the serial flash
- Configuration:
  - The 1st device of Flash A has to be paired with the 1st device of Flash B
  - The 2nd device of Flash A has to be paired with the 2nd device of Flash B
- The incoming address is divided by 2 and sent to the two flashes connected in parallel



QuadSPI: “Data Learning”

- Only applicable for QuadSPI DDR mode
- Provides a known pattern on the IOs for the controller to self calibrate
- However this is not standardized across vendors
- The QuadSPI controller provides a flexible instruction set that can emulate “Data learning” in any flash memory



QuadSPI

- Enhanced version of SPI
  - Up to 8 data + 2/4 control pins
  - 1.8V/3.3V supply
  - SDR 104 Mhz clock and 8-bit interface gives peak 104 MB/s transfer
  - DDR without learning 50 Mhz clock and 8-bit interface gives peak 100 MB/s transfer
  - DDR with learning 80 Mhz clock and 8-bit interface gives peak 160 MB/s transfer
- Appears as a memory-mapped resource to the CPUs
  - Has dedicated configurable buffers to optimise burst performance

Memory Architecture Design

- As a consequence of the architecture of the device and the memory systems available it is essential to spend time assessing the required configuration for your application
- The EVB can help because it includes all options available
  - But not necessarily with the capacity required
- The uSDHC module is multiplexed onto two ports on S32V234
  - One of these ports is the only port accessible to the QuadSPI
  - The second port is the only one available to VIU1

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Booting Options

- The processor can choose to boot from a number of different sources including serial connections
  - Typically an on-board NVM would be used during production
  - An SD card is most often used during development
- All flash boot sources use the same physical pins on the S32V234 so we need to multiplex between them if we need to have flexibility in booting
  - This means that switching from the boot flash source to another is non-trivial and restrictive

Using Fuses to Select Boot Interface

- Up to 32 fuses are used to select and configure the basic boot interface
  - Further fuses can influence the operation of a particular mode
- These fuses are latched into registers during reset.
- Out of reset, S32V234 runs code stored in the boot ROM which takes care of the interface setup and boot.
  - Warning: the boot ROM can alter modules from reset states

BOOT Modes

- BOOTMOD[1:0] pins are sampled out of reset – after this they can be used in the applications as required
  - BOOTMOD[0] : Muxed with PC9, FTM1 CH0, ENET timer 0, Safe State Engine input 0
  - BOOTMOD[1] : Muxed with PC10, FTM1 CH1, ENET timer 1, SSE input 1

BMODE[1]	BMODE[0]	BT_FUSE_SEL	Boot Type	Intended Use-Case
0	0	0	Serial Download	Production configuration - Virgin device
0	0	1	Boot from Fuses	Production configuration - Programmed device
0	1	X	Serial Download	Debug of programmed device
1	0	0	Boot from RCON	Development configuration
1	0	1	Boot from Fuses	Security loophole closure
1	1	X	Reserved	Reserved

RCONs

- RCON pins are GPIOs which can be used to override fuses only during development. Values are loaded upon reset.
- RCON boot can itself be disabled by fuse. Total of 32 pins mapping directly to BOOTCFG fuses.

PAD Number	RCON	eFuse
MSCR[7]	RCON0	BOOT_CFG1[0]
MSCR[8]	RCON1	BOOT_CFG1[1]
MSCR[9]	RCON2	BOOT_CFG1[2]
MSCR[10]	RCON3	BOOT_CFG1[3]
Etc…….		

- On the EVBs the GPIO pins are isolated during reset

Debugging Boot Behavior

- The boot configuration is latched in the SRC_BMR[1..2] registers
  - If the part isn't booting as expected, check these out.

29.2.2 Boot Mode Register 2 (SRC_BMR2)

Latch Boot Configuration from eFuse or GPIO's on RESET Deassertion

Phase : Phase 3

Secure/Non Secure : Non Secure

Address: 0h base + 4h offset = 4h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0					0	BMOD		0							
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Debugging Boot Behavior

- The boot configuration is latched in the SRC_BMR[1..2] registers
  - If the part isn't booting as expected, check these out.

29.2.1 Boot Mode Register 1 (SRC_BMR1)

Latch Boot Configuration from fuses or GPIOs based on BT_FUSE_SEL fuse on PHASE3 reset deassertion. Reset value is dependent on the values latched.

Phase : Phase 3

Secure/Non Secure : Non Secure

Address: 0h base + 0h offset = 0h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	BOOT_CFG4								BOOT_CFG3								BOOT_CFG2								BOOT_CFG1							
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Debugging Boot Behavior

- If any error occurs during internal boot, the device will be reset.
  - With each reset, a functional reset counter is incremented
  - If the Functional reset counter reaches a threshold value (8), the boot code switches to the Serial Download Mode
    - This allows rapid recovery of a device that has a temporary fault during boot (e.g. noise spike or a soft error) but allows incorrectly programmed boot code to be debugged
- Once the fuses are blown, the boot device is **fixed**
  - The processor can not be made to boot from a different boot device
  - When designing hardware it is helpful to include some form of control over the boot sources and behaviour rather than relying on burning fuses

Boot Process

- Once the boot source is recognised the device is effectively under software control and can
  - Begin executing directly from flash memory
  - Copy code from NVM into DRAM or on-chip RAM and execute from there
    - It is possible to configure the DRAM interface using constant writes before the code copy is done
  - In all cases it can execute the application code on the Cortex M4 or one of the Cortex A53s
- Once code is under application control it can start any other core in the system
- When designing hardware it might be wise to include some form of control over the boot sources and behaviour rather than relying on burning fuses

CAMERA CONNECTIVITY

Connecting Cameras

- Cameras can either be local to the board or remote, encoded (MJPEG/H264) or raw
- Local connection
  - Parallel digital input
    - 2 x VIU inputs at 200 MB/s on each (2 x 16bit input or 1 x 20 bit, 1 x 12 bit)
  - Serial input
    - 2 x 4 lane MIPI CSI2 modules at 1.5 Gb/s on each lane with up to 4 virtual channels per module
- Remote connection
  - Ethernet
    - 1 Gb/s port
  - Serializer input to MIPI-CSI2

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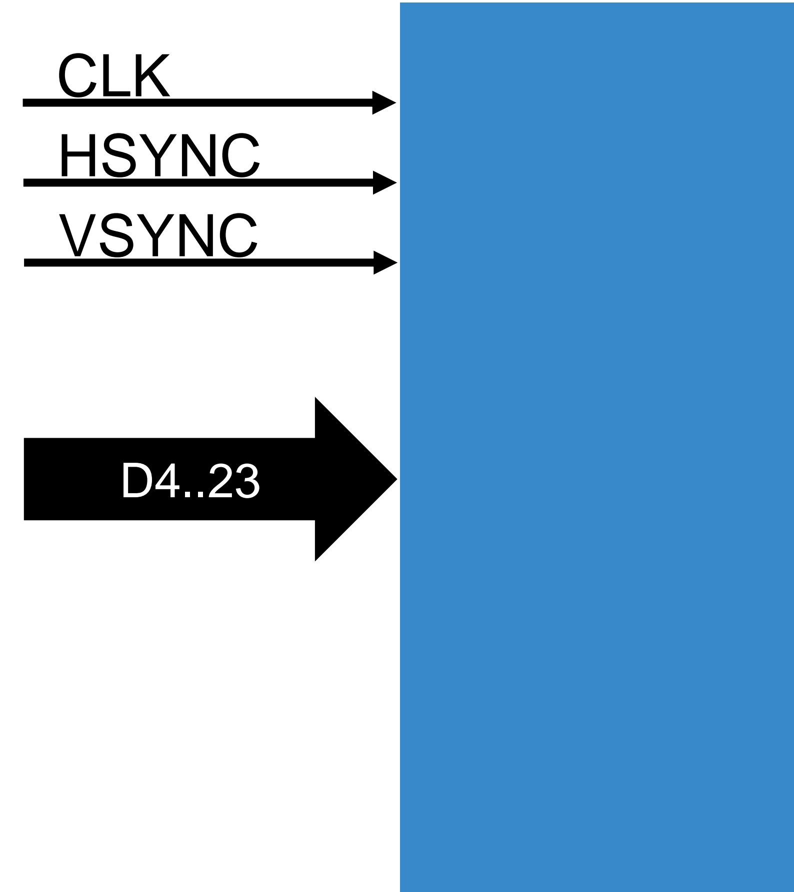
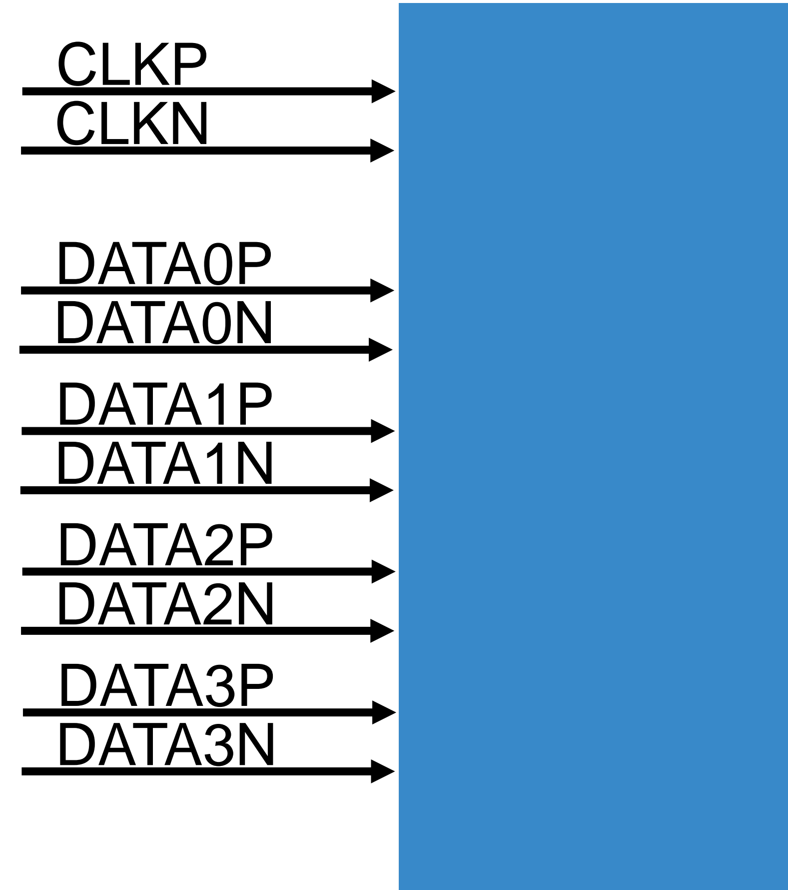
Video Interface Unit (VIULite)

- The Video Interface Unit (VIULite) allows capture of digital video
- ITU656 (YUV422) or RAW input
- Incoming video is stored in RAM
- De-interlacing is possible by adjusting RAM storage format
- ITU656 format (de-interlacing under software control)
- Digital 100 MHz clock and parallel signals required with associated connection and EMC concerns



MIPICSI2

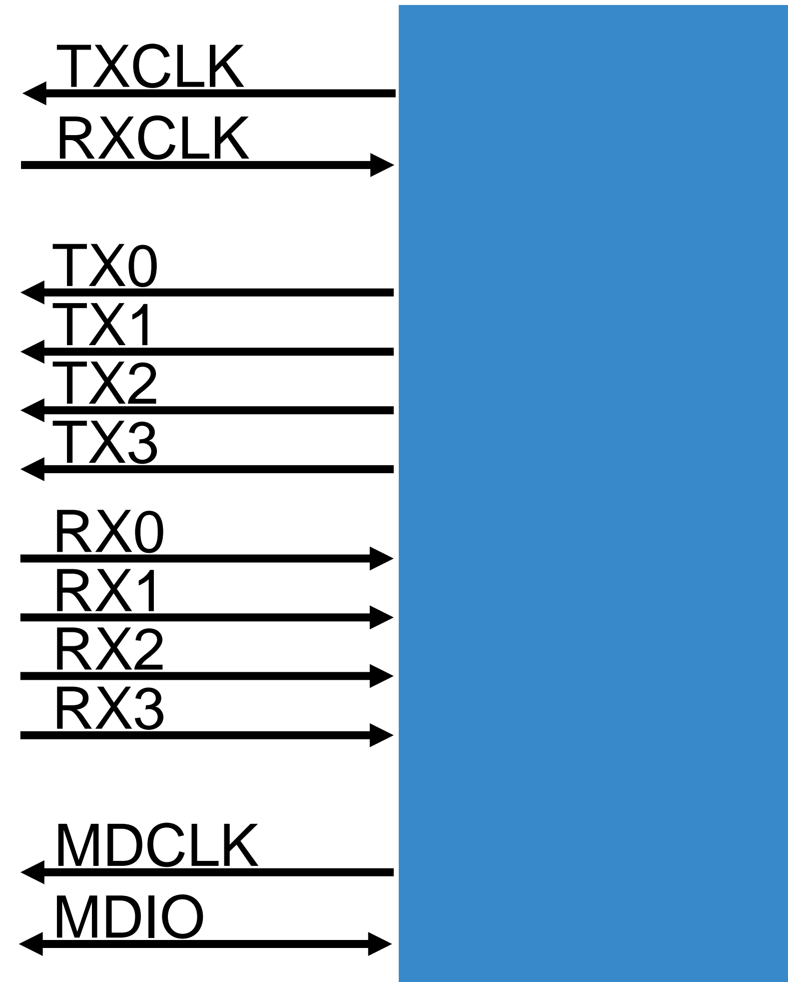
- Compliant to MIPI Alliance D-PHY Specification and MIPI Alliance CSI-2 Specification, v01-01-00 by MIPI® Alliance
- Input side data types: RGB888, RGB565, YUV422 8- and 10-bit, RAW8, RAW10, RAW12, RAW14, user defined, and embedded
- Independent data queues (SRAM Buffers) for the four virtual channels
- 1.5 GHz differential channels



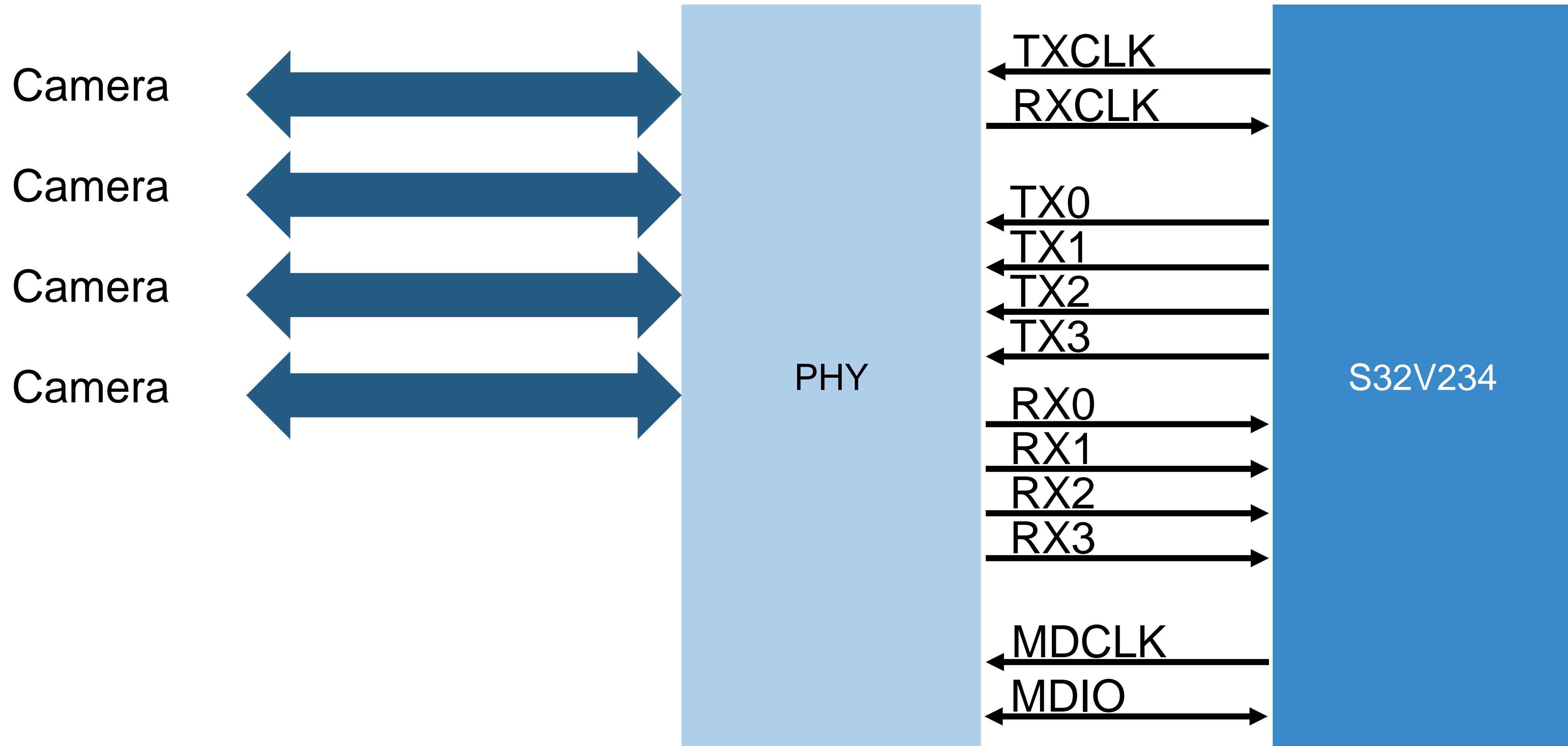
Gigabit Ethernet Controller with AVB

- 10/100/1000 Mbit/s full duplex operation
- Interfaces to Ethernet PHY devices via:
  - a 4-bit MII operating at 25 MHz, or
  - a 2-bit RMII operating at 50 MHz, or
  - a 4-bit RGMII operating at 125 MHz.
- MDIO master interface for PHY device configuration and management with two programmable MDIO base addresses

- For multiple camera connectivity an external switch is required



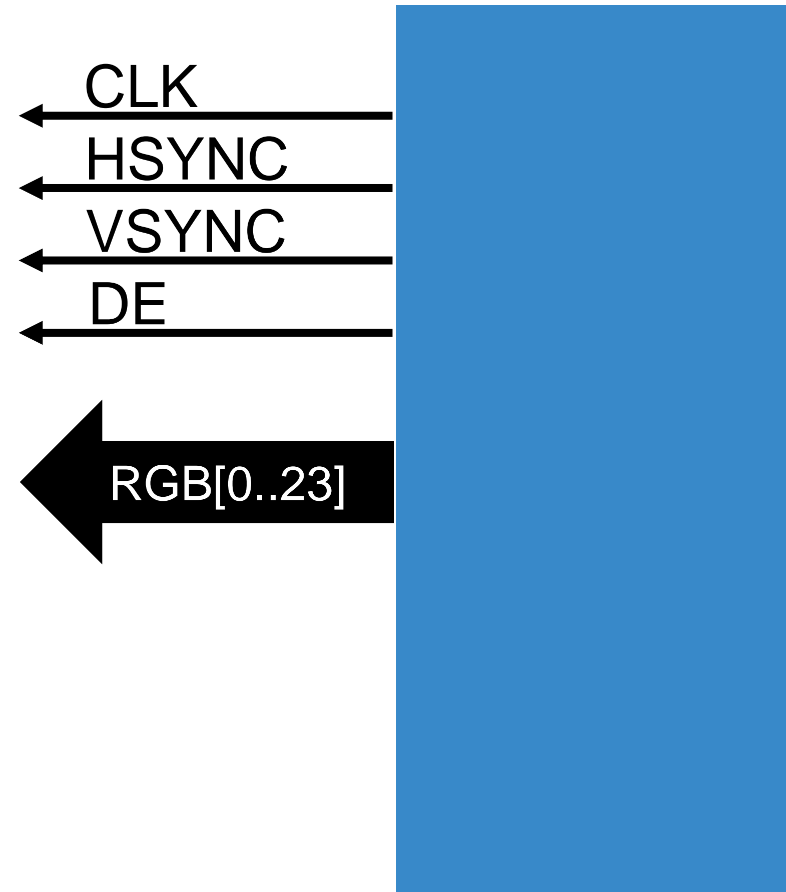
Camera Connectivity



DISPLAY CONNECTIVITY

2D-ACE

- The 2D-ACE is an advanced graphics compositing and blending engine that directly drives an external TFT LCD
  - Allows full flexibility of TFT display sizes
  - Fetches and blends bit-mapped "sprites" from on- or off-chip memory using DMA
  - Up to 156 MHz clock and 24 bit data
    - e.g. 1280 x 1024
  - Direct connection to display or via a codec to HDMI/DVI/LVDS



COMMUNICATIONS INTERFACES

Standard Communications Modules

- Ethernet
- FlexRay™
- FlexCAN FD
- ZIPwire
- SPI
- I2C
- LIN / UART

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POWER SUPPLY DESIGN

Power Supplies

- There are 250 power supply balls on the 528 pin package
  - GPIO0 for 3.3 V
  - Eight general I/O supply banks that can operate at 1.8 V - 3.3 V
    - VDD_GPIO1, VDD_GPIO2, VDD_HV_IO_ETH (possibly 2.5 V), VDD_HV_IO_VIU0, VDD_HV_IO_VIU1, VDD_HV_IO_DIS, VDD_HV_IO_FLA
    - Independently of each other
  - Core domain supply of 1.0 V
  - 1.8 V and 1.0 V supplies for MIPI CSI2 interfaces
  - 1.8 V supplies for various analog circuits
  - 1.0 V supply for PLLs
  - 1.8 V supply and reference for SAR ADC
  - 1.2 V – 1.5 V supply for DRAM I/O pins

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Power Supply Structure Suggestion

Input Supply

5V to 1V Buck2

5V to 3.3V Buck1

> 5W Core Use Case

5W Core Use Case

SW1ABC 0.3 to 1.875V 4.5A Buck

SW1AB 0.3 to 1.875V 2.75A Buck

SW3AB 0.4 to 3.3V 2.5A Buck

SW2 2.5V 1.25A Buck

SW4 0.4 to 3.3V 1A Buck

SW3 0.9 to 1.65V 1.5A Buck

SW2 0.4 to 3.3V 2.5A Buck

VREFDDR 10mA

VREFDDR 10mA

PF3000

PF0100

0.6V/0.75V

VCORE

1.8V

2.5V

LPDDR2 / 1.2V

3.3V

Power Supply Sequencing

- While designing the system, it is important to take care of following constraints:
  - PCIE_VP and PCIE_VPH supplies should be powered up within 50 ms of each other.
  - VDD_HV_CSI and VDD_LV_CSI should be powered up together on board to prevent any electrical crossover currents.
  - VREFH_ADC should never be more than 100 mV above VDD_HV_ADV.
  - DDR0_VREF0 and DDR1_VREF0 supplies are expected to be 0.5 of VDD_HV_DDR0 and VDD_HV_DDR1 I/O supplies and are to track VDD_HV_DDR0 and VDD_HV_DDR1 supply variations as measured at the receiver. Peak-to-Peak noise on DDR0_VREF0 and DDR1_VREF0 supplies should be between +/- 15 mV.
- All power supply pins must be connected

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MULTIPLEXING AND CONFIGURABLE SUPPLIES

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Multiplexing and I/O Voltage

- The I/O pins are heavily multiplexed which allows selection of functions in several places on the package
  - In addition the different I/O voltage banks allow operation of many of these modules at different voltages

- Take care that the module selection is compatible from a function point of view as well as a voltage setting

Port	Function	I/O Power Domai
	RXD	
PA12	GPIO[12]	VDD_GPIO0
	TXD	
	CH3	
	RCON4	
	CH3	
	EIRQ[12]	
PA13	GPIO[13]	VDD_GPIO2
	CH2	
	CS3	
	RCON5	
	CH2	
	EIRQ[13]	
	RXD	
PA14	GPIO[14]	VDD_GPIO2
	TXD	
	CH3	
	CS1	
	RCON6	
	CH3	
	EIRQ[14]	
PA15	GPIO[15]	VDD_GPIO0
	DATA	

GPIO Settings

- The GPIO pads can be configured to match the function of the peripheral and the board routing
  - Standard input and output functions
  - Pull up and down
  - Drive strength/impedance
    - 240 Ohm, 120 Ohm, 80 Ohm, 60 Ohm, 48 Ohm, 40 Ohm, 34 Ohm

- Consider matching the pad setting with the hardware connection

Data Sheet Recommendations

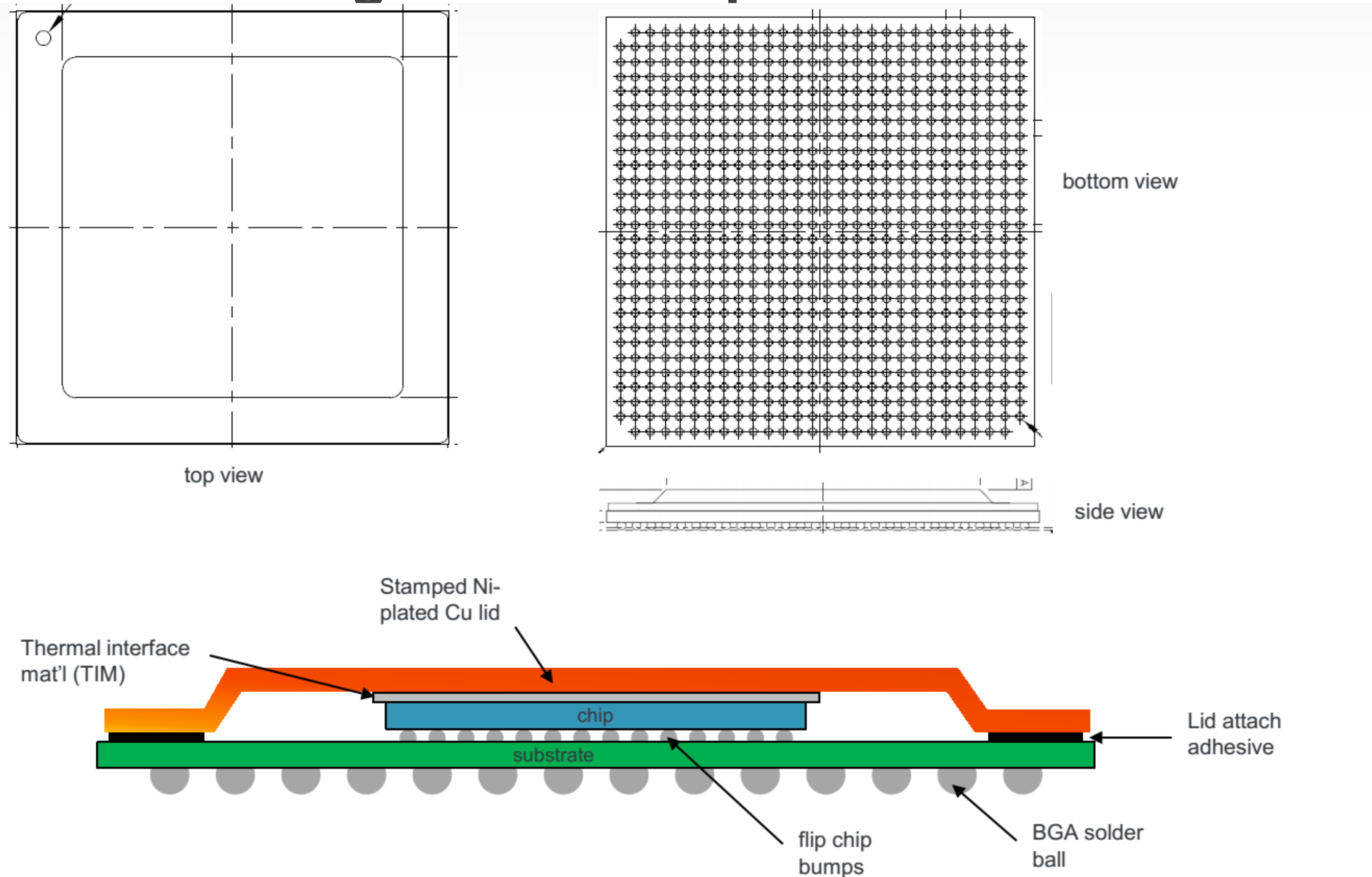
- The data sheet makes certain recommendations for some modules
  - QuadSPI
    - Put 22 ohm series termination on board when operating with DSE <2:0> 111
  - TRACE
    - Put 22 ohm series termination on board when operating with DSE <2:0> 111
  - ENET
    - Put 22 ohm series termination on board when operating with DSE <2:0> 111

PACKAGE CONSIDERATIONS

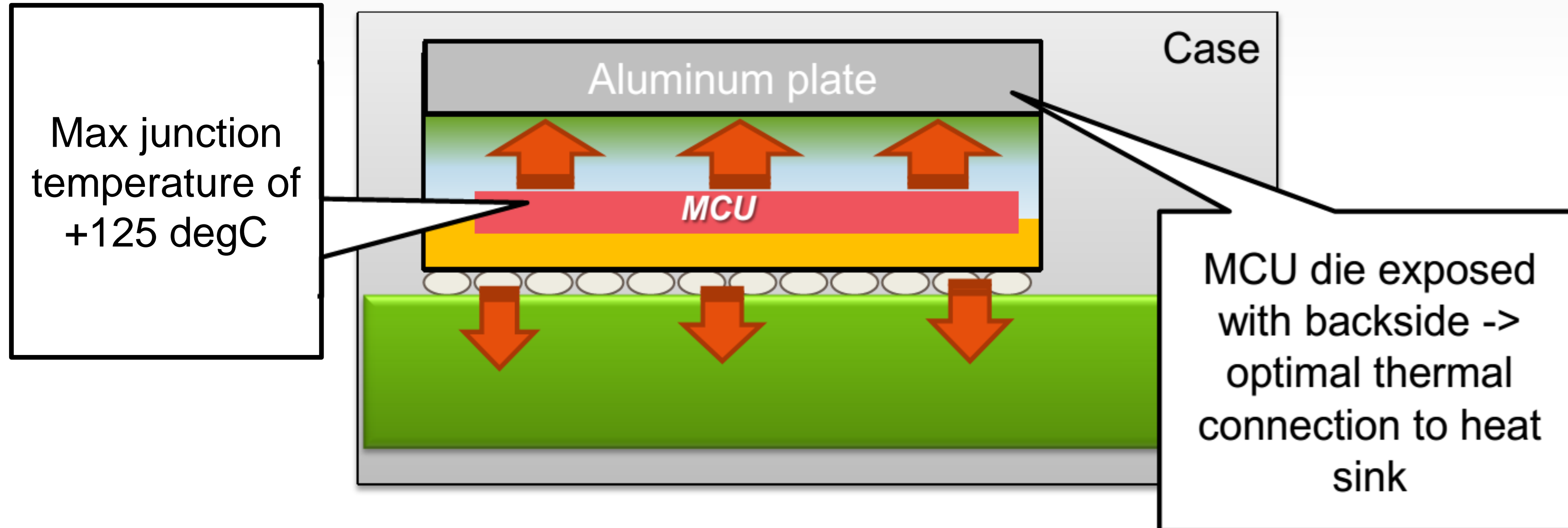
Package and Power Dissipation

- Device dissipation is highly dependent on the application use case
- Package is designed to allow maximum dissipation of heat
  - c. 8°C improvement against a plastic package on a 4 layer board
- Power dissipation values are still under investigation for typical use cases
  - Simulated values range from 2 W to 8 W

Flip Chip BGA Package With Stamped Lid



Quad Package Will Require Thermal Assessment



Simulation setup:

- Package: 621 17x17 mm FC-BGA, 0.65P
- PCB: e.g. 8-layer (2-4-2), 250x100x1.5mm
- Max Board Temp: ?°C
- Max Ambient Temp: ?°C
- Heat sink: e.g. 20x20mm aluminum plate or connection via thermal interface material to aluminum case

Summary

- Agree memory requirements
  - Select boot source
    - NAND or NOR flash
  - Choose memory type, number and size
- Choose camera connectivity approach
- Connect display as required
- Design power supply and heat dissipation approach based on application needs

SECURE CONNECTIONS
FOR A SMARTER WORLD

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