

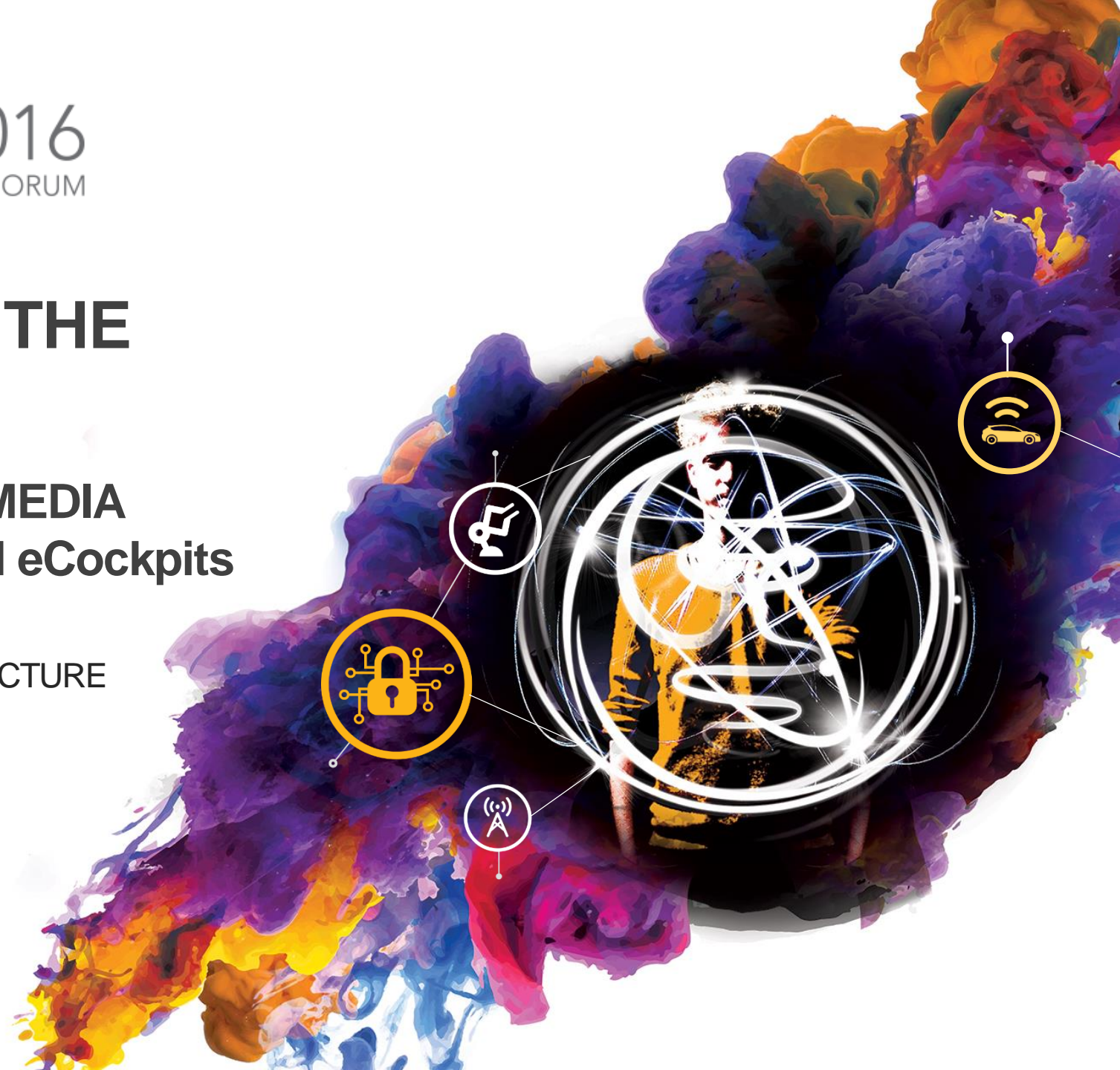


FTF 2016
TECHNOLOGY FORUM

DESIGN THE CAR OF THE FUTURE

i.MX 8 VIRTUALIZATION AND MEDIA CAPABILITIES FOR NEXT GEN eCockpits

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MAY 16, 2016



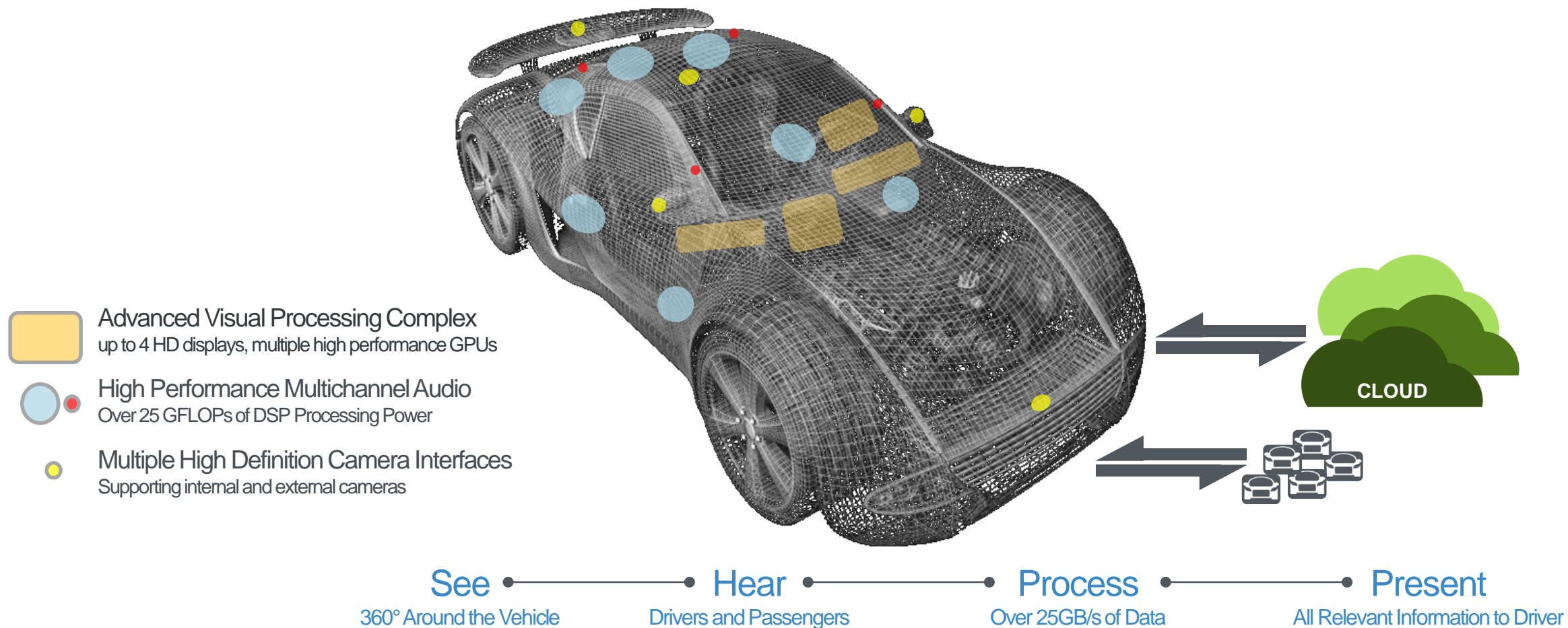
AGENDA

- What is eCockpit?
- Considerations When Building an eCockpit
- eCockpit using the i.MX 8QuadMax



i.MX 8 Family for Model Year 2020

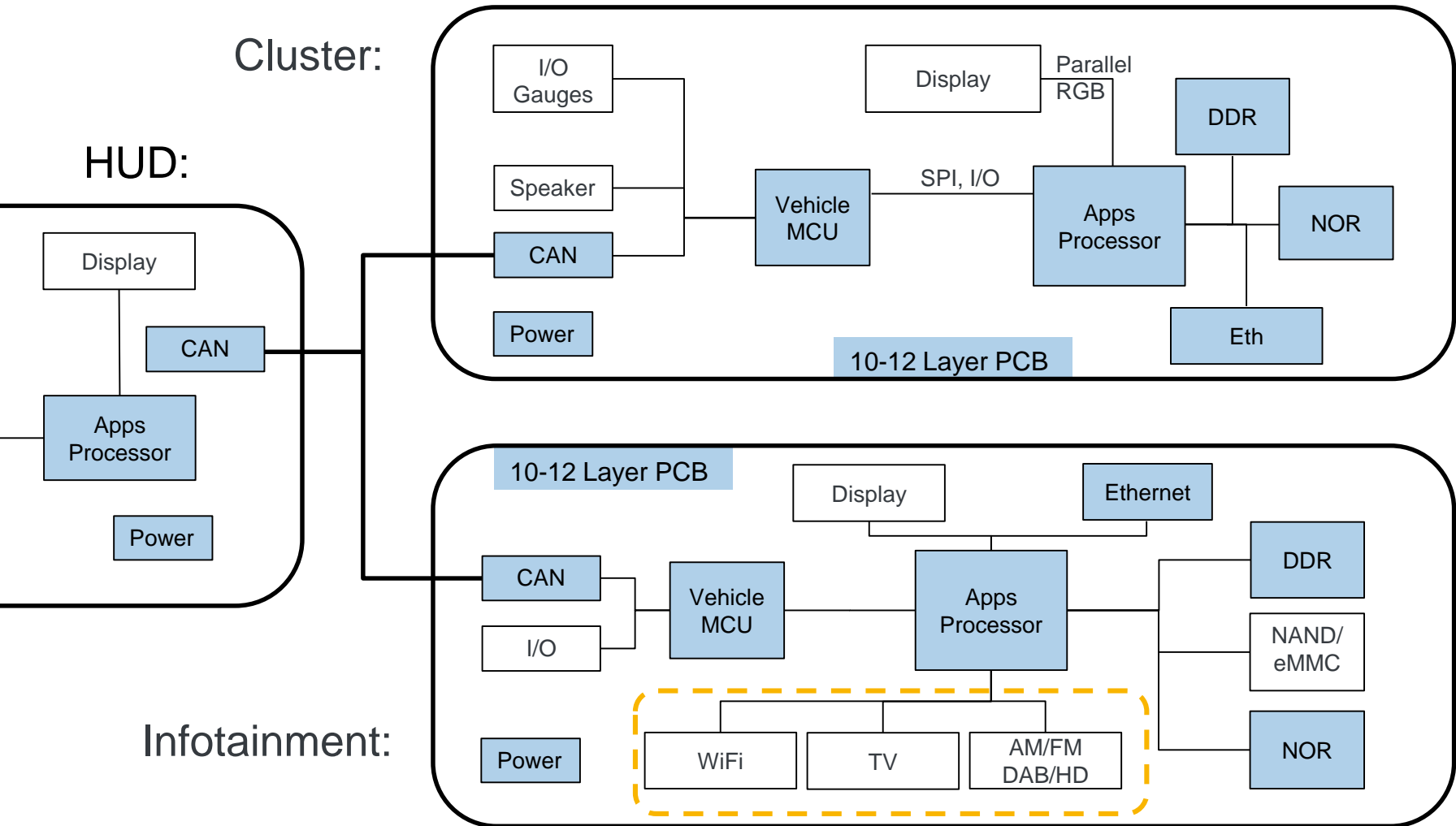
Next Generation Multimedia Processing Complex



WHAT IS eCockpit?



Before eCockpit... Function Duplication over Multiple Platforms

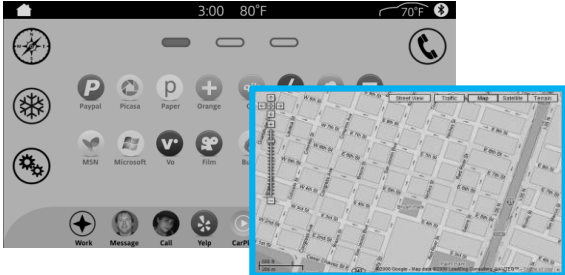


Duplicated:
ECU housing and design NRE
10 layer cluster PCB
5-6 power supplies / circuit protection
Applications Processor & Software
256MB DDR / 128MB NOR
Cluster VMCU + ASIL B OS
Speaker
CAN Tx/Rx and harness
Debug ports and hardware
Discrete components and connectors




eCockpit: Simplification and Efficiency

Single source for all graphics and display processing



Info Display + Media



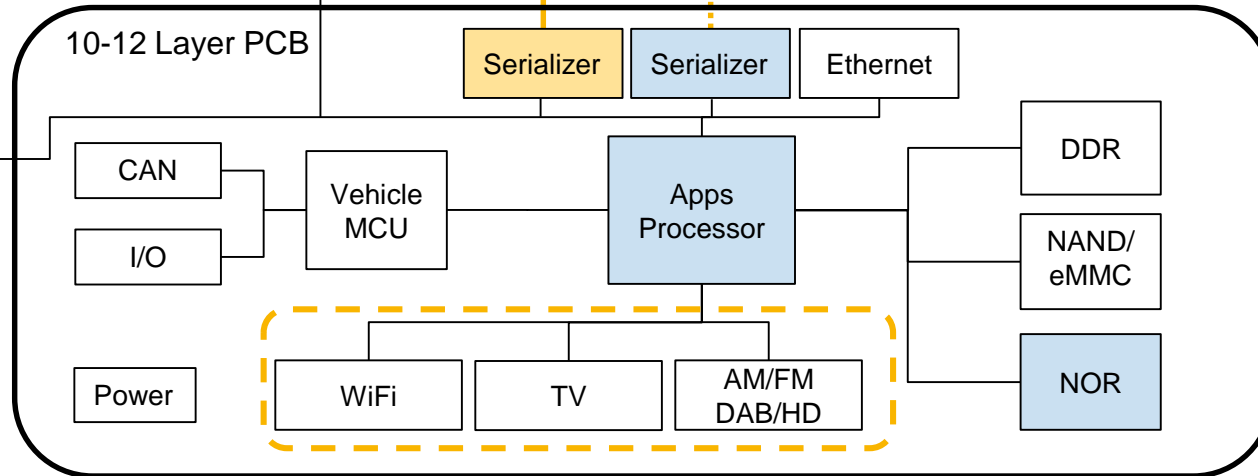
De-serializer
Cluster Display



De-serializer
HUD



RSE

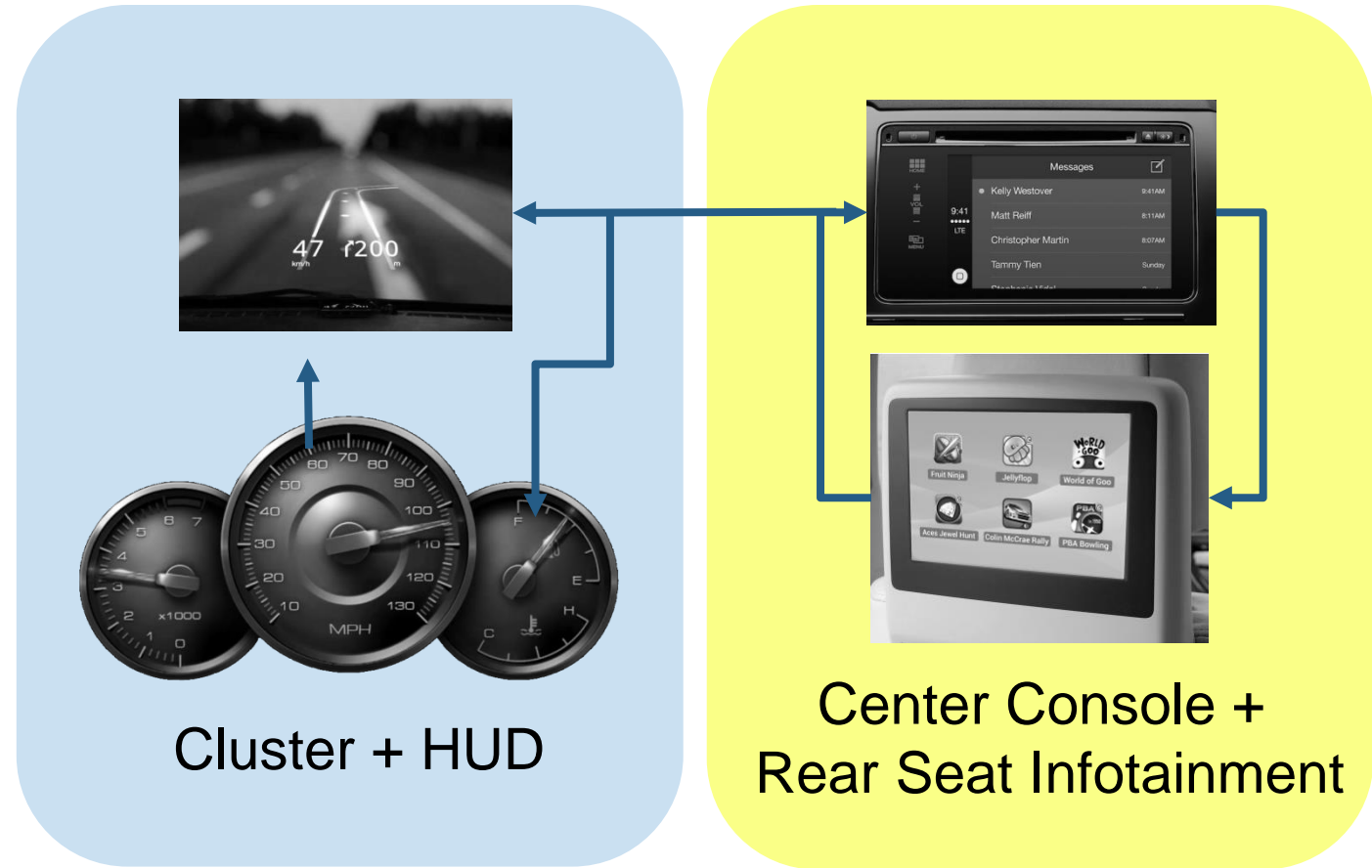


Additional eCockpit ECU requirements:

- Advanced Applications Processor (Delta from Infotainment SoC)
- ASIL B ARM Hypervisor
- Additional DDR / Additional program NVM
- Cluster plus optional HUD LVDS Serializers
- Cluster plus optional HUD Deserializers

Four Displays, Two Systems, One SoC...

- All car and media functionality combined in a single SoC to reduce BOM cost
- Capable of seamlessly integrating all appropriate information and control between driver and passenger functions



What are the Two Main Systems?

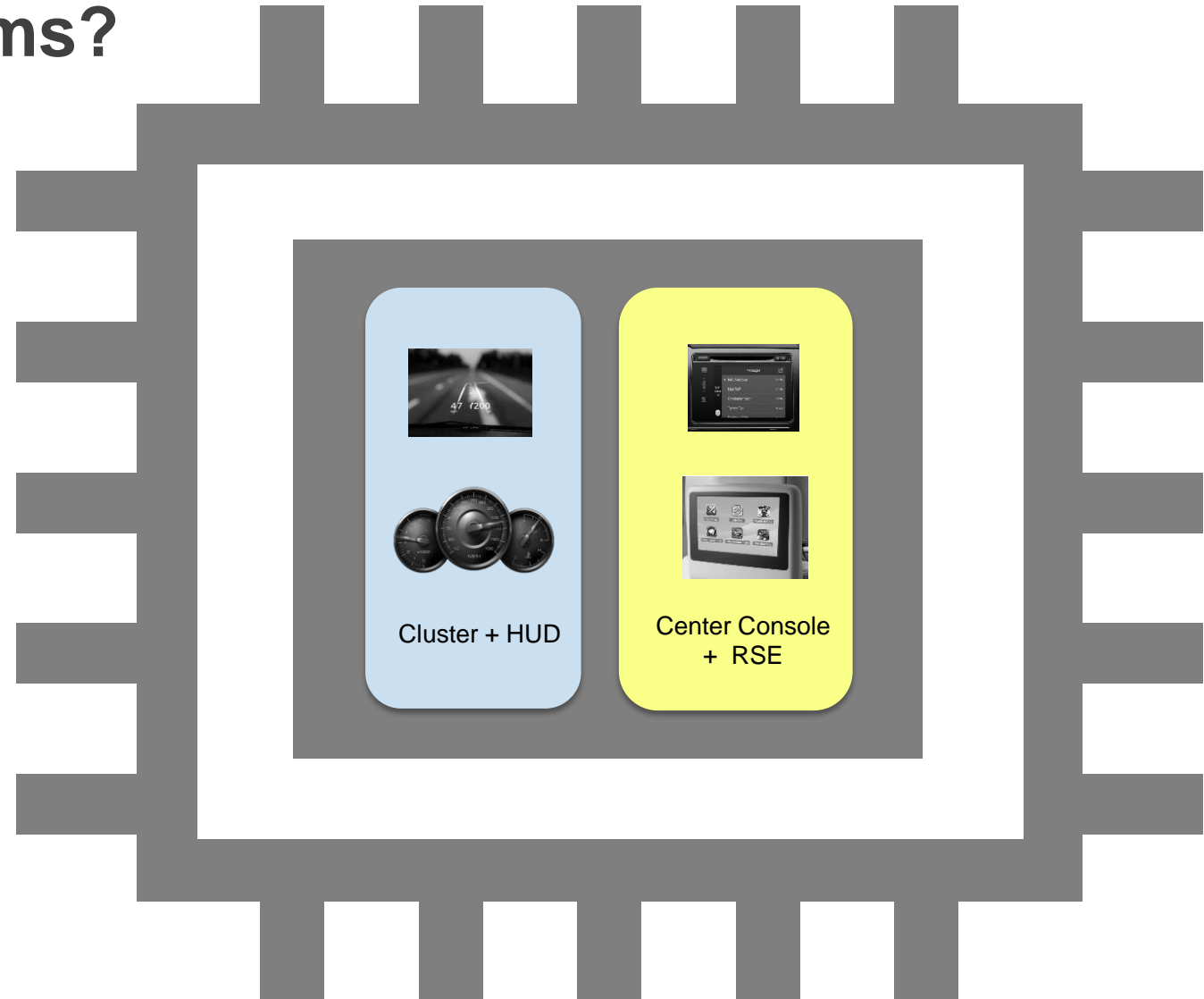
Two systems on the same silicon:

- **Cluster / HUD**

- Hardened Automotive Grade OS:
Inform the driver of car status and driving conditions

- **Center Console / RSE**

- Android or other Consumer OS:
Provide a fun and connected experience for all passengers



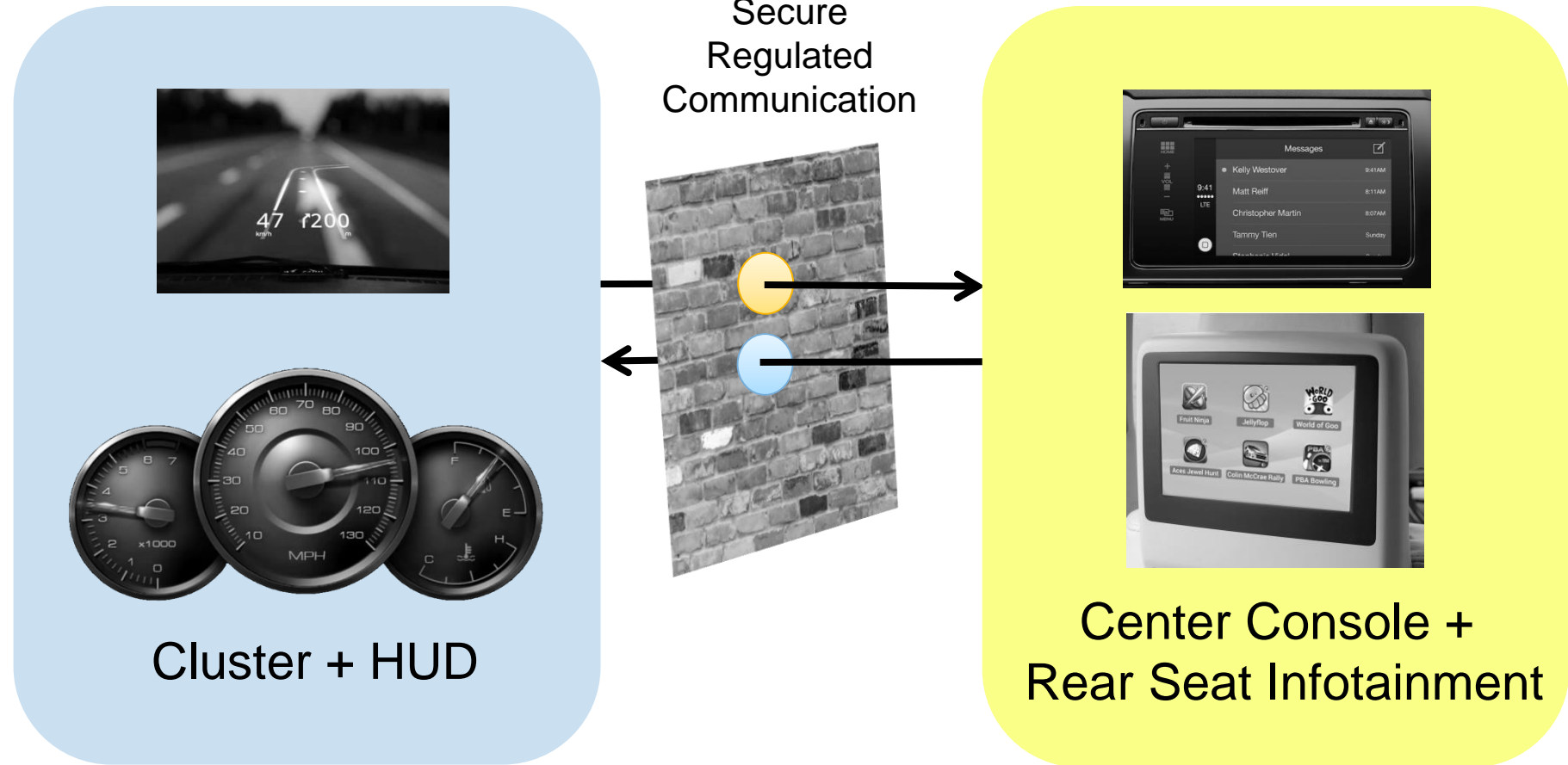
What Else Does eCockpit Contain?

- Granular Power / Wakeup Control of over 40 subsystems on the SoC
- The latest and greatest in 2D / 3D graphics capabilities to enable OpenGL Next and Vulkan
- Full Camera Capabilities to bring in Surround View / Rear (side) Mirrors
- Complete Audio DSP Complex to handle Media, Voice Control, Echo Cancellation, and Connectivity
- Vision Processing Acceleration for use cases like: Object Detection, Gesture, Image Signal Processing, and Stitching
- Quick and flexible boot strategies on A-cores or M-cores with HAB, Trust-zone.
- Video Processor for Multi-stream encode / decode, HEVC (d), h.264 (d/e), and legacy (d)

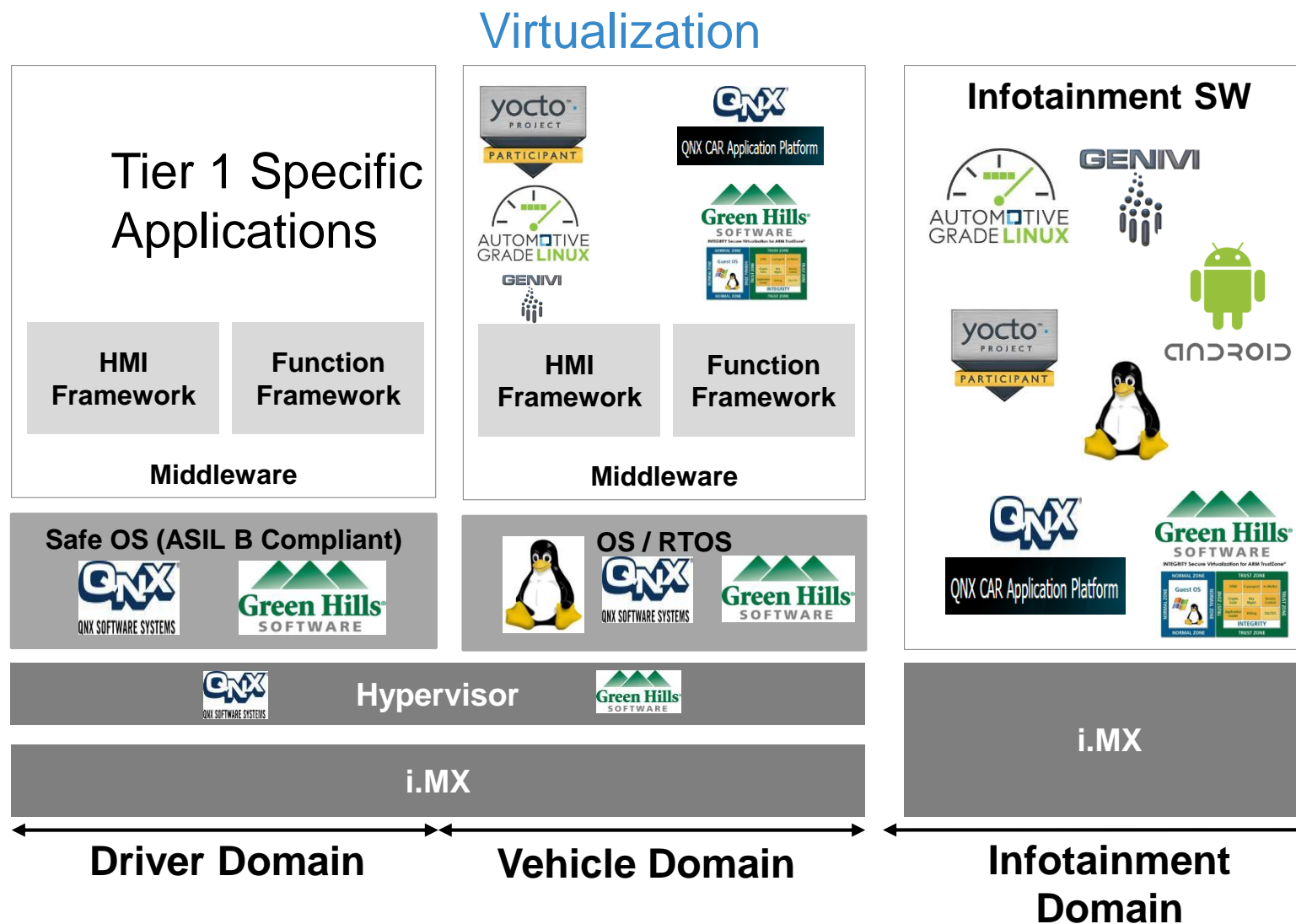
CONSIDERATIONS WHEN BUILDING AN eCockpit

What Issues Arise from eCockpit?

- System critical functionality should not be affected by entertainment functionality
- Quality of Service and Security are required for both systems
- Communication between systems should be limited and secure



How Do We Drive Multiple Systems Safely?



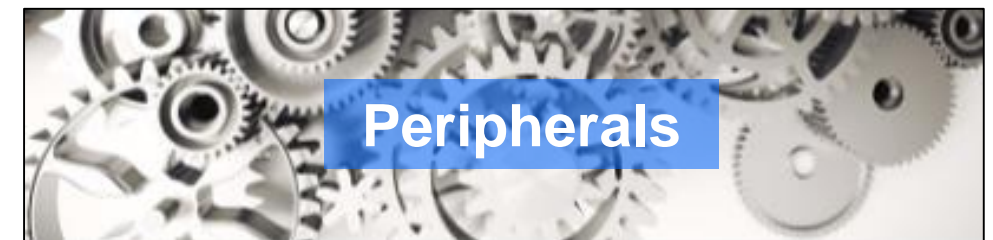
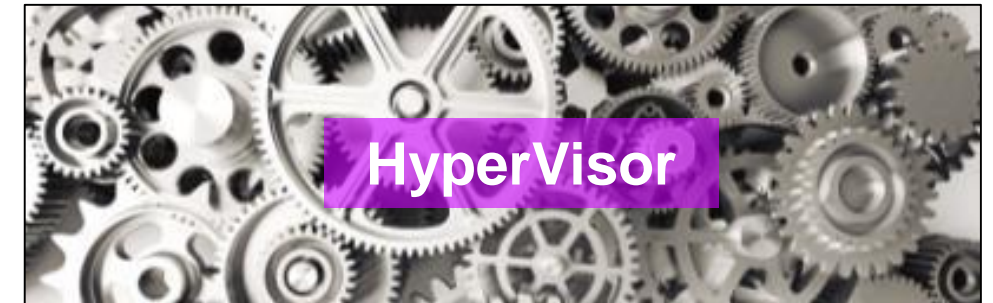
i.MX 8 Virtualization Partners

Multiple partners are supporting a wide variety of virtualization solutions on i.MX
Virtualization solutions are application-specific and vary depending on provider



What Problems Can Arise from Virtualization?

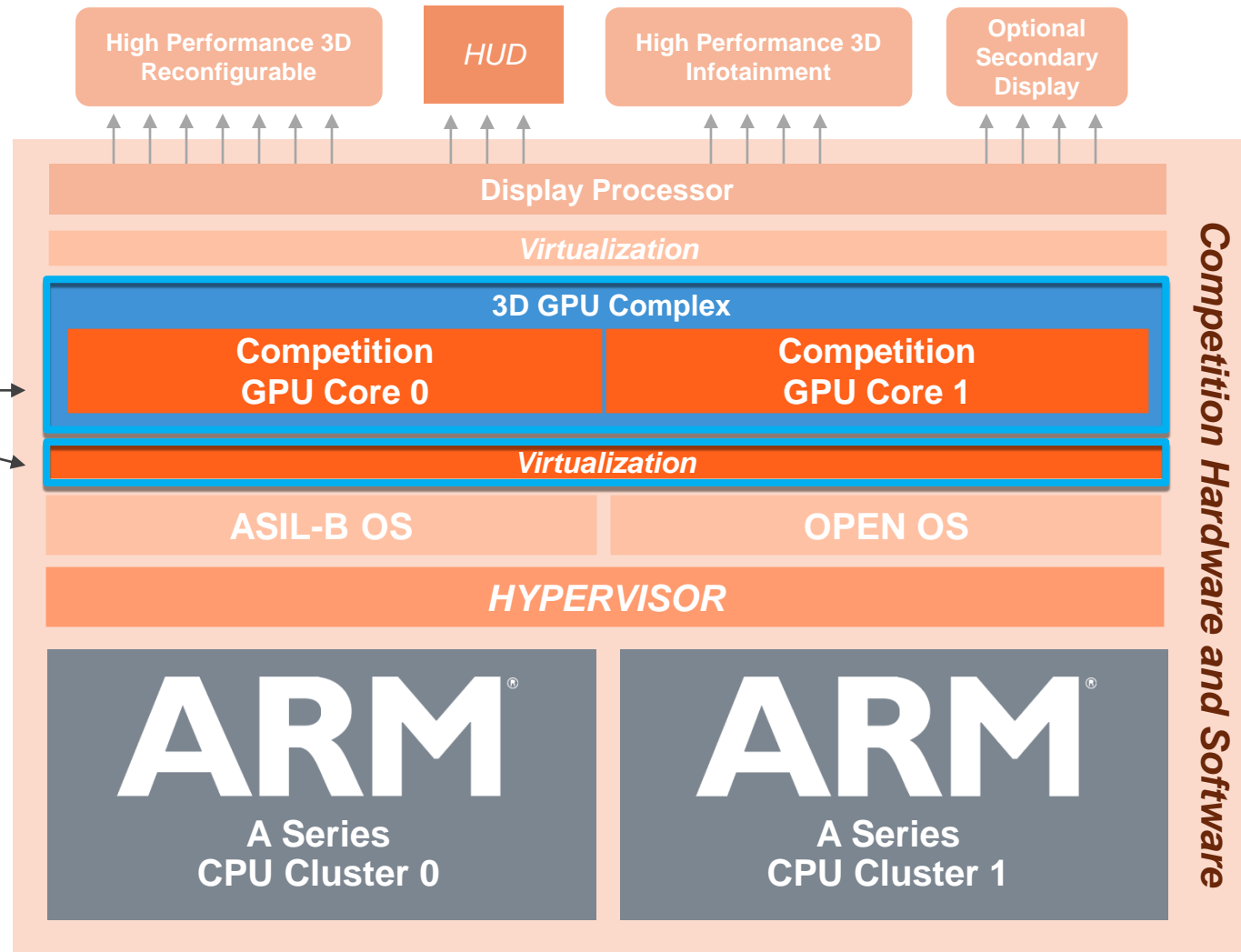
- Virtualization has many layers of abstraction to provide resource sharing and security
- Pure virtualization requires invasive code changes to reduce performance impact
- Each layer of abstraction can introduce new bugs
- Peripherals may require para-virtualized drivers which increases system software complexity



eCockpit on a Monolithic SoC: Graphics

Disadvantages

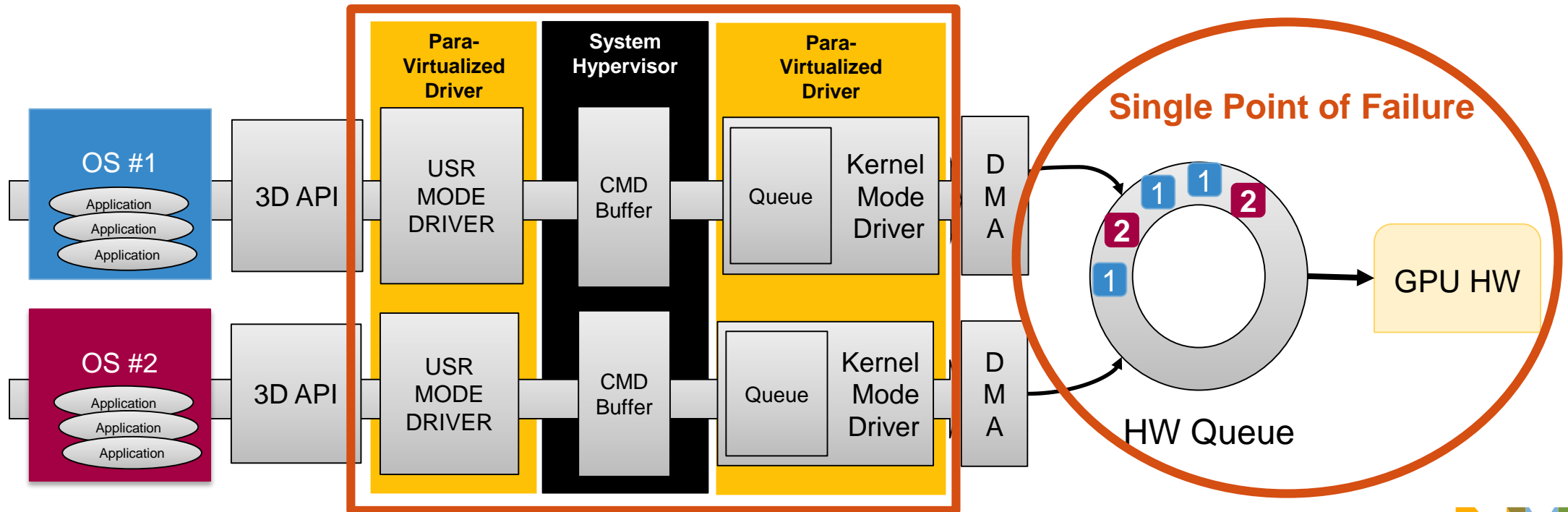
- 1) GPU “Cores” can not work independent from one another – complicated GPU virtualization is required



Para-virtualization of Graphics for Multiple OS

- Multiple Operating Systems can make use of a single graphics by making hyper-calls to a hypervisor to schedule jobs and resources using a command buffer queue.
- Both the User mode and Kernel Mode drivers require special modifications to reduce the overhead of context switching by a hypervisor.

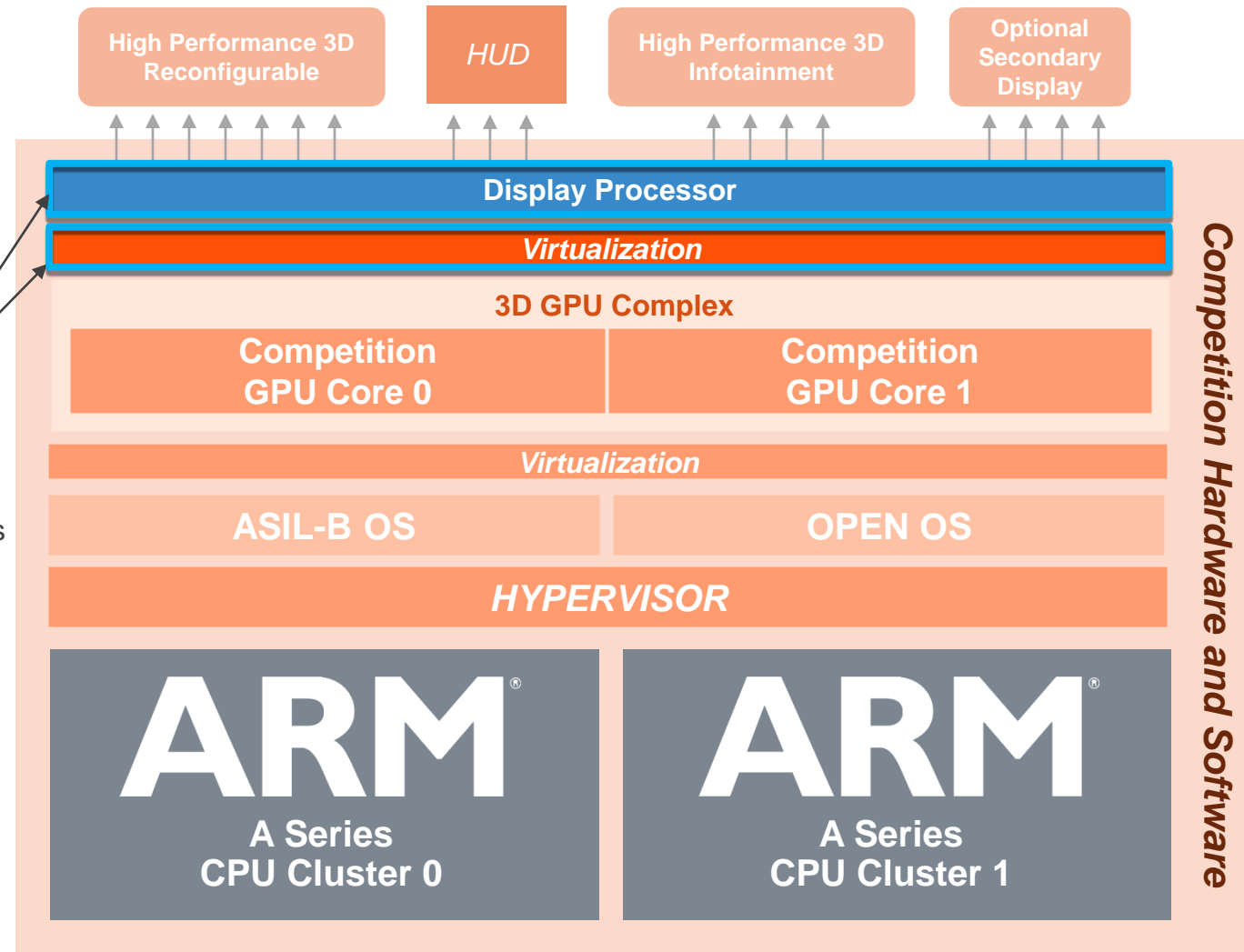
Complicated and Divergent Peripheral Drivers



eCockpit on a Monolithic SoC: Display

Disadvantages

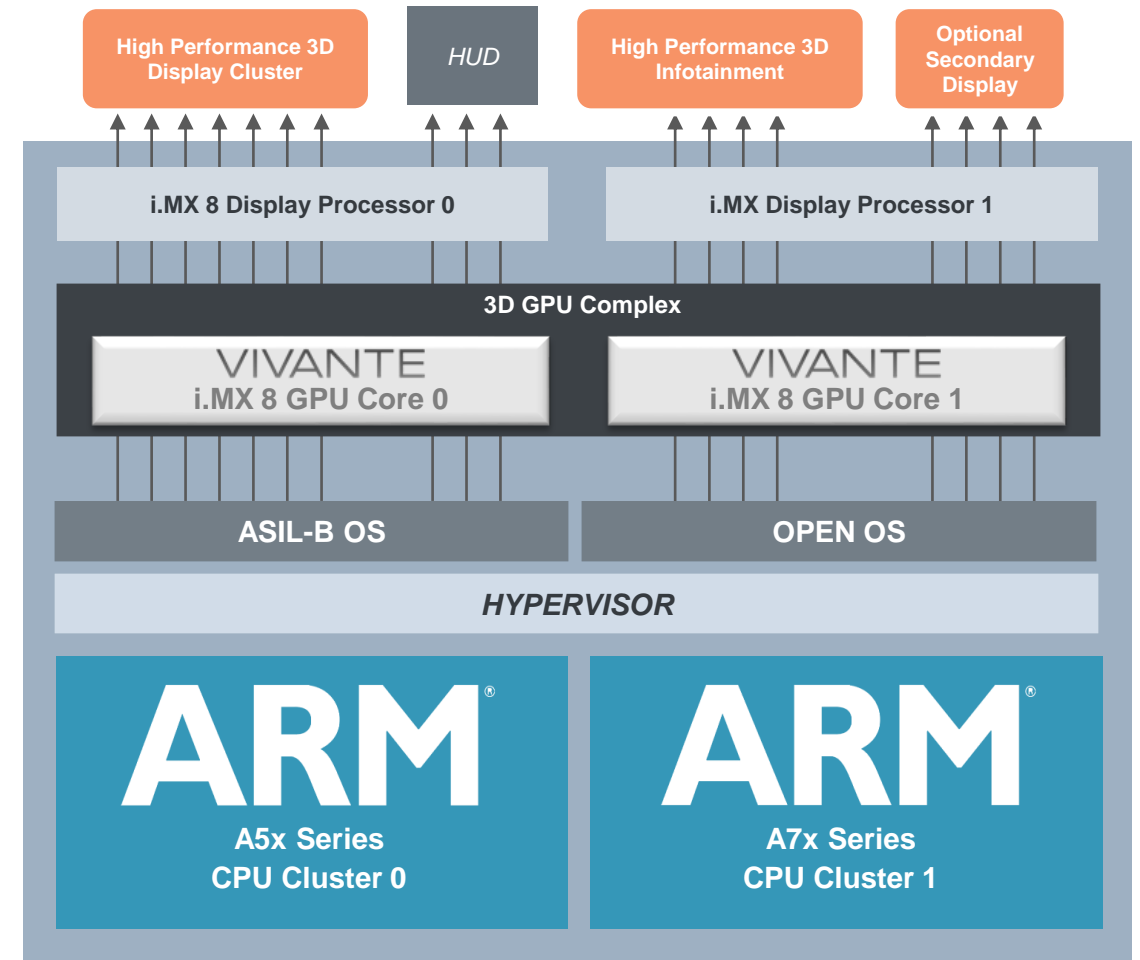
- 1) GPU “Cores” can not work independent from one another – complicated GPU virtualization is required
- 2) Display Processor is a single peripheral driving multiple displays – more complicated virtualization is required to share it between ASIL-B and Open operating systems



i.MX 8QuadMax eCockpit Strategy

Advantages

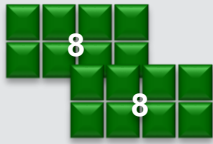


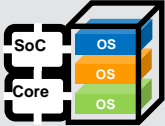




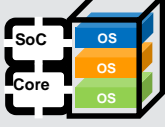




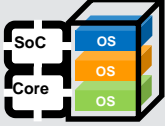



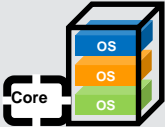



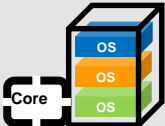

- Dual independent display controllers
- Configurable GPU cores
 - Single monolithic GPU
 - Dual independent GPUs
- Industry standard ARM enablement
- SoC level virtualization



i.MX8 FAMILY OVERVIEW



i.MX 8 Family of Application Processors

	GPU	Display	DSP	Virtualization	ARM CPU
eCockpit Class	8QuadMax  <ul style="list-style-type: none"> Dual Core GPU 16 Vec4 Shaders Up to 128 GFLOPS 64 execution units Tessellation / Geometry Shaders 	Up to 4 displays 	Audio DSP 	SoC Level 	Cortex-M4 Cortex-A53 Cortex-A72 
	8QuadPlus  <ul style="list-style-type: none"> Dual Core GPU 8 Vec4 Shaders Up to 64 GFLOPS 32 execution units Tessellation/Geometry Shaders 	Up to 4 displays 	Audio DSP 	SoC Level 	
	8Quad  <ul style="list-style-type: none"> Dual Core GPU 8 Vec4 Shaders Up to 64 GFLOPS 32 execution units Tessellation/Geometry Shaders 	Up to 4 displays 	Audio DSP 	SoC Level 	
	8Dual  <ul style="list-style-type: none"> Single Core GPU 8 Vec4 Shaders Up to 64 GFLOPS 32 execution units Tessellation/Geometry Shaders 	Up to 2 displays 2x 1080p total pixels 		CPU Level 	
	8DualLite  <ul style="list-style-type: none"> Single Core GPU 4 Vec4 Shaders Up to 32 GFLOPS 16 execution units Tessellation/Geometry Shaders 	Up to 2 displays 2x 1080p total pixels 		CPU Level 	



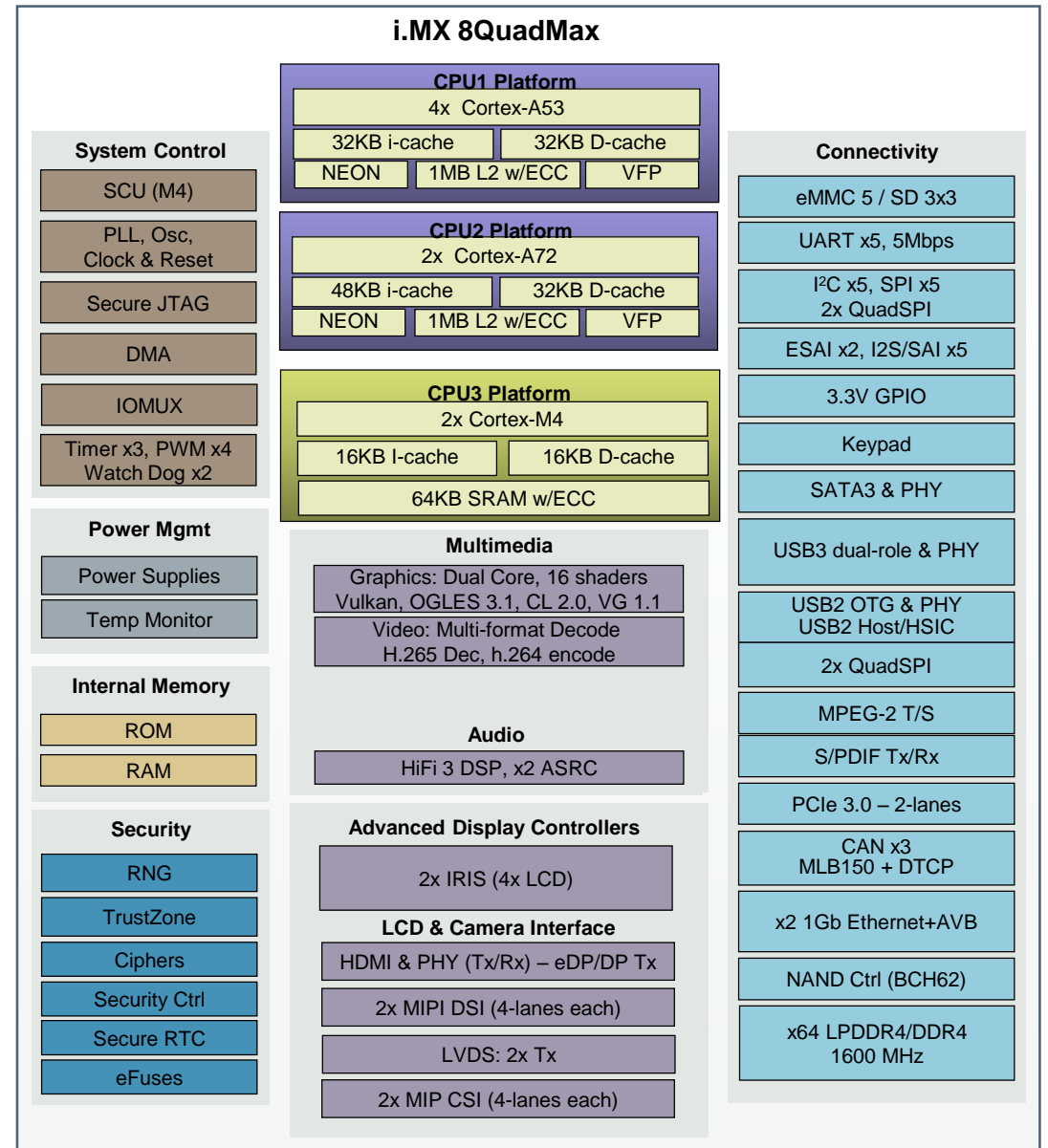
i.MX 8QuadMax Block Diagram

• Specifications

- Dual Complex Core System:
 - Complex 1: 4x Cortex A53 @ 1.0 GHz
 - Complex 2: 2x Cortex A72 @ 1.5 GHz
 - 2x Cortex M4 @ 266 MHz
 - 1x HiFi3 DSP @ 500MHz
- Package: Flip-chip BGA – 0.75mm pitch

• Feature Highlights*

- Multi-core Cortex-A53 & Cortex A72
 - ARM v8 64-bit instruction capability; Fully 32-bit capable
 - Integrated hardware virtualization capabilities
- 16 -Shader 3D (Vec4)
 - 16x Vec4 Shaders, 64 execution units
- 4k H.265 decode & 1080p h.264 enc/dec capable VPU
- Enhanced Vision Capabilities (via GPU)
- USB3.0 with PHY, 2x USB2.0 OTG
- 2x Cortex-M4 for advanced system control
- 64-bit LPDDR4, DDR4 1600MHz bus
- Dual Quad-SPI for fast boot from SPI NOR
- 2x MIPI-DSI with 4-lanes each
- eDP 1.2 output and DP 1.4 output
- HDMI 2.0 with HDCP 2.0 (Tx/Rx)
- 2x MIPI-CSI with 4-lanes each
- LVDS Tx (2x),
- PCIe 3.0 (2-lanes)
- Dual Gb Ethernet AVB
- SATA3 w/ PHY
- MPEG-2 Transport Stream



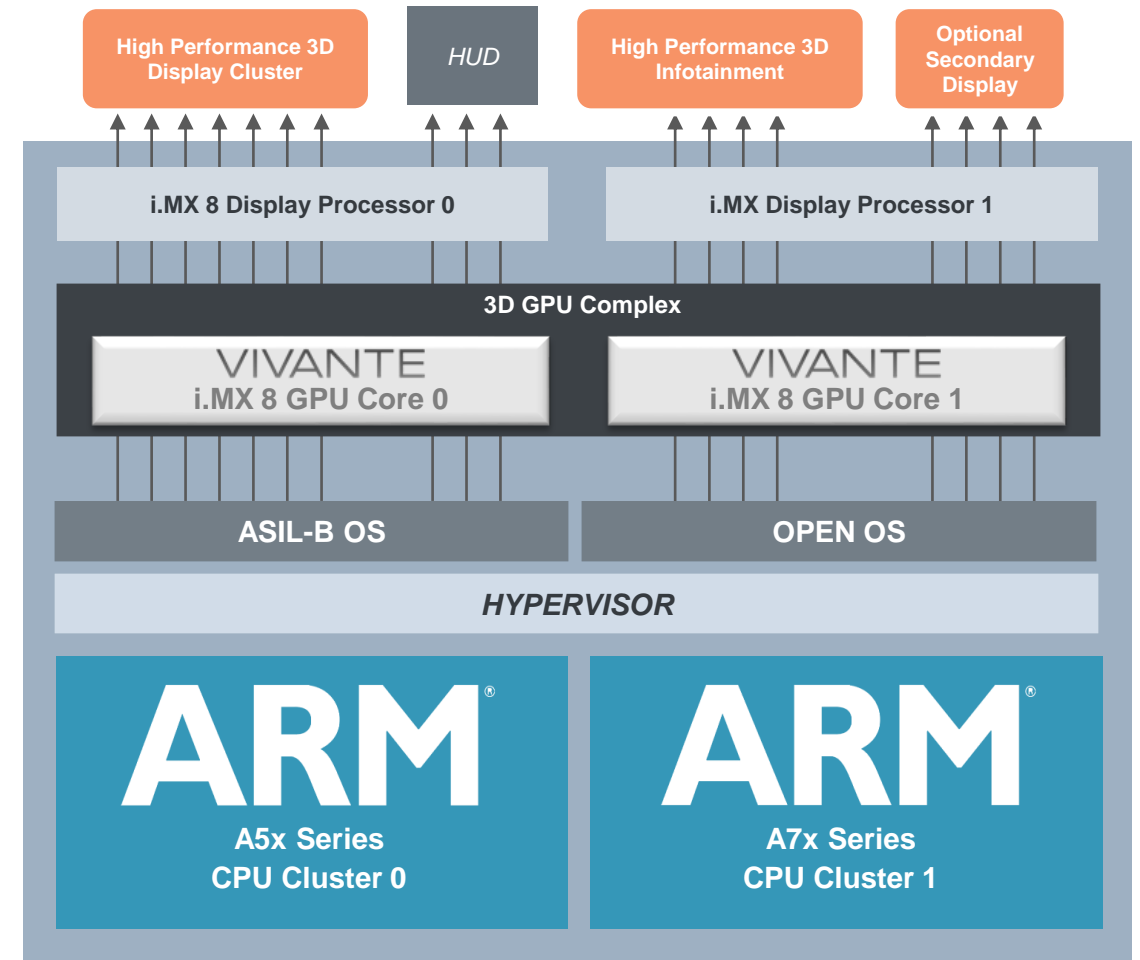
eCockpit USING THE i.MX8 QuadMax



i.MX 8QuadMax eCockpit Strategy

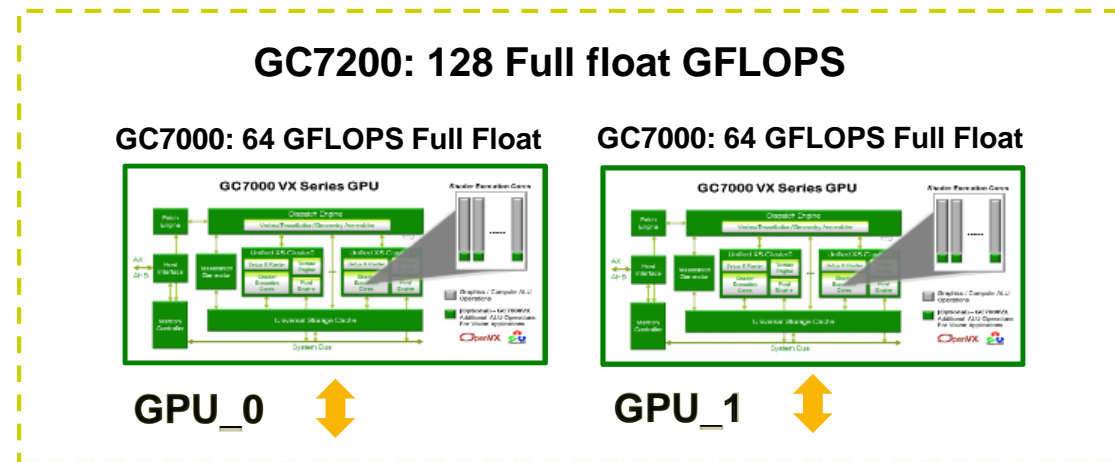
Advantages

- Dual independent display controllers
- Configurable GPU cores
 - Single monolithic GPU
 - Dual independent GPUs
- Industry standard ARM enablement
- SoC level virtualization



i.MX Graphic Strategy: 2 GPU Bridged = 1 Monolithic GPU

- **Strategy is focused on:**
 - Software simplicity
 - HW Isolation for Critical OS (Cluster)
 - Dedicated and predictable GPU performance for multiple OS systems
- **We are providing a GPU subsystem that can either be:**
 - Bridged in HW to make use of 128 GFLOPS in TDM fashion.
 - Isolated in HW to act like 2 distinct GPUs for dedicated 64 GFLOPS with no para-virtualized overhead

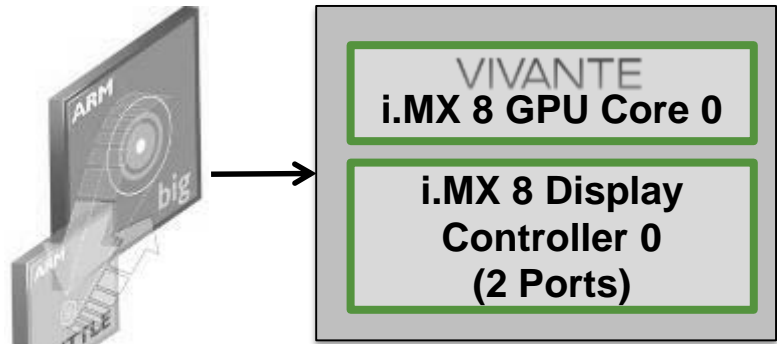


Virtualization: Supporting Multiple OS's on a Single SoC

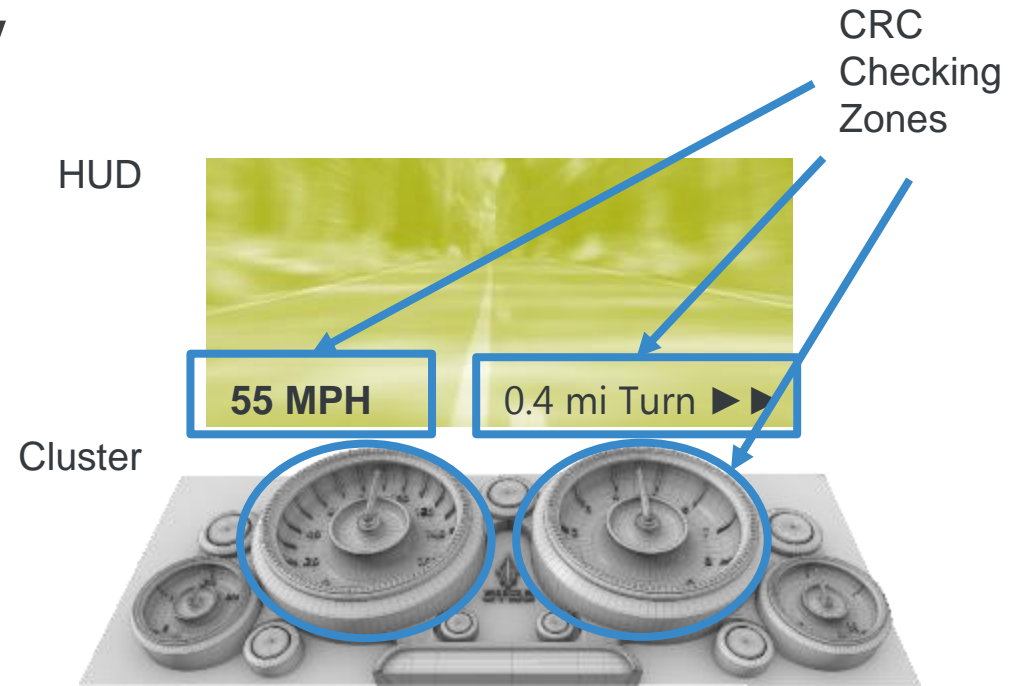
i.MX 8 Strategy

Feature	Software Hypervisor	HW Assisted Hypervisor	HW Assisted Para-Virtualization	Hardware Isolation
Operating System Modifications	Unnecessary	Unnecessary	Required	Unnecessary
Peripheral Driver Modifications	Unnecessary	Unnecessary	Required	Unnecessary
Resource Sharing Overhead	Very High	High	Medium	Low
Performance	Low	Fair	Good	Best
Load Balancing	Tunable	Tunable	Tunable	Fixed (50% - 50%)
Provide both Tunable and Fixed QoS Options				

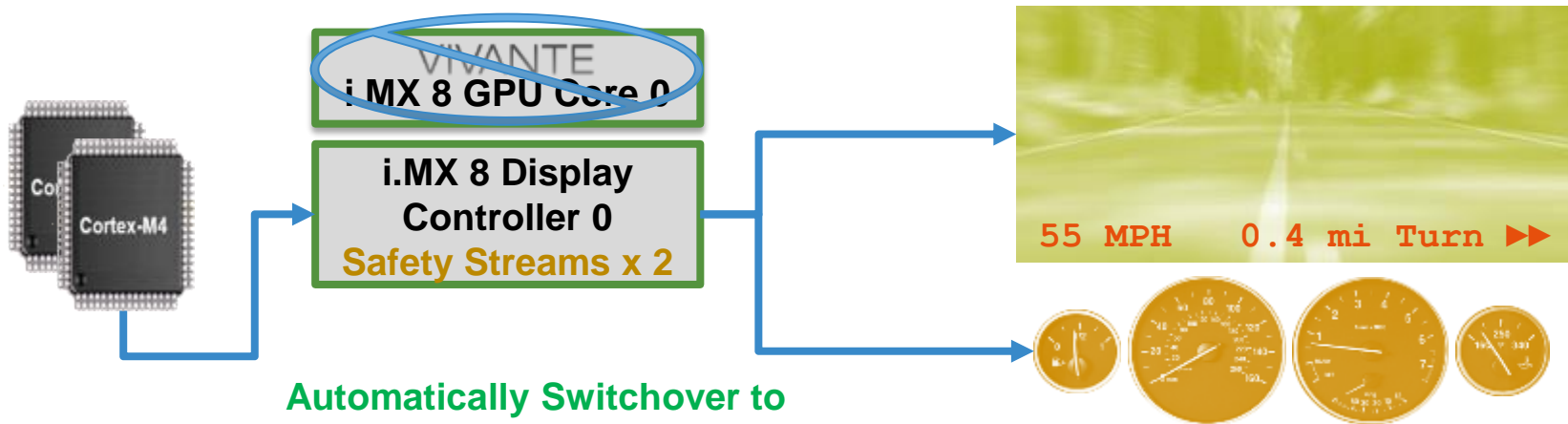
i.MX 8 Display Failover Strategy



Detects CRC MISMATCH



Failover images running in background



Automatically Switchover to Simplified Cluster / HUD

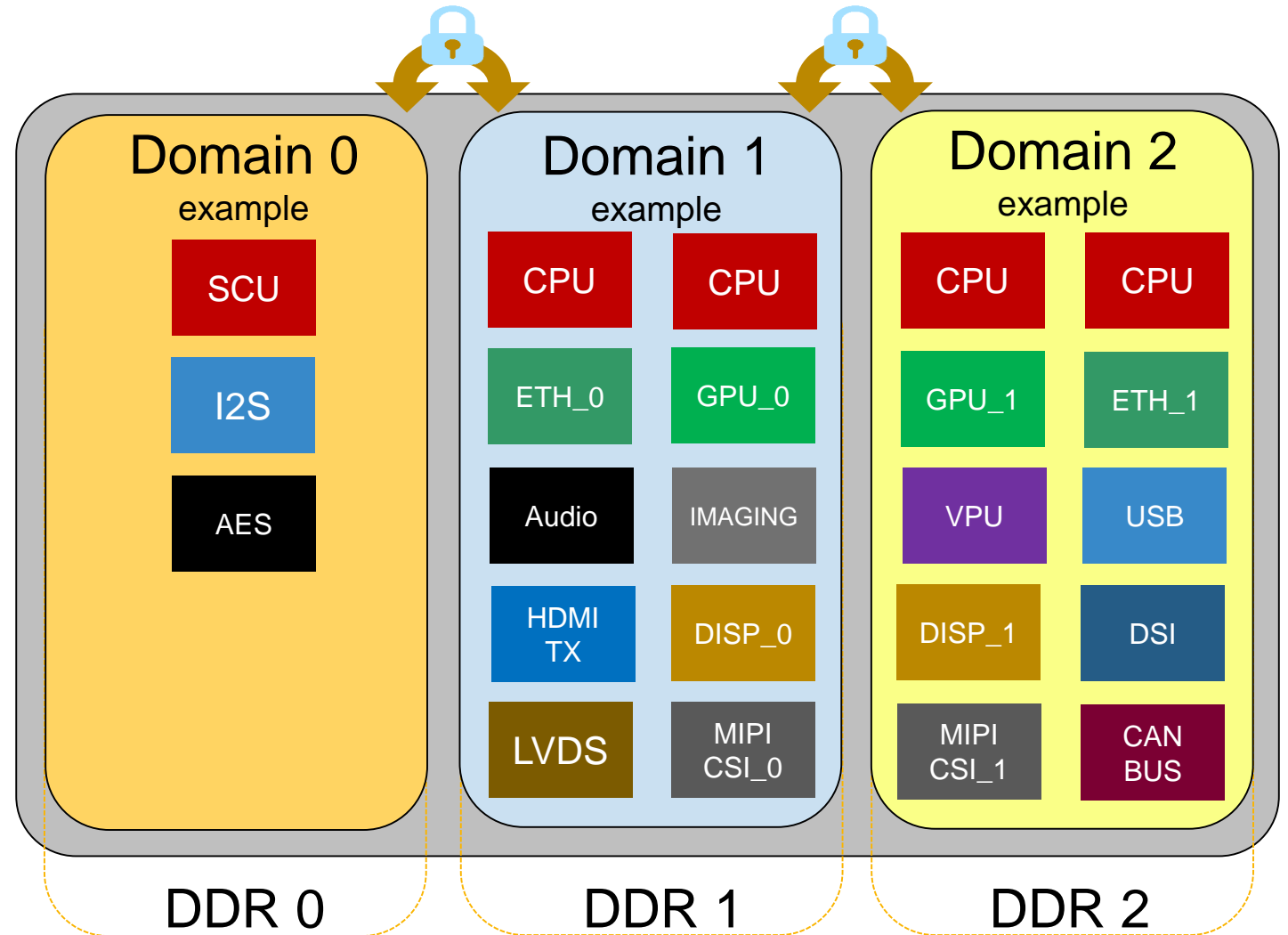
i.MX Domain Partitioning

How Partitioning Works:

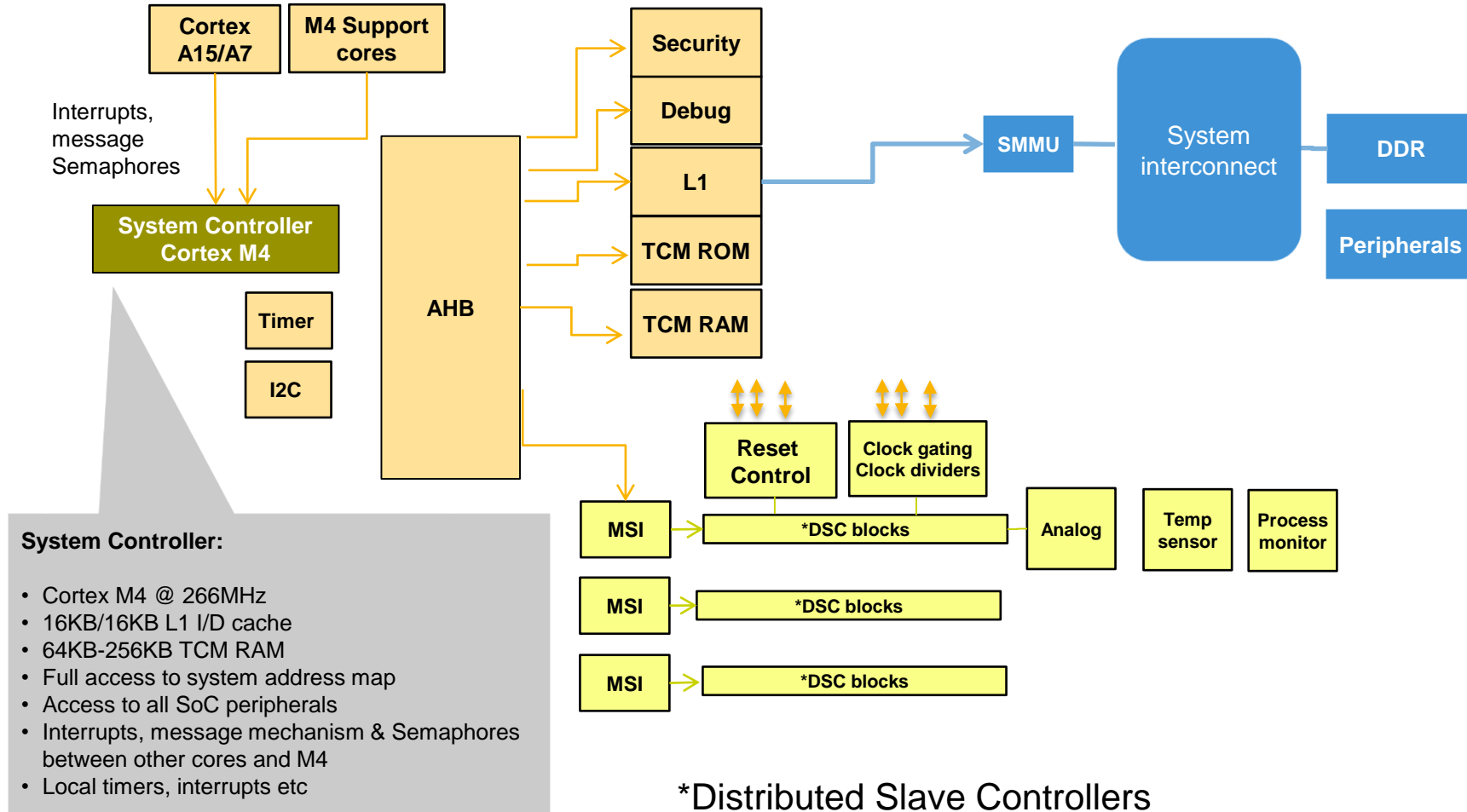
- The system controller commits peripherals and memory regions into a specific domains.
(This is customer defined)
- Any communication between domains are forced to use messaging protocols
If a domain peripheral tries to access other domains illegally, a bus error will occur.

Benefits of Partitioning:

- Reporting of immediate illegal accesses helps track down hard to find race conditions before they go to production. (AKA Sandbox Methods)
- Provides security on a finished product: protects system critical SoC peripherals from less trusted apps and intentional security breaches

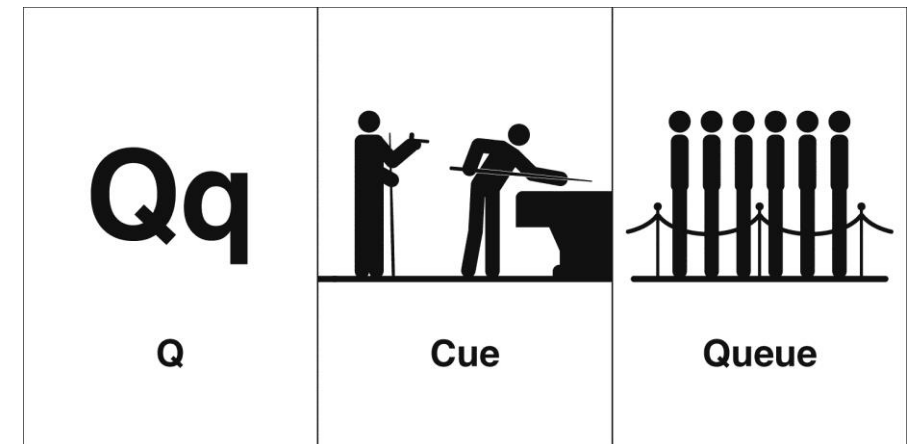


i.MX 8 System Controller



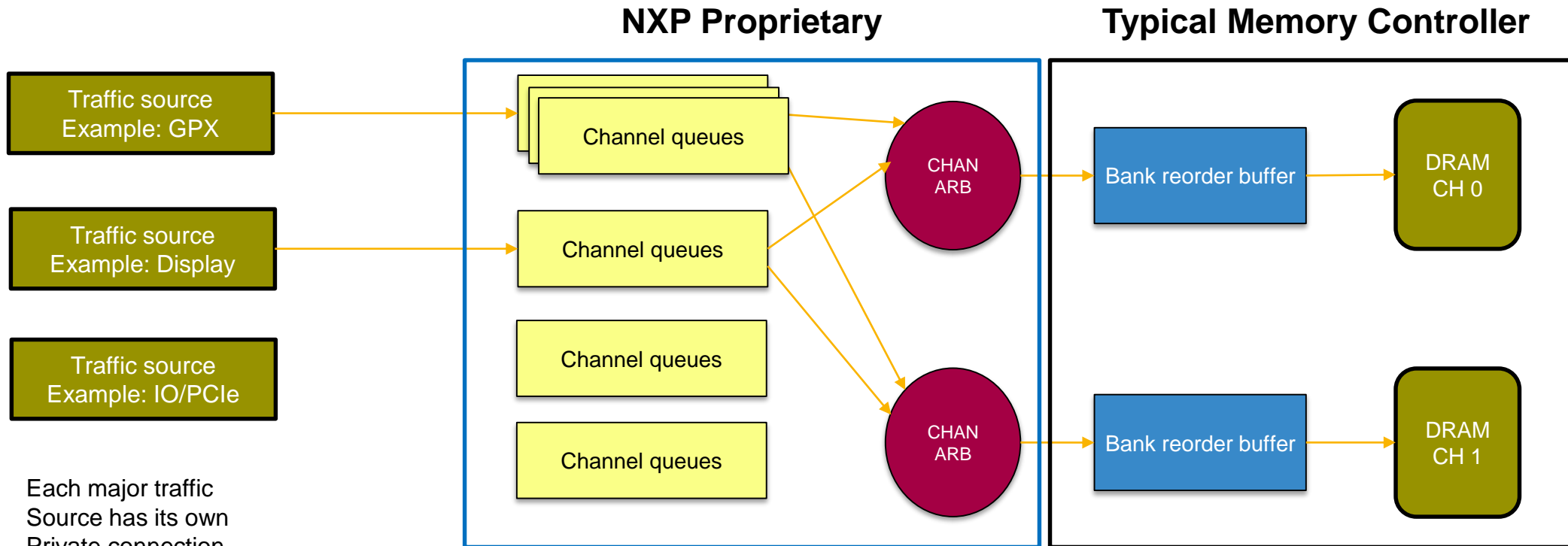
i.MX 8QuadMax DDR Advanced Quality of Service

- i.MX8 can arbitrate memory bandwidth by priority for all the peripheral subsystems on the SoC
- Memory controllers typically focus on page and direction optimization for burst (R/W)
- Our System goes further to ensure transport to and from memory is at full DRAM rate with guaranteed bandwidth



i.MX 8QuadMax DDR QoS Illustration

Highest request for each memory channel is scheduled each cycle



Each major traffic Source has its own Private connection To memory

Each traffic source has a Dedicated set of queues
These each have different priority
Multiple different policies

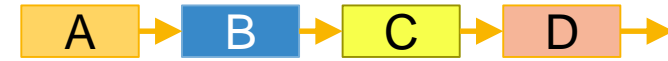
- Fixed
- Time waiting
- Fixed Time slot

Each memory channel Has its own controller
And bank scheduler
To optimize BW

i.MX 8QuadMax QoS / Schedule Policies

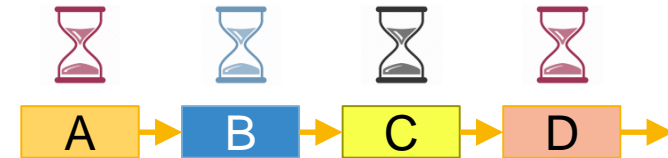
- **Fixed priority**

- Priority for each request in queue is the same
- Typically used for “best efforts” traffic



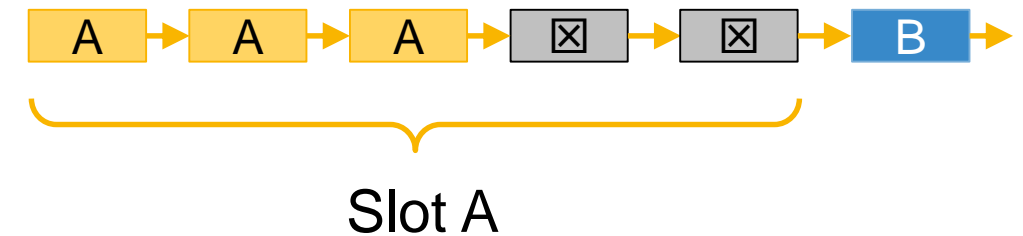
- **Time waiting**

- Priority increases as request waits in queue
- Used to ensure sufficient throughput for device, fixed bandwidth



- **Fixed time slot**

- Every time period this channel gets ALL the accesses, everyone else is blocked
- Used for real time devices, eg display
- Can be used for allocation of bandwidth for specific resource domain



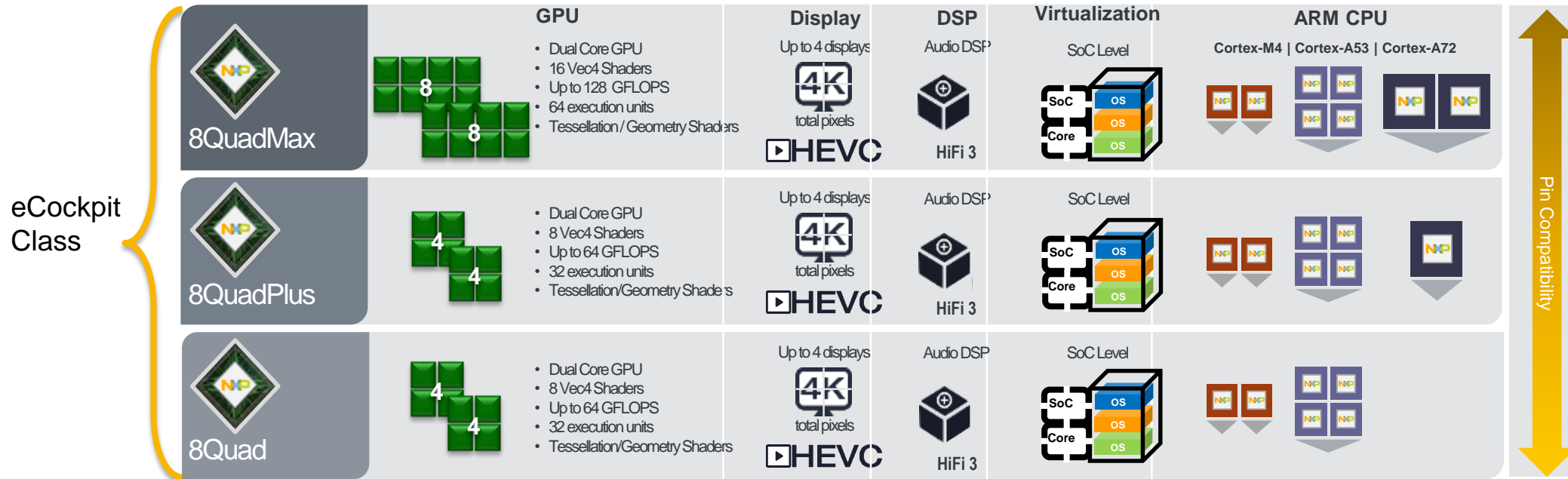
SUMMARY

i.MX8 Quad Series is Architected for eCockpit

eCockpit Class		GPU	Display	DSP	Virtualization	ARM CPU	
	8QuadMax	<ul style="list-style-type: none"> Dual Core GPU 16 Vec4 Shaders Up to 128 GFLOPS 64 execution units Tessellation/Geometry Shaders 	Up to 4 displays total pixels 	Audio DSP HiFi 3	SoC Level SoC Core	Cortex-M4 Cortex-A53 Cortex-A72 	
	8QuadPlus	<ul style="list-style-type: none"> Dual Core GPU 8 Vec4 Shaders Up to 64 GFLOPS 32 execution units Tessellation/Geometry Shaders 	Up to 4 displays total pixels 	Audio DSP HiFi 3	SoC Level SoC Core		
	8Quad	<ul style="list-style-type: none"> Dual Core GPU 8 Vec4 Shaders Up to 64 GFLOPS 32 execution units Tessellation/Geometry Shaders 	Up to 4 displays total pixels 	Audio DSP HiFi 3	SoC Level SoC Core		
	8Dual	<ul style="list-style-type: none"> Single Core GPU 8 Vec4 Shaders Up to 64 GFLOPS 32 execution units Tessellation/Geometry Shaders 	Up to 2 displays 2x 1080p total pixels 	Audio DSP HiFi 3	CPU Level Core		
	8DualLite	<ul style="list-style-type: none"> Single Core GPU 4 Vec4 Shaders Up to 32 GFLOPS 16 execution units Tessellation/Geometry Shaders 	Up to 2 displays 2x 1080p total pixels 	Audio DSP HiFi 3	CPU Level Core		



i.MX8 eCockpit Strategy Summary



- Display Pipe Duplication: 2D / 3D Graphics, Display Controller, Camera System
- Memory sculpting for whole SoC to better guaranty access to DDRAM
- Software and Pin Compatibility for 8QuadMax, 8QuadPlus, 8Quad
- Virtualization strategies to provide HW Isolation, conventional, and para-virtualized driver support with leading virtualization partners

BACKUP



i.MX 8 Support Cores

- **There are 3 M4 cores in the system in addition to the main A53/A72 cores**
 - All have local TCM ram plus L1 caches for Inst and Data
 - All have access to the entire system memory map (subject to access permissions)

1) The System controller is intended to run NXP Firmware which controls the system resources

- Controls of system power, temperature monitoring, clocks
- Management of shared system resources eg GIC, SMMU subject Access control permissions
- Private access to many of the system control functions via MSI and DSCs
- Boots first and using fast Ring Osc no need to wait for XTAL startup
- “runs” whenever the core is powered up

2) Two M4 Cores are unallocated and available for user code

- The System Controller can directly boot these M4s from shared flash/DRAM
- Any system interrupt can be steered to these M4 cores

The Cost of Para-virtualization on Competitive Products

Para-virtualization

- 1) Altering an operating system and driver stack directly to reduce virtualization overhead of memory and peripheral accesses.

Very expensive in terms of support and maintenance.

The operating system and peripheral drivers (GPU, Display) is no longer ignorant of the hypervisor.

Para-virtualization requires:

- Modifications to a guest operating system with kernel based mechanisms for dealing with memory management, interrupt handling, and context switching.
- Additional driver support for every peripheral to make “hyper-calls” into the hypervisor to avoid the software trapping mechanism for physical address translation.

Each variation of driver or OS will require long term maintenance over a higher layer of software complexity!



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