FTF 2016
TECHNOLOGY FORUM

# HARDWARE AND THERMAL DESIGN WITH SCM

## FTF-DES-N1991

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FTF-DES-N1991
MAY 17, 2016

PUBLIC USE

# AGENDA

- PCB Design For Success
  - Materials and Impact onto Thermal Behavior and Signal Integrity
  - Component Selections (Capacitors)
  - General Routing Rules and Common Mistakes
  - Copper Thickness
- Power Routing
  - Sources of Noise
  - Noise Ripple Reduction Strategy
- Thermal Management
- 6SX Breakout Example

# Myth #1: PCB Material Does Not Matter if Layout is Done Right

- PCB material selection is extremely important, especially for the systems with high speed routing
- Capacitive loading
  - Q = CV
  - C = (e * A)/d
- Signal propagation delay
  - tpd = sqrt(er)/c
    - Where c is the speed of light: approx. 3 * 10^8 m/s
    - er is the relative permittivity constant (er = ematerial/ e0 is free space permittivity or 8.85 * 10^-12 F/m)
      - er for free space is approximately 1. (8.85 * 10^-12 / 8.85 * 10^-12)
- Wrong material choice affects the performance of the board!!!

| Material | Tg | Permittivity (Dk or εr) | | | | Loss Tangent (Df) | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | Dk@100MHz | Dk@1GHz | Dk@5GHz | Dk@10GHz | Df@100MHz | Df@1GHz | Df@5GHz | Df@10GHz |
| FR4 | 130 | 4.8 | 4.34 | - | - | 0.008 | - | 0.008 | - |
| FR408 | 180 | 3.69 | 3.66 | 3.67 | 3.65 | 0.0094 | 0.0117 | 0.0127 | 0.0125 |
| 370HR | 180 | 4.24 | 4.17 | 3.92 | 3.92 | 0.0150 | 0.0161 | 0.0250 | 0.0250 |
| TU-768 | 190 | - | 4.4 | 4.3 | 4.3 | - | 0.019 | 0.021 | 0.023 |
| S1141 | 140 | 4.6 | 4.6 | - | - | 0.015 | - | - | - |



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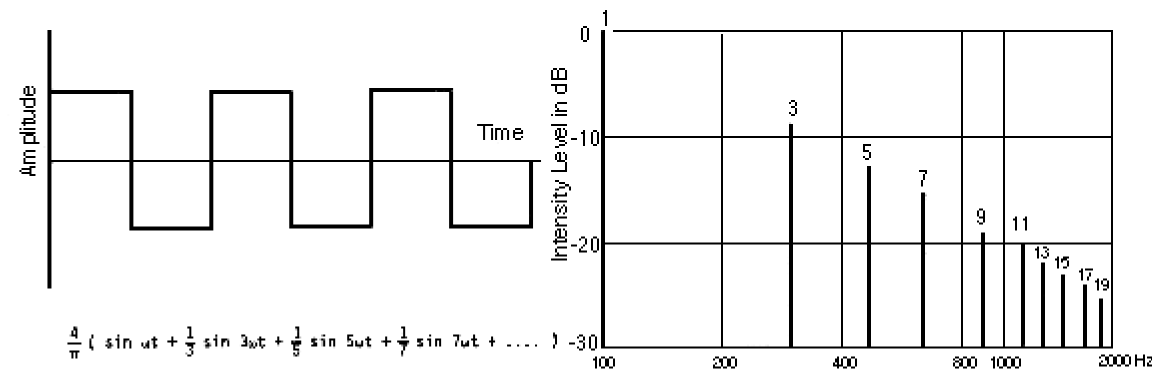
# Myth #2: PCB Layout Design to Meet the Fastest Clock Frequency

- Clock frequency only refers to the fundamental frequency. Does not take in considerations of the higher spectrum frequencies.

- Square waves consist of the fundamental frequencies and the odd partials (overtones).
  - Combination of the frequencies up to 5th or 7th partials must be taken into consideration




  - Slew rate is affected by the number of partials present in the signal.
  - BW = 0.35/RT

# Myth #2: PCB Layout Design to Meet the Fastest Clock Frequency (Cond.)

- How long can my trace be for slew rate of 0.5ns?
  - Assuming propagation delay of 0.18ps/mil

- The characteristics of PCB material

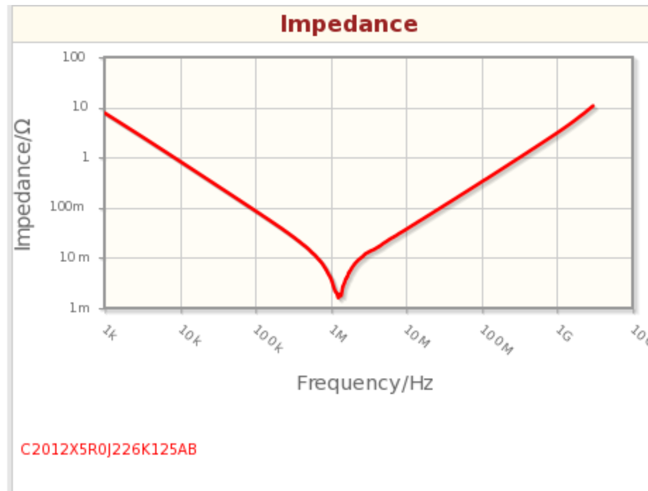
- Length matching:
  - Clock must always be the longest of all traces
  - Tolerance depends on the clock speed and slew rate

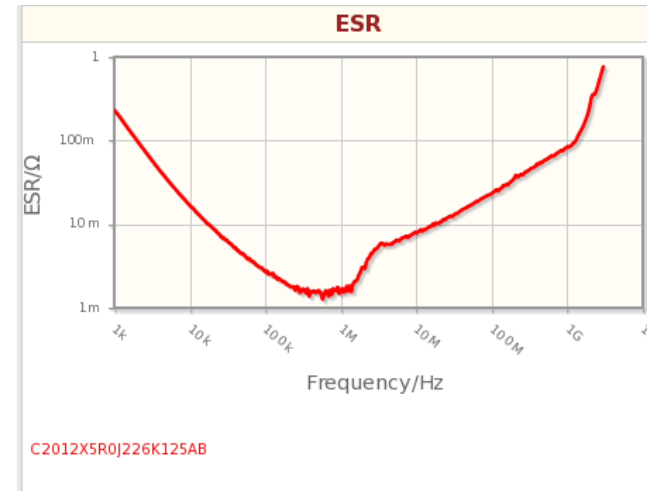
# Myth #3: Capacitor Value is Guaranteed Within Operating Range

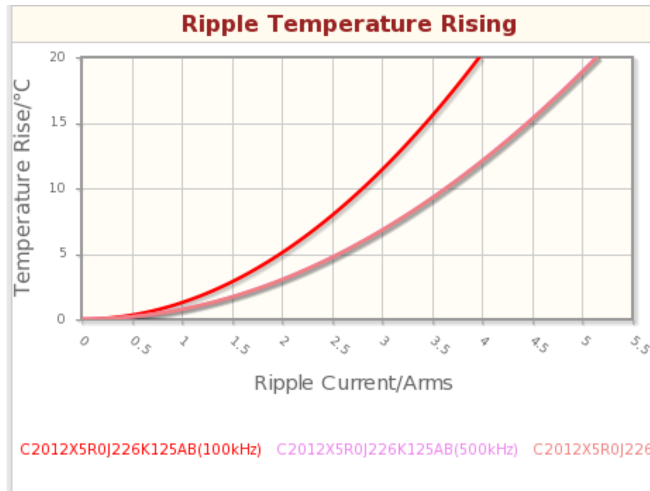
- Selecting capacitor values solely on capacitance and ESR will cause design issues
- Capacitance vary dramatically within operating parameter ranges

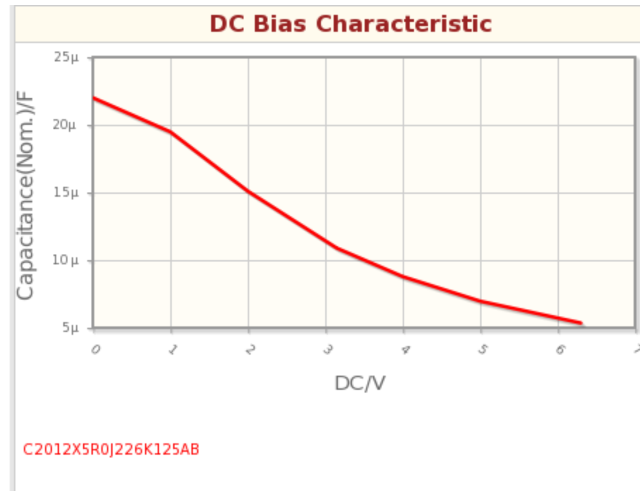
- You must take in account for:
  - Frequency response / impedance
  - ESR
    - Materials affect the ESR.  X5R, X5S, X7R, etc
  - Voltage rating / DC bias
    - Effective capacitance drop significantly as nominal DC voltage reach closer to rated voltage
    - Always choose 3x the nominal voltage rail
  - Temperature
    - As the temperature approaches the maximum, effective capacitance drops

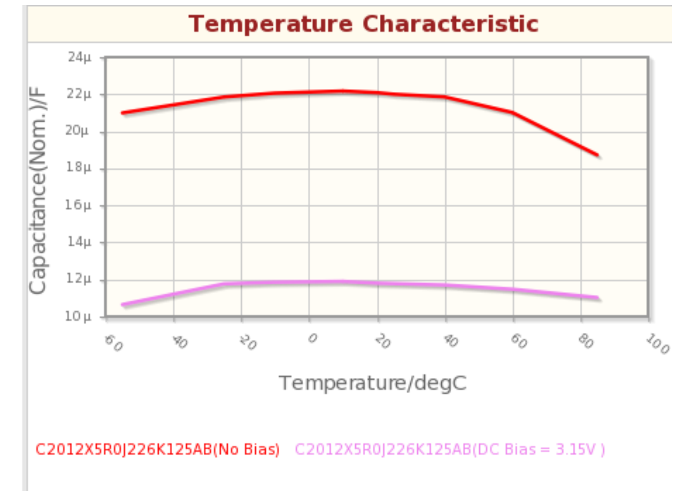
# 22uF X5R Capacitor Parameter Examples



# Effects of Choosing <3x DC Voltage Rating

- Nominal voltage @ 3.15V with 22uF 6.3V
  - Reactance calculation: Xc = 1/(wC)
  - Nominally 22uF reactance is the lowest at approximately 1MHz
  - DC bias voltage of 3.15V lowers the effective capacitance to 11uF.
- Higher temperature lowers the effective capacitance.
- The bulk capacitor may be less than half of the rated capacitance!!

| Frequency | Xc nominal capacitance (22uF) | Xc Derated capacitance (11uF) |
|---|---|---|
| 1 | 7234.529 | 14469.06 |
| 10 | 723.4529 | 1446.906 |
| 100 | 72.34529 | 144.6906 |
| 1kHz | 7.234529 | 14.46906 |
| 10kHz | 0.723453 | 1.446906 |
| 100kHz | 0.072345 | 0.144691 |
| 1MHz | 0.007235 | 0.014469 |



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# Reference Used

- ANSI / IPC-2221
  - Title:
  - Published:
- ANSI / IPC-2222
  - Title:  Sectional Design Standard for Rigid Organic Printed Boards
  - Published: Feb. 1998
- TDK corporation's capacitor selection page
  - http://www.tdk.com/capacitors.php
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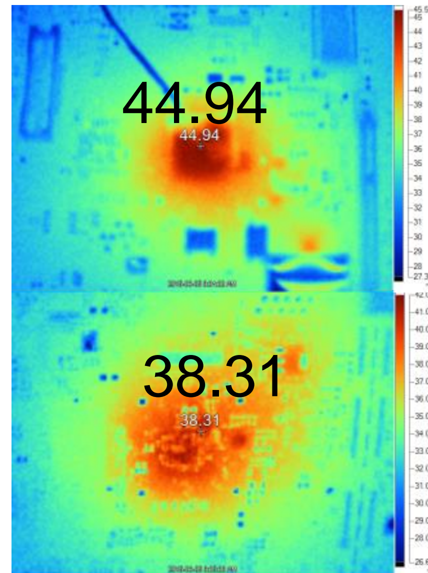
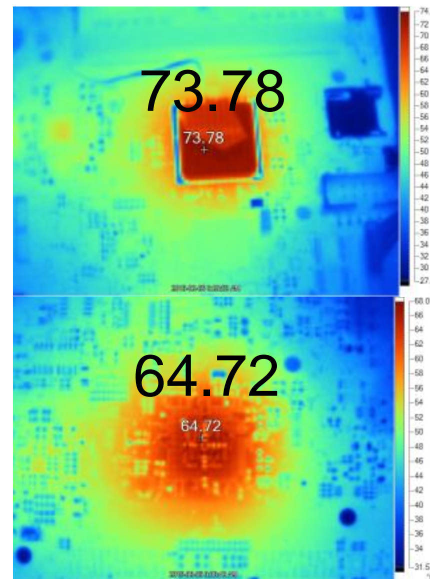
# THERMAL CONSIDERATIONS FOR SCM-IMX6D

# Thermal Measurements (Discrete vs SCM)

CODE RUNNING
HDMI , LVDS, MemTest



SCM6D running on a 14 Layer HVB running at 800MHz



Discrete iMX6DQ with SoDIMM DDR3, 8 Layer, running at 1GHz

# Thermal Profile

SCM
FO-WLP thermal

| Parameter Description | Test Condition | Symbol | Value | Unit |
|---|---|---|---|---|
| Junction to Ambient1,6 | Single-layer board (1s); natural convection 2 | $R_{\theta JA}$ | 36.5 | °C/W |
| | Four-layer board (2s2p); natural convection 2 | $R_{\theta JA}$ | 19.9 | °C/W |
| Junction to Ambient1,6 Forced Convection | Single-layer board (1s); air flow 200ft/min 3 | $R_{\theta JMA}$ | 27.7 | °C/W |
| | Four-layer board (2s2p); air flow 200ft/min 3 | $R_{\theta JMA}$ | 16.1 | °C/W |
| Junction to Board1,4,6 | - | $R_{\theta JB}$ | 6.6 | °C/W |
| Junction to top characterization parameter1,5,6 | - | $\Psi_{JT}$ | 2.9 | °C/W |

i.MX6DQ
FCPBGA thermal

| **Thermal Parameter** | **Test Conditions** | **Symbol** | **Value** | **Unit** |
|---|---|---|---|---|
| Junction to Ambient[1] | Single-layer board (1s); natural convection[2] | $R_{\theta JA}$ | 31 | °C/W |
| | Four-layer board (2s2p); natural convection[2] | $R_{\theta JA}$ | 22 | °C/W |
| Junction to Ambient[1] | Single-layer board (1s); air flow 200 ft/min[3] | $R_{\theta JMA}$ | 24 | °C/W |
| | Four-layer board (2s2p); air flow 200 ft/min[3] | $R_{\theta JMA}$ | 18 | °C/W |
| Junction to Board[1,4] | — | $R_{\theta JB}$ | 12 | °C/W |
| Junction to Case (top)[1,5] | — | $R_{\theta JCtop}$ | <0.1 | °C/W |

$R\theta JB$ is a significant contributor in thermal resistance reduction
Higher board layer lowers the thermal resistance

# RqJB Comparison (SCM vs. FCPBGA)

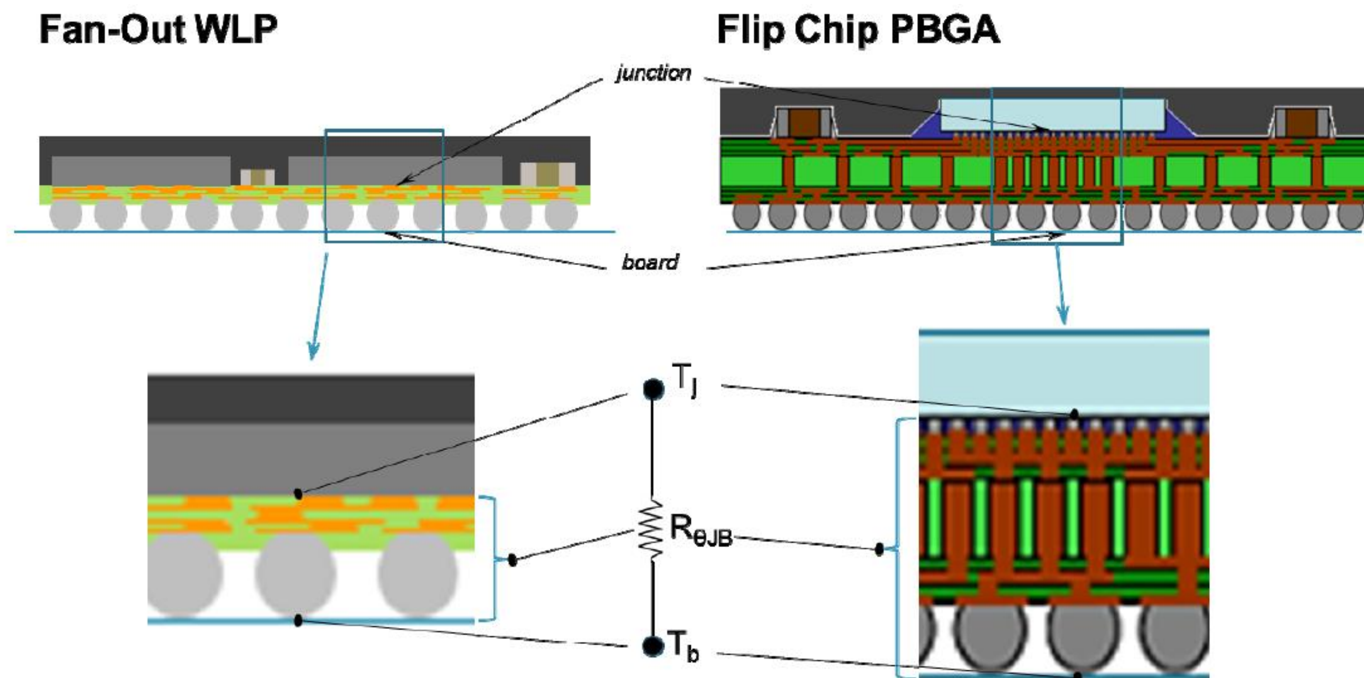



Table 3. Comparison of "$R_{\theta JB}$" Layer

| SCM (FO-WLP) | | | FCPBGA | | |
|---|---|---|---|---|---|
| $R_{\theta JB}$ Layer | Thickness (µm) | Thermal Cond. (W/m-K) | $R_{\theta JB}$ Layer | Thickness (µm) | Thermal Cond. (W/m-K) |
| RDL (Cu, dielectric) | 100 | 400, < 1.0 | Bump (Cu, UF) | 100 | 400, < 1.0 |
| | | | Substrate | 500 | < 0.5 |

# Thermal Conductivity of the Package Components

- Thermal conductivity equasion
  - q/A = (k*dT)/s
    - Where 'q/A' is the heat transfer per unit area (W/m^2)
    - Where 'k' is the thermal conductivity (W/mK)
    - Where 'dT' is the temperature difference (deg C)
    - Where 's' is the thickness
- Copper (400W/mK) will yield: 320,000,000 W/m^2
- Substrate (<0.5W/mK) will yield: 80,000 W/m^2 Insulates heat!!
- SCM package without substarate shows superior heat conduction…
- PCB employing SCM must consider thermal design

Table 3. Comparison of "$R_{\theta JB}$" Layer

| SCM (FO-WLP) | | | FCPBGA | | |
|---|---|---|---|---|---|
| $R_{\theta JB}$ Layer | Thickness (µm) | Thermal Cond. (W/m-K) | $R_{\theta JB}$ Layer | Thickness (µm) | Thermal Cond. (W/m-K) |
| RDL (Cu, dielectric) | 100 | 400, < 1.0 | Bump (Cu, UF) | 100 | 400, < 1.0 |
| | | | Substrate | 500 | < 0.5 |



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# Thermal Conductivity of the PCB Stack up

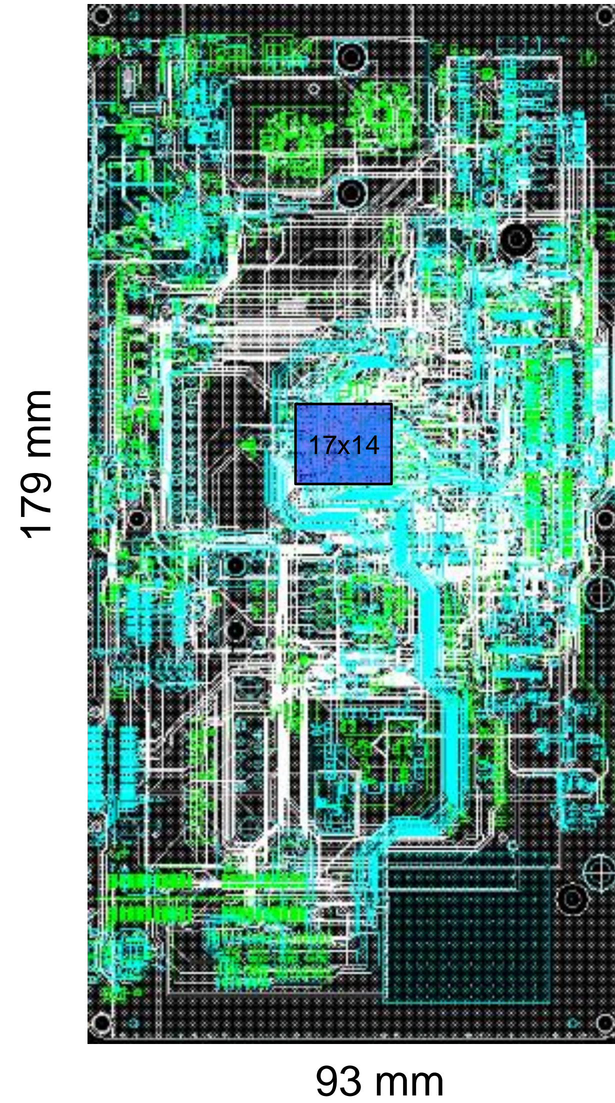
| Material | Thermal conductivity K(W/mK) | Thermal conductivity K((W/inK) |
|---|---|---|
| Copper | 355 | 9 |
| Air | 0.0275 | 0.0007 |
| Solder | 39 | 0.98985 |
| FR4 | 0.25 | 0.0064 |
| 370HR | 0.4 | 0.010 |
| Solder mask | 0.21 | 0.0054 |

- Thermal conductivity equasion
  - q/A = (k*dT)/s
    - Where ‘q/A’ is the heat transfer per unit area (W/m^2)
    - Where ‘k’ is the thermal conductivity (W/mK)
    - Where ‘dT’ is the temperature difference (deg C)
    - Where ‘s’ is the thickness
- Theta (q) or thermal resistance of the materials can be determined by:
  - q = length / (k * area)
    - Where k is the thermal conductivity (W/mK) or (W/inK). We are using (W/inK) for this example
    - We are using 1sq-in of PCB space for this example
    - Length can be the thickness of copper or the lateral distance from the heat.
    - Vertical heat conduction -> top side to bottom side
    - Lateral heat conduction -> same plane, lateral heat conduction about the cross sectoin

# EVB Layer Stack

| Name | Type | Material | Thickness (MIL) | C/W vertical | C/W lateral |
|---|---|---|---|---|---|
| | DIELECTRIC | TAIYO4000_SOLDERMK | 0.5 | 0.092592593 | 370370.3704 |
| TOP | CONDUCTOR | 3/8OZ_COPPER_PLATED | 1.7 | 0.000188889 | 65.35947712 |
| | DIELECTRIC | 370HR | 3 | 0.3 | 33333.33333 |
| L2_GND_1 | PLANE | 3/8OZ_COPPER | 1 | 0.000111111 | 111.1111111 |
| | DIELECTRIC | 370HR-2GHZ | 4.8 | 0.48 | 20833.33333 |
| L3_INT_1 | CONDUCTOR | 1OZ_COPPER | 1.5 | 0.000166667 | 74.07407407 |
| | DIELECTRIC | 370HR-2GHZ | 8.6 | 0.86 | 11627.90698 |
| L4_PWR_1 | PLANE | 1/2OZ_COPPER | 0.6 | 6.66667E-05 | 185.1851852 |
| | DIELECTRIC | 370HR | 5 | 0.5 | 20000 |
| L5_INT_2 | CONDUCTOR | 1/2OZ_COPPER | 0.6 | 6.66667E-05 | 185.1851852 |
| | DIELECTRIC | 370HR | 4.9 | 0.49 | 20408.16327 |
| L6_PWR_2 | PLANE | 1OZ_COPPER | 1.2 | 0.000133333 | 92.59259259 |
| | DIELECTRIC | 370HR | 3 | 0.3 | 33333.33333 |
| L7_PWR_3 | PLANE | 1OZ_COPPER | 1.2 | 0.000133333 | 92.59259259 |
| | DIELECTRIC | 370HR | 4.9 | 0.49 | 20408.16327 |
| L8_INT_3 | CONDUCTOR | 1/2OZ_COPPER | 0.6 | 6.66667E-05 | 185.1851852 |
| | DIELECTRIC | 370HR | 5 | 0.5 | 20000 |
| L9_GND_3 | PLANE | 1/2OZ_COPPER | 0.6 | 6.66667E-05 | 185.1851852 |
| | DIELECTRIC | 370HR | 8.6 | 0.86 | 11627.90698 |
| L10_INT_4 | CONDUCTOR | 1OZ_COPPER | 1.5 | 0.000166667 | 74.07407407 |
| | DIELECTRIC | 370HR | 4.8 | 0.48 | 20833.33333 |
| L11_GND_4 | PLANE | 3/8OZ_COPPER | 1 | 0.000111111 | 111.1111111 |
| | DIELECTRIC | 370HR-2GHZ | 3 | 0.3 | 33333.33333 |
| BOTTOM | CONDUCTOR | 3_8OZ_COPPER | 1.7 | 0.000188889 | 65.35947712 |
| | DIELECTRIC | TAIYO4000_SOLDERMK | 0.5 | 0.092592593 | 370370.3704 |

179 mm




93 mm



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# QWKS-Board rev0 vs rev1/rev2

Rev 0 : 12 Layers

LAY_28807.BRD

| Name | Type | Material | Thickness (MIL) | C/W vertical | C/W lateral |
|---|---|---|---|---|---|
| | DIELECTRIC | TAIYO4000_SOLDERMK | 0.5 | 0.092592593 | 370370.3704 |
| TOP | CONDUCTOR | 3/8OZ_COPPER_PLATED | 1.7 | 0.000188889 | 65.35947712 |
| | DIELECTRIC | 370HR | 3 | 0.3 | 33333.33333 |
| L2_GND_1 | PLANE | 3/8OZ_COPPER | 1 | 0.000111111 | 111.1111111 |
| | DIELECTRIC | 370HR-2GHZ | 4.8 | 0.48 | 20833.33333 |
| L3_INT_1 | CONDUCTOR | 1OZ_COPPER | 1.5 | 0.000166667 | 74.07407407 |
| | DIELECTRIC | 370HR-2GHZ | 8.6 | 0.86 | 11627.90698 |
| L4_PWR_1 | PLANE | 1/2OZ_COPPER | 0.6 | 6.66667E-05 | 185.1851852 |
| | DIELECTRIC | 370HR | 5 | 0.5 | 20000 |
| L5_INT_2 | CONDUCTOR | 1/2OZ_COPPER | 0.6 | 6.66667E-05 | 185.1851852 |
| | DIELECTRIC | 370HR | 4.9 | 0.49 | 20408.16327 |
| L6_PWR_2 | PLANE | 1OZ_COPPER | 1.2 | 0.000133333 | 92.59259259 |
| | DIELECTRIC | 370HR | 3 | 0.3 | 33333.33333 |
| L7_PWR_3 | PLANE | 1OZ_COPPER | 1.2 | 0.000133333 | 92.59259259 |
| | DIELECTRIC | 370HR | 4.9 | 0.49 | 20408.16327 |
| L8_INT_3 | CONDUCTOR | 1/2OZ_COPPER | 0.6 | 6.66667E-05 | 185.1851852 |
| | DIELECTRIC | 370HR | 5 | 0.5 | 20000 |
| L9_GND_3 | PLANE | 1/2OZ_COPPER | 0.6 | 6.66667E-05 | 185.1851852 |
| | DIELECTRIC | 370HR | 8.6 | 0.86 | 11627.90698 |
| L10_INT_4 | CONDUCTOR | 1OZ_COPPER | 1.5 | 0.000166667 | 74.07407407 |
| | DIELECTRIC | 370HR | 4.8 | 0.48 | 20833.33333 |
| L11_GND_4 | PLANE | 3/8OZ_COPPER | 1 | 0.000111111 | 111.1111111 |
| | DIELECTRIC | 370HR-2GHZ | 3 | 0.3 | 33333.33333 |
| BOTTOM | CONDUCTOR | 3_8OZ_COPPER | 1.7 | 0.000188889 | 65.35947712 |
| | DIELECTRIC | TAIYO4000_SOLDERMK | 0.5 | 0.092592593 | 370370.3704 |

Rev 1/Rev 2 : 6 Layers

LAY_28927.BRD

| Name | Type | Material | Thickness (MIL) | C/W vertical | C/W lateral |
|---|---|---|---|---|---|
| | DIELECTRIC | TAIYO4000_SOLDERMK | 0.7 | 0.12962963 | 264550.2646 |
| TOP | CONDUCTOR | 2OZ_COPPER_PLATED | 2.2 | 0.000244444 | 50.50505051 |
| | DIELECTRIC | 370HR | 4.5 | 0.45 | 22222.22222 |
| L2_GND_1 | PLANE | 1OZ_COPPER | 1.3 | 0.000144444 | 85.47008547 |
| | DIELECTRIC | 370HR-2GHZ | 4 | 0.4 | 25000 |
| L3_INT_1 | CONDUCTOR | 1OZ_COPPER | 1.3 | 0.000144444 | 85.47008547 |
| | DIELECTRIC | 370HR-2GHZ | 35 | 3.5 | 2857.142857 |
| L4_INT_2 | PLANE | 1OZ_COPPER | 1.3 | 0.000144444 | 85.47008547 |
| | DIELECTRIC | 370HR | 4 | 0.4 | 25000 |
| L5_PWR | CONDUCTOR | 1OZ_COPPER | 1.3 | 0.000144444 | 85.47008547 |
| | DIELECTRIC | 370HR | 4.5 | 0.45 | 22222.22222 |
| BOTTOM | CONDUCTOR | 2OZ_COPPER | 2.2 | 0.000244444 | 50.50505051 |
| | DIELECTRIC | TAIYO4000_SOLDERMK | 0.7 | 0.12962963 | 264550.2646 |

# Through Hole

- Through hole via thermal characteristics
- q = L/(k * pi * (r1^2 – r0^2))
- 18RD8 via is: 219 C/W

- Comparing this to one via, conduction of the PCB without via is approximately
  - q = thickness/(k * W*L) = 0.062in / (0.01 * 1in * 1in) = 6.2 C/W for 1sq inch
  - Heat is concentrated on each switcher
    - 3balls x 2balls (1.95mm x 1.3mm) is the thermal area of SW1A = 77mil * 51mil = 0.003927 in^2
    - If there were only dielectric and no via underneath: 6.2C/W in^2 / 0.003927 in^2 = 1578.8C/W

    - One 18RD8 via will provide 219 C/W of thermal resistance
    - Multiple vias will make the heat dissipation more efficient:
      - 2 parallel halves the thermal resistance
      - 4 clusters will be the quarter of the single thermal resistance

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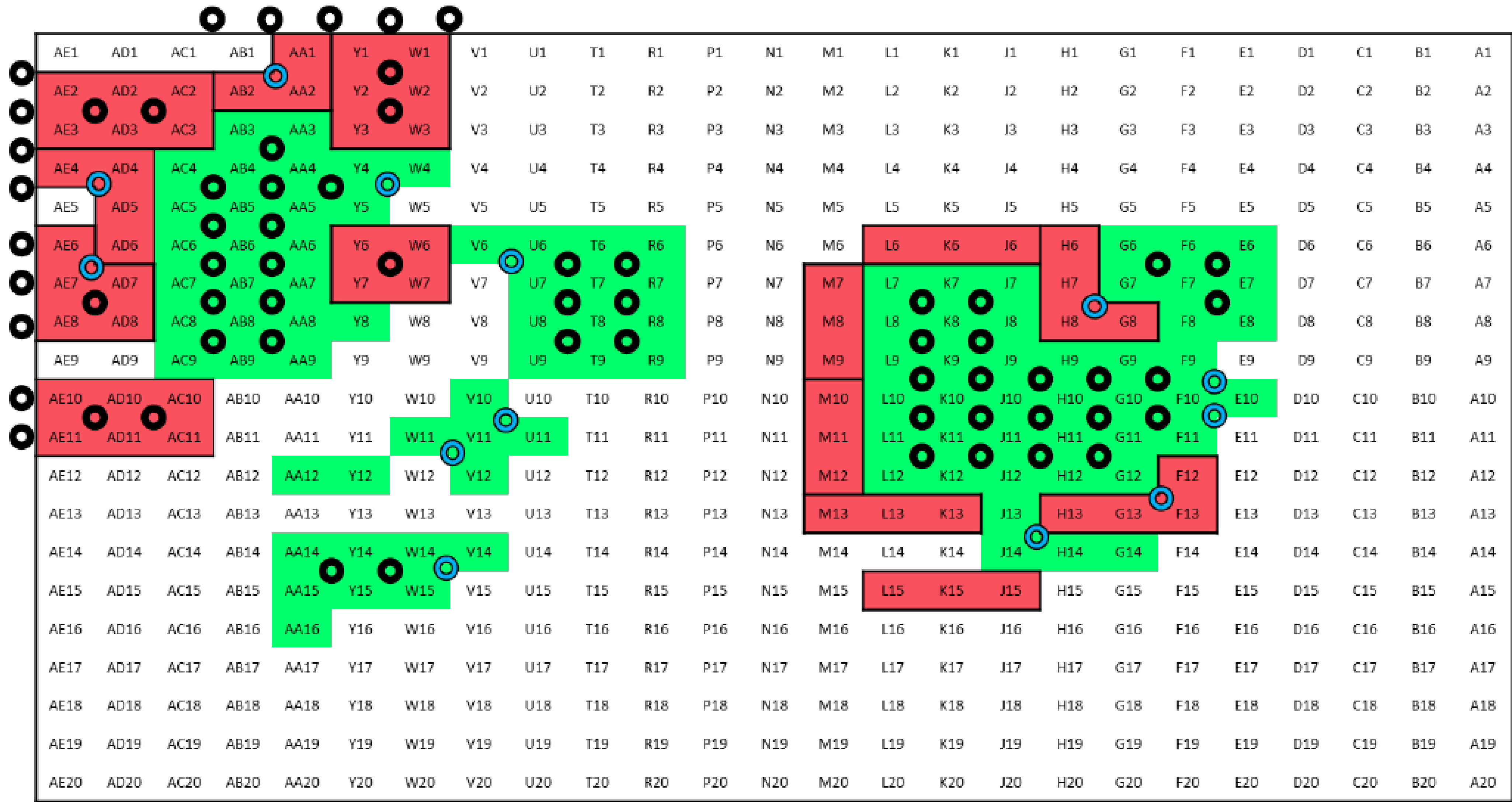
# SCM-i.MX6DQ: Thermal Via Placement Recommendation



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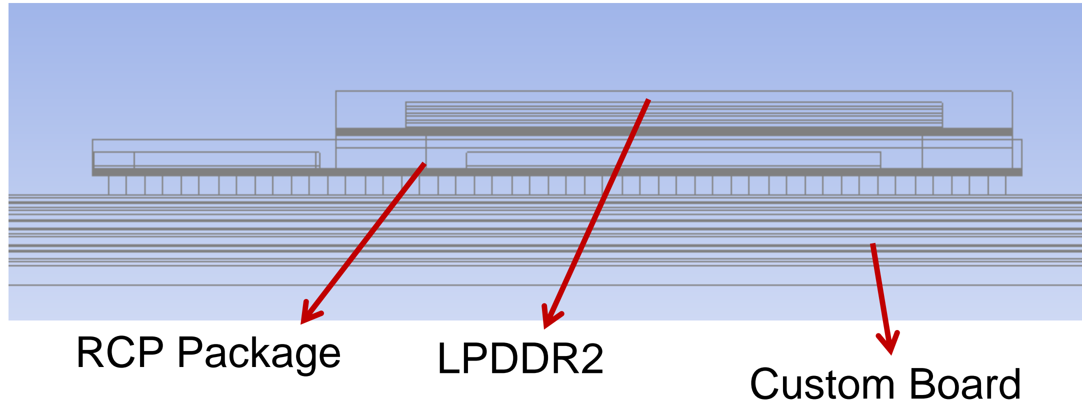
# Geometrical Model

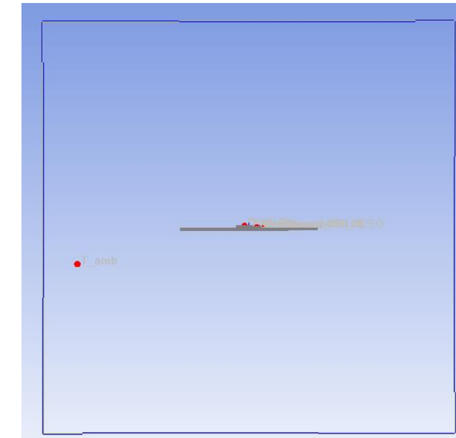
Cross Section – Z plane



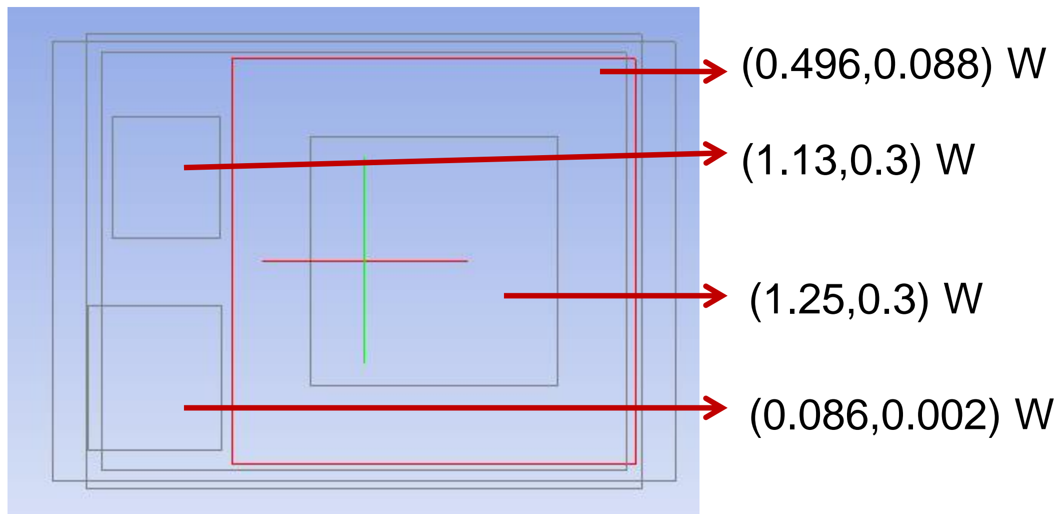
RCP Package

LPDDR2

Custom Board



ThetaJA Env



(0.496,0.088) W

(1.13,0.3) W

(1.25,0.3) W

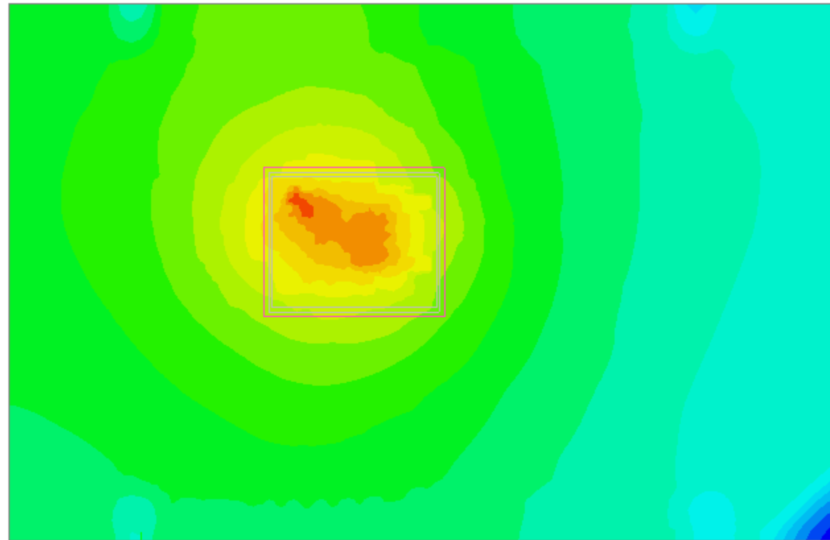
(0.086,0.002) W

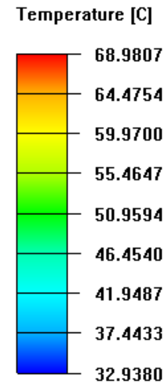
XY Plane

Total power dissipation = **2.96 W**

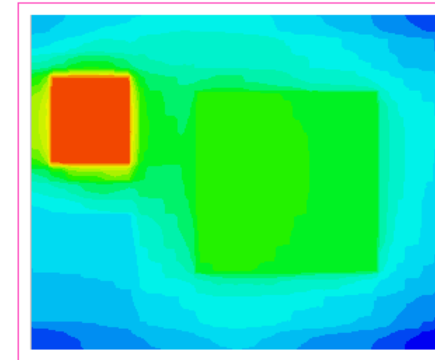
| | Active (W) | Idle (W) |
|---|---|---|
| PF0100 | 1.13 | 0.3 |
| NOR | 0.086 | 0.002 |
| LPDDR2 | 0.496 | 0.088 |
| iMX6 | 1.25 | 0.208 |
| Total | 2.962 | 0.51 |

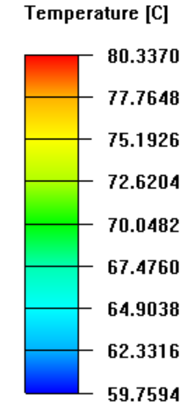
# Steady State Results – 6 Layer (Rev X1)



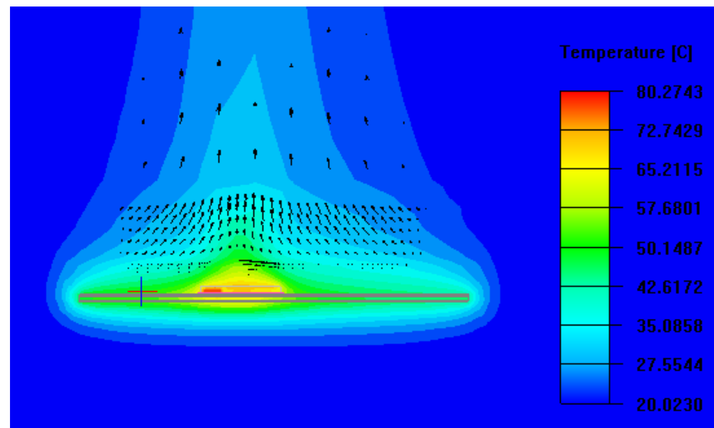



Board Top Layer Temperature Contour

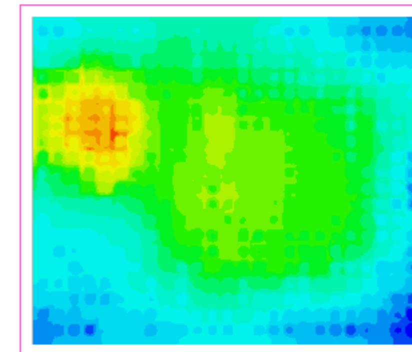


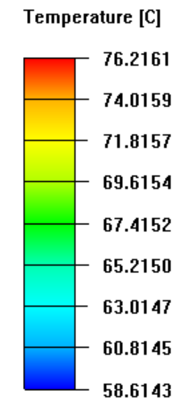



RDL Top Layer



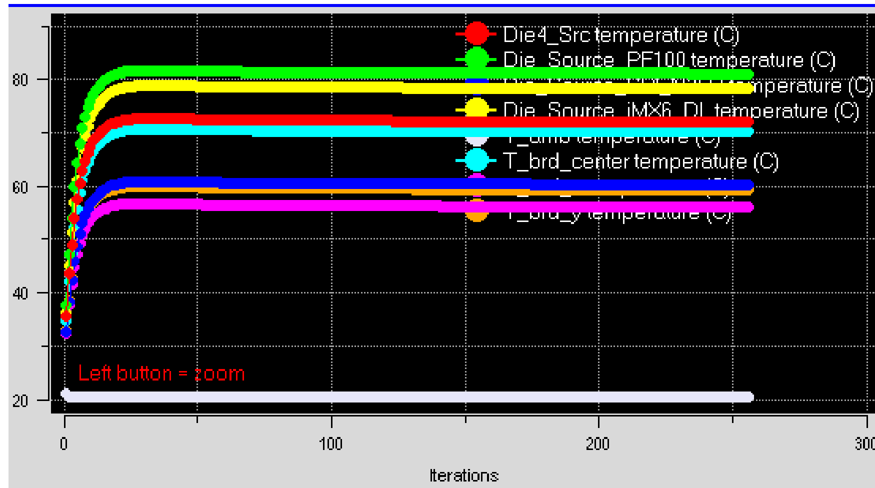

Natural Convection (Pkg + Board)

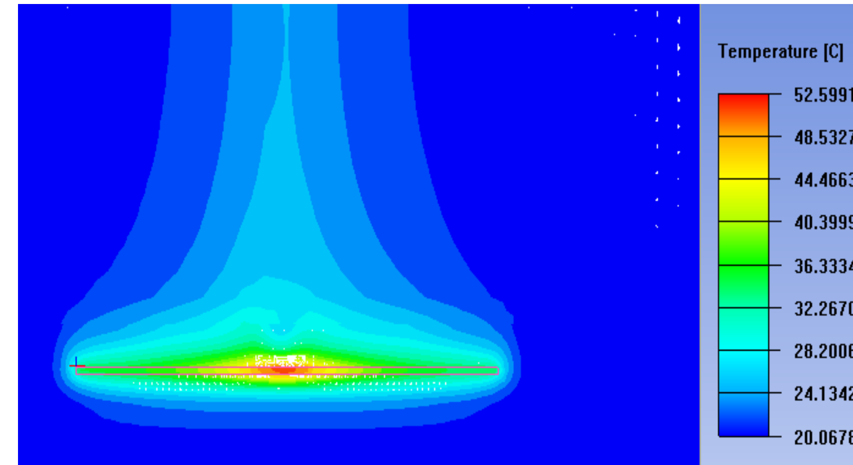





RDL Bottom Layer

# EVB Steady State Results

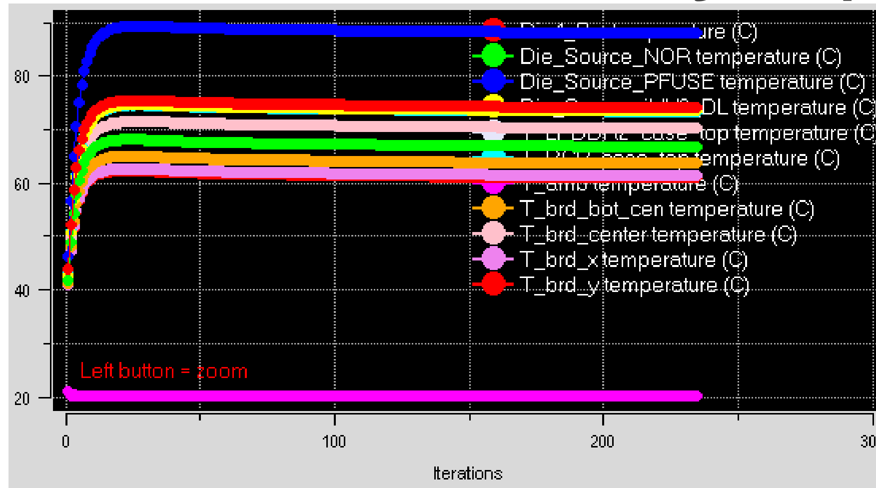


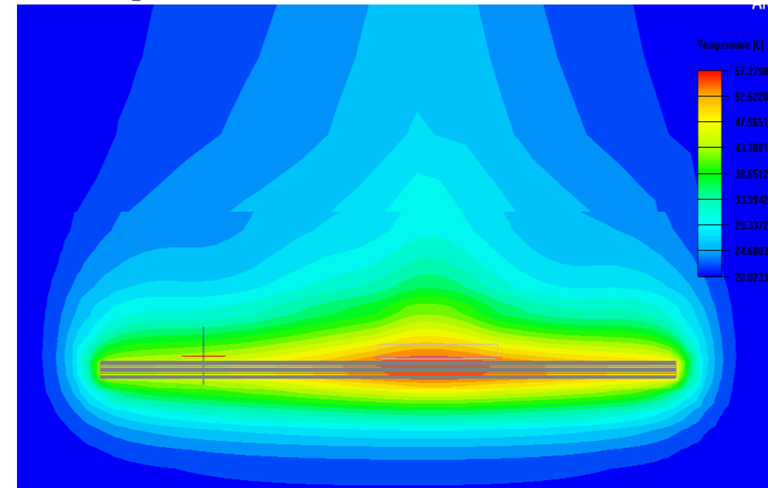




- Board Center (Just Under Package) ~ 70.1 degC
- LPDDR2 (Max temperature of 4 dies) ~ 72 degC
- Die iMX6_DL ~ 78.3 degC
- Die PF100 ~ **81.8** degC
- Die SPI_NP25Q ~ 60.3 degC
  - Simplistic assumption for RCP substrate based on earlier models & Jedec 2s2p board (100x100x1.6 mm) used.

Ambient temperature ~ 20 degC

# Steady State Results – 12 layer (Rev 0)



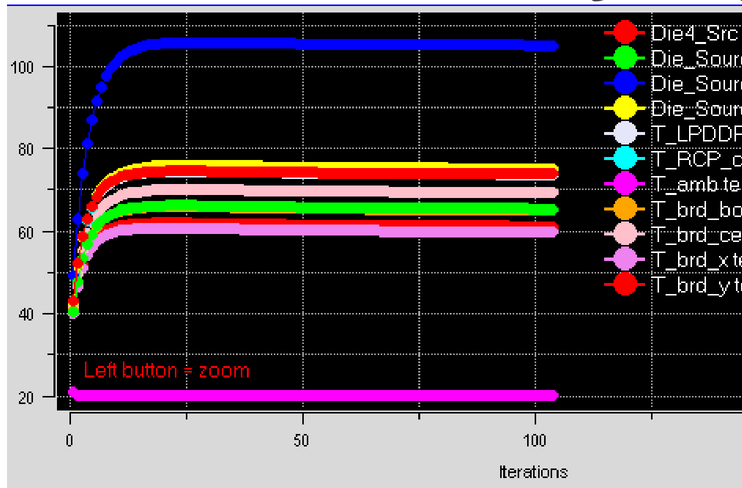
- Board Center (Just Under Package) ~ 70.23 C
- Board Center Bottom Center ~ 63.65 C
- LPDDR2 (Max temperature of 4 dies) ~ 74.07 C
- Case Top (LPDDR) ~ 74.0 C
- Die iMX6 ~ 73.45 C
- Die PFUSE ~ **88.0** C
- Die NOR ~ 66.8 C

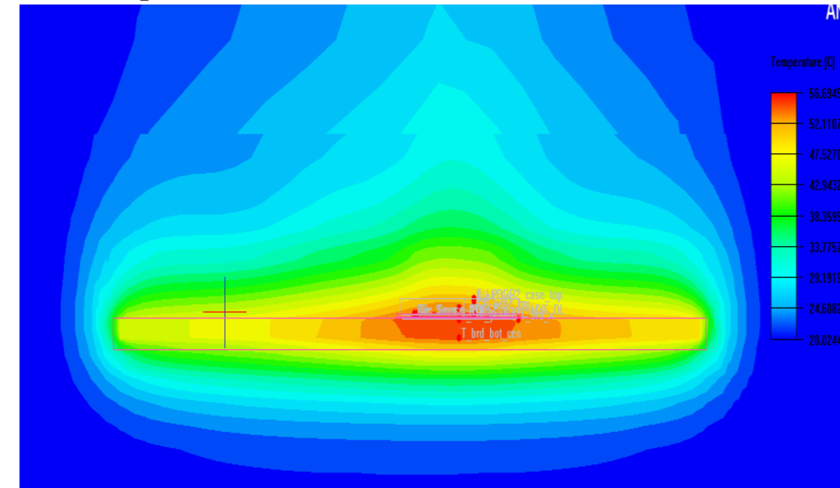
Total power dissipation = 2.96 W (peak)

Ambient temperature ~ 20 C

Detailed ECAD model both for RCP and board used

# Steady State Results – 6 layer (Rev 1)



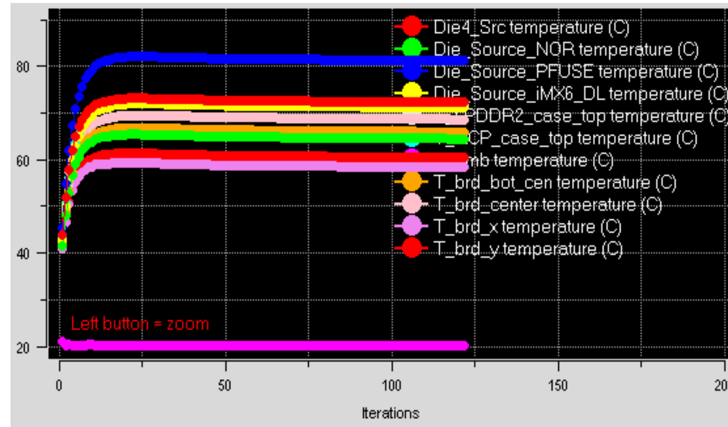
- Board Center (Just Under Package) ~ 69.4 C
- Board Center Bottom Center ~ 65.12 C
- LPDDR2 (Max temperature of 4 dies) ~ 73.8 C
- Case Top (LPDDR) ~ 73.7 C
- Die iMX6 ~ 75.2 C
- Die PFUSE ~ **105.0** C
- Die NOR ~ 65.3 C

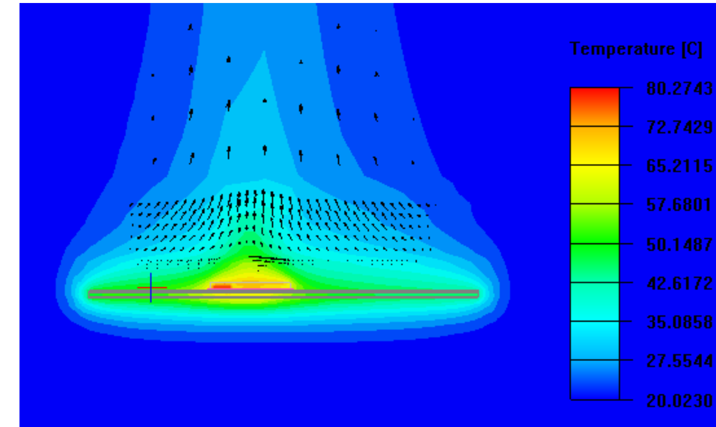
Total power dissipation = 2.96 W (peak)

Ambient temperature ~ 20 C

Detailed ECAD model both for RCP and board used

# Steady State Results – 6 layer (Rev 2)




- Board Center (Just Under Package) ~ 68.6 C
- Board Center Bottom Center ~ 65.9 C
- LPDDR2 (Max temperature of 4 dies) ~ 72.3 C
- Case Top (LPDDR) ~ 72.2 C
- Die iMX6 ~ 71.2 C
- Die PFUSE ~ **81.2** C
- Die NOR ~ 64.5 C

Total power dissipation = 2.96 W (peak)

Ambient temperature ~ 20 C

**Detailed ECAD model both for RCP and board used**

# Thermal Design Guideline

- Allocate enough plated through vias around PMIC and IMX6D’s GND and power balls.

- Use as many layers as possible.

- If lower count layer board stack up is desired, use 1OZ copper for Power and GND plane to alleviate thermal dissipation

- Layout with good power and GND plane for good heat conduction and dissipation.

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