FTF 2016
TECHNOLOGY FORUM

MAC57D5XX FOR HUMAN MACHINE INTERFACE

FTF-AUT-N1803

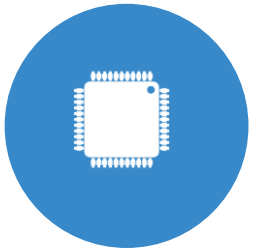
MATHIEU CLAIN
PRODUCT MARKETER
FTF-AUT-N1803
MAY 18, 2016

AGENDA

- Market Overview
- Value Proposition and Key Differentiators
- Product Enablement
- Technical Details
- Summary

Safe and Secure Instrument Clusters and Displays Management

- Targeting cluster market using single & dual high resolution with HUD
- Consumer demand for cutting-edge quality graphics
  - High performance graphics with low memory footprints.
- Larger single or dual high-resolution graphics displays with mechanical gauges and heads up display for increased user awareness
  - Single chip solution with optimized multicore architecture.
- Integrated safety & security is required within today's cyber-security
  - Compliance with ISO26262 / IEC61508 and with Hardware Security



MAC57D5xx Processor Target Application

Automotive

- Instrument clusters
- Heads-up display
- Multifunction display

Industrial

- Human machine interface
- Control gages and displays

Medical

- Safe display with content integrity verification

MAC57D5xx Key Differentiators

Performance Architecture

Multi-core for Application and Real-Time

Cortex®-M4 for real time applications and A5 for applications and HMI

Cortex-M0+ for I/O control and stepper motor drivers with stall detect

Functional Safety & Security

ISO-26262/IEC-61508 Functional Safety (ASIL-B/ SIL2)

Cryptography service engine with AES128

Large Memory for flexibility and future proofing

FlexECC on GRAM

QuadSPI and DDR/SDRAM for Flash & RAM expansion

Support for Execute-In-Place (XIP) from Flash

High Quality Graphics

Vivante 2D GPU OpenVG1.1

Needle animation, fonts & textures

Low memory footprint drivers

2D - Animation & Composition Engine

Some cases as much as 90% reduction in memory usage

CPU overhead reduction with H/W accelerators

Display content integrity verification

On the fly HUD Warping Engine

Reduce memory usage

Releases GPU bandwidth

Reduce hardware implementation cost

MAC57D5xx Block Diagram and Features

Cortex-A5 Application Processor

NEON MPE, 2x precision FPU, MMU

Cortex-M4 Vehicle Processor

64 KB TCM; 1x precision FPU

Cortex-M0+ I/O Processor

Intelligent Stepper Motor Drive, Low power mode peripheral management

System Memory

MPU, 4 MB flash w EEPROM emulation and 1 MB SRAM w ECC, 1.3 MB GRAM w FlexECC

Expendable Interface

2x Dual Quad SPI, SDR and DDR serial flash, DRAM controller supporting SDR and DDR2

Graphics Features

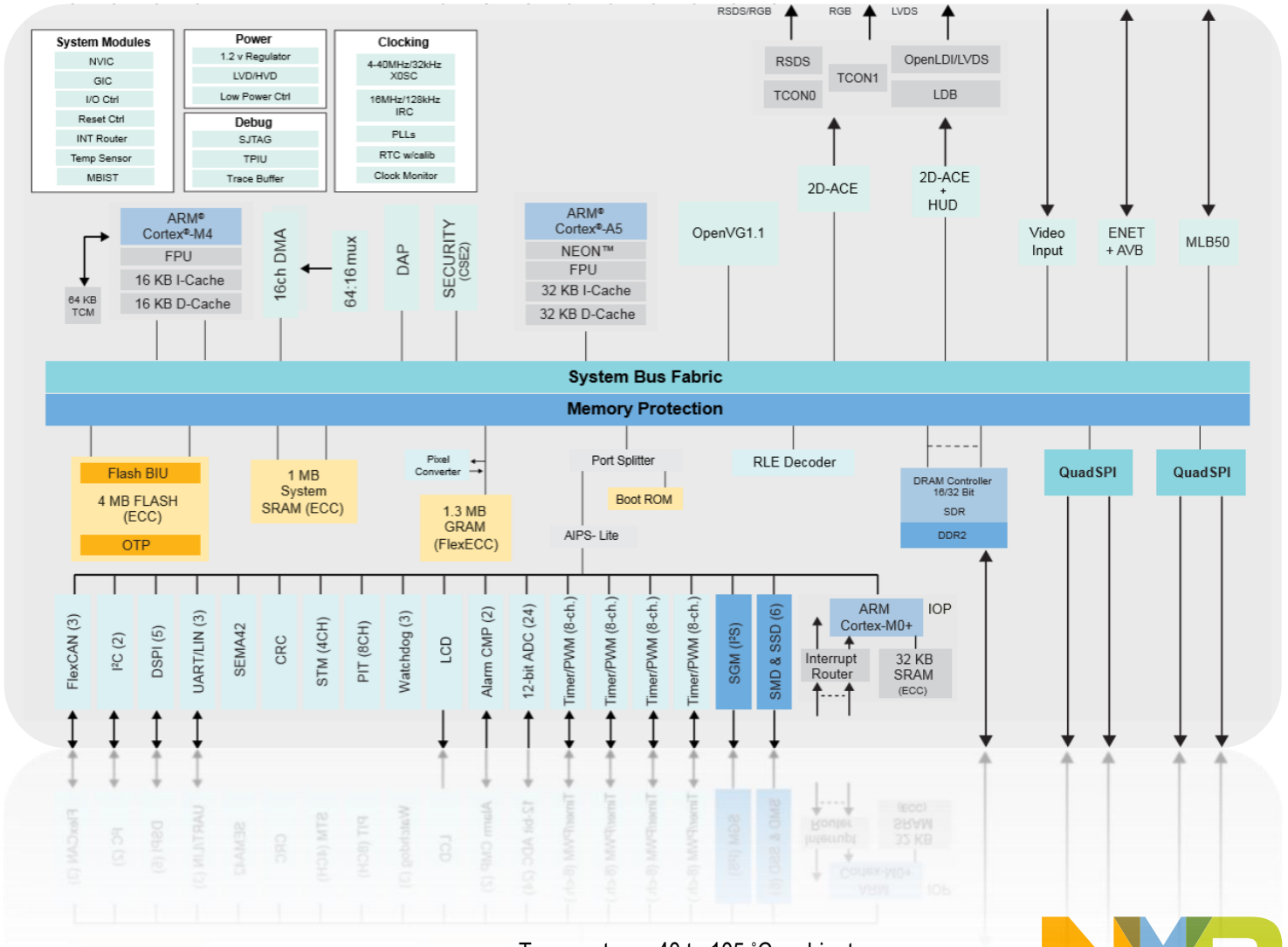
Vivante GC355 GPU, OpenVG, 2 x 2D-ACE, HUD warping engine, Digital RGB, Digital Video Input, RLE Decoder

Functional Safety and Security

ISO 26262 ASIL B, Cryptographic Service Engine

Featured Peripherals:

6x SMD with stall detect, Ethernet 10/100 + AVB, SGM, Autonomous real time clock



Temperature: -40 to 105 ˚C ambient
Packages: 516 MAPBGA, 208 LQFP
NXP.com/MAC57D5xx

MAC57D5xx Enablement

NXP: Sound Generator Module, IOP/Stepper Motor, Stepper Motor Stall Detect

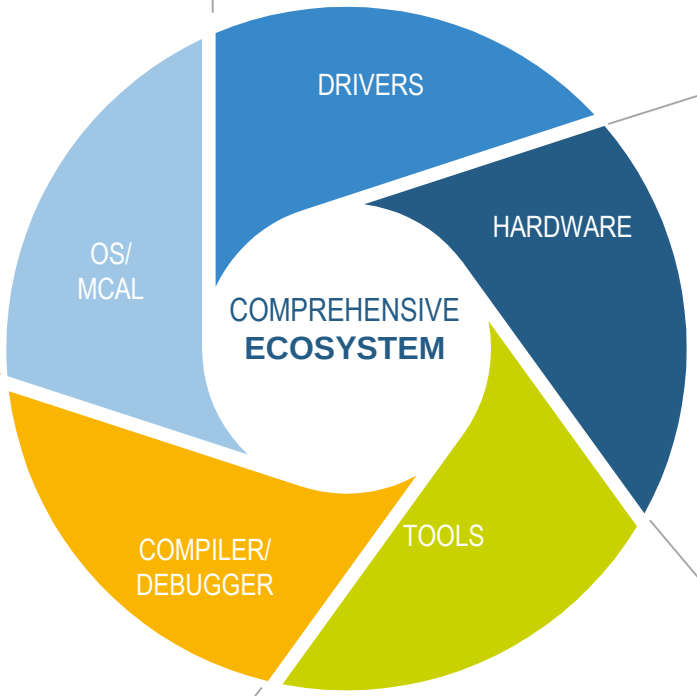
MQX Libraries: Multi-Core Communication Library, Embedded MS-DOS file system, Real-Time TCP/IP Communication Suite, OpenVG, TinyUI, Shell interface library

MQX Drivers: Cores, Interrupt controllers, Clocks, Memory, External Interface, DMA, 2D-ACE, TCON, RSDS, OpenLDI, LVDS, GPU, CAN (FD), I2C, LINFlex, SPI, 10/100 Ethernet+AVB, 12 bit ADC, PIT and FTM timers, Ethernet PHY, SDRAM Memory

MQX BSP (Cortex-A5, Cortex-M4)

Green Hills Integrity (Cortex-A5)

AUTOSAR OS and MCAL (Cortex-M4)



Mother Board:
MAC57D5-EVB

Daughter Card:
MAC57D5-208
MAC57D5-516

Reference Design:
Instrument Cluster Demo Design

Compiler
NXP S32 Design Studio, Green Hills, WindRiver, IAR, ARM

Debugger
Lauterbach, P&E Micro, Green Hills Probes

User Interface Design
Altia, ElectroBit, Crank

Flash Programming
P&E Cyclone Pro, Promik

MAC57D5xx Ordering Part Number

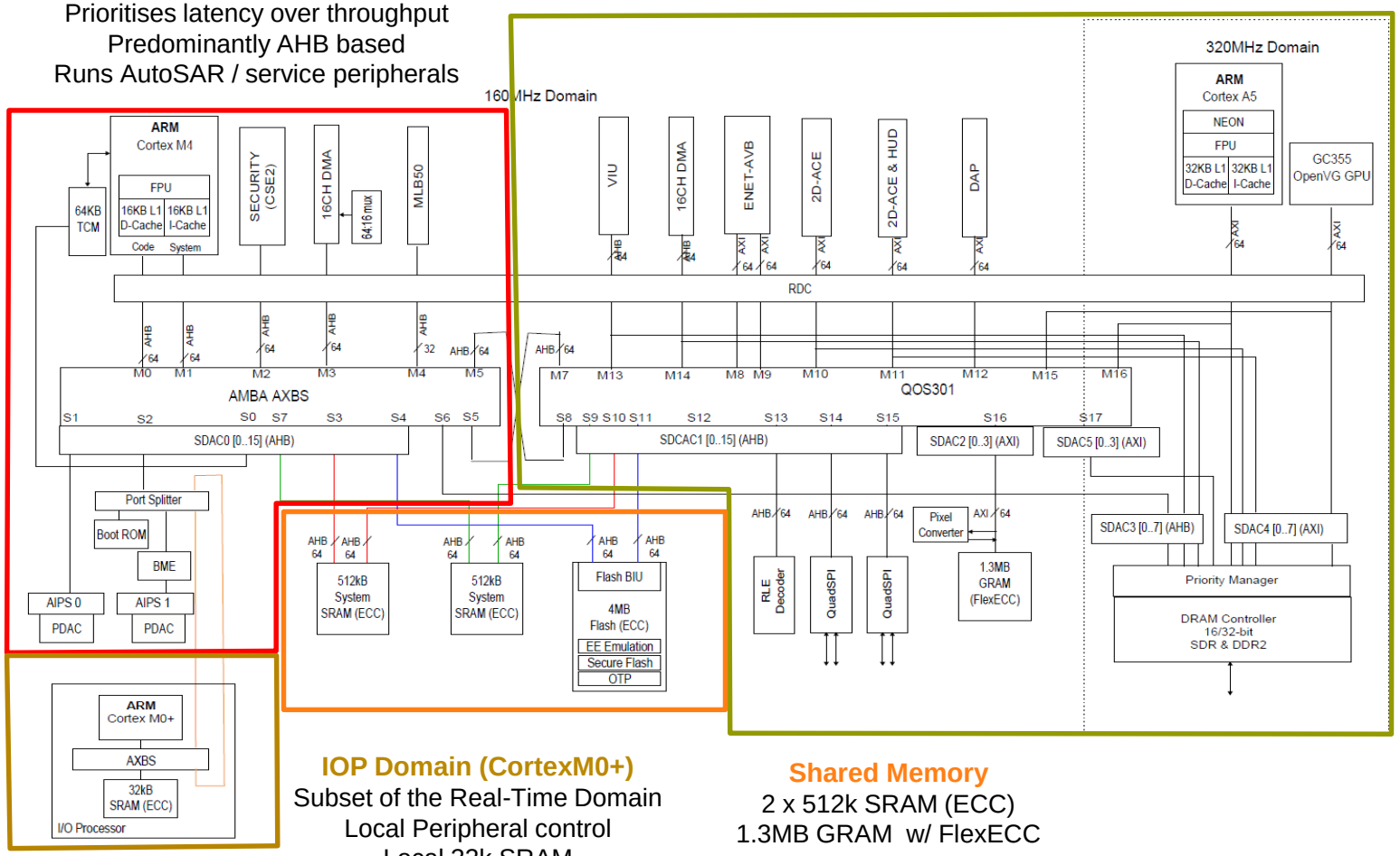
	Nomenclature	Description	Price	Availability
Silicon	SAC57D54HCVMO	4MB DDR2 516BGA	-	March 2016
	SAC57D54HCVLT	4MB SDR 208LQFP	-	March 2016
	SAC57D53MCVMO	3MB DDR2 516BGA	-	March 2016
	SAC57D53MCVLT	3MB SDR 208LQFP	-	March 2016
	SAC57D52LCVLT	2MB SDR 208LQFP	-	March 2016
Evaluation Board	MAC57D5-EVB	Mother Board	$500	March 2016
	MAC57D5-208	Daughter Card for 208LQFP	$250	March 2016
	MAC57D5-516	Daughter Card for 516BGA	$350	March 2016

PLATFORM ARCHITECTURE

MAC57D5xx Architecture

Application Domain (CortexA5)
Prioritises throughput over latency
Predominantly AXI based
Runs Graphics application

Real-Time Domain (CortexM4):
Prioritises latency over throughput
Predominantly AHB based
Runs AutoSAR / service peripherals



IOP Domain (CortexM0+)
Subset of the Real-Time Domain
Local Peripheral control
Local 32k SRAM
Low power operation : IOP mode

Shared Memory
2 x 512k SRAM (ECC)
1.3MB GRAM w/ FlexECC

- **Cortex-M4 *Vehicle* Processor**
  - 1.25DMIPS/MHz : 160MHz operation
- **Cortex-A5 *Application* Processor**
  - 1.57DMIPS/MHz: 320MHz operation
  - NEON SIMD
  - Memory Management Unit
- **AMBA AXBS & QOS301 Bus interconnect**
  - Mixed AXI/AHB
  - xRDC Memory Protection
- **I/O Processor**
  - Cortex-M0+
  - Intelligent Stepper Motor Control
  - Low power mode controller
- **Graphics Features**
  - 2 x 2D-ACE display controllers
  - GC355 OpenVG 1.1 GPU
  - GC255 Raster/Vector GPU
  - Digital Video Input
  - 1.3MB Graphics SRAM
- **Shared Embedded Memories**
  - 4MB Embedded Flash
  - 1MB System SRAM
- **Dual DDR QuadSPI Flash expansion**
- **16-bit SDR / 32-bit DDR2 DRAM options**

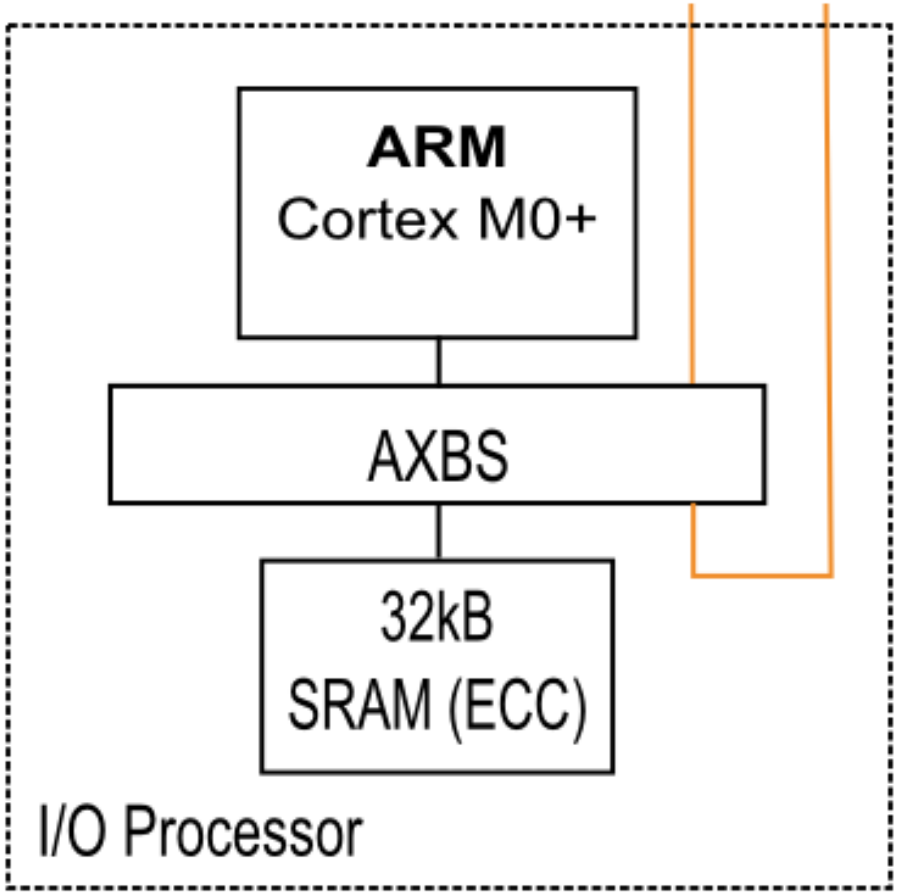
I/O Processor Features

Overview

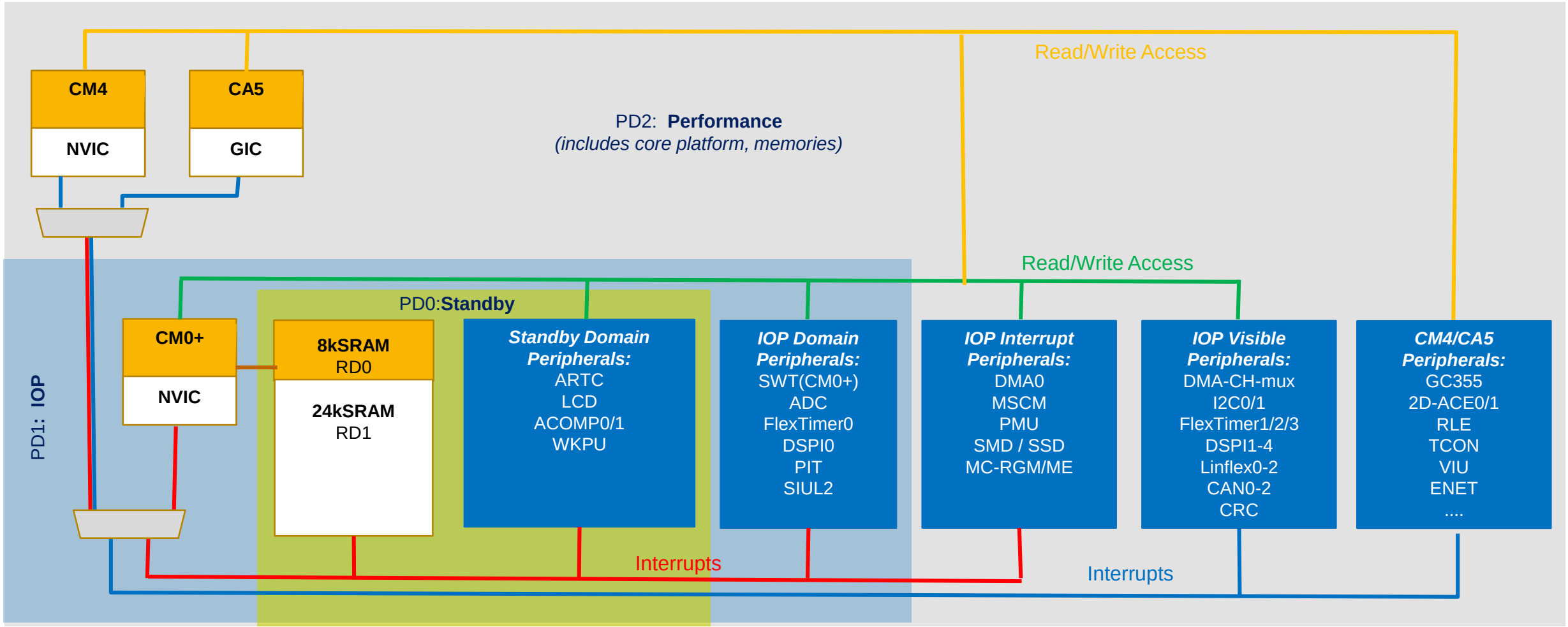
- Reduces main CPU workload and interrupt load
- Shared SRAM / registers for motor parameters
- Dedicated 32 KB SRAM ECC
  - Memory mapped for CA5/CM4
  - Serves as system standby RAM

Enables Intelligent Peripherals

- Autonomous stepper motor drive
- Available to other system peripherals
- Available in low power ‘IOP’ mode



I/O Processor Peripheral Access / Power Domains



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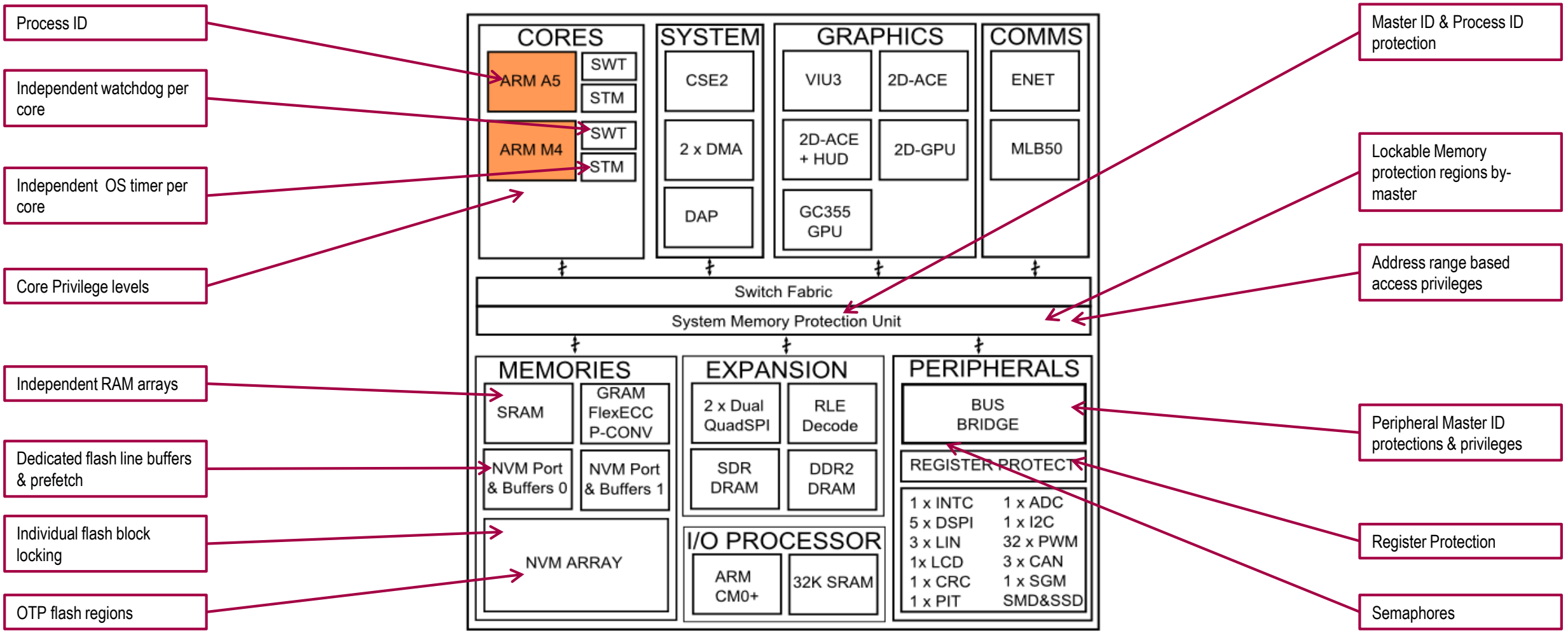
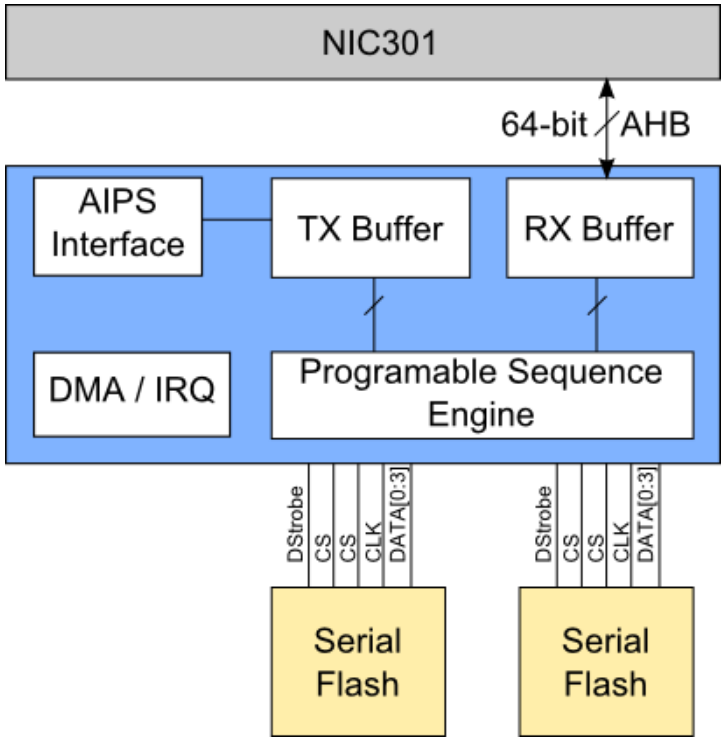
Multi-core Application Independence



MEMORY EXPANSION

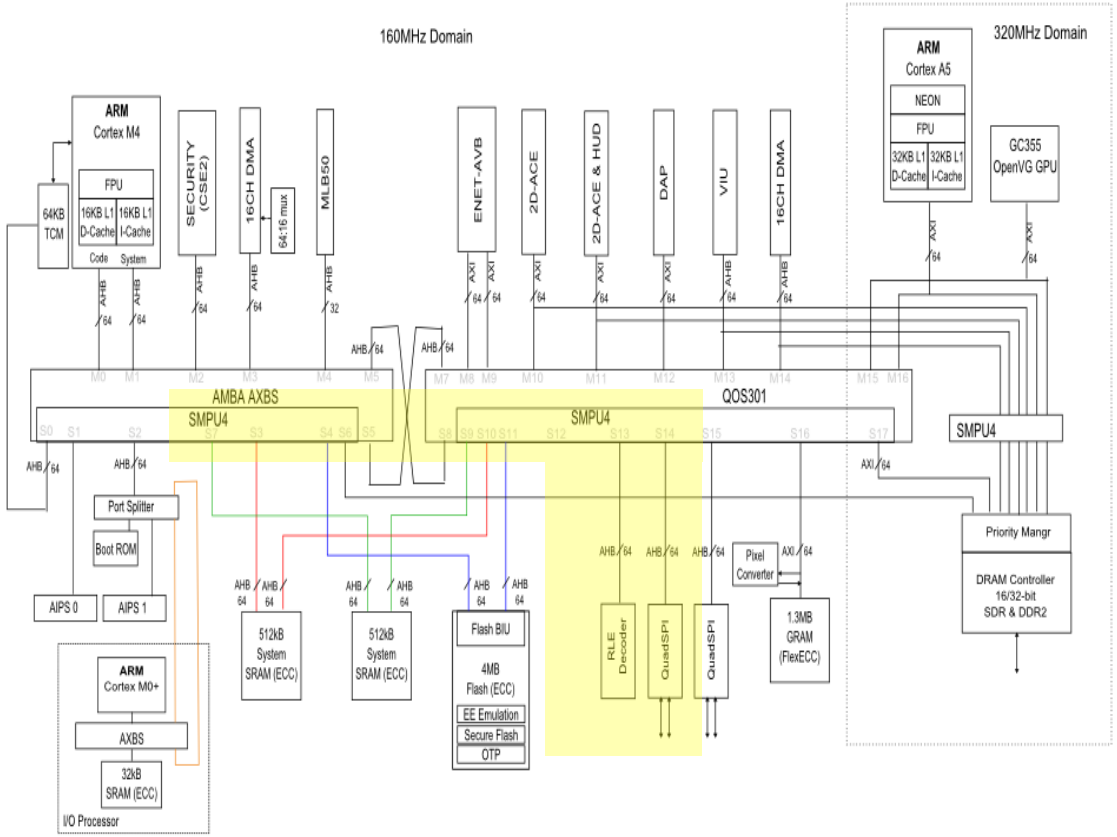
QuadSPI Serial Flash Controller

- Dual QuadSPI architecture supports:
  - 2 external Serial Flashes per QuadSPI module
  - SDR and DDR Serial Flash
  - Programmable Sequence Engine for compatibility to any Serial flash
  - Supports XIP: Code Flash Expansion
- QuadSPI can control 2 x 4-bit serial flashes:
  - Sequential addresses or….
  - Parallel mode enabling ‘octal flash’ with data recombination internally in QuadSPI
- Up to 100MHz DDR x8 => 200MByte/sec peak bandwidth
- Flexible Buffering Scheme:
  - Sub-buffers allocated to specific masters.
  - Master prioritisation
  - Pre-fetch capability
  - Suspend & resume for lower priority masters



DRAM Controller

- Supports SDR and DDR2 DRAM interfaces:
  - 16/32bit DDR2 (320MHz) in BGA516
  - 16bit SDR (160MHz target) in 208QFP/BGA516
- Direct access of CA5, GPU and graphics masters to DRAMC bypassing the QoS301
- Access controlled by local Priority manager



GRAPHICS

Overview

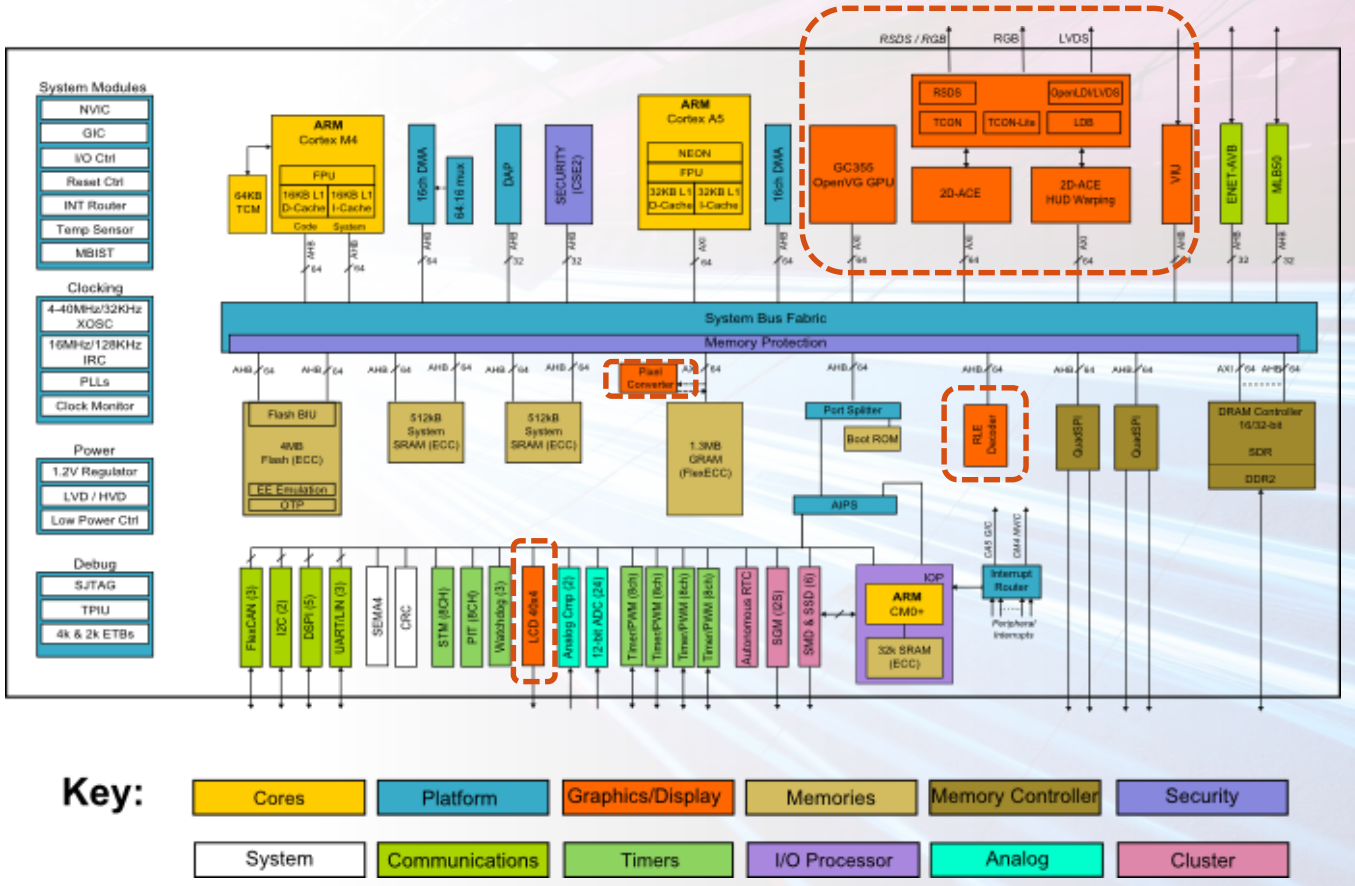
The graphics sub-system consists of

- 2 x 2D-ACE
- GPU (open VG1.1 GC355)
- VIU
- OCRAM Pixel Converter
- RLE
- LCD

+

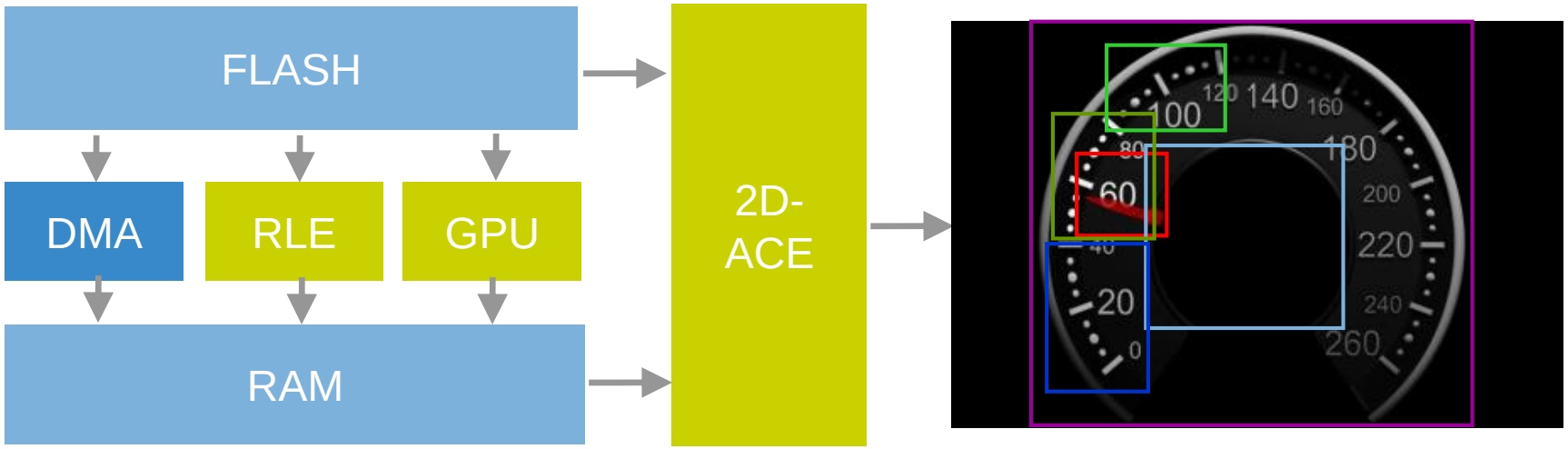
Inline HUD Warping

TCON, RSDS, OpenLDI/LVDS

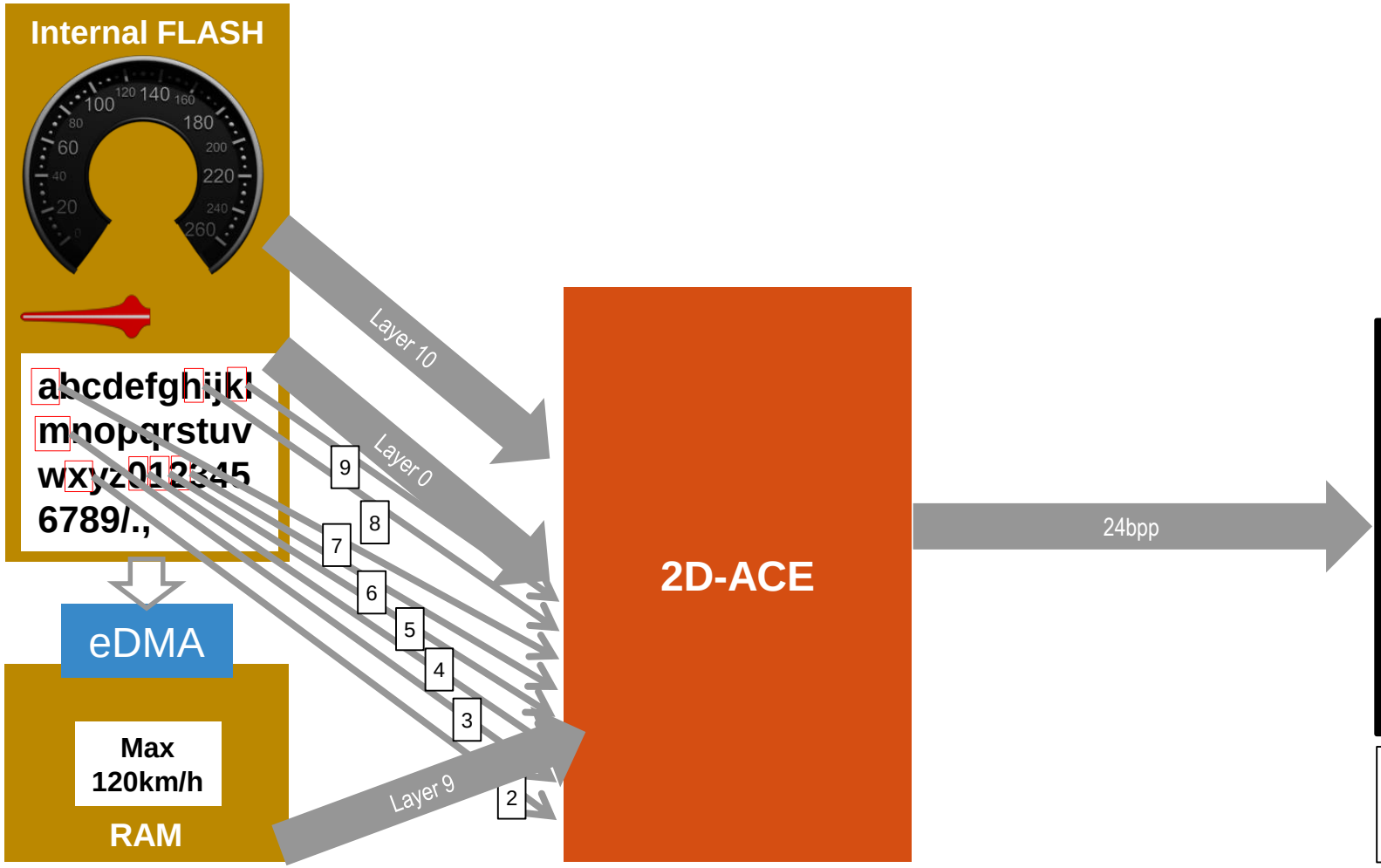


2D-ACE: Acceleration Composition Engine

- Real time, un-buffered screen composition
- Multiple color formats, optimized for high quality and low memory footprint
- Hardware-accelerated sprite animation, object, alpha, position, color key, scroll
- Automatic, synchronized and high latency-tolerant: needs very little CPU time



How does the 2D-ACE renders a frame?



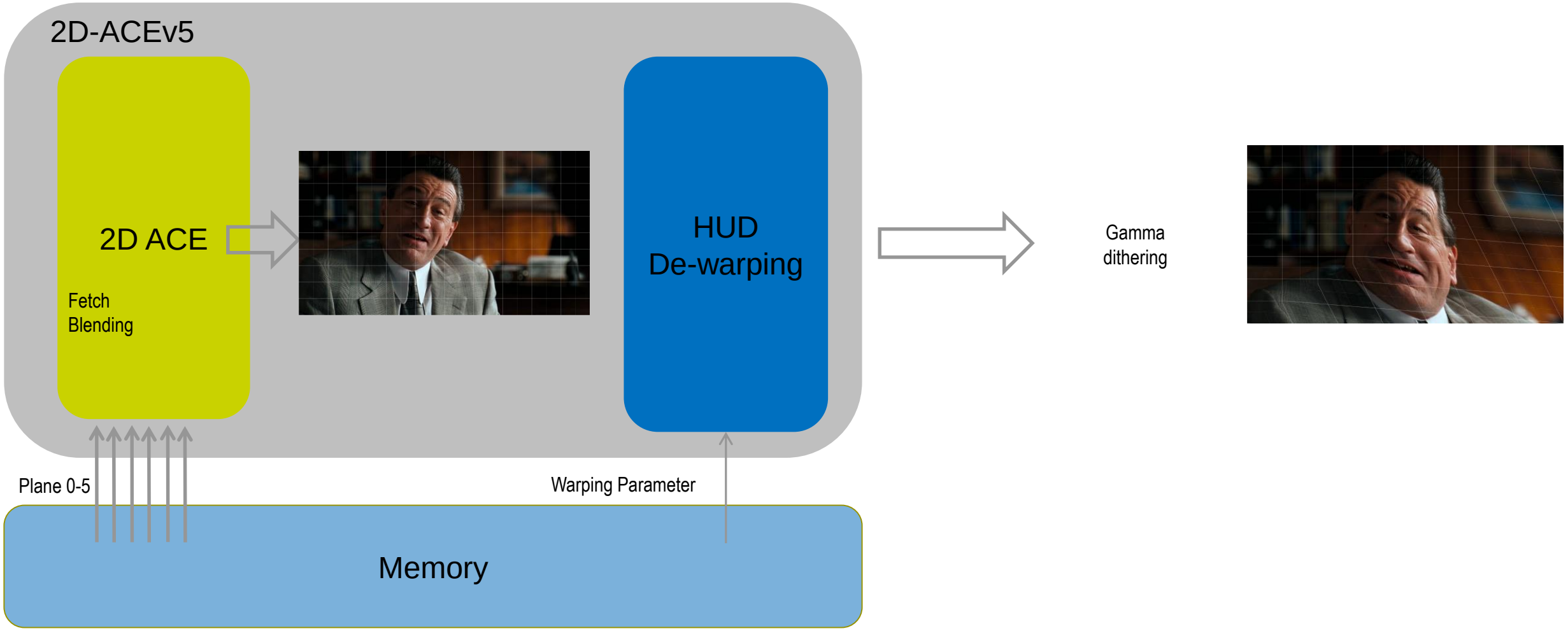
Object	Size
Speedometer	200x200 8bpp
Needle	120x20 8bpp
ascii font set	400x400 4bpp
text box max speed	60x40 4bpp

Total RAM used: 1200 bytes

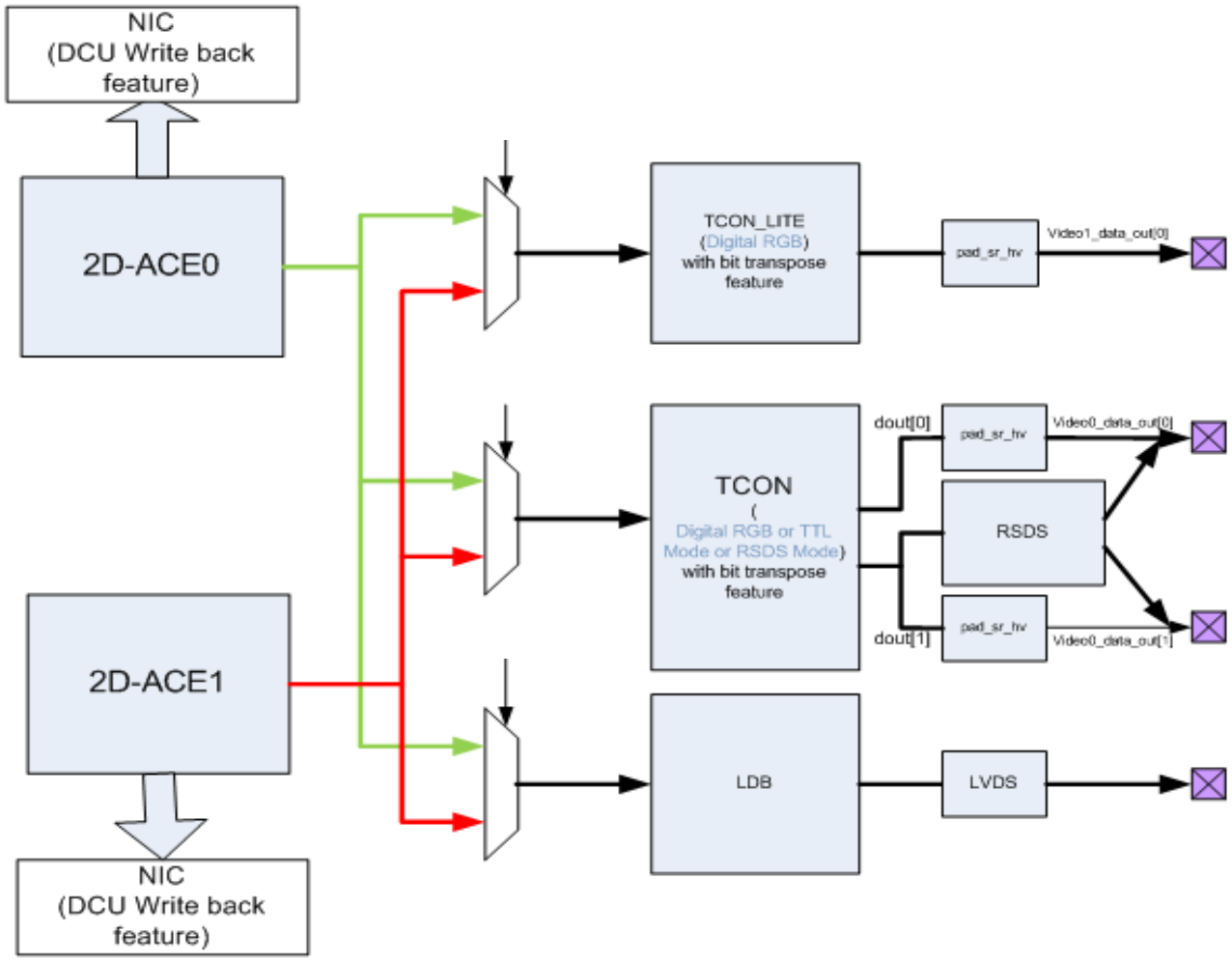
Total Flash used: 122400 bytes

480x272 24-bit screen
(would require ~400,000B buffer)

HUD Warping


2D-ACEv5
2D ACE
Fetch
Blending
HUD
De-warping
Gamma
dithering
Plane 0-5
Warping Parameter
Memory

Display Output Options



2D-ACE0(HUD)	2D_ACE1
Digital RGB	Digital RGB
Digital RGB	RSDS+TCON
Digital RGB	LVDS
RSDS+TCON	Digital RGB
RSDS+TCON	LVDS
LVDS	Digital RGB
LVDS	RSDS+TCON

GC355 Vector Graphics Engine

- Independent 2D Vector GPU Use-cases:
  - Instrument cluster: 2D engine accelerates needles at 60fps; 2D-ACE renders the rest of the scene
- Infotainment: UI acceleration
- Native rendering of true-type fonts, with 16x Anti-Aliasing
- Additional graphics acceleration for dual display systems

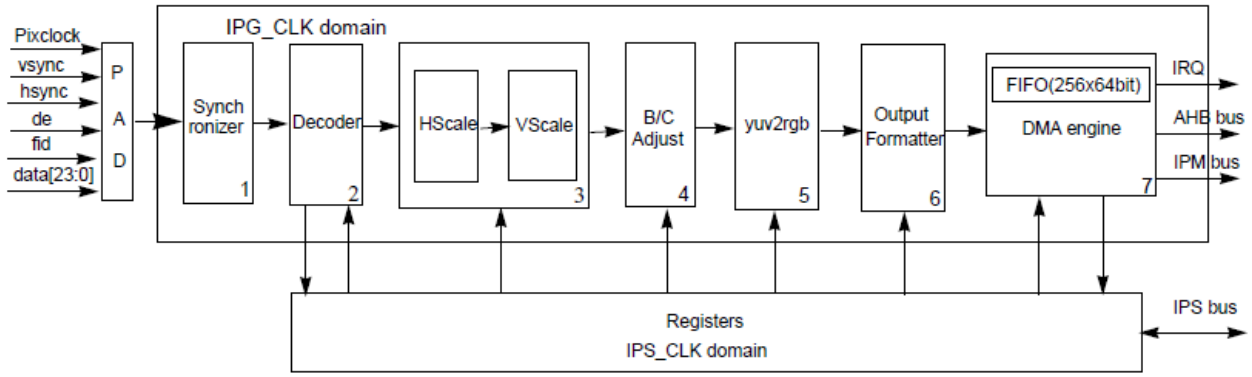
GC355 VGMark Performance @ 320MHz

GC355	VGA resolution 16X AA (Frames/sec)
	320MHz (projected)
Tiger (rotation)	85
UI	96
Navigation	28
Flash	42

Video Interface Unit (VIU4)

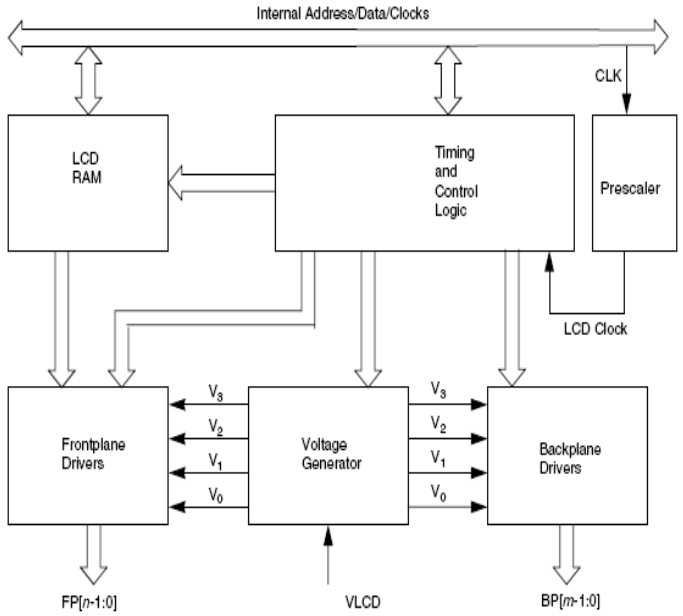
- QVGA to XVGA input/output resolution
- Brightness and Contrast Adjustment
- Up to 1/8th video down-scaling
- Up to 2x horizontal video up-scaling
- Horizontal Mirroring
- DMA for direct copy to system memory

Input Formats	Output Formats
ITU-R BT.565 Parallel RGB888/666/565 Serial RGB888 (3 cyc) Monochrome	8bpp, 16bpp, 32bpp 8bpp monochrome YUV422 YUV444



LCD Segment Controller

- Up to 40 front-plane drivers
- Up to 8 back-plane drivers
- Remapping of backplane drivers
- Programmable frame clock generator
- Programmable bias voltage level selector
- Programmable output current
- Optional output current boost during transitions.
- Optional LCD frame frequency interrupt event
- Contrast adjustment

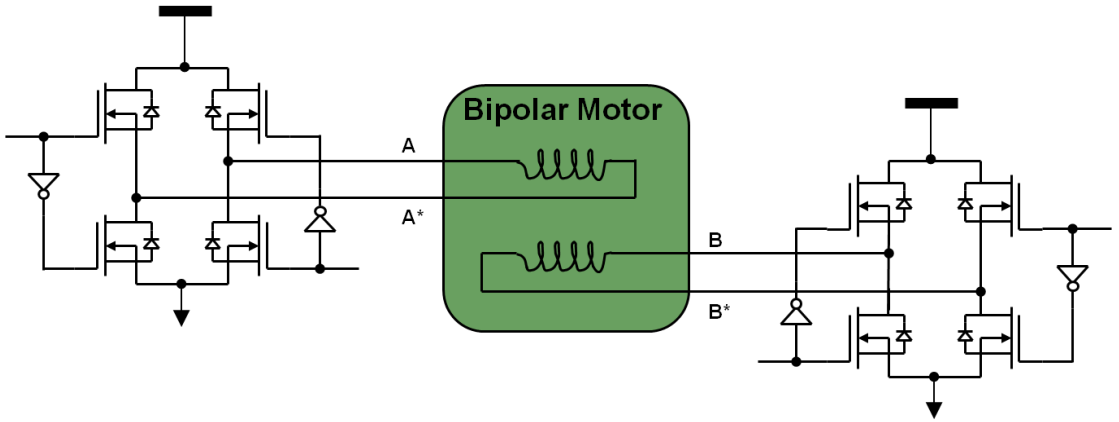


CLUSTER

Instrument MCU Motor Drivers Description

6 Independent Motor Drivers

- Two PWM channels per stepper motor
- Two H-Bridge Coil Drivers per Motor
- Channels can be operated in three modes depending on requirements
  - Half H-bridge, Full H-bridge or Dual Full H-bridge
- Integrated Stall Detection
- Unused motors drivers are configurable as GPIO



Sound Generator Module (SGM)

4-channel audio mixer

- Each channel capable of independent Tone generation or Wave playback
- Individual channel volume control (8-bit resolution)

Tone Mode

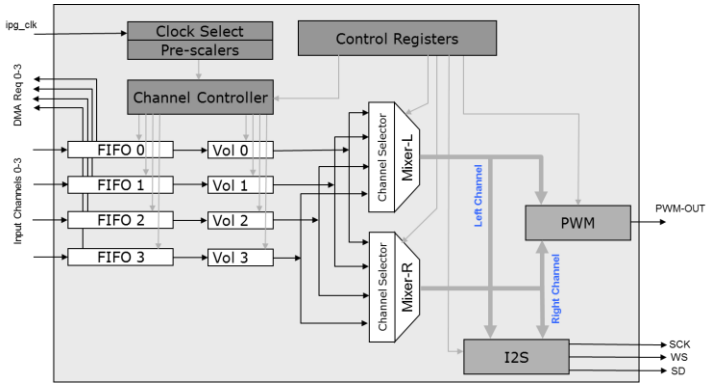
- Programmable Tone frequency
- Programmable amplitude envelope: attack, duration and decay
- Programmable number of tone pulses and inter-tone duration

Wave Mode:

- One FIFO per channel working in conjunction with eDMA
- Supports standard audio sampling rates
- 8bit, 12bit, 16bit input data formats
- Programmable wave duration and inter-wave duration
- Repeat mode with programmable number of wave playbacks

SGM Output:

- 16-bit PWM channel
- Integrated I2S master interface for connection to external audio DAC



COMMUNICATION PERIPHERAL

Ethernet Controller (ENET) Overview

Main Features

- Implements the full 802.3 specification
- HW support for low level protocol management
- IEEE 1588 frame support: Time-stamping, IC/OC
- HW support for Ethernet AVB standard, including multiple RX & TX queues
- Interrupt coalescing
- Traffic-shaping bandwidth distribution
- Statistics indicators for IEEE 802.3 basic and mandatory management information database (MIB) package and remote network monitoring (RFC 2819)

Frequency of Operation

- 10/100Mbps
- Full-duplex and half-duplex operation

PHY Interfaces

- MII, MII-Lite, RMII PHY data interfaces
- MDIO master interface for PHY device configuration and management

Use Cases

Remote Diagnostics

Multimedia Streaming

MLB50

- Interfaces to Intelligent Network Interface Controller (INIC50) via 3 external signals: MLBCLK(I), MLBDAT(I/O), MLBSIG(I/O)
- 3.3V I/O
- The MLB50 module implements a 3-pin interface providing a link to a MOST® data network, using the standardized MediaLB protocol
- Support for up to 16 logical channels and 31 physical channels running at a maximum speed of 1024 Fs
- Transmission of commands and data and reception of receive status when functioning as the transmitting device associated with a logical channel address.
- Reception of commands and data and transmission as receive status responses when functioning as the receiving device associated with a logical channel address.
- MediaLB lock detection
- System channel command handling
- Local channel buffer RAM (Single Port RAM) of 2k x 36-bits accessed

SAFETY AND SECURITY

SafeAssure from NXP

ISO26262 ASIL-B Compliant MCU (IEC61508 SIL2)

- Mature ISO26262 NPI process
  - Safe Assure Program
  - NXP has market proven
  - ASIL-D MCU's in Braking,
  - Powertrain & Radar Applications

- Safety Context
  - Guarantee the integrity of safety critical presentational information
    - Speed, Gear & Tell-tales
  - System Level Safety
    - Mixture of Hardware features & Software Counter-measures
    - Memory BIST, ECC, Dual Core, 2D-ACE Safety Mode, SMPU, LVD
    - ADC Monitoring, PWM Loopback Monitoring

System Level Functions

Safety context describes the system level safety goals and the MCU functions that need to be safety relevant to achieve these goals.

System level safety goals:

- Camera: image frozen (FTTI=500ms)
- Warning indications relating to safety critical systems: (FTTI=1000ms)
  - Red flashing warning tell-tales or audio signals
- Gauges: Wrong value displayed, frozen or corrupt image when screen is used to display value. (FTTI=1000ms)
- Gear selection display: Gear displayed does not match gear selected. (FTTI=1000ms)

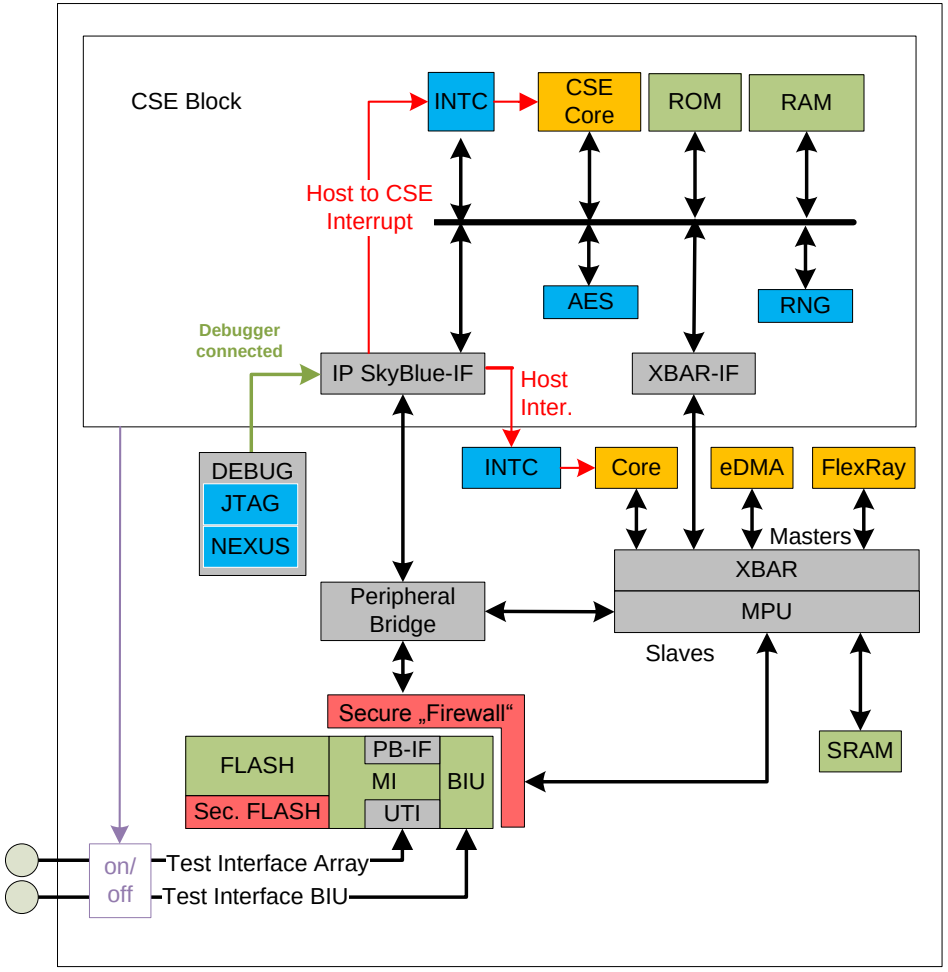
(FTTI = Fault Tolerant Time Interval)

Cryptographic Services Engine (CSE)

CSE: Cryptography service engine

Moves the crypto keys from public memory into the secure memory. Only the CSE can access the keys.

- 32-bit secure core up to 133 MHz
- AES-128
- 120bit Unique ID
- Secure Boot support
- Secure flash blocks assigned to CSE.
- No other masters can access this memory
- PRNG seed generation via TRNG

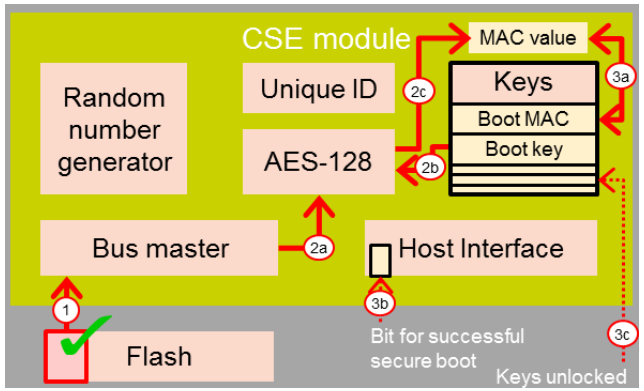


CSE Security Use Cases

Secure Boot

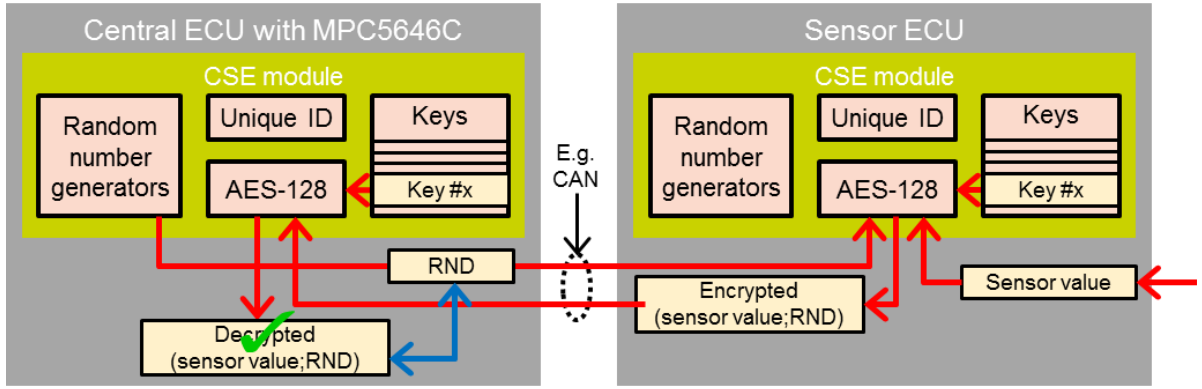
Check Boot Loader for Integrity and Authenticity

1. Check Boot Loader for Integrity and Authenticity
2. CSE module uses the boot key to calculates the MAC value of the bootloader
3. CSE module compares calculated MAC with stored boot MAC. If identical: successful secure boot → set respective bit in host interface and unlock keys
4. MCU always starts bootloader



Secure Communication

1. Central ECU obtains random number and sends it to sensors ECU (e.g., after power-on)
2. Sensor ECU reads sensor value and asks CSE module to encrypt it and the received random number (using key #x)
3. Sensor ECU sends encrypted message to central ECU.
4. Central ECU asks CSE module to decrypt received message (using key #x).
5. Central ECU checks sent random number vs. received/decrypted random number.

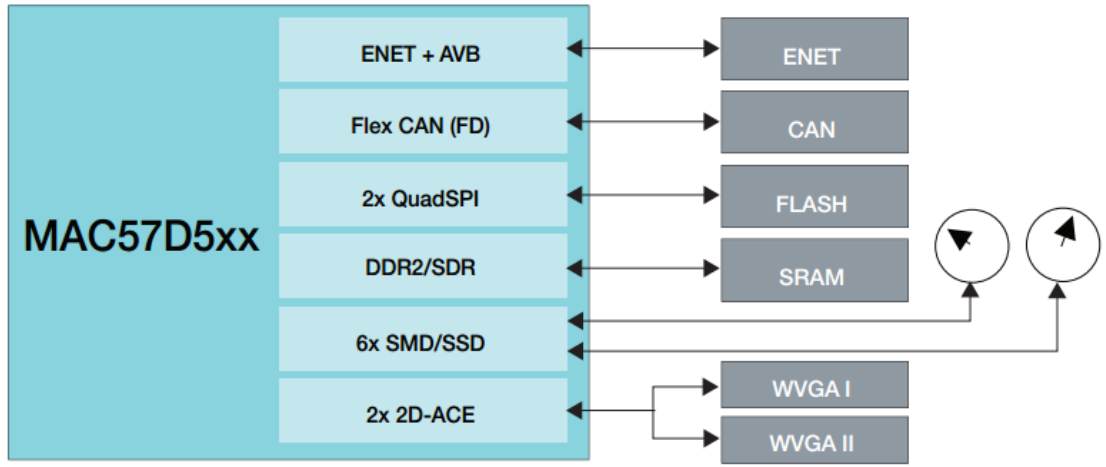


SUMMARY

MAC57D5xx

Multi-Core Graphics Oriented Single chip solution for hybrid clusters

- Dual high-resolution display with high-end graphics
- Integrated stepper motor control with stall detect
- Multi core ARM architecture for power efficiency
- Content integrity verification
- Functional Safety
- Hardware Security



SECURE CONNECTIONS
FOR A SMARTER WORLD

ATTRIBUTION STATEMENT