FTF 2016
TECHNOLOGY FORUM

ADAS PROCESSOR S32V FUNCTIONAL OVERVIEW

FTF-AUT-N1785

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AGENDA

- Introduction
- Device Architecture Overview
- ARM® Cortex®-A53/M4 Overview
- Memory Systems & DDR Controller
- Clocking & Reset
- Power Management
- Boot Up
- Serial Communication (CAN-FD, Ethernet, etc.)
- DMA
- Functional Safety
- Security
- EVB
- Vision & Graphics

INTRODUCTION

S32V Introduction

Safe, Secure & Reliable
Single Chip Solution
ADAS
Vision
Data Fusion

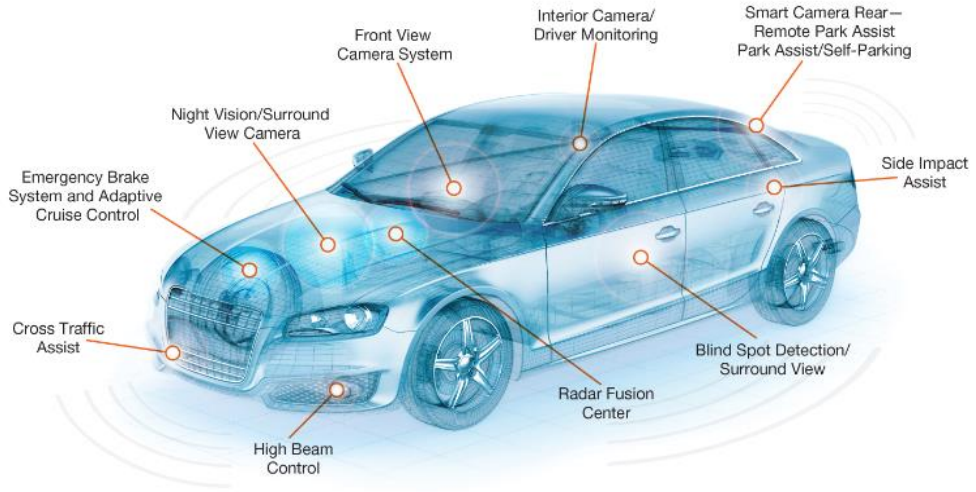
Applications

Front Camera

Rear Camera

360° Surround View

Sensor Data Fusion



ADAS Application Examples:

- Autonomous Emergency Brake (AEB)
- Lane Departure Correction (LDC)
- Pedestrian Protection (PD)
- Sensor Fusion

S32V234:

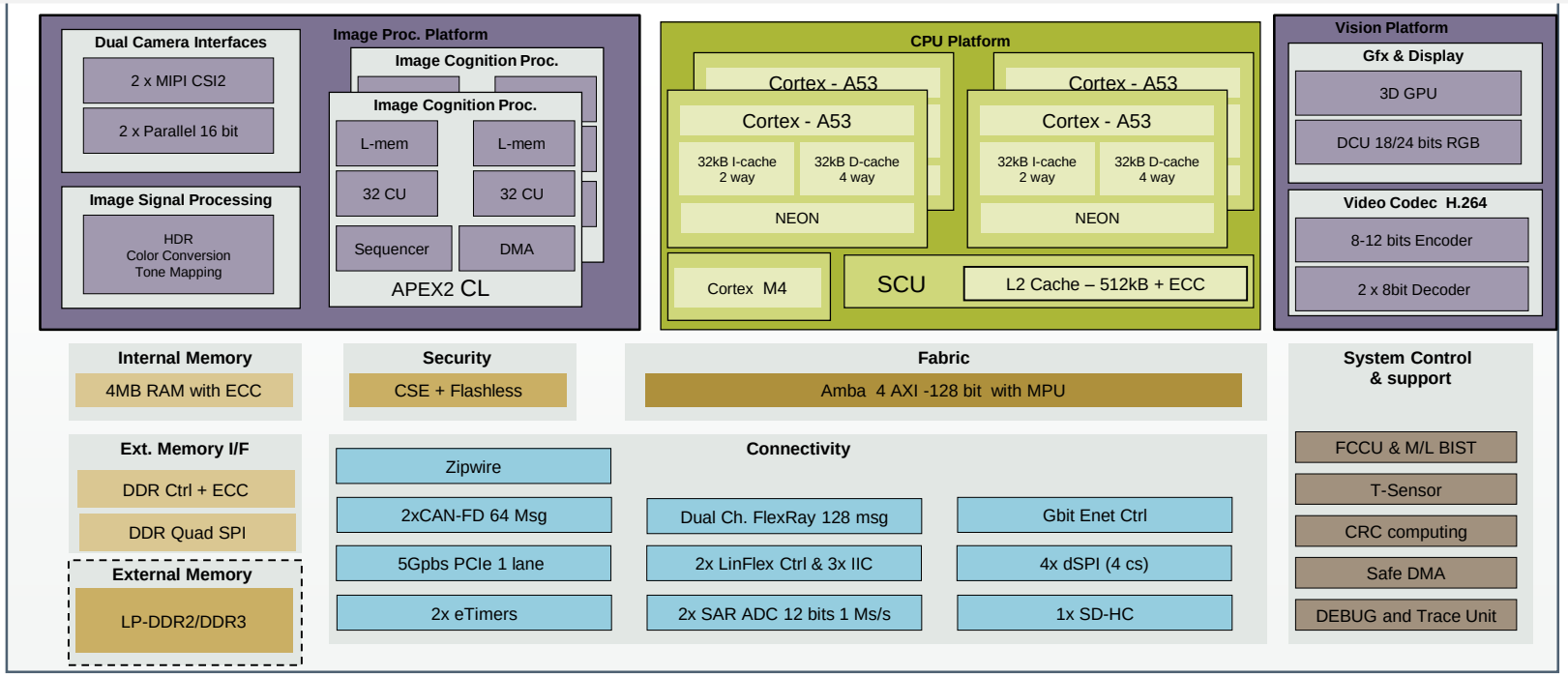
- Fully targeted at ISO26262 ASIL B
- Hardware security encryption (CSE)
- Designed for high performance vs power
- Manufactured *for automotive reliability*

S32V230 Family Options (C, G, K)

	ASIL B	Dual Core	Quad Core	3D GPU	ISP	APEX	Security
Automated Drive Sensor Fusion Many Core ASIL B – D	✓	✓	✓	Optional	N/A	Optional	✓
Surround View Surround Sense and Stitching Many Core ASIL B – C	✓	✓	✓	✓	Optional	✓	✓
Front / Rear Vision Vision NCAP Many Core ASIL B – C	✓	✓	✓	N/A	Optional	✓	✓

DEVICE ARCHITECTURE OVERVIEW

S32V234 Block Diagram



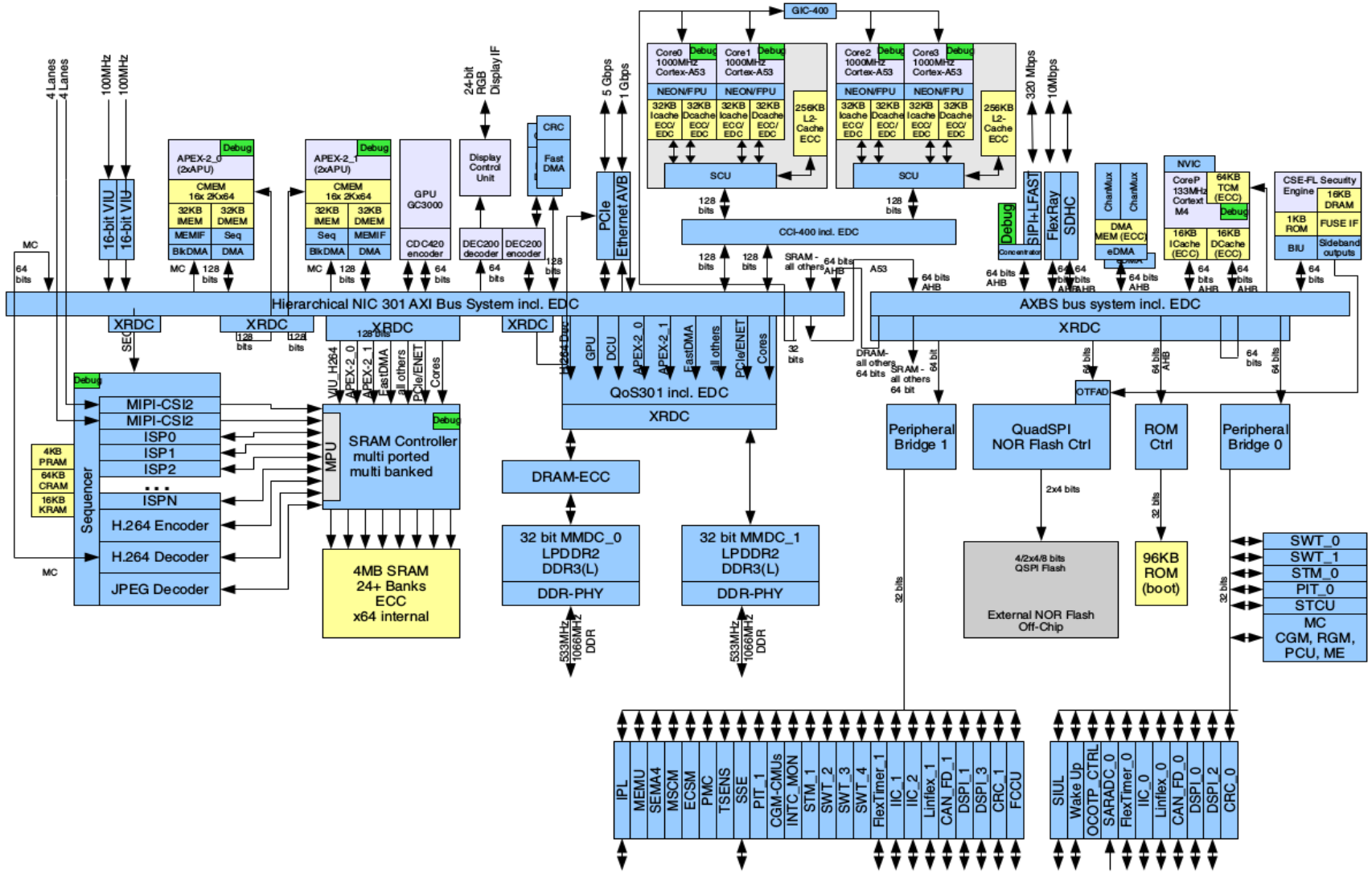
Specifications:

- **CPU1-4:** ARM Cortex-A53 @1GHz, L1/L2 cache with ECC & Neon
- **CPU5:** ARM Cortex-M4 for IO control with I/D Cache and ECC
- **ICP:** 2 x APEX2 CL (MIMD APU-64 CU each) at 400MHz
- **GPU:** GC3000 from Vivante
- **Package:** 17x17**FC-BGA**
- **Temp Range (Ta):** -40 to 105°C, 125 °C Tj, AEC-Q100 Grade 2
- **Main Supply:** 3.3V IO and 0.94V Core - external PMU + DDR rails

Key Features:

- **F. Safety:** developed as per ISO26262 with target ASILB
- **SW Enablement:** OpenCL Tools for ICP, GPU, NEON.
- **Video Codec:** H.264 Encoder (8-12 bit) + Decoder (8 bit)
- **DRAM:** External LPDDR2 & DDR3 supported
- **Security:** SHE (almost) compliant Crypto Security Engine
- **Surround 3D**: 3D unified architecture. 19/38Gflops at 600MHz
- **Video dist. Network**: 2X Mipi CIS2 – 4 Virtual channels each
- **Connectivity**: Gbit Etehrnet, PCIe, FD-Can & Flexray

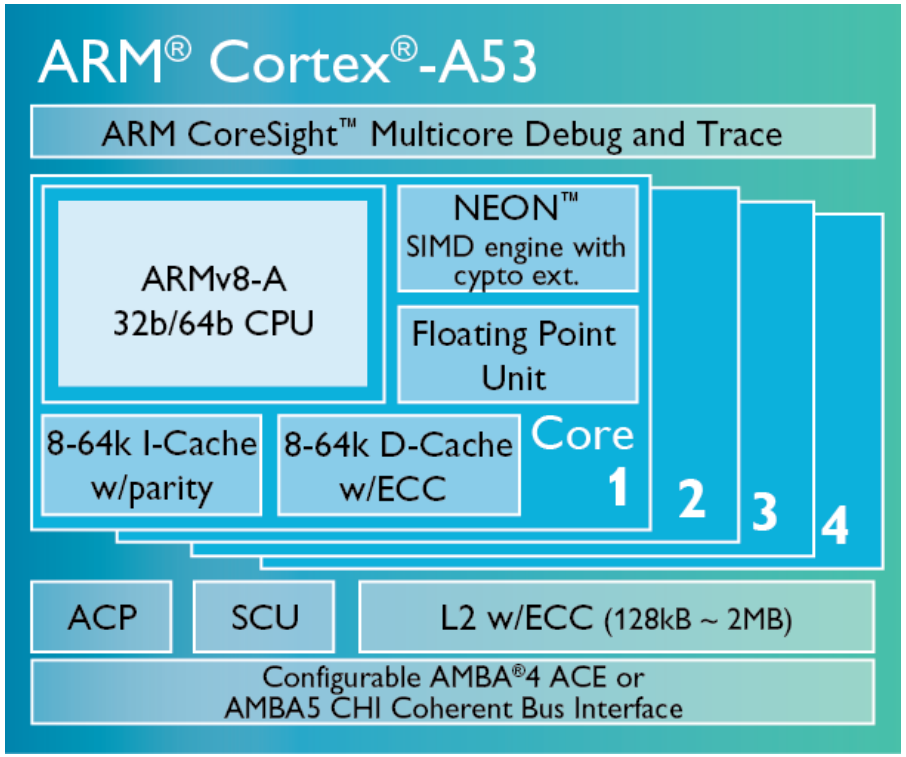
S32V234 Block Detailed Diagram



ARM CORTEX-A53/M4 OVERVIEW

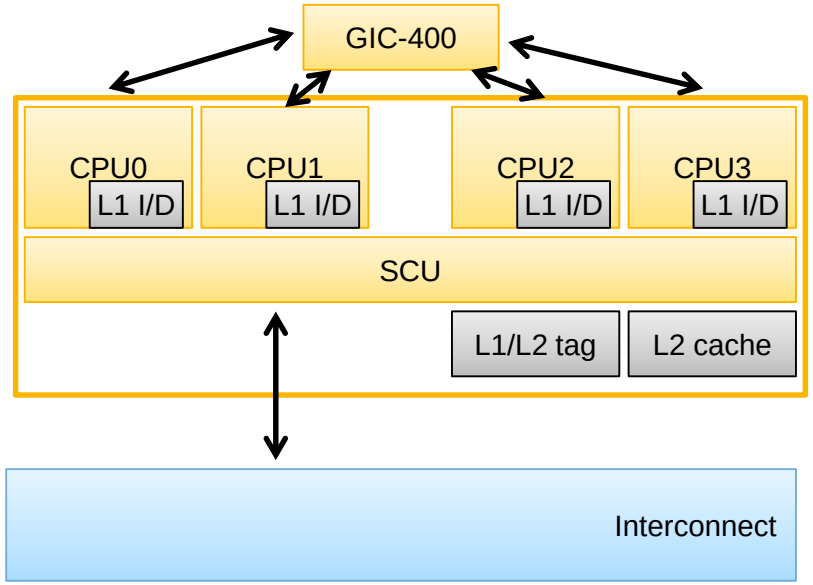
ARM Cortex-A53 x 4

- Operating speed of up to 1 GHz
- ARMv8-A instruction set architecture
- Asymmetric/Symmetric Multi-Processing
- Vector Floating-Point v4 architecture
- In-order 8-stage dual issue pipeline
- 32 KB/32 KB L1 Instruction/Data Cache
- 256KB L2 Cache with ECC protection
- MMU for memory virtualization
- NEON SIMD for vector processing



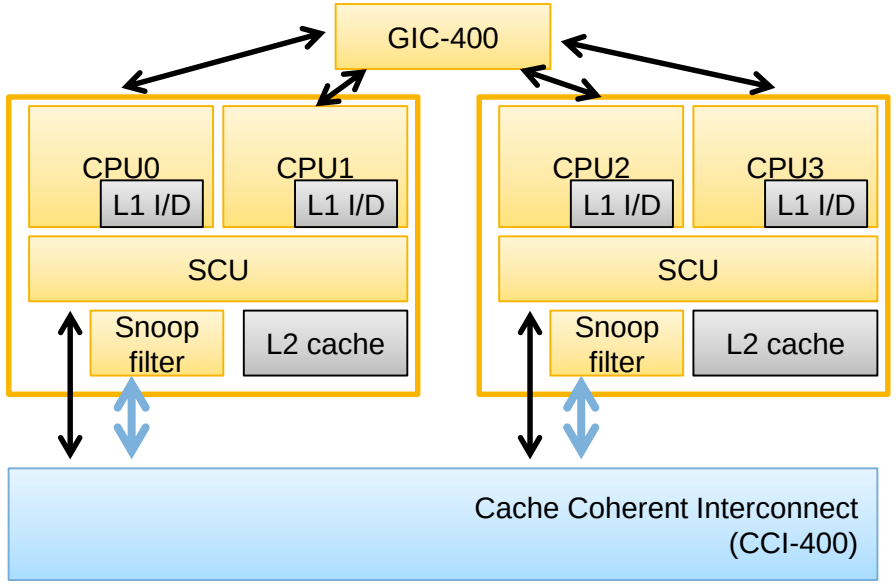
Two processor clusters are connected with a CCI-400 Cache Coherent Interconnect to ensure coherency across the cores

Core Cluster Enhancement



- SCU is a potential for common point failure
- L1/L2 tag RAM & control failures affect all CPUs
- L2 data RAM failures affect all CPUs

L1 I/D Cache of 32K
L2 Cache of 256K



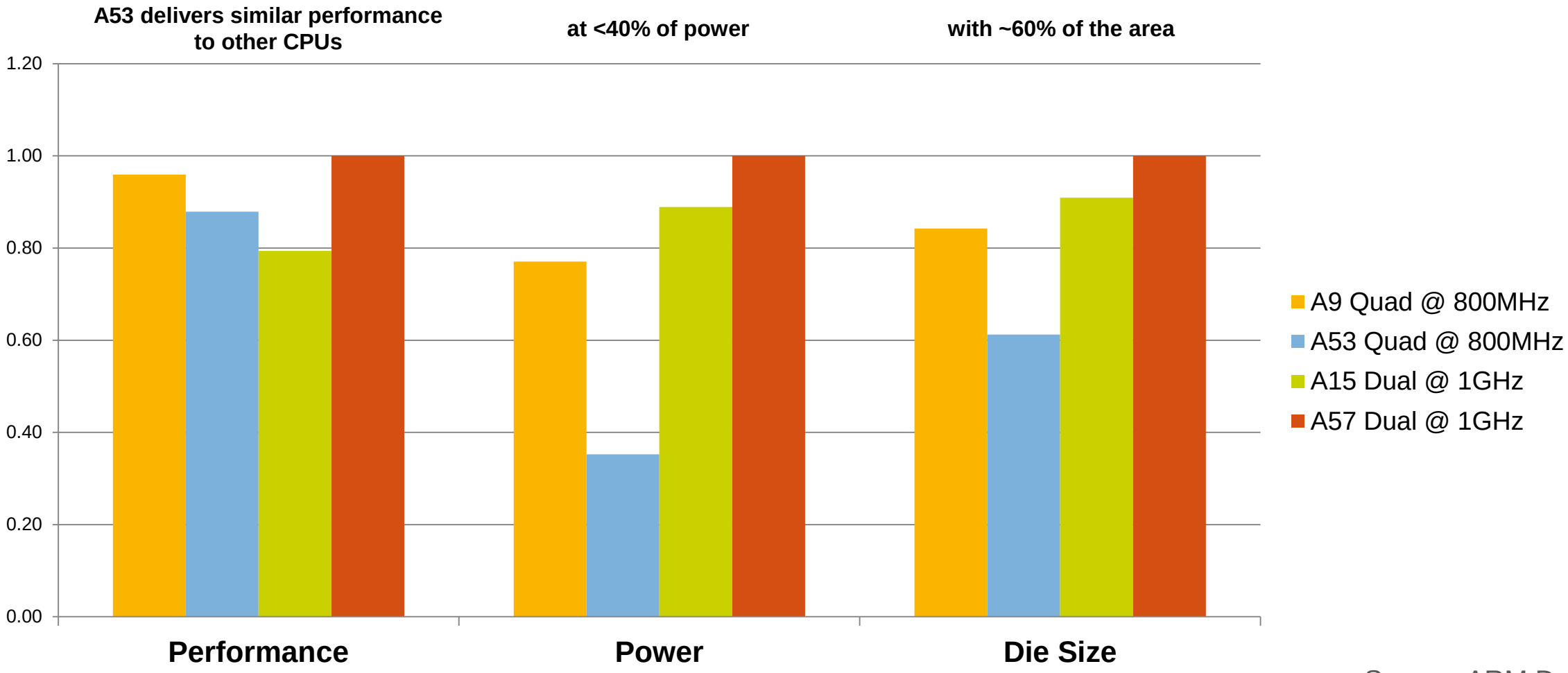
- CPU can snoop data from other cluster
- Snoop can be disabled for predefined regions
- HW-separation of clusters

ARM Cortex-A53 Additional Features

- MMU
  - Virtual-to-Physical address mappings and memory attributes
  - Caching, Sharing, etc.
  - Defined in page table
- Debug resources for supporting trace and cross-trigger functions1
- Set of generic timer registers
- Generic Interrupt Controller (GIC) CPU interface
  - Works in conjunction with the external GIC-400 Generic Interrupt Controller
  - Acts as a centralized resource for supporting and managing interrupts
  - Includes registers for managing interrupt sources, behavior and routing
  - Supports the ARM architecture Security Extensions
  - Supports enabling, disabling, and generating interrupts from peripheral HW
  - Supports generation of software interrupts
  - Supports interrupt masking and prioritization

ARM Cortex-A53 Cluster

Best Compromise Performance/Power/Die Size

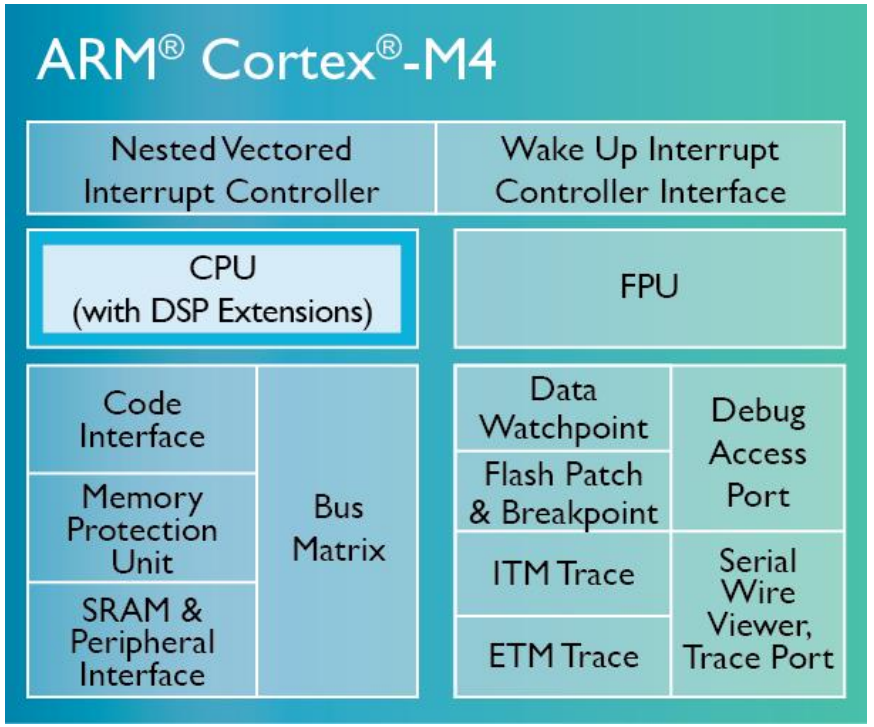


Source: ARM Data

Performance is DMIPS at synthesized frequency
Area is core with Neon + L1 cache, with L2 controller, MP2 or MP4 configuration, no L2 RAM included
Power measured as Dhrystone at nominal voltage

ARM Cortex-M4

- Operating speed of up to 133 MHz
- Supports ARMv7-M architecture
- Includes the single precision FPU
- Core-local Memory Protection Unit (CMPU)
- 3-stage single issue pipeline
- 1.25 DMIPS per MHz integer performance
- 64 KB of Tightly-Coupled Memory
- All local memories operate at core speed
- Zero wait states on “hits”
- 16 KB ICache/16 KB Dcache
- This is the Boot Up core
- Can boot directly from QSPI or other Flash



Since this is the Boot core and much less complex then the Cortex-A53 cores, it makes it perfect for hardware and test people for accessing peripherals and other system resources.

ARM Cortex-M4 Interrupt Controller

- Integrated Nested Vectored Interrupt Controller (NVIC)
  - Supporting low latency interrupt processing
  - Registers for managing interrupt sources, behavior, and routing
  - Enabling, disabling, and generating interrupts form peripheral HW
  - Generating software interrupts
  - Interrupt masking and prioritization

Note For Interrupt Mapping

Interrupts MUST be routed to one, or both of the core clusters. This is accomplished using the: **Interrupt Router Shared Peripheral Routing Control Registers (MSCM_IRSPRC*n*) l**ocated in the **Miscellaneous System Control Module (MSCM)**

Address: 0h base + 880h offset + (2d × i), where i=0d to 175d

A53 M4

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	RO	0													CP1E	CP0E
Write																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MEMORY SYSTEMS & DRAM CONTROLLER

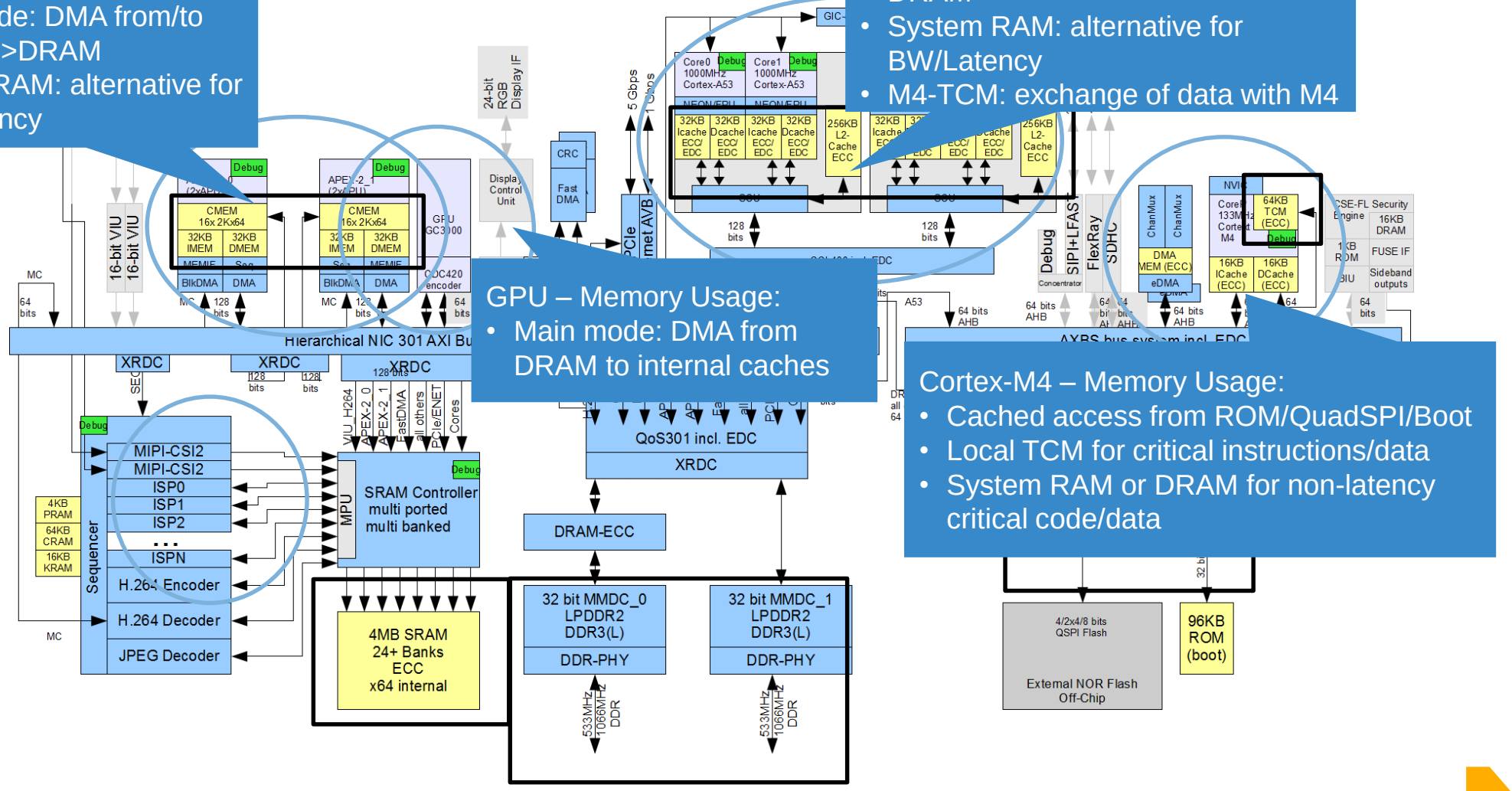
Memories & Bus Structure

APEX2 – Memory Usage:
- Main mode: DMA from/to CMEM<->DRAM
- System RAM: alternative for BW/Latency

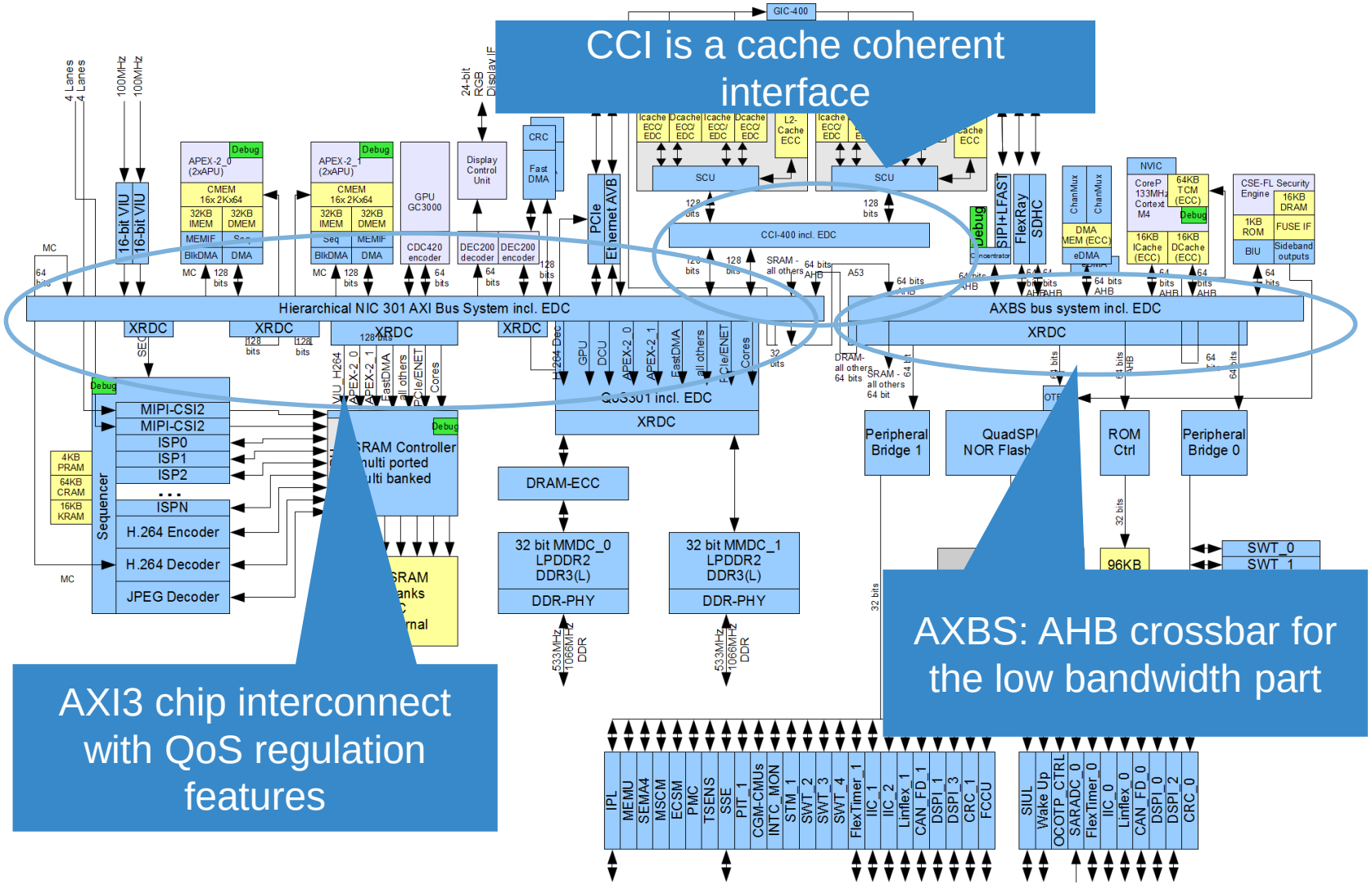
Cortex-A53 – Memory usage:
- Main mode: Cached access to DRAM
- System RAM: alternative for BW/Latency
- M4-TCM: exchange of data with M4

GPU – Memory Usage:
- Main mode: DMA from DRAM to internal caches

Cortex-M4 – Memory Usage:
- Cached access from ROM/QuadSPI/Boot
- Local TCM for critical instructions/data
- System RAM or DRAM for non-latency critical code/data

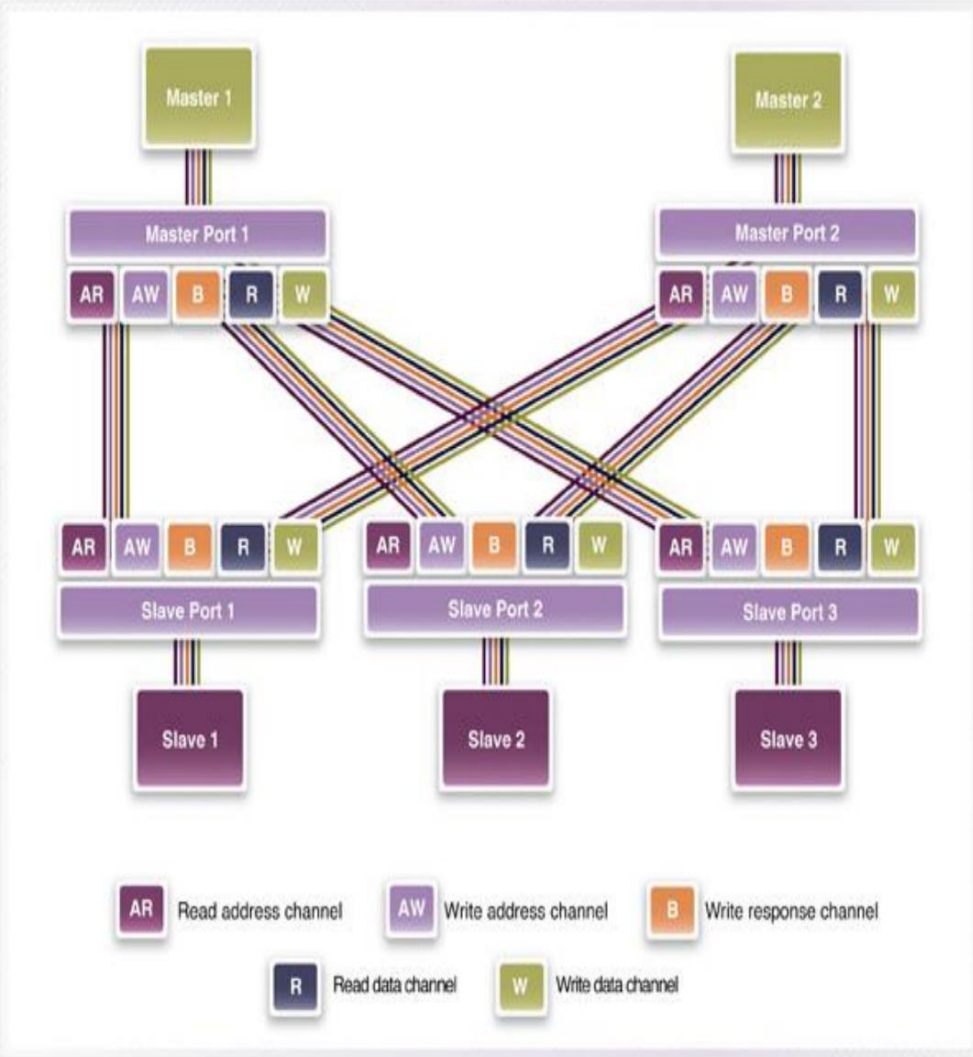


SoC Bus Structure



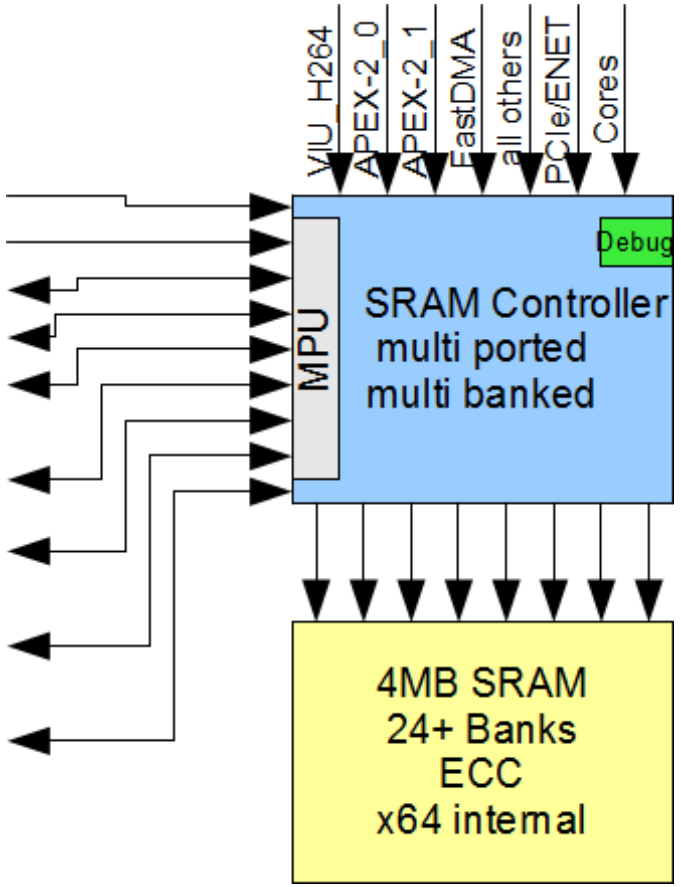
NIC 301 AXI High Performance Switch System

- Connects all Masters to all Slaves
- Up to 128bits wide
- Up to 533 MHz operation
- Up to 4.2 Gbytes/second / Master
- QoS – Quality Of Service features
  - Programmable Master priorities
  - Advanced methods for traffic regulation
    - Latency based regulation
    - Outstanding transactions regulation
    - Transaction rate regulation
      - Specify peak and average bandwidth



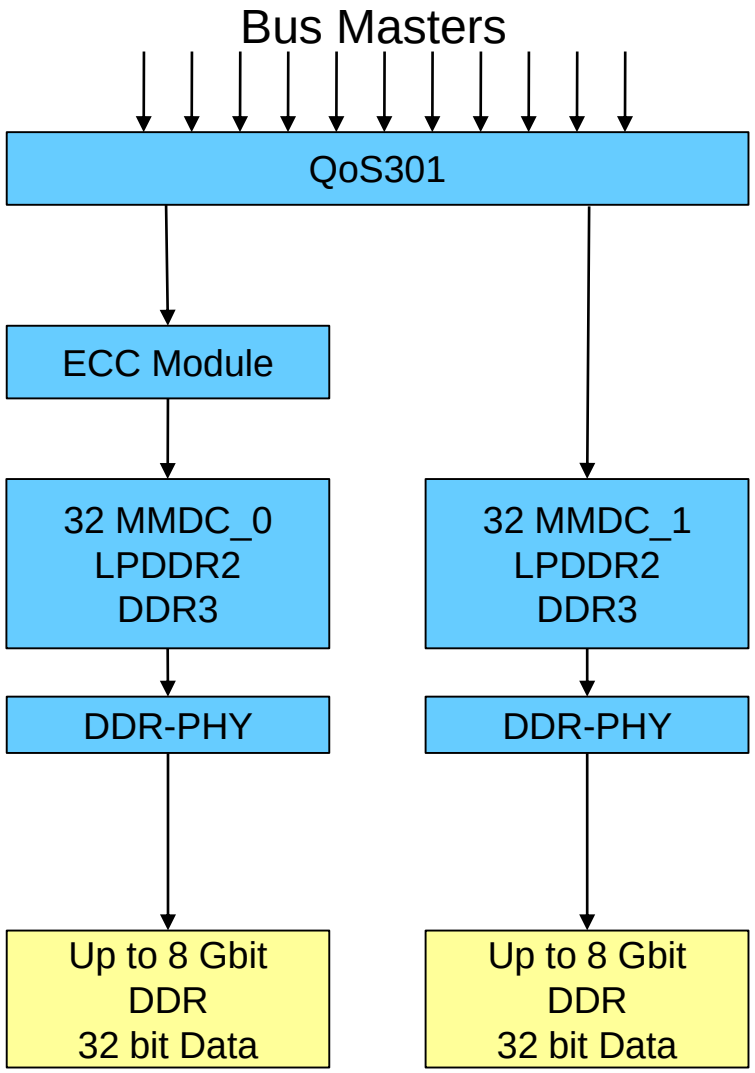
Multi-Ported Multi-Banked System RAM (HPSMI)

- 4 Mbytes total size to offload the DRAM
- Multiple memory banks allowing parallel access
  - 12*256 KBytes banks for 3 Mbytes of memory
  - 1 Mbytes in additional banks
  - Interleaved access (e.g. for ISP)
- Multiple ports for parallel master access
- Fast DMA
  - Transfers data between System RAM and DRAM
- ECC support
- Watchpoint HW for debug and trace



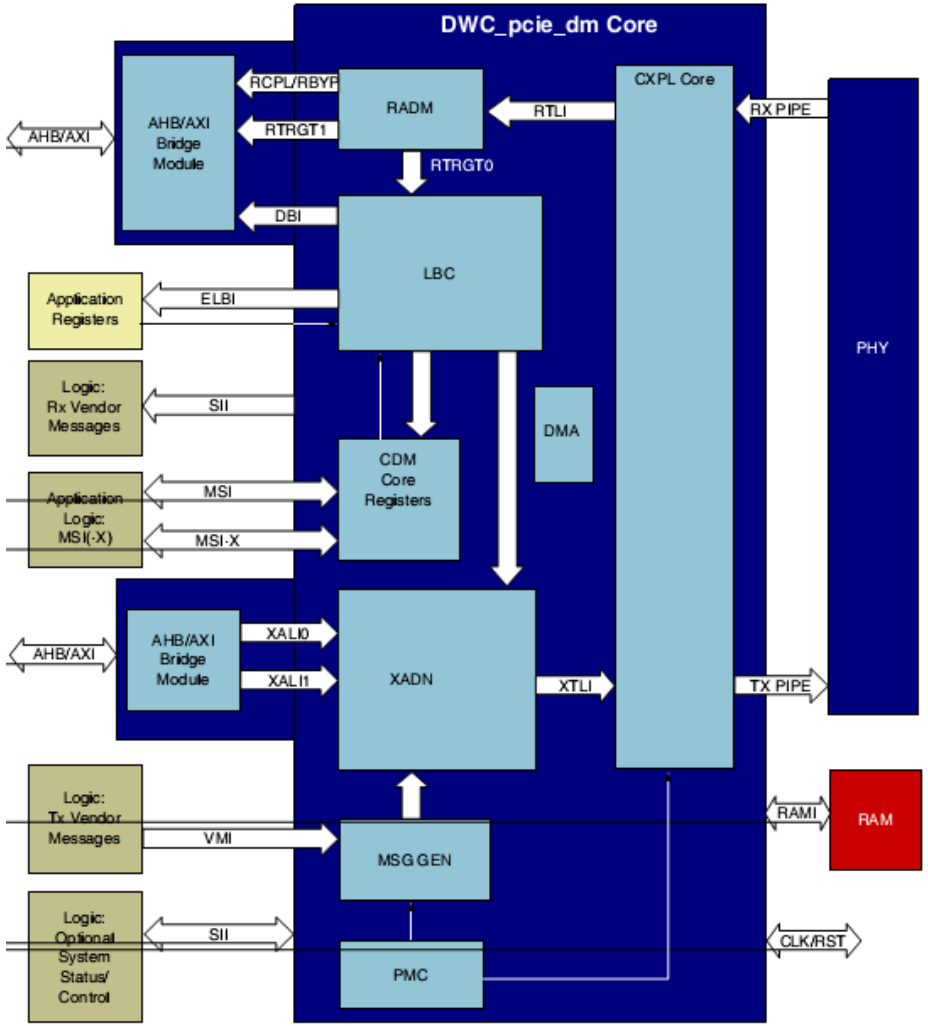
Multi-Mode DRAM Controller

- Connection of industry standard DRAMs
- DRAM Standards
  - DDR3L, DDR3 x16, x32
  - LPDDR2 2-channels x16, x32
  - Does not support LPDDR1, MDDR or DDR2
- DRAM Interface
  - x16, x32 data bus width
  - Density per DDR device of 256 Mbits–8 Gbits with the following column and row combinations:
    - Column size of 8–12 bits
    - Row size of 11–16 bits
  - Two chip selects per channel
  - Up to 4 Gbytes of address space with configurable partitioning between CS0 and CS1 (for LPDDR2 2ch x32 up to 2 Gbytes per channel)
  - Supports burst length of 8 (aligned) for DDR3
  - Supports burst length of 4 for LPDDR2
- ECC for selectable range of DDR space



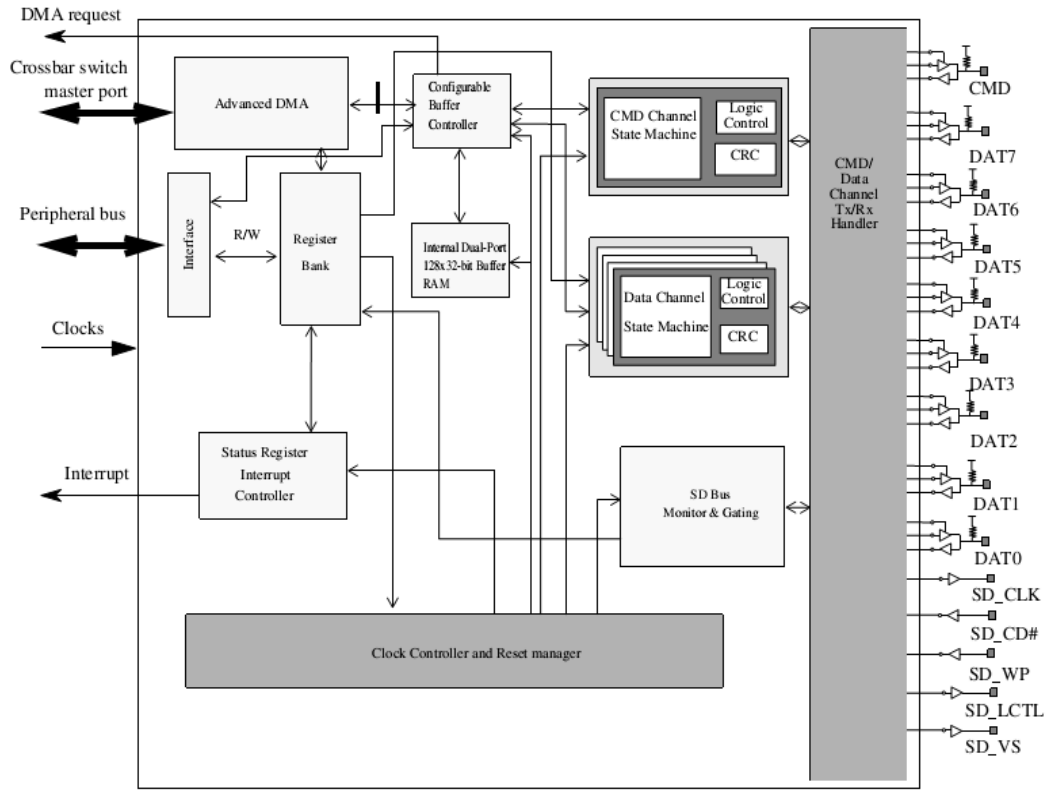
PCIe Bus

- Allows high bandwidth connection to external DSP and FPGA
- Allows expansion to 2nd device
- Modes supported:
  - 5Gb/s PCIe Gen 2
  - 2.5Gb/s PCIe Gen 1.1
- 1 Lane Supported
- Transfer rate:
  - Theoretical 500 MBytes/second
  - Practical peak of ~400MB/s



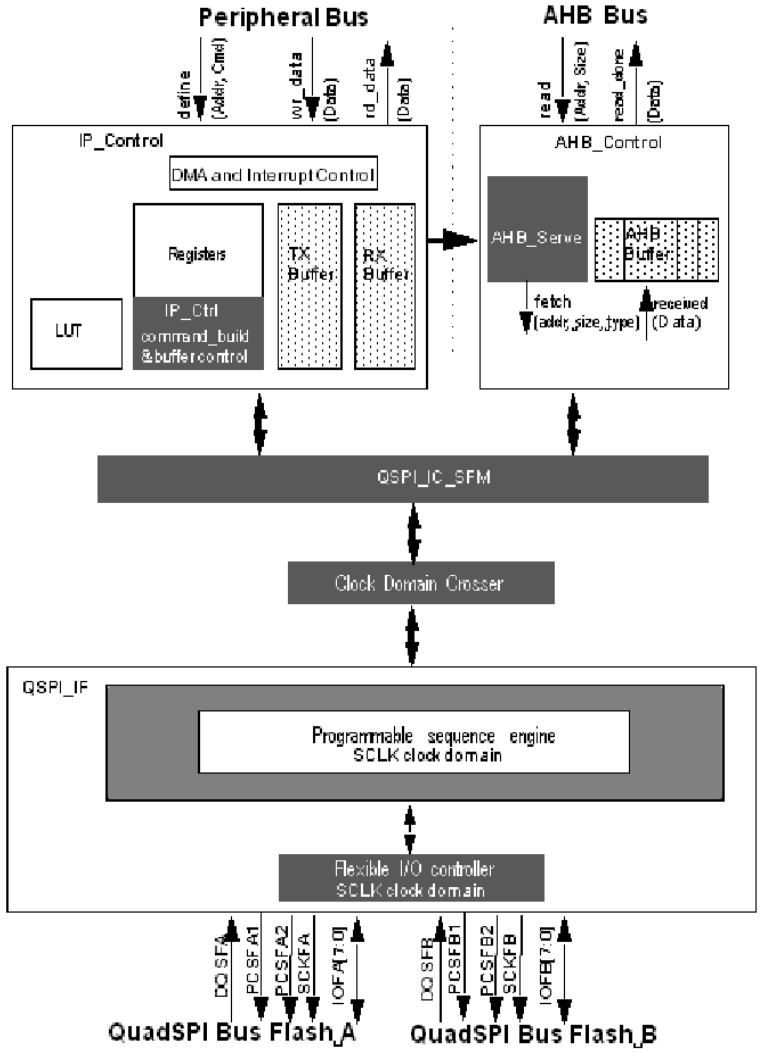
SDHC – Secure Digital Host Controller

- Conforms to the SD Host Controller Standard Specification version 2.0 including test event register support
- Compatible with the MMC System Specification version 4.4/4.5
- Compatible with the SD Memory Card Specification version 2.0 and supports the high capacity SD memory card
- Compatible with the SDIO Card Specification version 2.0
- MMC bus clock frequency up to 52 MHz
- Supports 1-bit/4-bit SD and SDIO modes, 1-bit/4-bit / 8-bit MMC modes devices
- Up to 400 Mbps of data transfer for SD/SDIO cards using 4 parallel data lines
- Up to 832 Mbps of data transfer for MMC cards using 8 parallel data lines



QuadSPI

- Dual QuadSPI Interface
  - Single, dual, quad and octal mode of operation
- DDR/DTR mode
  - data is generated on every edge of the serial flash
- Supports flash data strobe signal for data sampling in DDR & SDR mode
- DMA support to read RX Buffer data via AMBA AHB bus (64-bit width interface) or IP registers space (32-bit access)
- Flexible and configurable buffer for each master
- Programmable sequence engine to cater for current and future command/protocol operation
- Supports 3-byte and 4-byte addressing
- Maps serial data to defined memory space
  - Looks like address mapped memory to the user
- Can be used for system Boot flash

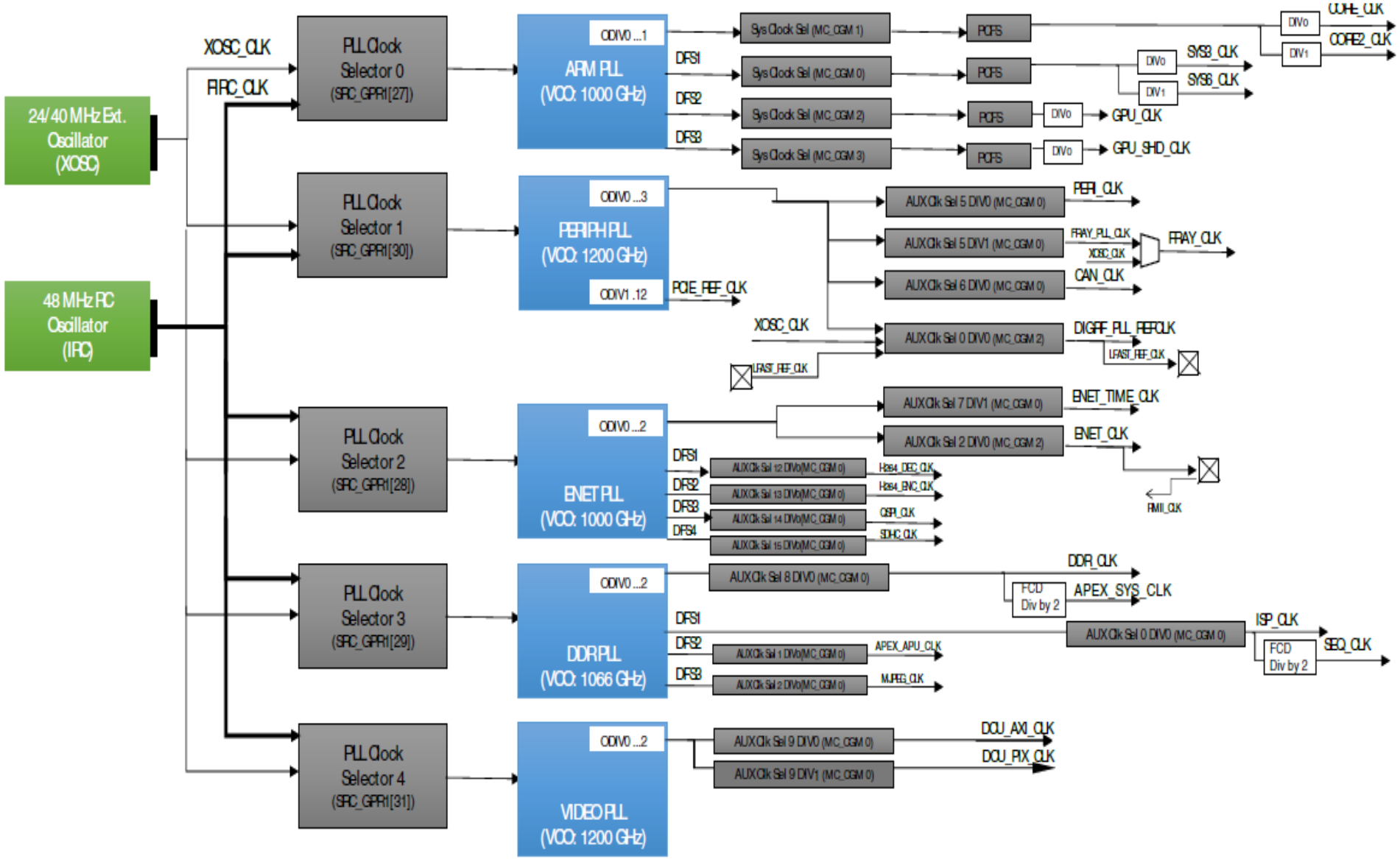


CLOCKING & RESET

Clock & PLLs

- External OSC which works with 24 and 40 MHz frequency
- 48 MHz FIRC as internal clock for reference and fast start-up
- Five PLL instances for the clocks inside the system
  - (Excluding local PLLs for PCIe, LFAST)
  - ARM PLL to generate a frequency of up to 1000 MHz
    - Spread spectrum supported, fractional divider outputs
  - PERIPH PLL to generate precise low jitter clocks for PCIe, timers, ADC
    - No spread spectrum, integer multiplication and division
  - ENET PLL with VCO frequency of 500 MHz
    - Used for Ethernet
    - Fractional divider support for a list of additional IP clocks
    - No additional OSC required
  - DDR PLL
    - No spread spectrum for low jitter DDR clock
    - Fractional divider support for a list of additional IP clocks
  - Video PLL
    - No spread spectrum, for highly accurate setting of display output frequency

Clock Architecture – Top Level



Mode Entry Module (ME)

- This device includes a Mode Entry Module
  - Commonly used on our PPC microcontroller families.
  - Modifications to Clock sources and operation parameters require a Mode Change to complete

Table 22-3. MC_ME controlled Clock Sources

Index	Clock Source	MC_ME controlled
0	FIRC	No (Always ON)
1	FXOSC	MC_ME_<MODE>_MC.CSRC1ON
2	ARM PLL	MC_ME_<MODE>_MC.CSRC2ON
3	PERIPH PLL	MC_ME_<MODE>_MC.CSRC3ON
4	ENET PLL	MC_ME_<MODE>_MC.CSRC4ON
5	DDR PLL	MC_ME_<MODE>_MC.CSRC5ON
6	VIDEO PLL	MC_ME_<MODE>_MC.CSRC6ON
7-15	Reserved	Reserved

Resets

- There are two different reset pins and two different types of reset
  - EXT_POR* and RESET*
  - Destructive and functional resets
- Destructive resets completely restart the MCU after a critical event
  - Register and memory contents are not guaranteed
- Functional resets restart digital modules
  - Preserve analog and debugging module settings

Destructive Resets

SOURCE	DESCRIPTION	IRQ	BIDI
D_POR	Power on reset or assertion of EXT_POR pin	no	yes
D_SOFT_DEST	Software initiated destructive reset	no	yes
D_FFRR	FCCU failure to react reset	no	yes
D_SUF	STCU unrecoverable fault reset	no	yes
D_DDR_HNDSHK_TO	DRAM self refresh handshake timeout	no	yes
D_EFR	Functional reset escalation	no	yes
D_DBGRST	Debugger initiated destructive reset	no	yes
D_HVD_CORE	HVD of 1.0V core voltage supply	no	yes
D_LVD_CORE	LVD of 1.0V core voltage supply	no	yes
D_LVD_33_PMC	LVD of 3.3V voltage supply	no	yes
D_HVD_18	HVD of 1.8V PMC voltage supply	no	yes

Functional Resets

SOURCE	DESCRIPTION	Short	Long	IRQ	BIDI
F_EXT_RST	External reset event through RESET Pin	opt	opt	no	yes
F_ST_DONE	Reset generated after self test is complete	yes	no	no	opt
F_SOFT_FUNC	Software initiated functional reset	opt	opt	no	opt
F_FCCU_HARD	FCCU hard reaction request	yes	no	no	opt
F_FCCU_SOFT	FCCU Soft reaction request	no	yes	no	opt
F_JTAG_OR_DBG	JTAG or Debugger Reset Request	opt	opt	opt	opt
F_SWT4	SWT4 timeout reset request	opt	opt	no	opt

Reset Process Modules

Module	Contribution Type		
	event	gating	control
Reset Generation Module (MC_RGM)	Yes	Yes	Yes
Power Management Digital Controller (PMC-Dig)	Yes	Yes	Yes
Mode Entry Module (MC_ME)	Yes	—	—
On Chip One Time Programmable (OCOTP) Controller	—	Yes	—
Self-Test Control Unit (STCU)	Yes	—	—
Fault Collection and Control Unit (FCCU)	Yes	—	—
JTAG Controller (JTAGC)	Yes	—	—
Miscellaneous Debug Module (MDM) AP	Yes	—	—
Clock Generation Module (MC_CGM)	—	Yes	—
Software Watchdog Timer 4 (SWT4)	Yes	—	—

Contribution Type	Description
event	The module may generate events which may trigger the entry into a reset state, if the event configuration in the MC_RGM allows this.
gating	The module can prevent the exit of a reset state if it has not reached a certain internal state.
control	The module controls the sequence of the reset process.

Reset Process

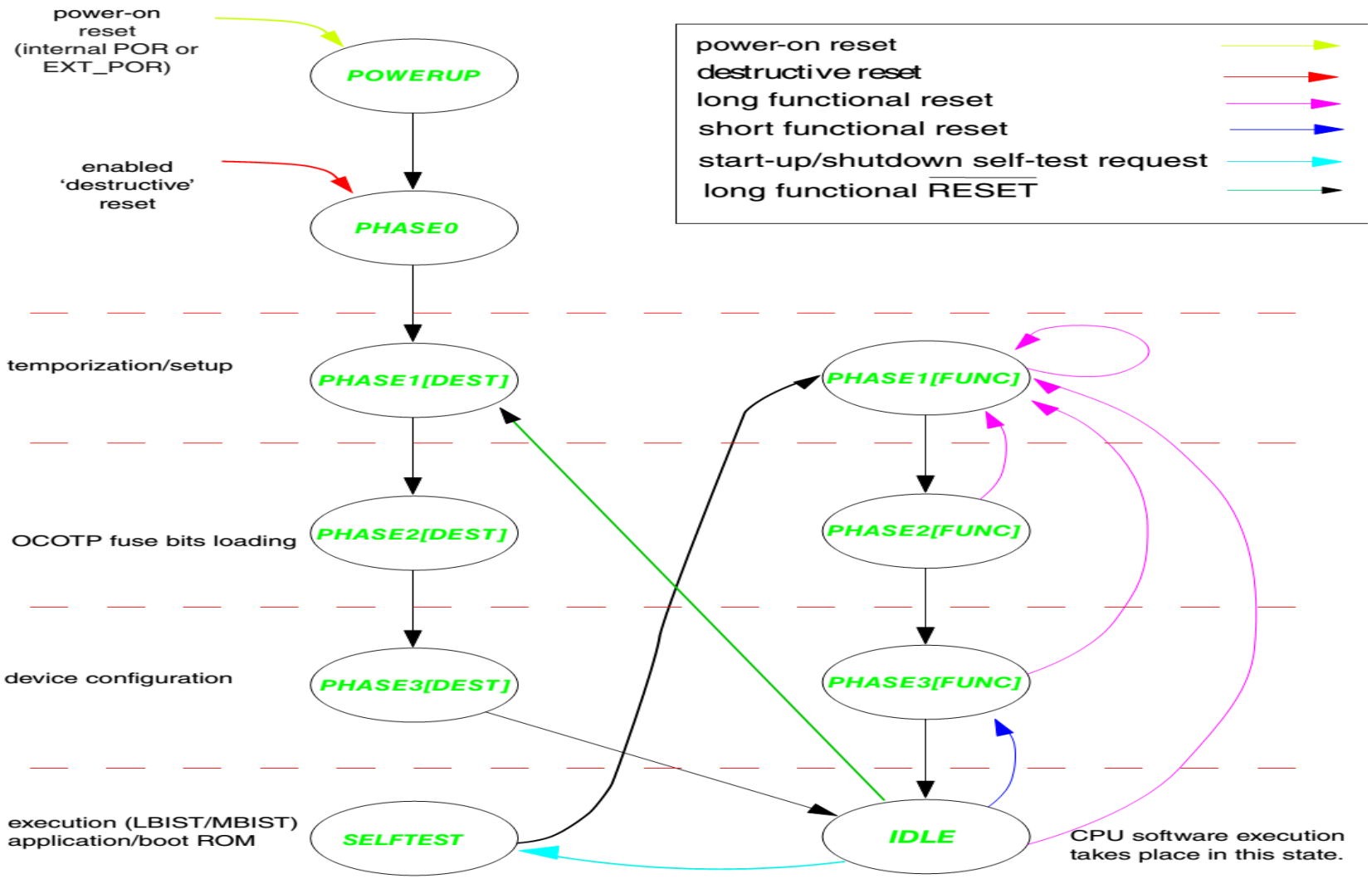
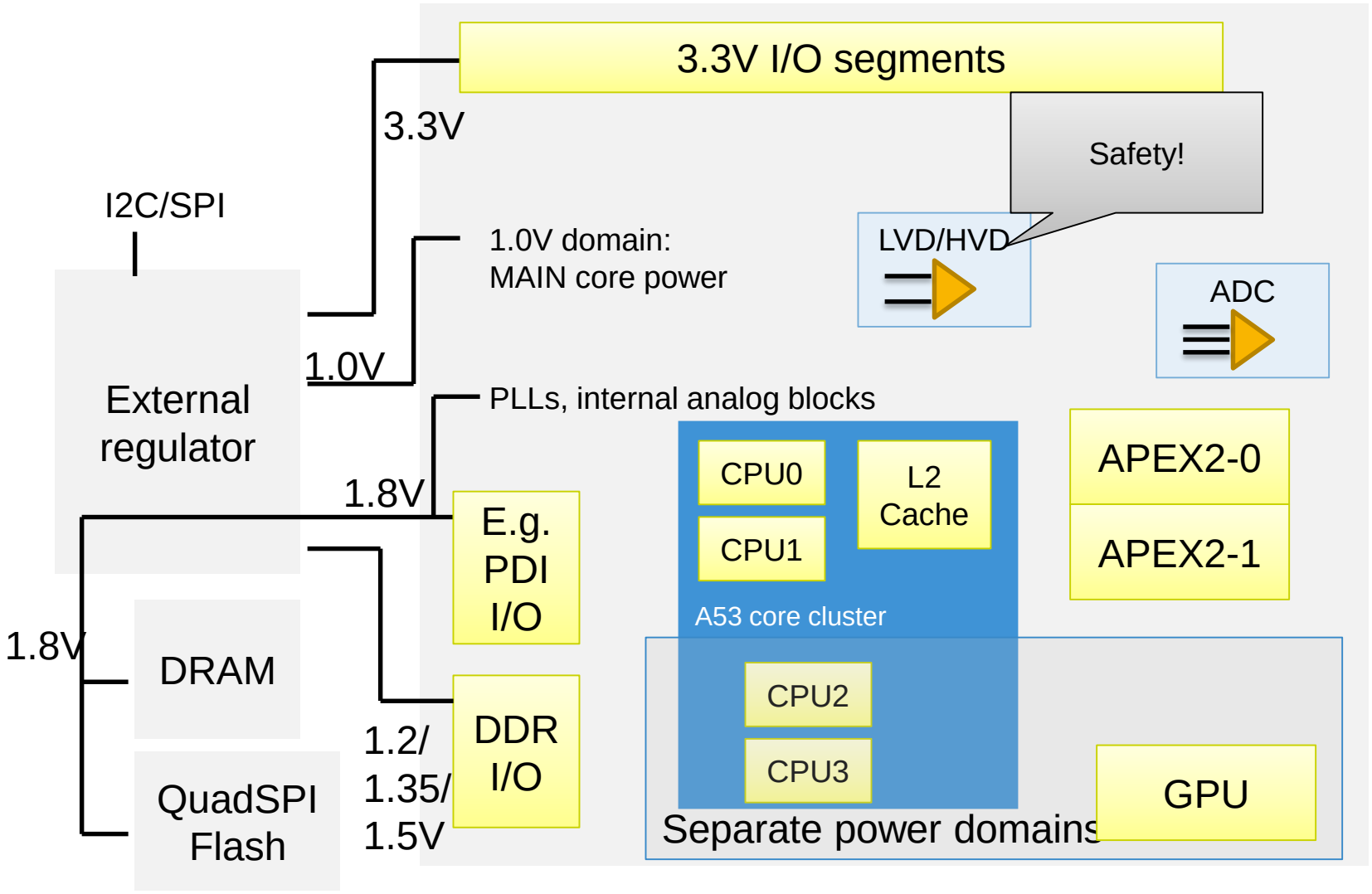


Figure 28-1. Reset Process Sequences

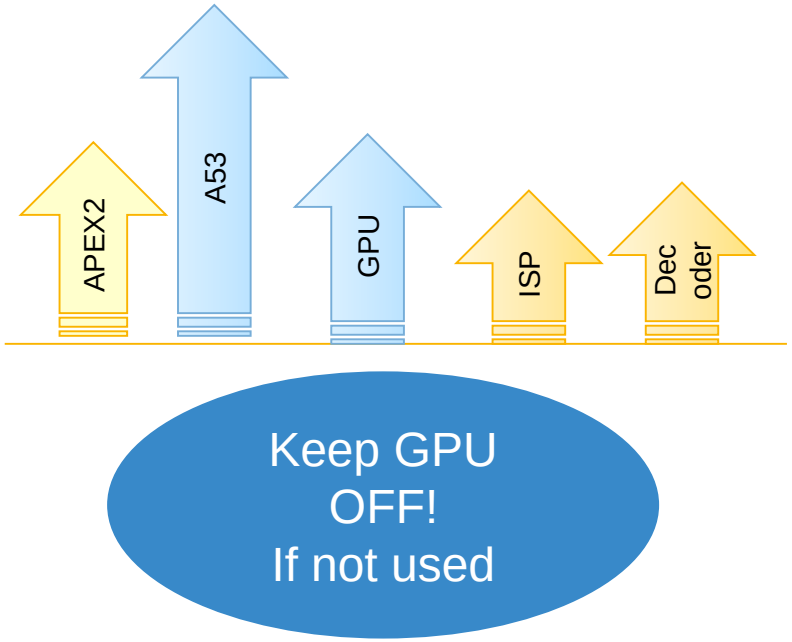
POWER MANAGEMENT

Power Supplies



Power Modes

- Power Modes:
  - Manage run time power via
    - Clock gating for each peripheral and processing block
    - Independent scaling of clocks between the important processing blocks: Cortex A53 cluster, APEX2, GPU, ISP, Video en/decoders
    - Power gating of Cortex A53 CPUs (each 2nd CPU in a cluster)
    - Power gating of the GPU
  - No real stop mode support
  - No standby mode support
  - No standby RAM



Static and Dynamic Power Dissipation

Use case examples	Estimation range (to be narrowed during validation) Tj=125 degC, worst silicon	Estimation range (to be narrowed during validation) Tj=125 degC, typical silicon	Estimation range (to be narrowed during validation) Tj=25 degC, typical silicon
4xA53s running with 800 MHz, front camera use case, low power version	This Data Is Currently Confidential Expect numbers from 3.5W – 10W		
4x A53s running with 1 GHz, APEX and GPU powered off			
4x A53s running with 1 GHz, APEX running@500 MHz and GPU powered off			
4x A53s running with 1 GHz, APEX running@500 MHz and GPU@600 MHz			
Surround view case (as row above plus video codecs, ISP operating			

- Static power consumption (leakage) at Tj=125degC is estimated as 5.1W w/o GPU
  - 6.3W with all blocks powered with worst silicon.
  - Low power version with max 2.3W leakage (w/o GPU)
- Dynamic power consumption can be managed with clock gating/frequency adjustment
- Static power gating option for the GPU and the 2nd Cortex A53 CPU per cluster

BOOT UP

Boot ROM Features & Boot Options

- The main features of the ROM include:
- Support for booting from various boot devices
- Serial Downloader support (FlexCAN, and UART)
- Device Configuration Data (DCD)
- Online Self Test execution
- Fast Reboot (DDR Self Refresh)
- Secure boot
- Configuration via fuses and/or BOOT_MOD/RCON input pins
- Boot ROM supports the following boot devices:
  - SD/MMC
  - QuadSPI

Boot Process Summary

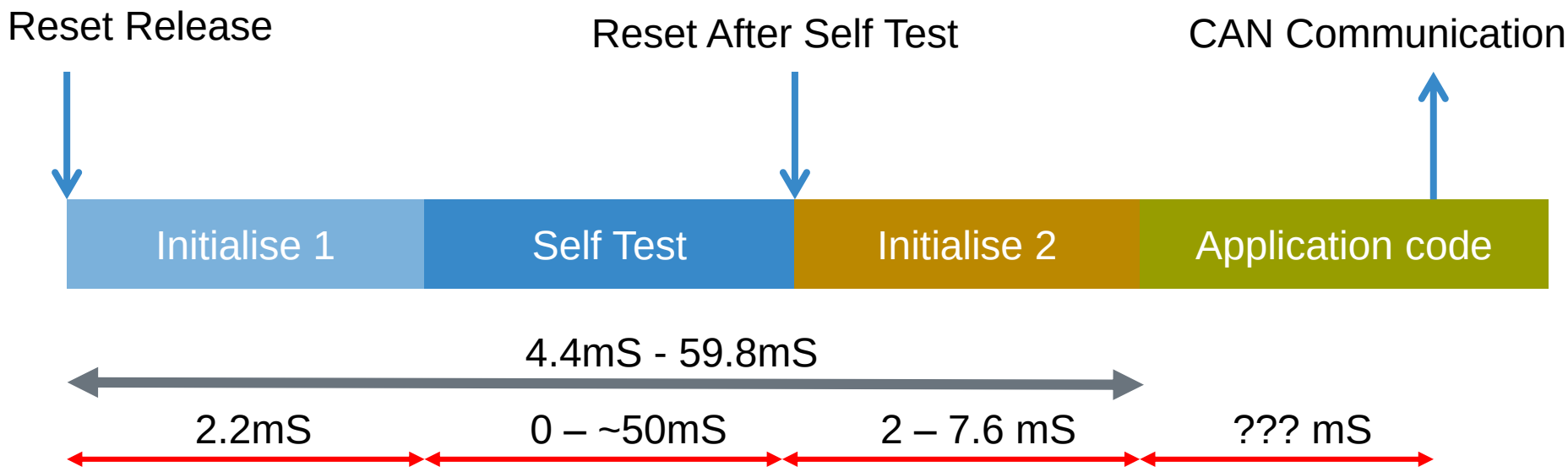
- Reset
- Begin execution of Boot ROM code
  - The boot process depends on SRC_BMR2[BMOD], SRC_BMR1
- Read the Image Vector Table and boot data structures
  - Device Configuration Data (DCD)
- Optionally, download image to memory. (Code can execute from QSPI)
- Execute image (user code)

- Note:
  The Boot ROM uses the state of the SRC_BMR1, SRC_BMR2 and eFuses to determine the boot device. For development purposes, there is also an option to use GPIO pin inputs to override the fuse values to determine the boot device.

Boot Mode Pin Settings

BMODE[1]	BMODE[0]	BT_FUSE_SEL	Boot Type	Intended Use-Case
0	0	0	Serial Download	Production configuration - Virgin device
0	0	1	Boot from Fuses	Production configuration - Programmed device
0	1	X	Serial Download	Debug of programmed device
1	0	0	Boot from RCON	Development configuration
1	0	1	Boot from Fuses	Security loophole closure
1	1	X	Reserved	Reserved

Boot Timing



- System and clock init
- QSPI Init
- Self Test Configuration

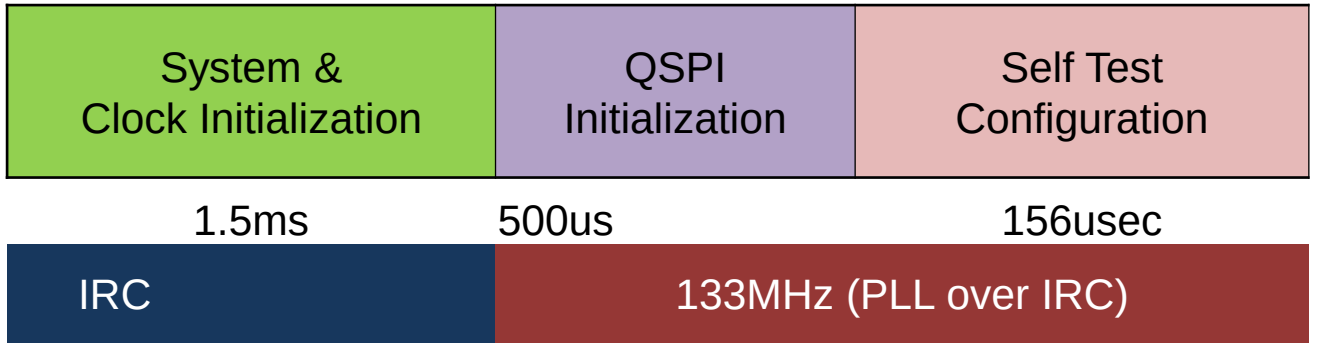
- LBIST execute
- MBIST execute

- System and clock init
- QSPI Init
- DCD Execute
- CSE Secure call back
- CSE Secure boot
- Jump to application code

- Application start up
- CAN communications
- Further MBIST
- Load full application
- Start A53 cores

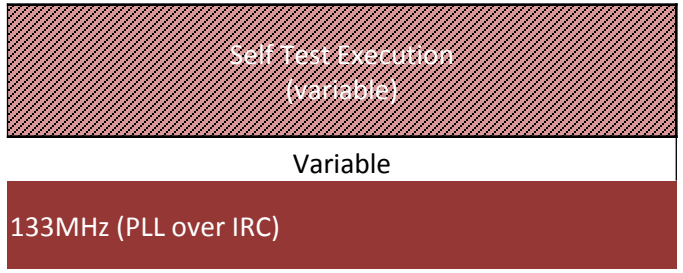
Initialise 1

- Systems & Clock Init (PLL take 500uS to lock) - 1.5mS
- QSPI Init – read initial config from QSPI and reconfigure – 500uS
- Self Test Config – Setup the STCU with data stored in QSPI – 156uS



Self Test

Execute Self Test



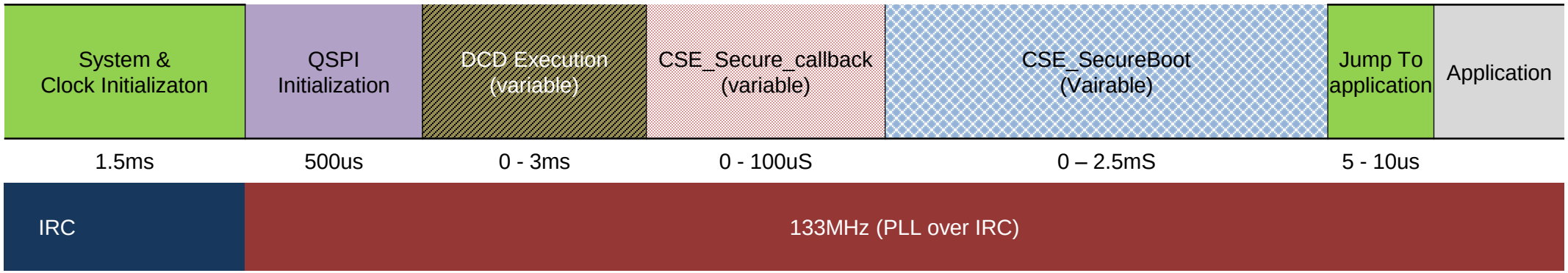
- LBIST:
  - 27 logic partitions. Can be executed 3-4 in parallel – ~8 runs
  - Each run:
    - 3000 patterns (number required to reach 90% SA coverage)
    - 88 clocks in each pattern
  - Time to LBIST all logic – ~ 40mS (shorter if not all partitions are tested)

- MBIST:
  - Time to test all memories (checkerboard 4N) – ~10mS
  - Portion of memories can be tested after CAN communications is started if required

  - (All BIST timing is preliminary and may change during validation)

Initialise 2 (2mS to 7.6mS)

- Systems & Clock Init (PLL take 500uS to lock) - 1.5mS
- QSPI Init – read initial config from QSPI and reconfigure – 500uS
- DCD Execution
  - Execution time depends on how many DCDs are programmed in flash (0-3mS)
- CSE Secure Callback
  - This is a small customer function that returns pointers to the CSE key file. This could be as simple as returning a couple of fixed values or it could be interrogating the file system or EEPROM emulation scheme to retrieve the pointers (wild estimate 100uS – 13k clock cycles)
- CSE Initialisation and Secure Boot
  - This depends on the size of boot code (Example: 32k bytes = 1.1mS; 64k bytes = 1.6mS; 128k bytes = 2.5mS)
- Clean up boot and jump to customer code (5-10uS)



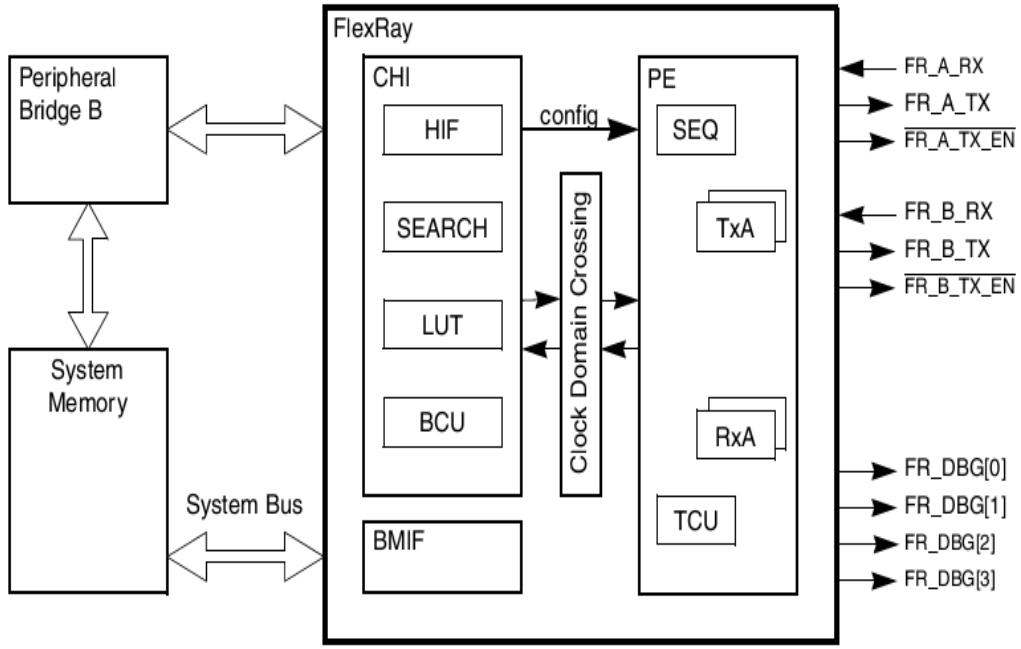
Application Code

- Boot code runs on ARM Cortex-M4 @ approx 133MHz using PLL and internal RC oscillator.
- Application code should switch to crystal oscillator and relock the PLL (approx 1.5mS)
- Application code can use Cortex M4 Caches and TCM. Code can be executed from serial flash.
- Application code should start CAN communication.
- Application code can then:
  - Test DRAM (application software)
  - MBIST all other on-chip RAMs (<10mS – running in parallel with code)
  - Load and authenticate main application code to RAM
    (12.5mS/M byte assuming QSPI @ 80MHz DDR 4 bits wide
    6.25mS/M bytes assuming 8 bit wide)
  - Start executing Cortex A53s from code in DRAM

SERIAL COMMUNICATION (CAN-FD, ETHERNET, ETC.)

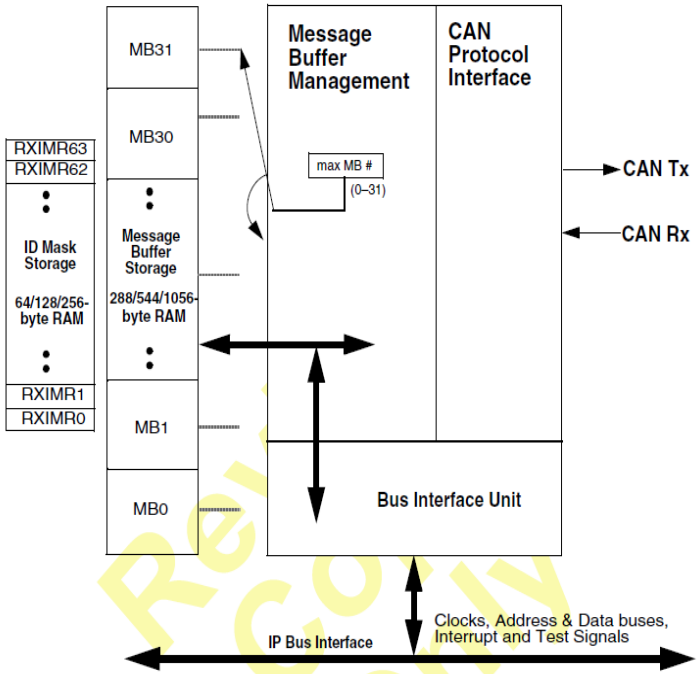
FlexRay

- FlexRay Communications System Protocol Specification, Version 2.1 Rev A-compliant protocol implementation[end]
- FlexRay Communications System Electrical Physical Layer Specification, Version 3.0-compliant bus driver interface[end]
- Dual channel
- FlexRay bus data rates of 10 Mbit/s, 8 Mbit/s, 5 Mbit/s, and 2.5 Mbit/s supported
- 128 configurable message buffers with
  - Individual frame ID filtering
  - Individual channel ID filtering
  - Individual cycle counter filtering
- Message buffer header, status, and payload data stored in system RAM



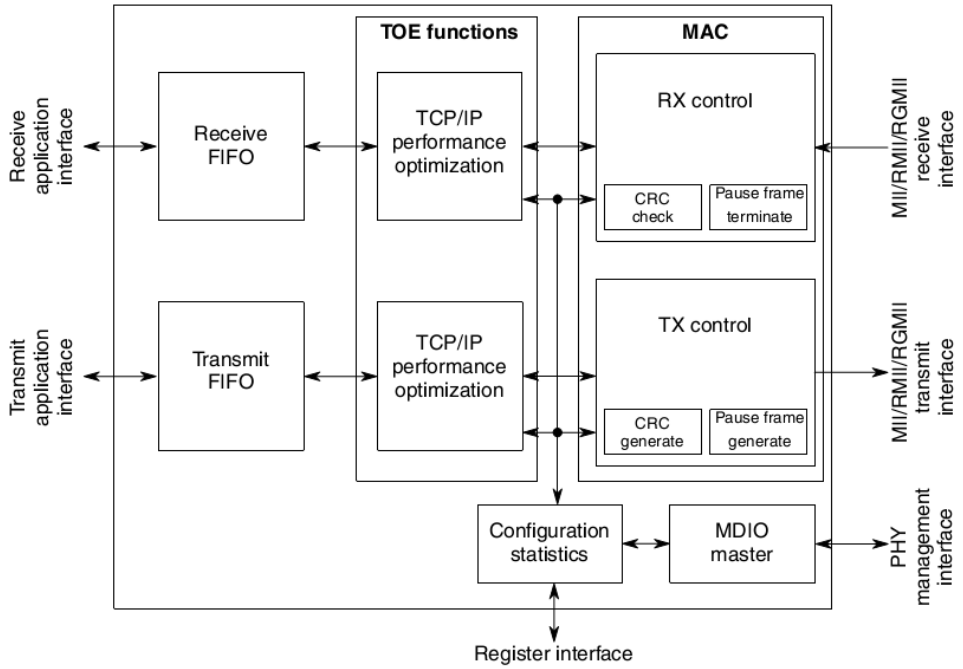
FlexCAN3 With CAN FD Support

- CAN FD support (Latest Version)
- Full Implementation of the CAN protocol specification, Version 2.0B
- Flexible Message Buffers (64) of zero to eight bytes data length
- 64 MB each configurable as Rx or Tx
  - Supporting standard and extended messages
- Individual Rx Mask Registers per Message Buffer
- Pretended network support
- Full featured Rx FIFO with storage capacity for 6 frames
- DMA request for Rx FIFO
- Powerful Rx FIFO ID filtering
  - Capable of matching incoming IDs against either 8 extended, 16 standard or 32 partial (8 bits) IDs, with individual masking capability
- Programmable clock source to the CAN Protocol Interface
  - System bus clock or crystal oscillator
- Programmable transmission priority scheme:
  - Lowest ID, lowest buffer number or highest priority
- Time Stamp based on 16-bit free-running timer



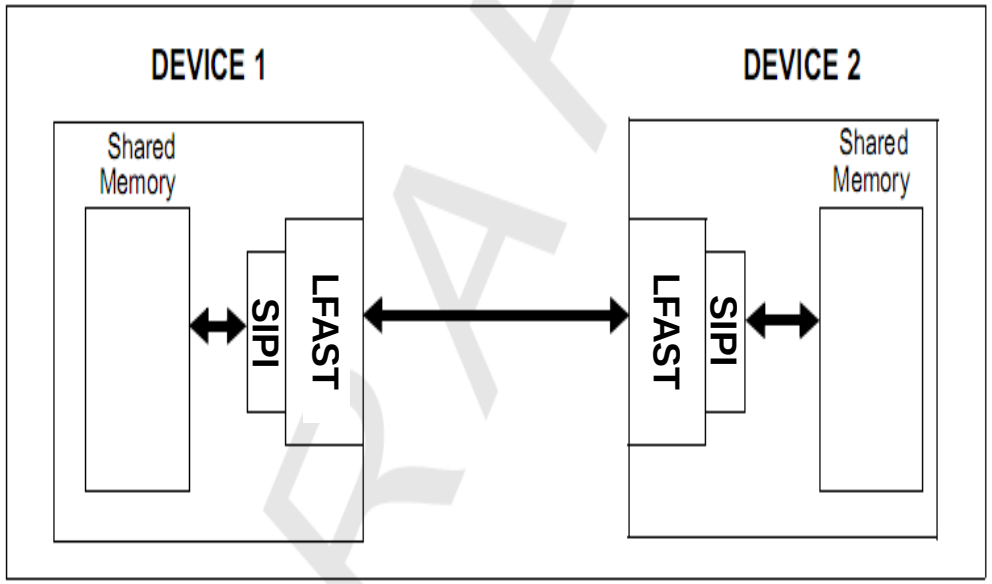
Gigabit Ethernet Controller with AVB

- Implements the full 802.3 specification with preamble/SFD generation, frame padding generation, CRC generation and checking
- Supports zero length Preamble
- Dynamically configurable to support 10/100 Mbit/s and Gigabit operation
- Supports 10/100 Mbit/s full-duplex and configurable half-duplex operation
- Supports gigabit full-duplex operation
- Compliant with the AMD magic packet detection with interrupt for node remote power management
- Seamless interface to commercial Ethernet PHY devices via:
  - a 4-bit Medium Independent Interface (MII) operating at 25 MHz, or
  - a 2-bit Reduced MII (RMII) operating at 50 MHz, or
  - a (double data rate) 4-bit Reduced GMII (RGMII) operating at 125 MHz.
- Supports VLAN-tagged frames according to IEEE 802.1Q
- MDIO master interface for PHY device configuration and management with two programmable MDIO base addresses
- AVB features:
  - AVB endpoint talker and listener support
  - Support for arbitration between different priority traffic (e.g., AVB class A, AVB class B, and non-AVB)
  - Credit-based shaper bandwidth policing



Zipwire (LFAST + SIPI Inter-processor Bus)

- Full duplex Multimaster Memory Access from one MCU/ASIC to another
- No CPU load at the target node
- DMA support for large transfers
- CRC protection for complete message
- Designed to run on top of LFAST
- LFAST
  - Full duplex
  - 5 wire interface (2 x LVDS pairs)
  - 320M / 20M / 5M baud data rates
- Point to point communication between two devices
- Full duplex communication
- 4 independent channels
  - 1 channel supports data streaming capability (32 bytes per message)
- All channels support 32, 16 or 8 bit read and write with a 32 bit address
- All channels can generate an event/interrupt request at the target node
- All commands produce an acknowledge message
- Automatic timeout protection mechanism for acknowledge messages
- Priority mechanism for channels – fixed priority (Channel 0 highest)



Also Included

- SPI
- I2C
- LINFlex
  - LIN / UART

DMA

Fast DMA

- DMA optimised for moving large amounts of image data quickly between on chip SRAM and external DRAM

- DMA Engine allowing:
  - Efficient transfers between DDR memory and SRAM
  - Pipelined of bursts (4-8 transactions) to SRAM
  - 2 x128 Bit Ports:
    - One to the DDR controller the other to the System Crossbar
    - Support back to back data transfers to/from the DDR RAM
    - Queuing of DMAs multi burst commands
    - HW support to control data coherency
    - Handling of (incremental) check sums (CRC) for functional safety

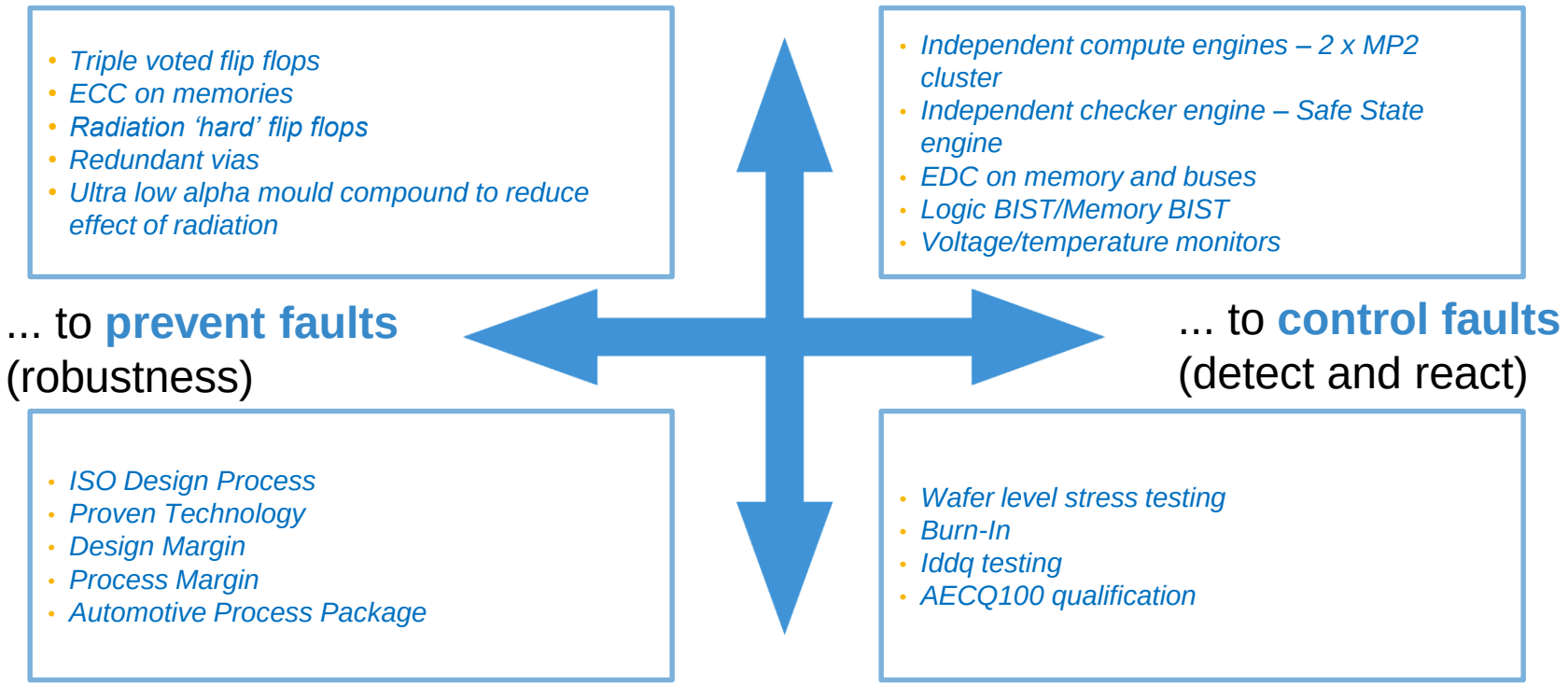
Enhanced DMA

- 32 Channels with 32 Channel Multiplexer
- Programmable source and destination addresses and transfer size
- Connections to the crossbar switch for bus mastering the data movement
- Transfer control descriptor (TCD) organized to support two-deep, nested transfers
- 32-byte TCD stored in local memory for each channel
- An inner data transfer loop defined by a minor byte transfer count
- An outer data transfer loop defined by a major iteration count
- Channel activation via one of three methods:
  - Explicit software initiation
  - Initiation via a channel-to-channel linking mechanism for continuous transfers
  - Peripheral-paced hardware requests, one per channel
- Fixed-priority and round-robin channel arbitration
- Channel completion reported via optional interrupt requests
- One interrupt per channel
  - Optionally asserted at completion of major iteration count
- Optional error terminations per channel
  - Logically summed together to form one error interrupt to the interrupt controller
- Optional support for scatter/gather DMA processing
- Support to cancel transfers via software

FUNCTIONAL SAFETY

ISO26262 Fault Prevention and Control Measures

... implemented as **product features**
against random faults (architecture, function)



... during **develoment** and **production**
against systematic faults (process, procedures)

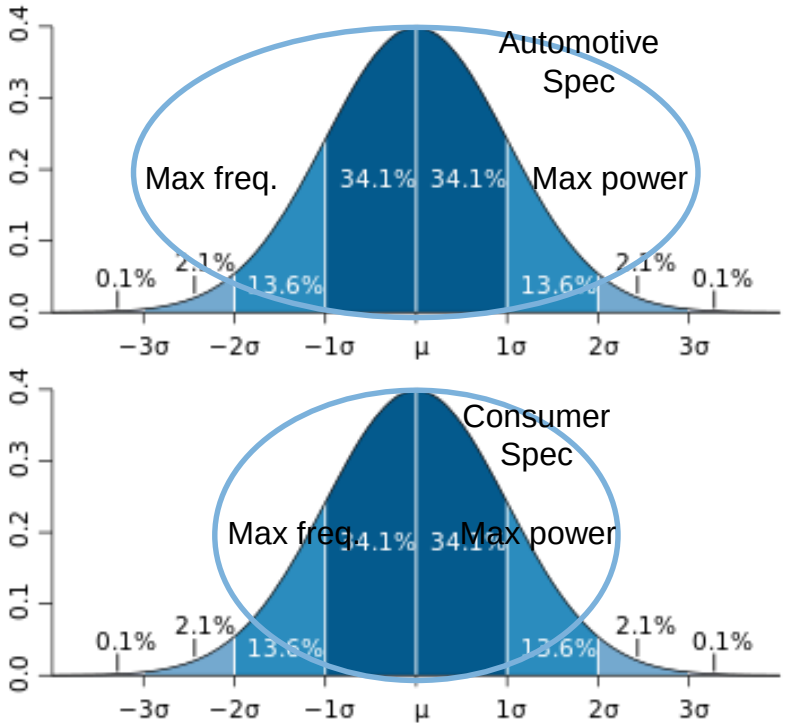
ISO26262 can NOT be retro-fitted !!!

Design Margin for Automotive Products

- Silicon designs must be simulated to ensure correct timing (Timing Closure) at all extremes of silicon Process, Temperature & Voltage (PVT)
- Temperature and Voltage are documented in the data sheet (0.9V +/-10%; -40deg C to 125 deg C Junction)
- Silicon manufacturing process yields a standard distribution between slow low power transistors & fast leaky transistors

Automotive simulates based on +/-3 sigma silicon process and defines spec limits based on this data.
Data sheet is “Guaranteed by Design”

Consumer simulates based on +-2.5 sigma silicon process and defines faster spec limit based on characterisation.
Data sheet is “Tested”

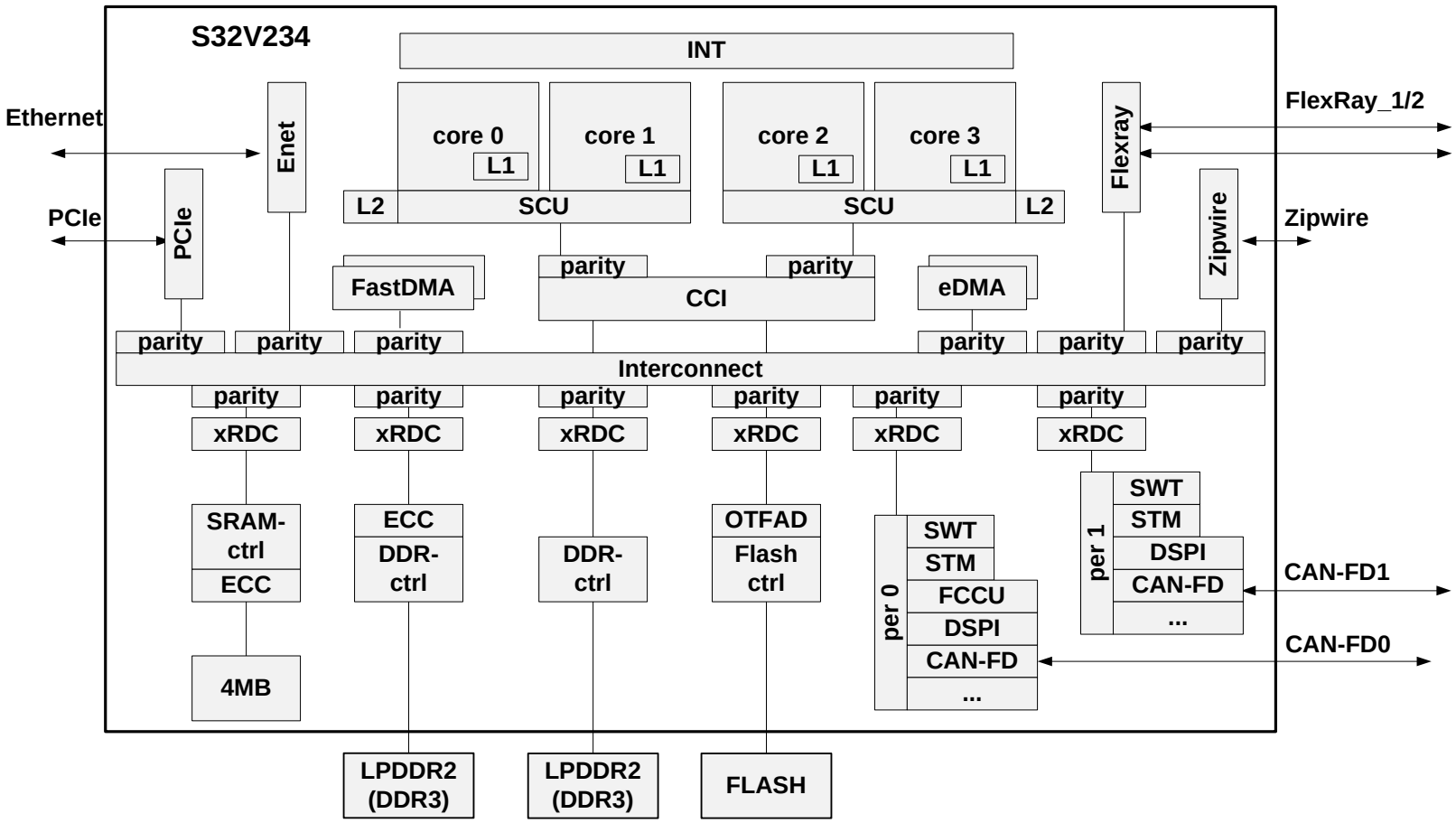


Assumed Safety Goals for Target Applications

Application / Safety Goals	ASIL	Behavior in Case of Fault
Adaptive headlight control	False positive: ASIL B False negative: QM	Fail-safe (Fail-silent or fail-indicate)
Driver assist functions (lane departure warning, blind spot detection, traffic sign recognition, obstacle/pedestrian detection, collision warning).	False positive: ASIL A False negative: ASIL A	
Mirror replacement	QM (redundant mirrors) / ASIL A (single mirror)	
Emergency brake (obstacle detection and emergency brake request).	False positive: ASIL B / ASIL C False negative: QM	
Collision avoidance (obstacle detection and active steering)	False positive: ASIL D False negative: QM	
Lane keeping	False positive: ASIL C False negative: ASIL C	
(Semi-) autonomous driving	False positive: ASIL D False negative: ASIL D (graceful degradation: maintain limited operation in case of a fault)	Failure-tolerant system (high availability system)

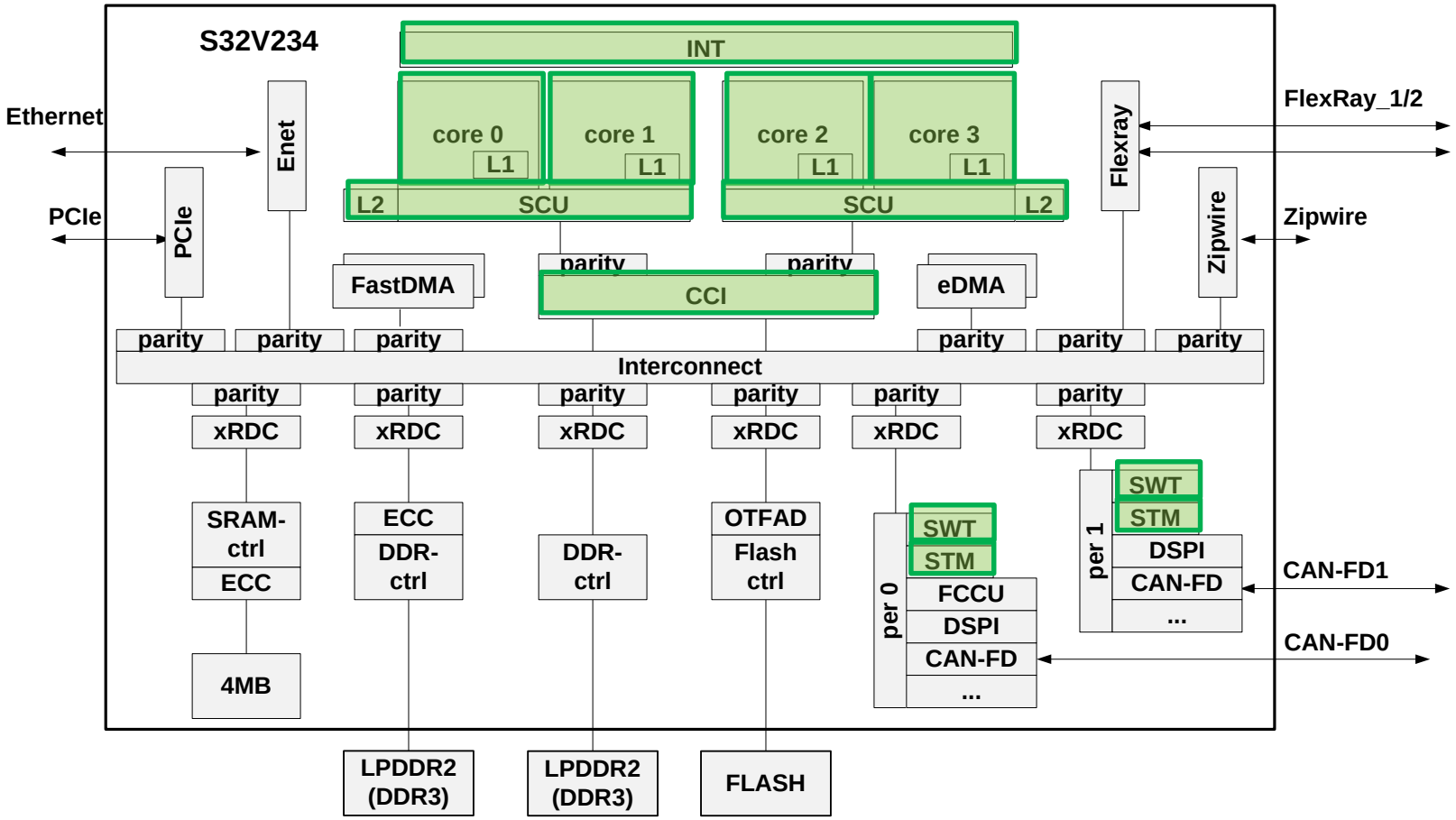
S32V34 Summary

- FSL ASIL D development process
- FSL ASIL D collateral
  - FMEDA, DFA, Safety Manual
- Many identical blocks with other MCUs targeting ASIL D
- HW-self-test
  - LBIST >90% coverage, MBIST >99% coverage



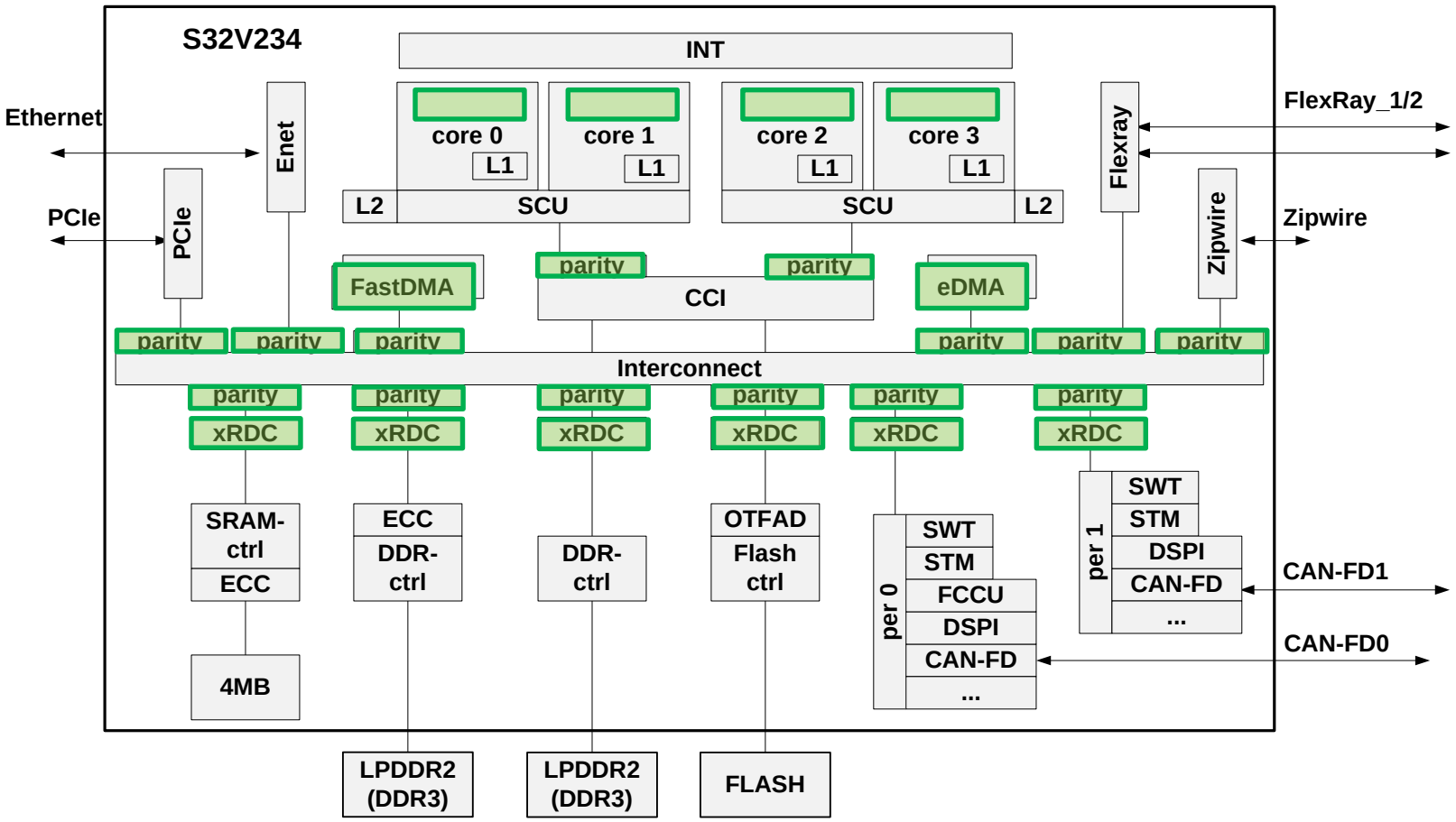
Core Cluster

- Program sequence monitoring (watchdog)
- Individual timers
- Low-latency interrupt monitor
- Snoop Filter with CCI-400 & Dual SCUs
- Core SW safety mechanisms (depending on safety concept), e.g.
  - Reciprocal comparison by software
  - Software Core Self-Test (within FTTI)
  - Temporal redundancy



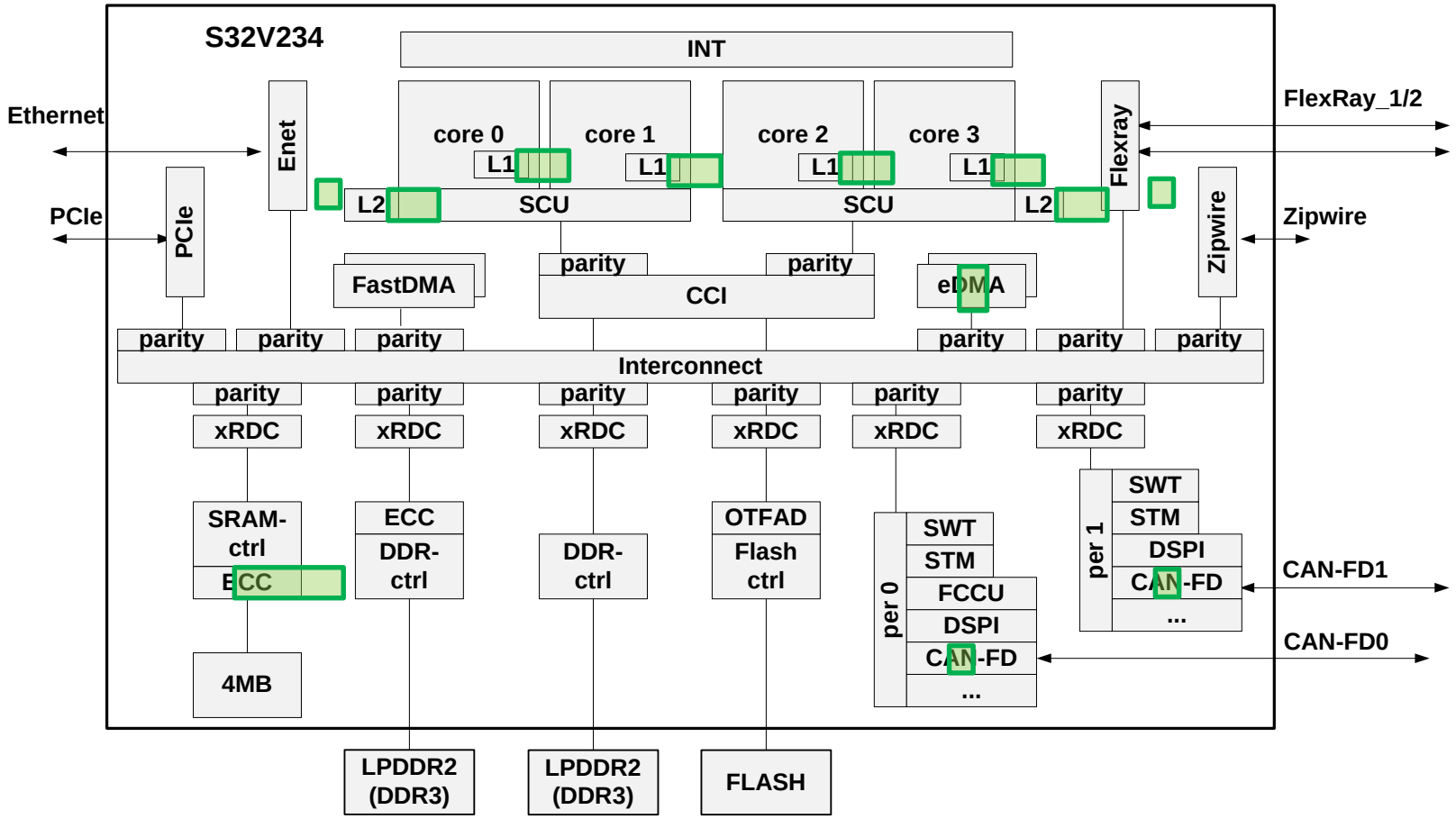
Bus System & Accesses Protection

- Multiple-parity protection on system buses
- FastDMA and eDMA in lock-step
- Resource Domain Controller (XRDC)
- MMU in A53
- Configuration Register protection



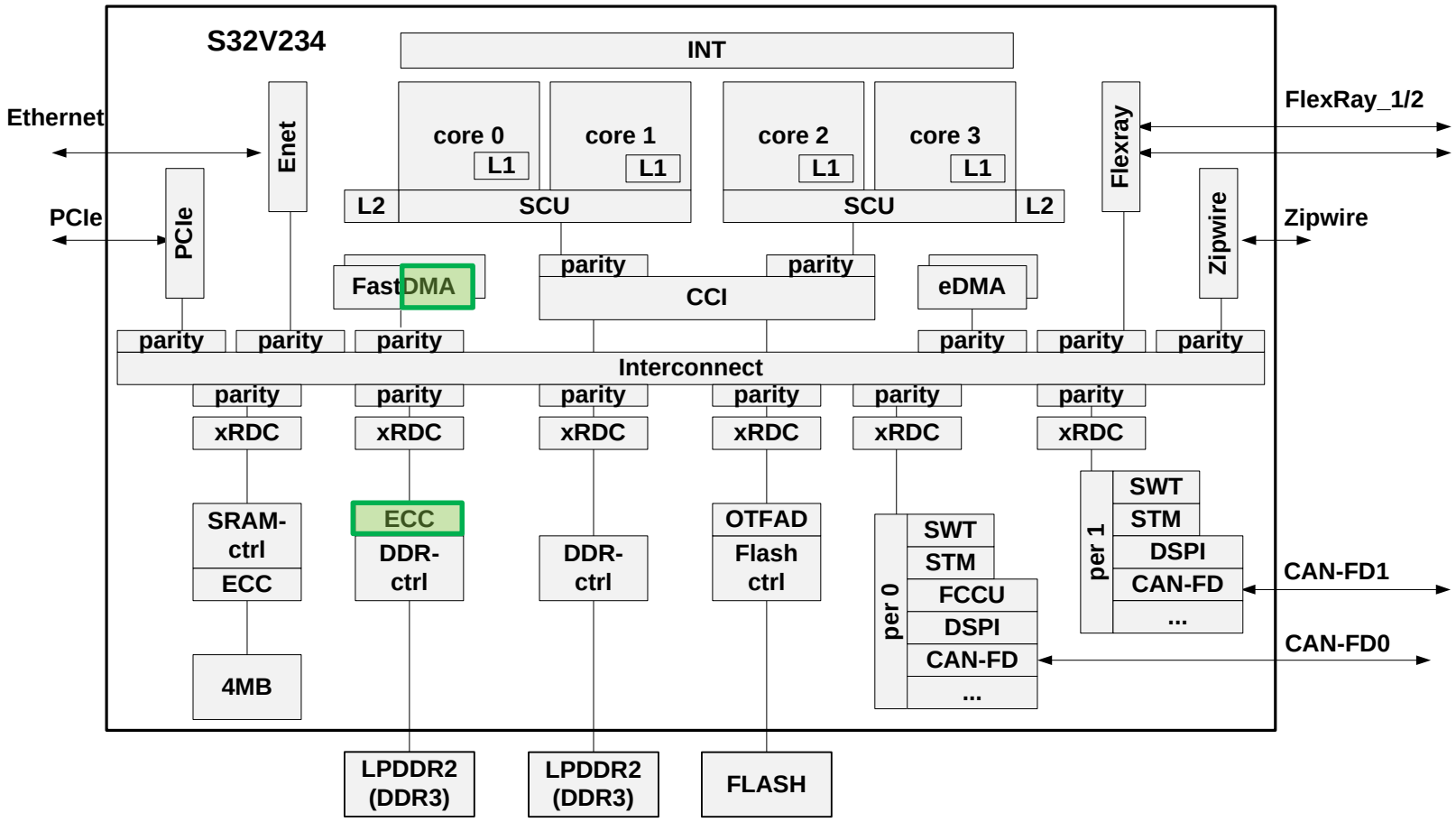
Volatile Memory (SRAM)

- E2E ECC on SRAM, TCM, and Data Cache
- Parity on Instruction Cache
- E2E ECC on FlexRay, FlexCAN, and Ethernet Buffers
- Don’t forget to initialize these memories before use!



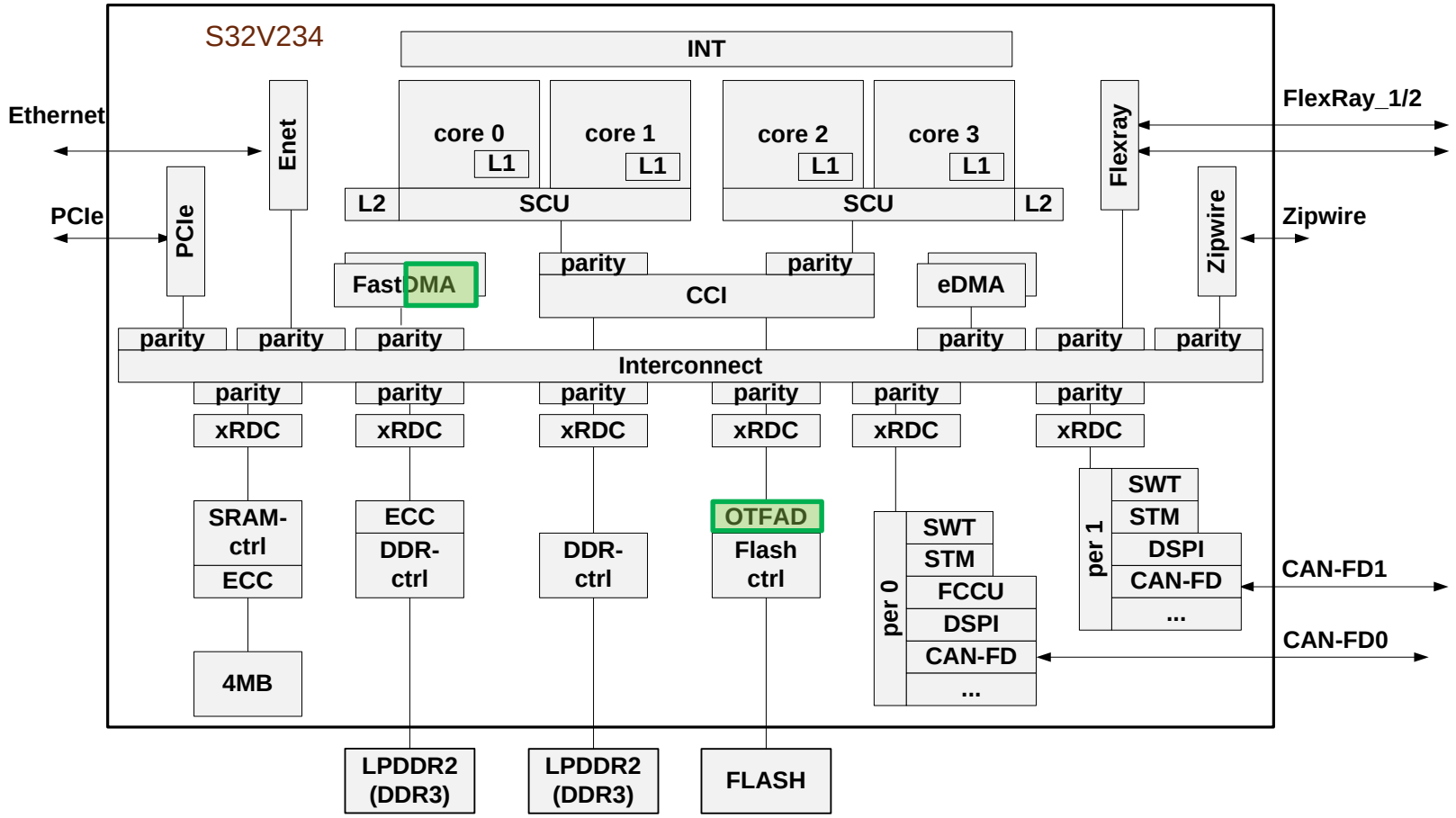
Volatile Memory (DRAM)

- Configurable region of memory which can be protected by ECC
  - SEC/DED/TED for data (single/dual and triple data errors are detected)
  - SED/DED for addresses (within the address range)
  - No additional memory device required for ECC



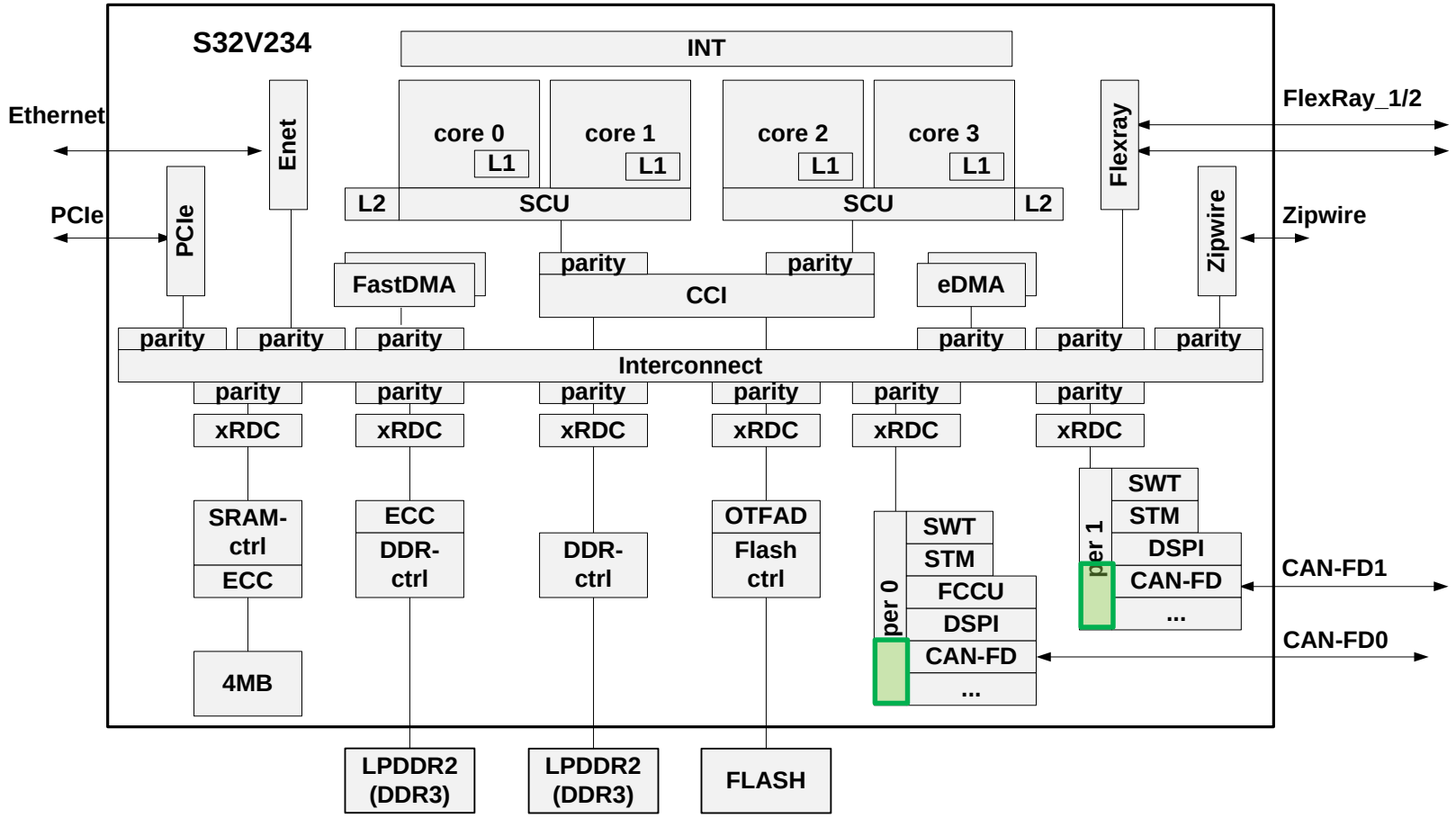
Non-Volatile Memory (FLASH)

- Simple error correction scheme (correction of one single bit failure for 32/128 KByte flash blocks)
- AES Decryption Engine
  - validate the fault freeness by decryption and authentication
- CRC calculation



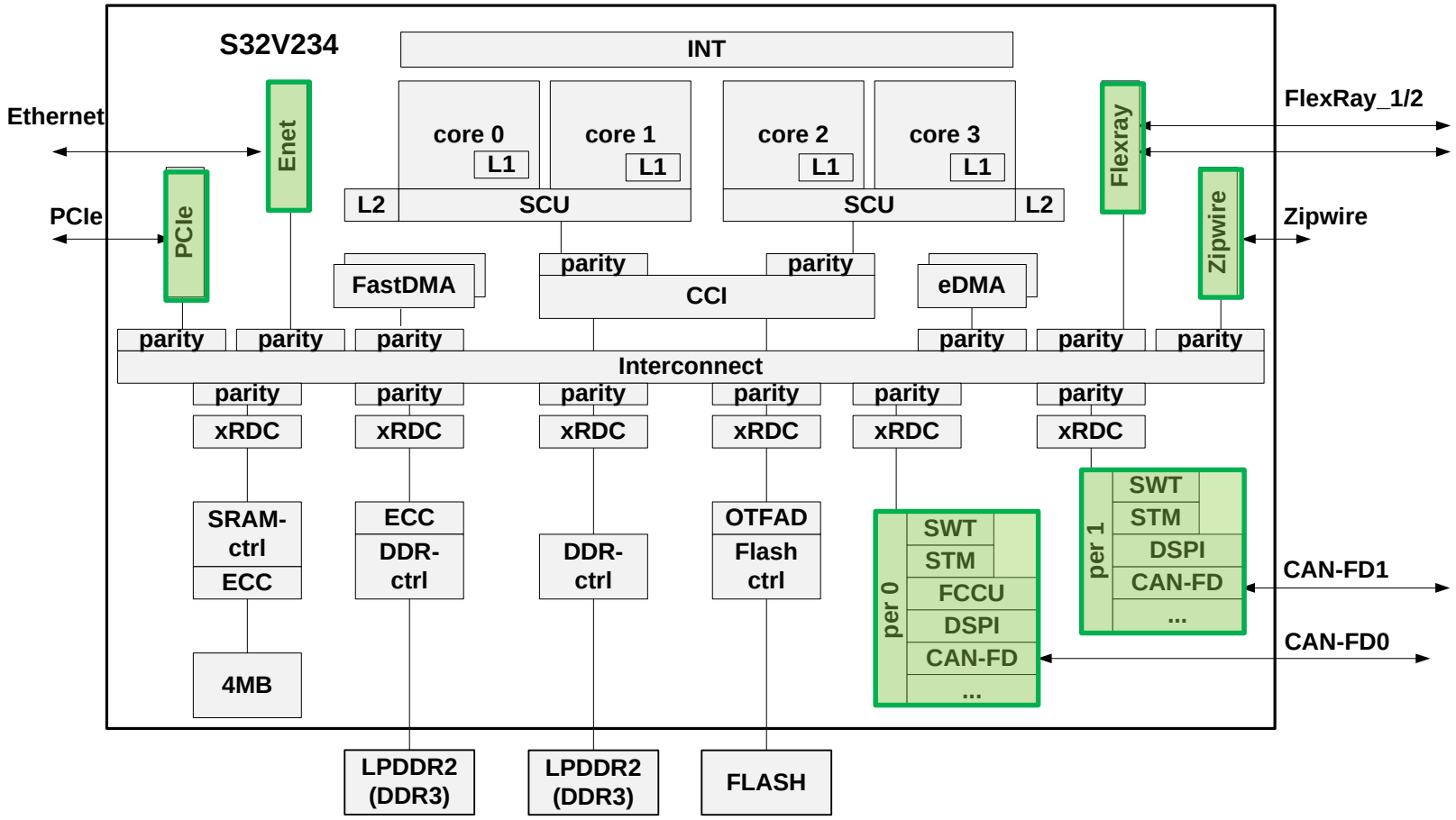
Clock, Power & Temperature

- Clock Redundancy (internal RC oscillator and XOSC)
- Clock monitoring
- Temperature Supervision/Sensing
- Supply Voltage Monitoring
  - under/over-voltage detectors
  - voltage level supervision with ADC



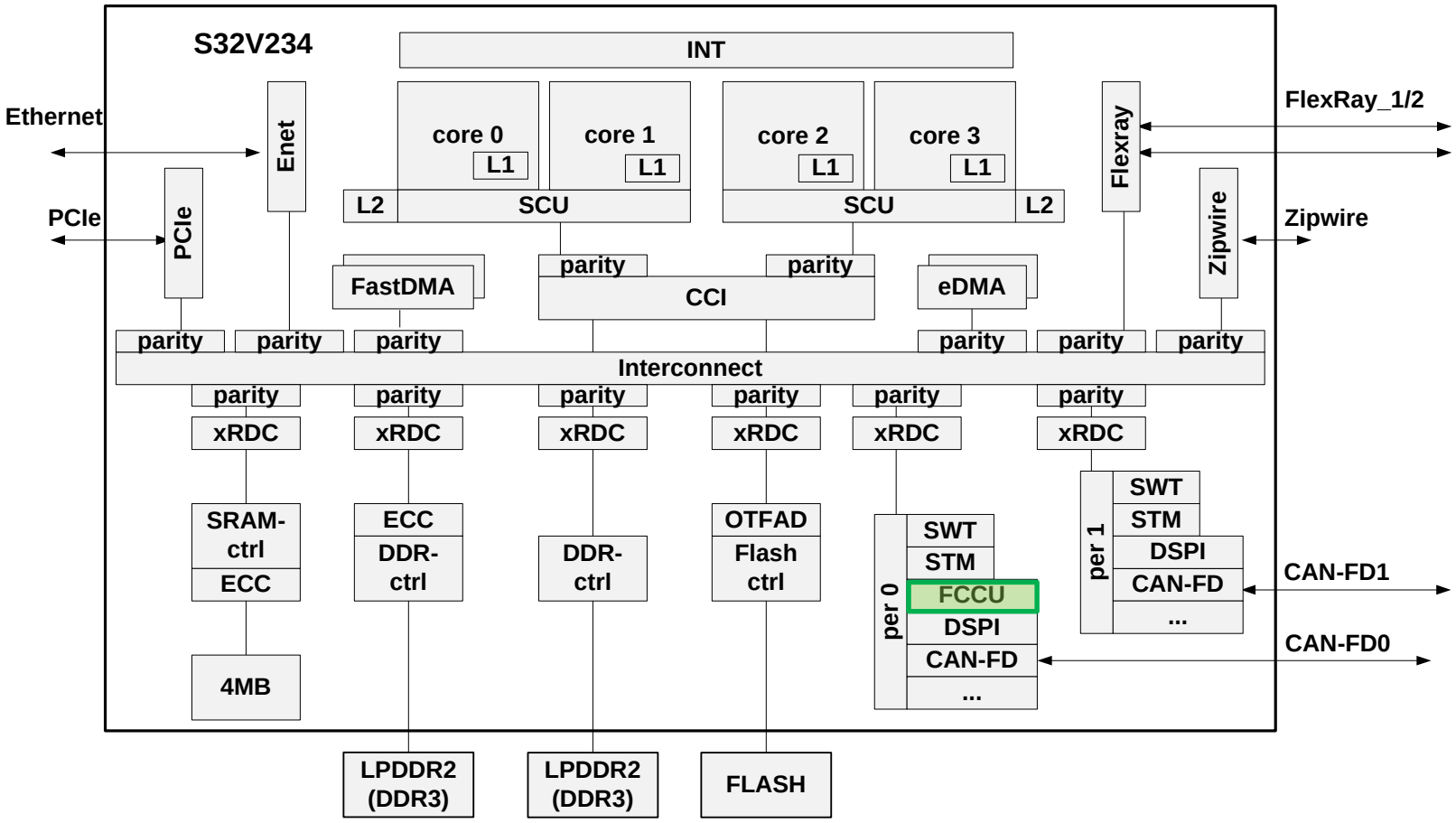
Peripherals & Communication

- Replicated and separated peripherals
  - Redundant usage by application
- Communication layer with SW-based safety protocol



Error Reporting

- FCCU – Fault Collection & Control Unit
  - Configurable Fault Detection
  - Alarm, Interrupt, Reset generation

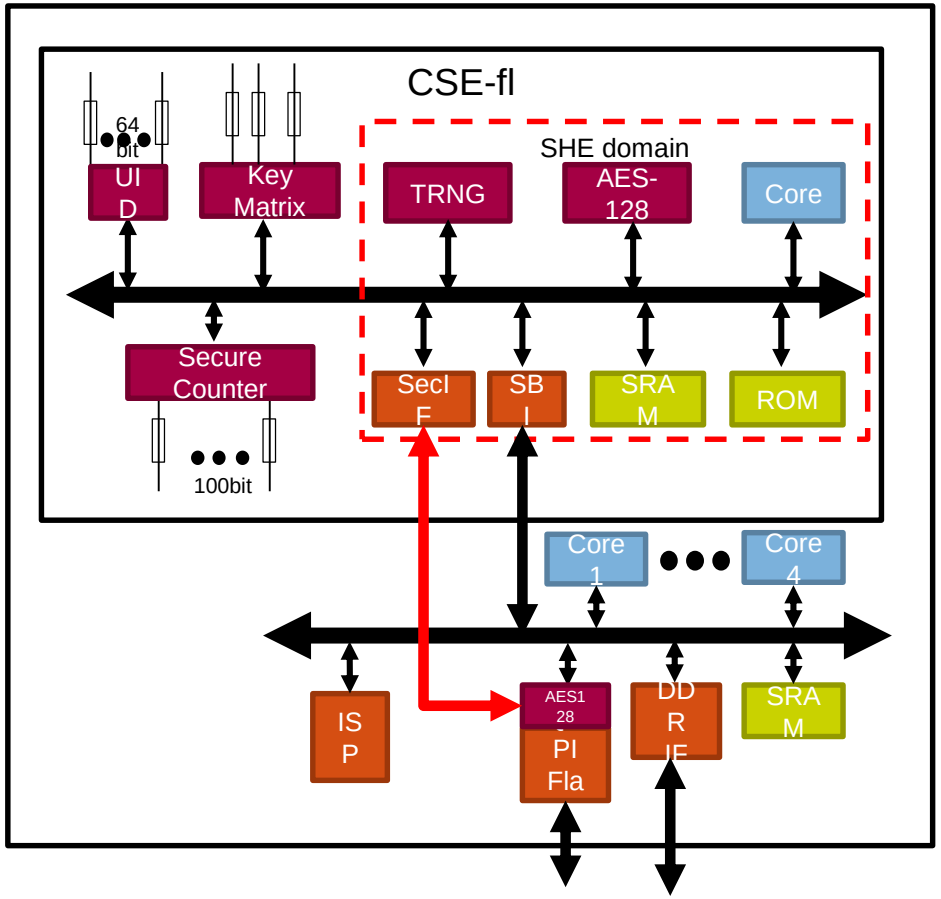


SECURITY

Cryptographic Services Engine (CSE-FL)

- Secure storage for cryptographic keys
- AES-128 encryption and decryption
- AES-128 CMAC authentication
- Random number generation
- Secure boot mode
- Secure RAM support
- System bus master interface
- Flashless

The CSE3 implements a comprehensive set of cryptographic functions as described in the SHE Functional Specification, including secure key storage, AES encryption, secure boot, AES CMAC authentication, and random number generation.

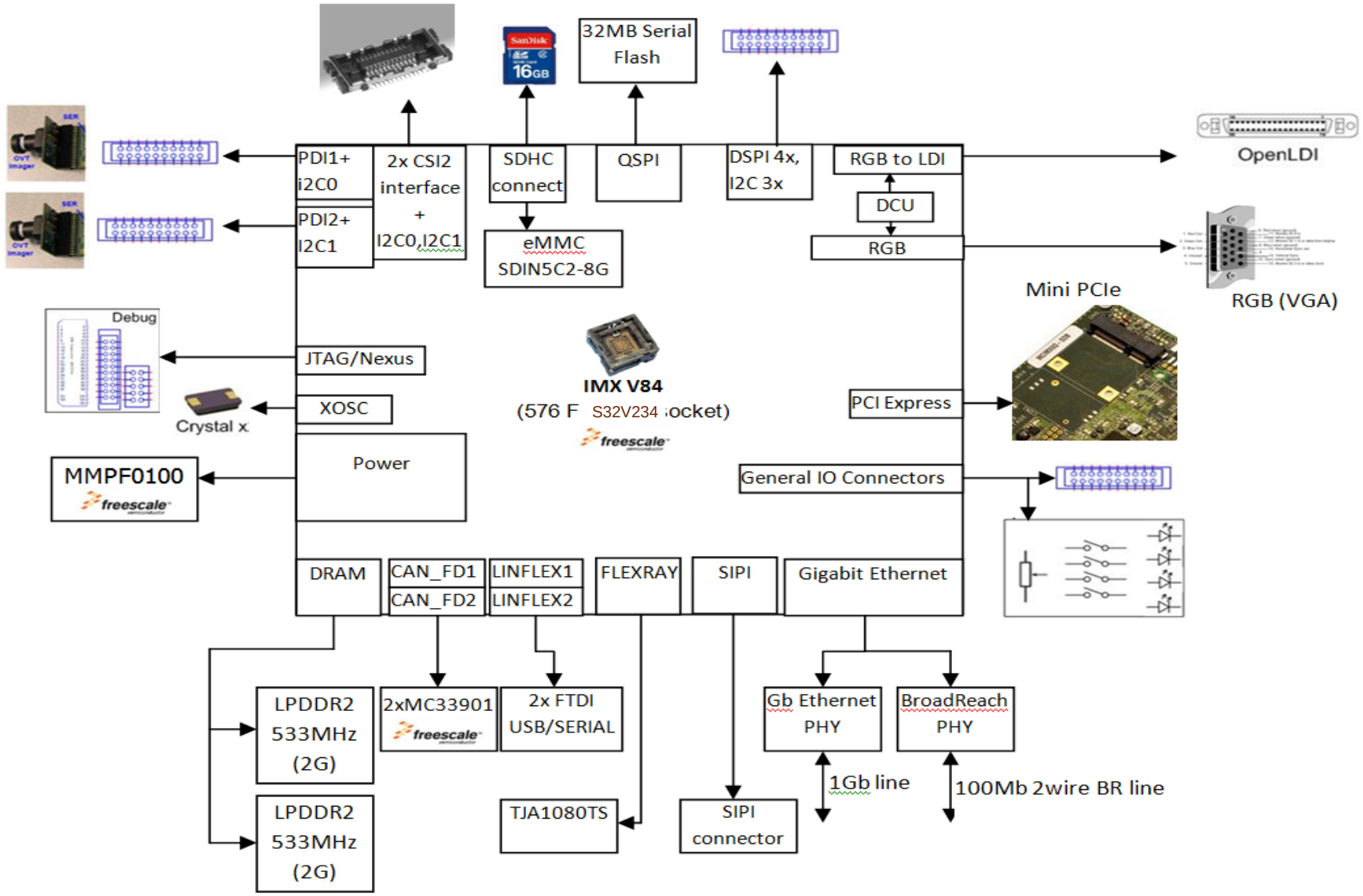


EVB

S32V234 Evaluation Board Picture

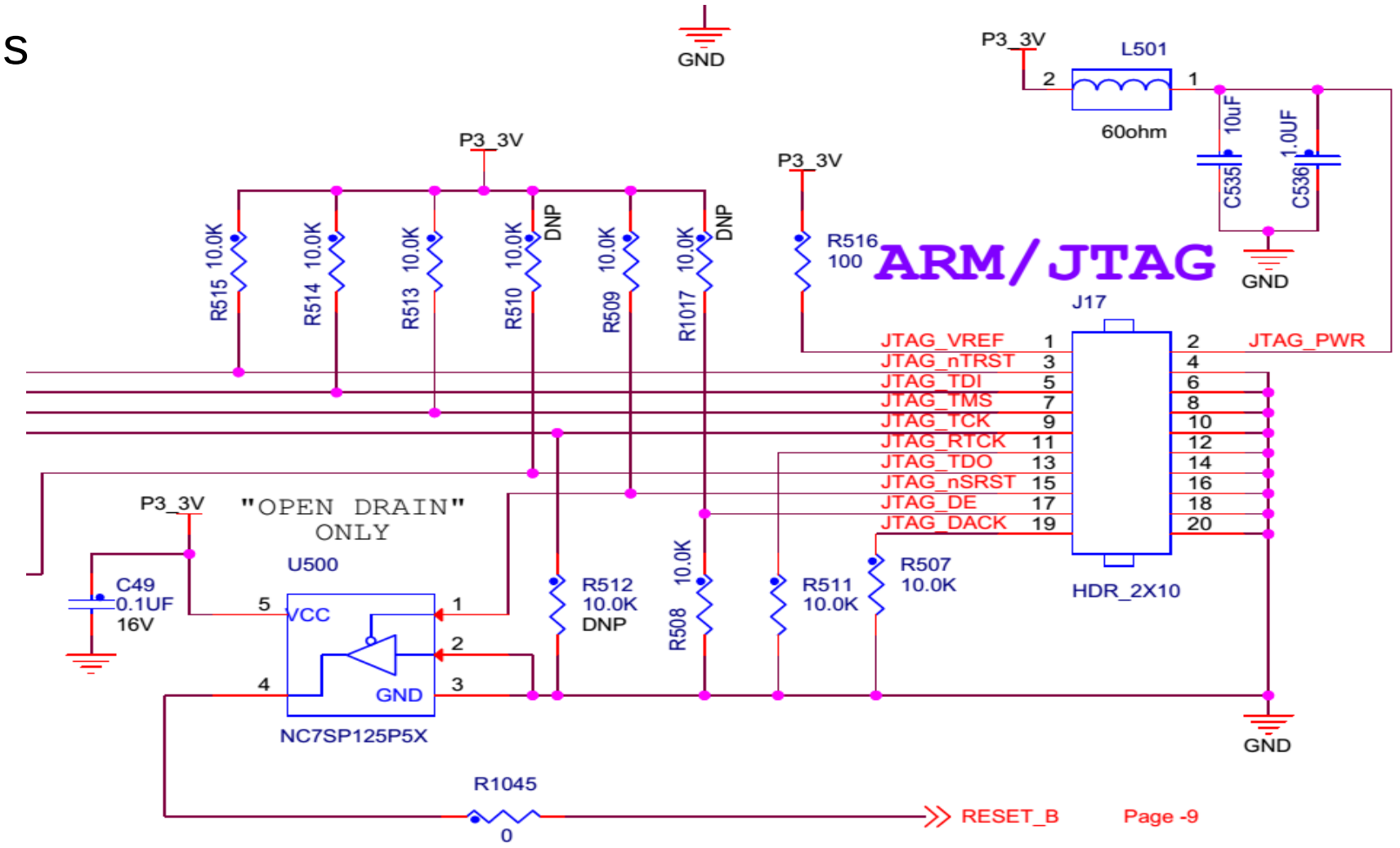
- Available Today
- Complete with
  - Display
  - CPU Fan!

S32V234 Evaluation Board



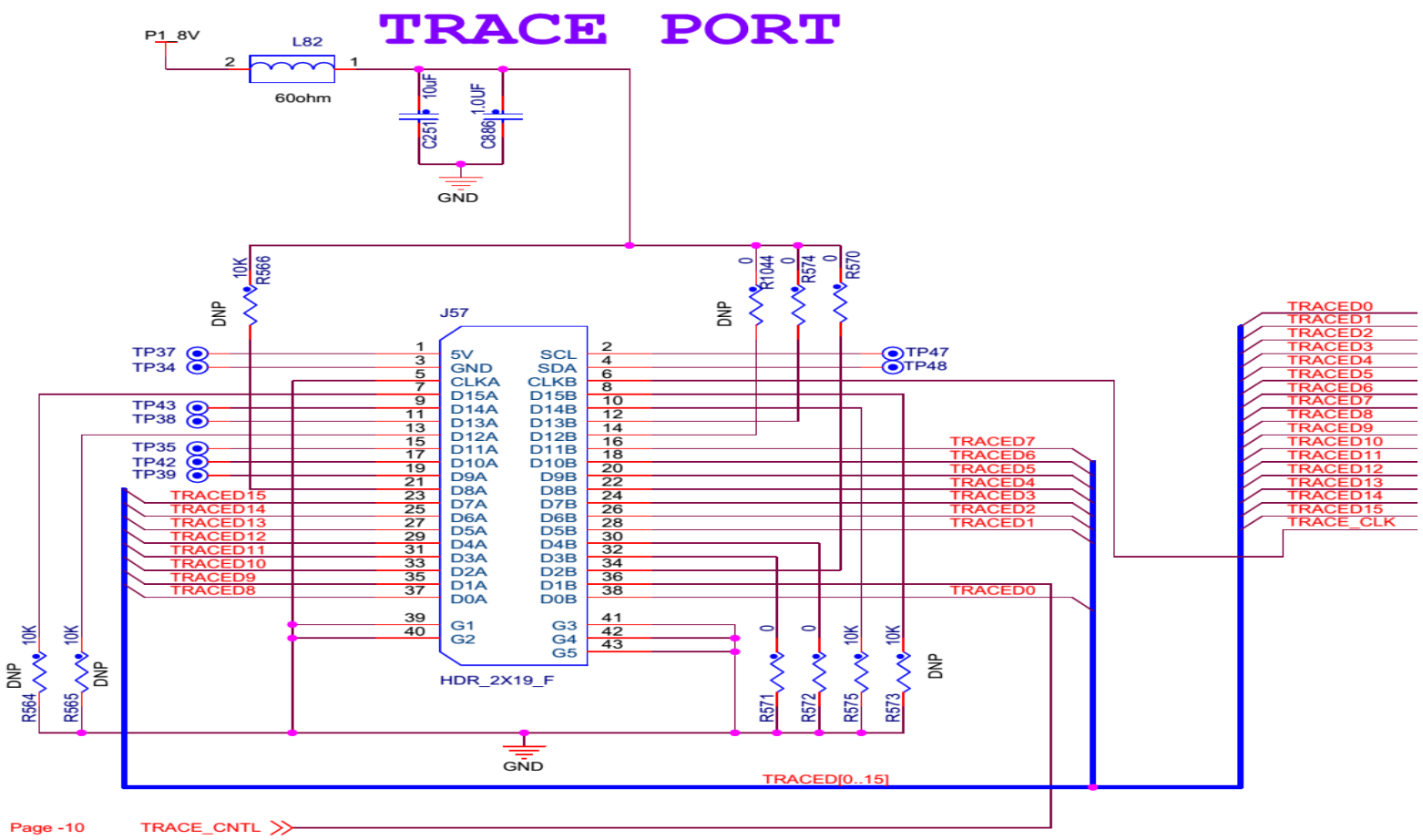
Debugger Connections

- JTAG Connections from EVB



Debugger Connections

- ETM Trace Port From EVB
- Note that the JTAG signals are not present on the Trace Port
- All Data Lines and TRACE_CNTL lines MUST be same length

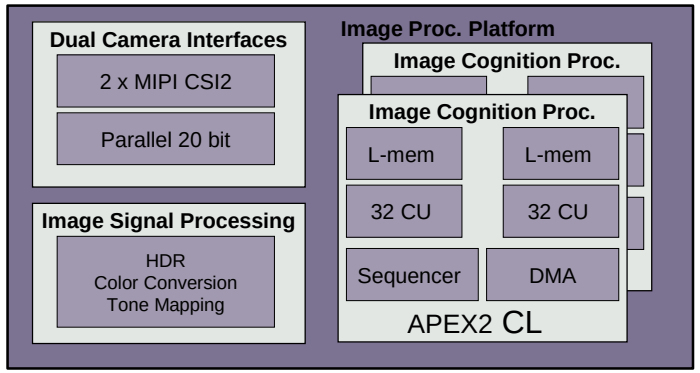


VISION & GRAPHICS

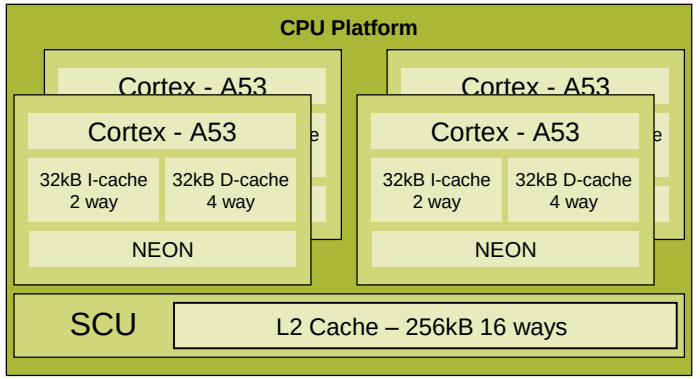
So, What is This All For Anyway?

Image Processing & Data Fusion

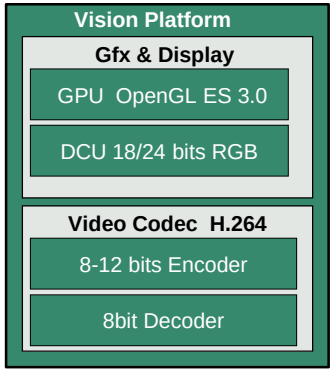
Image Pre-Processing	Features Extraction	Features Classification & Prediction	Multi Image Processing	Object Recognition & Fusion	Gfx Overlay & Video Distribution
• ISP • Multi-streams Connectivity	• Corners, • Edges, • Intensity gradients • shapes	• SVM • Adaboost • K-nearest Neighbor	• Tracking, Motion Estimation • Optical Flow & Disparity • Stitching	• Object Recognition/Pedestrian • Augmented Reality • Face Detection	• Safe Fusion • Graphic Overlay & Display • 2D vs. 3D Projection



High BW Operations
Scalable MIMD Local Memory
Soft ISP



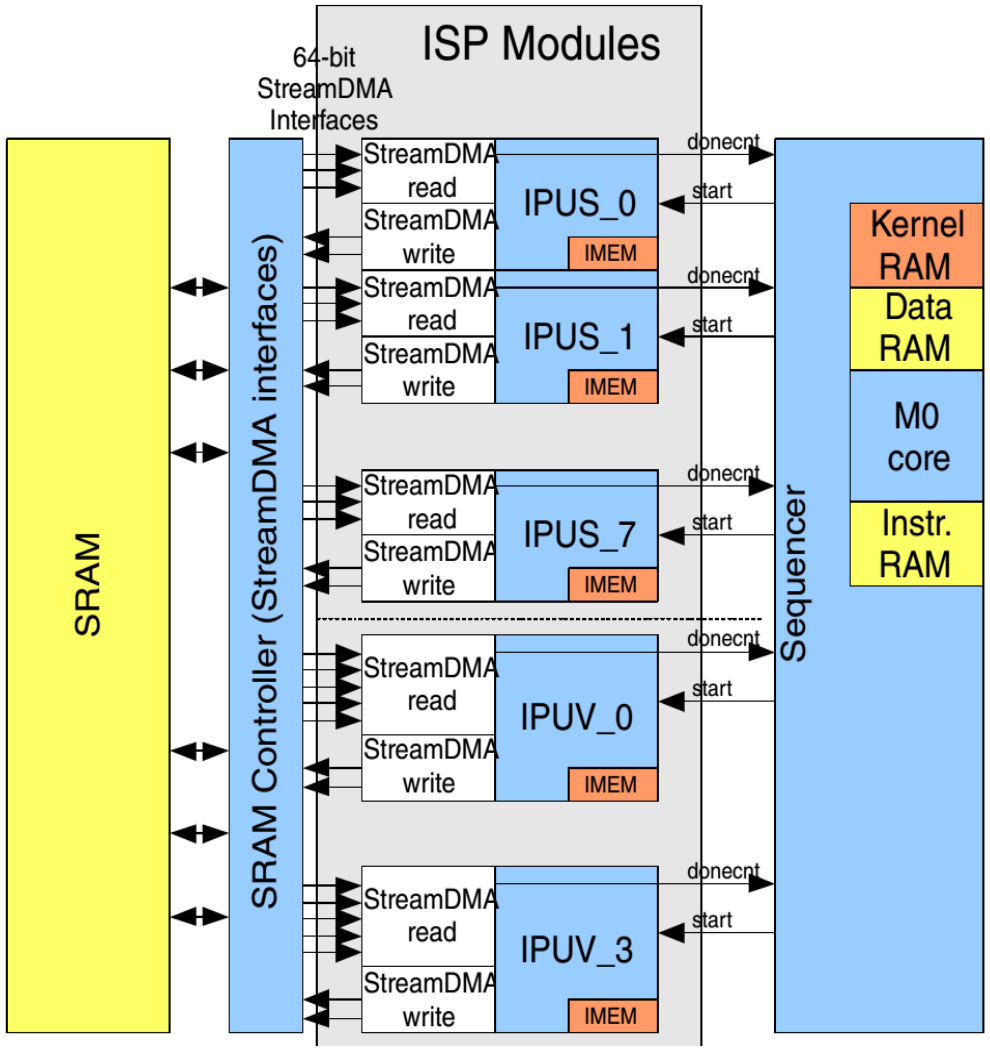
Scalable RISC – Data Fusion
SIMD Co-Processor - Neon
Memory Hierarchy and coherency



Graphic
Video Codec
Smart Display

Image Signal Processing Sub-System

- Multi Core IPU (image processing unit)
- Pipelined MIMD processing
- Each IPU is a DMA-processing engine
  - 8x Scalar (1 result at a time)
  - 4x 4way Vector SIMD (4 results at a time)
  - Total: 12x 500MHz = 6000MHz
- Multiple RISC instructions per cycle
  - Median Image: 89 RISC-Instr/cycle
  - Peak total > 0.5 T RISC-Instr/sec
- Sliding input window
  - 3x3 in scalar
  - 5x5 in vector
- HW accelerators in scalar engine
  - AdderTree, SorterTree, MatrixALU
  - Histogram: 4engines x 256bins x 32bits
  - Statistics:
    - 1engine x 4fields x 256objects(records) x 32bits
  - LUT: 2engines x 4Kelements x 16bits)
  - Best 5 of N (for optimization functions)
  - Saturation / Overflow mode in Signed and Unsigned
  - Dedicated channels for video encode/decode



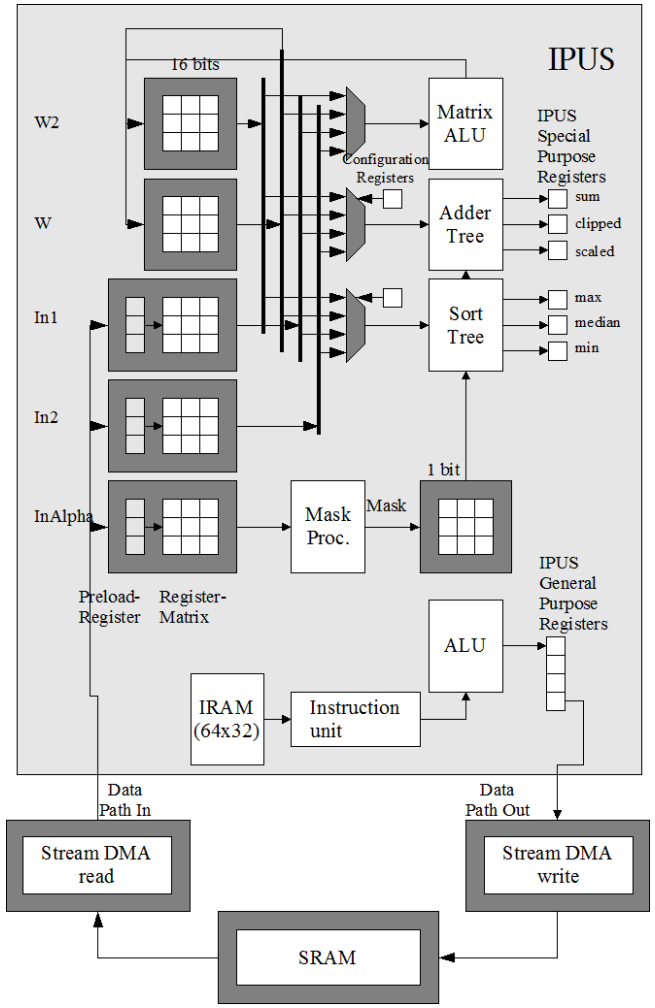
IPU Instantiation

Parameter	IPUS0	IPUS1	IPUS2	IPUS3	IPUS4	IPUS5	IPUS6	IPUS7
INA	X	X	X	X	X	X	X	X
INB					X	X		
INAlpha					X	X		
Output channels	1	3	4	1	3	3	1	1
LUT (words)			4K	4K				
Histogram engine	X	X	X	X				
Statistics engine								X
PRNG				X	X			
Best5ofN				X	X			

Parameter	IPUV0	IPUV1	IPUV2	IPUV3
Output channels	1	3	2	1

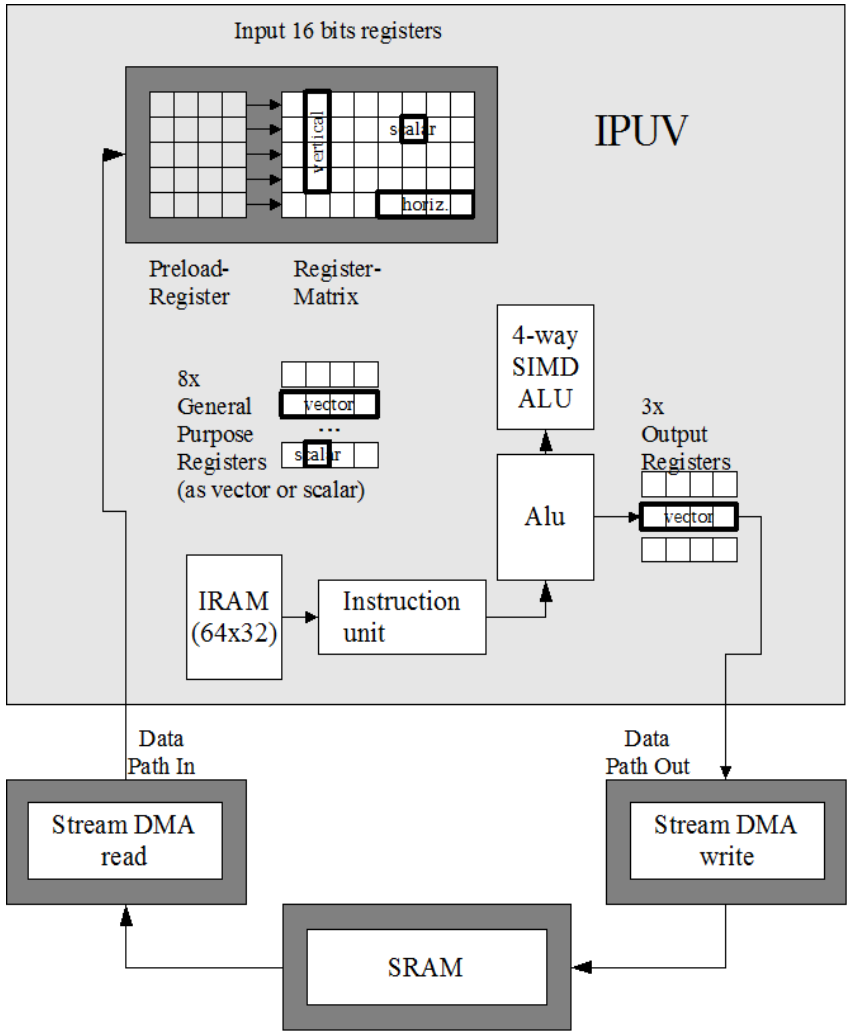
The Scalar Engine (IPUS)

- In1: 3x3 input window (or 9x1)
- Optionally In2 and InAlpha
- 1-4 output image lines
  - e.g. 1x R, 1x G, 1x B
- No data memory (no load/store), only registers
- Some accelerators for the 3x3 input window
- Matrix ALU (3x3 -> 3x3)
- Some more accelerators:
  - Histogram, PRNG, …
- Best apt for
  - rule based functions,
  - recursive functions,
  - functions with data dependencies
- 8 Engines



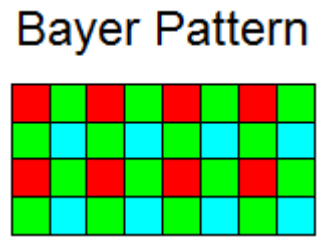
The Vector Engine (IPUV)

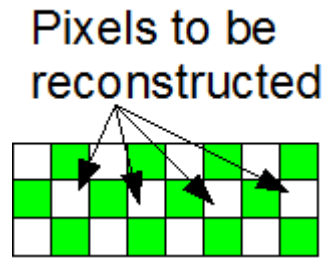
- In: 5x5 input window
  - Extended to 8x5 pixels
- 1-3 output image lines
- Scalar and 4-way SIMD ALU
- Addressing of vertical and horizontal vectors in input matrix
- No accelerators
- 4 Engines



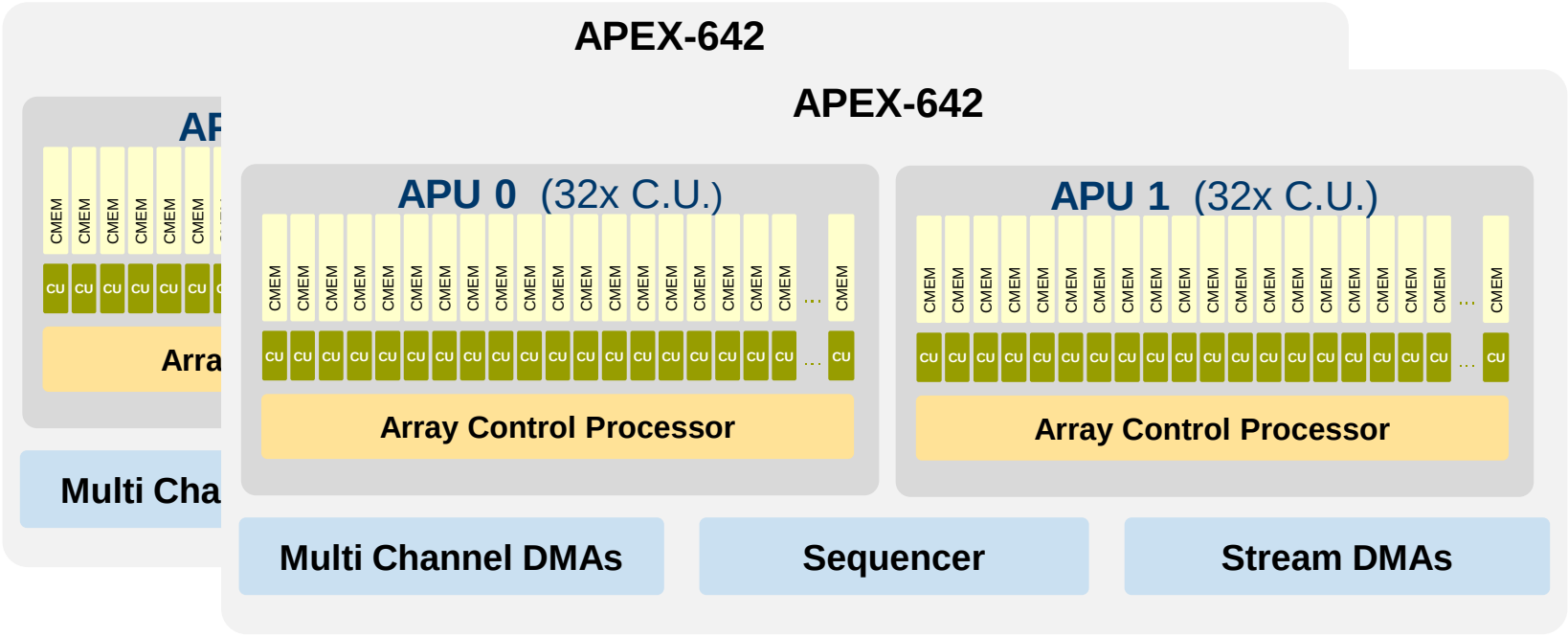
ISP Functionality

Function	Type
Black Level and Dead Pixel processing	LUT, Linked List
Black level, Vignetting	2D LUT (low res)
Exposure control, color balance analysis	Histogram/Stats
Geometric distortion corrections, chromatic aberration	calibrated per color, 2D LUT (low res), bi-linear interpolation
High Dynamic Range Imaging (HDR)	LUT, α-blending, conditional selection of exposure plane
De-mosaic Bayer pattern	Reconstruct missing Green values based on edge direction
RGB->YUV420, channel gain	Matrix multiplication, factors based on Histogram
Spatial de-noise	Edge aware thresholding
Gamma correction	LUT
Image Scaling	Anti-alias (FIR), bi-linear interpolation





APEX-642 – Programmable Image Cognition Processor



2 x APEX2 - 642 blocks

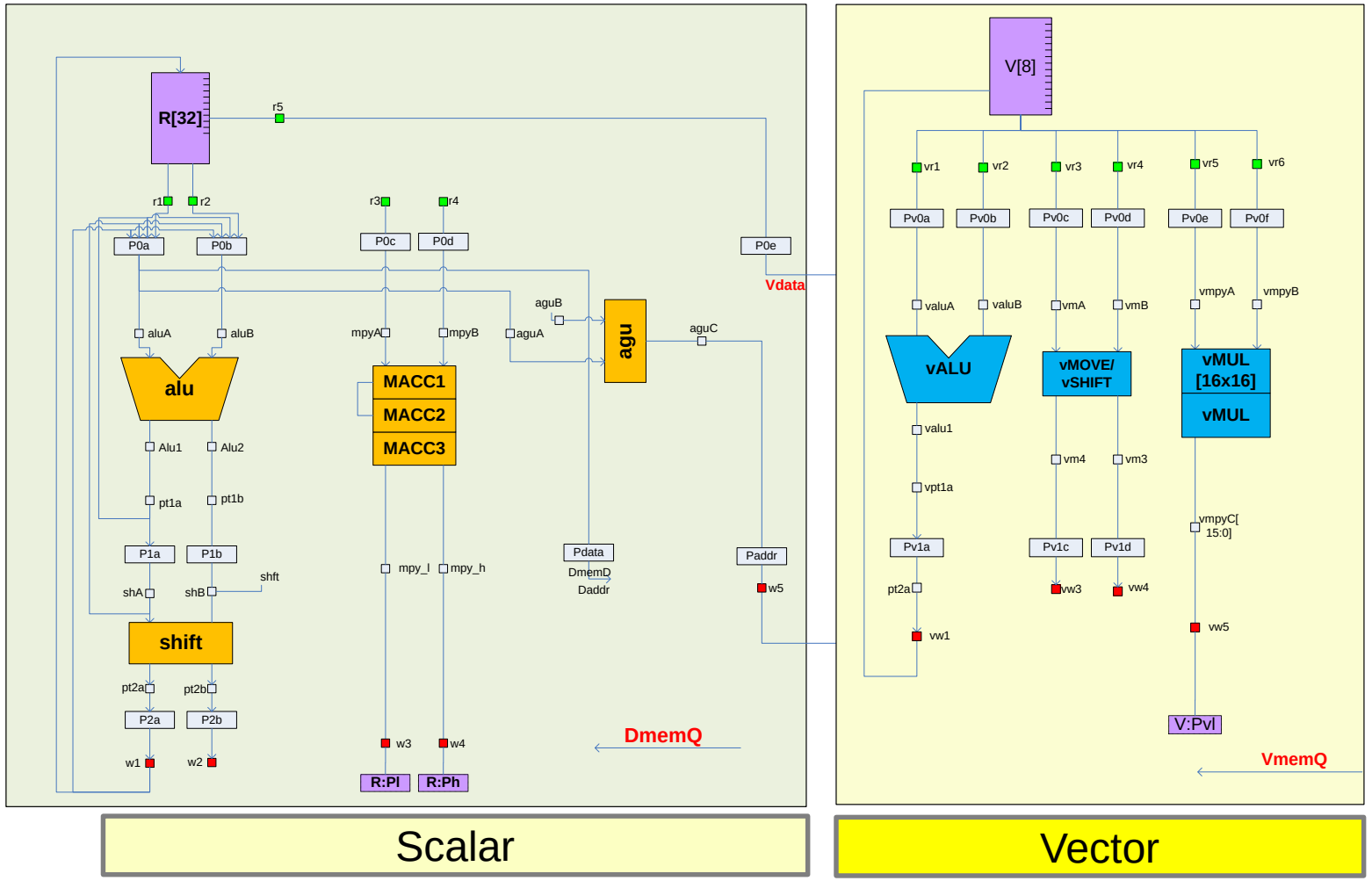
2 APEX-642 =

2 x (32 x 2 C. U. , 2 ACP, 256KByte ram) =

128 C.U. 4 ACP 512KByte RAM - 2 complex DMA

APEX642 – CU Architecture Overview

Scalar and Vector processors have his own separated address space and stack



APEX Gen 2 DMA Architecture

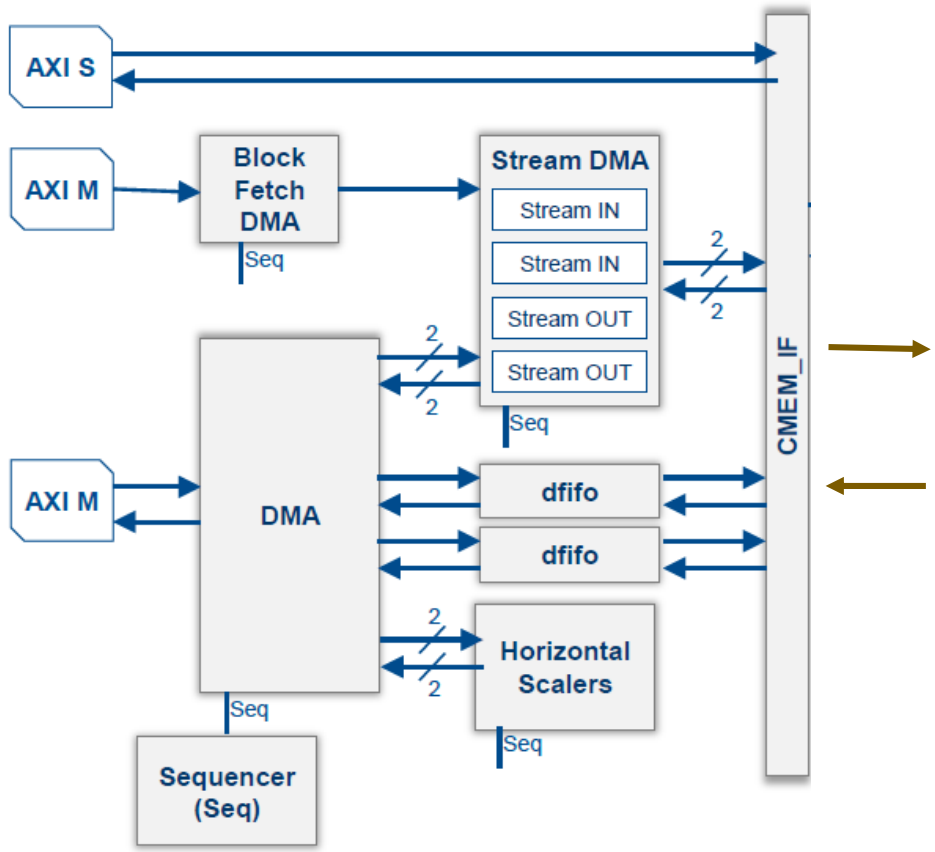
128bit AXI3
- 2 Master AXI3 (1-ReadWrite; 1-ReadOnly)
  – Only utilized for data transfer
- 1 Slave AXI3
  – 1 Slave AXI3

- **Multi Channel DMA**
  – K Channels dictated by system use case for Area optimization
  – Amount of Source and Destination Peripherals Configurable
  – Optional external Source/Destination for external HW Accelerator (3D Engine)
    • Must be ACF Aware for Resource Management

- **Stream DMA**
  – N stream IN and M stream OUT channels supported.
    • N/M dictated by system use case, for Area optimization
  – Converts from CU data format to system data format.
  – Highly configurable to support different data formats (YUYV4xx, YUVPlanar, UV planar, RGBIr, etc).

- **Block Fetch DMA**
– DMA specialized to move small scattered 2D data blocks.
– Single Channel, mem2per
– Linked list capable

DMA micro-machine
sys clk domain = 266MHz



APEX Typical Functions - Any Kernel Based Filter

- Sobel X
- Median
- Histogram
- Integral Image
- FAST
- BRIEF
- ARB
- FIR
- Kirsh
- Laplace filter
- Gaussian
- RGB to YUV
- YUV 2 RGB
- YUV 420 to RGB565
- Harris Corner
- Shi–Tomasi Corner
- Lens Correction

GC3000 Graphics Processing Unit

- OpenGL ES 3.1, including mandatory extensions and Android Extension Pack (AEP)
- OpenGL ES 3.0 / 2.0 / 1.1
- OpenVG 1.1
- IEEE 32-bit/16-bit floating-point pipeline
- Ultra-threaded, unified vertex and fragment (pixel) shaders
- Low bandwidth at both high and low data rates
- Low CPU loading
- Up to 16 programmable elements per vertex
- Dependent texture operation with high-performance
- Alpha blending
- Depth and stencil compare
- Point sampling, bi-linear sampling, tri-linear filtering, and cubic textures
- Resolve and fast clear
- 8k x 8k texture size and 8k x 8k rendering target
- 3D Composition engine
- Secure MMU support
- Wide AA line support
- Primitive restart support
- Software programmable Big Endian support
- Performance Counters for DMA Profiling
- Frame buffer compression support

SECURE CONNECTIONS
FOR A SMARTER WORLD

ATTRIBUTION STATEMENT