



**FTF 2016**  
TECHNOLOGY FORUM

# DDR SYSTEM DESIGN USING IBIS MODELS

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FTF-DES-N1854  
MAY 18, 2016

PUBLIC USE



# AGENDA

- DDR Bus Topology Overview
- Data Bus
- MCK and Address Bus
- DDR TOOLS – QCVS
- IO Buffer Models for DDR
- Basic Simulation Examples
- PCB Design Considerations for DDR

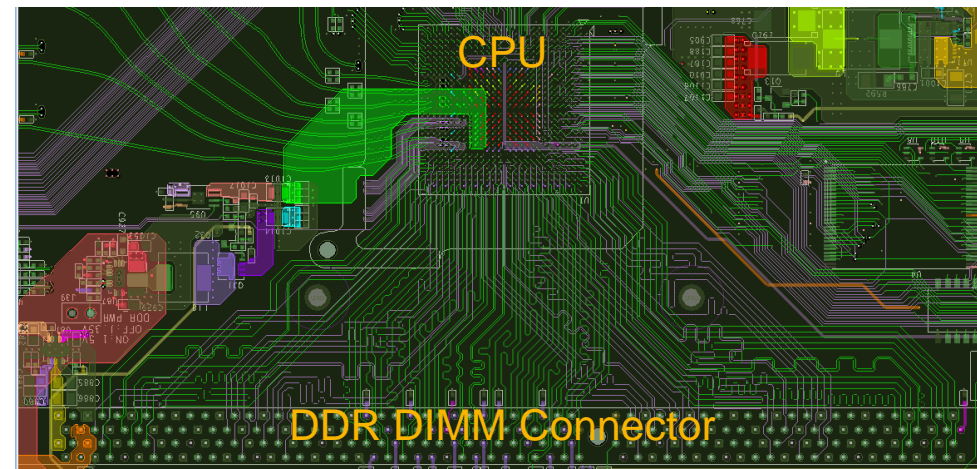
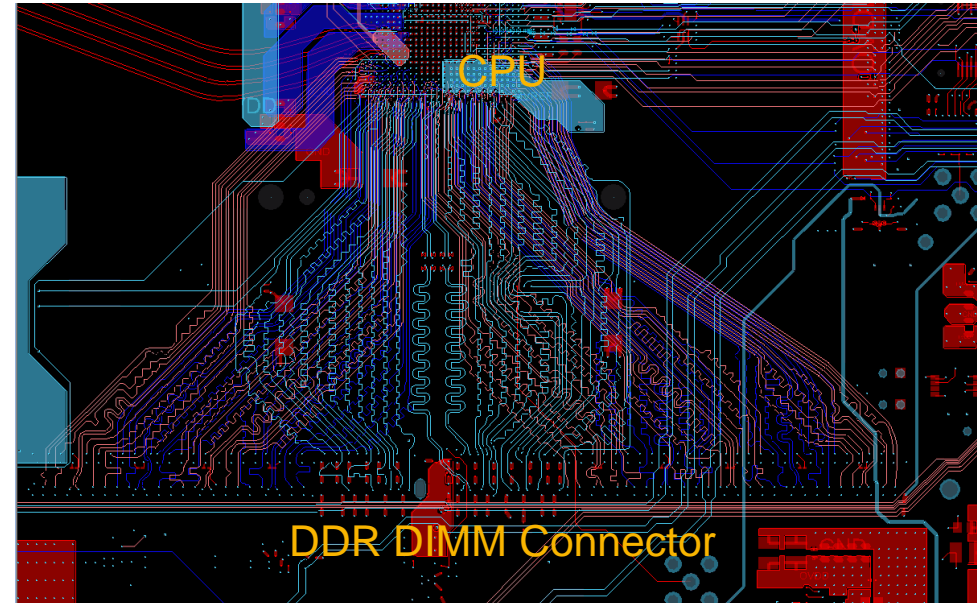
# DDR BUS TOPOLOGY OVERVIEW

# DDR Bus Overview

- Source Synchronous Bus
- Large, parallel bus
- Bus timing
  - Strobe to Data (DQS to DQ)
    - DDR Dual Data Rate – DDR bus is DQ
  - Clock to Address/Command/Control (MCK to ADDR,CMD,CNTL)
    - Not Double Data Rate
  - Clock to Strobe (MCK to DQS)
- PCB Applications
  - DIMM-based
  - Memory-Down Discrete-Memory based

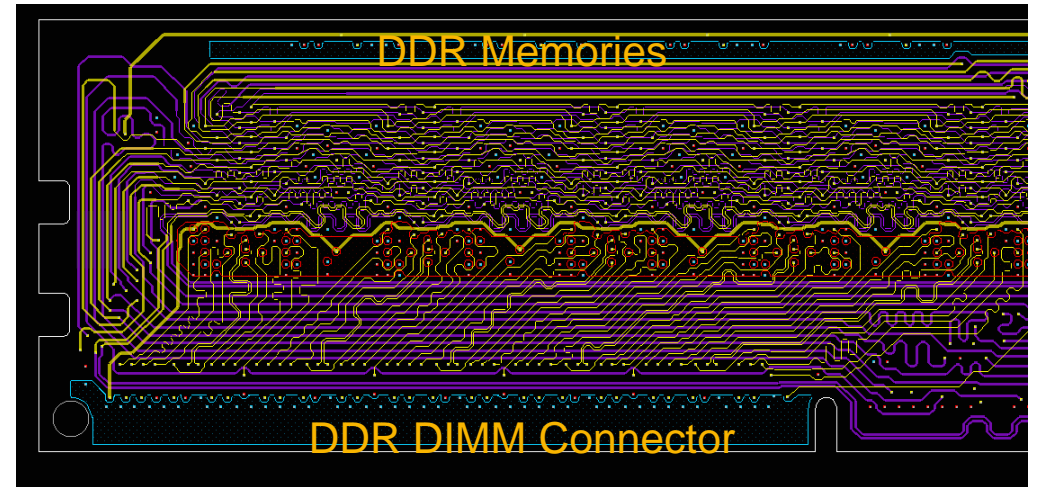
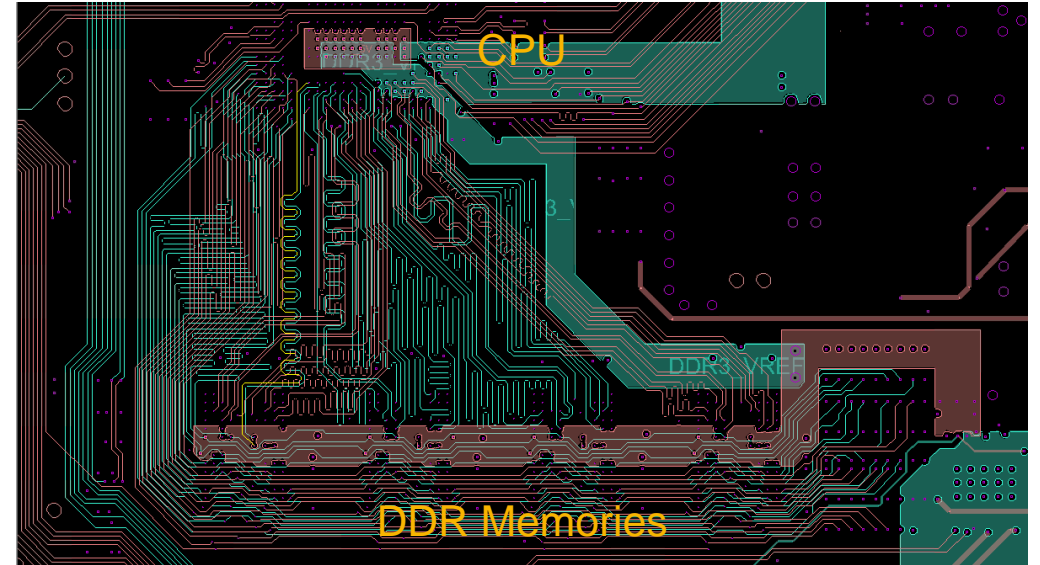
# DIMM-based Design

- PCBs with DIMM connector
- Note Data vs. Address Bus
- Number of Layers
- Alternating Layers for Byte Lanes
- Mostly/usually stripline routes



# Memory-Down Design

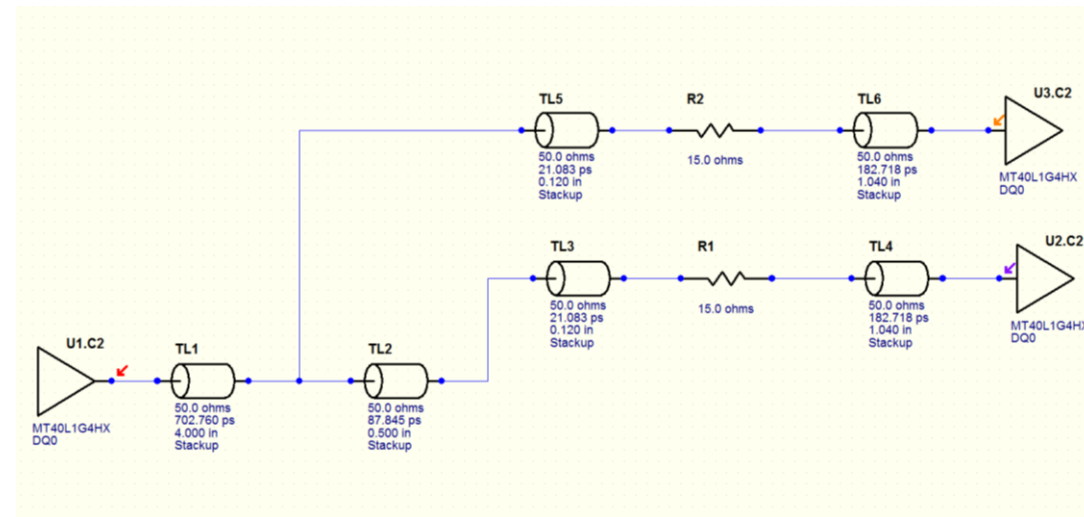
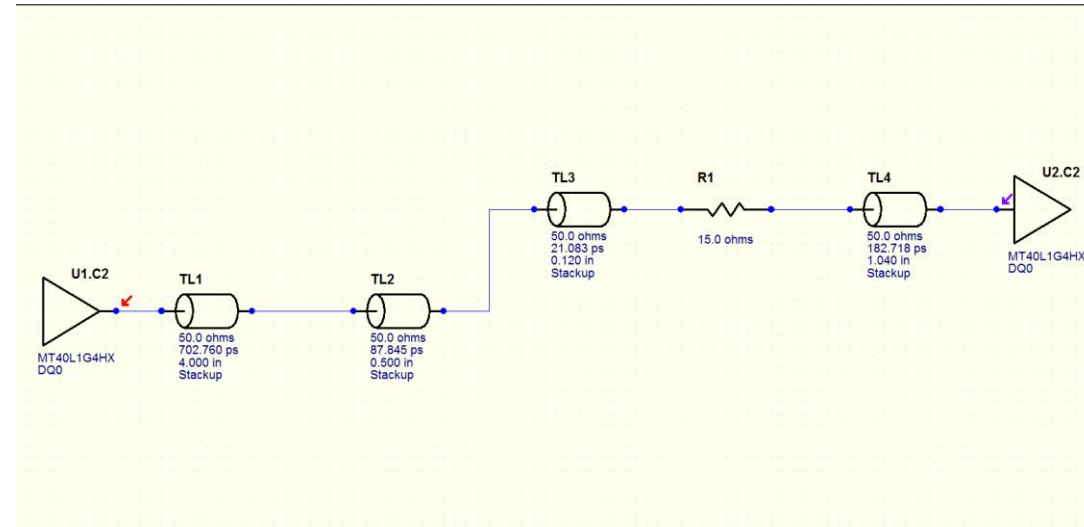
- PCBs with on-board memory
- Note Data vs. Address Bus
- Lighter loads often
- If lower layer count PCB, can be congested



# DATA BUS

# Data Bus Topology

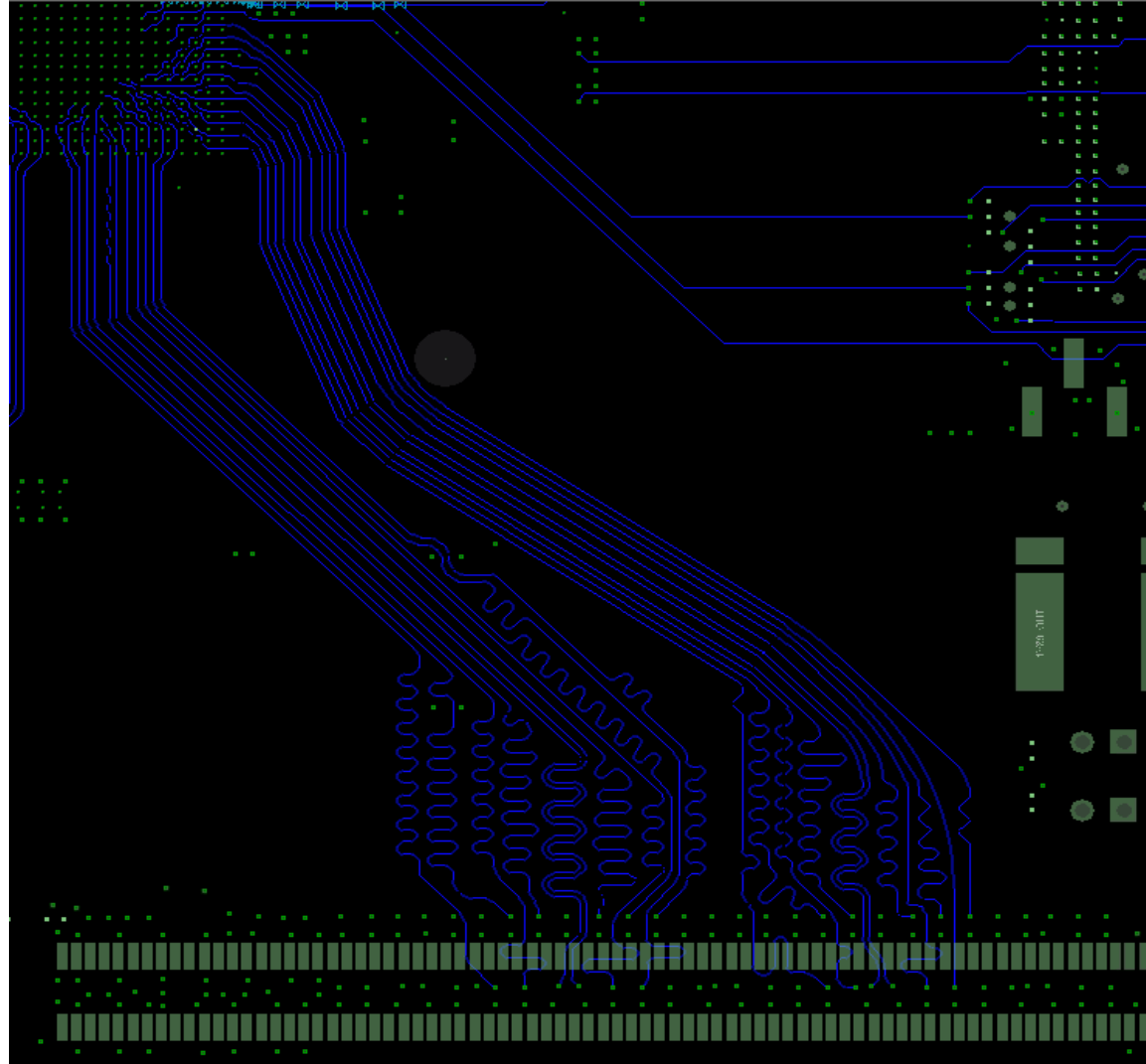
- Driver
- Receiver
- PCB
- Termination on Board?
- Details to Optimize
  - Driver Strength
  - PCB Impedance
  - Receiver ODT





# DQS-DQ

- DQS Diff Pair
- Byte Lane
- Read/Write De-Skew



# Byte Lanes

- Note Alternating Byte Lanes

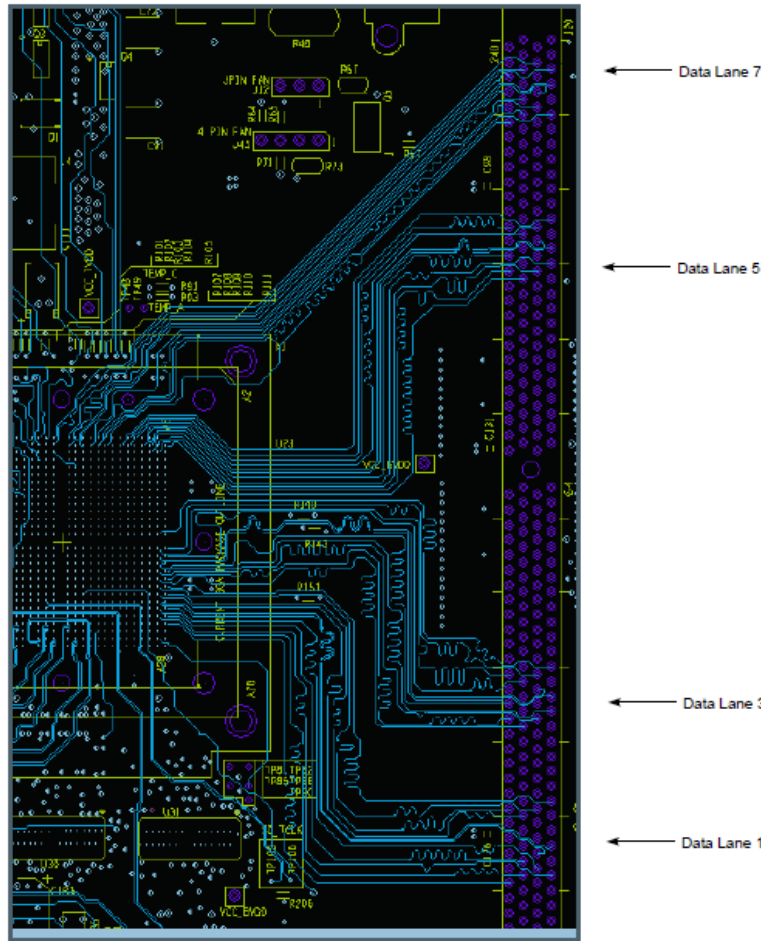


Figure 1. Alternating Data Byte Lanes on Different Critical Layers—Part 1

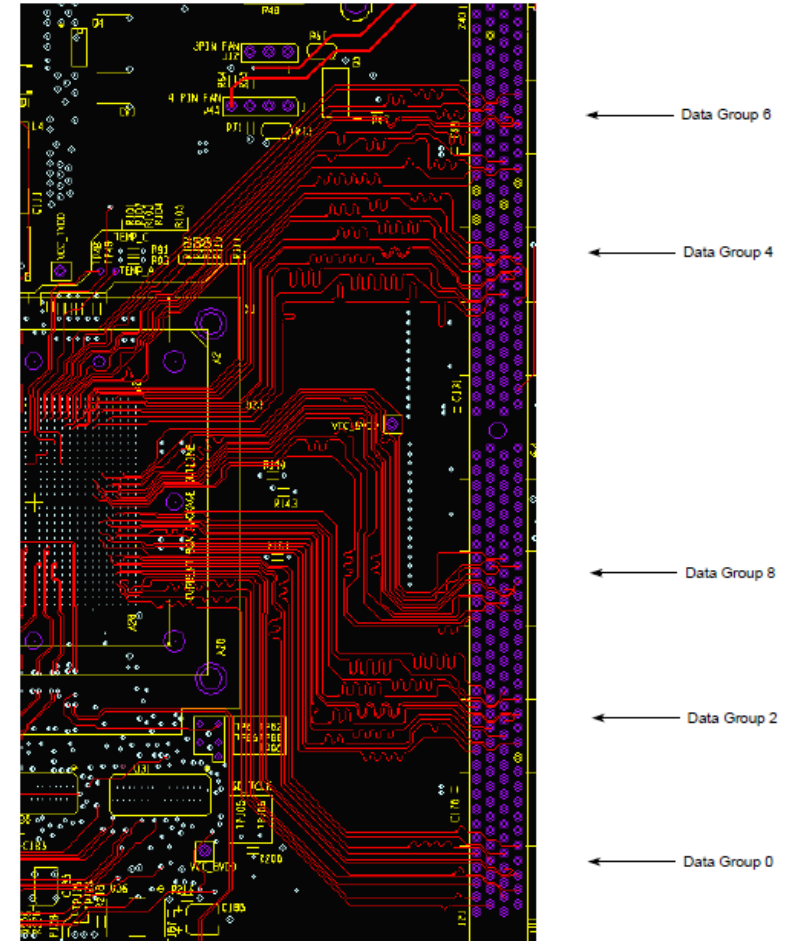
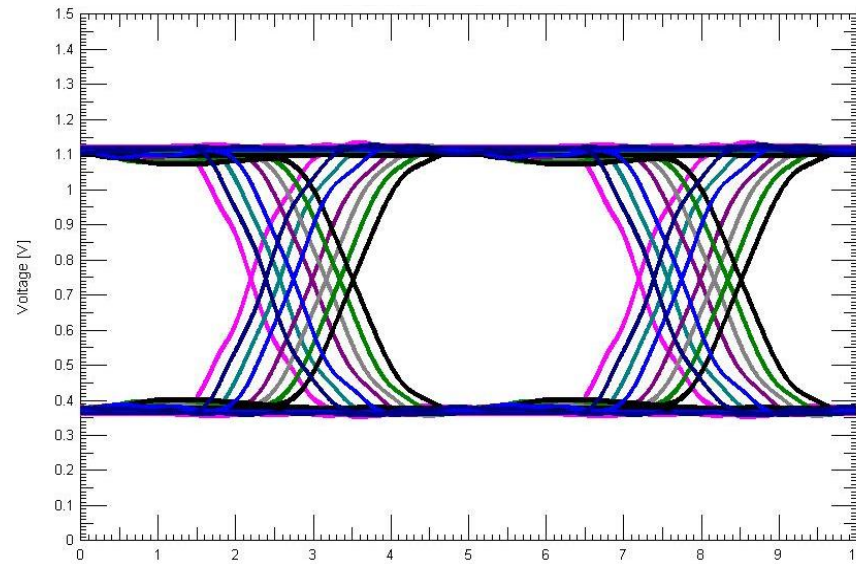
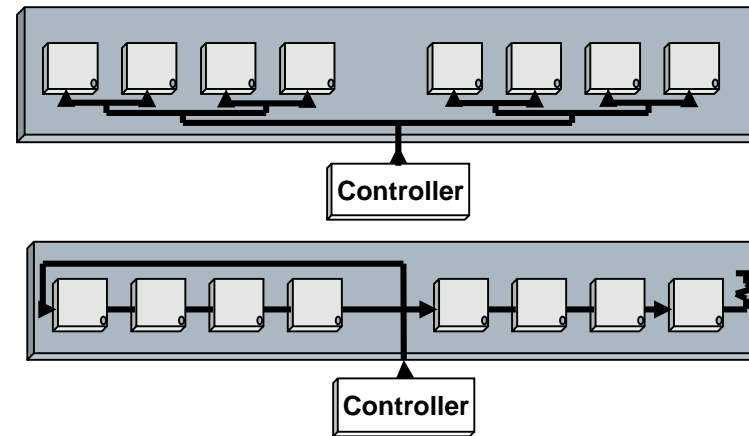


Figure 2. Alternating Data Byte Lanes on Different Critical Layers—Part 2

# MCK AND ADDRESS BUS

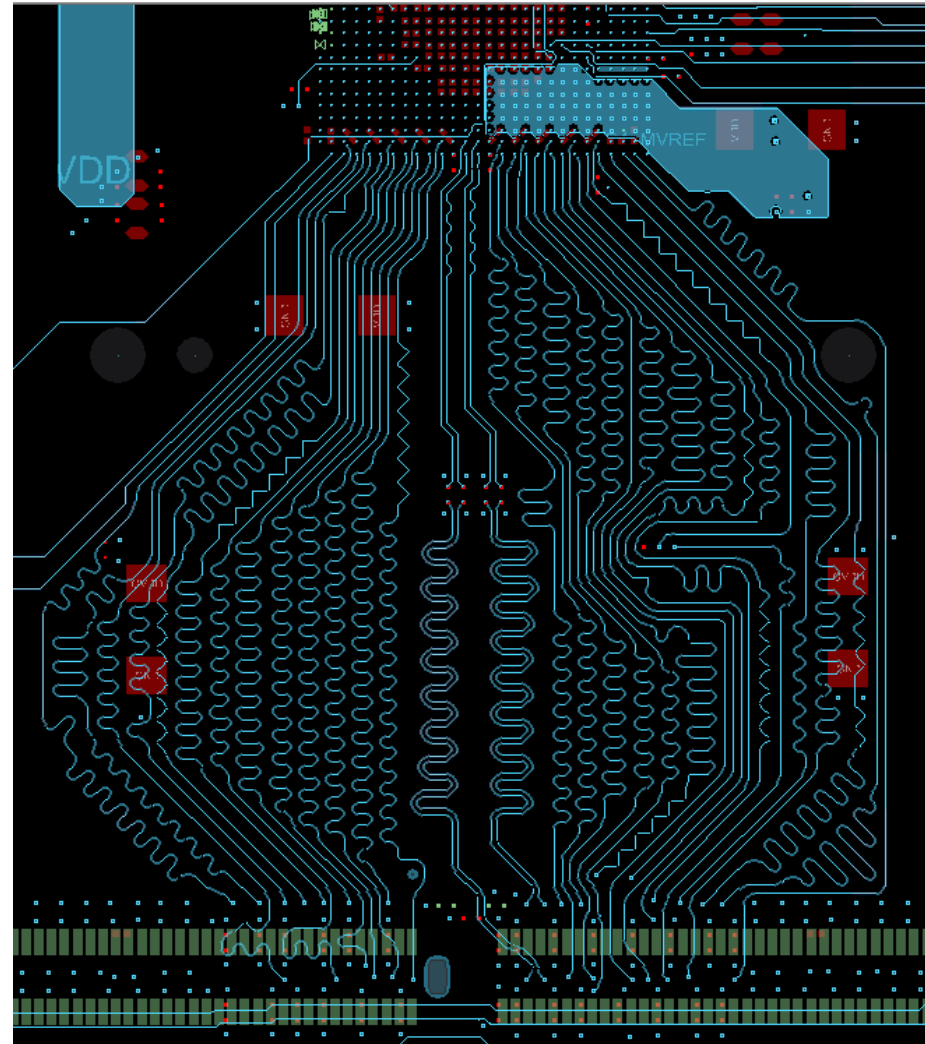
# MCK, ADDR Bus Topology

- Show ADDR, MCK
- Driver
- Receiver
- PCB
- Termination on Board ( $R_{tt}$ )
- Mention DDR2 vs. DDR3 style
  - DDR2 tee structure
  - DDR3 fly by routing



# MCK – ADDR Bus

- MCK differential vs. ADDR SE
- Key Specs

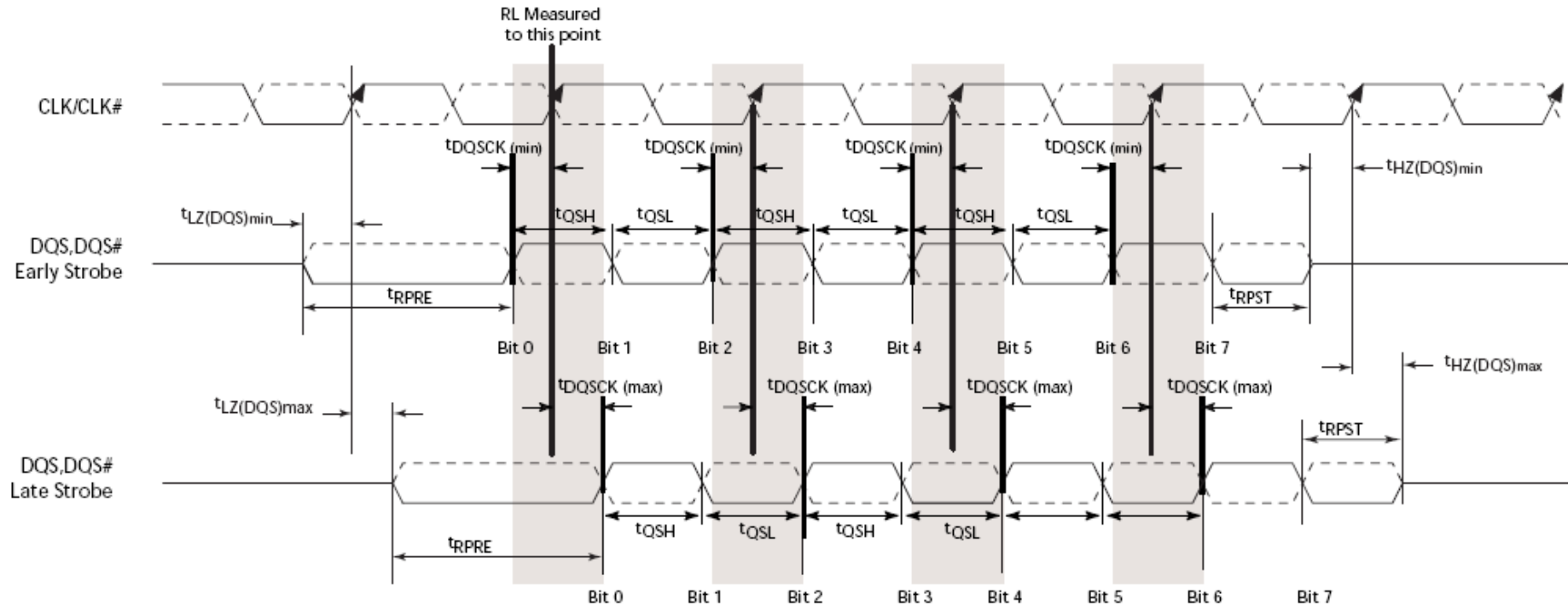


# Write Leveling – MCK to DQS

- Write Leveling
  - How to associate the serial routed MCK to the DQS?
  - Show MCK loads vs. DQS route

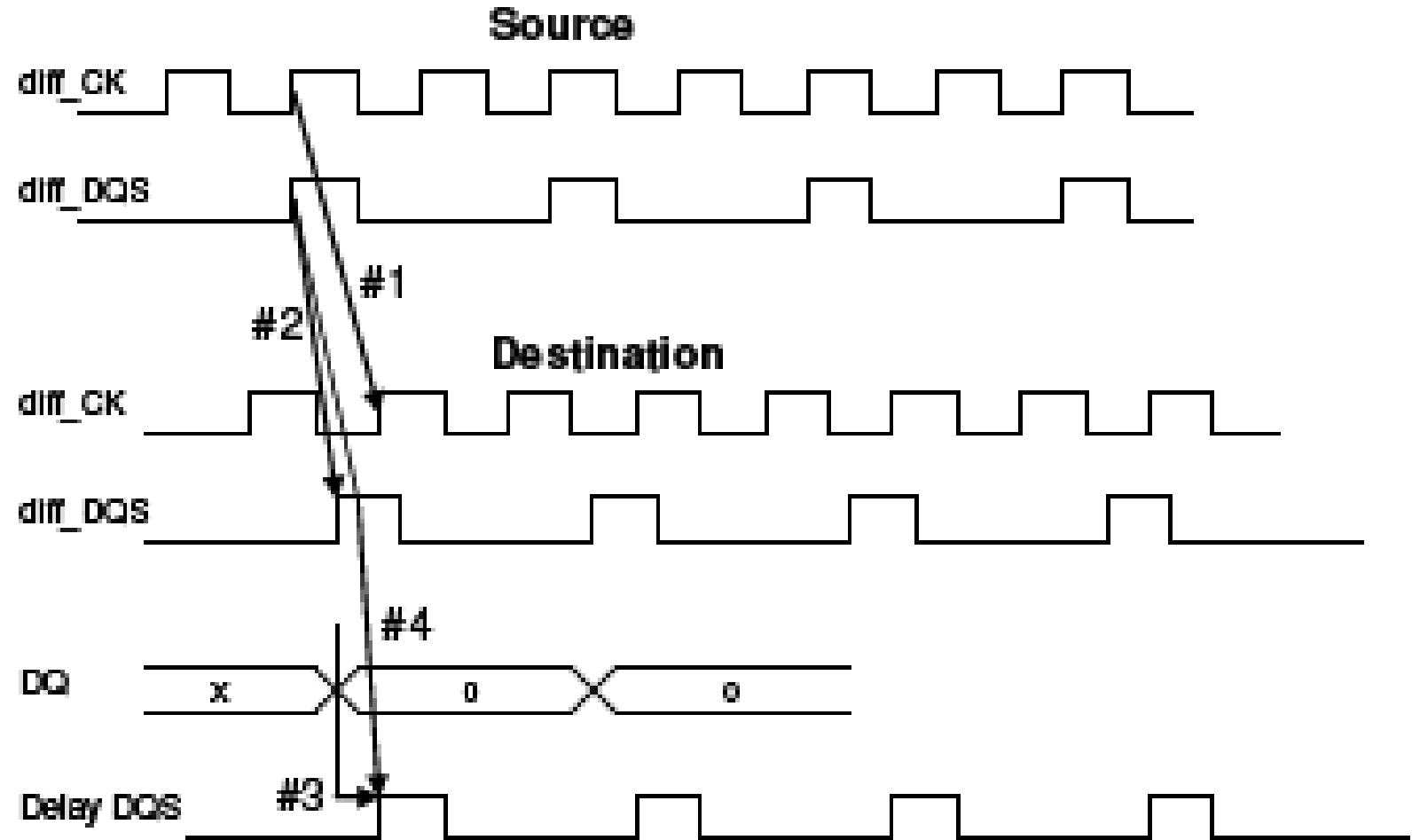
# The need for write-leveling....

- tDQSS requirement:
  - DQS/DQS# rising edge to CK/CK# rising edge
  - Clock to Strobe should be within a certain range for proper write operation to DDR SDRAMs
- tDQSS spec:  $\pm 0.25 \cdot t_{ck}$



# What is Write Leveling

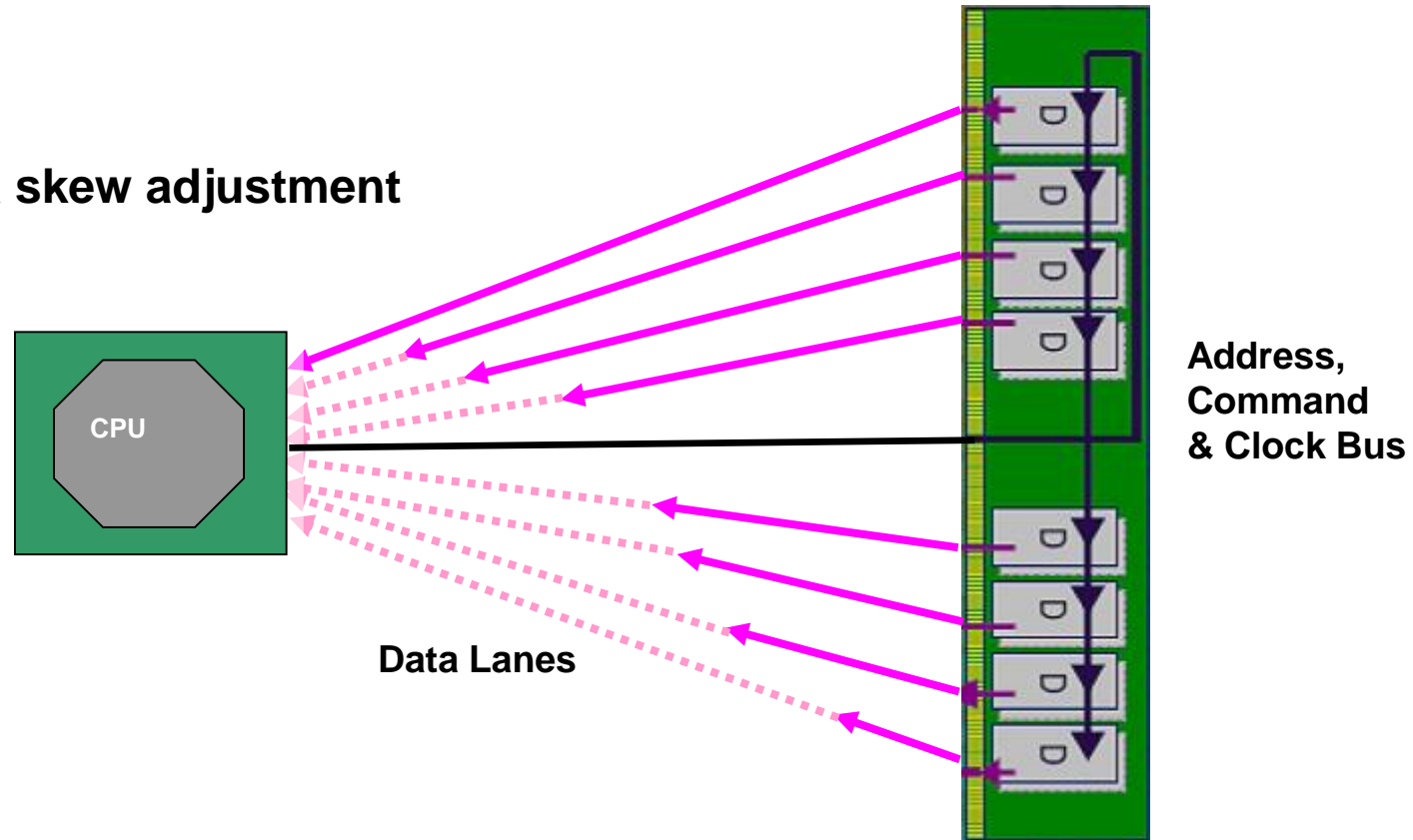
- During a write cycle, the skew between the clock and strobes is increased due to the fly-by topology. The write leveling will delay the strobe (and the corresponding data lanes) for each byte lane to reduce/compensate for this delay





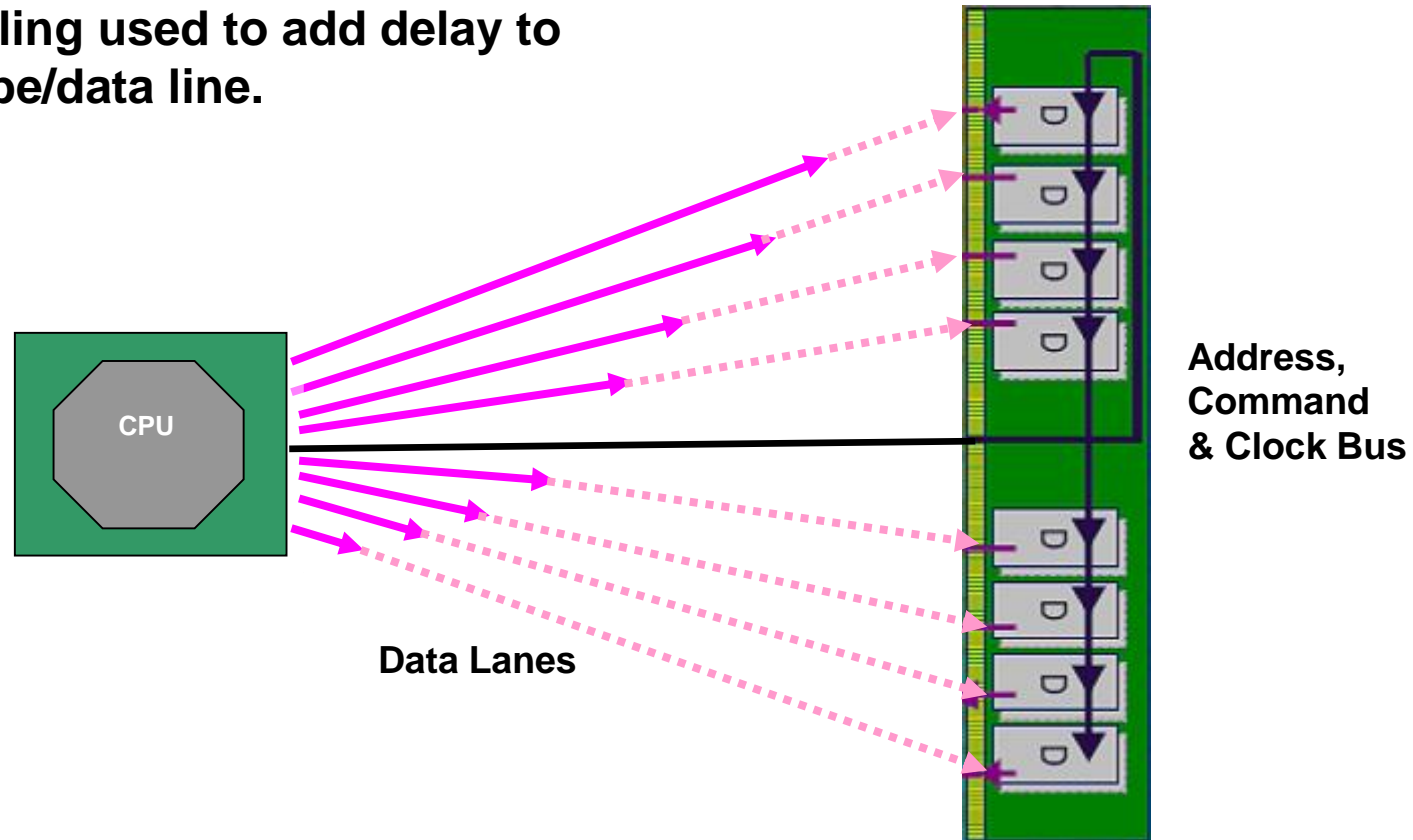
# Read Adjustment

Data strobe to data skew adjustment



# Write Adjustment

Write leveling used to add delay to each strobe/data line.



# DDR TOOLS – QCVS

# DDR Design Tools – QCVS

- Selects best ODT value
- Selects Driver Strength
- CLK\_ADJ

# Centering of the Clock Results

The screenshot shows the Component Inspector interface. On the left, a tree view shows the test hierarchy: Validation stage (40.39% complete), Centering the clock, Read ODT and driver, Write ODT and driver, and Operational DDR tests. The main area displays a table of results for the 'Centering the clock' test, categorized by 'WRLVL\_START' and 'CLK\_ADJ'.

	CLK_ADJ									
	0 clocks	1/8 clocks	1/4 clocks	3/8 clocks	1/2 clocks	5/8 clocks	3/4 clocks	7/8 clocks	1 clocks	
0 clock delay	0/3	3/3	2/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3
1/8 clock delay	0/3	3/3	3/3	3/3	0/3	0/3	0/3	0/3	0/3	0/3
1/4 clock delay	0/3	3/3	3/3	3/3	1/3	0/3	0/3	0/3	0/3	0/3
3/8 clock delay	0/3	3/3	3/3	2/3	2/3	2/3	0/3	0/3	0/3	0/3
1/2 clock delay	0/3	3/3	2/3	3/3	3/3	3/3	3/3	0/3	0/3	0/3
5/8 clock delay	0/3	3/3	2/3	3/3	3/3	3/3	3/3	3/3	0/3	0/3
3/4 clock delay	0/3	0/3	3/3	3/3	3/3	3/3	3/3	2/3	0/3	0/3
7/8 clock delay	0/3	0/3	0/3	2/3	3/3	3/3	3/3	3/3	0/3	0/3
1 clock delay	0/3	0/3	0/3	0/3	1/1					
9/8 clock delay										
5/4 clock delay										
11/8 clock delay										
3/2 clock delay										
13/8 clock delay										
7/4 clock delay										
15/8 clock delay										
2 clock delay										
17/8 clock delay										
9/4 clock delay										
19/8 clock delay										
5/2 clock delay										

Click “cell” to choose Write level start and CLK\_ADJ values.

# DDR read ODT and Driver Strength – Test Results

The screenshot shows the Component Inspector window with the Validation tab selected. The 'Test' pane on the left lists several tests, with 'Read ODT and driver' checked and showing a 100% result. The 'Results' pane on the right displays a table of DRAM driver strength test results for various controller ODT values.

		DRAM driver strength	
		40 ohm - half	34 ohm - full
controller ODT	43 ohm	3/3	3/3
	50 ohm	3/3	2/3
	55 ohm	3/3	3/3
	60 ohm	3/3	3/3
	75 ohm	3/3	3/3
	120 ohm	3/3	3/3
	150 ohm	3/3	3/3

Click “cell” to choose optimized ODT value.

# DDR Write ODT and Drive Strength – Test Results

The screenshot displays the Component Inspector software interface. On the left, the 'Test' list shows the following items:

- Validation stage
  - Centering the clock (100%)
  - Read ODT and driver
  - Write ODT and driver
- Operational DDR tests

On the right, the 'Results' table shows the following data:

		DRAM ODT				
		20 ohm	30 ohm	40 ohm	60 ohm	120 ohm
Controller DRV Strength	Half Strength	3/3	2/3	3/3	3/3	3/3
	Full Strength	3/3	3/3	3/3	3/3	3/3

Click “cell” to choose optimized ODT value.

# Centering of the Clock – After ODT Optimization

Results		Choose tests								
		CLK_ADJ								
		0 clocks	1/8 clocks	1/4 clocks	3/8 clocks	1/2 clocks	5/8 clocks	3/4 clocks	7/8 clocks	1 clocks
WRLVL_START	0 clock delay	0/3	3/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3
	1/8 clock delay	0/3	3/3	3/3	3/3	0/3	0/3	0/3	0/3	0/3
	1/4 clock delay	0/3	3/3	3/3	3/3	0/3	0/3	0/3	0/3	0/3
	3/8 clock delay	0/3	3/3	3/3	3/3	3/3	3/3	0/3	0/3	0/3
	1/2 clock delay	0/3	3/3	3/3	3/3	3/3	3/3	0/3	0/3	0/3
	5/8 clock delay	0/3	3/3	3/3	3/3	3/3	3/3	3/3	3/3	0/3
	3/4 clock delay	0/3	0/3	3/3	3/3	3/3	3/3	3/3	3/3	0/3
	7/8 clock delay	0/3	0/3	0/3	3/3	3/3	3/3	2/3	3/3	0/3
	1 clock delay	0/3	0/3	0/3	0/3	3/3	3/3	3/3	3/3	0/3
	9/8 clock delay	0/3	0/3	0/3	0/3	0/3	3/3	3/3	3/3	0/3
	5/4 clock delay	0/3	0/3	0/3	0/3	0/3	0/3	2/3	3/3	0/3
	11/8 clock delay	0/3	0/3	0/3	0/3	0/3	0/3	0/3	3/3	0/3
	3/2 clock delay	0/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3
	13/8 clock delay	0/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3
	7/4 clock delay	0/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3
	15/8 clock delay	0/3	3/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3
	2 clock delay	0/3	3/3	0/3	0/3	0/3	0/3	0/3	0/3	0/3
	17/8 clock delay	0/3	3/3	3/3	3/3	0/3	0/3	0/3	0/3	0/3
	9/4 clock delay	0/3	3/3	3/3	3/3	0/3	0/3	0/3	0/3	0/3
	19/8 clock delay	0/3	3/3	3/3	3/3	3/3	3/3	0/3	0/3	0/3
5/2 clock delay	0/3	3/3	3/3	3/3	3/3	3/3	0/3	0/3	0/3	

Centering of clock scenario was re-run after finding the right ODT values



# IO BUFFER MODELS FOR DDR

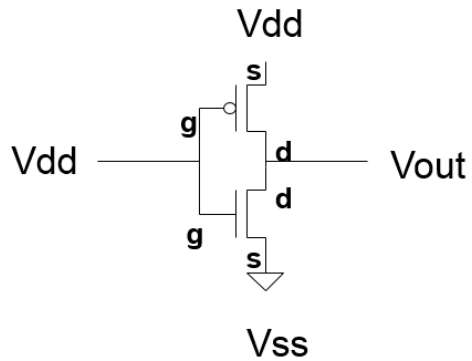
# DDR Bus IO Buffer Models

- Often simulated using IBIS
  - IBIS (IO Buffer Interface Standard)
    - Standard since 1993
    - Simplified IO buffer model
    - Data format to describe IO buffer
    - Runs much faster than SPICE models, typically
  - SPICE buffer models for large, parallel bus like DDR may take a while to simulate

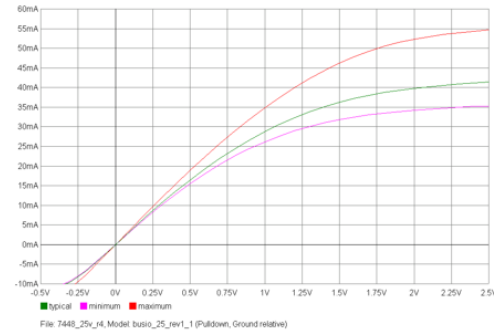
# IBIS Data: DC Data

- Example Voltage vs. Current data from IBIS models
- Note Pullup, Pulldown, Clamp data
- Note ODT vs. Driver data

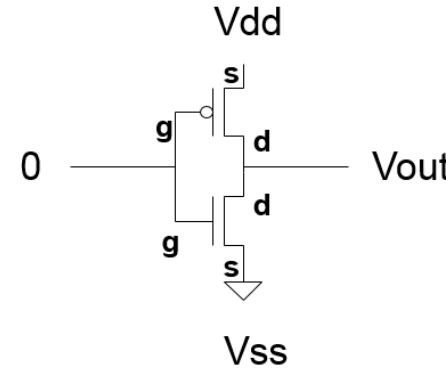
### DC IV Data: Pulldown



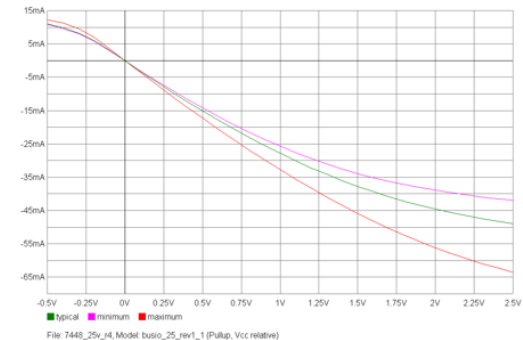
Pulldown Extraction:  
Excite Pulldown (e.g. NMOS)  
Sweep I vs.  $-V_{dd}$  to  $2V_{dd}$



### DC IV Data: Pullup



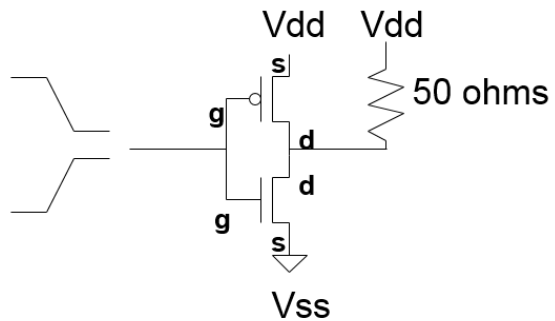
Pullup Extraction:  
Excite Pullup (e.g. PMOS)  
Sweep I vs.  $-V_{dd}$  to  $2V_{dd}$



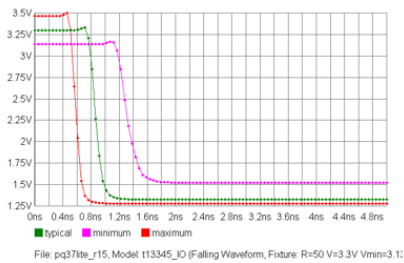
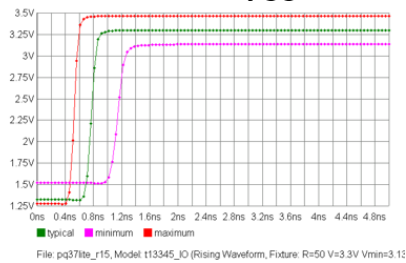
# IBIS Data: Transient Data

- Example Voltage vs. Time Data
- Note four sets of curves

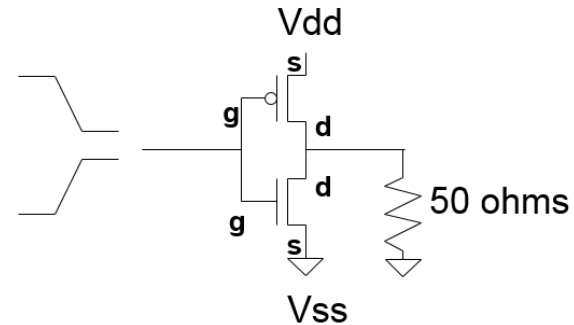
**Transient Data: 50 ohm resistor tied to VDD**



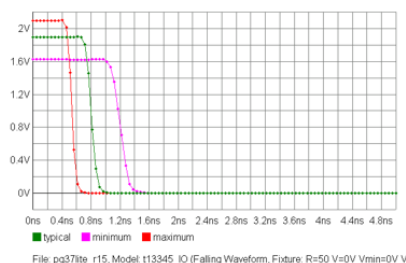
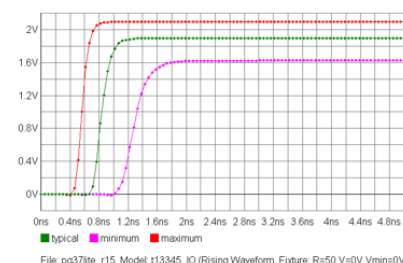
Rising and Falling Voltage vs. Time table with 50 ohm resistive load tied high



**Transient Data: 50 ohm resistor tied to Ground**

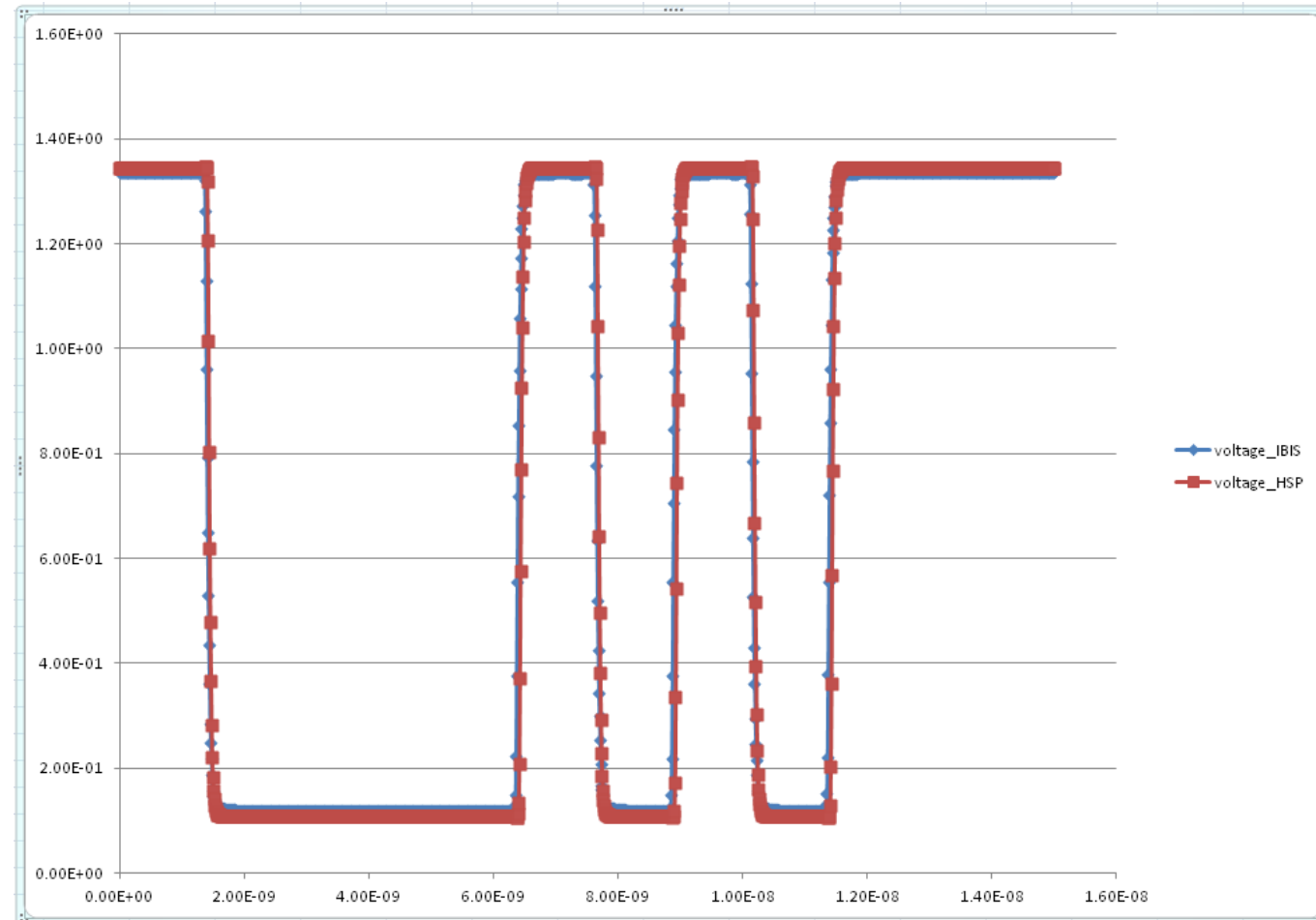


Rising and Falling Voltage vs. Time table with 50 ohm resistive load tied low



# HSPICE DDR3/3L DDR3L/4 IO

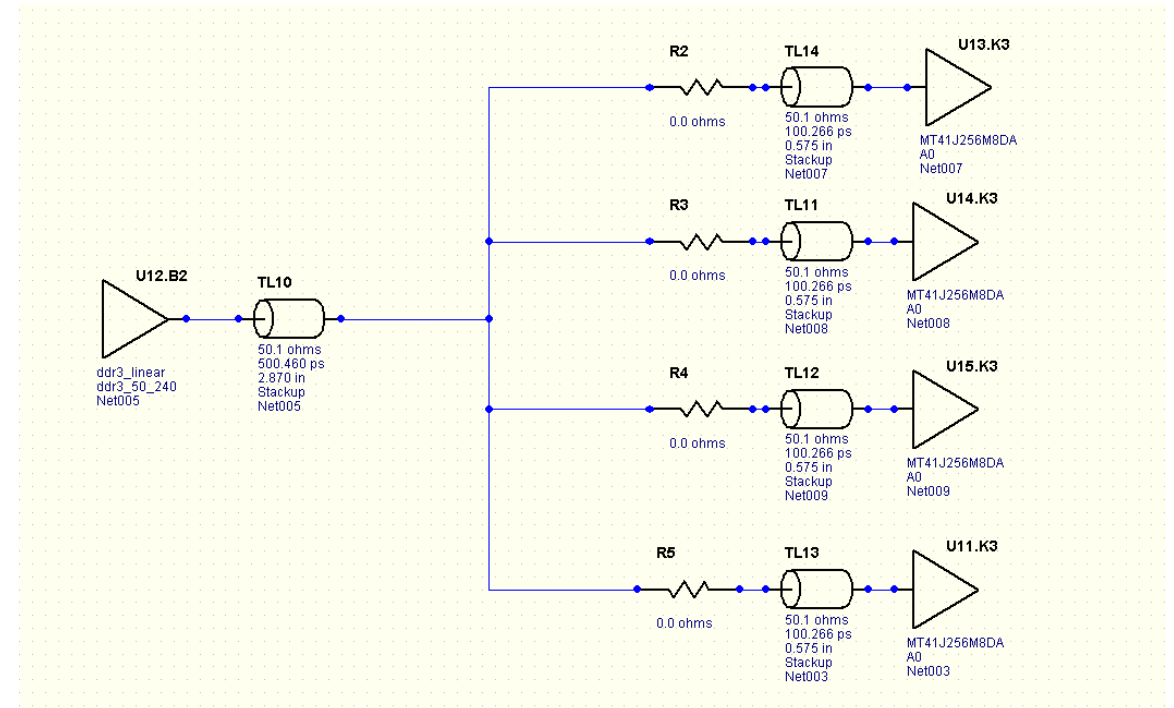
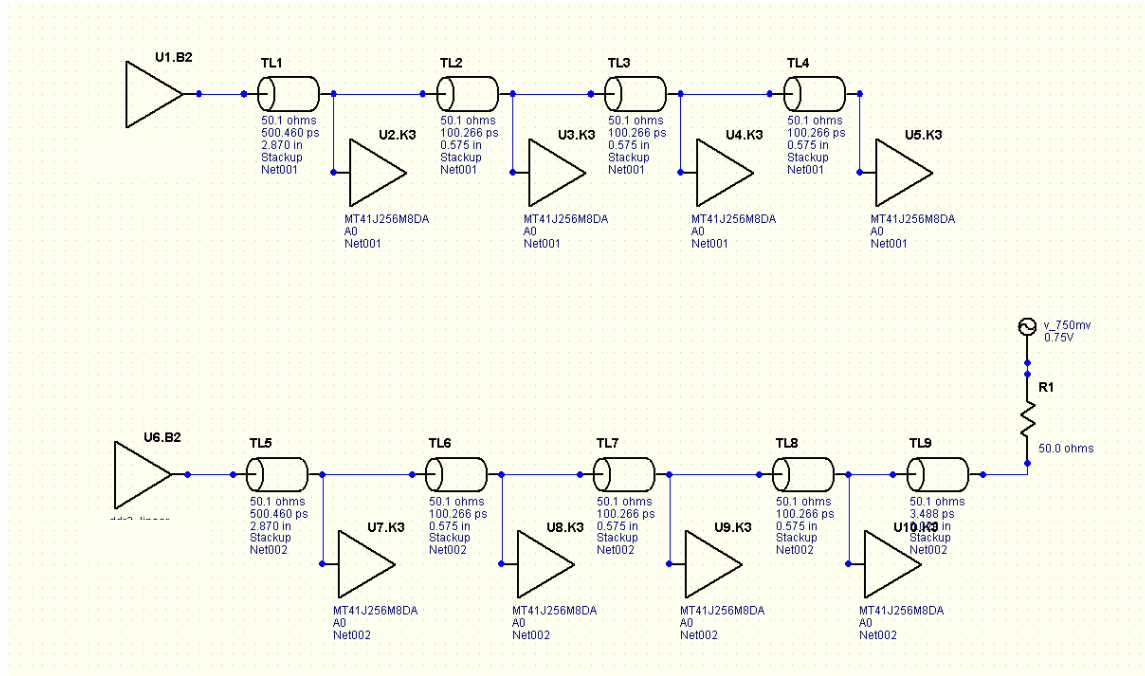
- Recent Digital Networking Devices have added HSPICE IO buffer model support
- Encrypted HSPICE
- Matches IBIS results



# BASIC SIMULATION EXAMPLES

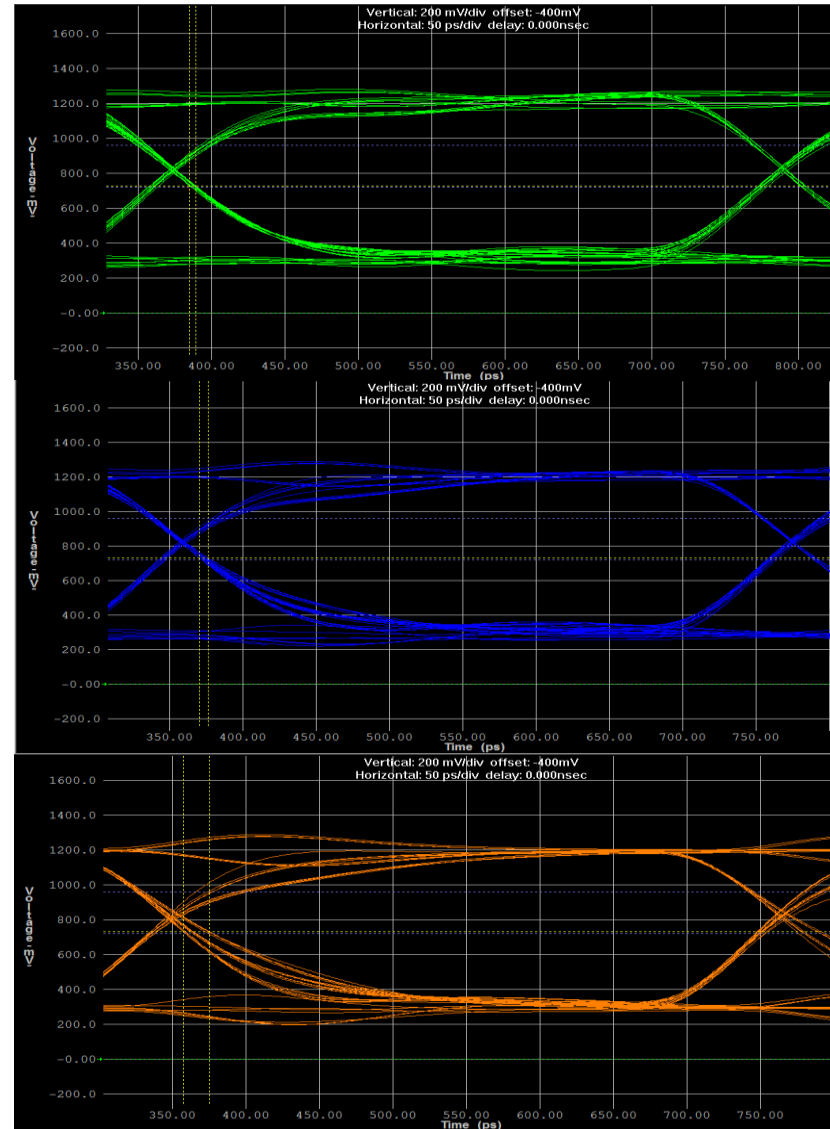
# Tee vs. Daisy Chain

- Basic options for connecting multiple loads
- Tee to multiple, parallel route
- Daisy chain, serial route
- SSTL (Stub Series Terminated Logic)



# Example of DQ optimization

- Sweep TX
- Sweep Zo
  - 40, 50, 60 ohm shown at right
- Sweep RX ODT





# Example of DQS vs. DQ

- Note DQS vs. DQ for Writes vs. Reads
- DQS centered DQ in Specs for Writes
- DQS aligned with DQ in Specs for Reads

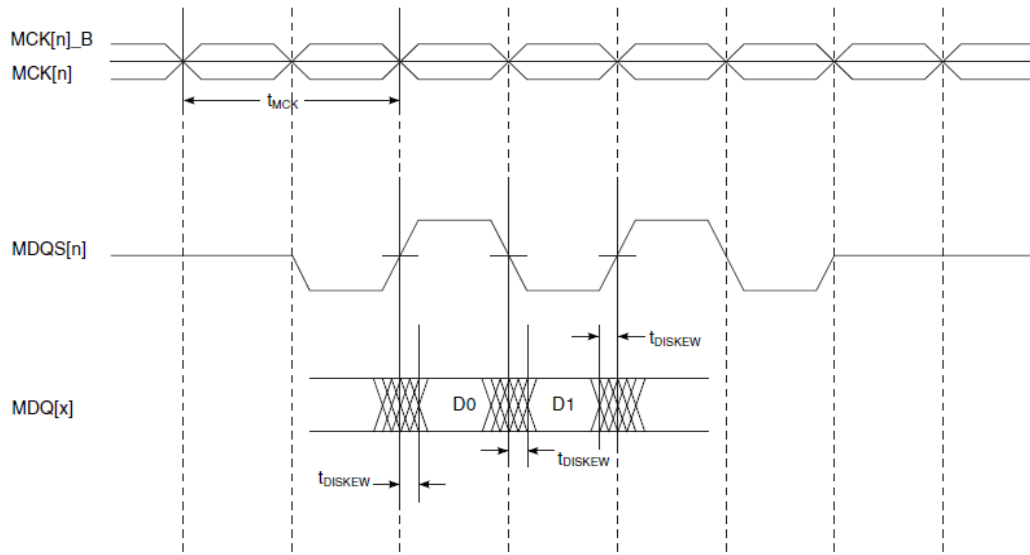


Figure 9. DDR3 and DDR3L SDRAM Interface Input Timing Diagram

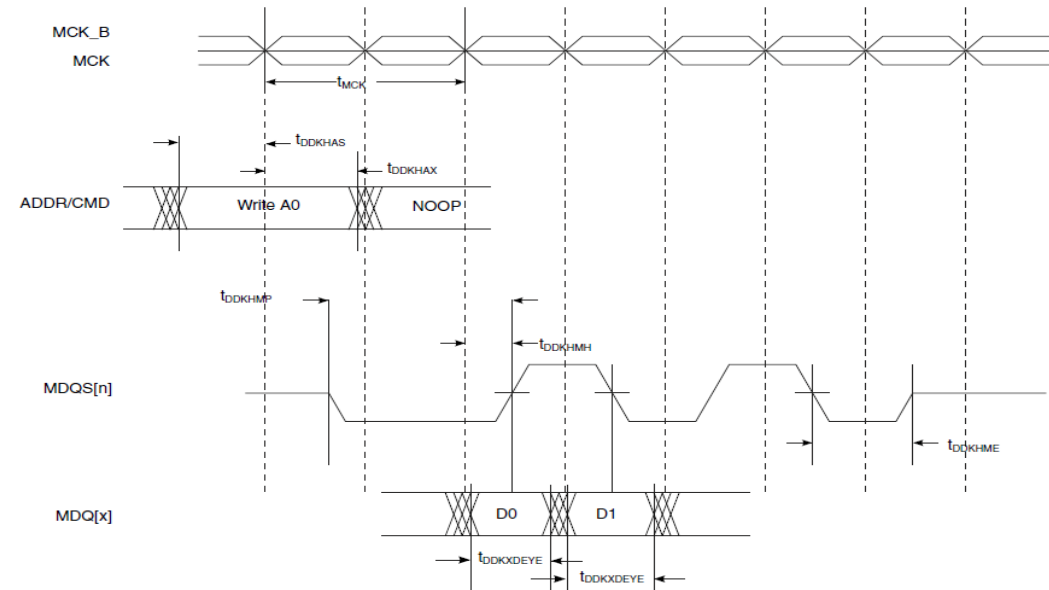
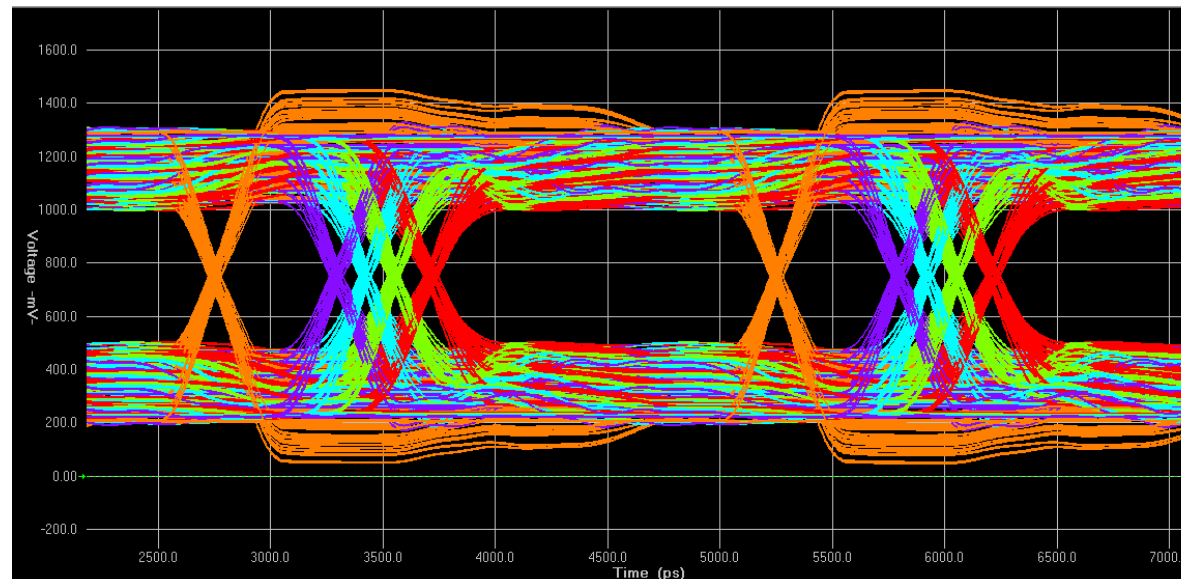
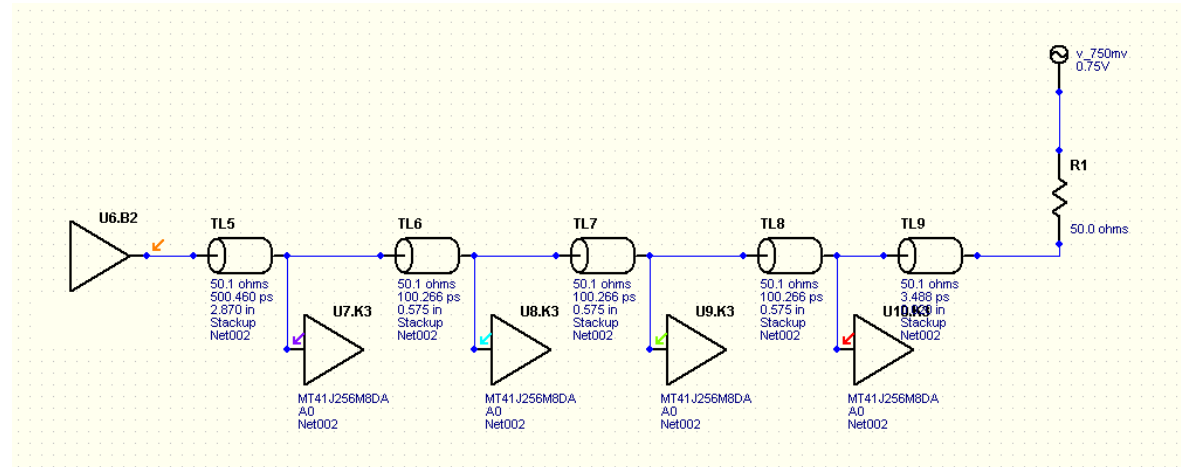


Figure 11. DDR3 and DDR3L output timing diagram

# Example of MCK/ADDR Optimization

- Sweep TX
- Sweep Zo
- Sweep Rtt



# Example of MCK/ADDR Timing

- How to place MCK in ADDR eye
- 1T vs. 2T timing
- CLK\_ADJ

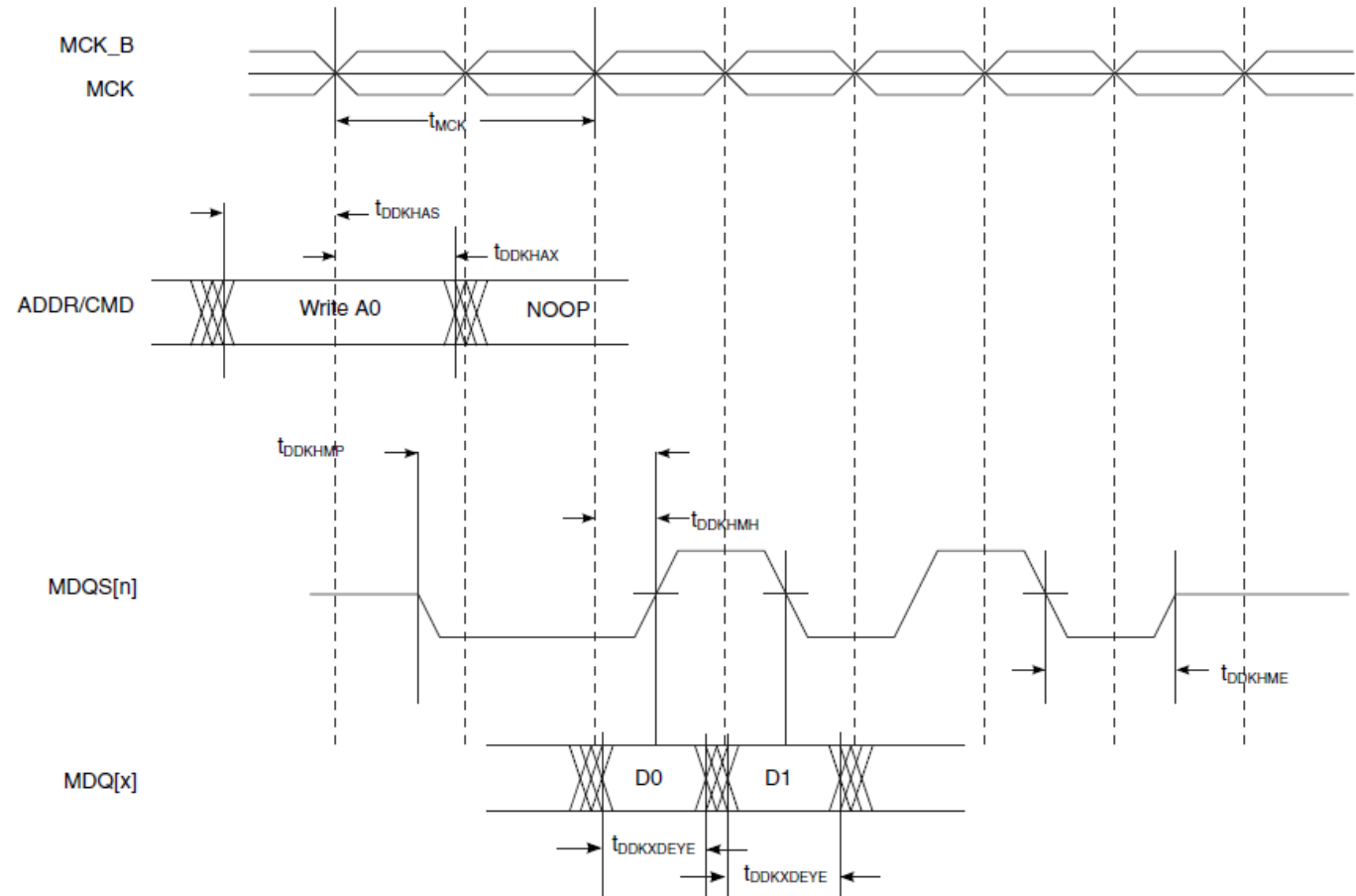
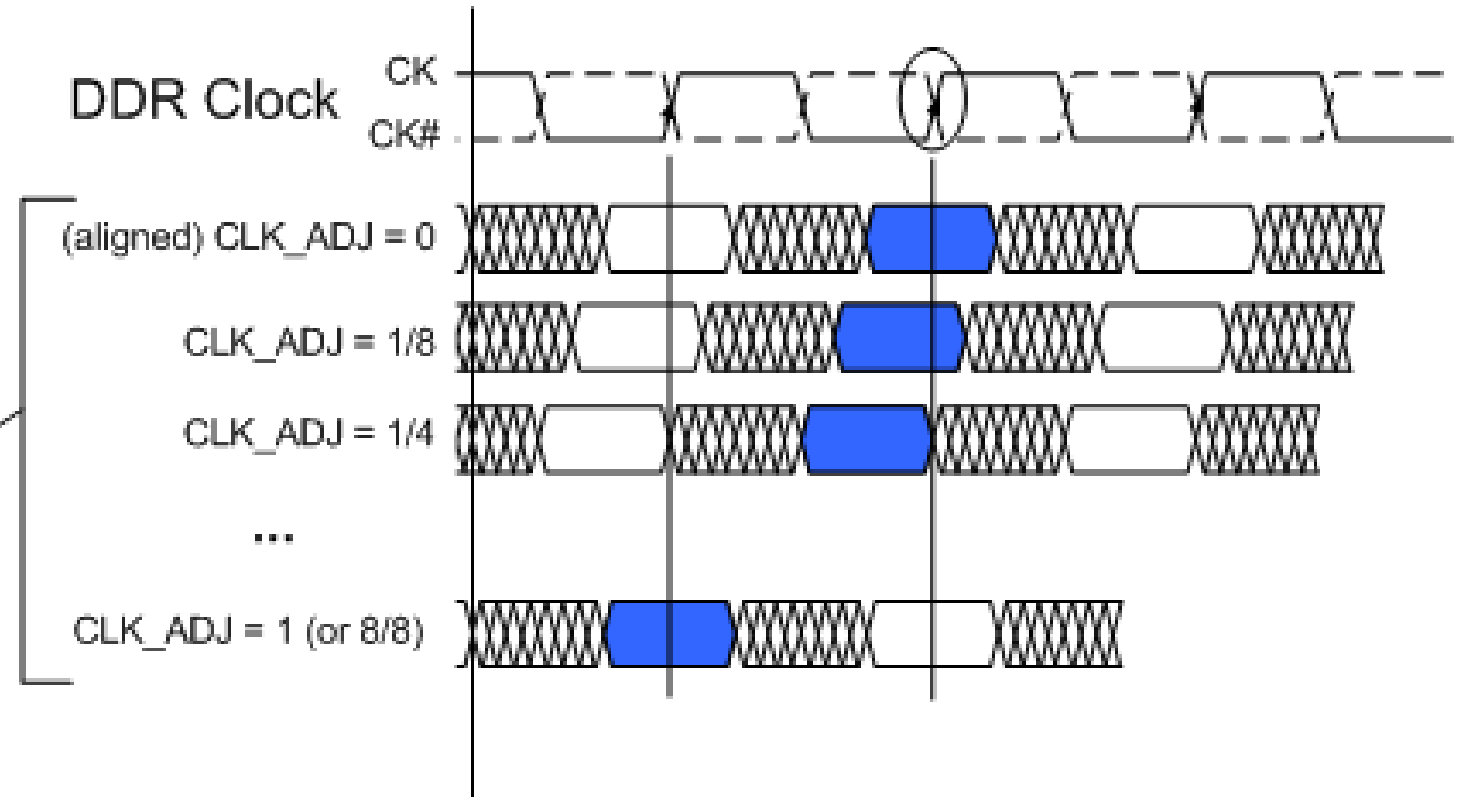


Figure 11. DDR3 and DDR3L output timing diagram

# CLK\_ADJ – Clock Adjust

- CLK\_ADJ defines the timing of the address and command signals relative to the DDR clock.

**Address and Command signal position relative to the clock by varying CLK\_ADJ**



# Data Eye, Bit Time and Unit Interval

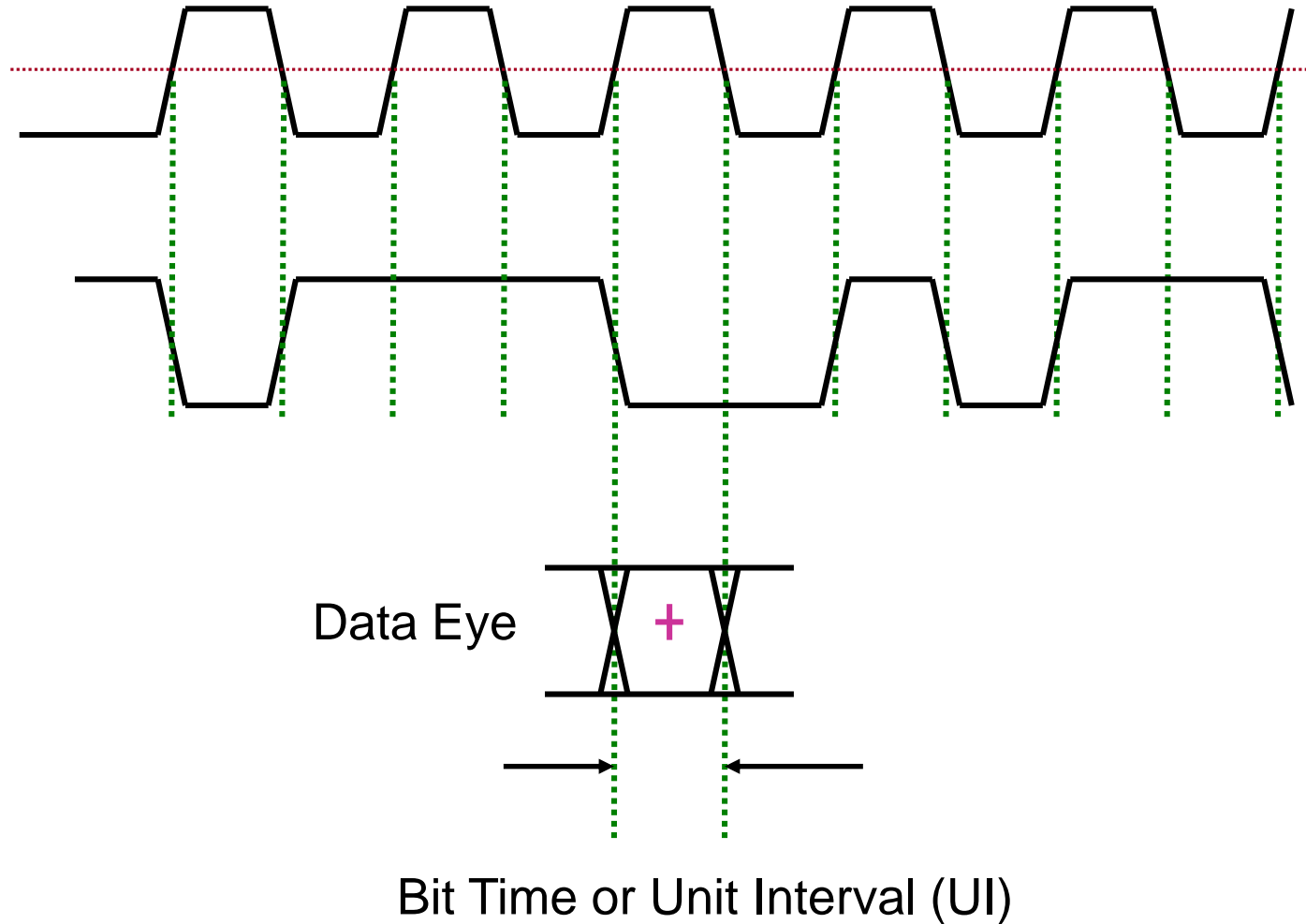
## Note: GHz vs. Gbps

Clock: 1.0 GHz

- Rising Edge to Rising Edge:  
1000 ps
- Bit Time: 500 ps
- Data Rate:  $1/\text{Bit Time}$  or  $1/\text{UI} = 1/500\text{ps}$  or 2 Gbps

So Data Rate is 2x “Clock”

But Nyquist frequency is “Clock”  
Rate or 2 GHz



# Die vs. Pin Probing

- Important for Read Timing Simulations if CPU has larger package size

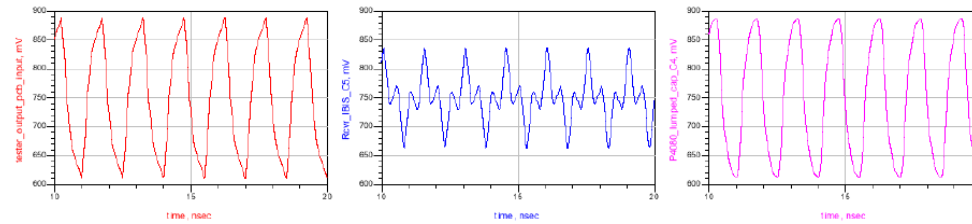


Figure 4. QorIQ memory controller receiver simulation results

From left to right:

- Sent strobe (DQS) signal by DRAM during a read cycle
- Same DQS signal observed at the QorIQ memory controller pin
- Same DQS signal observed at the QorIQ memory controller die

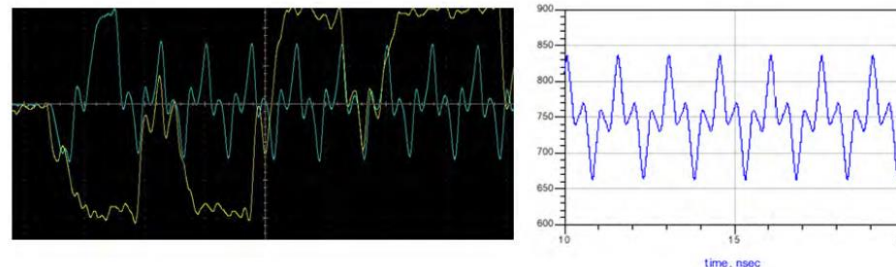


Figure 5. Measurement vs. simulation

From left to right:

- Measured DQS (blue signal in scope shot) at QorIQ memory controller pin during a read cycle with ODT off
- simulated DQS at QorIQ memory controller pin during a read cycle with ODT off

# PCB DESIGN CONSIDERATIONS FOR DDR

# PCB Related Items in Routing Guidelines

- Routing Order
- Byte Routing on different layers
- Trace Length Matching
- PCB  $Z_0$
- Trace Separation
- MCK to DQS limits
- Route vs. GVdd or Ground
- Split Planes



# DN HW Spec Specific Items

- No Slew Rate Derating
- Measure at Vref
- Slew Rate to Vref Translation
- Measure at Die, not Pin
- QCVS DDR tool for margins, optimization

## 6.1 Important read timing budget simulation considerations

Consider the following:

- Do not perform slew-rate derating for the FSL DDR3 controllers on reads (that is, DDR3 inputs (DQS/DQ) to the FSL DDR3 controllers do not need to be derated per JESD79-3E)
- Timing budgets for reads can be done with customer's simulation tool by adding the setup and hold margins rather than looking at the setup or hold margins by themselves (to account for the DQS-DQ calibration).
- Read timing should be taken at Vref rather than Vin levels (that is, read timing measurements for DQ shall be taken at Vref. No read timing measurements are taken at Vih(ac), Vil(ac), Vih(dc), or Vil(dc)).

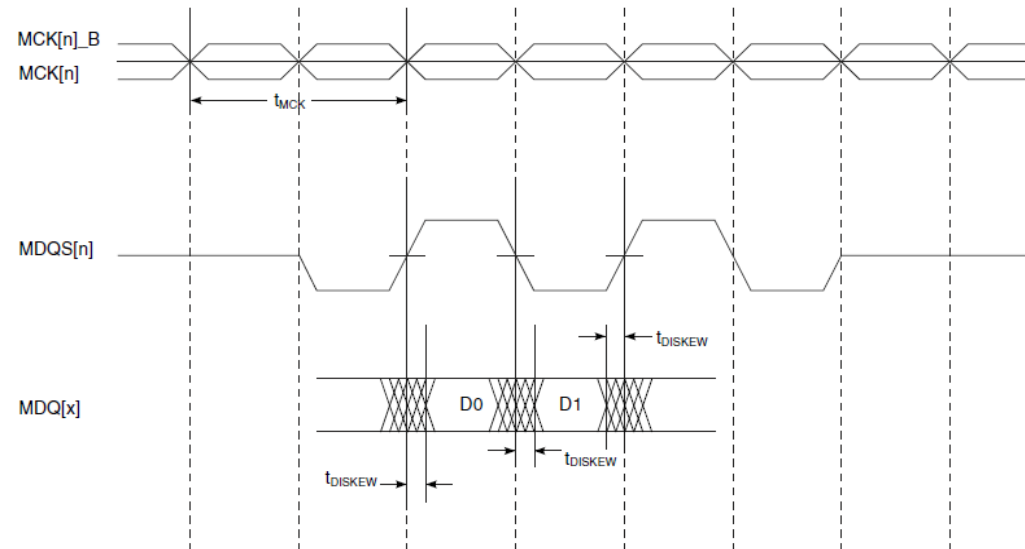


Figure 9. DDR3 and DDR3L SDRAM Interface Input Timing Diagram

# QUESTIONS?

Thanks For Your Time And Attention!



SECURE CONNECTIONS  
FOR A SMARTER WORLD

# ATTRIBUTION STATEMENT

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