MAC57D5xx ARM® Core MCUs
for Automotive Instrument Clusters

APF-ACC-T1093

Tian Maoxin | Auto FAE

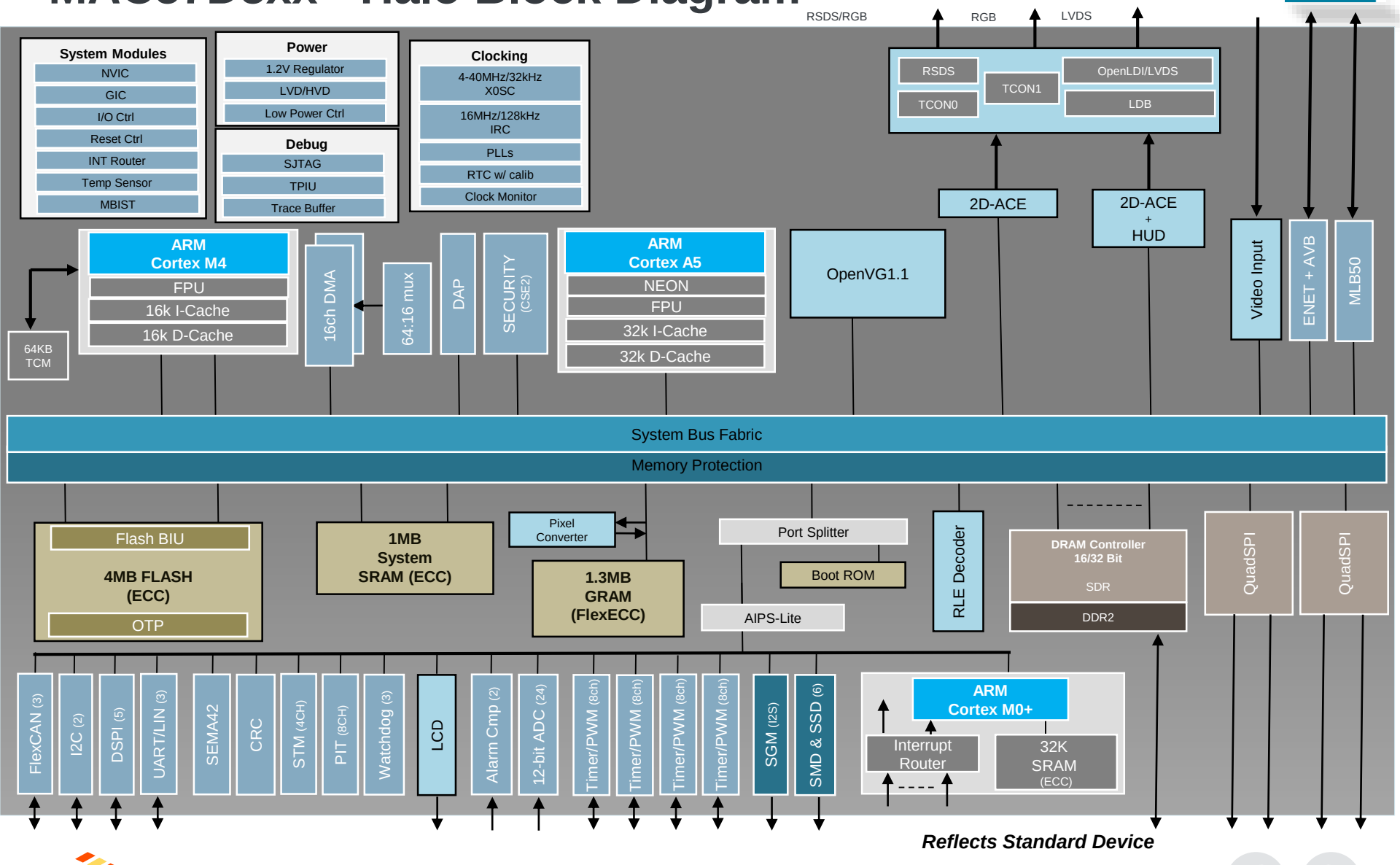
J U L Y . 2 0 1 5

External Use

MAC57D5/4xx Family Key Differentiators

- **Heterogeneous Multi-core architecture for Application and Real-Time Processing**
  - Integrates CortexM4 for real time applications and the CortexA5 for applications and HMI
  - Support for dual OS (Linux, Integrity, etc. on CortexA5 and MQX, AutoSAR RTOS on CortexM4)
  - Integrates Cortex M0+ for I/O control and intelligent stepper motor drivers
- **Intelligent Stepper Motor Drivers**
  - Built in Cortex M0+ to control I/O, offload stepper motor algorithms, peripheral Control & low power performance
  - Stepper Stall Detect
- **Integrated Power Management**
  - Core supply generated on-chip eliminating the need for complicated external PMIC
  - Simple LDO to drive IO supply
- **Flexibility with Internal Memory**
  - 2.3MB of internal SRAM (ECC support for 1MB -1.65MB) for Halo
  - QuadSPI and DDR/SDRAM for expansion of Flash and RAM for future-proofing
- **Quad SPI Flash Interface**
  - Support for Dual DDR QuadSPI for Halo
  - Up to 160MB/s or 200MB/s peak bandwidth (limited by external Memory bandwidth)
- **2x 2D-ACE**
  - 2D-Animation and Composition Engine: Significantly reduces RAM requirements
  - In-line Head-Up Display Warping on one 2D-ACE
  - Digital RGB, RSDS(TCON) and OpenLDI (LVDS) output options
- **Graphics Processing Unit**
  - Vivante GC355: High performance Open VG with low footprint drivers
- **Unique Security Capabilities**
  - Uses CSE2 for the latest security enhancements
    - supports SHE specification and GM's Global B Cyber security requirements

MAC57D5xx - Halo Block Diagram



Reflects Standard Device

Class Leading Performance

Clusters highest performance ARM-based triple-core single-chip solution

- **>70% more performance***
- **50% more** frequency performance*

- Proprietary graphics display hardware **significantly reduces** CPU overhead and requirement for additional RAM by as much 80%**
- High speed QuadSPI Serial flash controller
  - **Realtime fetch** of graphic content **reducing** the need for additional RAM
  - **>5x faster read** throughput with the support of HyperBusTM interface***

Triple-Core architecture enables a flexible OS strategy

- Industry standard AUTOSAR OS supporting real-time vehicle processing tasks
- Customer-specified OS supporting applications & HMI
- Application-specific code on I/O Processor offloading the other core
  - Intelligent Stepper Motor control
  - Low-power mode I/O peripheral control

• Comparison done against instrument cluster competitors comparing operating Frequency & DMIPs
** Comparison with a traditional double frame buffer scheme of a typical customer animation
*** Data taken from Spansion site at http://www.spansion.com/Products/memory/HyperFlash-Memory/Pages/HyperFlash-Memory.aspx

Addressing Functional Safety and Security

SAFE ASSURE™ by Freescale

- **ASIL-B compliant MCUs – meets ISO26262 requirements**
- **Safe Assure functional safety program:**
  - **Safety Process** - integrating functional safety into dev process
  - **Safety Hardware** – built in self tests, error code correction, etc
  - **Safety Software** – AUTOSAR MCAL, OS, core self tests, etc
  - **Safety Support** – training, documentation and tech support

- **Designed to support next generation security needs** using Secure Boot, Secure Mileage & Component Protection
- **Hardware Security Module (HSM)**
  - Meets **SHE** Spec requirements
  - **Dedicated** security core
  - **Secure Flash and SRAM**
  - **Cryptographic module** – AES-128 & random number generator that helps protects security keys, secure boot up, tamper detection, advanced debug support, etc.

Superior Equipped and Quality Graphics

At a fraction of the memory & CPU overhead

ARM Cortex-A5
Application Processor

Architected for high performance
- Up to 320 MHz
- 1.57 DMIPs/Mhz

Vivante 2D GPU
OpenVG1.1

Exceptional performing 2D GPU
- Needle animation, fonts & textures
- Low memory footprint drivers

2D - Animation & Composition Engine

Significantly reduces RAM & CPU overhead requirements
- Some cases as much as 90% reduction in memory usage
- CPU overhead reduction with H/W accelerators
- Display content integrity verification

On the fly HUD Warping Engine

Industry's 1st On the fly warping helps optimize solutions
- Reduce memory usage
- Releases GPU bandwidth
- Reduce hardware implementation costs

MAC57D5xx - Product Family Scalability

Target Applications

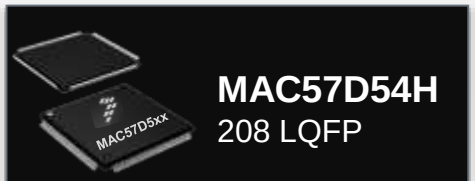
- Instrument clusters
- Heads-up displays
- Multifunction displays

Standard	Advanced	Premium
		
Cluster with high res. TFT	Cluster with dual high res. TFTs	Cluster with high res. TFT & HUD

WVGA with only internal memory
dRGB & RSDS display interface
QFP Pin compatible family

MAC57D54H
176 LQFP

Advanced Communications: Ethernet-AVB / MLB
SDR DRAM expansion on 2-layer PCB
Dual display drive and Video input



MAC57D54H
208 LQFP

DDR2 DRAM expansion
On-the-fly hardware HUD warping engine
OpenLDI LVDS display interface

MAC57D54H
516 MAPBGA

Summary MAC57D5xx Family Matrix

Family Product	FLASH	SRAM	Package Options	SDR	DDR2	Quad SPI	GPU	Target RunIDD
MAC57D54H (Halo_High)	4MB	1.3 MB (non ECC)/ 2x 512 kB (w/ ECC)	176 LQFP	None	None	1x Dual SDR/DDR QuadSPI, 100MHz(200MB/s)	GC355 (Open VG1.1 & Tiny UI)	500mA
			208 LQFP	16 Bit, 160MHz	None	2x Dual SDR/DDR QuadSPI, 100MHz(200MB/s)		600mA
			516 MAPBGA	16 Bit, 160MHz	16 or 32 Bit, 320MHz			750mA
MAC57D53M (Halo_Mid)	3MB	1.3 MB (non ECC)/ 2x 512 kB (w/ ECC)	176 LQFP	None	None	1x Dual SDR/DDR QuadSPI, 100MHz(200MB/s)	GC355 (Open VG1.1 & Tiny UI)	500mA
			208 LQFP	16 Bit, 160MHz	None	2x Dual SDR/DDR QuadSPI, 100MHz(200MB/s)		600mA
			516 MAPBGA	16 Bit, 160MHz	16 or 32 Bit, 320MHz			750mA
MAC57D52L (Halo_Low)	2MB	1.3 MB (non ECC)/ 2x 512 kB (w/ ECC)	176 LQFP	None	None	1x Dual SDR/DDR QuadSPI, 100MHz(200MB/s)	GC355 (Open VG1.1 & Tiny UI)	500mA
			208 LQFP	16 Bit, 160MHz	None	2x Dual SDR/DDR QuadSPI, 100MHz(200MB/s)		600mA

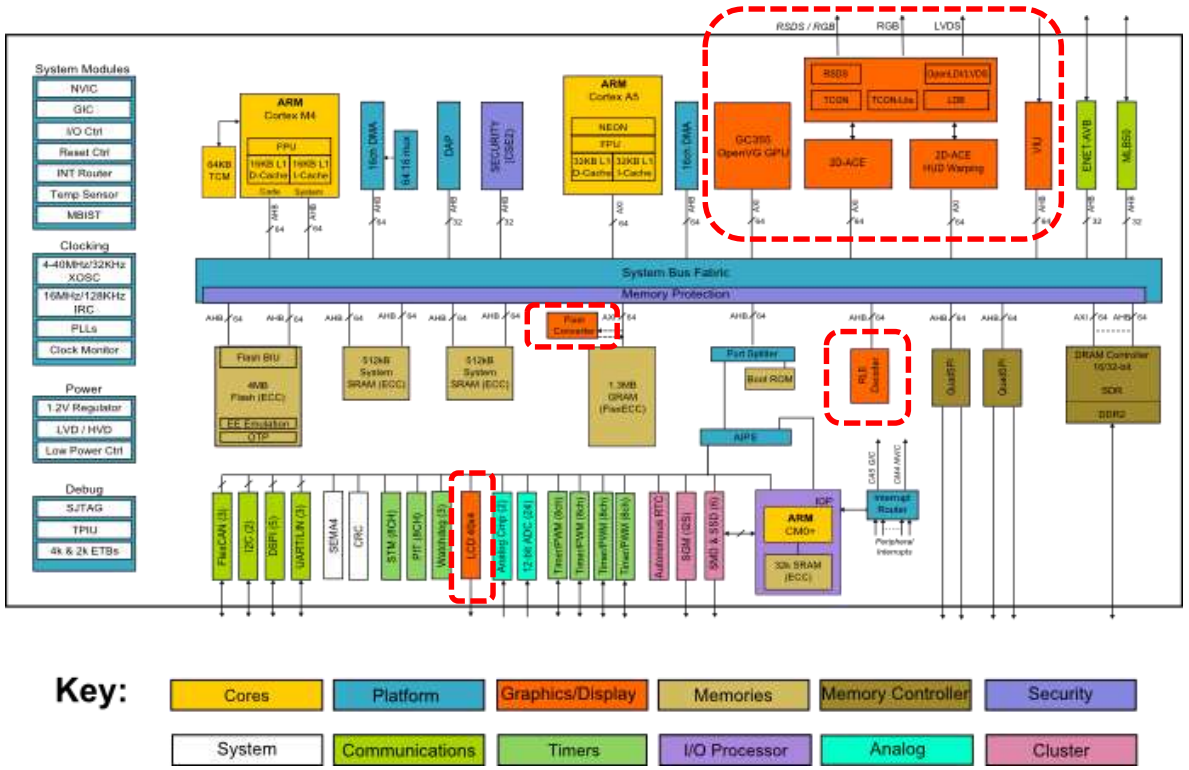
**Not all feature differences shown in table above, refer to Product Brief for specific feature details

Detailed MAC57D5xx Family Matrix

	Technical Details	MAC57D54H Halo High	MAC57D53M Halo Mid	MAC57D52L Halo Low
Cores	Cortex-A5 (320Mhz, 32K/32K L1 Cache, FPU, MNU, NEON)	Yes	Yes	Yes
	Cortex-M4 (160Mhz, FPU, 16/16K L1 Cache)	Yes	Yes	Yes
	Cortex - M0+ I/O Processor (80MHz)	Yes	Yes	Yes
Internal Memory	ECC Flash	4MB	3MB	2MB
	Graphics SRAM	1.3MB	1.3MB	1.3MB
	System SRAM (w/ECC)	2 x 512kB	2 x 512kB	2 x 512kB
External Memory Interfaces	QuadSPI Serial Flash Interface	2x Dual QuadSPI	2x Dual QuadSPI	2x Dual QuadSPI
	16 bit SDR DRAM	Yes	Yes	Yes
	32-Bit DDR2 DRAM	Yes	Yes	Yes
System Connectivity	CAN (FD)	x3	x3	x3
	I2C	x2	x2	x2
	UART/LIN	x3	x3	x3
	SPI	x5	x5	x5
	MLB 3-wire	Yes	Yes	Yes
	10/100 Ethernet + AVB	Yes	Yes	Yes
Analog Connectivity	SMD/SSD	x6	x6	x6
	12 Bit SAR ADC	Yes	Yes	Yes
System & General Purpose	Memory Protection	Yes	Yes	Yes
	Security	CSE2	CSE2	CSE2
	DMA	Yes	Yes	Yes
	Watchdog Timer	3	3	3
	Autonomous Real Time Clock	Yes	Yes	Yes
	IC/OC Timers/PWM	Yes	Yes	Yes
	GPIO	Yes	Yes	Yes
Audio/GFx/Video/Display	2D-ACE	x2	x2	x2
	HUD Warping	Yes	Yes	Yes
	GPU	GC355 (Open VG1.1 & Tiny UI)	GC355 (Open VG1.1 & Tiny UI)	GC355 (Open VG1.1 & Tiny UI)
	Digital Video In	Yes	Yes	Yes
	OpenLDI/LVDS	Yes	Yes	Yes
	TCON/ RSDS	Yes	Yes	Yes
	TCON-lite	Yes	Yes	Yes
	SGM	Yes	Yes	Yes
	LCD Segment Display	Yes	Yes	Yes
Package Options	LQFP	176/ 208 LQFP	176/ 208 LQFP	176/ 208 LQFP
	BGA	516 MAPBGA	516 MAPBGA	-

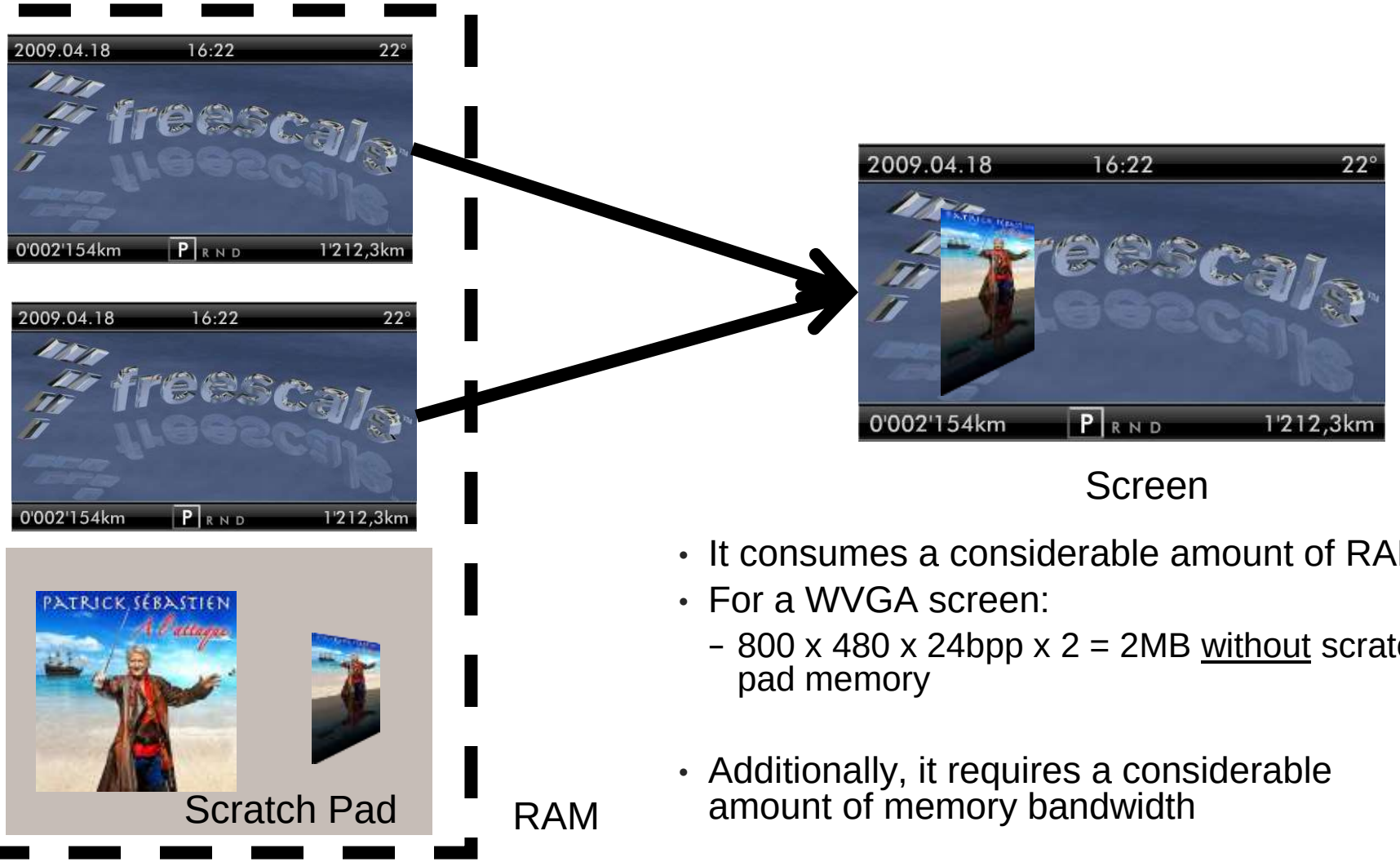
MAC57D5xx
Graphics Sub-system

Graphics



- ✓Vector Graphic Processor
- ✓2D-ACE
- ✓Inline HUD Warping
- ✓TCON, RSDS, OpenLDI/LVDS

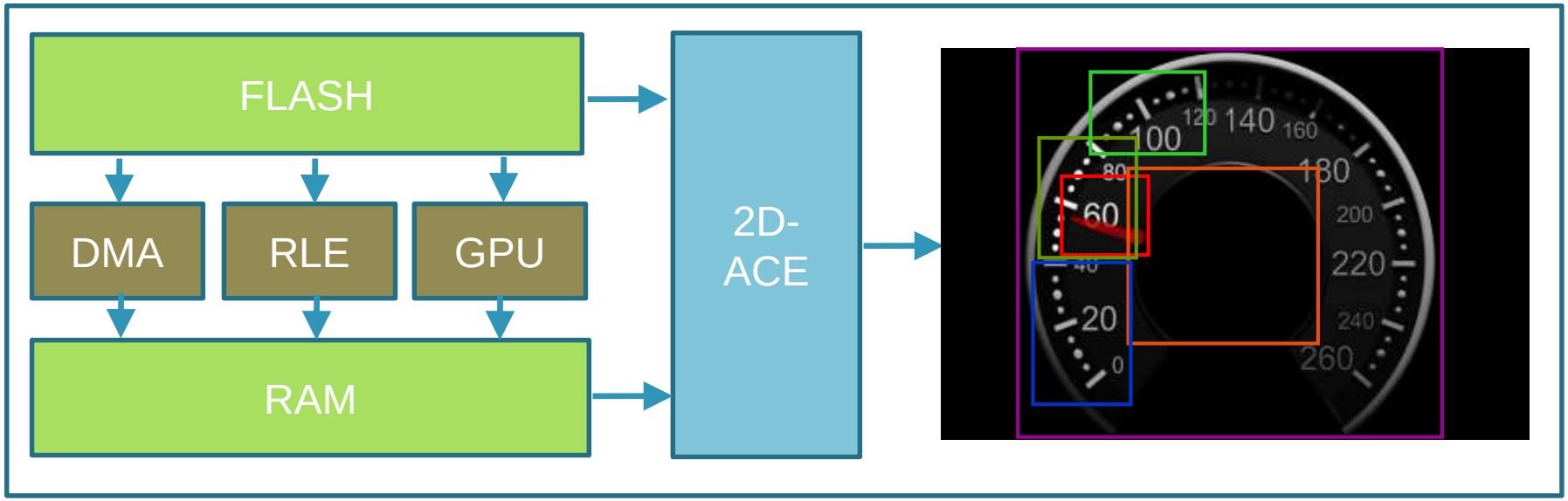
How graphics are typically rendered?



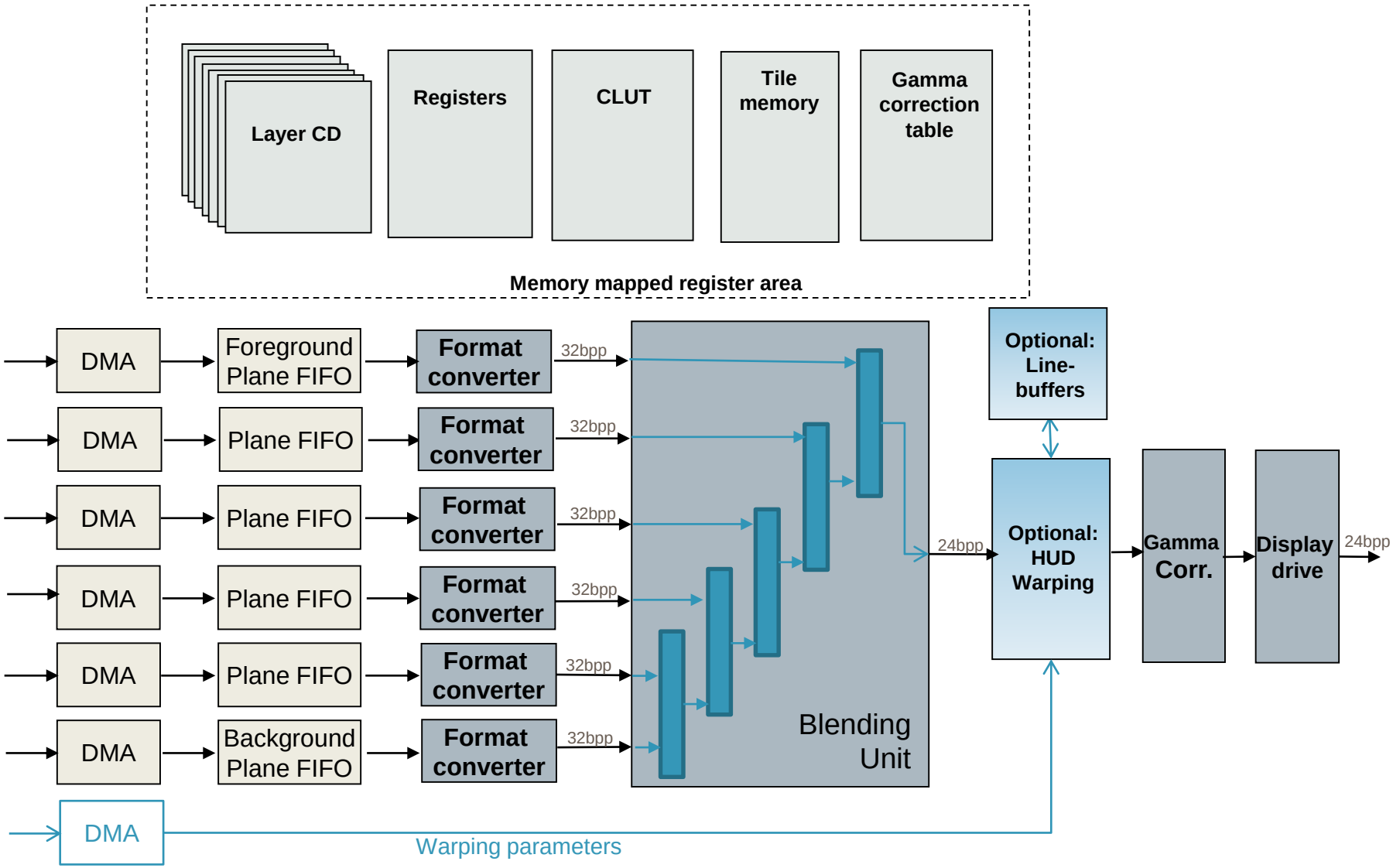
- It consumes a considerable amount of RAM
- For a WVGA screen:
  - 800 x 480 x 24bpp x 2 = 2MB without scratch pad memory
- Additionally, it requires a considerable amount of memory bandwidth

2D-ACE: Concept

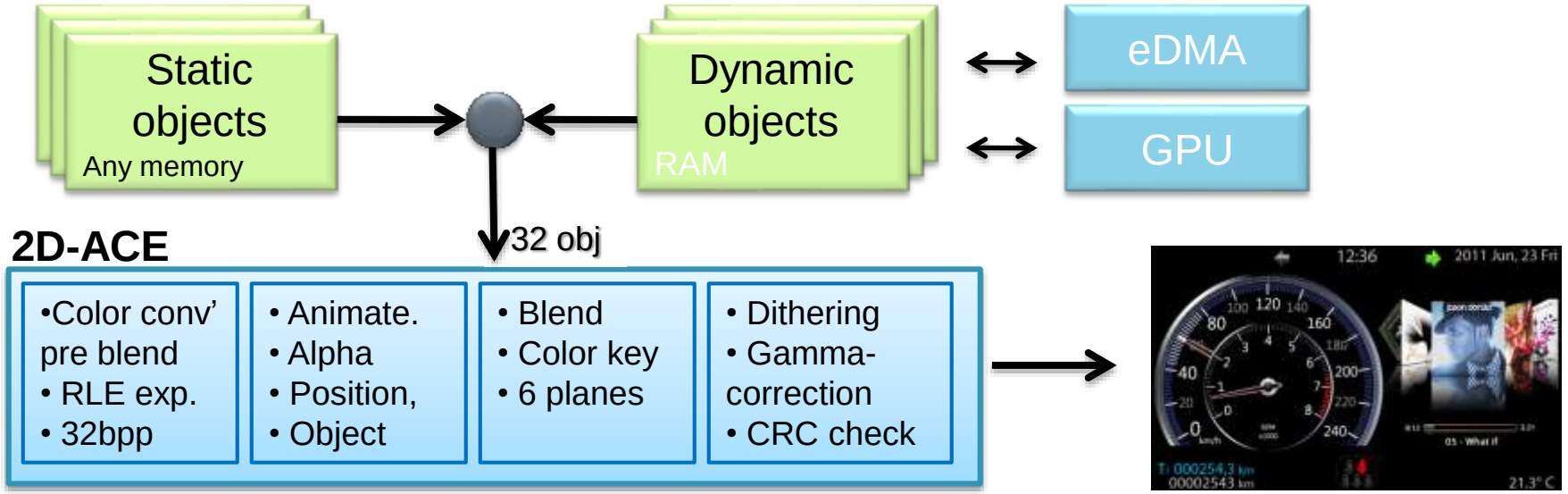
- Real time, un-buffered screen composition
- Multiple color formats, optimized for high quality and low memory footprint
- Hardware-accelerated sprite animation, object, alpha, position, color key, scroll
- Automatic, synchronized and high latency-tolerant: needs very little CPU time



2D-ACE block diagram



2D-ACE: High Level Overview



- 32 layers
- 6 planes
- Up to 80MHz pixel clock
- Memory size optimized
- Per-object animation at frame rate
- Frame buffer limited by memory size (all memories, RAM, ROM INT, EXT)
- Support 16, 24, 32 bit color depth.
- Support 1, 2, 4, 8bpp indirect color mode
- Alpha blend (per pixel & per layer in 6 planes)
- Chroma key (range per RGB component in 6 planes)
- Combined alpha blend and chroma key modes
- Font mode blending (transparency mode/alpha map)
- Highlight area mode. (luminance offset)
- Tile mode
- Safety mode support

2D-ACE: Color conversion

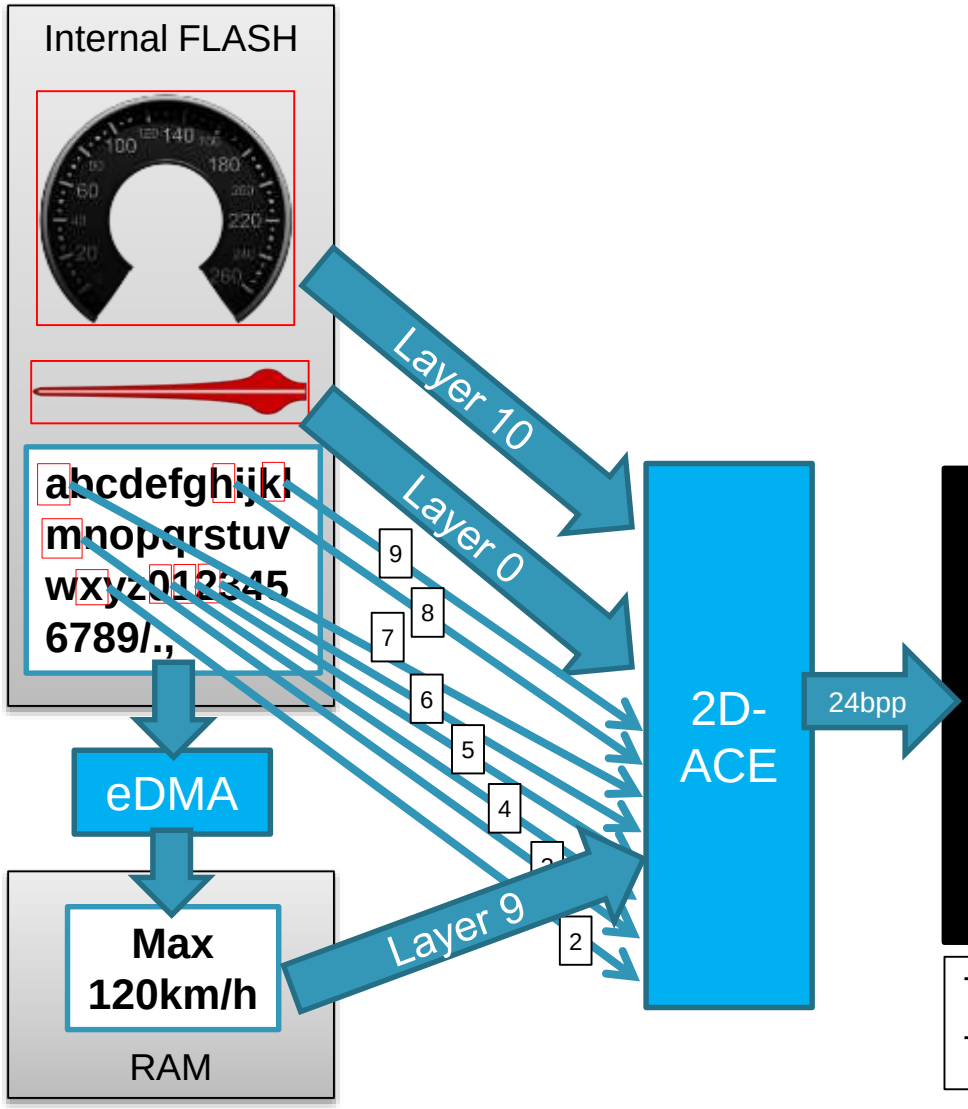
Notes

- **YUV4:2:2** (YCbCr422)
.. Programmable coefficient
- **RLE**
.. 8,16,32bpp expansion
- **A4, A8**
.. Pre blend with fore and back color
- **LO4, LO8**
.. Luminance offset, pre-blend alpha
- **ARGB8888**
.. normal or pre-multiplied alpha
- **APAL88**
.. Indexed 8bpp + 8bpp alpha

Object color format

- **Indexed** (RGBA8888 CLUT)
..1,2,4,8 bpp
..APAL88
- **Direct**
..RGB565, ..ARGB4444, ..ARGB1555, ..RGB888, ..ARGB8888,
..YUV4:2:2
- **Special**
..A4, A8
..LO4, LO8.
..RLE

How does the 2D-ACE renders a frame?



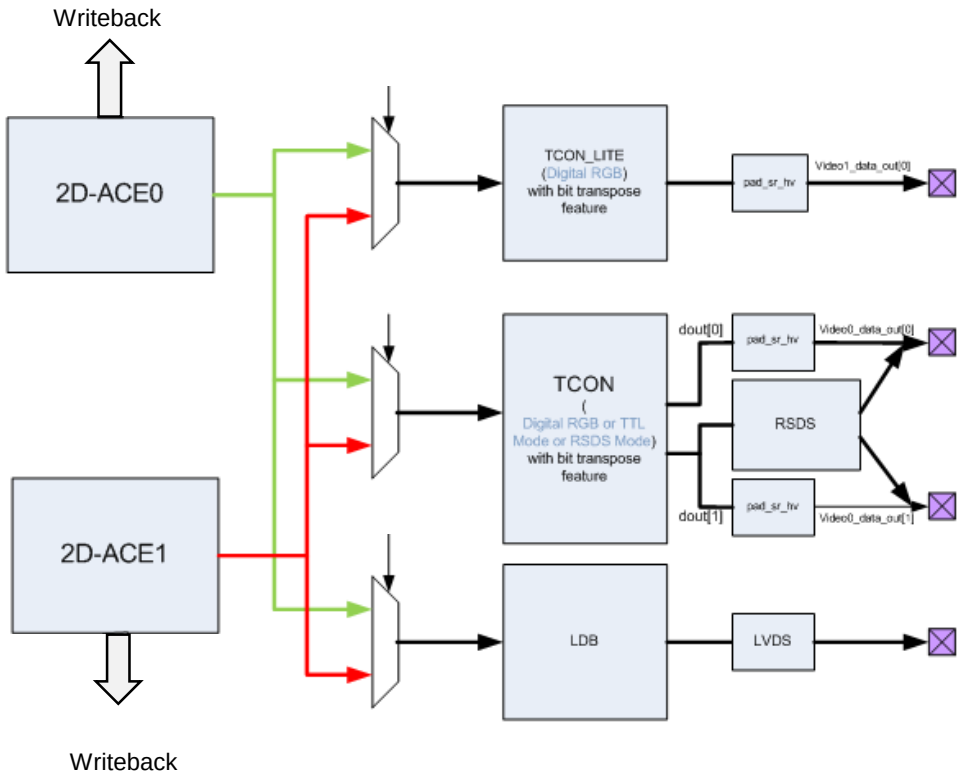
Object	Size
Speedometer	200x200 8bpp
Needle	120x20 8bpp
ascii font set	400x400 4bpp
text box max speed	60x40 4bpp

Total RAM used: 1200 bytes

Total Flash used: 122400 bytes

480x272 24-bit screen
(would require ~400,000B buffer)

Display Output Options



2D-ACE0(HUD)	2D_ACE1
Digital RGB	Digital RGB
Digital RGB	RSDS+TCON
Digital RGB	LVDS
RSDS+TCON	Digital RGB
RSDS+TCON	LVDS
LVDS	Digital RGB
LVDS	RSDS+TCON

2D-ACE Software Graphics Libraries

- Drivers were made to work together in an abstract way
- Architecture allows correct interaction between software layers
- Users can focus in movie clips and functionality without worrying about lower layers

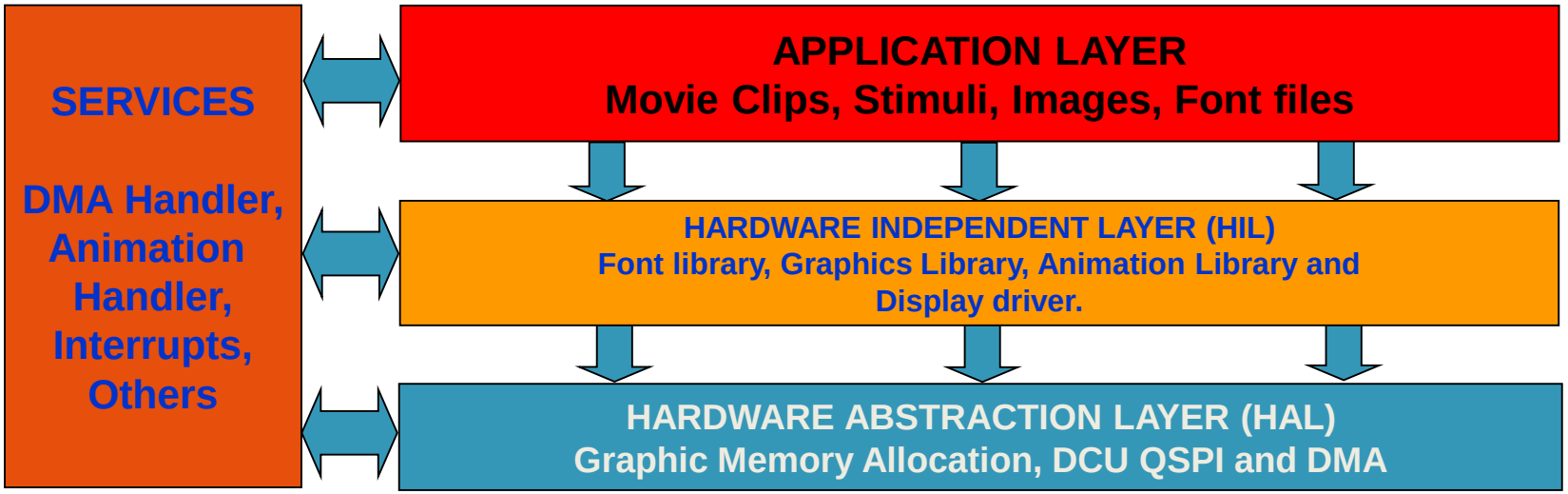
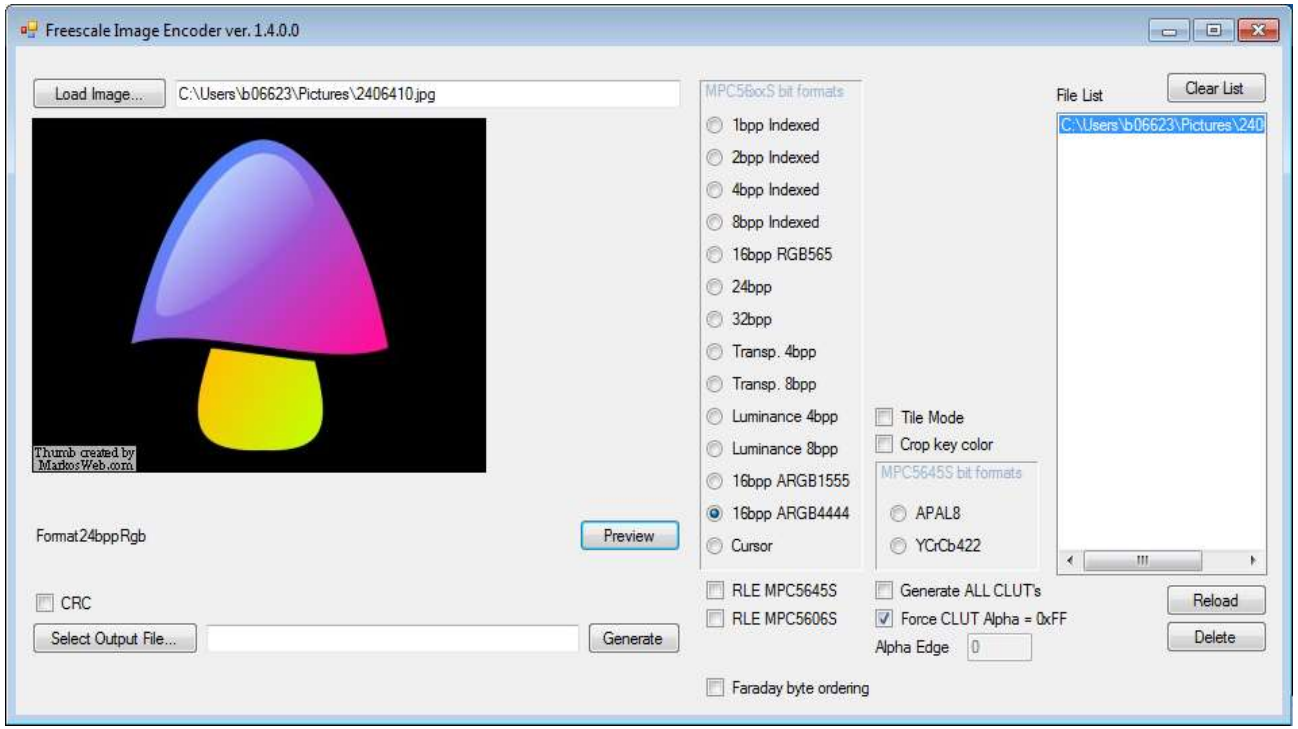
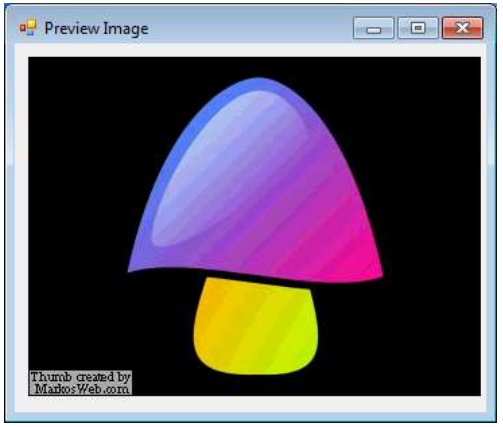


Image Encoder Tool

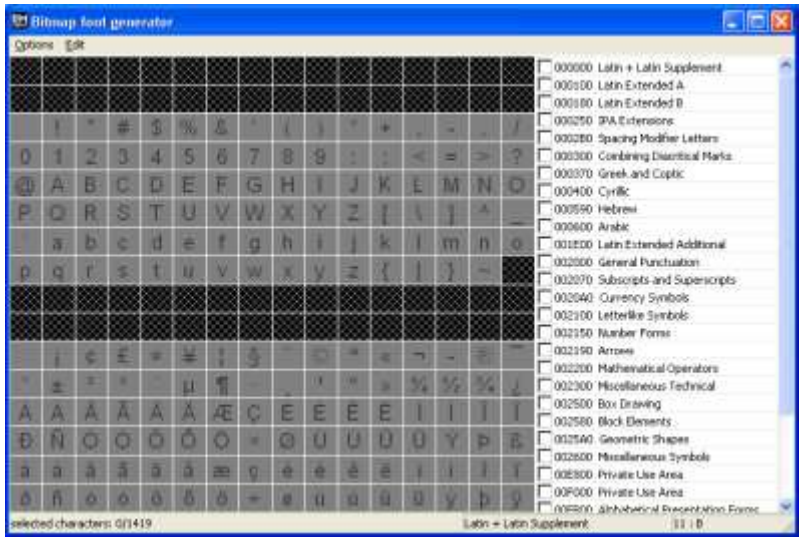
- Supports ALL 2D-ACE formats
- Special features such: RLE, Indexing, Preview window and Image array list.

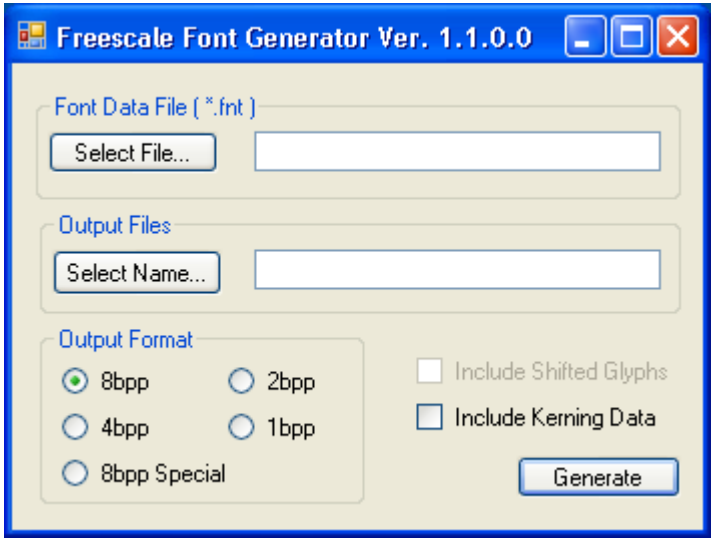




Font Encoder Tool

- HW accelerated DMA transfers for 8bpp and 4bpp
- Includes Kerning
- CPU rendering for size optimized 2bpp, 1bpp





GC355 Vector Graphics Engine

GC355 VGMark Performance @ 320MHz

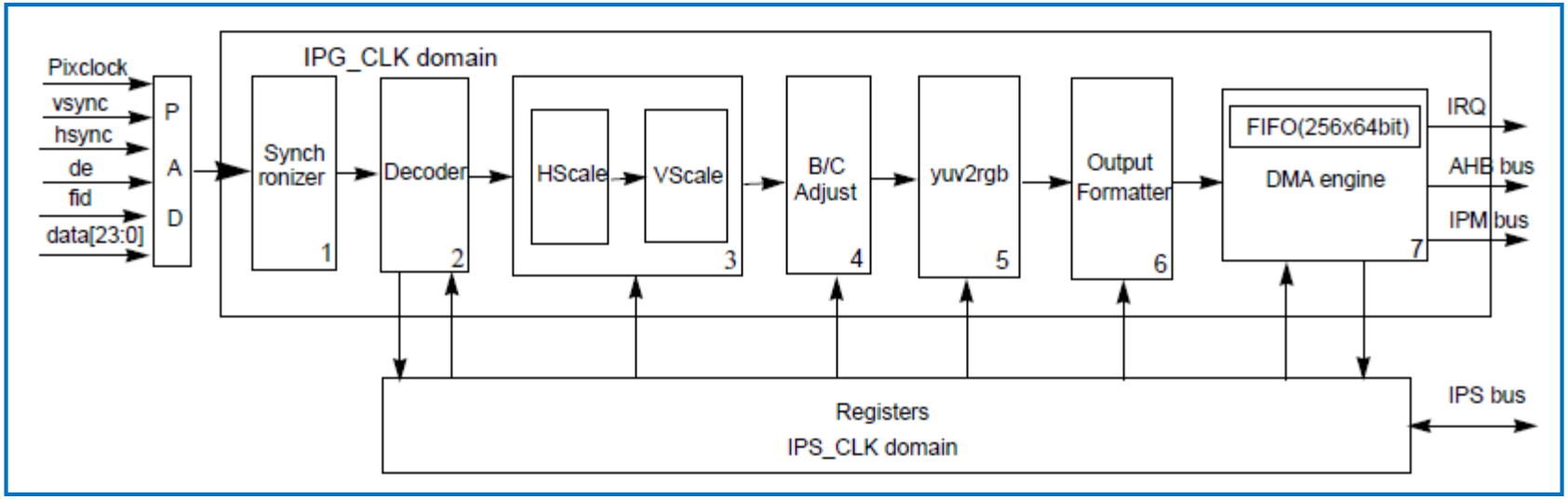
GC355	VGA resolution 16X AA (Frames/sec)
	320MHz (projected)
Tiger (rotation)	85
UI	96
Navigation	28
Flash	42

- Independent 2D Vector GPU Use-cases:
  - Instrument cluster: 2D engine accelerates needles at 60fps; 2D-ACE renders the rest of the scene
- Infotainment: UI acceleration
- Native rendering of true-type fonts, with 16x Anti-Aliasing
- Additional graphics acceleration for dual display systems

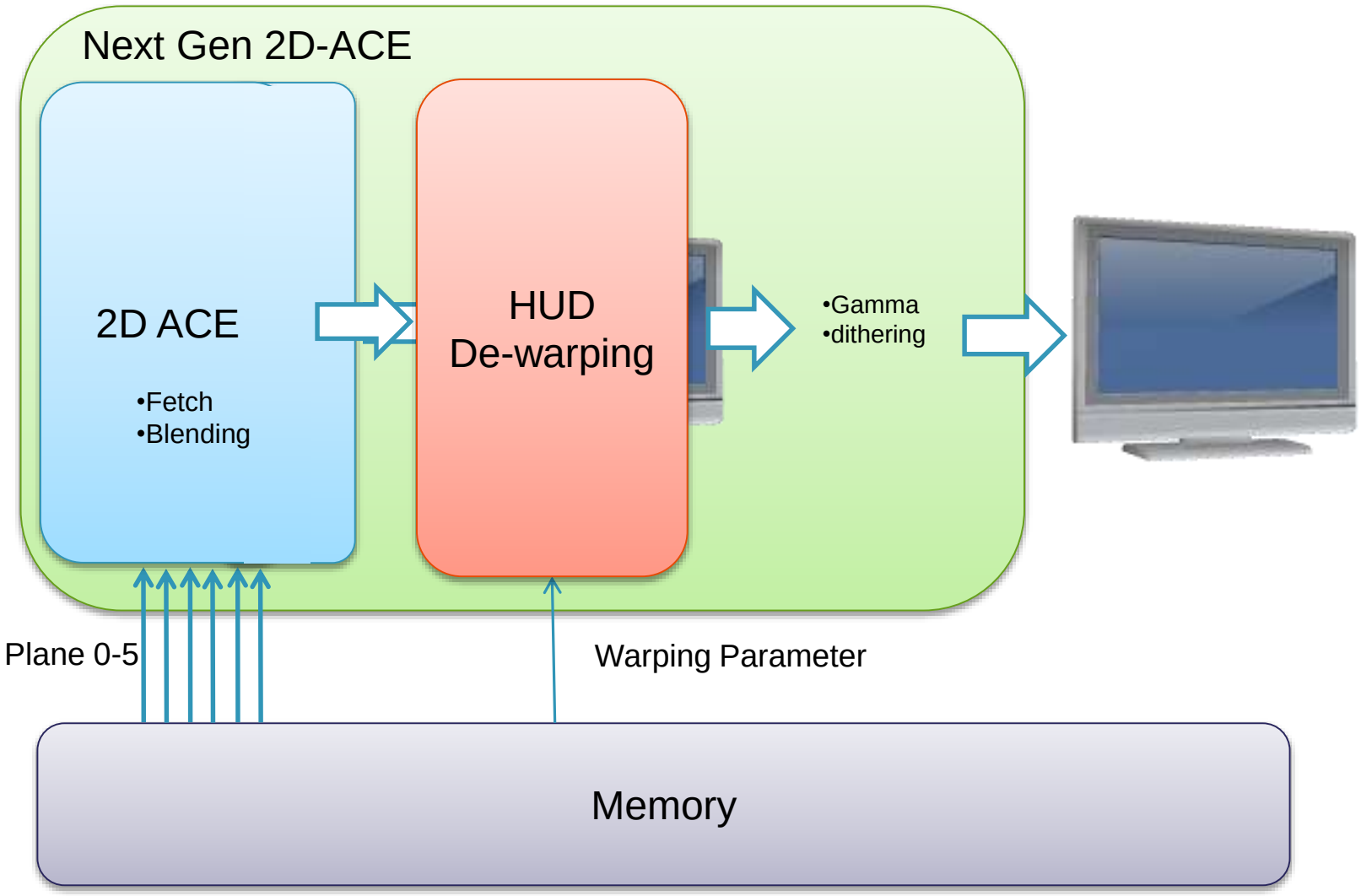
Video Interface Unit (VIU4)

- QVGA to XVGA input/output resolution
- Brightness and Contrast Adjustment
- Up to 1/8th video down-scaling
- Up to 2x horizontal video up-scaling
- Horizontal Mirroring
- DMA for direct copy to system memory

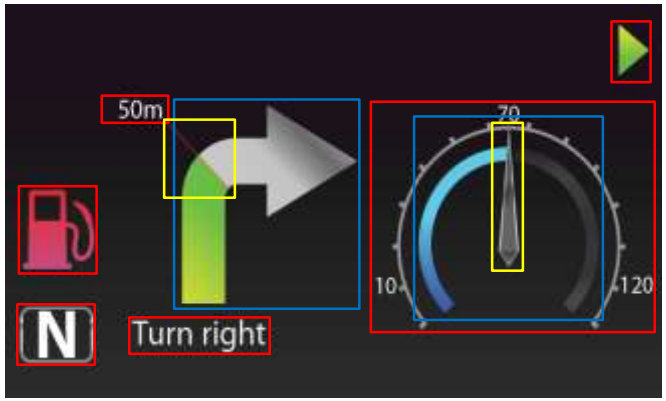
Input Formats	Output Formats
ITU-R BT.565 Parallel RGB888/666/565 Serial RGB888 (3 cyc) Monochrome	8bpp, 16bpp, 32bpp 8bpp monochrome YUV422 YUV444



HUD Warping / Architecture



In-the-loop De-warping



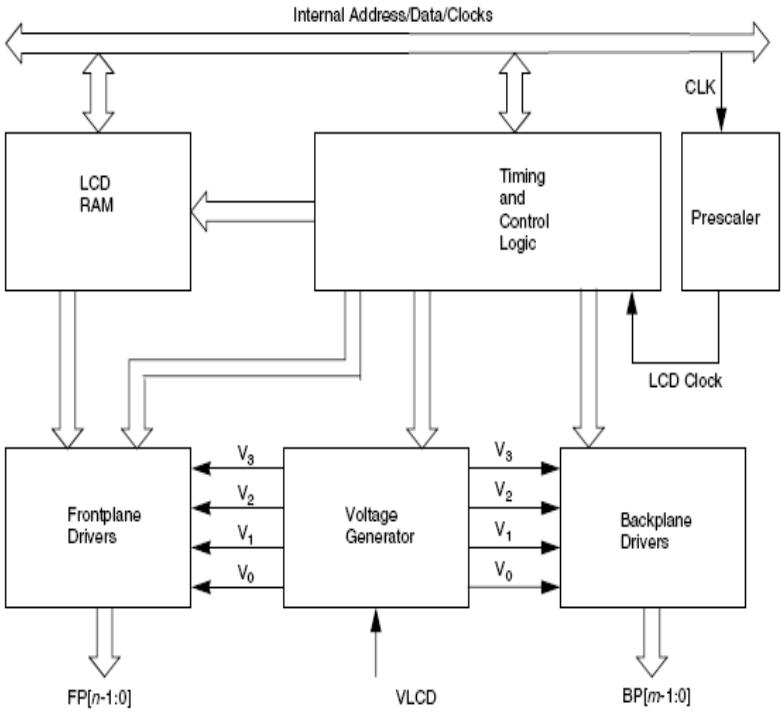
Fetch graphic data

Blend result

Apply de-warping

LCD Segment Controller

- Up to 40 front-plane drivers
- Up to 8 back-plane drivers
  - 40x4, 38x6, 36x8
- Remapping of backplane drivers
- Programmable frame clock generator
- Programmable bias voltage level selector
- Programmable output current
- Optional output current boost during transitions.
- Optional LCD frame frequency interrupt event
- Contrast adjustment
  - Contrast Adjustment phases



MAC57D5xx - Enablement Support

Operating Systems & MCAL's

- AUTOSAR MCAL & OS
- Green Hills Integrity
- MQX

Drivers

- Tiny 2D API
- OpenVG1.1
- 2D-Animation Composition Engine
- Sound Generator Module
- Ethernet AVB
- IOP/Stepper Motor
- Stepper Motor Stall Detect

HW Development & Reference Design

- Evaluation Board
  - 516 BGA
  - P/N & ASP TBD
- Instrument Cluster Reference Design
  - 516 MAPBGA
  - 208 LQFP

Compilers

- Green Hills
- Wind River
- ARM DS-5
- IAR

Debuggers

- Lauterbach
- P&E Micro ICDACMP
- Green Hills Probes

User Interface Design Tools

- Altia
- ElectroBit
- PEG

Flash Programming Tools

- P&E Cyclone Max
- Promik

Enablement

2015 Best Product In-vehicle of EDN

- Samples and EVB
- Reference designs
- Documents(DS, RM, SCH..)

DIS 55nm NPI Schedules *(Timing Reflects Lead Customer)*

Last Updated 2 September 2014

Preliminary Samples (Room Temp)
Final Samples (Tn Temp + Bl, Qual Intent)
Final MC Qualification
Production

32-bit 55nm FSL Driver Information Systems NPIs

NPI	Status	PNs	Packages	2013 Q1	2013 Q2	2013 Q3	2013 Q4	2014 Q1	2014 Q2	2014 Q3	2014 Q4	2015 Q1	2015 Q2	2015 Q3	2015 Q4	2016 Q1	2016 Q2	2016 Q3	2016 Q4
MAC57D5xx Halo	In Execution*	*MAC57D54HAVLU*	516 MAPBGA						Jun				Jun		Nov				
		MAC57D54HAVLT	208 LQFP						Jun				Jun		Nov				
		MAC57D54HAVMO	176 LQFP									Feb		Sep		Jan			

- Halo System IO Definition_JAN14.xlsx
- MAC57D5_4xx Halo_Corona Product Brief_Rev10.pdf
- MAC57D5xx Halo Datasheet Rev2.pdf
- MAC57D5xx Halo Reference Manual Rev1.pdf
- MACDISMCUHALOFS.pdf
- Halo_AdapterBoard - TFTDisplay_Schematic.pdf
- MAC57D5xH_516BGA_EVB - Quick Start Guide.pdf
- MAC57D5xH_516BGA_EVB - Quick Start Guide_PRELIMIN.pdf
- MAC57D54H Quick Start Template.zip
- MAC57D54H_CustomerEVB_RevA1_Schematic.pdf
- MAC57D54H_CustomerEVB_RevB1_Schematic.pdf
- MAC57D54H_Eratta_27June2014.pdf

Summary

Industry's highest performance, multi-core, single-chip instrument cluster solution based on ARM technology

- Automotive cluster manufacturers see an increasing demand for cutting edge graphics, Freescale's MCUs deliver **the widest range of performance and memory expansion options** to enable scalable, attention-grabbing instrument clusters.

- Automotive cluster manufacturers can optimize their solution with the ARM Cortex-based **multi-core** MCU family which offers premium level graphics capability, including heads-up display, which traditionally required multiple external components, in a **single-chip and balanced architecture solution**.

- Automotive cluster manufacturers can differentiate thanks to Freescale providing a simplified development environment for a more **streamlined** approach, leveraging **proprietary IP** and **optimized code** for quicker time to market.

www.Freescale.com