Industrial Networking: Leverage QorIQ Communications Processors for PROFIBUS, PROFINET, EtherNet/IP, CAN, etc.

APF-IND-T0049

Hao Sun

J A N . 2 0 1 5

External Use

Agenda

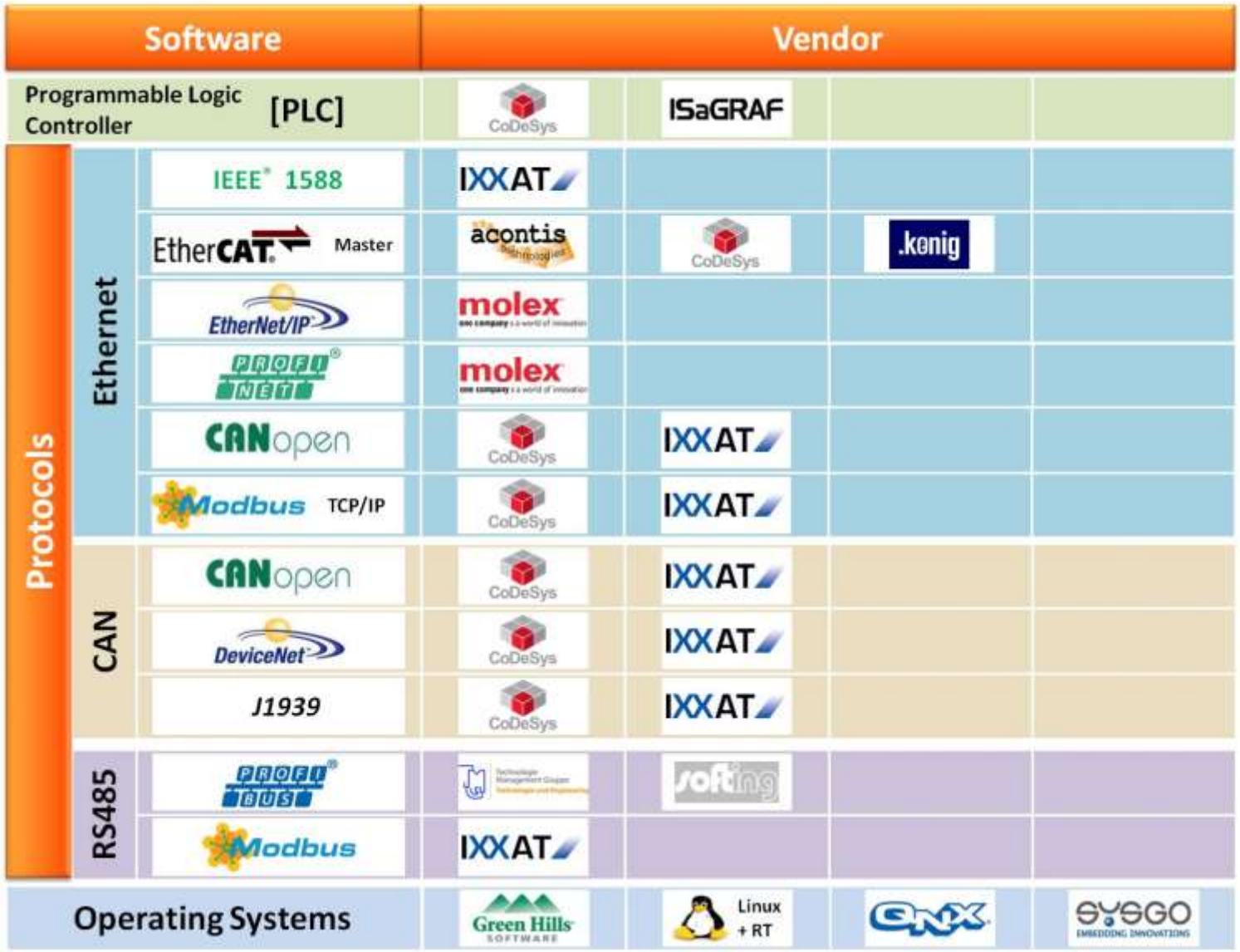
- Protocols
- Serial Based Protocols
- Ethernet

Protocols and Physical Interfaces



	IEEE 802.11	IEEE 802.3	RS485	CAN
Interface	PCIe/USB/SPI/I²C	MII/RMII/RGMII/SGMII	UART/QE UCC	CAN
Topology	Multi Point	Point to Point	Multi Drop	Multi Drop
Distance	70 – 250m	100m	100 – 1,200m	40 – 1,000m
Protocol	PROFINET	PROFINET	PROFIBUS	
	Modbus TCP/IP	Modbus TCP/IP	Modbus	
	EtherNet/IP	EtherNet/IP		DeviceNet
	ETHERNET POWERLINK	ETHERNET POWERLINK		
	CANopen	CANopen		CANopen
		EtherCAT Master		J1939
	P-Series T-Series MPC8309 (PCI) LS-Series	P-Series T-Series MPC8306/9 LS-Series	P1025/16/21/16 T1040/42/20/22 MPC8306/9 LS102xA	P1010 MPC8306/9 LS102xA

Industrial Support Software



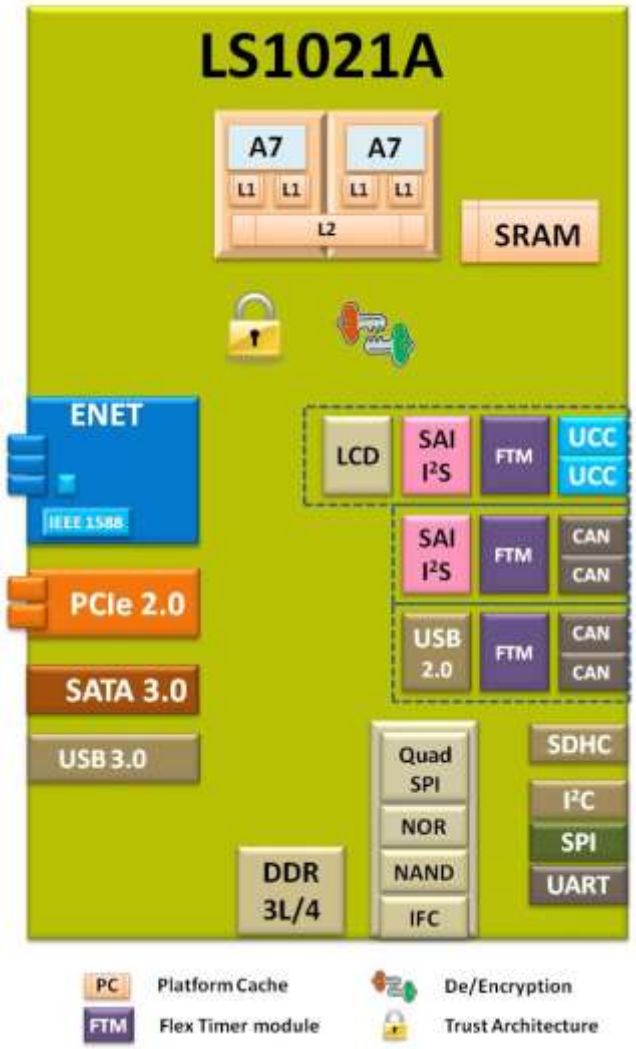
Serial Based Protocols

UART
CAN
PROFIBUS

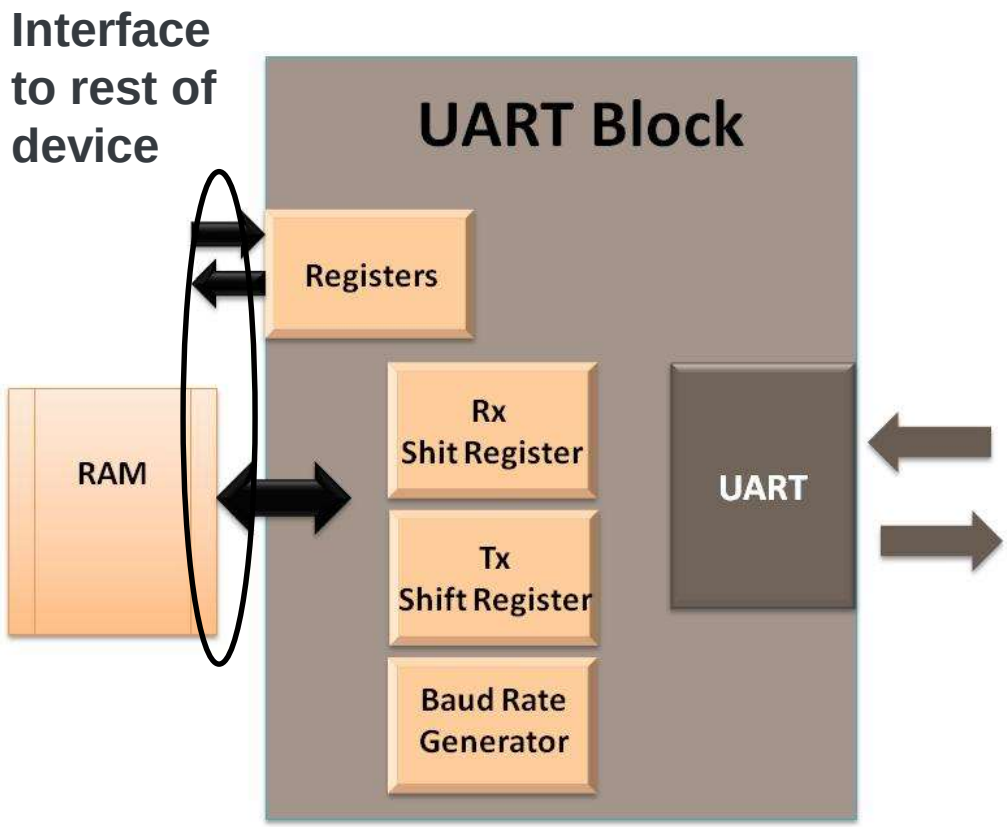
Example Device that Covers Most of the Protocols

	LS1021A	LS1020A	LS1022A
Core Type	ARM Cortex™-A7 MPCore™ + NEON		
Cores/Threads	2 / 2		
Frequency	Up to 1GHz		Up to 600MHz
L1 I/D	32kB / 32kB with ECC		
L2 (Unified)	512kB Shared with ECC		
SRAM	128kB with ECC		
DDR	1x(16/32B it+ECC) DDR3L/4 up to 1.3GT/s		1x(16bit+ECC) DDR3Lup to 1.0GT/s
SerDes	4 up to 6.0GHz		1 up to
Ethernet	3 x 1GE		2 x 1GE
PCIe	2 x Gen 2.0 (up to 5.0GT/s)		1 x Gen 2.0 (up to 5.0GT/s)
SATA 3.0	1 up to 6.0GHz		No
USB	1 x USB 3.0,1 x USB 2.0		1 x USB 2.0
CAN	Up to 4	0	Up to 4
TDM/HDLC	2		No
UART/I²C/SPI	Up to 8 / 3 / 2		
I²S	Up to 4		
LCD	1 x Controller	No	
Acceleration	SEC,QE		No
	Trusted architecture		
	Pin Compatible 19x19mm, 0.8mm pitch		

Low Power < 3W



Simplified UART Hardware Block



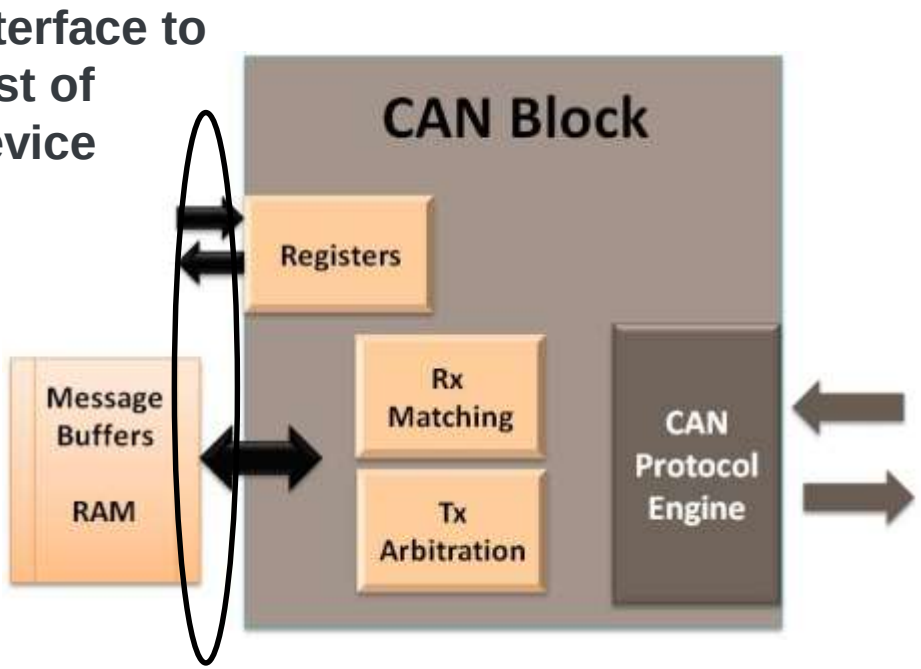
- Hardware block to perform the UART function

Simplified CAN Hardware Block

DeviceNet

CANopen

J1939



- The CAN 2.0 B protocol specification is performed in a hardware block

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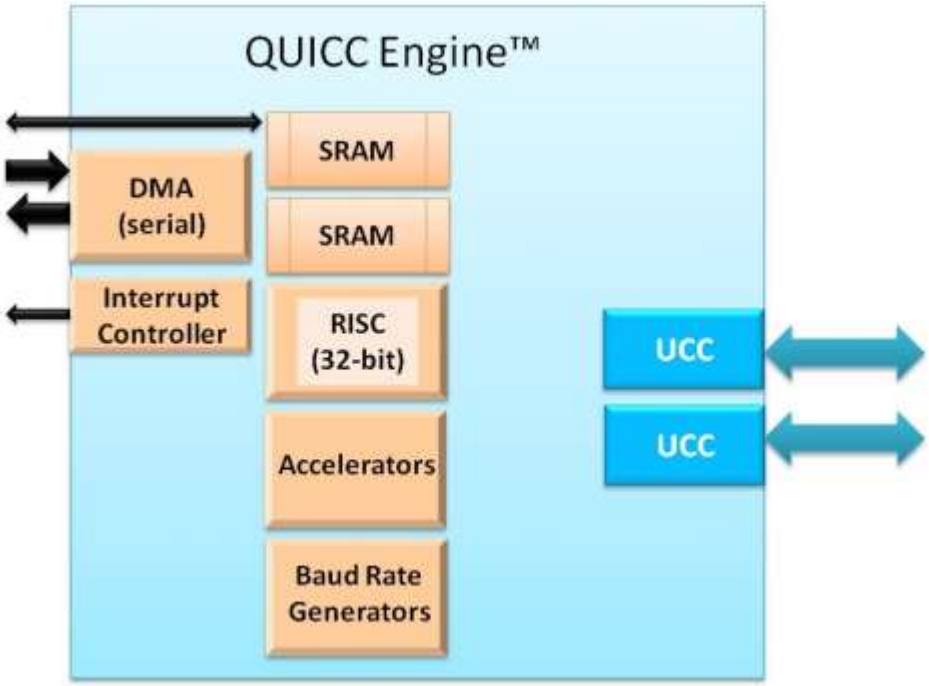
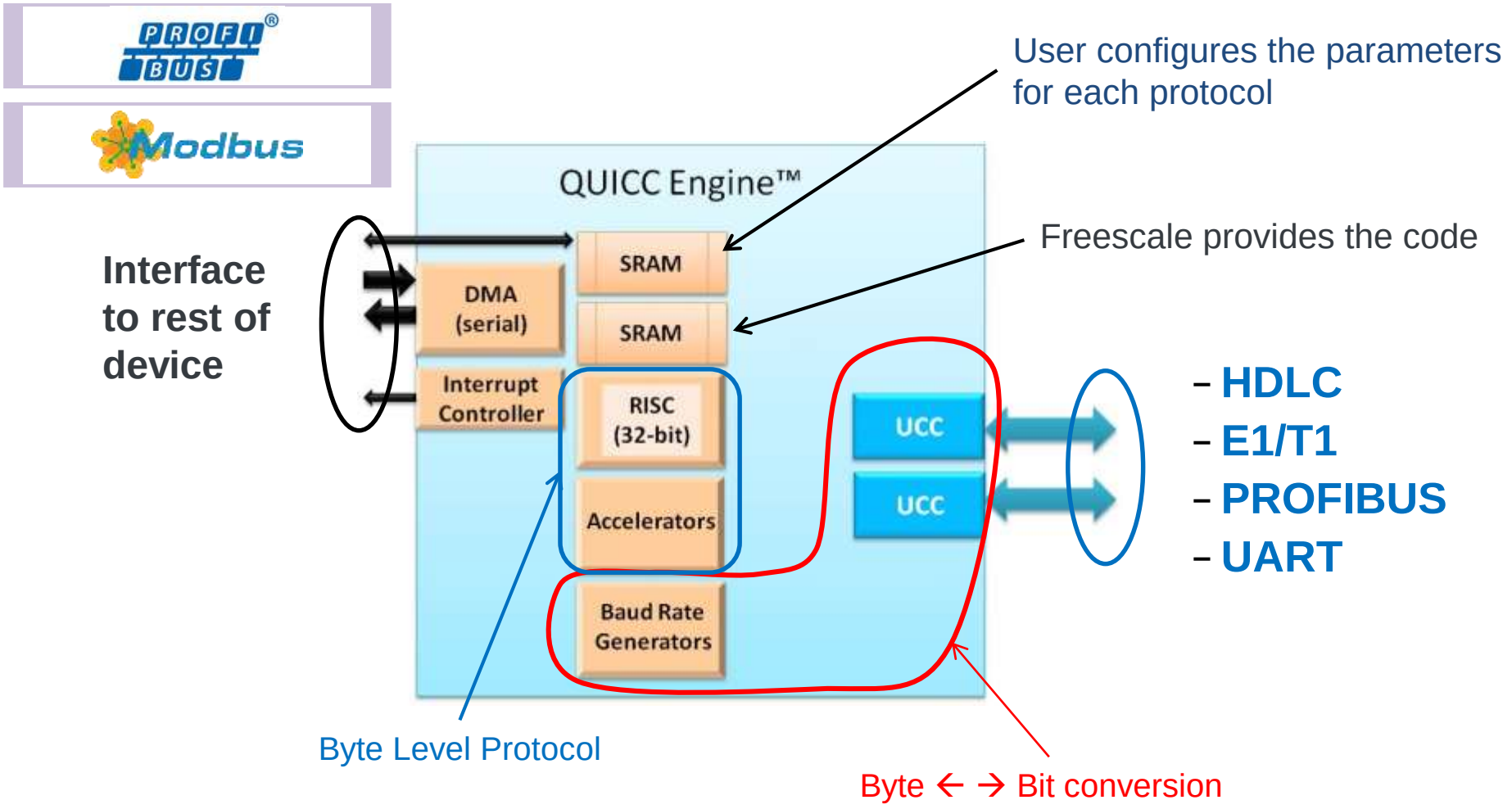
Simplified QUICC Engine Block Diagram



Protocols

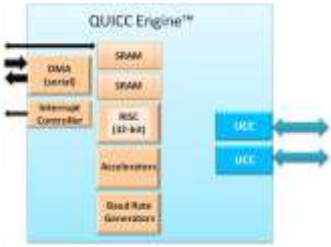
- Ethernet
- ATM
- HDLC
- E1/T1
- PROFIBUS
- UART

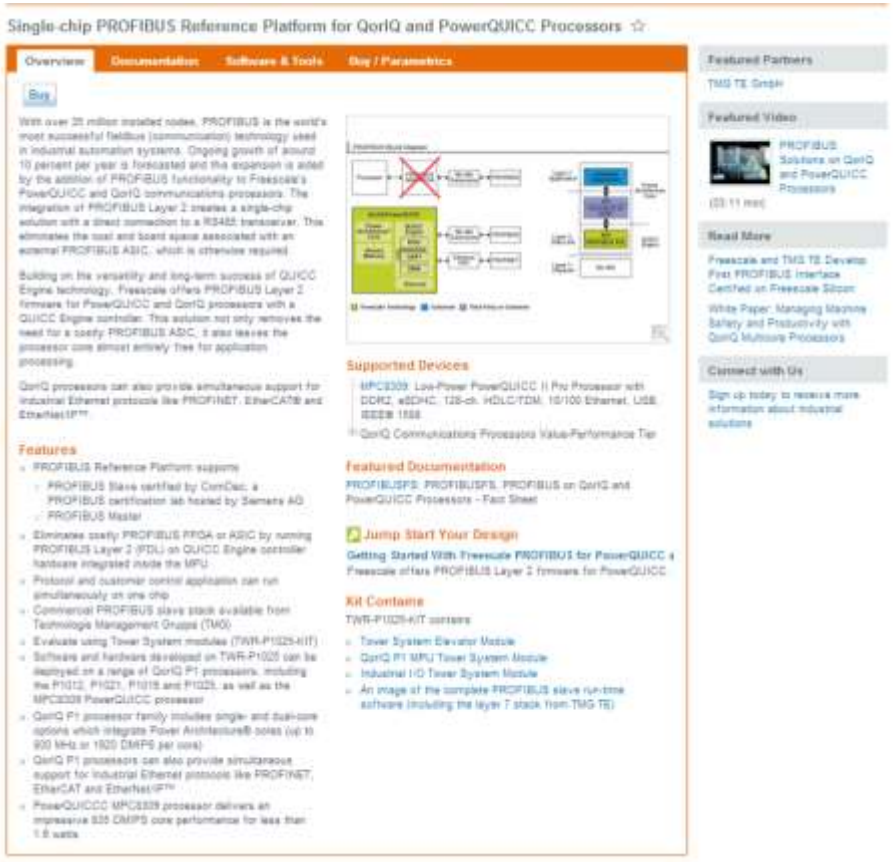
Simplified QUICC Engine Block Diagram



Example Protocol PROFIBUS

www.freescale.com/profibusQorIQ





For more information contact

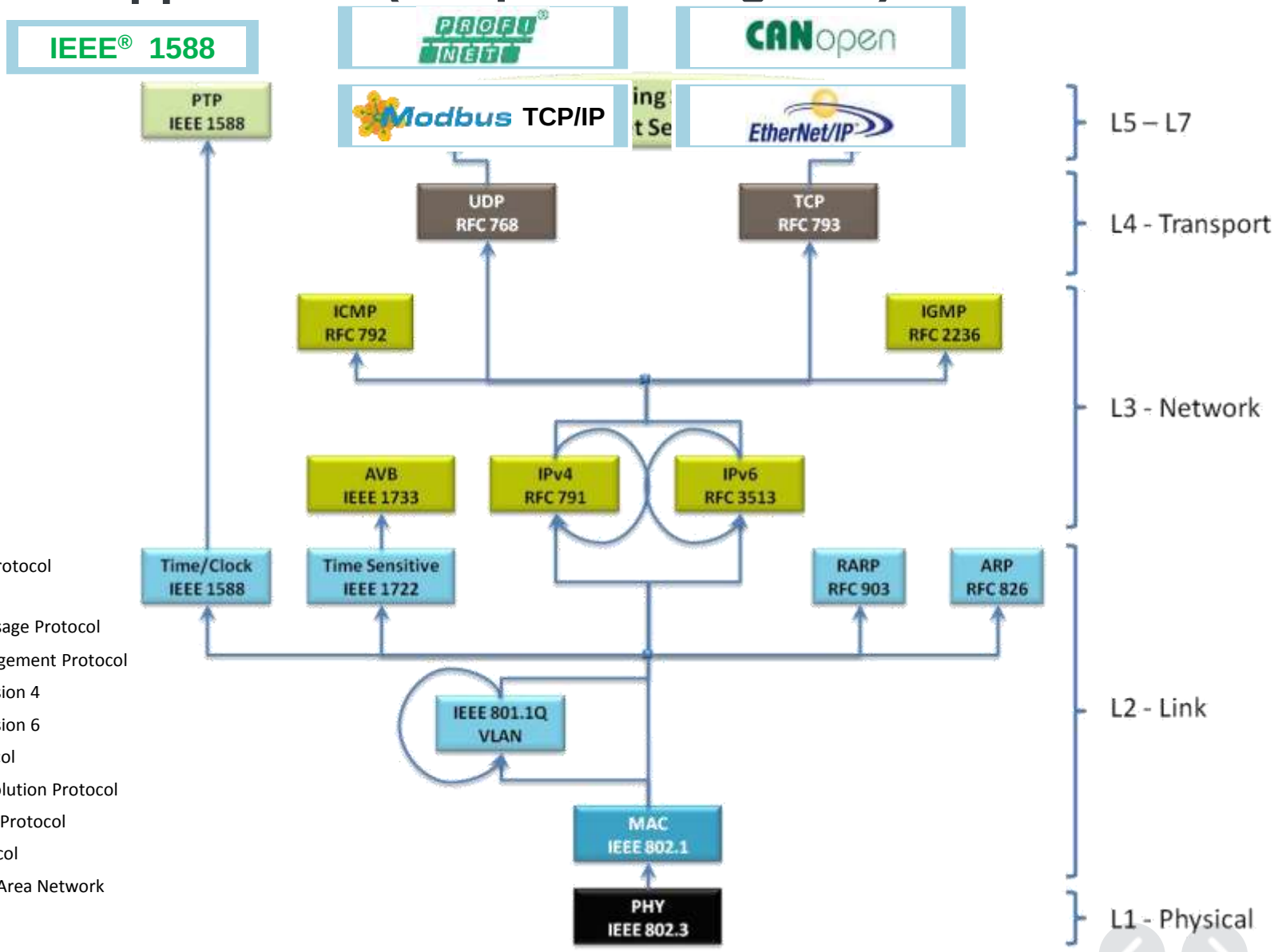
iain.davidson@freescale.com **or** profibus@freescale.com

Ethernet

Internet Protocol / Ethernet

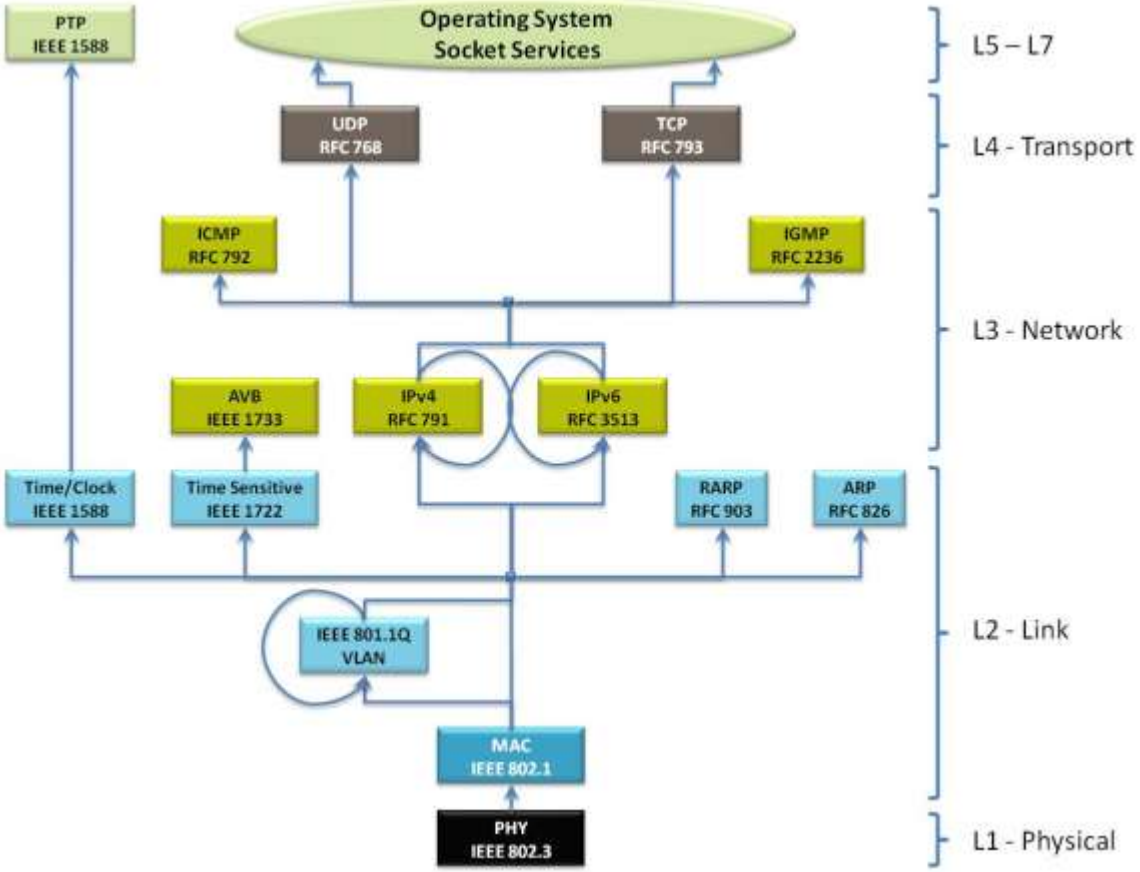
- Machines (devices) are now using Internet Protocol (IP) over Ethernet more and more.
- To connect, you need an Ethernet controller with at least the capabilities of doing the low level media access control (MAC) linked to a physical interface (PHY).
- Applications do not generally directly “talk” IP. They normally use a software abstracted method, like sockets.
- So how do you get from the Ethernet to the application layer?

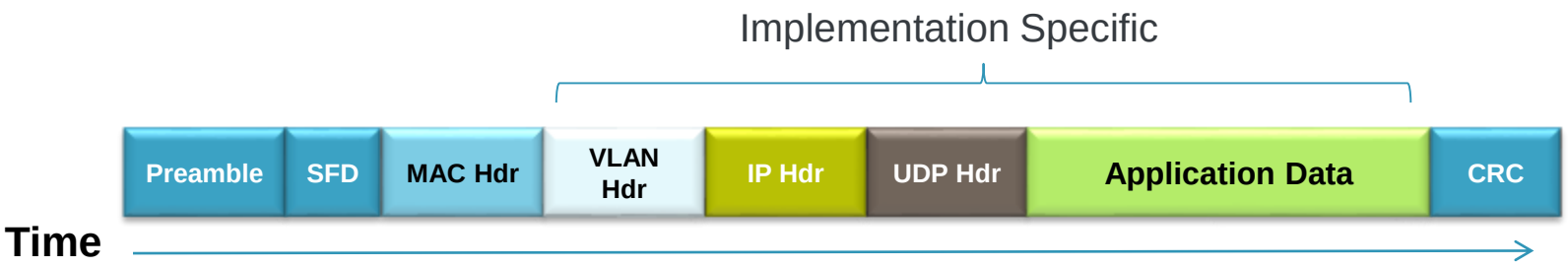
Ethernet to Application (Simplified Diagram)



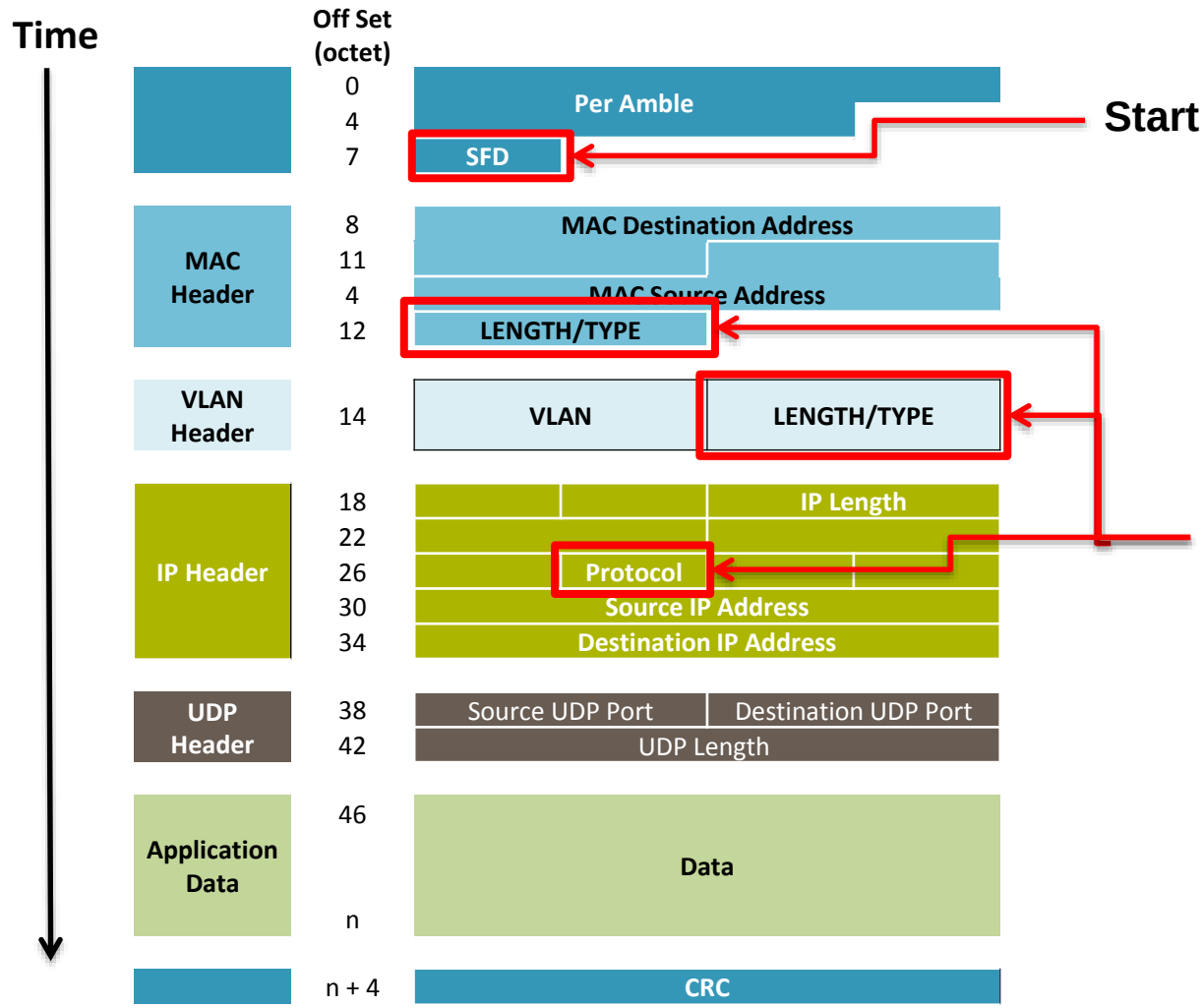
ARP Address Resolution Protocol
AVB Audio Video Bridging
ICMP Internet Control Message Protocol
IGMP Internet Group Management Protocol
IPv4 Internet Protocol version 4
IPv6 Internet Protocol version 6
PTP Precision Time Protocol
RARP Reverse Address Resolution Protocol
TCP Transmission Control Protocol
UDP User Datagram Protocol
VLAN Virtual Bridged Local Area Network

Ethernet Frame





Ethernet Frame [Protocols]



Start Frame Delimiter

To determine what the next Header type is, and hence it's format. This is achieved via a field in each of the headers. This is highlighted for the example sequence

Ethernet Frame [Addressing]

Time

Off Set (octet)

0 Per Amble
4
7 SFD

MAC Header
8 MAC Destination Address
11
4 MAC Source Address
12 LENGTH/TYPE

VLAN Header
14 VLAN LENGTH/TYPE

IP Header
18 IP Length
22
26 Protocol
30 Source IP Address
34 Destination IP Address

UDP Header
38 Source UDP Port Destination UDP Port
42 UDP Length

Application Data
46 Data
n

n + 4 CRC

Selects this Ethernet Controller

Selects the LAN network

Selects the IP address linked to this application

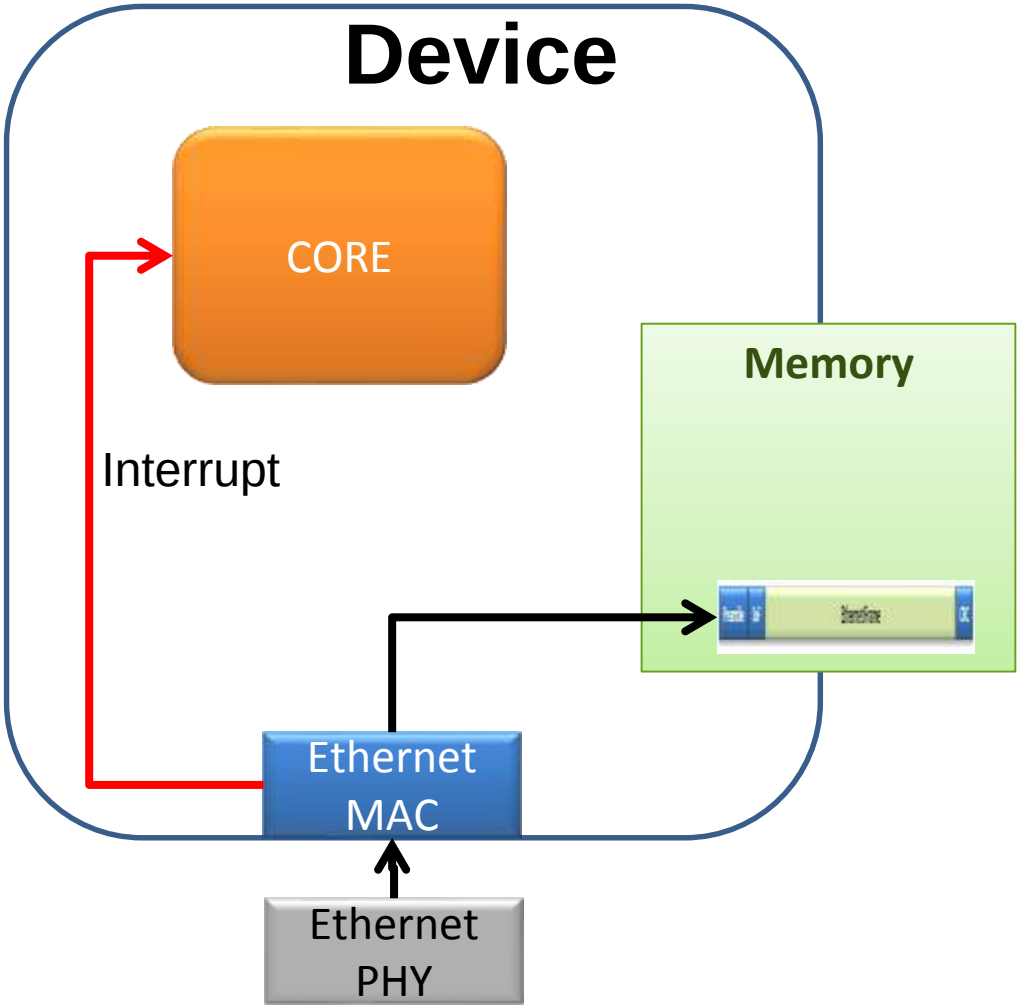
Selects the port number linked to this applications' socket

Basic Ethernet Controller

Ethernet **Media Access Control (MAC)** (Hardware)

1. On Receive detects Ethernet Frame and places it into memory

2. On Transmit takes the contents of memory and sends it to the PHY



Different Types of Ethernet Controllers

SIMPLE Controller

Ingress

This takes each of the received frames from the PHY and places them into a buffer and informs the CORE/CPU

Checks CRC to see if the frame is valid

Egress

CORE passes a buffer containing the frame to be transmitted and the controller DMAs it to the PHY

Generates the CRC for the frame being transmitted

IEEE 1588 Assist

In addition to the functions performed by SIMPLE controller, it performs:

Ingress

Copies the value of the IEEE 1588 clock when SFD is detected and the value is passed to the CORE/CPU referenced to this received frame

Egress

If the frame is flagged to have the IEEE 1588 time stamp included, the controller copies the value of the IEEE 1588 clock to the time stamp field

QUEUE Assist

In addition to the functions performed by IEEE 1588 Assist controller, it performs:

Ingress

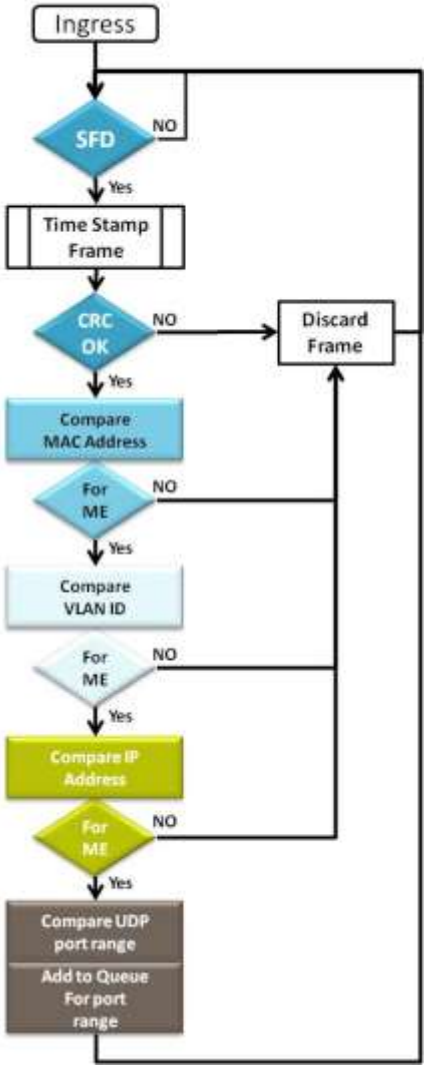
There is a comparison performed on fields in the frame being received, to determine which queue that the information about this frame is placed in for the CORE/CPU

Egress

A round robin or some other selection method is used to check the transmit queues to obtain the next frame to be transmitted

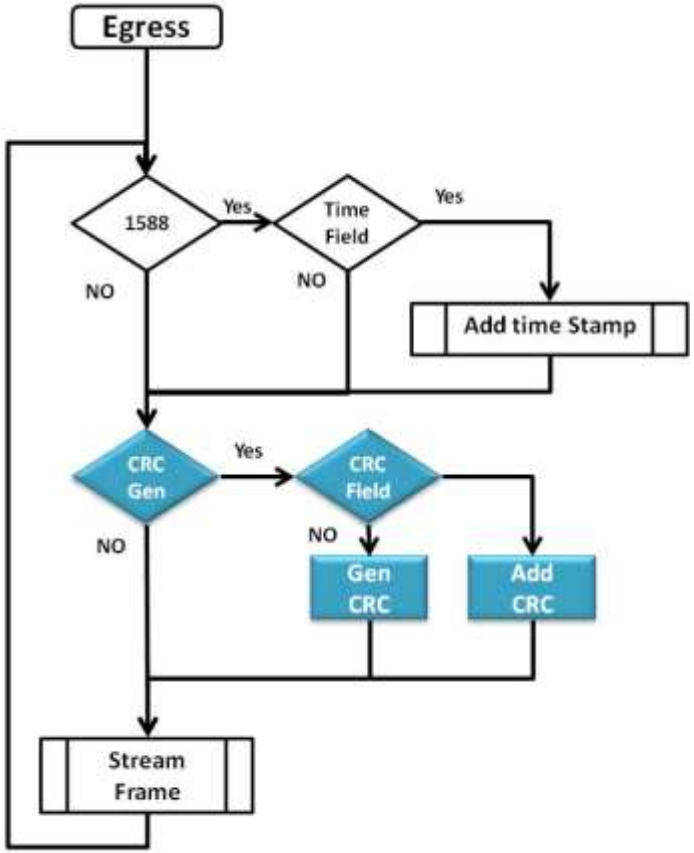
Features of Ethernet Controllers (INGRESS)

Ethernet Controller Type		
Queue Assist	IEEE 1588 Assist	Simple
Hardware	Hardware	Hardware
Hardware	Hardware	n/a
Hardware	Hardware	Hardware
Hardware	Software	Software
Hardware	Software	Software
Hardware	Software	Software
Hardware	Software	Software



Features of Ethernet Controllers (EGRESS)

Ethernet Controller Type		
Queue Assist	IEEE 1588 Assist	Simple
Hardware	Hardware[2]	Software[1]
Hardware	Hardware	Hardware
Hardware	Hardware	Hardware



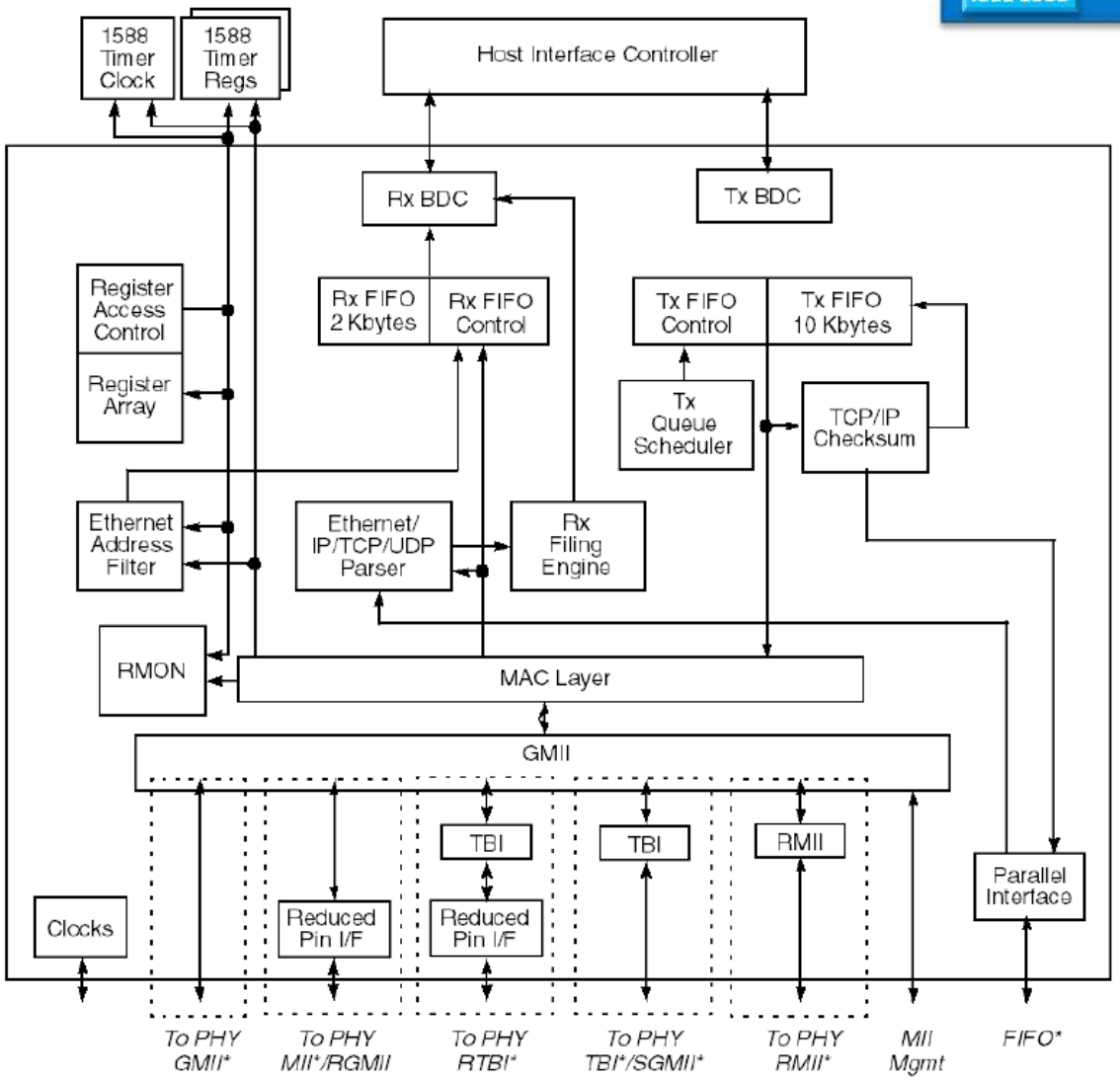
1. *Software has to generate the frame, then pass it to the Ethernet Controller, hence for PTP the time stamp will have a larger jitter than a hardware implementation*
2. *Will be required to generate the checksums for UDP/TCP/IP if they are required by the system*

Ethernet Controller in Value-Performance QorIQ

This is called the Enhanced Three-Speed Ethernet Controller (eTSEC).

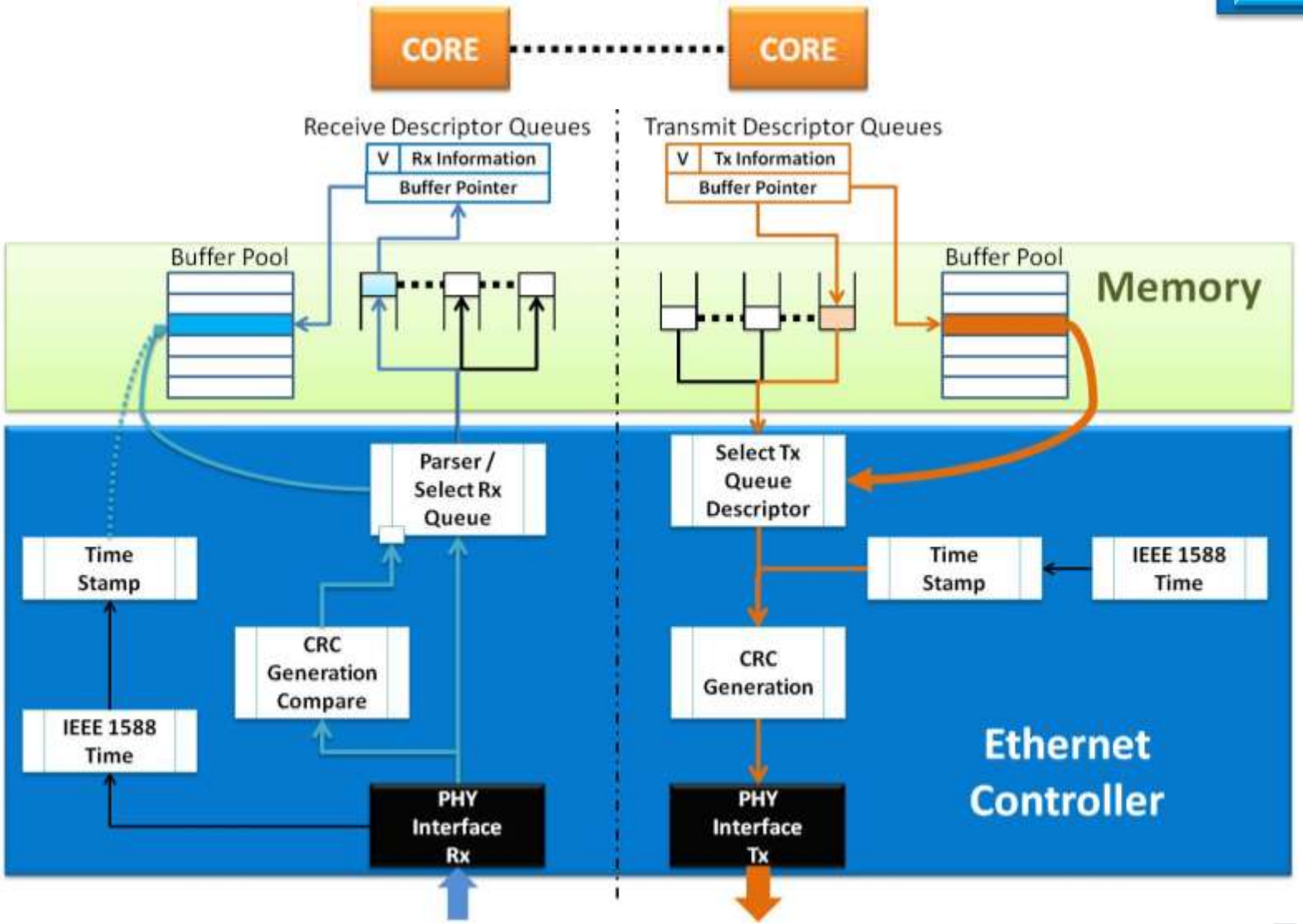
eTSEC falls into the Queue Assist category of Ethernet controllers.

There is also virtualization support in the latest versions.

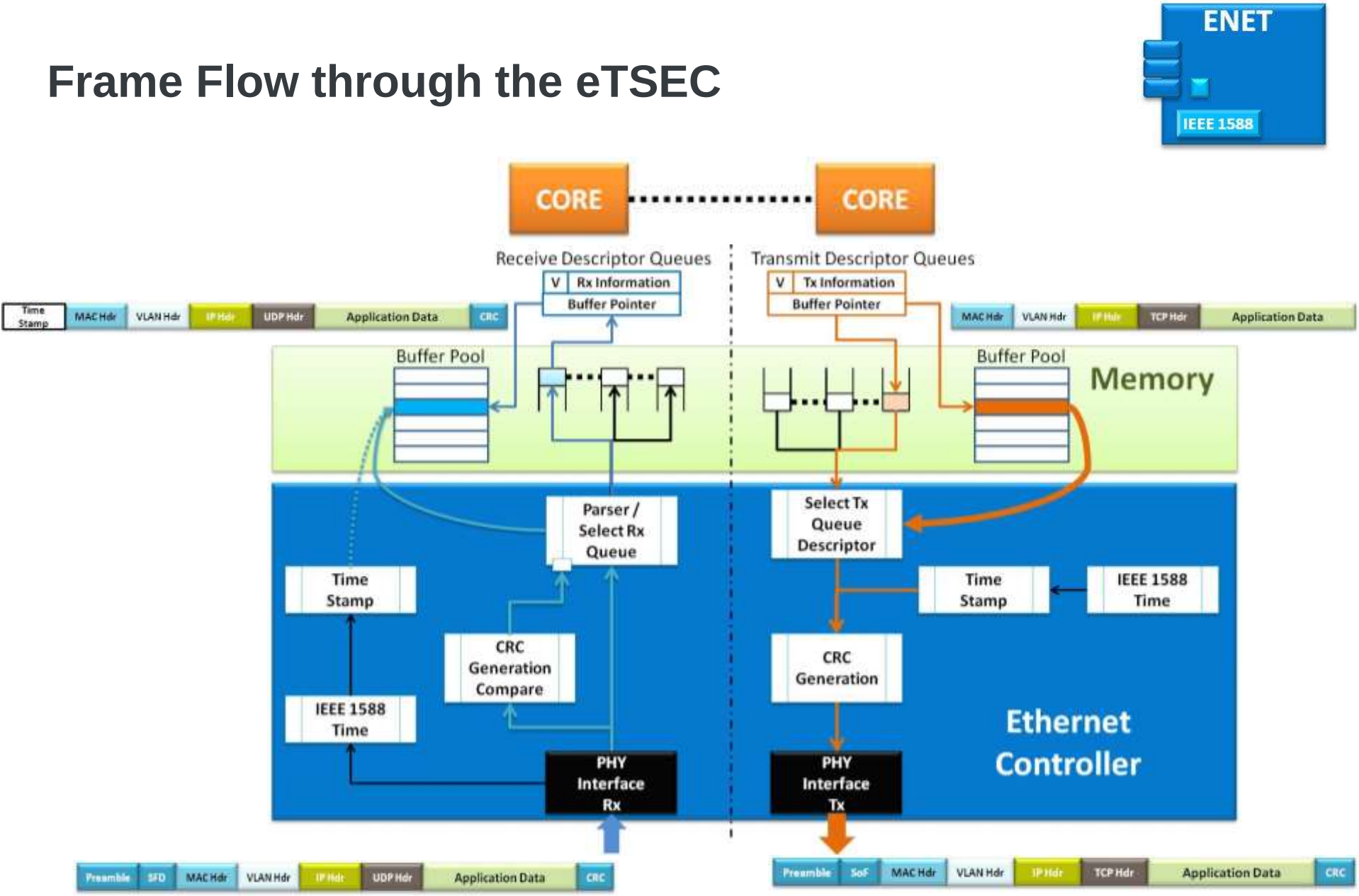


* Note: Not all interfaces may be supported on this device

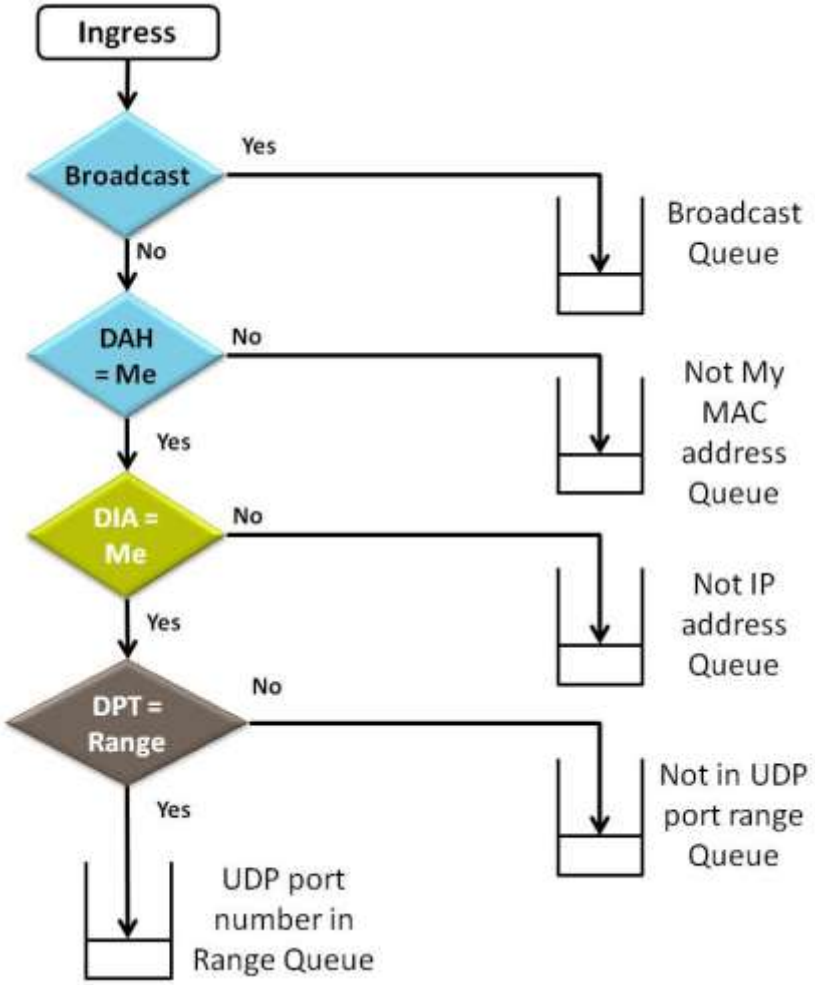
Simplified View of Ethernet Controller (eTSEC)



Frame Flow through the eTSEC



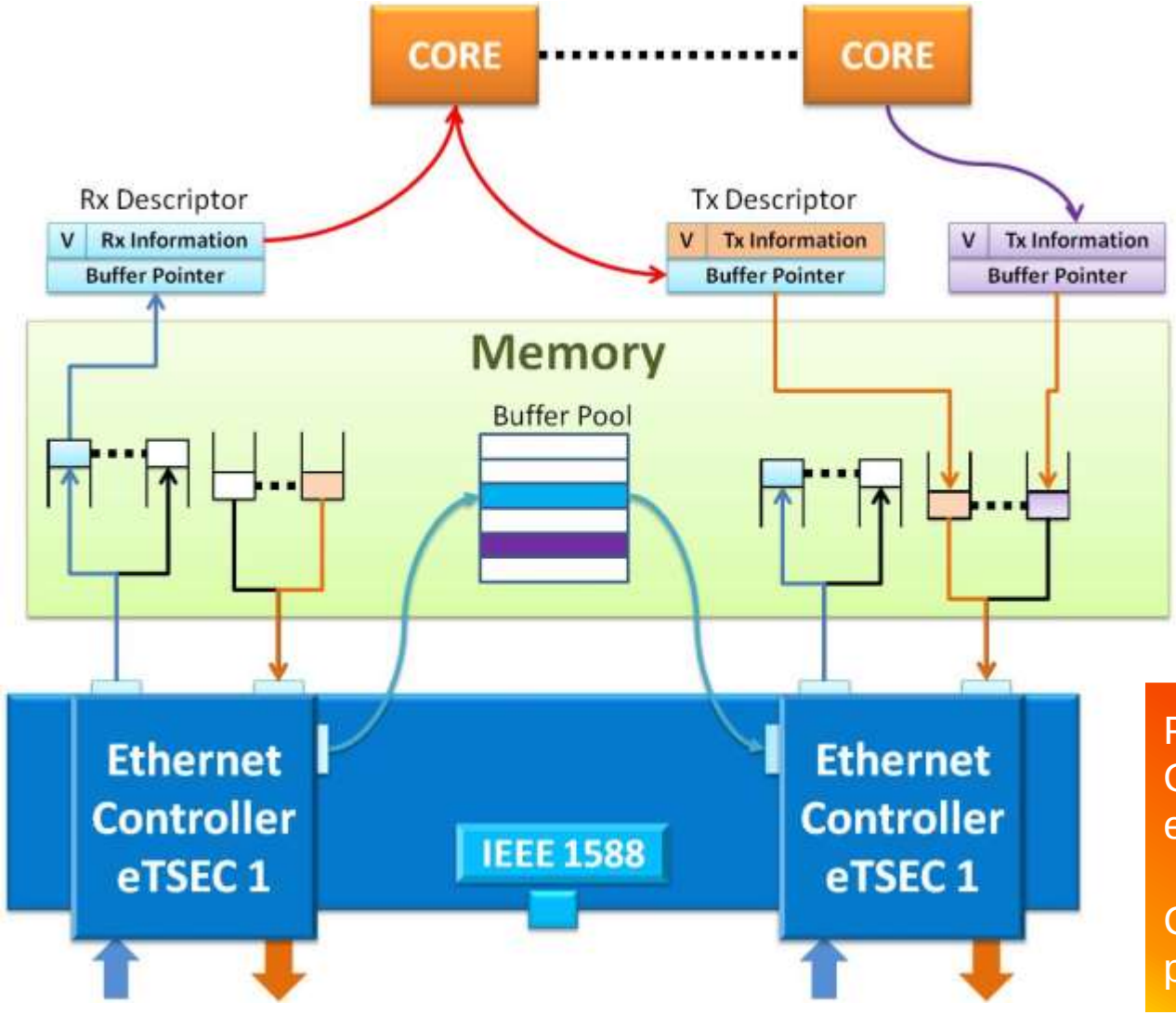
Simple Parsing Flow



Field	Description
MASK	Generic MASK
DAH	Destination MAC address most significant 24 bits
SAH	Source MAC address, most significant 24 bits
SAL	Source MAC address, least significant 24 bits
ETY	Ethertype of next layer protocol
VID	VLAN network identifier (as per IEEE Std 802.1Q)
PRI	VLAN user priority (as per IEEE Std 802.1p)
TOS	IPv4 header Type Of Service field or IPv6 Traffic Class field
L4P	Layer 4 protocol identifier as per published IANA specification
DIA	Destination IP address (IPv4 or IPv6 header) 32 most significant bits
SIA	Source IP address (IPv4 or IPv6 header) 32 most significant bits
DPT	Destination port number for TCP or UDP headers
SPT	Source port number for TCP or UDP headers

Parser also knows protocol header definitions and the user can instruct a decision tree

Simple Switch Application



Parser places in Switch Queue if not for this device, excluding broadcast frames

Core only needs to move pointer to Tx queue

This shows some of the capabilities of the eTSEC used in the QorIQ family of communications processors from Freescale.

Note the eTSEC Ethernet controller is just the junior member of the Ethernet controllers used in the QorIQ family, in both hardware acceleration and line rate performance.

For more information go to
http://www.freescale.com/QorIQ

Introducing The QorIQ LS2 Family

Breakthrough, software-defined approach to advance the world's new virtualized networks

New, high-performance architecture built with ease-of-use in mind

Groundbreaking, flexible architecture that abstracts hardware complexity and enables customers to focus their resources on innovation at the application level

Optimized for software-defined networking applications

Balanced integration of CPU performance with network I/O and C-programmable datapath acceleration that is right-sized (power/performance/cost) to deliver advanced SoC technology for the SDN era

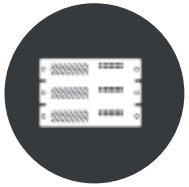
Extending the industry's broadest portfolio of 64-bit multicore SoCs

Built on the ARM® Cortex®-A57 architecture with integrated L2 switch enabling interconnect and peripherals to provide a complete system-on-chip solution

QorIQ LS2 Family

Key Features

SDN/NFV Switching



Data Center

Wireless Access

Unprecedented performance and ease of use for smarter, more capable networks

High performance cores with leading interconnect and memory bandwidth

- 8x ARM Cortex-A57 cores, 2.0GHz, 4MB L2 cache, w Neon SIMD
- 1MB L3 platform cache w/ECC
- 2x 64b DDR4 up to 2.4GT/s

A high performance datapath designed with software developers in mind

- New datapath hardware and abstracted acceleration that is called via standard Linux objects
- 40 Gbps Packet processing performance with 20Gbps acceleration (crypto, Pattern Match/RegEx, Data Compression)
- Management complex provides all init/setup/teardown tasks

Leading network I/O integration

- 8x1/10GbE + 8x1G, MACSec on up to 4x 1/10GbE
- Integrated L2 switching capability for cost savings
- 4 PCIe Gen3 controllers, 1 with SR-IOV support
- 2 x SATA 3.0, 2 x USB 3.0 with PHY

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4 new demos built on QorIQ LS2 processors:

- Performance Analysis Made Easy
- Leave the Packet Processing To Us
- Combining Ease of Use with Performance
- Tools for Every Step of Your Design

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