



FTF | **FREESCALE
TECHNOLOGY
FORUM 2015**

Migrating from **QorIQ P1 Series** to **QorIQ T1 Series** Processors

FTF-SNT-F1240

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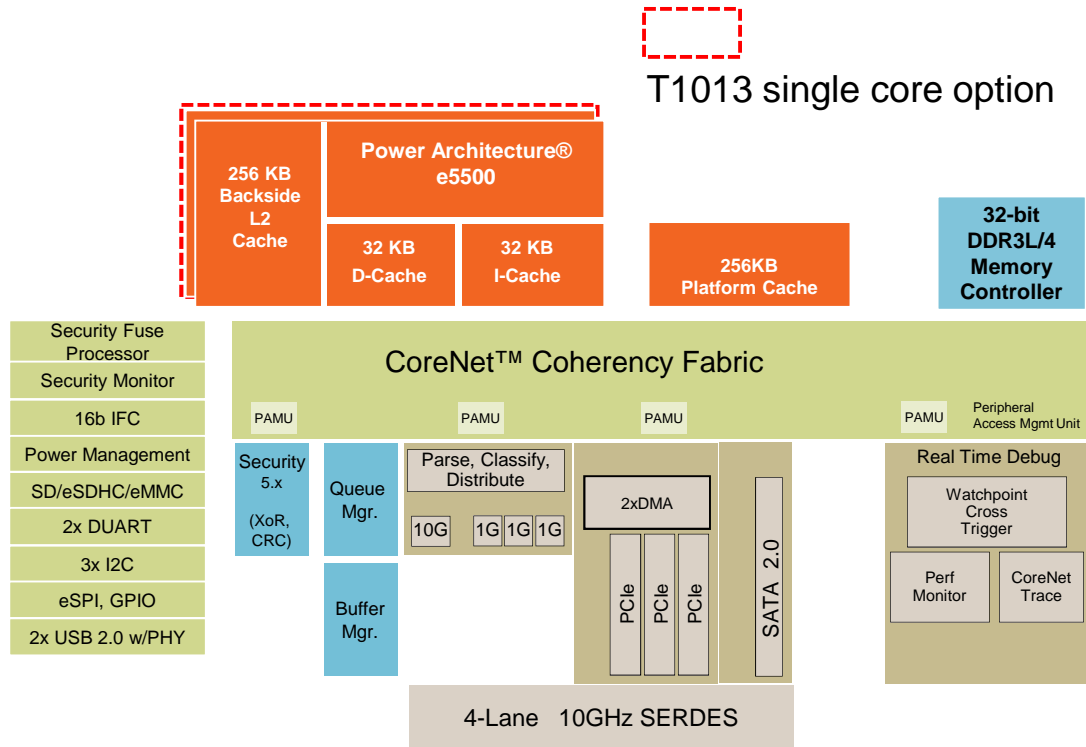


Agenda

- QorIQ T1023/24 Processors
- QorIQ 64-bit e5500 Core
- Reset Configuration Word (RCW)
- Data Path Acceleration Architecture (DPAA)
- QorIQ Linux SDK



QorIQ T1013/23 Processor



Device

- 28nm Process
- 525-pin package
- 19x19mm, 0.8mm pitch

Datapath Acceleration

- SEC- crypto acceleration
- Full MACsec/CAPWAP/DTLS offload for WLAN

Processor

- 1-2x e5500, 64b, up to 1.4GHz
- Each with 256 KB backside L2 cache
- 256KB Shared Platform Cache w/ECC
- Supports up to 64GB addressability (36 bit physical addressing)

Memory Subsystem

- 36b DDR3L/4 Controller up to 1600MT/s

CoreNet Switch Fabric

High Speed Serial IO

- 3x PCIe Gen2 Controllers
- 1x SATA 2.0, 3GB/s
- 2 USB 2.0 with PHY

Network IO

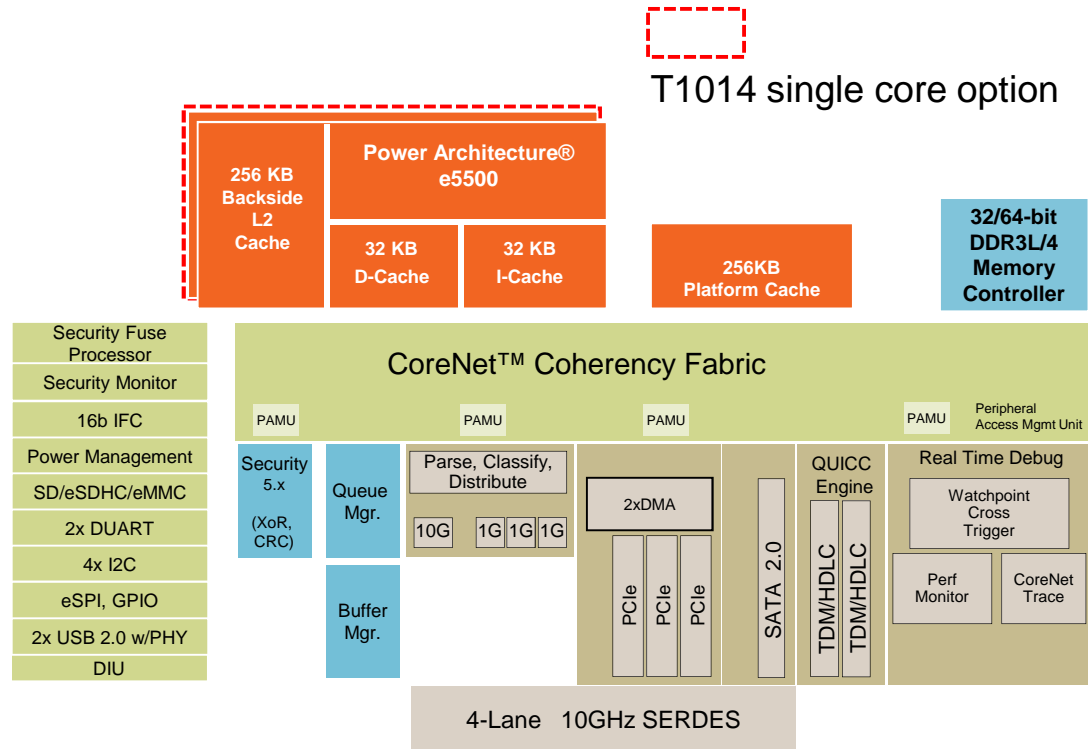
- FMan packet Parse/Classify/Distribute
- Lossless Flow Control, IEEE 1588
- 4x 10/100/1000 Ethernet Controllers
- 4x GbE or 3x GbE+ 1x 1/10GbE or QSGMII
- 10G KR supported for backplane
- MACsec on all ports

Green Energy Operation

- Fanless operation dual-core 1.4GHz



QorIQ T1014/24 Processor



Device

- 28nm Process
- 780-pin package
- 23x23mm, 0.8mm pitch

Datapath Acceleration

- SEC- crypto acceleration
- Full MACsec/CAPWAP/DTLS offload for WLAN

Processor

- 1-2x e5500, 64b, up to 1.4GHz
- Each with 256 KB backside L2 cache
- 256KB Shared Platform Cache w/ECC
- Supports up to 64GB addressability (36 bit physical addressing)

Memory Subsystem

- 36/72b DDR3L/4 Controller up to 1600MT/s

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- 4x 10/100/1000 Ethernet Controllers
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 - 10G KR supported for backplane
- MACsec on all ports
- QUICC Engine
 - HDLC, 2x TDM, Profibus, Ethercat

Green Energy Operation

- Fanless operation dual-core 1.2GHz
- Packet lossless deep sleep
 - Programmable wake-on-packet
 - Wake-on-timer/GPIO/USB/IRQ



QorIQ T1040 Processor

Processor

- 4x e5500, 64b, up to 1.4GHz
- Each with 256KB backside L2 cache
- 256KB Shared Platform Cache w/ECC
- Supports up to 64GB addressability (36 bit physical addressing)

Memory Subsystem

- 36/72b DDR3L/4 Controller up to 1600MT/s

Corenet Switch Fabric

High Speed Serial IO

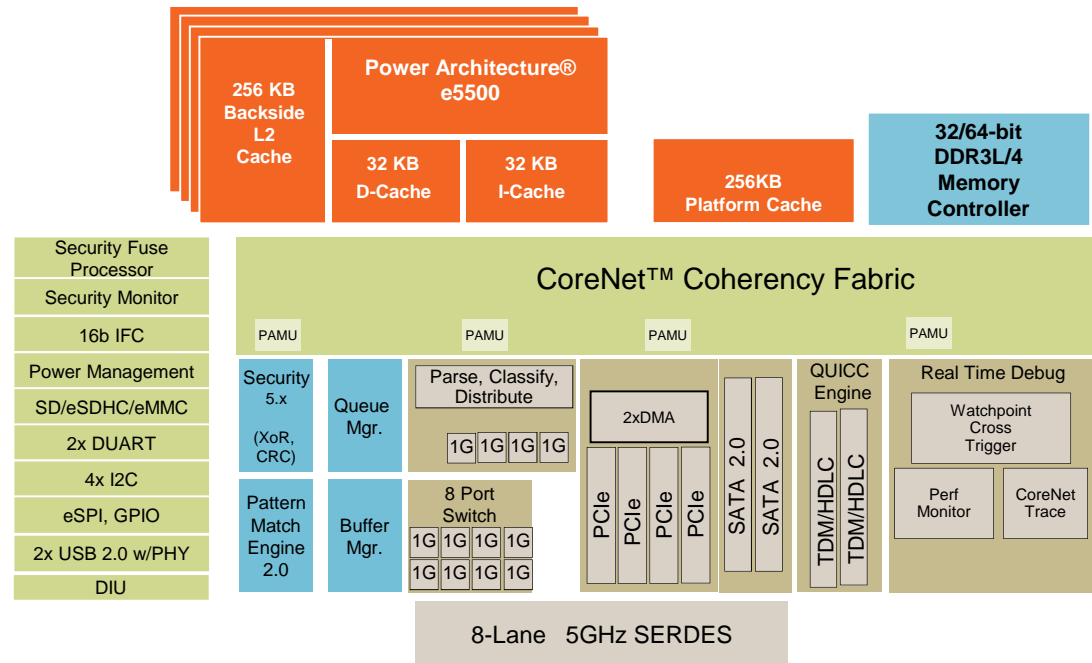
- 4x PCIe Gen2 Controllers
- 2x SATA 2.0, 3Gb/s
- 2x USB 2.0 with PHY

Network IO

- FMan packet Parse/Classify/Distribute
- Lossless Flow Control, IEEE 1588
- Up to 4x 10/100/1000 Ethernet Controllers
- 8-Port Gigabit Ethernet Switch
- QUICC Engine
 - HDLC, 2x TDM

Green Energy Operation

- Fanless operation quad-core 1.2GHz
- Packet lossless deep sleep
 - Programmable wake-on-packet
 - Wake-on-timer/GPIO/USB/IRQ



Device

- 28nm Process
- 780-pin package
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Power Targets

- Enable Convection cooled system design

Datapath Acceleration

- SEC- crypto acceleration
- PME- Reg-ex Pattern Matcher



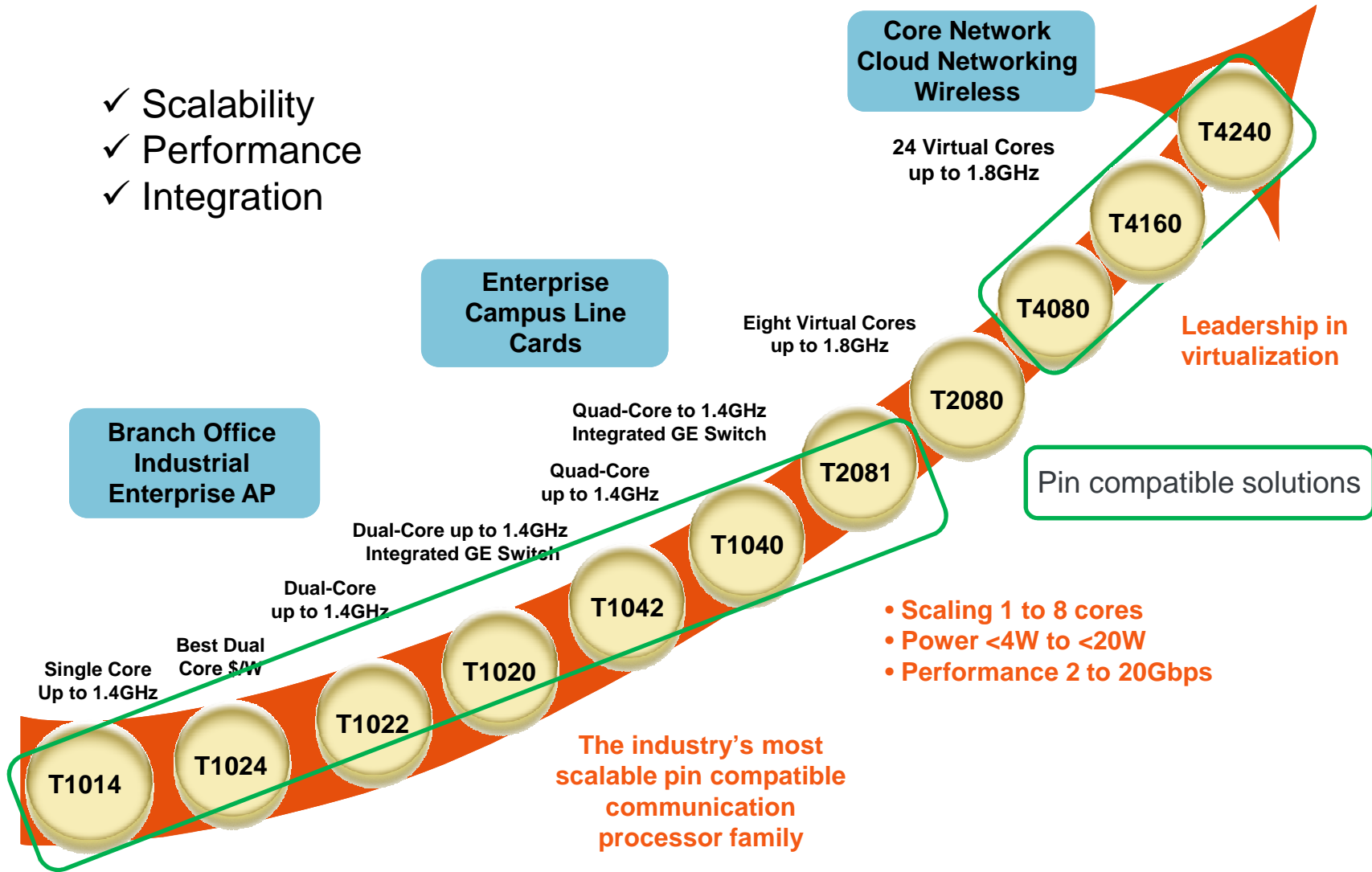
QorIQ P1, P2 and T1 Families – Feature Set Comparison

P102X vs T10XX Comparisons									
	P1020	P1022	P2020	T1023	T1013	T1024	T1014	T1022/20	T1042/40
Core	2x e500v2	2x e500v2	2x e500v2	2x e5500	1x e5500	2x e5500	2x e5500	2x e5500	4x e5500
Power ISA	32b	32b	32b	64b	64b	64b	64b	64b	64b
Max Coremarks	4,960	7,440	8,265	10,360	5,180	10,360	5,180	10,360	20,720
fmax MHz	800	1200	1333	1400	1400	1400	1400	1400	1400
L2 BS cache	-	-	-	256KB BS	256KB BS	256KB BS	256KB BS	256KB BS	256KB BS
Platform cache	256KB	256KB	256KB	256KB	256KB	256KB	256KB	256KB	256KB
DDR Type	2/3	2/3	2/3	3L/4	3L/4	3L/4	3L/4	3L/4	3L/4
DDR speed	to 1333MTs	to 1600MTs	to 1600MTs	to 1600MTs	to 1600MTs	to 1600MTs	to 1600MTs	to 1600MTs	to 1600MTs
DDR width	36b	36b/72b	36b/72b	36b	36b	36b/72b	36b/72b	36b/72b	36b/72b
SERDES	4	6	4	4	4	4	4	8	8
PCIe type	v1	v1	v1	v2	v2	v2	v2	v2	v2
PCIe lanes	2x 1	3x 1	2x 1	3x 1	3x 1	3x 1	3x 1	4x 1	4x 1
GbE	3	2	up to 3	up to 4	up to 4	up to 4	up to 4	up to 5	up to 5
2.5G SERDES	No	No	No	Yes	Yes	Yes	Yes	Yes	Yes
QSGMII	No	No	No	Yes	Yes	Yes	Yes	Yes	Yes
10GbE I/O	-	-	-	1	1	1	1	-	-
Switch option	-	-	-	-	-	-	-	(T1020 only) 8 port	(T1040 only) 8 port
SRIO	-	-	x2	-	-	-	-	-	-
MACSEC	-	-	-	all ports	all ports	all ports	all ports	all ports	all ports
HW offload	-	-	-	DPAA v3	DPAA v4	DPAA v3	DPAA v3	DPAA v3	DPAA v4
Crypto	SEC 3.x	SEC 3.x	SEC 3.x	SEC 5.x	SEC 5.x	SEC 5.x	SEC 5.x	SEC 5.x	SEC 5.x
PME	-	-	-	-	-	-	-	Yes	Yes
TDM/HDLC	Yes	-	-	-	-	Yes	Yes	Yes	Yes
SATA	-	1.0 x 2	1.0 x 2	2.0 x1	2.0 x1	2.0 x1	2.0 x1	2.0 x2	2.0 x2
USB	2.0 x2	2.0 x2	2.0 x2	2.0 x2 w Phy	2.0 x2 w Phy	2.0 x2 w Phy	2.0 x2 w Phy	2.0 x2 w Phy	2.0 x2 w Phy
Deep Sleep	-	Yes	Yes	-	-	Yes	Yes	Yes	Yes
Auto Response	-	-	-	-	-	Yes	Yes	Yes	Yes
DIU	-	Yes	-	-	-	Yes	Yes	Yes	Yes
1 clock source	-	-	-	Yes	Yes	Yes	Yes	Yes	Yes
Fwd perf	~1Gbps	~1Gbps	~1Gbps	≥ 2.5Gbps	≥ 2.5Gbps	≥ 2.5Gbps	≥ 2.5Gbps	≥ 2.5Gbps	≥ 2.5Gbps
Package	31x31 PBGA	31x31 PBGA	31x31 PBGA	19x19 FCBGA	19x19 FCBGA	23x23 FCBGA	23x23 FCBGA	23x23 FCBGA	23x23 FCBGA
W (Typ)	~3-4W	~5-6W	~7-9W	~3-5W	~3-4W	~3-5W	~3-4W	~5-8W	~6-10W
Pin Compatible	No	No	No	Yes			Yes		



Continuing Power Architecture Innovation

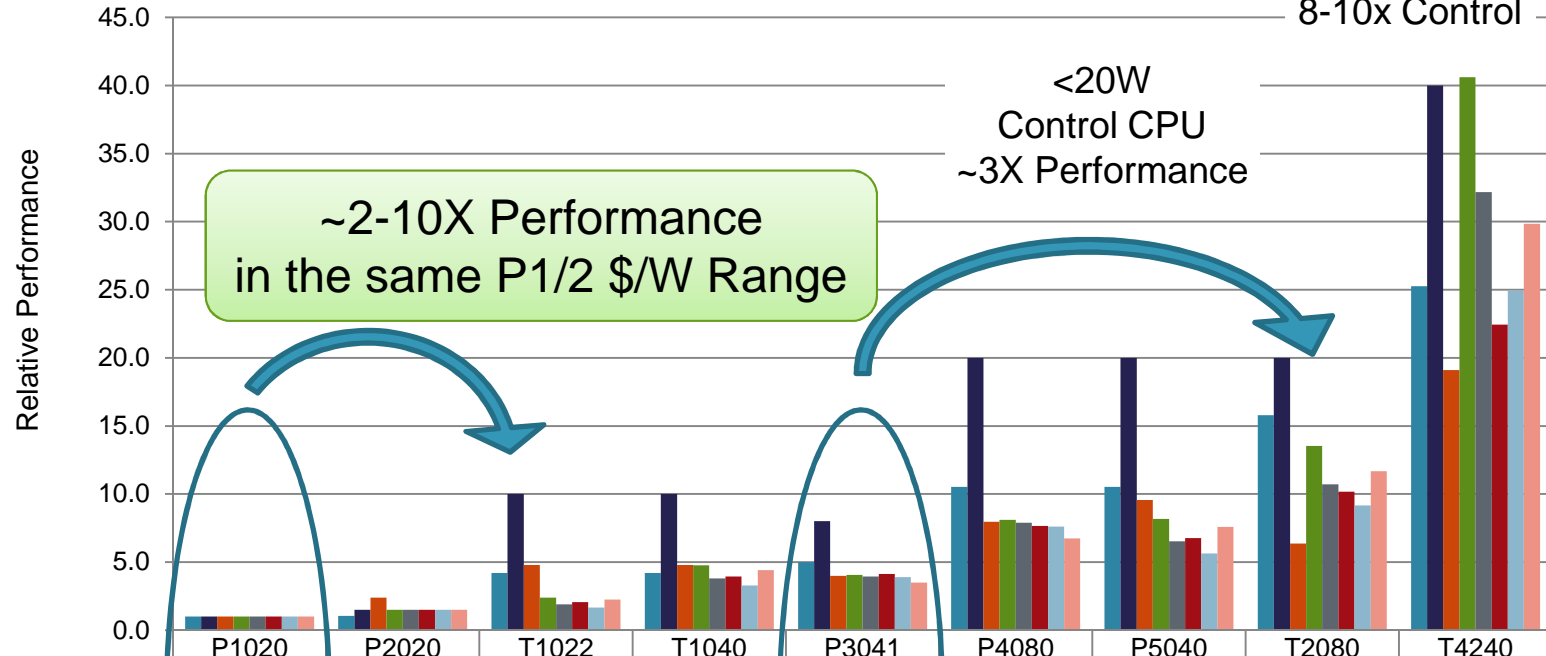
- ✓ Scalability
- ✓ Performance
- ✓ Integration



Performance Upgrade – QorIQ P Series to T Series SoCs

Aggregate Multi-core SoC Performance

4-5x Data
8-10x Control



	P1020	P2020	T1022	T1040	P3041	P4080	P5040	T2080	T4240
Ipfwd Gbps (IMIX)	1.0	1.1	4.2	4.2	5.0	10.5	10.5	15.8	25.3
IPSec Gbps (IMIX)	1.0	1.5	10.0	10.0	8.0	20.0	20.0	20.0	40.0
DDR bandwidth (Gbyte/s)	1.0	2.4	4.8	4.8	4.0	8.0	9.6	6.4	19.1
DMIPS	1.0	1.5	2.4	4.8	4.1	8.1	8.2	13.5	40.6
Coremark	1.0	1.5	1.9	3.8	3.9	7.9	6.5	10.7	32.2
EEMBCv2-IPMark	1.0	1.5	2.1	4.0	4.1	7.7	6.8	10.2	22.4
EEMBCv2-TCPMark	1.0	1.5	1.7	3.3	3.9	7.6	5.6	9.1	24.9
EEMBCv2-DENMARK	1.0	1.5	2.3	4.4	3.5	6.7	7.6	11.7	29.8



e5500 Core



QorIQ 64-bit e5500 Core

The e5500 core is a low-power implementation of the resources for embedded processors defined by the Power ISA™

- **64-bit Core Architecture** for higher performance, computational intensive applications
 - 64-bit ISA support (Power Architecture v2.06 compliant)
 - Increased addressable memory space
 - Supports up to 2 GHz CPU frequency
- **High-Performance Classic Floating Point Unit (FPU)** for Industrial applications
 - Supports IEEE Std. 754™ FPU Double Precision Floating Point
- **Hybrid 32-bit mode** to support legacy software and transition to 64-bit architecture
 - Register settings allow users to utilize 32-bit mode or 64-bit mode, easing transition to 64-bit architecture

Leveraging the e5500

- Based on the e500mc architecture with 64-bit ISA
- Core frequency up to 2GHz
- Up to 64GB addressable memory space
- Supports up to 512KB backside L2 cache
- High performance classic FPU

Advantages of e5500

Features	Benefits
64-bit ISA Support	<ul style="list-style-type: none">• Provides the ability for the core to utilize twice the amount of data per CPU cycle (64-bit vs 32-bit), which increase performance for computational-intensive applications with large data sets• Increased addressable memory space makes programming easier as it allows a single process to have a larger address space, and enables more complex applications that need more memory space.
7-stage Pipeline with Out-of-Order Execution	<ul style="list-style-type: none">• Allows the core to continue to do productive work in the event of a stalled instruction or a wrong branch prediction.
Floating Point Unit	<ul style="list-style-type: none">• Classic double precision floating point supported which allows for faster, more accurate computation
Backside L2 Cache	<ul style="list-style-type: none">• Provides a lower latency cache with higher bandwidth to the core, enabling higher performance, and Reduces the transactions on the shared interconnect and DDR memory
Up to 2GHz CPU Frequency	<ul style="list-style-type: none">• Higher frequency provides additional performance for 32-bit & 64-bit applications. Applications with complex numerical algorithms will particularly see a performance improvement due to 64-bit and higher frequency.

e5500 vs e500 Performance Deltas

New e5500 Features

- Link stack branch predictor
- Faster integer divider
 - 3 bits of result per cycle vs. 2
- Instructions
 - SPR instructions handled in CFX improves SFX instruction issue
- cmpb instruction
 - finds string differences quickly;
- 64-bit load/store instructions for strcmp()
- Dhrystone Results:

Backside Cache Advantage

- e5500 Backside L2 cache can significantly improve performance
 - L2 cache operates at CPU frequency rather than platform frequency
 - Much lower L2 latency

Core	Dhrystone DMIPS/MHz
e500v2	2.4
e5500	3.0

Core	L2 Latency
e500v2 (Frontside L2)	23 core cycles
e5500 (Backside L2)	12 core cycles

Reset Configuration Word (RCW)



Reset Configuration Word (RCW)

- An external memory interface is used to import a subset of the reset configuration information from a memory device during reset.
 - This information is called reset configuration word (RCW) data.
- The pre-boot loader (PBL) loads RCW data from a non-volatile memory device interface, as specified by the RCW source configuration inputs.
 - This approach does not completely remove the necessity for at least a few power-on reset (POR) configuration signals.
- The logic involved is clocked directly from SYSCLK since RCW importing takes place before on-chip PLLs are configured.
- The RCW is 512 bits long in order to contain all necessary configuration information for the chip. RCW data is read from external memory and written to the RCW status registers.

Reset Configuration Pins (SoC Specific)

- RCW source
 - `cfg_rcw_src[0:8]`
 - Select the source for RCW data: NOR Flash, SD/MCC, I2C, SPI, NAND Flash
- General purpose input
 - `cfg_gpinput[0:7]`
 - Available for application-specific use
- IFC external transceiver enable polarity select
 - `cfg_ifc_tc`
- DRAM type select
 - `cfg_dram_type`
 - DDR3L technology (1.35V) or DDR4 technology (1.2V)
- "Single Oscillator Source" clock select
 - `cfg_eng_use0`



Pre-Boot Loader

- Simplifies boot operations, replacing pin strapping resistors with configuration data loaded from nonvolatile memory
- Loads PBL image from chosen source
 - Loads RCW from external memory device
 - Loads pre-boot initialization (PBI) commands - optional
- Uses the configuration data to initialize other system logic and to copy data from low speed memory interfaces (I2C, IFC, eSPI, and SD/eSDHC/eMMC) to configuration registers or memory
- Releases CPU 0 from reset, allowing the boot processes to begin

PBI Commands

- Allows configuration of various interfaces before allowing cores to boot
- Similar to boot sequencer on previous devices
- Write to CCSR space (ACS = 0)
- Write to alternate space such as DDR or CPC SRAM (ACS=1)
- Commands
 - Flush – Ensure previous write has taken effect
 - CRC Check – performs CRC check on all data since last CRC check
 - Jump – provide next address to jump to
 - Wait – can't poll registers but can set a number of sysclks to wait

QCVS Configuration and Validation Suite (QCVS): PBL Configuration Tool

- Assists the user in creating a complete PBL image
- Supports both the PBL RCW and Pre-Boot Initialization (PBI) commands
- Provides a method for decoding previously generated PBL images
- Performs basic data integrity checks
- <http://www.freescale.com/qcs>

QCVS: PBL Configuration Tool

The screenshot shows the QorIQ Configuration - Processor Expert Software interface. The 'Component Inspector - PBL' window is open, and the 'Import' button is circled in red. The 'SerDes Protocol Selection' section is also circled in red. The main configuration area displays a table for SRDS_PRTCL_S1 [128-136].

SRDS_PRTCL_S1	SERDES				RGMII EC1, EC2
	A	B	C	D	
00 (0b0000000000)	Used by hard-coded value (T1024)				
40 (0b0010000000)	PCIe1 (2.5)				2 RGMII (FMAN MAC4, MAC3)
95 (0b010010101)	XFI (MAC1)	PCIe3 (5/2.5)	PCIe2 (5/2.5)	PCIe1 (5/2.5)	2 RGMII (FMAN MAC4, MAC3)
D5 (0b011010101)	qs.m1-4	PCIe3 (5/2.5)	PCIe2 (5/2.5)	PCIe1 (5/2.5)	0 RGMII
D6 (0b011010110)	qs.m1-4	PCIe3 (5/2.5)	PCIe2 (5/2.5)	SATA (3/1.5)	0 RGMII
99 (0b0100110001)	XFI (MAC1)	PCIe3 (5/2.5)	sg.m2 (1G)	PCIe1 (5/2.5)	2 RGMII (FMAN MAC4, MAC3)
6B (0b001101011)	PCIe1 (5/2.5)	sg.m3 (1G)	sg.m2 (1G)	sg.m1 (1G)	1 RGMII (FMAN MAC4). No EC2
5B (0b010110111)	PCIe1 (5/2.5)	PCIe3 (5/2.5)	sg.m2 (1G)	sg.m1 (1G)	2 RGMII (FMAN MAC4, MAC3)
6A (0b001101010)	PCIe1 (5/2.5)	sg.m3 (1G)	sg.m2 (1G)	SATA (3/1.5)	1 RGMII (FMAN MAC4). No EC2
5A (0b001011010)	PCIe1 (5/2.5)	PCIe3 (5/2.5)	sg.m2 (1G)	SATA (3/1.5)	2 RGMII (FMAN MAC4, MAC3)
46 (0b001000110)	PCIe1 (5/2.5)		PCIe2 (5/2.5)	SATA (3/1.5)	2 RGMII (FMAN MAC4, MAC3)
119 (0b100110101)	Aurora (5/2.5)	PCIe3 (5/2.5)	sg.m2 (2.5G)	PCIe1 (5/2.5)	2 RGMII (FMAN MAC4, MAC3)
77 (0b001110111)	PCIe1 (5/2.5)	sg.m3 (2.5G)	PCIe2 (5/2.5)	sg.m1 (1G)	1 RGMII (FMAN MAC4). No EC2
135 (0b100110101)	Aurora (5/2.5)	sg.m3 (2.5G)	PCIe2 (5/2.5)	PCIe1 (5/2.5)	1 RGMII (FMAN MAC4). No EC2

SerDes Protocol Select - SerDes 1
 Bits 128-135
 For additional information see description of the SRDS_PRTCL_S1 field in device documentation.
 This item modifies SRDS_PRTCL_S1[31:23] bit field in the RCWSR5 register.



QCVS: PBL Configuration Tool (Con't)

QorIQ Configuration - Processor Expert Software

File Edit Navigate Search Project Processor Expert Run Window Help

Project Explorer

- PBL_T1024
 - Documentation
 - Generated_Code** (circled in red)
 - PBL.pbl
 - Sources
 - ProcessorExpert.pe

Component Inspector - PBL

Components Library

Basic Advanced

Properties Import

Name	Value	Details
▶ Group A Pin Configuratio		
▶ Group B Pin Configuratio		
▶ SoC-Specific Configuratio		
SDHC [410-417]	0b00 - SDHC_CD, SDHC_WP	
EC1 [418-419]	0b00 - Frame Manager MAC1 RGMII	
1588_EC2 [420-421]	0b10 - EC2_RXD[0:1], EC2_RX_CLK	
I2C4 [422-425]	0b00 - IIC4_SCL, IIC4_SDA	
QE_TDMA [424-426]	0b000 - TDMA	
QE_TDMB [427-429]	0b000 - TDMB	
DVDD_VSEL [430-431]	0b00 - 1.8V	
L1VDD_VSEL [432-433]	0b00 - 1.8V	
LVDD_VSEL [434-435]	0b00 - 1.8V	
CVDD_VSEL [436-437]	0b00 - 1.8V	
EVDD_VSEL [438-439]	0b00 - 1.8V	
IRQ1_EXT_SEL [440]	0b0 - Base functionality selected	
HDLC1_MODE [441]	0b0 - TXD in normal mode	
HDLC2_MODE [442]	0b0 - TXD in normal mode	
MDIO_MDC1 [443]	0b0 - MDIO/MDC1	
GPIO [444-445]	0b00 - GPIO3[24:28]	
IRQ1_EXT [446]	0b0 - USB_CLK	
IIC2_EXT0_1 [447]	0b0 - Default functionality on IIC2_...	
▶ PLL and Clocking Configuratio		

Problems

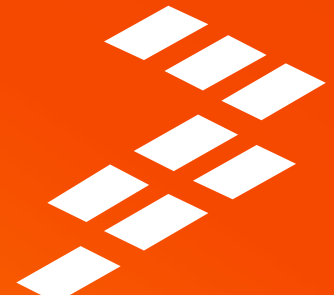
0 errors, 2 warnings, 0 others

Description	Resource	Path	Location	Type
▶ Warnings (2 items)				

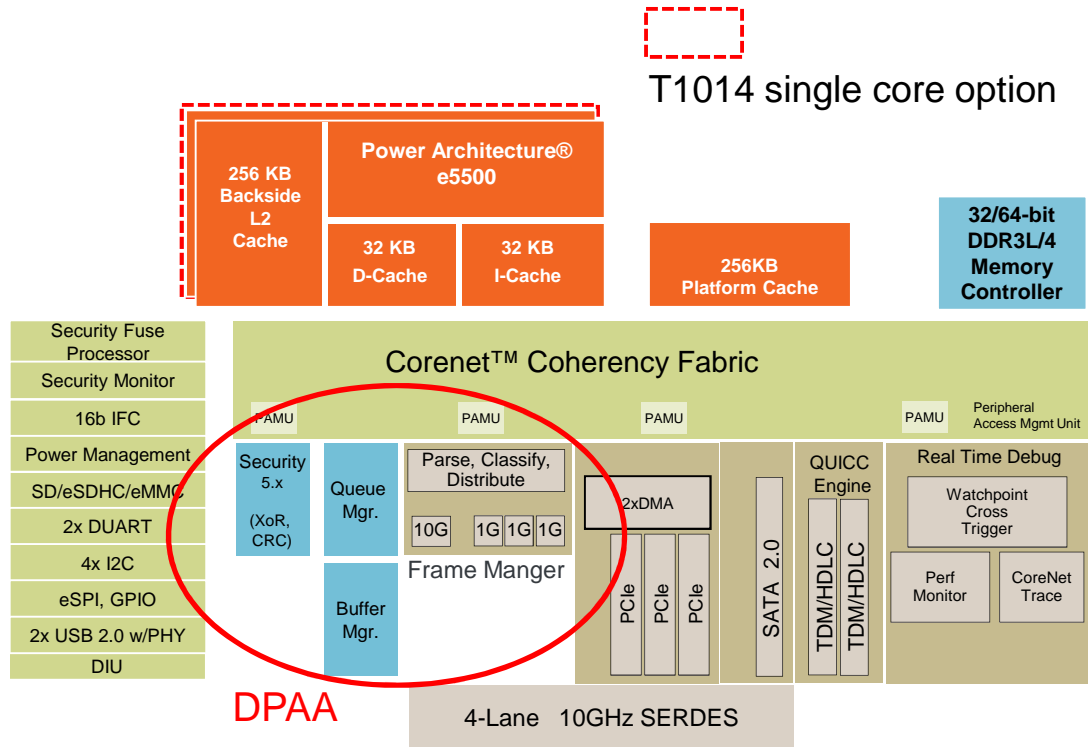
PBL_T1024/ProcessorExpert.pe



Data Path Acceleration Architecture (DPAA)



QorIQ T1014/24 Processor



Datapath Acceleration Architecture (DPAA)

- Frame Manager (FMan)
- Queue Manager (QMan)
- Buffer Manager (BMan)
- SEC- crypto acceleration

Processor

- 1-2x e5500, 64b, up to 1.4GHz
- Each with 256 KB backside L2 cache
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- Supports up to 64GB addressability (36 bit physical addressing)

Memory Subsystem

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- 4x 10/100/1000 Ethernet Controllers
- 4x GbE or 3x GbE+ 1x 1/10GbE or QSGMII
- 10G KR supported for backplane
- MACsec on all ports
- QUICC Engine
 - HDLC, 2x TDM, Profibus, Ethercat

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- Packet lossless deep sleep
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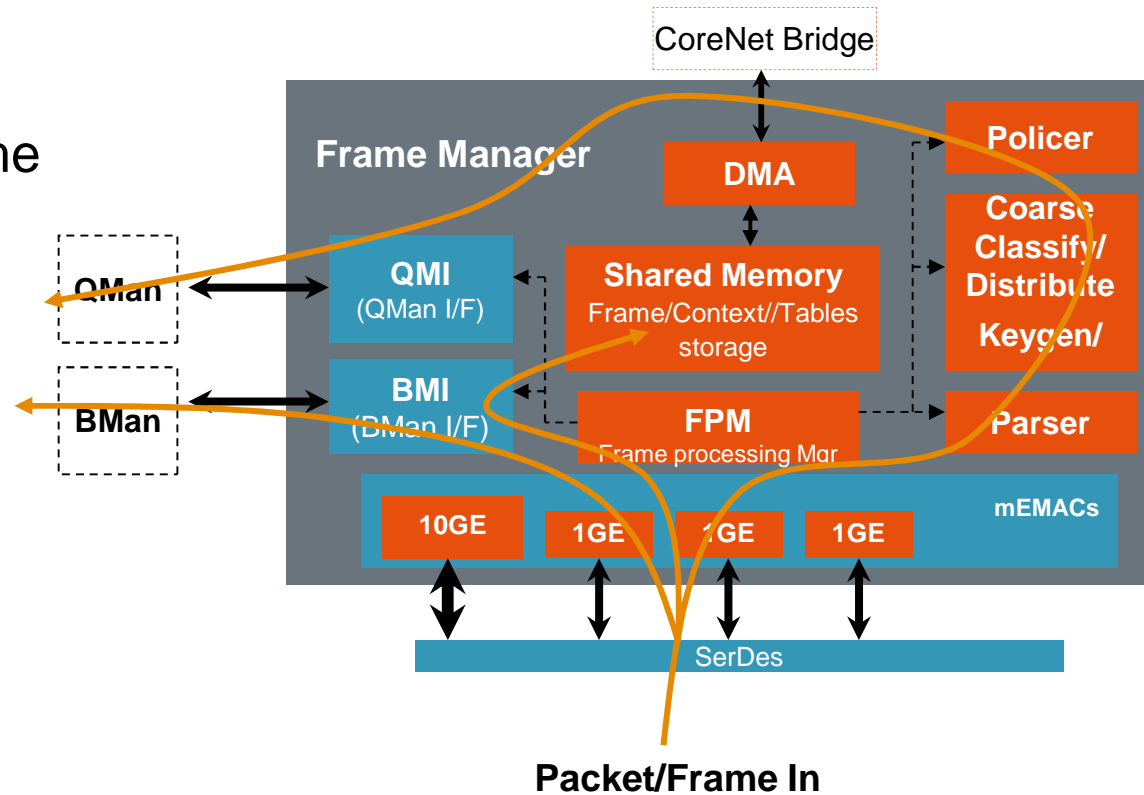
Multirate Ethernet Media Access Controller (mEMAC)

- IEEE 802.3ae (MAC layer and reconciliation sub-layer)
- IEEE802.3az (EEE (Energy Efficient Ethernet))
- CRC-32 checking with optional forwarding of the FCS
- CRC-32 generation and append on transmit
- Ethernet pause frame (802.3 Annex 31A) termination
- Priority Flow Control (PFC) frame support allowing 8 classes for higher layer congestion management
- Magic packet detection
- Support for VLAN tagged frames according to IEEE 802.1Q and double VLAN Tags (Stacked VLANs)
- Statistic counters
- Deficit Idle Counter (DIC) for optimized performance with minimum IPG for LAN applications
- IEEE 1588 support



Frame Manager (FMan)

- FMan supports a flexible pipeline of packet processing elements
- Frame data and per frame context is stored in internal memory while frame is processed
- Frame Processor Manager (FPM) “schedules” frames for processing by different elements to create appropriate pipeline
- Default pipeline configured for each port



Frame Manager: Parse-Classify-Distribute (PCD)

- Header Parsing
 - L2/L3/L4 parse and validate (checksum)
 - User defined protocols supported
- Distribution
 - Hash based queue selection for load spreading
 - Form “key” from selected header fields
 - Key is input to hash function
 - Frames from same flow will placed in same queue
- Classification
 - Exact match
 - Table lookup using selected header field
 - Place frames in queues based on results of table lookup
- Policing
 - Color aware dual rate, 3 color
 - RFC4115 and RFC2968
- Configure Frame Manager for PCD using Frame Manager Configuration (FMC) Tool
- Import FMC input files to Frame Distributor Wizard Tool for “viewing” and editing



Default PCD Configuration: Flow 1

Frame Distributor Wizard

Hashing: Flows definition

Select fields for hashing flows

Wizard Traffic1 - frame view Traffic2 - frame view

Frame view (read-only)

Layer 4: Transport
udp segment

sport 2B	dport 2B	len 2B	crc 2B	payload
-------------	-------------	-----------	-----------	---------

Layer 3: Network
ipv4 packet

ver 1B	hlen 1B	tos 1B	tlen 2B	identification 2B	ttl 1B	nextp 1B	hchecksum 2B	src 4B	dst 4B	payload
-----------	------------	-----------	------------	----------------------	-----------	-------------	-----------------	-----------	-----------	---------

Layer 2: Data link
ethernet frame

dst 6B	src 6B	type 2B	payload
-----------	-----------	------------	---------

Legend:

- Field not used in a Key
- Field used in Hash Key
- Field used in Lookup Key
- Field used in Hash & Lookup Key

Default PCD Configuration: Flow 2

Frame Distributor Wizard

Hashing: Flows definition

Select fields for hashing flows

Wizard Traffic1 - frame view Traffic2 - frame view

Frame view (read-only)

Layer 4: Transport tcp segment

sport	dport	seq	ack	hlen	res	flags	win	crc	urg	payload
2B	2B	4B	4B	2B	2B	2B	2B	2B	2B	

Layer 3: Network ipv4 packet

ver	hlen	tos	tlen	identification	ttl	nextp	hchecksum	src	dst	payload
1B	1B	1B	2B	2B	1B	1B	2B	4B	4B	

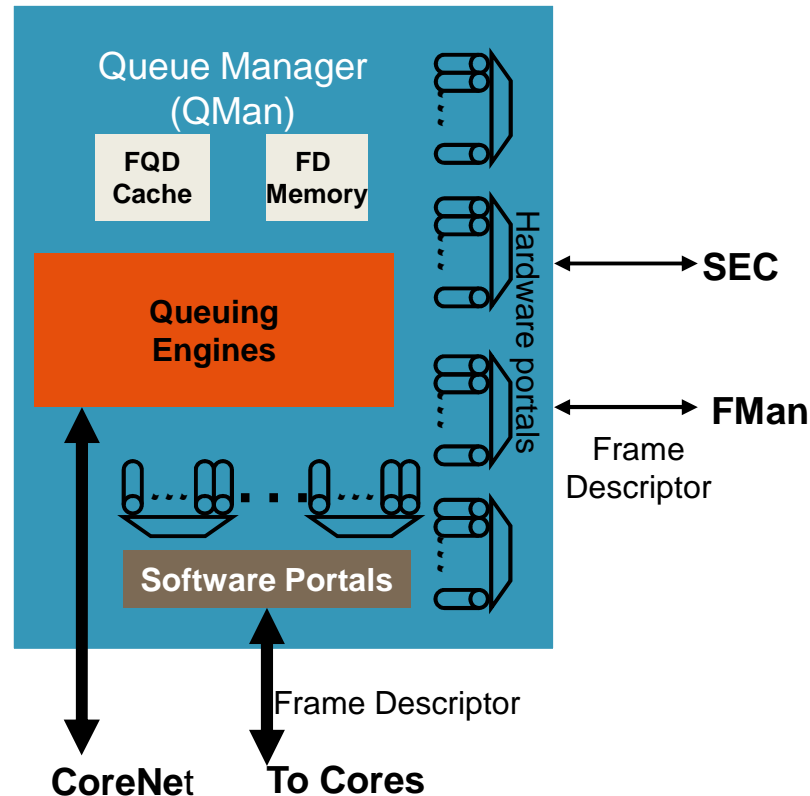
Layer 2: Data link ethernet frame

dst	src	type	payload
6B	6B	2B	

Legend:

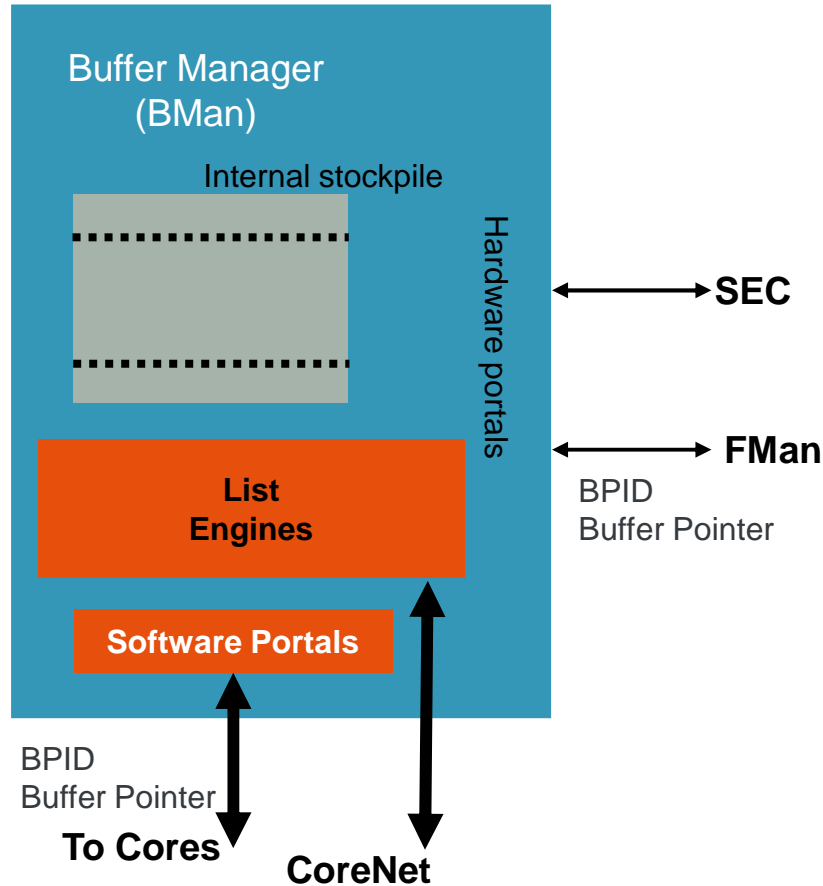
- Field not used in a Key
- Field used in Hash Key
- Field used in Lookup Key
- Field used in Hash & Lookup Key

Queue Manager (QMan)



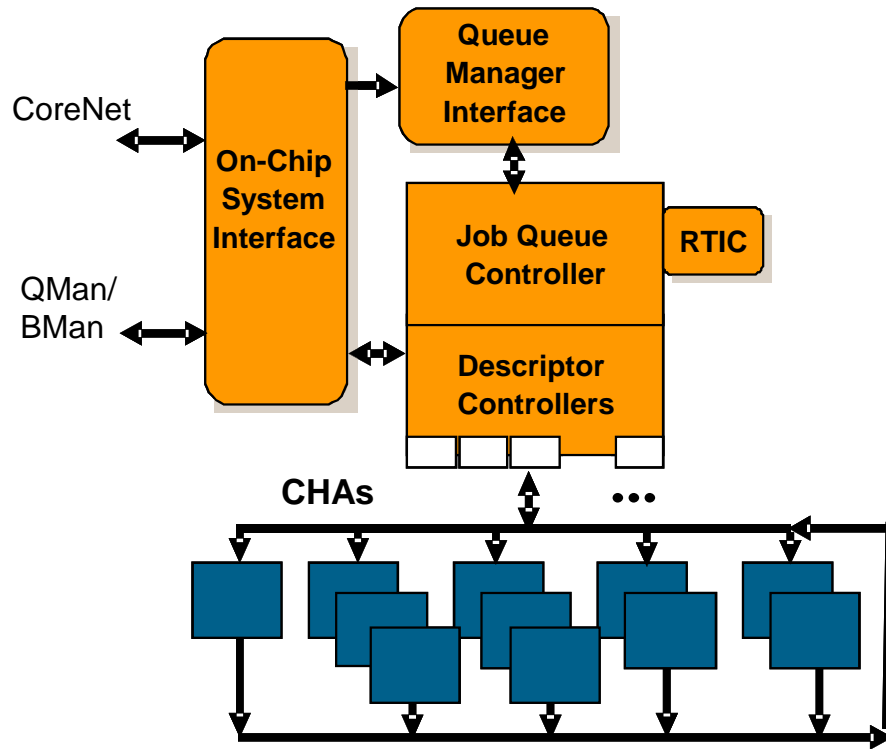
- Low latency, prioritized queuing of descriptors between cores, network I/O, and accelerators
- Lockless shared queues for load spreading and device “virtualization”
- Order restoration as well as order preservation through queue affinity
- Active queue management (WRED)
- Optimized core interface which can pre-position data/context/descriptors in core’s cache
- Delivery of per-queue accelerator specific commands and context information to offload accelerators along with dequeued descriptors

Buffer Manager (BMan)



- BMan manages 64 pools of buffer pointers
 - All buffers in a pool are expected to have “like” characteristics (e.g., same buffer size)
 - BMan places no restrictions on these characteristics
- Hardware (and software) acquire and release of buffer pointers from/to pools
 - BMan is primarily intended to reduce the buffer management load on SW
- Pool depletion thresholds for pool replenishment and lossless flow control
 - All thresholds have hysteresis

SEC 5.x



- Public Key Hardware Accelerators (PKHA)
 - RSA and Diffie-Hellman (to 4096b)
 - Elliptic curve cryptography (1023b)
 - Supports Run Time Equalization
- Data Encryption Standard Accelerators (DESA)
 - DES, 3DES (2K, 3K)
 - ECB, CBC, OFB modes
- Advanced Encryption Standard Accelerators (AESA)
 - Key lengths of 128-, 192-, and 256-bit
 - ECB, CBC, CTR, CCM, GCM, CMAC,
 - OFB, CFB, and XTS
- Message Digest Hardware Accelerators (MDHA)
 - SHA-1, SHA-2 256,384,512-bit digests
 - MD5 128-bit digest
 - HMAC with all algorithms
- ARC Four Hardware Accelerators (AFHA)
 - Compatible with RC4 algorithm
- Kasumi/F8 Hardware Accelerators (KFHA)
 - F8 , F9 as required for 3GPP
 - A5/3 for GSM and EDGE
 - GEA-3 for GPRS
- Snow 3G Hardware Accelerators (STHA)
 - Implements Snow 3.0
- CRC Unit
 - CRC32, CRC32C, 802.16e OFDMA CRC
- Random Number Generator, random IV generation
- Header & Trailer off-load for the following Security Protocols:
 - IPSec, 802.1ae, SSL/TLS, SRTP, 802.11i, 802.16e
- Modular & Scalable with simplified device driver



QorIQ Linux SDK



QorIQ Linux SDK

- SDK 1.7 supports T1014/24 rev 1.0
- SDK 1.8 supports T1014/24 rev 1.0, T1013/T1023 rev 1.0 (June 2015)

- Download Linux SDK for QorIQ Processors
<http://freescale.com/sdk>

- For help with SDK see documentation on Infocenter
<http://freescale.com/infocenter>

- Git repositories available online
<http://git.freescale.com>



QorIQ SDK Documentation on Freescale Infocenter

The screenshot displays the Freescale Infocenter website. The browser address bar shows www.freescale.com/infocenter/index.jsp. The page features a navigation menu with links for [Products](#), [Applications](#), [Design Resources](#), [Support](#), [Sample and Buy](#), and [About](#). The main content area is titled "Information Center" and includes a search bar with the text "Go Scope: scope1". A left-hand navigation pane shows a tree structure under "Software and Tools Information Center", with "QorIQ SDK 1.7 Documentation" expanded to show "Components" as the selected item. The main content area displays the "Components" section, listing top-level components in the QorIQ SDK:

- Yocto
- GNU Toolchain
- U-Boot Boot Loader
- Linux Kernel and Virtualization
- Linux Kernel and Device Drivers
- Application Specific Fastpath (ASF)
- User Space Datapath Acceleration Architecture (USDPA) and Applications
- Freescale Embedded Hypervisor (Topaz)
- Other Tools and Utilities

Below this list, there are sections for "Yocto" and "GNU Toolchain", each with a bulleted list of details. The "Yocto" section includes "Yocto/Poky 1.6.1 'Daisy'" and "Open source collaboration project that provides templates, tools and methods for building custom Linux-based systems for embedded products". The "GNU Toolchain" section lists "power: gcc-4.8.1, eglibc-2.15, binutils-2.23.2, gdb-7.6.2" and "arm: gcc-linaro-4.8.3-2014.04, eglibc-linaro-2.18-r2014.04, binutils-linaro-2.23.2-r2014.03, gdb-linaro-7.6.1-r2013.10". A "U-Boot Bootloader" section contains a note: "NOTE: FLASH MAP CHANGE FOR SDK 1.6 AND LATER". At the bottom of the page, there is a "Request Support" link and a copyright notice: "© Freescale Semiconductor, Inc. 2004 - 2014. All Rights Reserved."



Freescale Infocenter

The screenshot shows the Freescale Infocenter website. At the top, there is a navigation bar with tabs for [Products](#), [Applications](#), [Design Resources](#), [Support](#), [Sample and Buy](#), and [About](#). The page title is "Information Center". Below the navigation bar is a search bar with the text "Search:" and a "Go" button. The search results show "Scope: scope1".

The main content area is divided into two columns. The left column is titled "Contents" and lists various categories under "Scope scope1: [Show all](#)". The categories include:

- Software and Tools Information Center
 - QorIQ SDK 1.7 Documentation
 - SDK Overview
 - Introduction
 - Yocto SDK File System Images
 - What's New
 - Components**
 - Supported Targets
 - Feature Support Matrix
 - Acronyms and Abbreviations
 - Known Issues
 - Getting Started with Yocto Project
 - Software Deployment Guides
 - System Recovery
 - About Yocto Project
 - Linux Configuration
 - Linux Kernel Drivers
 - Linux User Space
 - U-Boot
 - Virtualization
 - Debug Tools
 - Standard for Embedded Power Archi
 - Benchmark Reproducibility Guides

The right column is titled "Linux Kernel Device Drivers" and lists the following drivers:

- Crypto driver supporting SEC 2, 3, 4 & 5 (Talitos and CAAM)
- Display Control Unit (DCU) and HDMI [LS1021A]
- Display Interface Unit (DIU) [T1042 and P1022]
- DPAA Offloading Driver [T4240, T2080, P4080, P2041, B4860, B4420]
- DUART, eSPI, I2C
- Ethernet DPAA
- Ethernet eTSEC (gianfar)
- FlexCAN [P1010/14]
- Frame Manager (FMan)
- Frame Manager uCode
- IEEE1588
- Integrated Flash Controller (IFC) NOR and NAND flash
- Local Bus Controller (eLBC) NOR and NAND flash
- LPUART [LS1021A]
- Multiprocessor Interrupt Controller (MPIC)
- PCIe
- Platform DMA
- Pattern Matching Engine (PME)
- Peripheral Access Management Unit (PAMU)
- PHY support: RGMII, SGMII, XFI and XAUI
- Power Management (PM)
- Power Monitor using on-board sensors [T4240QDS, P5020DS, P1022DS]; direct access or through FPGA-OCM
- Queue Manager (QMan) and Buffer Manager (BMan)
- QUICC Engine UART, Ethernet, TDM
- RAID Engine & support for hardware-assist [P5020]
- Real-Time Clock
- SATA
- Secured Digital Host Controller (eSDHC) and SD/MMC support (all except for TF on T2080)

At the bottom of the page, there is a "Request Support" link and a copyright notice: "© Freescale Semiconductor, Inc. 2004 - 2014. All Rights Reserved."



DPAA Primer for Software Architecture

The screenshot shows a web browser window with the URL www.freescale.com/infocenter/index.jsp. The page features the Freescale logo and a navigation menu with links for Products, Applications, Design Resources, Support, Sample and Buy, and About. A search bar is present with the text "Go Scope: All topics".

The main content area is titled "Information Center" and displays a breadcrumb trail: [Software and Tools Information Center](#) > [QorIQ SDK 1.7 Documentation](#) > [Linux Kernel Drivers](#). The primary heading is "DPAA Primer for Software Architecture".

A left-hand navigation pane lists various topics, with "DPAA Primer for Software Architecture" selected. Sub-topics under this selection include DPAA Primer, DPAA Goals, FMan Overview, QMan Overview, QMan Scheduling, BMan, Order Handling, Pool Channels, Application Mapping, and FQ/WQ/Channel.

The main content area contains several sections, each with a blue link header and a brief description:

- DPAA Primer**: A brief overview of the DPAA elements in order to contextualize the application mapping activities. For more details on the DPAA architecture, see the [QorIQ Data Path Acceleration Architecture \(DPAA\) Reference Manual](#).
- FMan Overview**: The FMan inspects traffic, splits it into FQs on ingress, and sends traffic from the FQs to the interface on egress.
- QMan Overview**: The QMan links the FQs to producers and consumers (of data traffic) within the SoC. The producers/consumers are either FMan, acceleration blocks, or CPU cores.
- QMan Scheduling**: The QMan links the FQs to producers and consumers (of data traffic) within the SoC.
- BMan**: The BMan block manages the data buffers in memory. Processing cores, FMan, SEC and PME all may get a buffer directly from the BMan without additional software intervention. These elements are also responsible for releasing the buffers back to the pool when the buffer is no longer in use.
- Order Handling**: The DPAA helps address packet order issues that may occur as a result of running an application in a multiple processor environment. And there are several ways to leverage the DPAA to handle flow order in a system. The order preservation technique maps flows such that a specific flow always executes on a specific processor core.
- Pool Channels**: A user may employ a pool channel approach where multiple cores may pool together to service a specific set of flows. This alternative approach allows potentially better processing balance, but increases the likelihood that packets may be processed out of order allowing egress packets to pass ingress packets.
- Application Mapping**: The first step in application mapping is to determine how much processing capability is required for flows that may be partitioned.

At the bottom of the page, there is a "Request Support" link and a copyright notice: "© 2004-2015 Freescale Semiconductor, Inc. All Rights Reserved." The footer also includes links for Site Map, Terms of Use, Privacy Practices, View Agreement, and Contact Us.



Flash Images

- QorIQ Linux SDK provides images and binaries ready for use on supported reference design boards
 - U-Boot
 - RCW
 - Frame Manager microcode
 - Linux kernel
 - Linux device tree
 - RAM disk (root file system)
- After Yocto Project build, images will be located in directory
 - QorIQ-SDK-V1.7-20141218-
yocto/build_t1024rdb_release/tmp/deploy/images/t1024rdb/



Q&A





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