FTF FREESCALE TECHNOLOGY FORUM 2015

Introducing i.MX 7 Series Applications Processors

FTF-INS-F1134

Nik Jedrzejewski | i.MX 7 Product Line Manager

J U N E . 2 0 1 5

freescale™

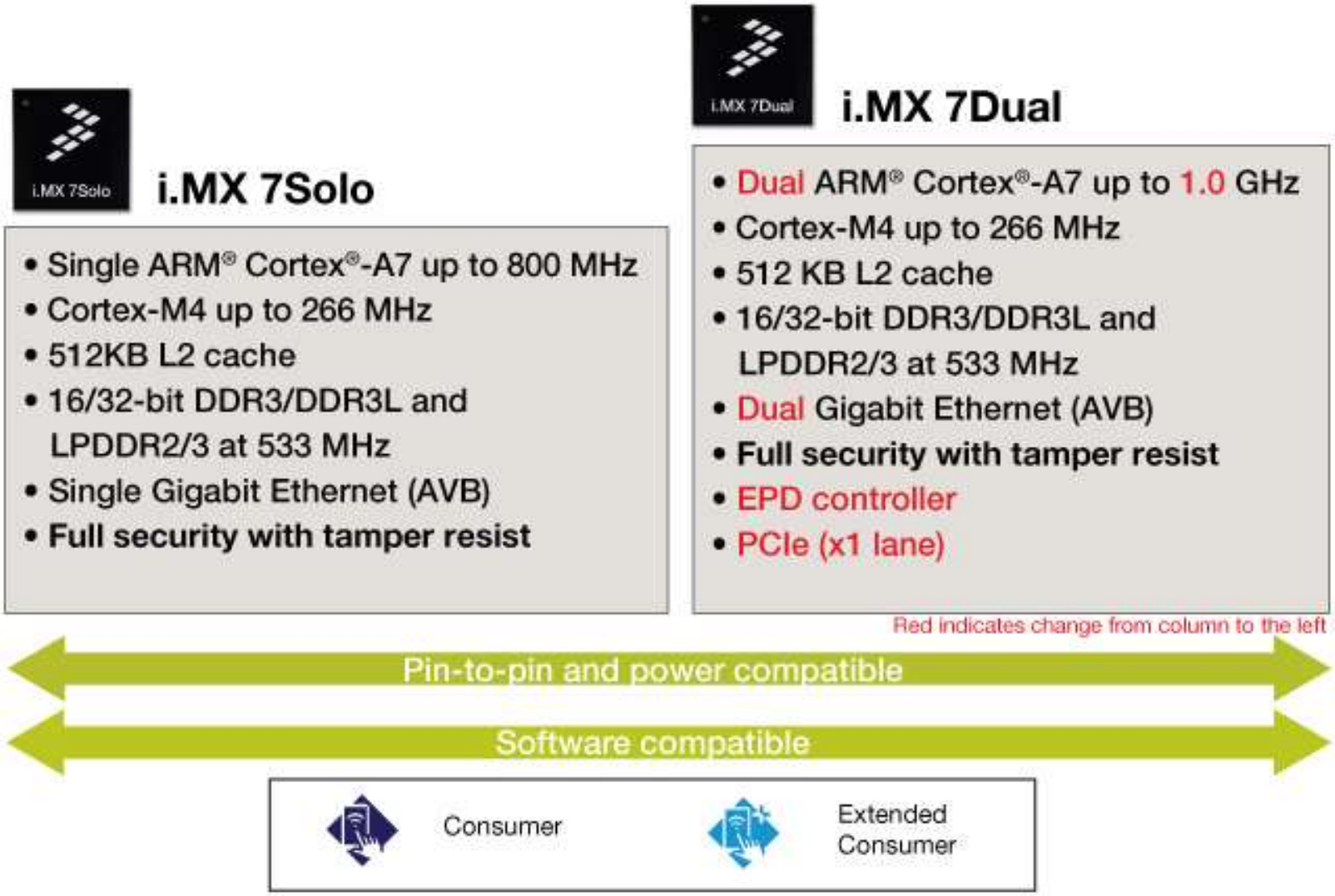
External Use

Market Challenges Addressed by i.MX 7 series

- Achieving longer battery life
- Addressing system security needed in IoT systems
- Integrating memory standards which produce best performance and cost
- Maintaining latest high speed connectivity standards
- Achieving small form factors for space constrained applications
- Supporting the latest EPD technology

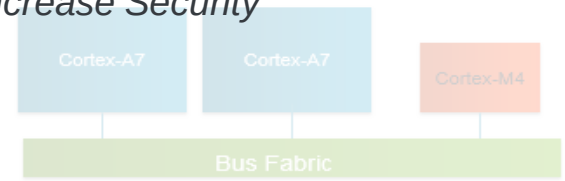
i.MX 7 Series

i.MX 7 Series Overview



i.MX 7 Series Advantages

- **Advanced Heterogeneous Architecture**
  - Single and Dual Cortex-A7 Core up to 1GHz
  - Cortex-M4 up to 266MHz
    - *Offload Tasks*
    - *Optimize Power*
    - *Increase Security*

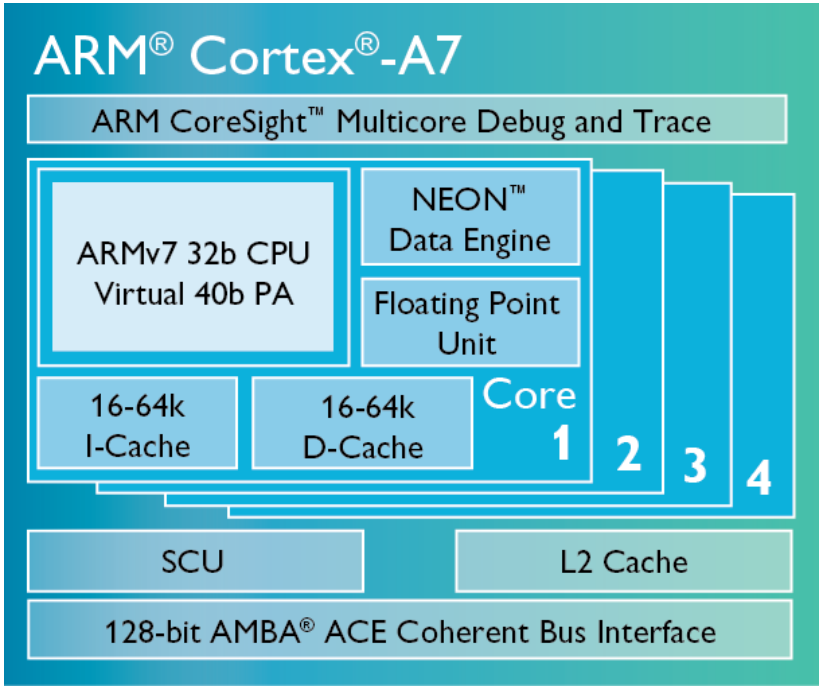


- **Unmatched Power Efficiency**
  - **3x improvement in Power Efficiency vs. i.MX 6**
  - **100 uW/MHz for Cortex-A7**
  - **70 uW/MHz for Cortex-M4**
  - **One third the power consumed in the Low-Power suspend mode (250 uW) vs. i.MX 6.**

- **Enabling Flexible High Speed connectivity**
  - PCI-e v2.1
  - Dual Gbit Ethernet with AVB
  - DDR QuadSPI support
  - eMMC 5.0

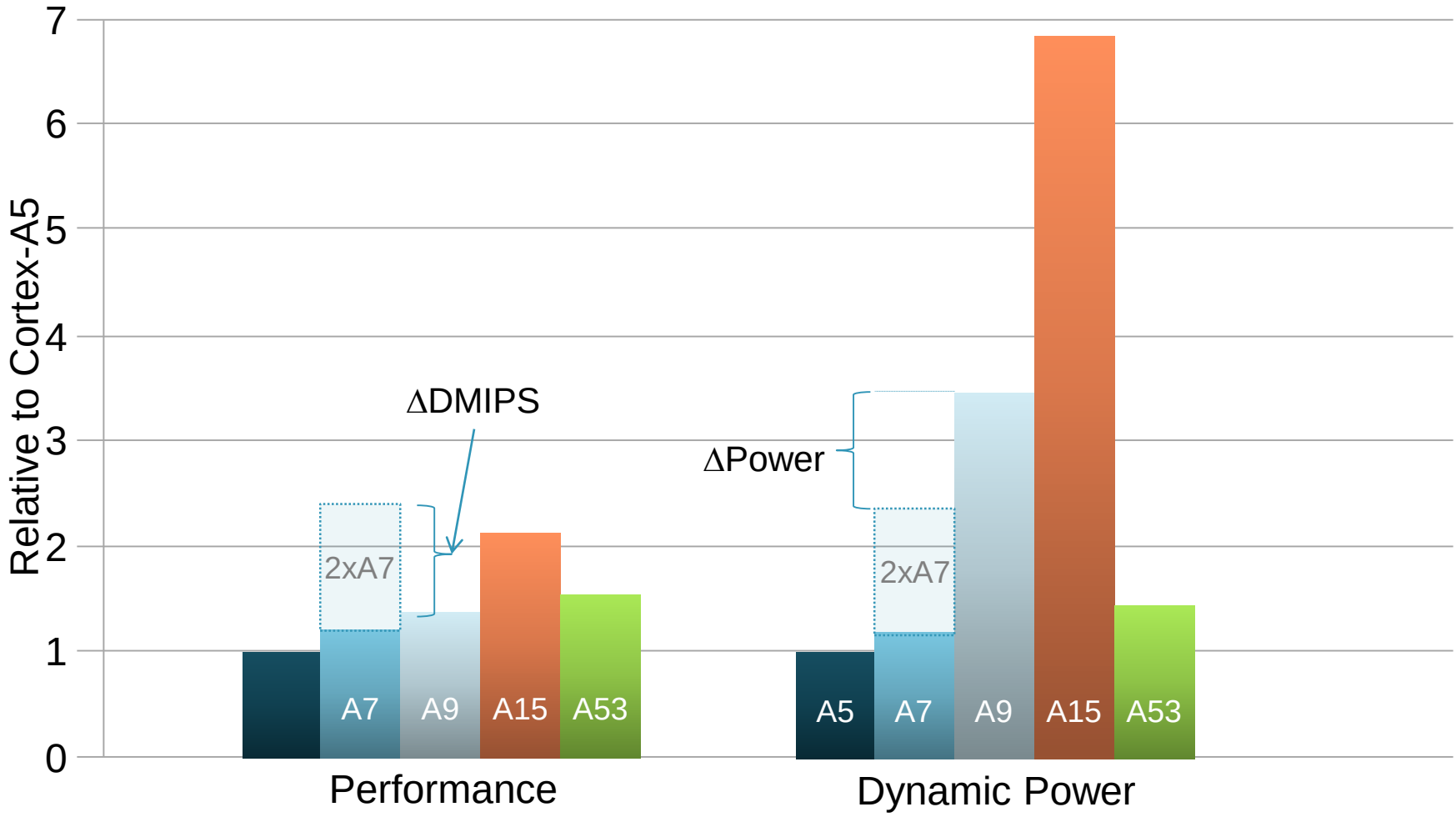
- **Complete Security Infrastructure**
  - Secure Boot
  - Crypto H/W Acceleration
  - Internal and External Tamper Detection
  - Secure RAM
  - DPA attack Resistance
  - Secure JTAG

- ARMv7-A
- Thumb-2
- TrustZone® security technology
- NEON™ Advanced SIMD
- DSP & SIMD extensions
- VFPv4 Floating point



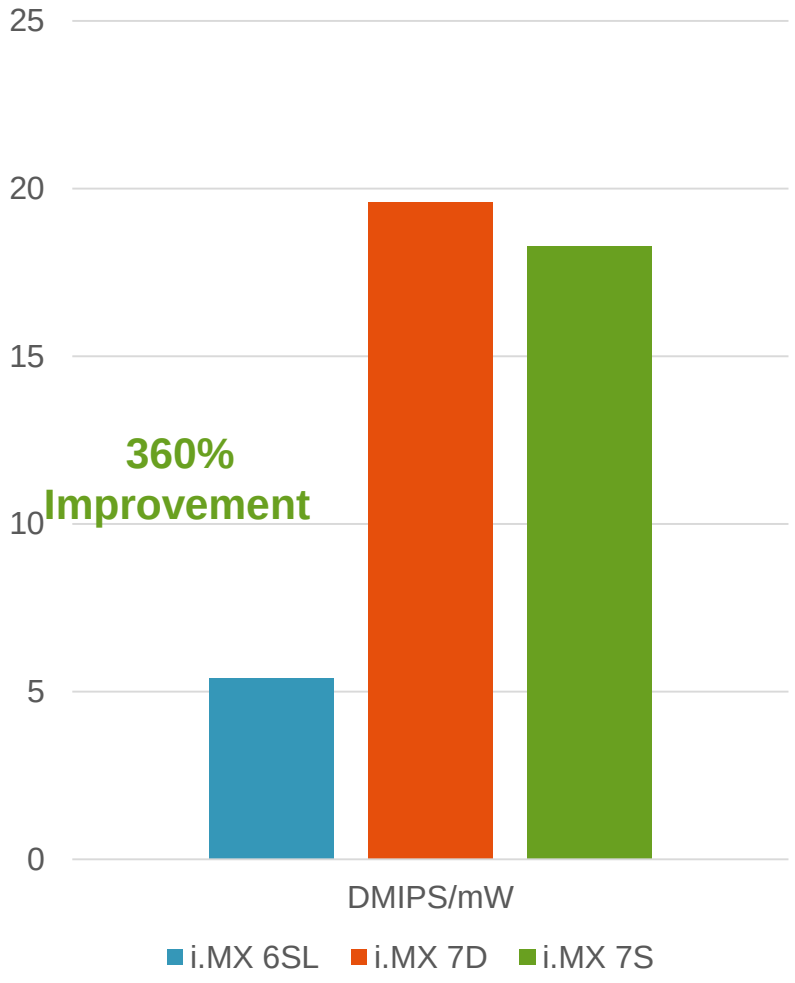
"The ARM Cortex-A7 processor is the most power-efficient multi-core processor."

Comparison (2xCortex-A7 vs 1xCortexA9)

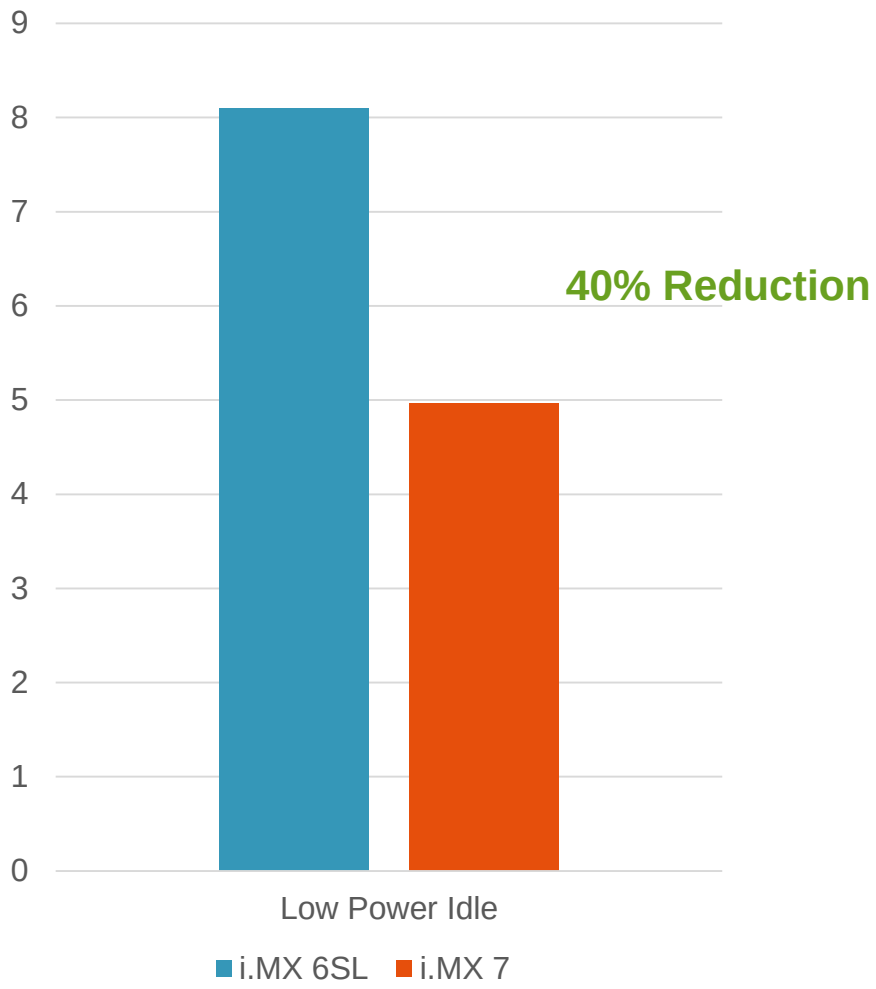


Performance is Specint2000 at synthesized frequency
Area is core with Neon + L1 cache, with L2 controller, MP1 configuration, no L2 RAM included
Power measured as Dhrystone at nominal voltage

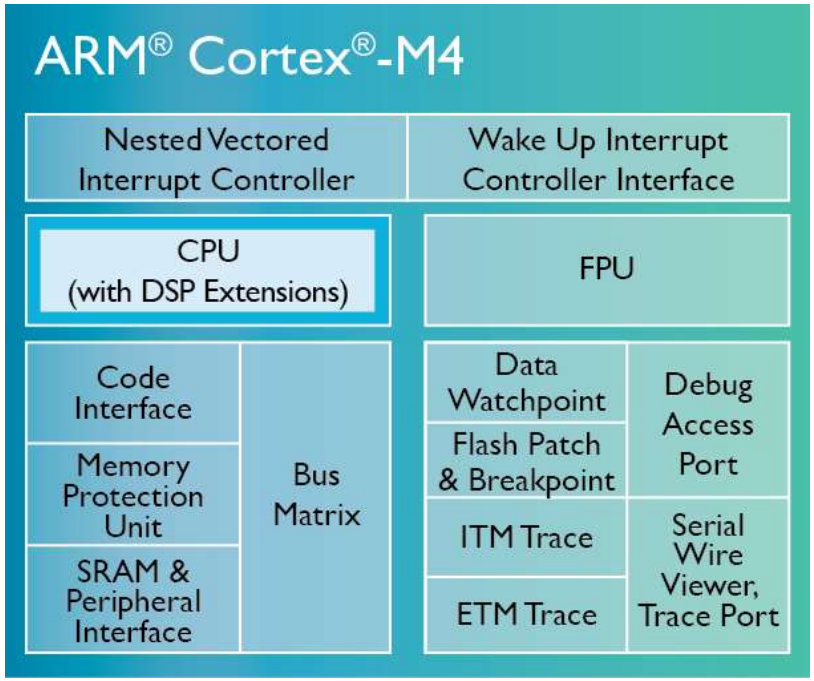
Power Efficiency Compute Complex



Low-Power Idle (mW)

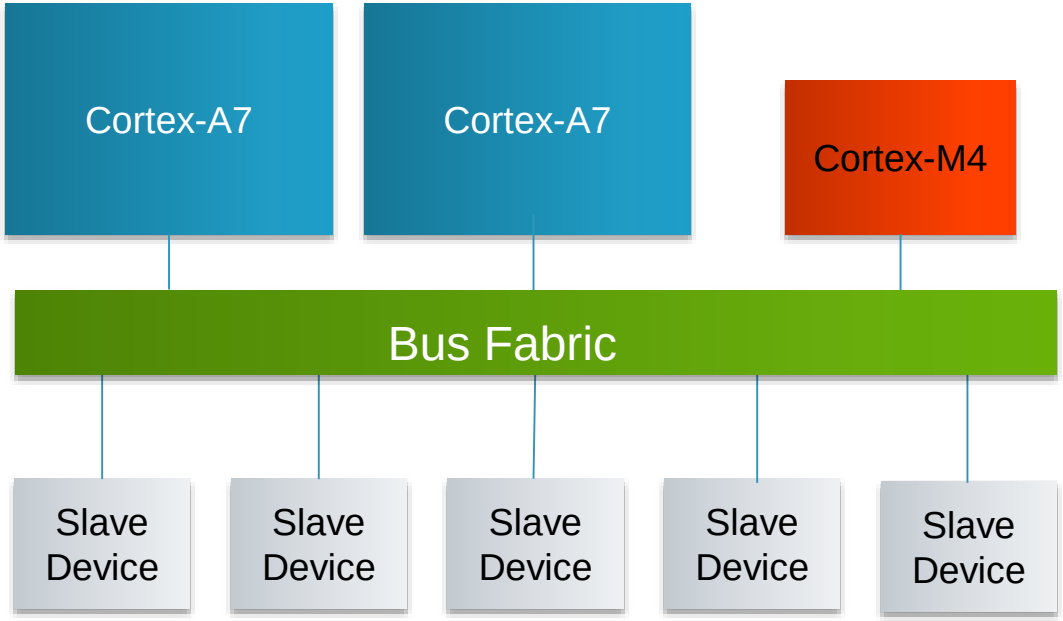


- ARMv7-M
- Thumb-2
- DSP Extensions & SIMD arithmetic
- FPU - Single precision floating point unit, IEEE 754 compliant
- 3.40 CoreMark/MHz



Heterogeneous Multi Processing (HMP)

Shared Topology



Shared bus topology

- Peripherals can be shared between both cores.
- Flexible partitioning of memory

Split bus topology

- Lacks flexibility to repartition the resources
- Duplication of Resources

Market Challenge

- Growing number of embedded use cases require concurrent execution of isolated and secure software environments
- Multiple software execution environments are needed for:
  - Real-time performance
  - System integrity and security
  - Power consumption
  - Faster boot

i.MX 7 Series Target Applications

MOBILE DEVICES

LPDDR2/3
Small Package

CONNECTED DEVICES

Low Cost DDR3
Larger Pitch Package

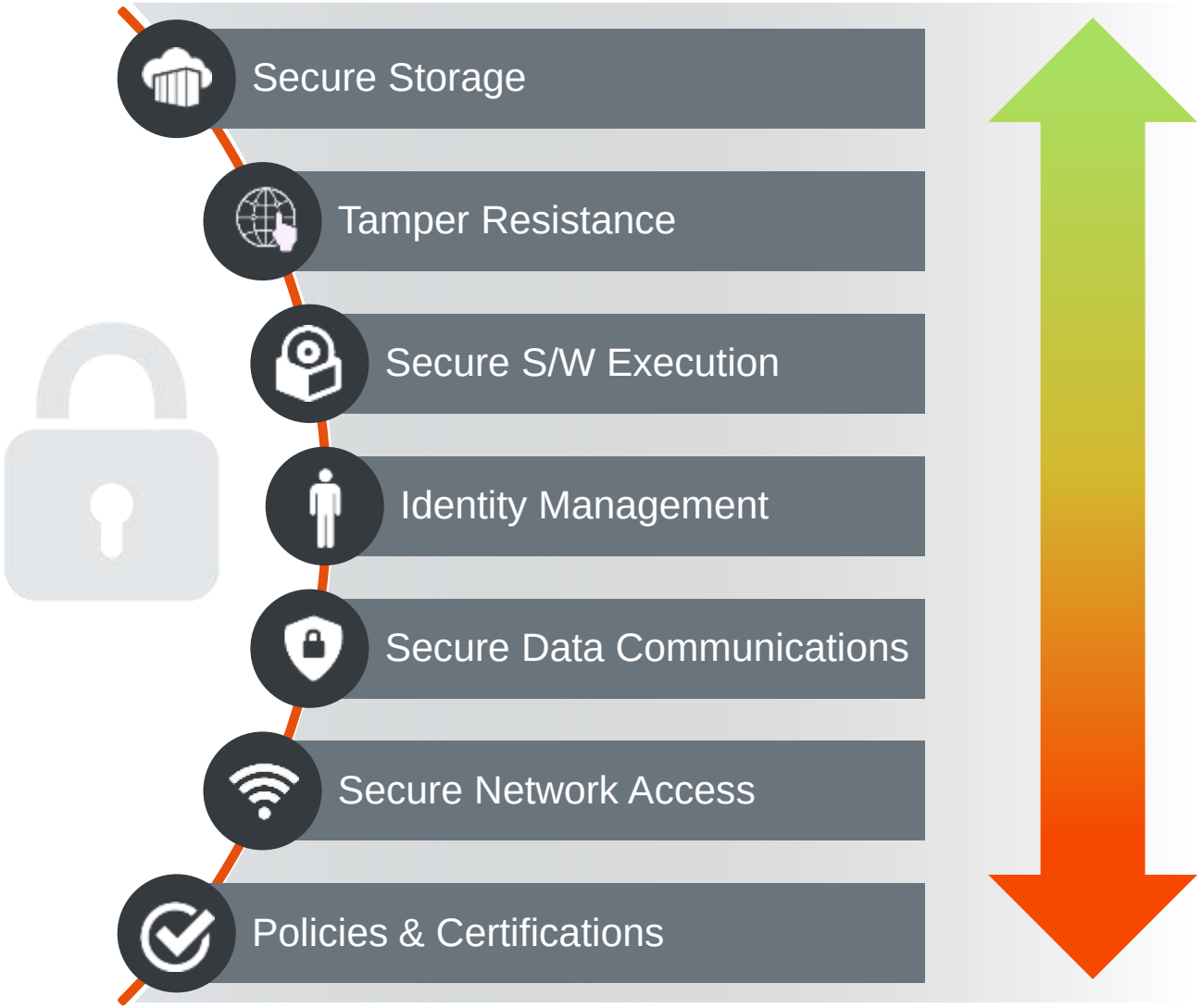
- e-Readers
- Building automation
- Wearables
- Point-of-Sale
- Enterprise scanners and printers
- Smart home controls
- Patient monitoring
- IoT solutions

Securing IoT

- i.MX 7 Hardware Security enables a safe and secure IoT
  - Healthcare – patient monitoring, fitness equipment, wearables
  - Factory, process and building automation (thermostats, gateways, surveillance, HMI)
  - Appliances, VoIP
  - Test and Measurement




Security – i.MX Hardware Enablement



In-Line Encryption (Memory)

Manufacturing Protection

Authenticated debug & Field returns

Run-time integrity

Trust Zone

Secure Storage

Zeroizable RAM

Root of trust

Cryptographic Acceleration

Symmetric & Asymmetric accl.

Random Number Generator

Attack Protection

Active Tamper Detection (Physical)

DPA Protection (Side Channel)

Secure S/W Execution

Resource Domain Control

System Memory Protection Unit

i.MX 7Solo

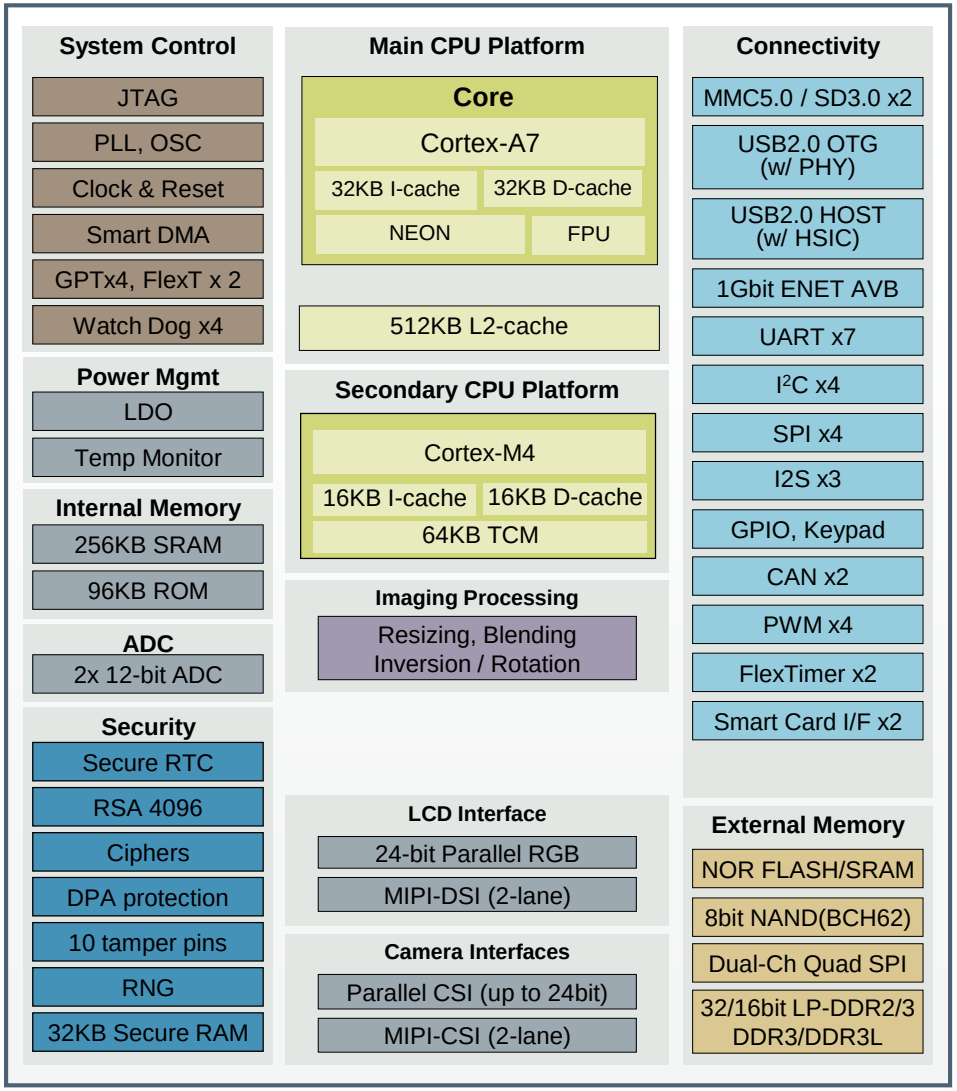
Specifications:

- **CPU**: Single Core Cortex-A7 @ 800MHz (Nominal)
- **Package:** 19x19@0.75mm BGA
  12x12@0.4mm BGA*
- **Qualification**: Consumer (0C to 95C Tj)
  Extended Consumer (-20C to 105C Tj)
  - 10yr lifetime at 100% duty cycle

Key Features and Advantages

- **800MHz, Cortex-A7, 32KB I/D, 512KB L2 Cache**
- **266MHz Cortex M4, 16KB I/D, 64KB TCM**
- **Memory Support**
  - 16/32bit LP-DDR2/3, DDR3/L @ 533MHz;
  - Total of 256KB OCRAM
  - 2x SDIO3.0/eMMC5.0, 8-bit NAND Flash with ECC(BCH62)
- **Display / Camera**
  - 24-bit Parallel LCD and MIPI DSI (2-lane)
  - Parallel (up to 24-bit) and MIPI CSI (2-lane)
- **I/O**
  - 1x USB 2.0 OTG w/ PHY + 1xUSB 2.0 HOST/HSIC
  - 1x GigE Ethernet Ports-AVB;
  - 4x SPI (1x is 60MHz and 3x at least 10MHz);
  - 4x 32-bit Timer (GPT), 2x FlexTimer
  - 4x PWMs; 4x I2C,
  - 7x UARTs
  - SIMv2/EMVSIM (ISO7816/EMV2000L1 support)

- **Security module - enabling PCI 4.0 compliance**



* Feature limited (1 ADC, 4 tamper pins)

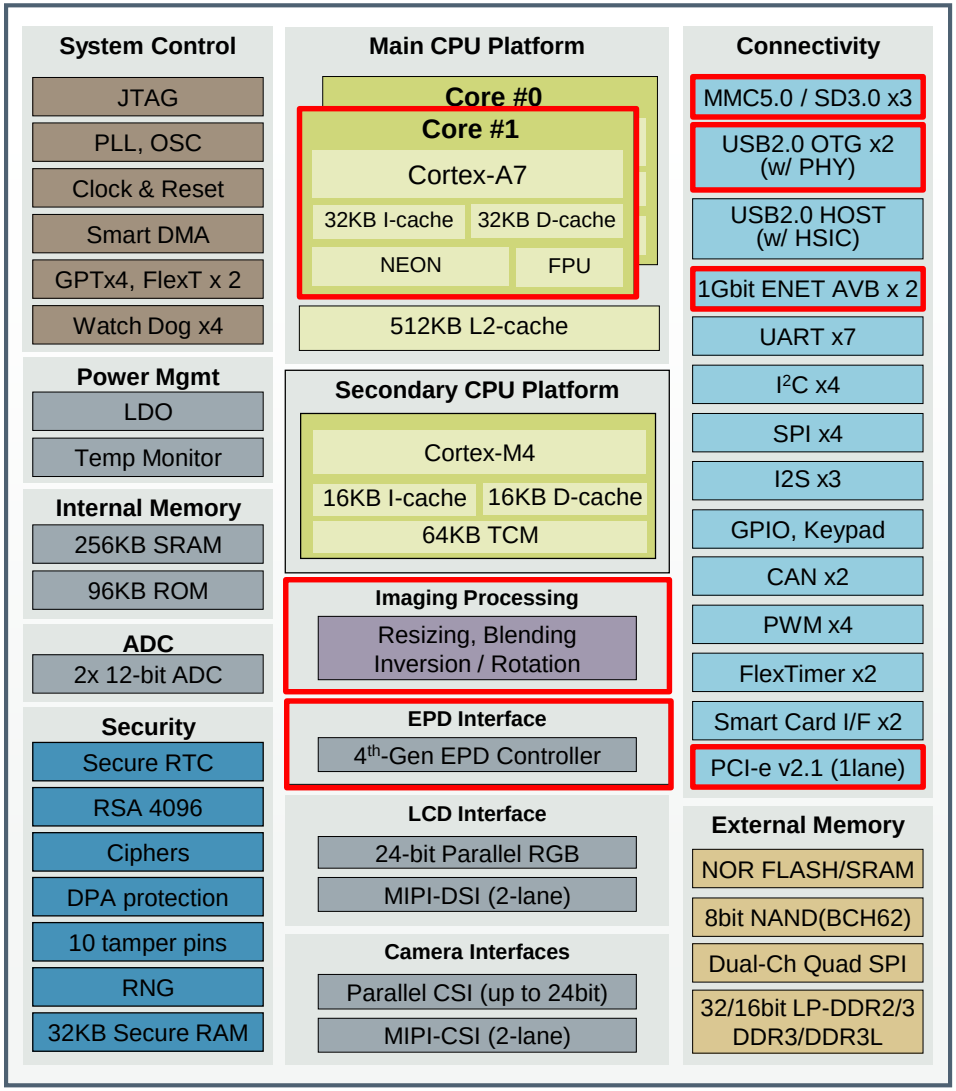
i.MX 7Dual

Specifications:

- **CPU**: Dual Core Cortex-A7 @ 1GHz
- **Package:** 19x19@0.75mm BGA
  12x12@0.4mm BGA*
- **Qualification**: Consumer (0C to 95C Tj)
- Extended Consumer* (-20C to 105C Tj)
  - *10yr lifetime at 100% duty cycle

Key Features and Advantages

- **1GHz, Cortex-A7, 32KB I/D, 512KB L2 Cache**
- **266MHz Cortex M4, 16KB I/D, 64KB TCM**
- **Memory Support**
  - 16-/32-bit LP-DDR2/3, DDR3/L @ 533MHz;
  - Total of 256KB OCRAM (128KB dedicated to EPDC if used)
  - 3x SDIO3.0/eMMC5.0, 8-bit NAND Flash with ECC(BCH62)
- **Display / Camera**
  - 4th generation EPD Controller (2332x1650@106Hz)
  - LCD: 24-bit Parallel LCD and MIPI DSI (2-lane)
  - Parallel (up to 24-bit) and MIPI CSI (2-lane)
- **I/O**
  - 1x PCI-e (1-lane)
  - 2x USB 2.0 OTG w/ PHY + 1xUSB 2.0 HOST/HSIC
  - 2x GigE Ethernet Ports-AVB;
  - 4x SPI (1x is 60MHz and 3x at least 10MHz);
  - 4x 32-bit Timer (GPT), 2x FlexTimer
  - 4x PWMs; 4x I2C,
  - 7x UARTs
  - SIMv2/EMVSIM (ISO7816/EMV2000L1 support)
- **Security module - enabling PCI 4.0 compliance**



* Feature limited (1 ADC, 4 tamper pins)

Updated from i.MX 7Solo

Product Longevity and Energy Efficiency Programs

- Freescale provides a product longevity program for the market segments we serve. For all market segments in which Freescale participates, Freescale will make the i.MX 7 family extended consumer range of devices available for a period of 10 years.

- The Freescale Energy-Efficient Solutions mark designates products whose implementation of energy or power management technologies and/or performance within a specified energy budget over the life of the application is truly optimal and/or best-in-class.

- For terms and conditions and to obtain a list of available products, visit www.freescale.com/productlongevity and www.freescale.com/energyefficiency

Connectivity

i.MX non-GPU/VPU Product Lineup

Feature	i.MX25x	i.MX28x	i.MX 6UL	i.MX 7Solo	i.MX 7Dual
Core	ARM9	ARM9	**Cortex-A7 @ 528 MHz**	Cortex-A7 **@800 MHz**	**Dual** Cortex-A7 **@1GHz**
L2 Cache	-	-	128KB	**512KB**	512KB
RAM	128KB	128KB	128KB	**256KB**	256KB
2nd Core	-	-	-	**Cortex-M4**	Cortex-M4
Flash Interface	MLC/SLC NAND Flash w/ 8-bit RS, NOR Flash	SLC/MLC/Managed NAND Flash w/ 20-bit BCH	SLC/MLC/Managed NAND Flash w/ 40-bit BCH	SLC/MLC/Managed NAND Flash 60-bit BCH, 8-bit RS	SLC/MLC/Managed NAND Flash 60-bit BCH, 8-bit RS
DRAM Interface	150 MHz 16-bit DDR2, mDDR, SDRAM	**200 MHz** 16-bit DDR2, LV-DDR2, mDDR	**400 MHz 16-bit DDR3/L, LPDDR2**	**533 MHz 32-bit** DDR3/L, LPDDR2, **LPDDR3**	**533 MHz 32-bit** DDR3/L, LPDDR2, **LPDDR3**
Display	24-bit Parallel-640x480	24-bit Parallel RGB-640x480	24-bit Parallel RGB-**1366x768**	24-bit Parallel RGB-**1920x1080** **MIPI-DSI (2 lane) 1.5Gbps**	24-bit Parallel RGB-1920x1080 MIPI-DSI (2 lane) 1.5Gbps **EPDC**
Imaging	1 overlay, alpha blending, panning	**8 overlays**, alpha blending, scaling, rotation, color space conversion	PXP – Scaling, Alpha Blending, CSC, Dithering	PXP – Scaling, Alpha Blending, CSC, Dithering. **Pixel Buffer integration**	PXP – Scaling, Alpha Blending, CSC, Dithering. Pixel Buffer integration
Camera Interface	Parallel Camera I/F	-	Parallel Camera I/F	Parallel Camera I/F, **MIPI-CSI**	Parallel Camera I/F, **MIPI-CSI**
CAN	x2	x2	x2	x2	x2
10/100 Ethernet	Single 10/100	Dual 10/100 **and L2 Switch**	Dual 10/100	Single **1Gb (AVB)**	**Dual** 1Gb (AVB)
Analog Audio	I2S	I2S	I2S	**MQS**, I2S	MQS, I2S
S/PDIF	No	**1 output**	1 output	No	No
USB 2.0	HS port (Host/Device) HS PHY x1,HS Host with FS PHY x1	HS port (Host/Device) with PHY x1, HS port Host with PHY x1	OTG with PHY x2	OTG with PHY x1 **HSIC**	OTG with PHY **x2** HSIC
SIM	x2	-	x2	x2	x2
PCIe	-	-	-	-	Yes
Security	Tamper Detection, RNG	HAB4, PRNG	**Secure Boot/HAB, PRNG, AES/3DES/Ellipitical Curve/RSA, DPA protection, Up to 10 Tamper Pins, OTF RAM Encryption / Decryption**	**Secure Boot/HAB, PRNG, AES/3DES/Ellipitical Curve/RSA, DPA protection, Up to 10 Tamper Pins,**	**Secure Boot/HAB, PRNG, AES/3DES/Ellipitical Curve/RSA, DPA protection, Up to 10 Tamper Pins,**
Power Management	External	**Fully integrated PMIC (LDOs, DCDCs, Batt Charger)**	Analog LDOs	Analog LDOs	Analog LDOs

Performance Advantage | BOM Advantage

Migration from i.MX 6 Series Simplified

Maximizing i.MX IP reuse

IP Re-Use

- DMA, fabric, SRAM
- Semaphores
- Peripherals
  - UART
  - I2C
  - I2S
  - PWM
  - GPIO…
- Ethernet
- Cortex-M4 + MQX
- USB
- FlexCAN

+

Updated IP

- 4th gen EPDC
- LCD
- PXP
- Gbit Ethernet
- Power Mgmt
- SDIO/MMC
- NAND
- DEBUG / JTAG
- SNVS
- Central Security
- SIM Card
- IOMUX

+

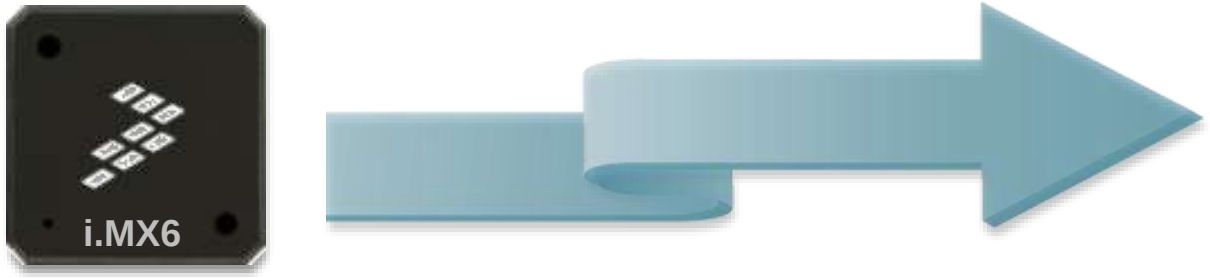
New IP

- CPU Complex
  - v7 Core keeps compatibility
- eMMC
- PCIe
- MIPI
- DDR Controller

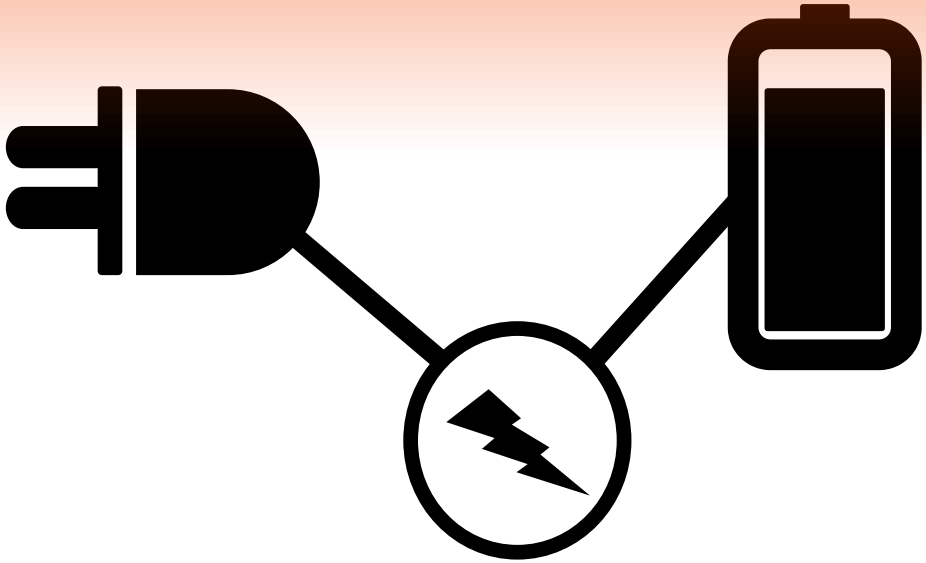
=

Easy Migration

- **Familiar SW & Tools**
  - Known Environment
  - Similar BSP code / validation
- **Focus on enhanced value**
  - Low-power, high performance
  - Scalability for the future
  - use models via M4 core offload



i.MX 7: Power Architecture

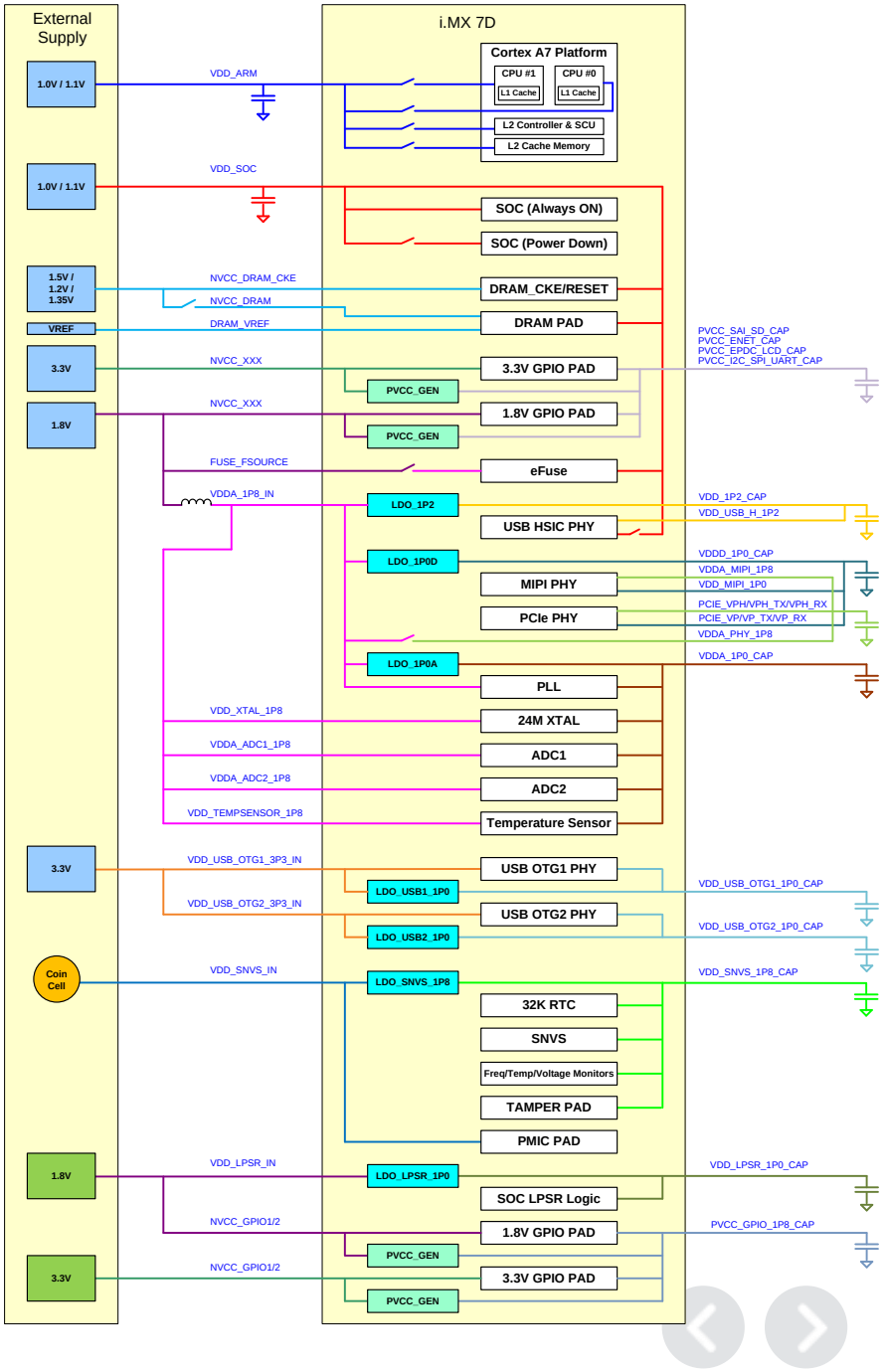


i.MX 7: Power Diagram

Full configuration

- **External Supply**
  - 1.0V **ARM CPU**
  - 1.0V **SOC**
  - 1.2/1.5/1.35 **DRAM IO**
  - 1.8V **Analog**
  - 1.8V / 3.3V **I/O**
  - 3.3V **USB**
  - 1.8V **LPSR**
  - 1.8V / 3.3V **IO in LPSR**
  - 2.8V – 3.6V **SNVS / Coin Cell**

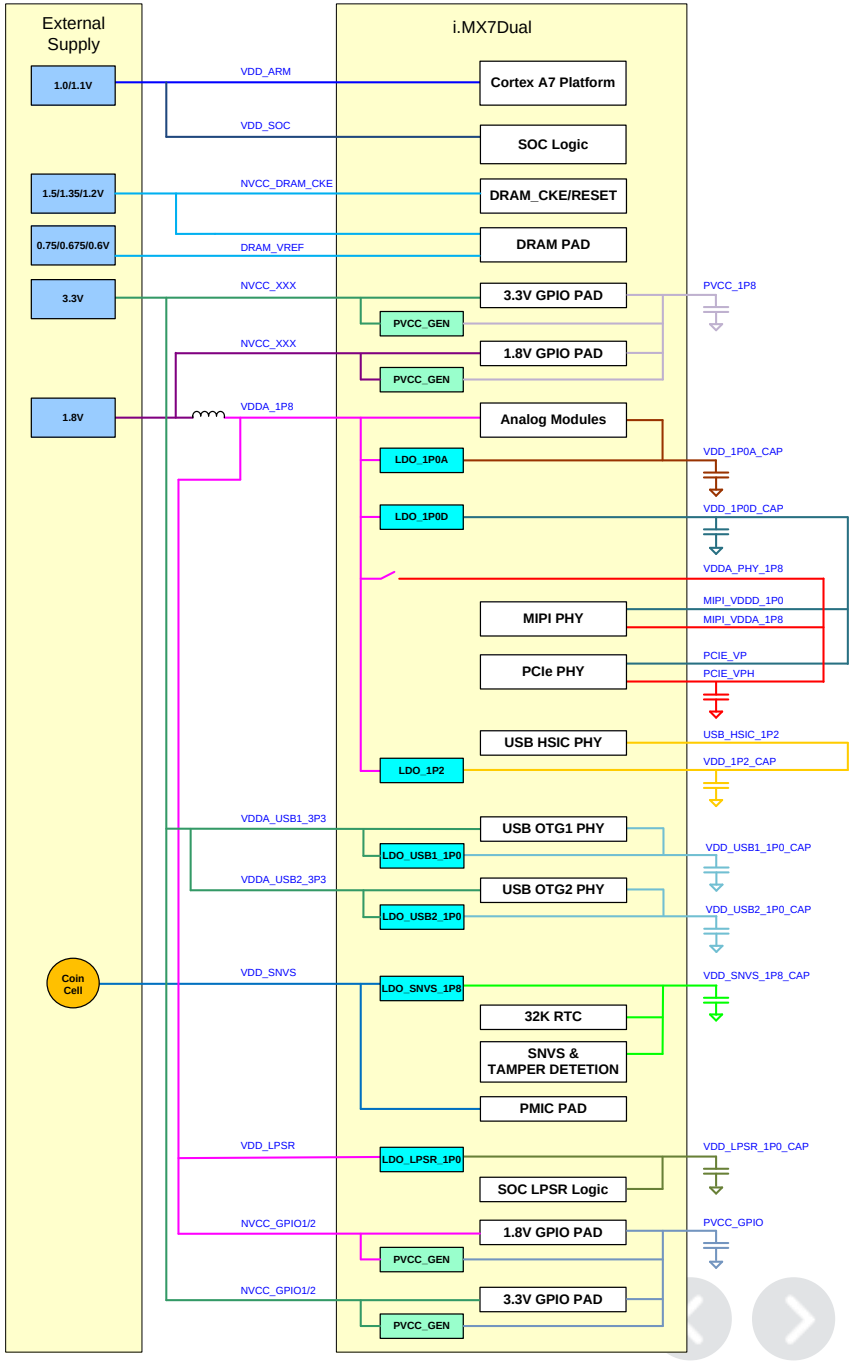
- **Integrated LDO**
  - **Analog Modules (bypass allowed)**
  - **MIPI PHY and PCIe PHY.**
  - **USB HSIC PHY.**
  - **USB PHY1.**
  - **USB PHY2.**
  - **LPSR logic.**
  - **SNVS and 32K RTC**.



i.MX 7: Power Diagram

Simplified configuration

- **VDD_ARM + VDD_SOC**
- **Single 3.3V supply**
  - **No wake up from GPIO**
- **Single 1.8V supply**



i.MX 7: External Power Rails

Power rail	Voltage (V)	Description
VDD_ARM	**1.0/1.1**	Power supply for ARM A7 platform.
VDD_SOC	**1.0/1.1**	Power supply for all SOC digital logic except ARM A7
NVCC_DRAM	**1.2/1.35/1.5**	DRAM IO power supply 1.2V for LPDDR2/LPDDR3, 1.35V for DDR3L, 1.5V for DDR3
VDDA_1P8	**1.8**	Power supply for all analog module, also used as the input power source for internal analog LDOs
NVCC_XXX	**1.8/2.5/3.3**	Power supply for GPIO banks outside of state retention domain
VDDA_USB1_3P3 **VDDA_USB2_3P3**	**3.3**	Power supply for USB PHY
VDD_LPSR	**1.8**	Power supply for low power state retention domain
VDD_SNVS	**3.0**	Power supply for RTC and tamper detection logic, usually supplied by coin cell
NVCC_GPIO1	**1.8/3.3**	Power supply for GPIO bank1 in state retention domain
NVCC_GPIO2	**1.8/3.3**	Power supply for GPIO bank 2 in state retention domain

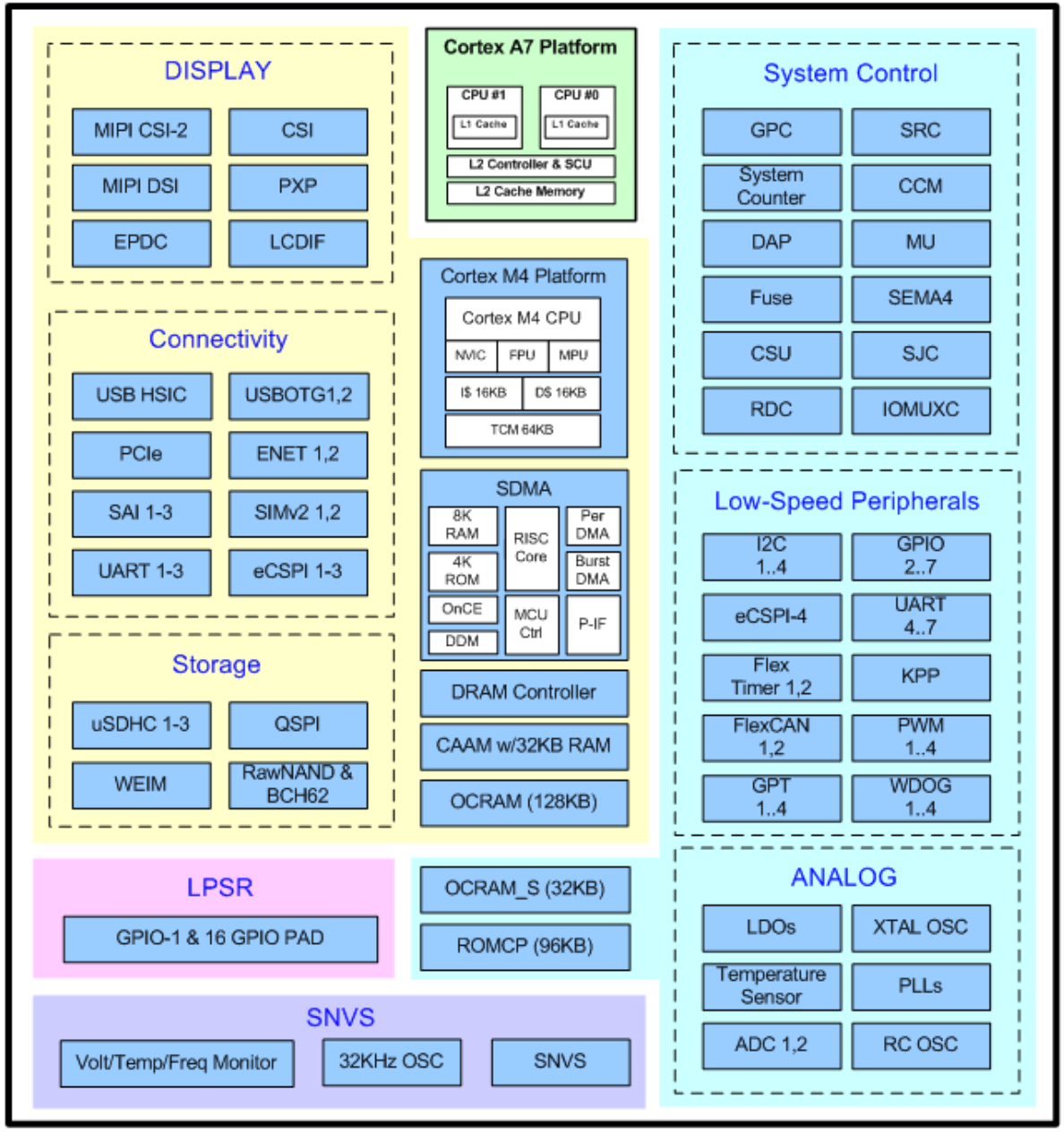
i.MX 7: Power Modes

Mode	Description
RUN	All external power rails are on, CPU is active and running, other internal module can be on/off based on application
SYSTEM IDLE	CPU automatically clock gated when in WFI state. 2 PLLs remain active, 24MHz XTAL on. Most of the peripherals remain active and running at 24MHz clock. 32K RTC and Tamper Detection are active. DRAM in auto-refresh.
LOW POWER IDLE	CPU power gated, most of the peripherals are clock gated. All PLL shut off, 24MHz XTAL off, 24MHz RC OSC on. Timer or other low speed peripheral can be running at 1MHz clock. 32K RTC and Tamper Detection are active. DRAM stay in self-refresh.
SUSPEND	CPU power gated, most of the peripherals are power gated. All PLL shut off, 24MHz XTAL off, all system clock shut off. 32K RTC and Tamper Detection are active. DRAM stay in self-refresh.
LPSR (SNVS&GPIO)	All digital/analog modules power down, only 16 GPIO pads keep alive for wake up, 32K RTC and Tamper Detection are active. DRAM can stay in self-refresh if NVCC_DRAM is active.
SNVS(RTC)	Only 32K RTC and Tamper Detection are active.
OFF	All power rails are off

*Targets are for typical silicon at room temp and are subject to change.

i.MX 7 Multiple Power Domains

Allows for most of SoC Digital and Analog logics to be power gated with internal power switch or LDO in low power mode.

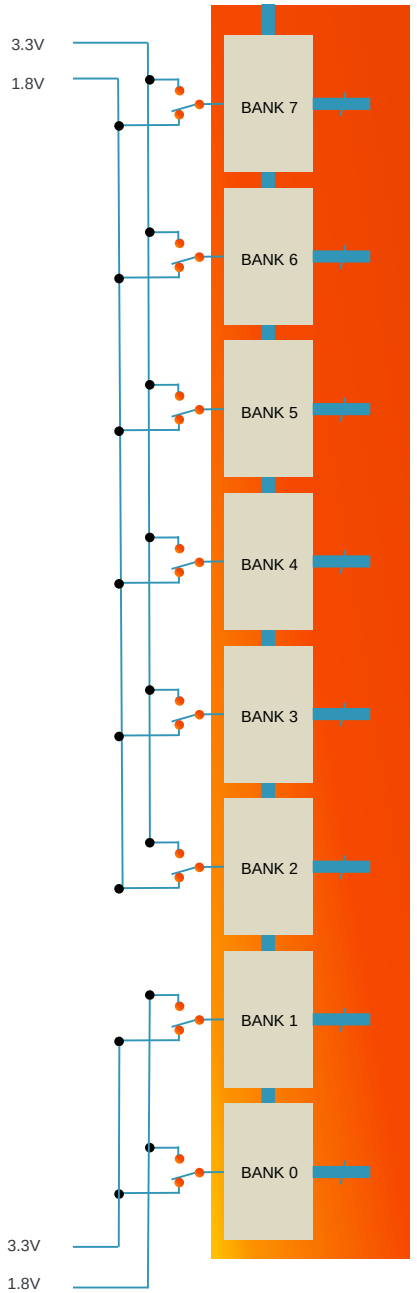


i.MX 7: General Input Output

I/O

I/O

- The GPIO pads grouped into banks,
  - each bank contains 8-16 GPIO pads;
- Each bank has own I/O power supplied,
  - supplied independently with either 3.3V or 1.8V;
- Possible to Configure All the I/O power supply to 1.8V for power efficiency.



Clock Pins

- Clock Input

Name	Frequency
XTAL	24MHz
RTC XTAL	32.768KHz

- Clock Output (to save external oscillator)

	Frequency
Audio Master Clock	24MHz / Audio PLL (Programmable)
CSI Master Clock	24MHz / System PLL/PFD (Programmable)
ENET Reference Clock	25MHz / 50MHz / 125MHz

I/O & PINMUX

GPIO Pins

PIN Type	Count	Power	Description
GPIO	12	NVCC_GPIO1	8 GPIO + POR_B, TEST_MODE, BOOT_MODE[1:0]
GPIO	14	NVCC_GPIO2	8 GPIO + 6 JTAG
EPDC	16	NVCC_EPDC1	Up to 8 alternative functions on each pin. All of them can be configured as GPIO. (see pinmux table for details)
EPDC	16	NVCC_EPDC2	
LCD	29	NVCC_LCD	
UART	8	NVCC_UART	
I2C	8	NVCC_I2C	
ECSPI	8	NVCC_ECSPI	
ENET1	16	NVCC_ENET1	
SD1	9	NVCC_SD1	
SD2	9	NVCC_SD2	
SD3	12	NVCC_SD3	
SAI	11	NVCC_SAI	
Total	**168**		

PINMUX

		Alt0	Alt1	Alt2	Alt3	Alt4	Alt5	Alt6	Alt7 (Test Signals)
106	UART3_RXD	uart3.RX	usb.OTG1_OC	sai3.RX_SYNC	ecspi1.MISO	enet1.1588_EVENT0_IN	gpio4.IO[4]	usdhc1.LCTL	sim_m.HADDR[28]
107	UART3_TXD	uart3.TX	usb.OTG1_PWR	sai3.TX_BCLK	ecspi1.MOSI	enet1.1588_EVENT0_OUT	gpio4.IO[5]	usdhc2.LCTL	sim_m.HADDR[29]
108	UART3_RTS	uart3.RTS_B	usb.OTG2_OC	sai3.TX_DATA[0]	ecspi1.SCLK	enet1.1588_EVENT1_IN	gpio4.IO[6]	usdhc3.LCTL	sim_m.HADDR[30]
109	UART3_CTS	uart3.CTS_B	usb.OTG2_PWR	sai3.TX_SYNC	ecspi1.SS0	enet1.1588_EVENT1_OUT	gpio4.IO[7]	usdhc1.VSELECT	sim_m.HADDR[31]
110	I2C1_SCL	i2c1.SCL	uart4.CTS_B	can1.RX	ecspi3.MISO	anatop.24M_OUT	gpio4.IO[8]	usdhc2.VSELECT	sim_m.HBURST[0]
111	I2C1_SDA	i2c1.SDA	uart4.RTS_B	can1.TX	ecspi3.MOSI	ccm.ENET1_REF_CLK_ROO	gpio4.IO[9]	usdhc3.VSELECT	sim_m.HBURST[1]
112	I2C2_SCL	i2c2.SCL	uart4.RX	wdog3.WDOG_B	ecspi3.SCLK	ccm.ENET2_REF_CLK_ROO	gpio4.IO[10]	usdhc3.CD_B	sim_m.HBURST[2]
113	I2C2_SDA	i2c2.SDA	uart4.TX	wdog3.WDOG_RST_B_DEB	ecspi3.SS0	ccm.ENET3_REF_CLK_ROO	gpio4.IO[11]	usdhc3.WP	sim_m.HRESP
114	I2C3_SCL	i2c3.SCL	uart5.CTS_B	can2.RX	csi1.VSYNC	sdma.EXT_EVENT[0]	gpio4.IO[12]	epdc.BDR[0]	sim_m.HSIZE[0]
115	I2C3_SDA	i2c3.SDA	uart5.RTS_B	can2.TX	csi1.HSYNC	sdma.EXT_EVENT[1]	gpio4.IO[13]	epdc.BDR[1]	sim_m.HSIZE[1]
116	I2C4_SCL	i2c4.SCL	uart5.RX	wdog4.WDOG_B	csi1.PIXCLK	usb.OTG1_ID	gpio4.IO[14]	epdc.VCOM[0]	sim_m.HSIZE[2]
117	I2C4_SDA	i2c4.SDA	uart5.TX	wdog4.WDOG_RST_B_DEB	csi1.MCLK	usb.OTG2_ID	gpio4.IO[15]	epdc.VCOM[1]	sim_m.HWRITE
118	ECSPI1_SCLK	ecspi1.SCLK	uart6.RX	**usdhc2.DATA4**	csi1.DATA[2]		gpio4.IO[16]	epdc.PWRCOM	sim_m.HREADYOUT
119	ECSPI1_MOSI	ecspi1.MOSI	uart6.TX	**usdhc2.DATA5**	csi1.DATA[3]	gpc.OBS0	gpio4.IO[17]	epdc.PWRSTAT	tpsmp.CLK
120	ECSPI1_MISO	ecspi1.MISO	uart6.RTS_B	**usdhc2.DATA6**	csi1.DATA[4]	gpc.OBS1	gpio4.IO[18]	epdc.PWRIRQ	tpsmp.HDATA_DIR
121	ECSPI1_SS0	ecspi1.SS0	uart6.CTS_B	**usdhc2.DATA7**	csi1.DATA[5]	gpc.OBS2	gpio4.IO[19]	epdc.PWRCTRL[3]	tpsmp.HTRANS[0]
122	ECSPI2_SCLK	ecspi2.SCLK	uart7.RX	**usdhc1.DATA4**	csi1.DATA[6]	lcdif.DATA[13]	gpio4.IO[20]	epdc.PWRCTRL[0]	tpsmp.HTRANS[1]
123	ECSPI2_MOSI	ecspi2.MOSI	uart7.TX	**usdhc1.DATA5**	csi1.DATA[7]	lcdif.DATA[14]	gpio4.IO[21]	epdc.PWRCTRL[1]	tpsmp.HDATA[0]
124	ECSPI2_MISO	ecspi2.MISO	uart7.RTS_B	**usdhc1.DATA6**	csi1.DATA[8]	lcdif.DATA[15]	gpio4.IO[22]	epdc.PWRCTRL[2]	tpsmp.HDATA[1]
125	ECSPI2_SS0	ecspi2.SS0	uart7.CTS_B	**usdhc1.DATA7**	csi1.DATA[9]	lcdif.RESET	gpio4.IO[23]	epdc.PWRWAKE	tpsmp.HDATA[2]
126	SD1_CD_B	**usdhc1.CD_B**		uart6.RX	ecspi4.MISO	flextimer1.CH[0]	gpio5.IO[0]	ccm.CLKO1	tpsmp.HDATA[3]
127	SD1_WP	**usdhc1.WP**		uart6.TX	ecspi4.MOSI	flextimer1.CH[1]	gpio5.IO[1]	ccm.CLKO2	tpsmp.HDATA[4]
128	SD1_RESET_B	**usdhc1.RESET_B**	sai3.MCLK	uart6.RTS_B	ecspi4.SCLK	flextimer1.CH[2]	gpio5.IO[2]	ccm.OUT0	tpsmp.HDATA[5]
129	SD1_CLK	**usdhc1.CLK**	sai3.RX_SYNC	uart6.CTS_B	ecspi4.SS0	flextimer1.CH[3]	gpio5.IO[3]	ccm.OUT1	tpsmp.HDATA[6]
130	SD1_CMD	**usdhc1.CMD**	sai3.RX_BCLK		ecspi4.SS1	flextimer2.CH[0]	gpio5.IO[4]	ccm.OUT2	tpsmp.HDATA[7]
131	SD1_DATA0	**usdhc1.DATA0**	sai3.RX_DATA[0]	uart7.RX	ecspi4.SS2	flextimer2.CH[1]	gpio5.IO[5]	ccm.EXT_CLK1	tpsmp.HDATA[8]
132	SD1_DATA1	**usdhc1.DATA1**	sai3.TX_BCLK	uart7.TX	ecspi4.SS3	flextimer2.CH[2]	gpio5.IO[6]	ccm.EXT_CLK2	tpsmp.HDATA[9]
133	SD1_DATA2	**usdhc1.DATA2**	sai3.TX_SYNC	uart7.CTS_B	ecspi4.RDY	flextimer2.CH[3]	gpio5.IO[7]	ccm.EXT_CLK3	tpsmp.HDATA[10]
134	SD1_DATA3	**usdhc1.DATA3**	sai3.TX_DATA[0]	uart7.RTS_B	ecspi3.SS1	flextimer1.PHA	gpio5.IO[8]	ccm.EXT_CLK4	tpsmp.HDATA[11]
135	SD2_CD_B	**usdhc2.CD_B**	enet1.MDIO	enet2.MDIO	ecspi3.SS2	flextimer1.PHB	gpio5.IO[9]	sdma.EXT_EVENT[0]	tpsmp.HDATA[12]
136	SD2_WP	**usdhc2.WP**	enet1.MDC	enet2.MDC	ecspi3.SS3	usb.OTG1_ID	gpio5.IO[10]	sdma.EXT_EVENT[1]	tpsmp.HDATA[13]
137	SD2_RESET_B	**usdhc2.RESET_B**	sai2.MCLK	usdhc2.RESET	ecspi3.RDY	usb.OTG2_ID	gpio5.IO[11]		tpsmp.HDATA[14]
138	SD2_CLK	**usdhc2.CLK**	sai2.RX_SYNC	mqs.RIGHT	gpt4.CLK		gpio5.IO[12]		tpsmp.HDATA[15]
139	SD2_CMD	**usdhc2.CMD**	sai2.RX_BCLK	mqs.LEFT	gpt4.CAPTURE1	sim2.PORT1_TRXD	gpio5.IO[13]		observe_mux.OUT[0]
140	SD2_DATA0	**usdhc2.DATA0**	sai2.RX_DATA[0]	uart4.RX	gpt4.CAPTURE2	sim2.PORT1_CLK	gpio5.IO[14]		observe_mux.OUT[1]
141	SD2_DATA1	**usdhc2.DATA1**	sai2.TX_BCLK	uart4.TX	gpt4.COMPARE1	sim2.PORT1_RST_B	gpio5.IO[15]		observe_mux.OUT[2]
142	SD2_DATA2	**usdhc2.DATA2**	sai2.TX_SYNC	uart4.CTS_B	gpt4.COMPARE2	sim2.PORT1_SVEN	gpio5.IO[16]		observe_mux.OUT[3]
143	SD2_DATA3	**usdhc2.DATA3**	sai2.TX_DATA[0]	uart4.RTS_B	gpt4.COMPARE3	sim2.PORT1_PD	gpio5.IO[17]		observe_mux.OUT[4]
144	SD3_CLK	**usdhc3.CLK**	rawnand.CLE	ecspi4.MISO	sai3.RX_SYNC	gpt3.CLK	gpio6.IO[0]		tpsmp.HDATA[16]

- Each GPIO supports up to 8 alternative mux options, very flexible for customer.

i.MX 7: Enablement

i.MX Overview: Enablement

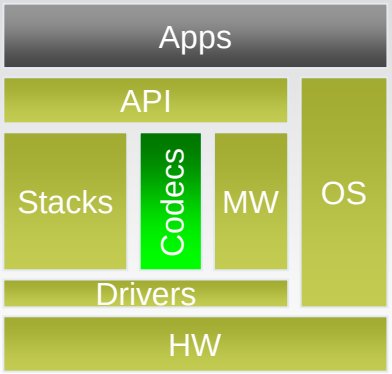
Hardware Platform

PDKs, EVKs, SABRE, Quick Start Board

- Ease of Use – BSP and demo images, development environment build demonstration, video tutorials, schematic and layout, documentation
- Ranging from $149 development board to $999 full reference platform.

Full Hardware evaluation and Development Platforms

+ Software



- Full-featured, scalable, optimized and proven OS – Linux, Windows, Android
- Software codecs for video, audio, graphics and communications.
- Product-worthy software for reference platforms and product development

Complete software package to streamline software development

+ Ecosystem

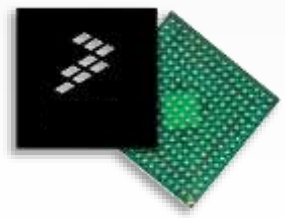
- Tool chains
- Software – RTOS, OS, codecs, middleware/applications
- Hardware – embedded board solutions
- Design services
- System integrators
- Training

Technology alliances for building smarter, better

www.imxcommunity.org

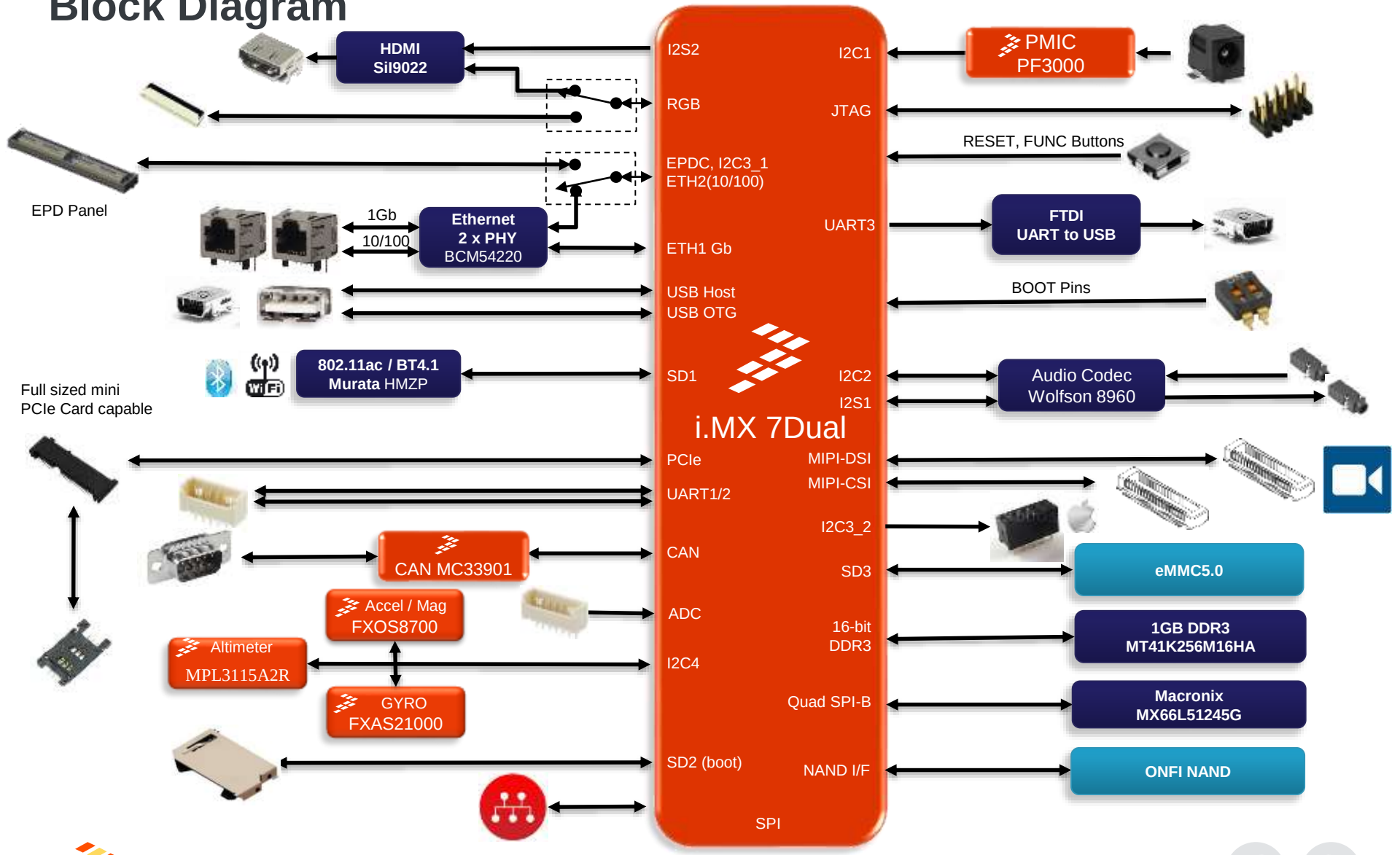
Freescale Full Solutions

i.MX 7 Family Processors	+	PF3000 PMIC	+	Sensors	=	i.MX 7 SABRE Development Platform
• **1 GHz** ARM® Cortex™-A7 • **NEON™ coprocessor** • ARM® Cortex™-M4, • **Electronic Paper Display (EPD)** in addition to LCD. • Targeting a broad range of applications including many **low power**, **portable** consumer devices		• Integration of Freescale's PMIC chip set with i.MX processor for optimization of power efficiency and software/hardware integration • One-stop customer service and support during development phase to enable the design process		• MEMS gyroscopes for reliable sensing and measuring • Magnetometers: measuring the magnitude and direction of magnetic fields • Pressure Sensing Devices, composed of single silicon, piezoresistive devices		Development platform: • Single-board evaluation kit • Linux® and Android™ Board Support Packages are available through Freescale



A Single Solution for Streamlined Performance

i.MX 7 Platform Block Diagram



Populated by default

Footprint only, unpopulated by default

i.MX 7: SABRE Platform Planned Key Features

Processor
- Freescale i.MX 7Dual
  - Dual Cortex™-A7 @1GHz
  - 512KB L2$
- Freescale PF3000 PMIC

Memory
- 1 GB DDR3
- eMMC5.0 footprint
- QuadSPI Flash
- SD/MMC socket
- NAND footprint

Display/Camera Connectors
- HDMI
- Parallel LCD
- MIPI-DSI
- Electronic Paper Display
- MIPI-CSI (camera)

Wireless
- Wi-Fi (802.11ac) onboard
- BT4.0 / BLE onboard

Audio
- Audio HP Jack
- External speaker connection

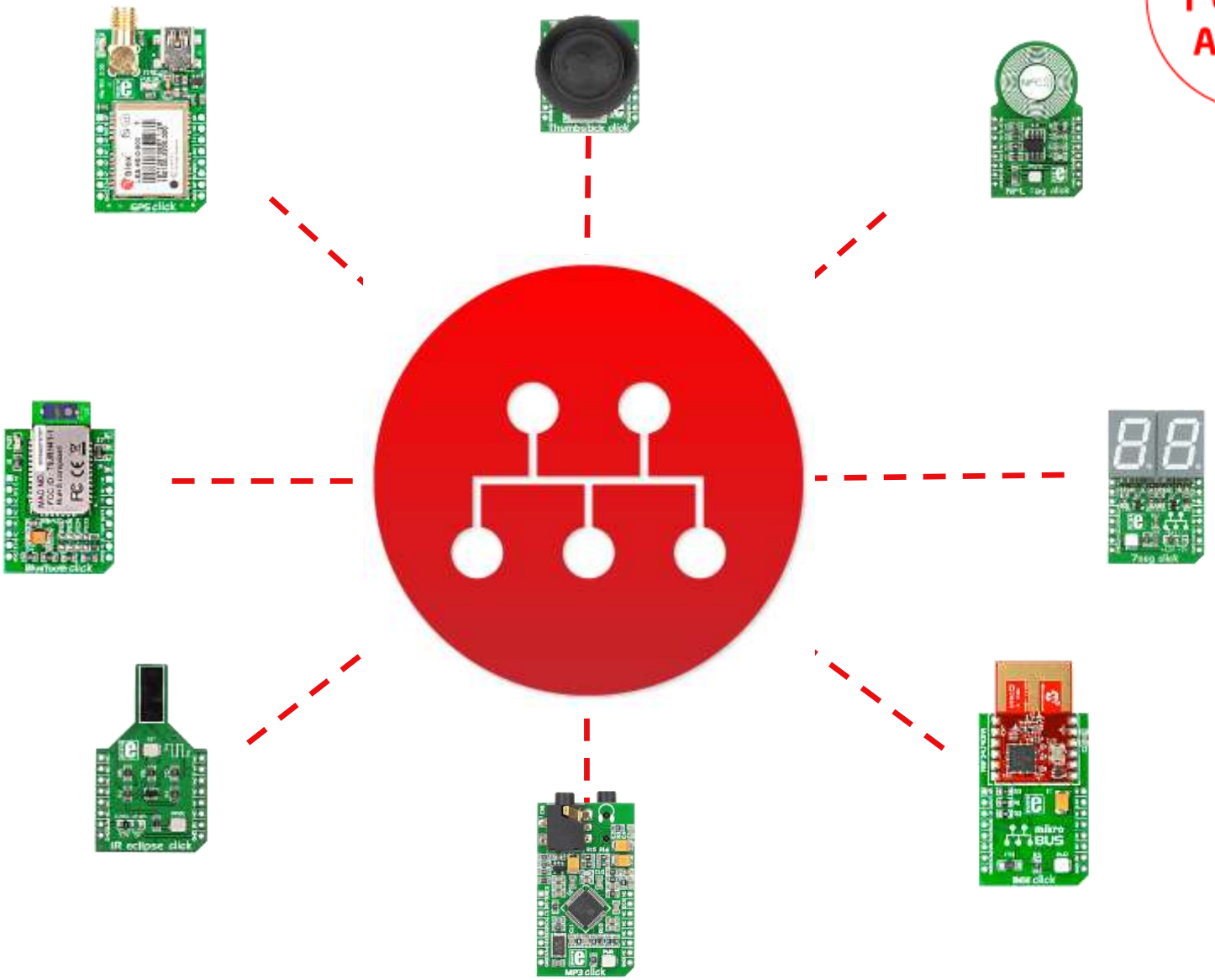
Connectivity
- USB Host connectors
- microUSB OTG connector
- ETH (1Gbit) Receptacle
- ETH (10/100) Receptacle
- Full Mini PCIe socket
- SIM Card slot
- CAN (DB-9)
- GPIO
- MFi Module support
- MikroBus expander

Debug
- JTAG connector
- UART via USB

Sensors
- **FXOS8700** three-axis digital accelerometer/Magnetometer
- **MPL3115A2R** Altimeter/Pressure sensor
- **FXAS21000** three-axis digital Gyroscope

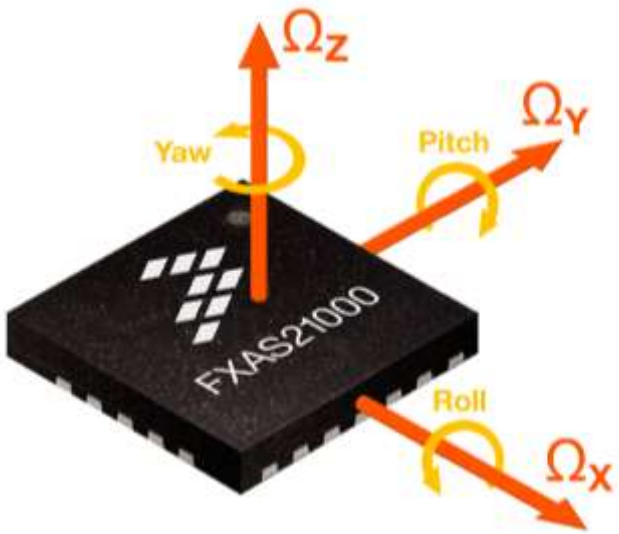
Tools & OS Support
- Linux®
- Android™
- FreeRTOS

mikroBus Expansion Boards



Sensor Type: Gyroscopes

- MEMS gyroscopes reliably sense and measure the angular rate of an object, under complex and severe operating conditions
- They enable both user interface and image stabilization applications
- *When you see an accelerometer, think gyroscope too!*



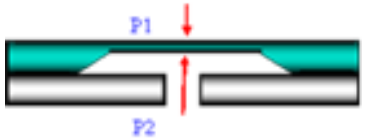
Sensor Type: Magnetometers

- Magnetometers: instrument for measuring the magnitude and direction of a magnetic field
- When combined with an accelerometer to compensate the tilt, it is primarily used as an eCompass. It allows map alignment while moving.

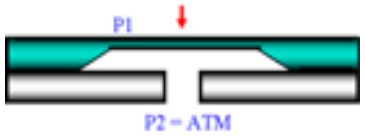
Sensor Type: Pressure Sensors

Devices are composed of single silicon, piezoresistive devices capable of monitoring processes in the industrial, medical, automotive, and avionics industries. Pressure sensors are composed of the following reference designs:

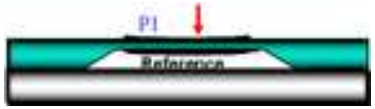
- Differential: difference in pressure between two points is measured as pressure is applied to both sides of the die/sensing element



- Gauge: bottom side is exposed to the atmosphere, while pressure is applied to top of die



- Absolute: pressure is applied to the top of the die while the bottom of the die is a vacuum-sealed reference



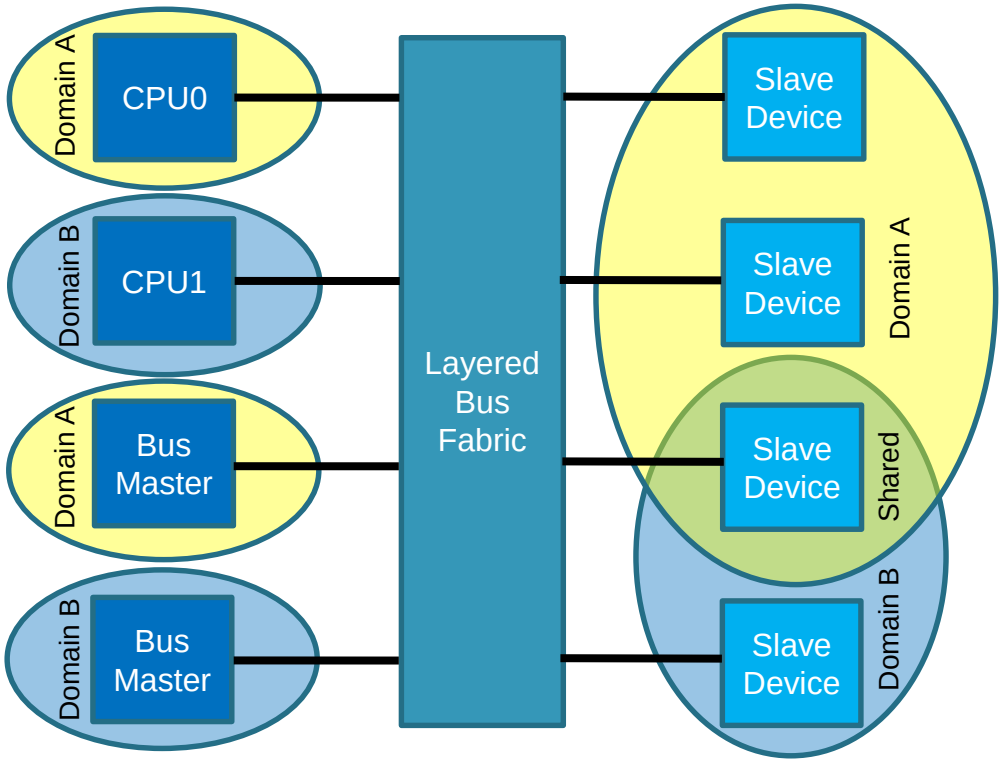
i.MX 7: Software

yocto PROJECT

i.MX HMP Architecture

Resource Domains

- Use ***resource domains*** to partition the system
  - Masters are assigned to a resource domain
  - Slave access permissions are defined per resource domain
  - Memory region access permissions are defined per resource domain
- Sideband signals of bus fabrics carry resource domain ID



Inter Processor Communication (IPC) Hardware Summary

Hardware	Features
Messaging Unit (MU)	Mailbox registers to send/receive messages Provided interprocessor interrupts
SEMA4	Hardware-based general-purpose semaphore module
Shared Memory	Bus topology allows shared memory RDC and CSU can provide memory protection/isolation
Exclusive Access	ARMv7-A and ARMv7-M defines exclusive access instructions (LDREX/STREX)

i.MX 7: Debug Approach

- The architecture will support both Cortex-M4 and Cortex-A7 debug.
- i.MX 7Dual will have one DAP block where user will be able to access both Cortex-M4 and Cortex-A7 through a standard JTAG interface.
  - automatically detects the components in the whole debug system. .

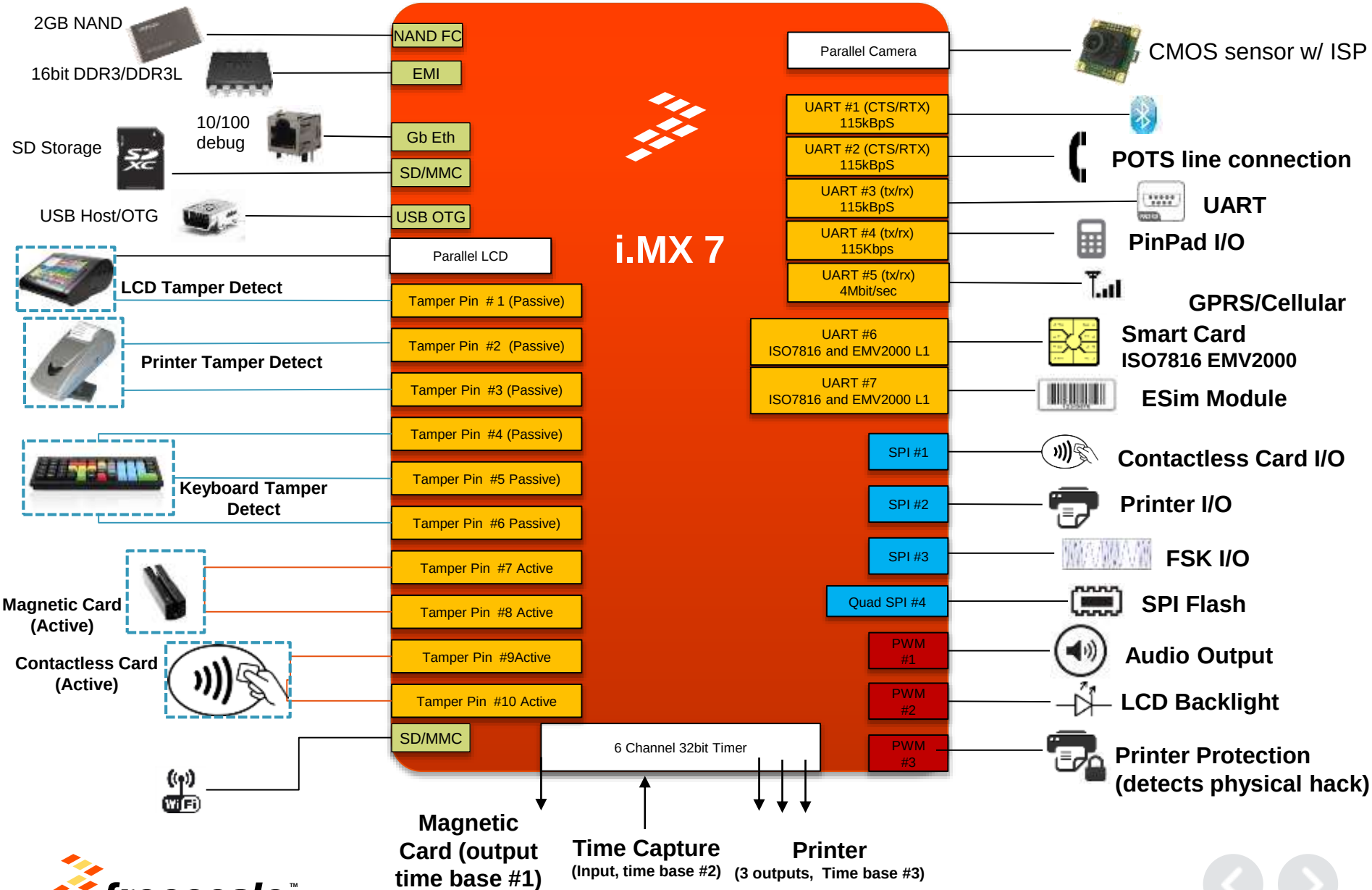
i.MX 7: EPD Controller

i.MX 7: EPD Feature Comparisons

Feature	i.MX 508	i.MX 6SL	i.MX 7Dual
Max Resolution	2048x1536@106Hz	2332x1650@106Hz	2332x1650@106Hz
Pixel Depth	Up to 5-bit	Up to 5-bit	Up to 5-bit
LUT Entry	16	64 or 16	64
LUT Index	14-bit	14-bit	**16-bit**
LUT Memory	64KB	64KB	**128KB**
Histogram Statistic based on Update Buffer	Yes	Yes	Yes
Histogram Statistic based on Update Pixel	No	Yes	Yes
Collision Detection	Yes	Yes	Yes
Dry-Run Mode For Collision Detection	No	Yes	Yes
RGB656 to RGBW4444 Conversion	No	Yes	Yes
CFA for Color Panel	No	Yes	Yes
E-INK Gen-I Waveform Processing in HW	Yes	Yes	Yes
E-INK Gen-II Waveform Processing (REAGL/-D) in HW	No	No	**Yes**
Programmable Engine for Waveform Processing	No	No	**Yes**
Cortex M4 for Waveform Processing	No	No	**Yes**
HW Dithering Engine	No	No	**Yes**
Per-Pixel Update Support	No	No	**Yes**

i.MX 7: Security

Point of Sale Use Case– i.MX 7



PRELIMINARY

i.MX 7 Security HW Comparison with i.MX 25

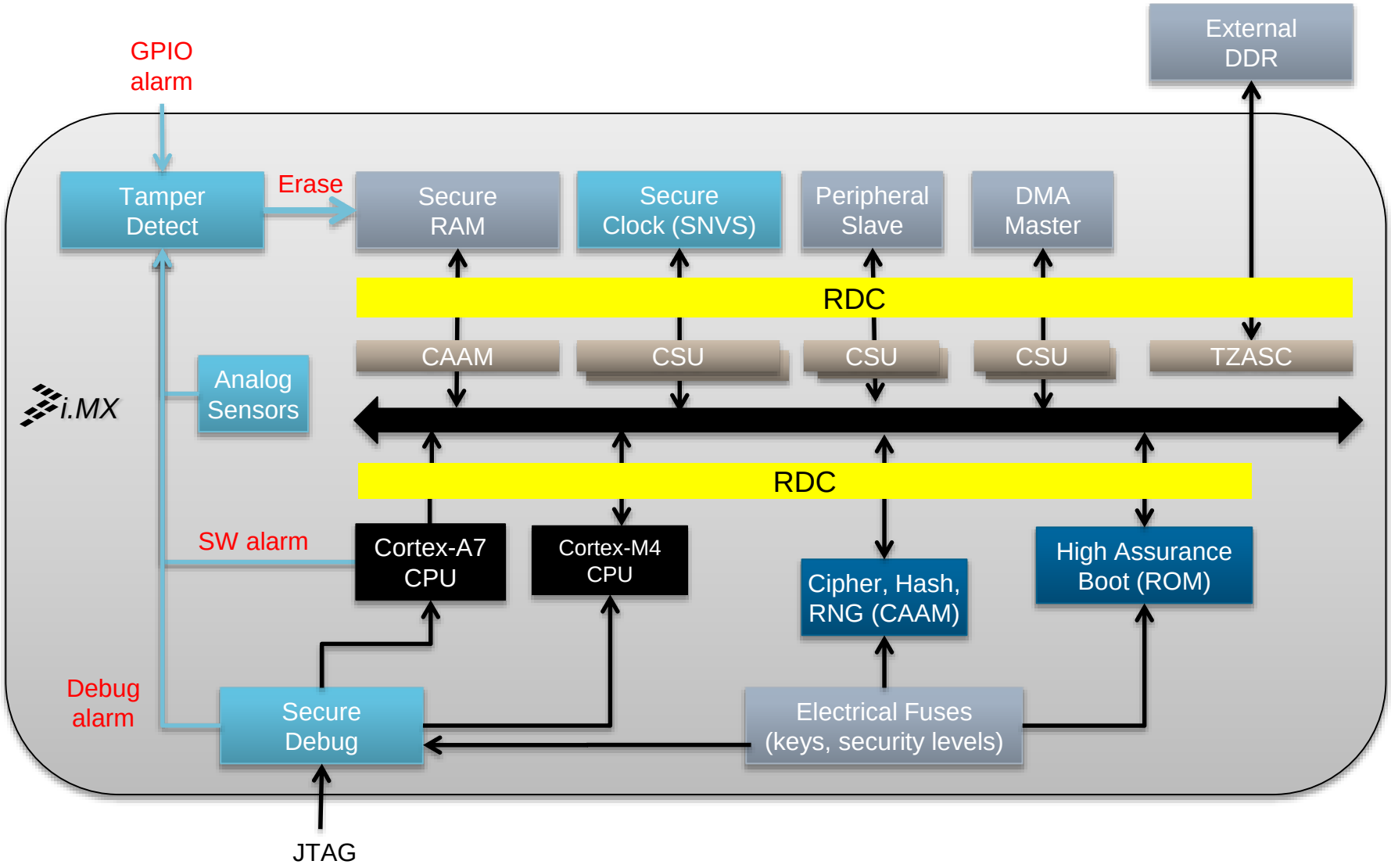
Feature	i.MX25	i.MX 7
Trusted Execution	Peripheral access control (CSU)	TrustZone, (**ARM Cortex-A7**) Peripheral access control (CSU, **RDC**) Memory access control (ARM TZASC, **RDC**) Interrupt separation (ARM GIC) Secure storage separation (CAAM/SNVS) Cryptographic separation (CAAM)
High Assurance Boot	HABv3 Based Secure boot	**HABv4.2 Secure boot with 256-bit security**
External Tamper Detection	Tamper Input GPIO	**Dedicated Tamper Inputs both passive and active for wire mesh (10 pins / 5 active cuircits).**
Internal Tamper Sensing	Voltage, Temp, Freq Monitoring	Voltage, Temp, Freq Monitoring Customer programmable trim settings
Encrypted boot	None	**Authenticated + Encrypted Boot**
Secure Storage	On-chip zeroizable 2kB Secure RAM	On-chip zeroizable **8x4kB Secure RAM** Off-chip key/data blobs AES-256 master key (CAAM/SNVS)
True Random Number Gen	Yes	Yes. Designed to be compliant with NIST SP800-90A and includes a hardware entropy source. NISTI/BSI >2015 to comply with PCI
Cryptographic Accelerators	None	**Asymmetric: RSA (up to 4096)** **ECDSA** Symmetric: AES-128/256, DES, 3DES, ARC4 Hash & HMAC: MD5, SHA-1, SHA-224/256 **256-bit security** (CAAM)
Secure Clock	SNVS	SNVS
DPA Protection	None	AES, 3DES
Secure Debug	Full or Controlled Disable (3 modes)	Full or Controlled Disable (3 modes)
Device Configuration	Open, Closed, Field Return	Open, Closed, Field Return

i.MX Trust Architecture Deployment

Feature	i.MX 6x	i.MX 7x
High Assurance Boot	V4	V4
Secure Storage	✓	✓
Hardware RNG	✓	✓
Secure Clock	✓	✓
Secure Debug	✓	✓
Tamper Detection	✓	✓
AES, SHA, 3DES	✓	✓
Elliptic Curve, RSA (upto 4096 bits) Accelerator		✓
Encrypted Boot		✓
Manufacturing Protection		✓

* External Digital Tamper only monitored when main power is supplied.

i.MX7x Security Architecture – Overview



i.MX 7 Series – Security Options

- HW Cryptographic Accelerators 
  - True + Pseudo random number generator
  - Symmetric: AES-128, AES-256, 3DES, ARC4,
  - Asymmetric: RSA4096, ECDSA
  - Message Digest & HMAC: SHA-1, SHA-2, SHA-256, MD-5

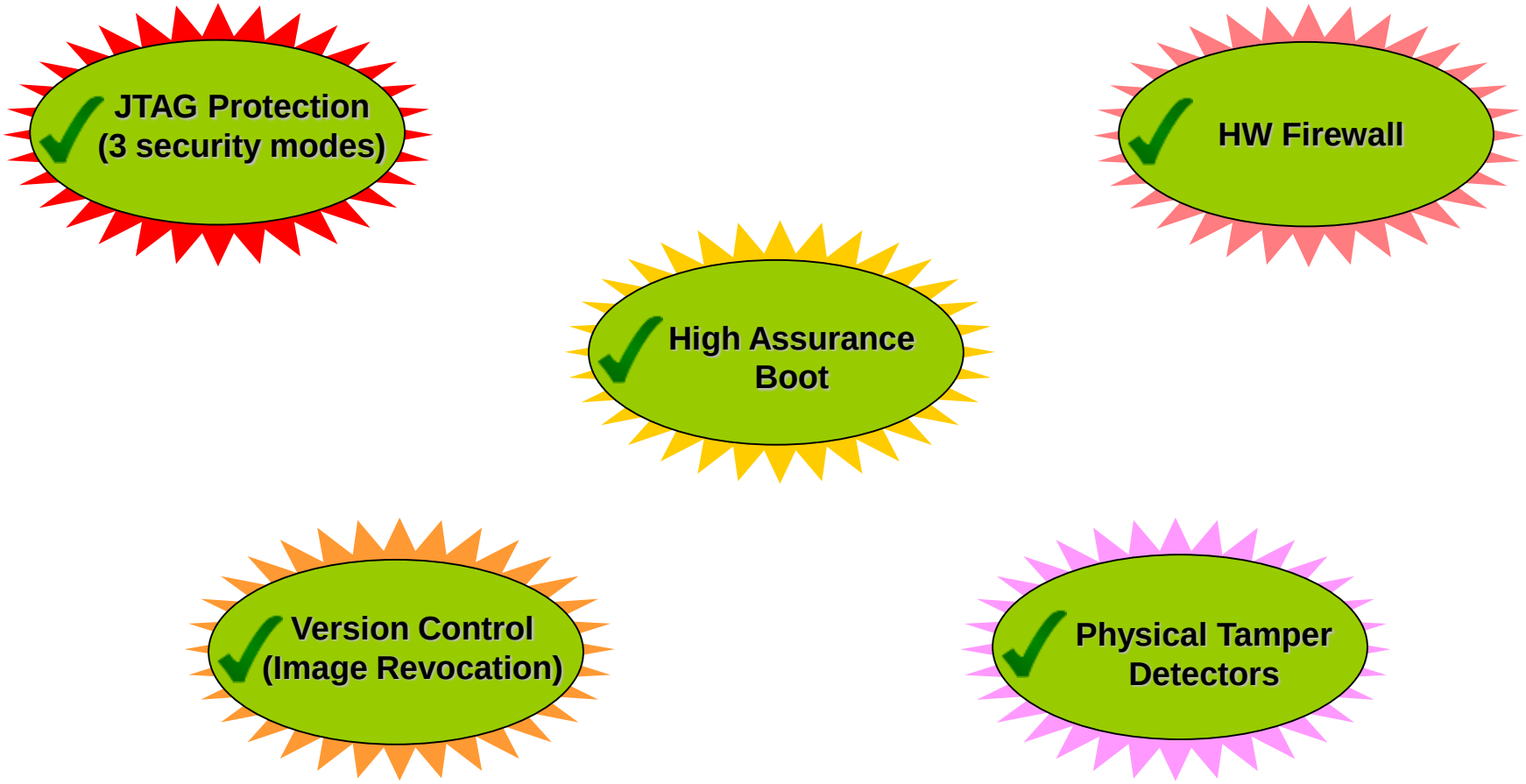
- High Assurance Boot: 
  - Security library embedded in tamper-proof on-chip ROM
  - Authenticated boot: protect against unauthorized SW
    - Verify SW signature during boot
    - RSA-1024/2048/3072/4096 keys anchored to OTP fingerprint (SHA-256)
  - Run every time i.MX is reset
  - Image Version Control (on-chip OTP-based)
  - Customer programs the keys and enables Secure Boot on their line

i.MX 7 Series – Additional Security Options

- Secure JTAG: 
  - Configurable protection against unauthorised JTAG manipulation
  - Three security levels + complete JTAG disable
- Secure Real-Time Clock 
  - On-chip, self-powered real-time clock
- Physical Tamper Detection 
  - Wire-Mesh by combination of Passive/Active tamper.
    - Tamper detection of Covers, Keyboards, Pin Pads, Magnetic and touchless card readers.
      - Passive Tamper (max 10 inputs)
      - Active tampers (max 5 pairs)
      - HW and SW tamper response. (Zeroizable RAM/Secure Key erasure)
- Secure Storage: 
  - Programmable TrustZone protected region within On-chip RAM
  - Independent On-chip zeroizable Secure RAM (32 KB)
  - Off-chip storage protected using AES-256 and chip's unique HW-only key

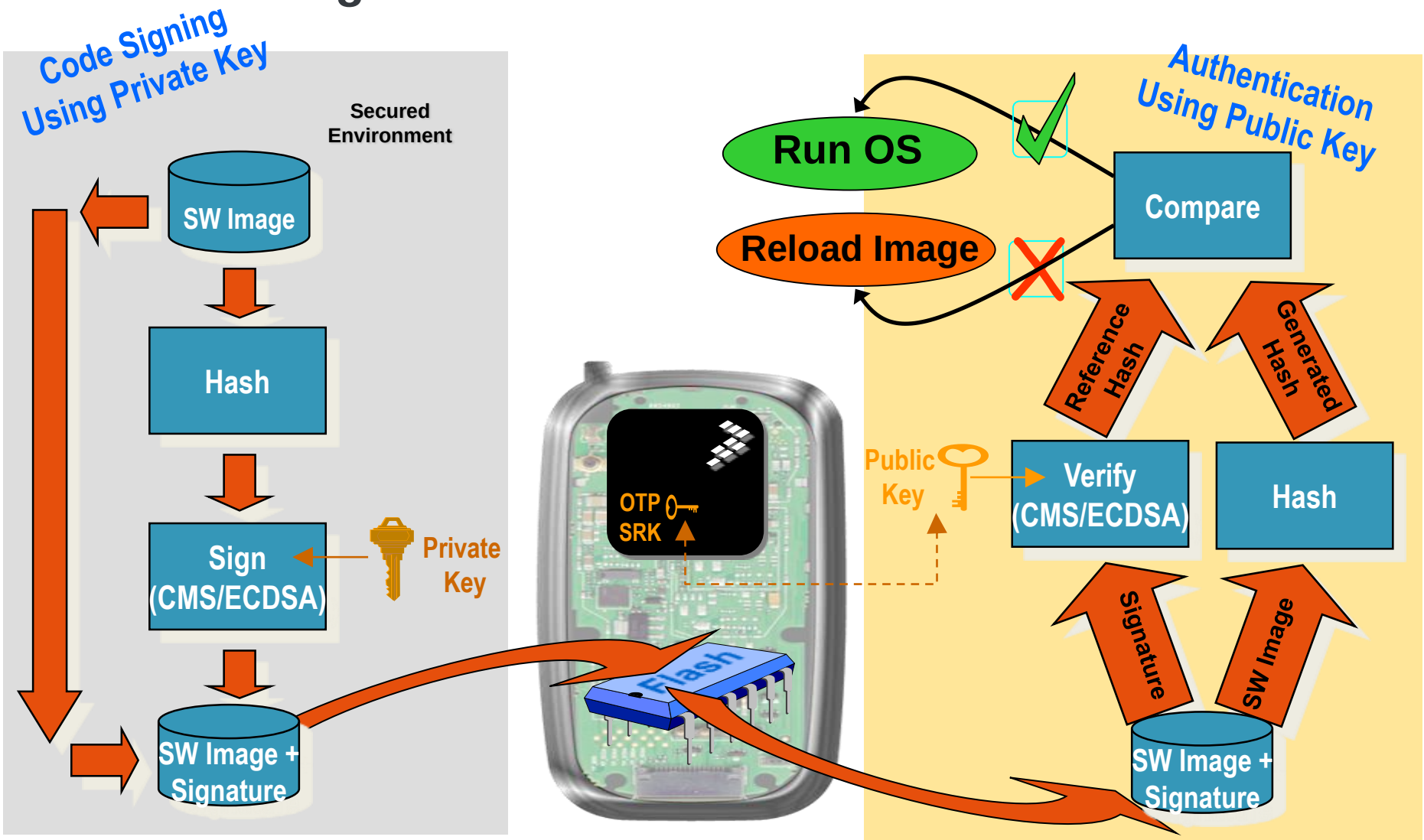
i.MX 7 Security Infrastructure

Common Security Attacks

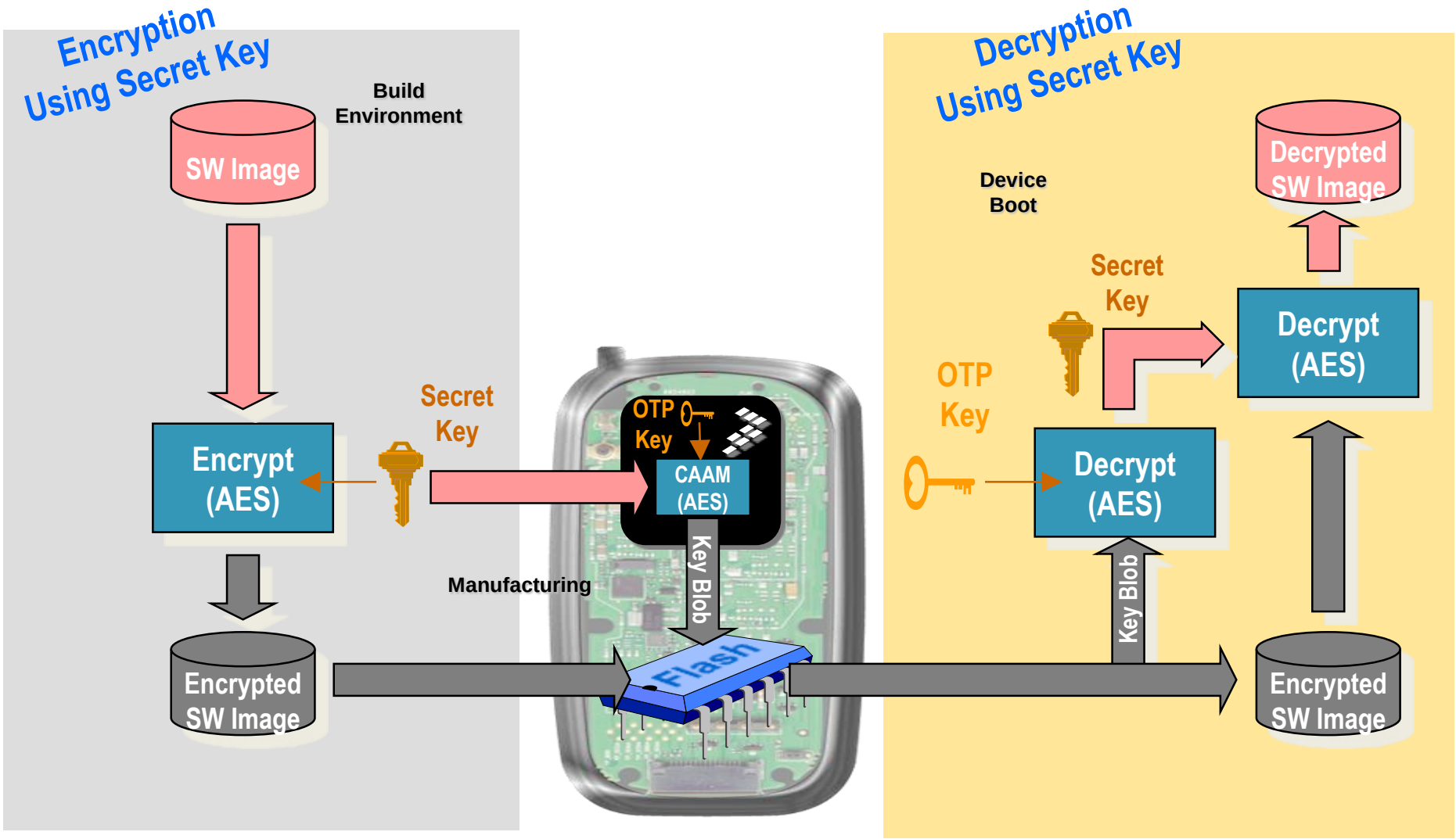


Secure Boot

Boot ROM: High Assurance Boot

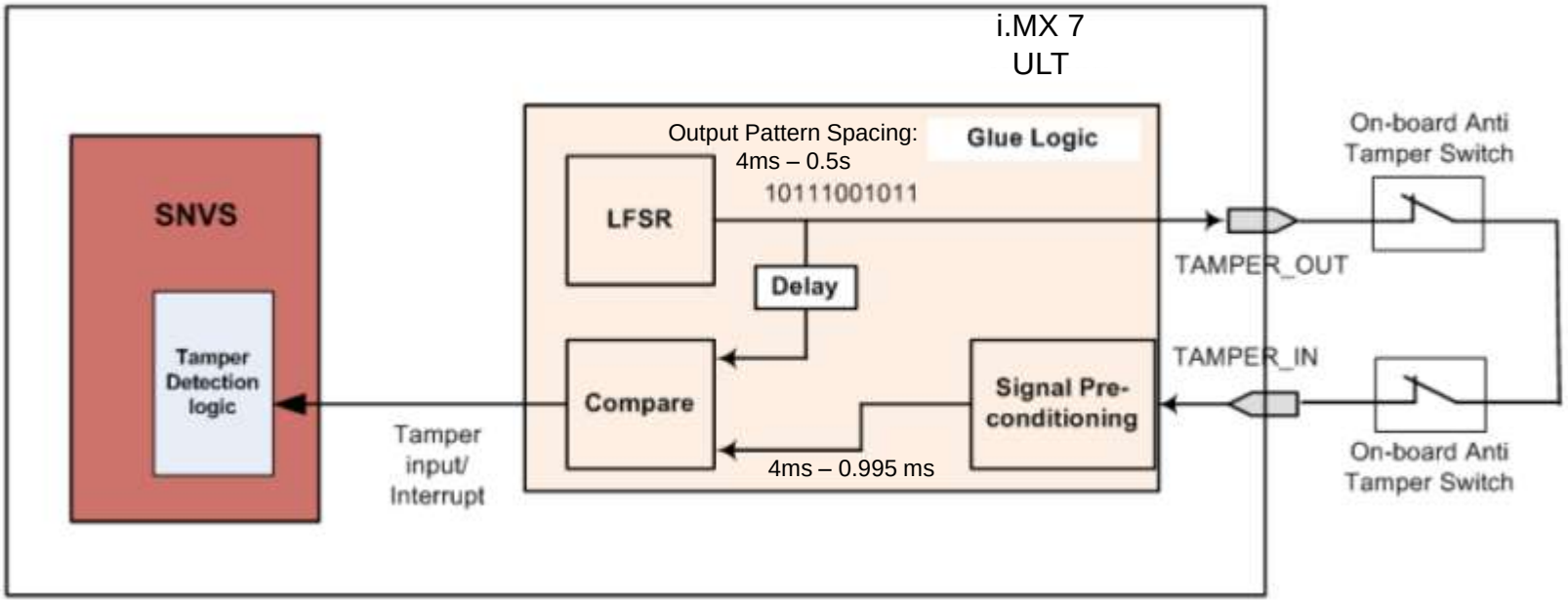


Boot ROM: High Assurance Boot – Encrypted



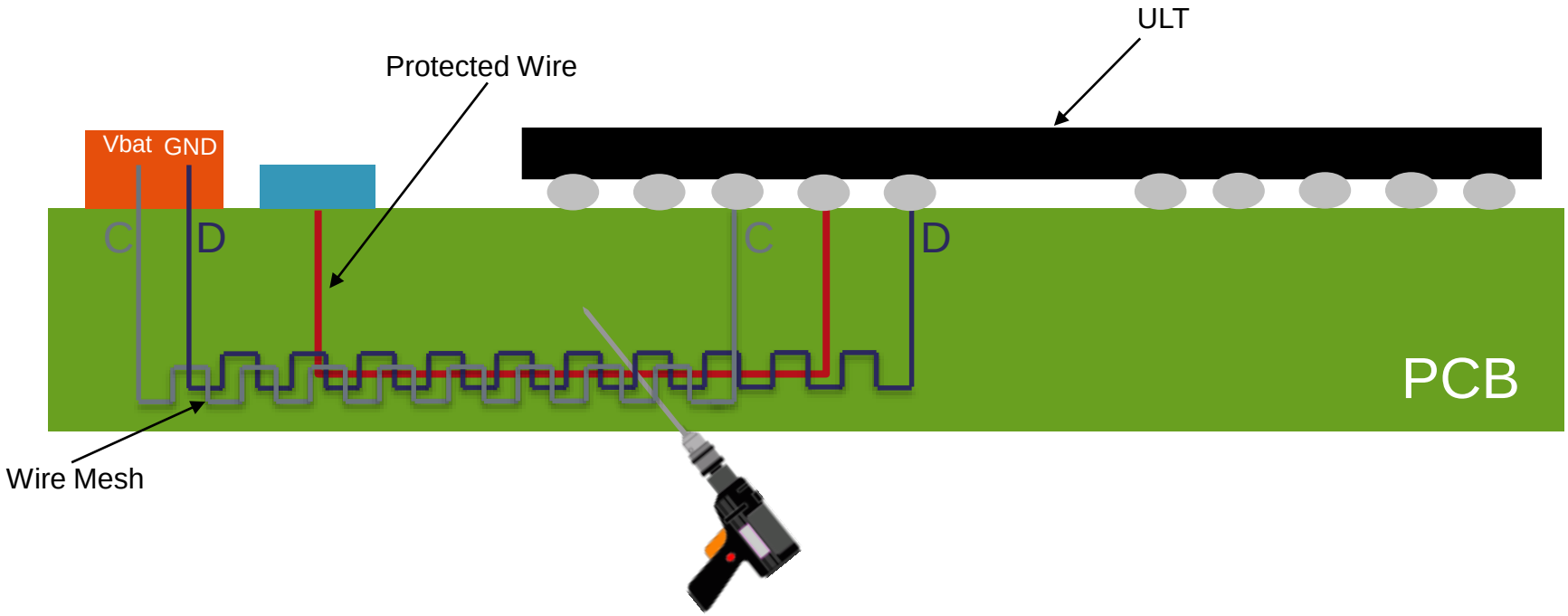
Tamper Detect

External Tamper Detection – PCI4.0 ComplianceTargeted



- **10 dedicated pins for active tamper detection**
  - Each pair of pins is used for active wire-mesh outputs/inputs that provides up to 5 active meshes
- **Pattern generated via 16-bit LFSR. Configurable generator polynomial**
- **Glitch filter per active tamper input pin.**
- **LFSR seed randomized by scrambling internal design signals.**

Differential PCB Tamper Detection (Wire Mesh)



- **SNVS module will detect Tamper and initiate key erasure when:**
  - C is disconnected (floating)
  - D is disconnected (floating)
  - C and D are short-circuited

Sensitive Pins

- Sensitive Pins located at least 3 Row deep within BGA package
  - Include All passive tamper pins
  - Include All Active tamper pins
  - Include internal
  - Battery Supply
  - Others

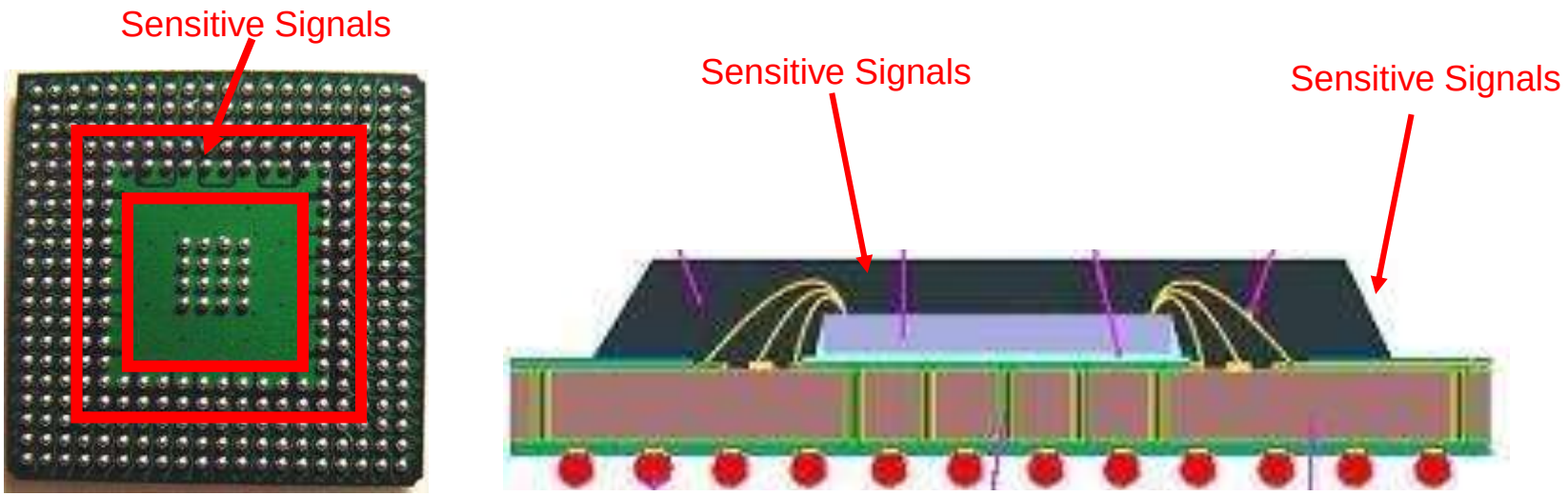


Image does not represent actual i.MX 7 ULT packaging

Analog Tamper Sensors

- Voltage Sensor Trim Range

- Temperature Sensor Trim Range

- SRTC Frequency Sensor Trim Ranges

www.Freescale.com