An Overview of the QorIQ T1040 Communications Processor

APF-SNT-T1359

John Chang

Chun Chang | Application Engineer

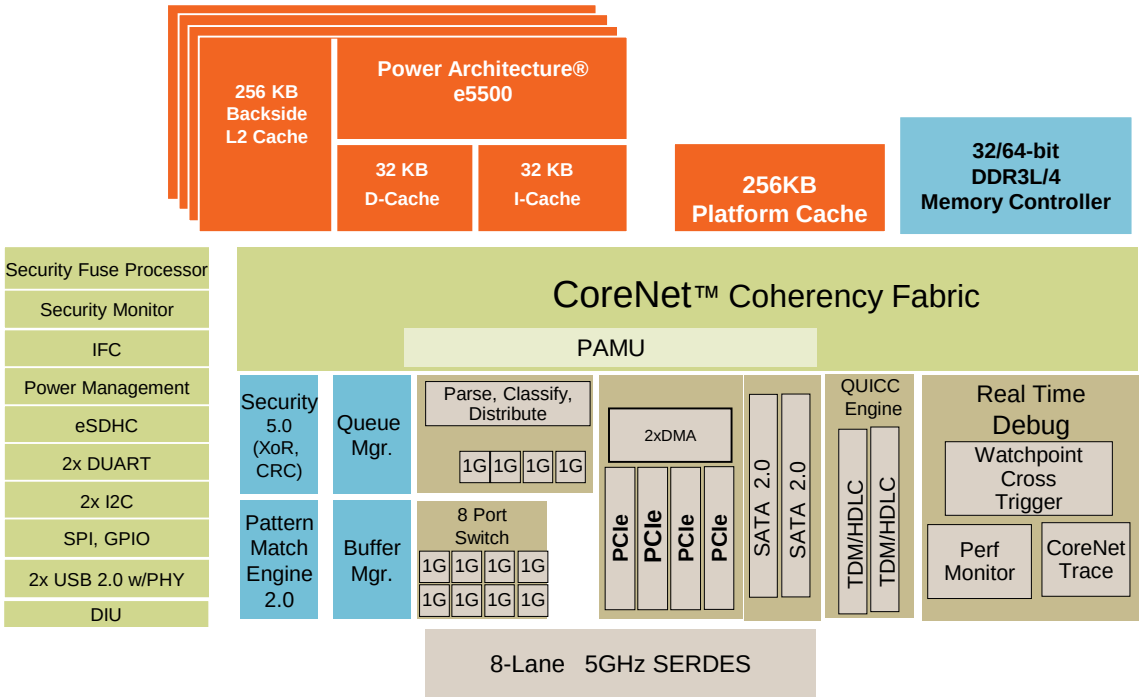
MAY.2015

External Use

Agenda

- Introduction
  - Block Diagram
  - Market Trend
- QorIQ T1040 processor features
  - Ethernet Switch
  - Serdes
  - Clocking
  - Power Management
- Collaterals
- Summary

QorIQ T1040 Processor



Device

- 780-pin FC-PBGA package
- 23x23mm, 0.8mm pitch

Power targets

- Enable Convection cooled system design

Datapath Acceleration

- SEC- crypto acceleration
- PME- Reg-ex Pattern Matcher

Processor

- 4x e5500, 64b, up to 1.4GHz
- Each with 256KB backside L2 cache
- 256KB Shared Platform Cache w/ECC
- Supports up to 64GB addressability (36 bit physical addressing)

Memory Subsystem

- 32/64b DDR3L/4 Controller up to 1600MHz

CoreNet Switch Fabric

High Speed Serial IO

- 4x PCIe Gen2 (5Gbps) Controllers
- 2x SATA 2.0, 3Gbps
- 2x USB 2.0 with PHY

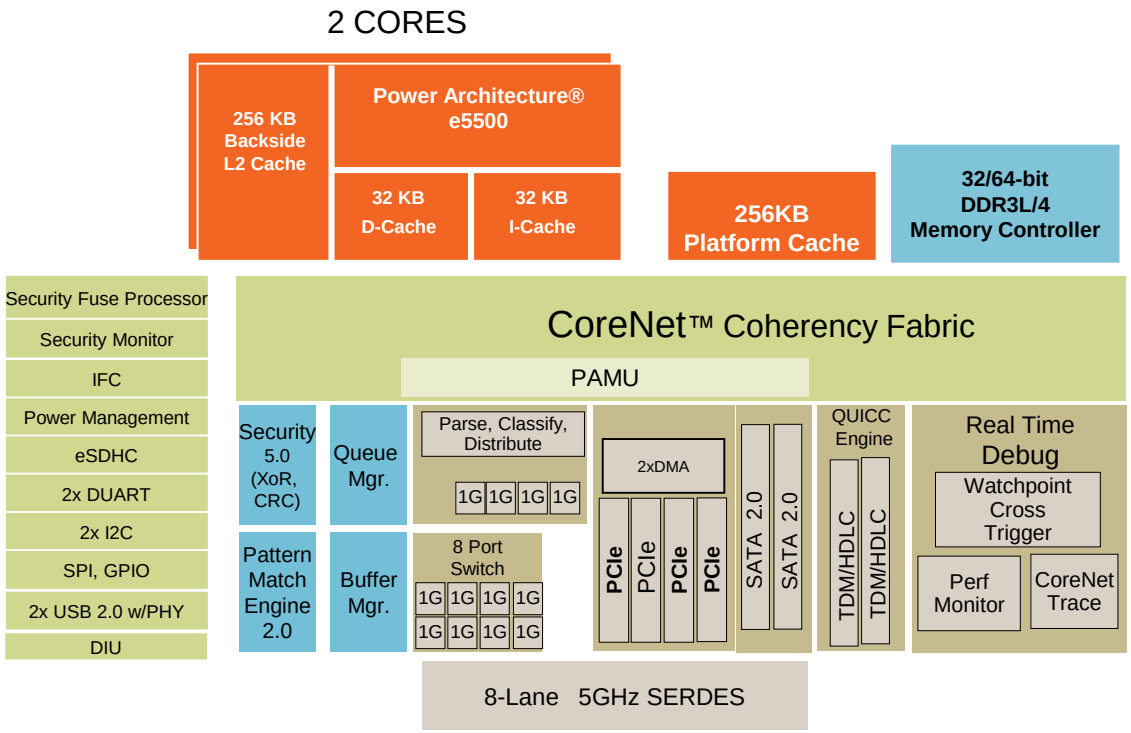
Network IO

- FMan packet Parse/Classify/Distribute
- Lossless Flow Control, IEEE 1588
- Up to 4x 10/100/1000 Ethernet Controllers
- **8-Port Gigabit Ethernet Switch**
- QUICC Engine
  - HDLC, 2x TDM

Green Energy Operation

- Fanless operation quad-core 1.4GHz
- Packet lossless deepsleep
  - Programmable wake-on-packet
  - Wake-on-timer/GPIO/USB/IRQ

QorIQ T1020 Processor



Device

- 780-pin FC-PBGA package
- 23x23mm, 0.8mm pitch

Power targets

- Enable Convection cooled system design

Datapath Acceleration

- SEC- crypto acceleration
- PME- Reg-ex Pattern Matcher

Processor

- 2x e5500, 64b, up to 1.4GHz
- Each with 256KB backside L2 cache
- 256KB Shared Platform Cache w/ECC
- Supports up to 64GB addressability (36 bit physical addressing)

Memory Subsystem

- 32/64b DDR3L/4 Controller up to 1600MHz

CoreNet Switch Fabric

High Speed Serial IO

- 4 PCIe Gen2 Controllers
- SATA 2.0, 3Gbps
- 2 USB 2.0 with PHY

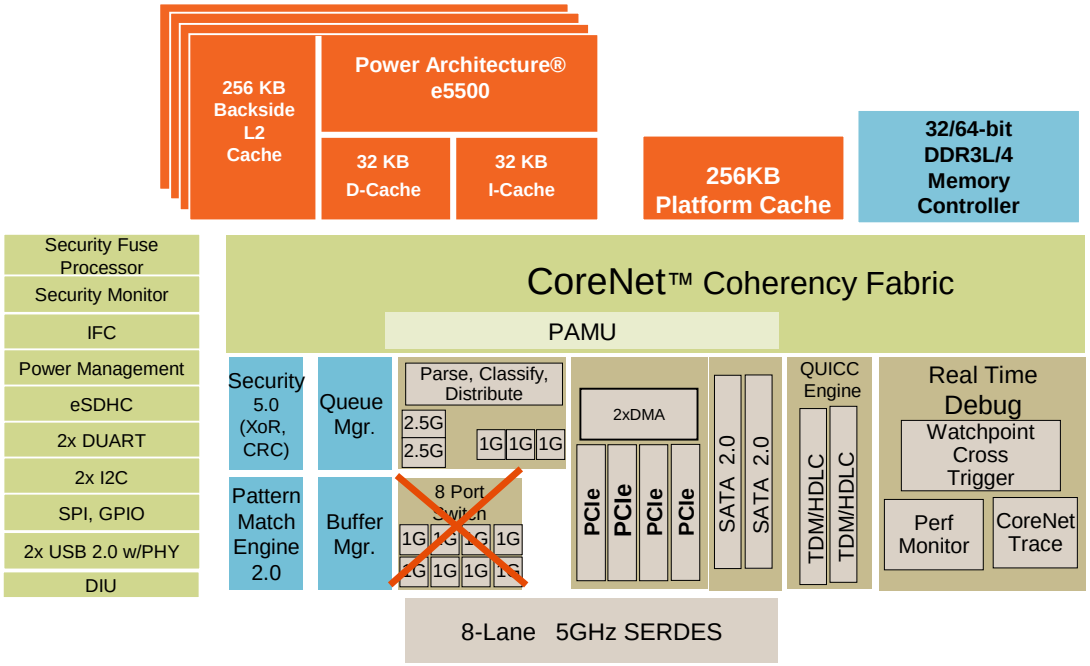
Network IO

- FMan packet Parse/Classify/Distribute
- Lossless Flow Control, IEEE 1588
- Up to 4x 10/100/1000 Ethernet Controllers
- **8-Port Gigabit Ethernet Switch**
- QUICC Engine
  - HDLC, 2x TDM

Green Energy Operation

- Fanless operation dual-core 1.4GHz
- Packet lossless deepsleep
  - Programmable wake-on-packet
  - Wake-on-timer/GPIO/USB/IRQ

QorIQ T1042 Processor



Device

- 780-pin FC-PBGA package
- 23x23mm, 0.8mm pitch

Power targets

- **Target Deep Sleep 150mW on special Part Numbers (1/2W AC System)**

Datapath Acceleration

- SEC- crypto acceleration
- PME- Reg-ex Pattern Matcher

Processor

- 4x e5500, 64b, up to 1.4GHz
- Each with 256 KB backside L2 cache
- 256KB Shared Platform Cache w/ECC
- Supports up to 64GB addressability (36 bit physical addressing)

Memory Subsystem

- 32/64b DDR3L/4 Controller up to 1600MHz

CoreNet Switch Fabric

High Speed Serial IO

- 4 PCIe Gen2 Controllers
- SATA 2.0, 3Gbps
- 2 USB 2.0 with PHY

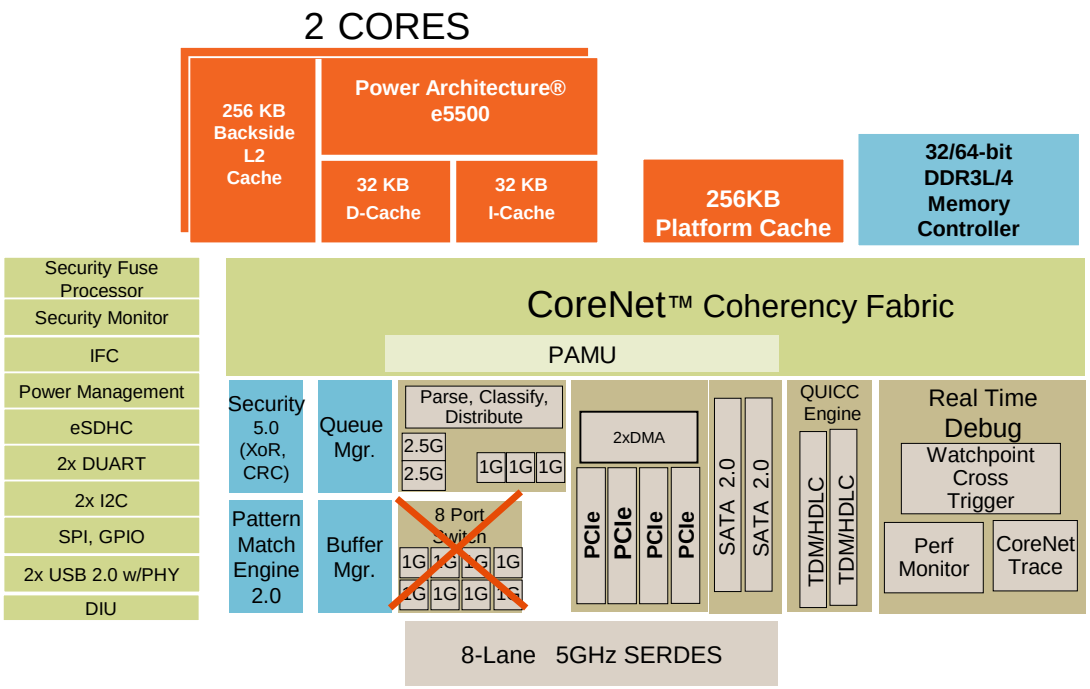
Network IO

- FMan packet Parse/Classify/Distribute
- Lossless Flow Control, IEEE 1588
- 5x 10/100/1000 Ethernet Controllers
- QUICC Engine
  - HDLC, 2x TDM

Green Energy Operation

- Fanless operation quad-core 1.4GHz
- Packet lossless deepsleep
  - Programmable wake-on-packet
  - Wake-on-timer/GPIO/USB/IRQ

QorIQ T1022 Processor



Device

- 780-pin FC-PBGA package
- 23x23mm, 0.8mm pitch

Power targets

- **Target Deep Sleep 150mW on special Part Numbers (1/2W AC System)**

Datapath Acceleration

- SEC- crypto acceleration
- PME- Reg-ex Pattern Matcher

Processor

- 2x e5500, 64b, up to 1.4GHz
- Each with 256 KB backside L2 cache
- 256KB Shared Platform Cache w/ECC
- Supports up to 64GB addressability (36 bit physical addressing)

Memory SubSystem

- 32/64b DDR3L/4 Controller up to 1600MHz

CoreNet Switch Fabric

High Speed Serial IO

- 4 PCIe Gen2 Controllers
- SATA 2.0, 3Gb/s
- 2 USB 2.0 with PHY

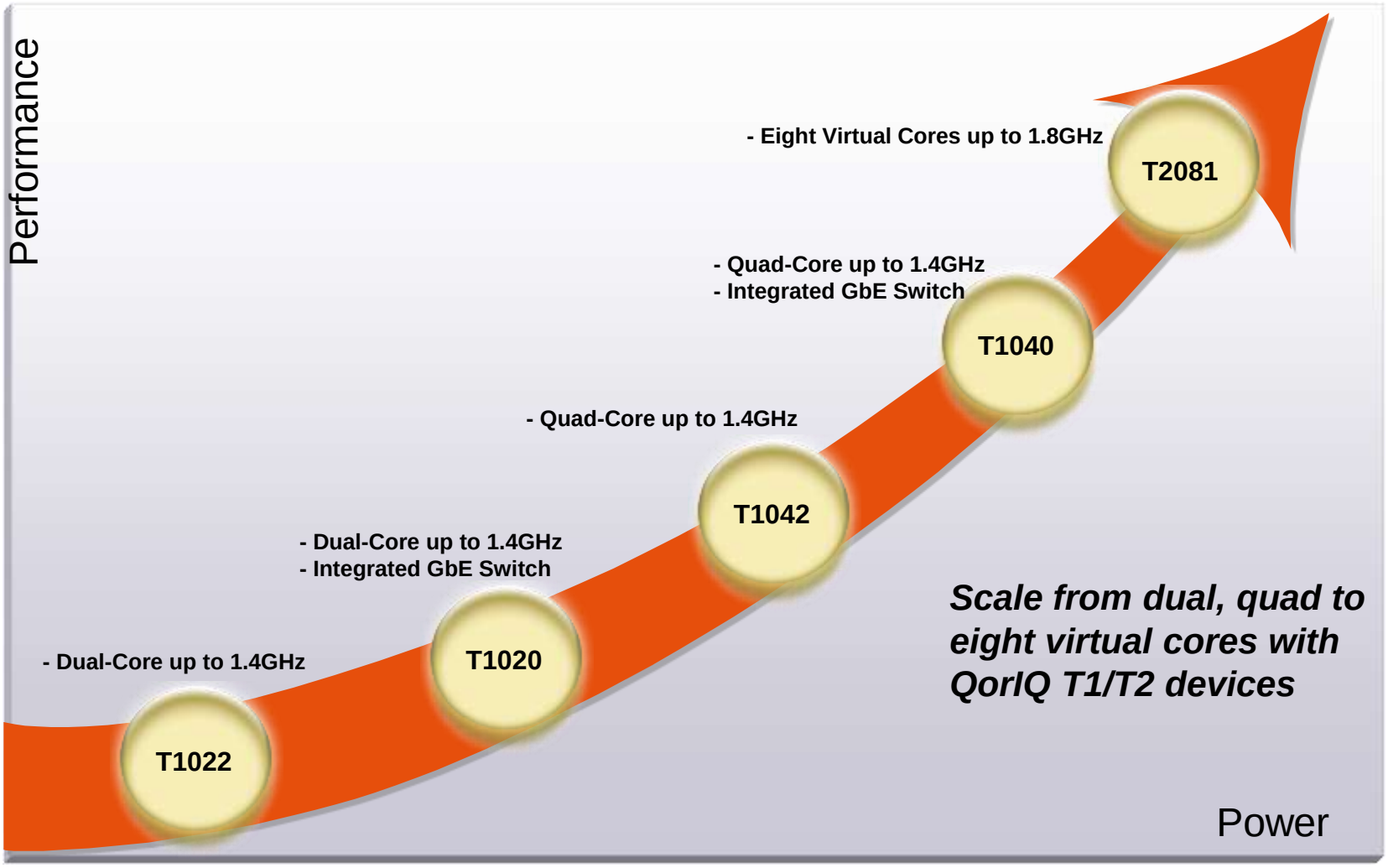
Network IO

- FMan packet Parse/Classify/Distribute
- Lossless Flow Control, IEEE 1588
- 5x 10/100/1000 Ethernet Controllers
- QUICC Engine
  - HDLC, 2x TDM

Green Energy Operation

- Fanless operation dual-core 1.4GHz
- Packet lossless deepsleep
  - Programmable wake-on-packet
  - Wake-on-timer/GPIO/USB/IRQ

QorIQ T Series: One of the Industry's Most Scalable, Pin-Compatible Communications Processor Family



Personality Comparison Chart

	P1020, P1011, P1021, P1012	P1022, P1013	T1020	T1022	T1040	T1042	T2081
CPU	1 to 2 x e500	1 to 2 x e500	2 x e5500	2 x e5500	4 x e5500	4 x e5500	4 x e6500/8 threads
	Up to 800MHz	Up to 1200MHz	1200-1400MHz	1200-1400MHz	1200-1400MHz	1200-1400MHz	1500 - 1800MHz
	32K I/D	32K I/D	32K I/D	32K I/D	32K I/D	32K I/D	32K I/D
L2 Cache	256KB	256KB	256KB/Core	256KB/Core	256KB/Core	256KB/Core	2MB shared
Platform Cache			256KB	256KB	256KB	256KB	512KB
DDR I/F Type/Width	DDR2/3	DDR2/3	DDR3L/4	DDR3L/4	DDR3L/4	DDR3L/4	DDR3/3L
	16/32-bit , 800MHz	32/64-bit, 800MHz	32/64-bit, 1600MT/s	32/64-bit, 1600MT/s	32/64-bit, 1600MT/s	32/64-bit, 1600MT/s	32/64-bit, 2133MT/s
10/100/1000 Ethernet (with IEEE1588v2)	3 x 10/100/1000	2 x 10/100/1000	4 x 10/100/1000	2x 2.5 + 5 x 10/100/1000	4 x 10/100/1000	2x 2.5 + 5 x 10/100/1000	2x 2.5/10G + 6x 1G
Ethernet Switch	--	--	8-Port GE Switch	No	8-Port GE Switch	No	No
TDM	Yes	Yes	Yes	Yes	Yes	Yes	No
QUICC Engine	In P1021/12	No	TDM and HDLC	TDM and HDLC	TDM and HDLC	TDM and HDLC	No
SERDES	4 lanes	6 lanes	8 lanes(5GHz)	8 lanes(5GHz)	8 lanes(5GHz)	8 lanes(5GHz)	8 lanes(10GHz)
PCI-Exp	2 (Gen-1)	3 (Gen-1)	4 (Gen-2)	4 (Gen-2)	4 (Gen-2)	4 (Gen-2)	3 (Gen2) and 1 (Gen3)
Package			Pin Compatible				

Personality Comparison Chart

	P1020, P1011, P1021, P1012	P1022, P1013	T1020	T1022	T1040	T1042	T2081
DIU	--	Yes	Yes	Yes	Yes	Yes	No
SATA	--	2 controller	2 controller	2 controller	2 controller	2 controller	No
		1.5 or 3Gbaud	1.5 or 3Gbaud	1.5 or 3Gbaud	1.5 or 3Gbaud	1.5 or 3Gbaud	No
USB2.0	2 ULPI controllers	2 ULPI controllers	2 with PHY	2 with PHY	2 with PHY	2 with PHY	2 with PHY
Memory Card	SD/MMC	SD/MMC	SD/MMC/SDXC	SD/MMC/SDXC	SD/MMC/SDXC	SD/MMC/SDXC	SD/MMC/SDXC
Accelerators	SEC3.3	SEC3.3	DPAA, PME SEC5.0 with Trust Architecture	DPAA, PME SEC5.0 with Trust Architecture	DPAA, PME SEC5.0 with Trust Architecture	DPAA, PME SEC5.0 with Trust Architecture	DPAA, PME, DCE, SEC5.2 with Trust Architecture
Power Management	Power Management	Power Management with Deep sleep	Power Management with Deep sleep	Power Management with Deep sleep	Power Management with Deep sleep	Power Management with Deep sleep	Power Management
Package			Pin Compatible				

QorIQ T1 Family Features & Benefits

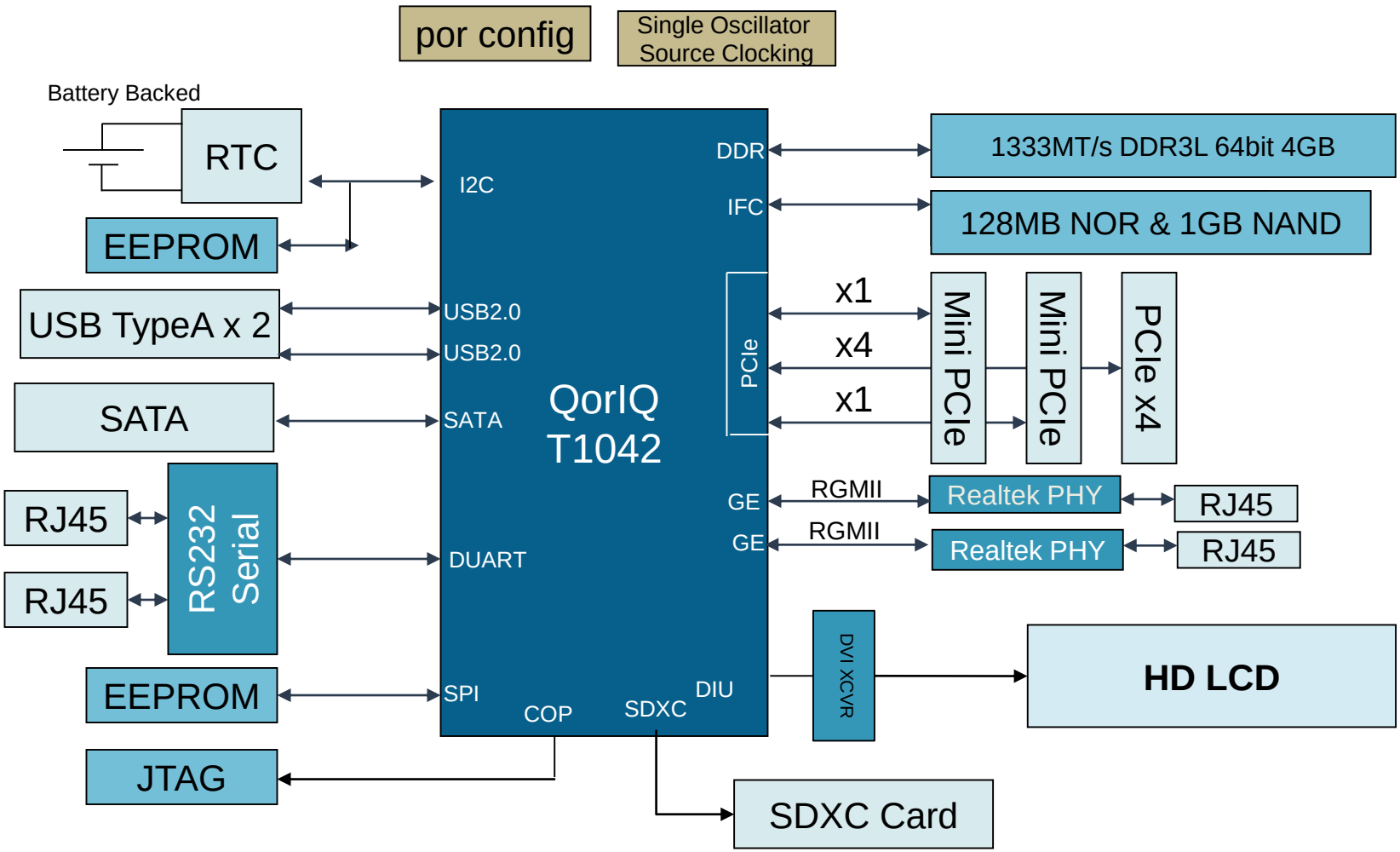
Features	Benefits
Scalable Performance Pin compatible dual core to eight virtual cores	**Future Proofing** Upgrade to higher performance as needed >2x-4x the performance of existing P1 series
Gigabit Ethernet Switch Integrated Gigabit Ethernet Switch	**Lowers System Cost/Simplifies design** Eliminates cost of external GE switch Simplifies HW and SW implementation Reduces overall system power
Accelerators DPAA - Classification, Traffic Management Pattern Matching Security	**Enforce SLAs/Reduce CPU cycles** Manage traffic guarantees to enforce SLAs Security policies based on application/services High performance HW based encryption VortiQa Security Appliance S/W and AppID
Hardware Assisted Virtualization Hypervisor level I/O MMU – controls memory I/Os can access Support for Topaz, KVM, Linux Containers,	**Higher performance (Vs. software emulation)** Enables virtualization layer to enforce system security Simplifies I/O virtualization and sharing Flexibility to use multiple options to meet system needs Support for S/W Hypervisor, KVM and Linux Containers
Power Management Best performance per watt Deep Sleep – proxy for sleeping hosts Enables ½ Watt AC	**Green Energy Efficient System Designs** Optimized for best performance and power Enables Compliance with Energy Consumption standards (ECC, EnergyStar, ECMA 393) Power Management software as part of SDK

QorIQ T1040 Software & Tools at a Glance

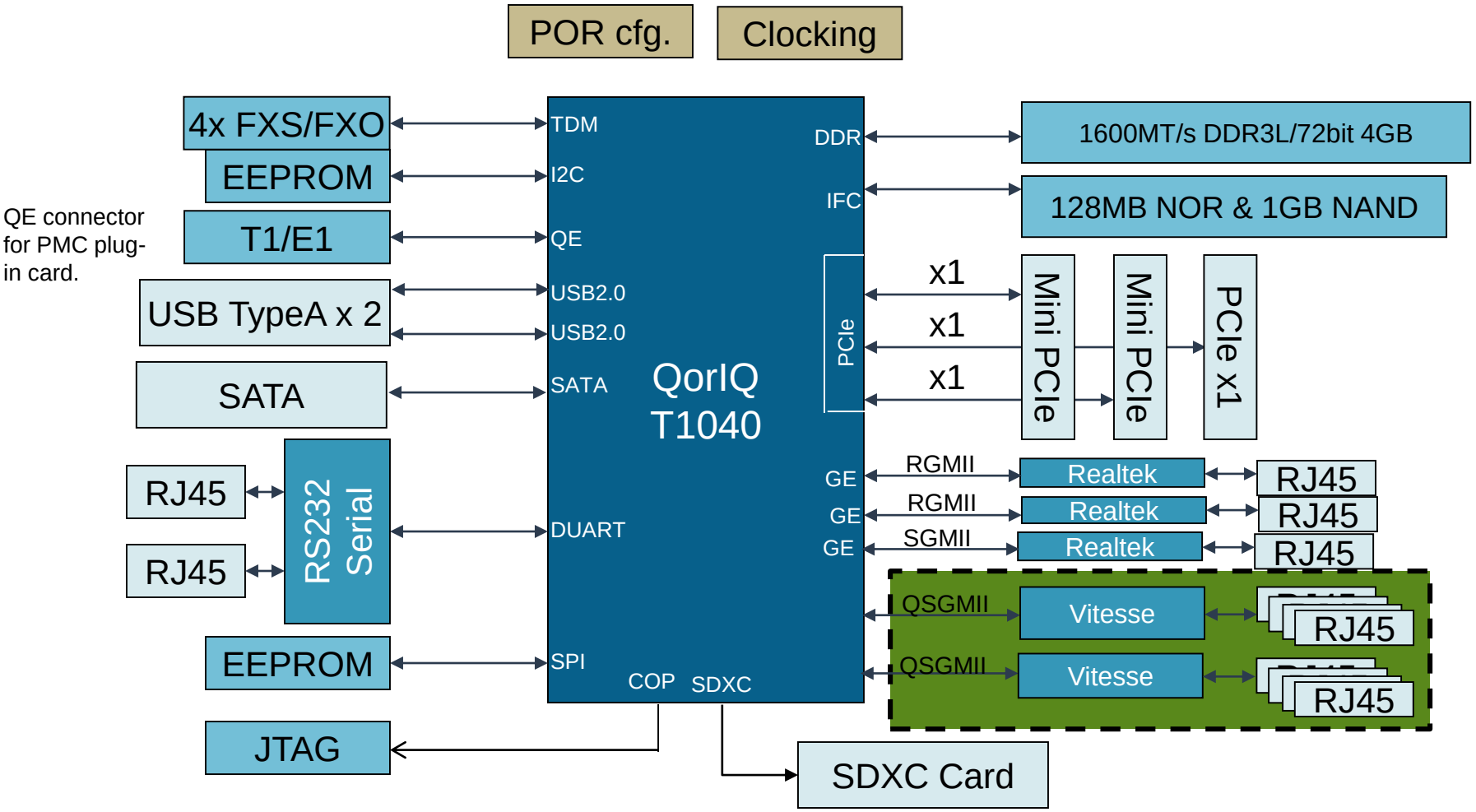
- Two Reference Design Boards
  - T1040RDB
  - T1042RDB
- Software Support
  - Yocto based SDK
  - SDK support includes
    - Legacy features (refer SDK 1.4 release notes)
    - New features
    - FMAN and QE microcode
    - Linux based QE drivers for TDM, UART and HDLC
- QorIQ Configuration Suite
- Code Warrior based debugger, flash programmer

QorIQ T1040RDB System

QorIQ T1042RDB Block Diagram

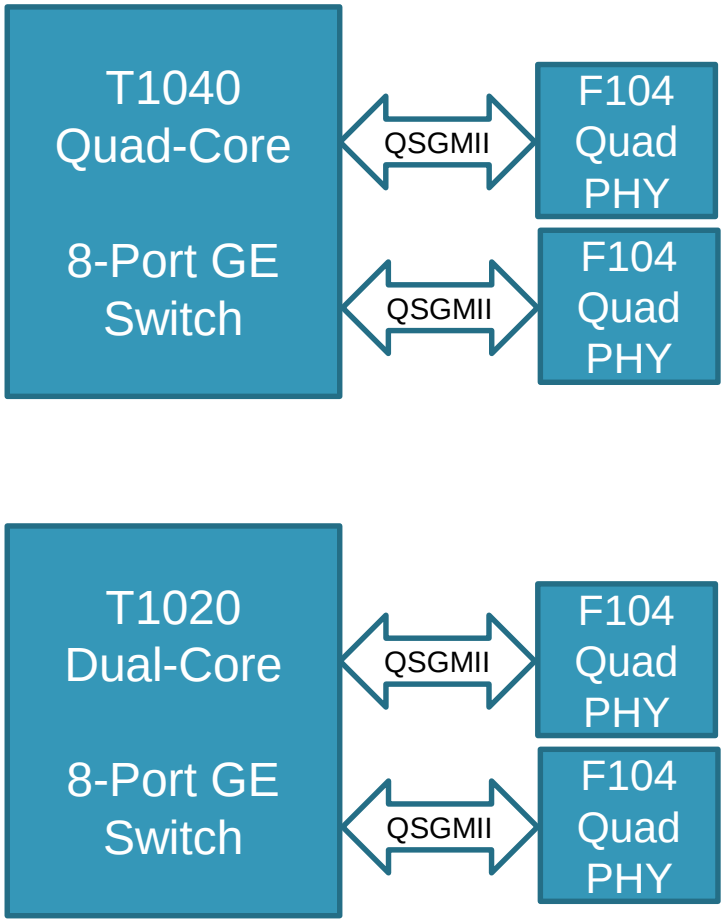


QorIQ T1040RDB Block Diagram



QorIQ T10xx Product Kit Options

Integrated Gigabit Ethernet Switch And bundled 2x QUAD PHYs

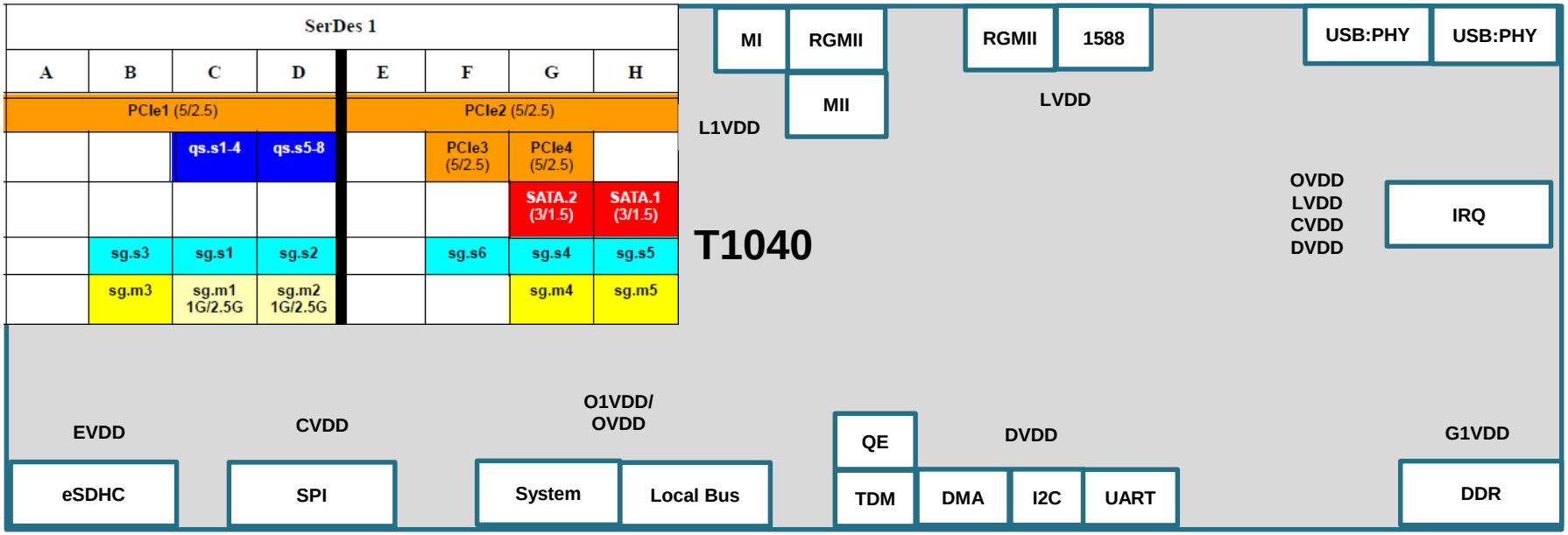


Without Gigabit Switch

T1042
Quad-Core

T1022
Dual-Core

Pin Multiplexing



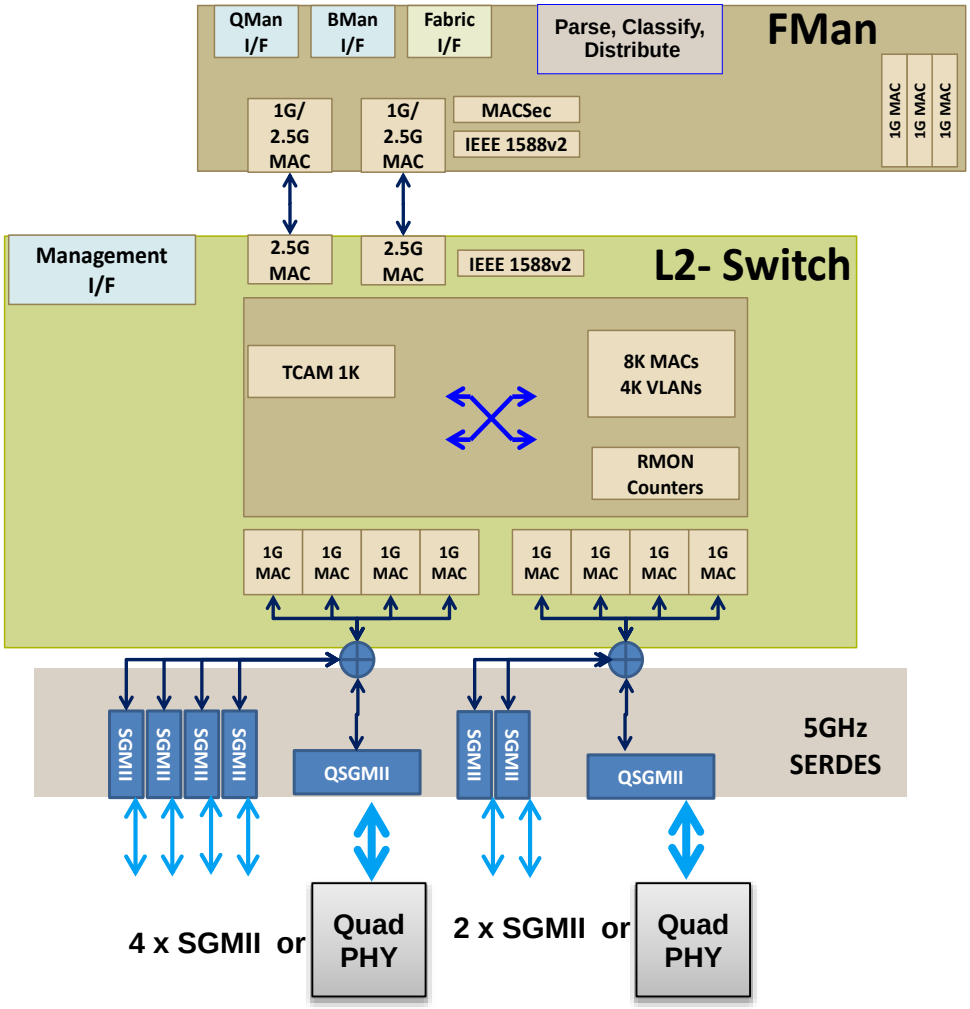
- O1VDD/OVDD (1.8V)
- L1VDD (3.3V/ 2.5V)
- LVDD (2.5 V)
- DVDD (3.3V/2.5V)
- CVDD (3.3V/1.8V)
- EVDD (runtime switchable supply 1.8V / 3.3 V)
- G1VDD (1.35V / 1.2V)

Agenda

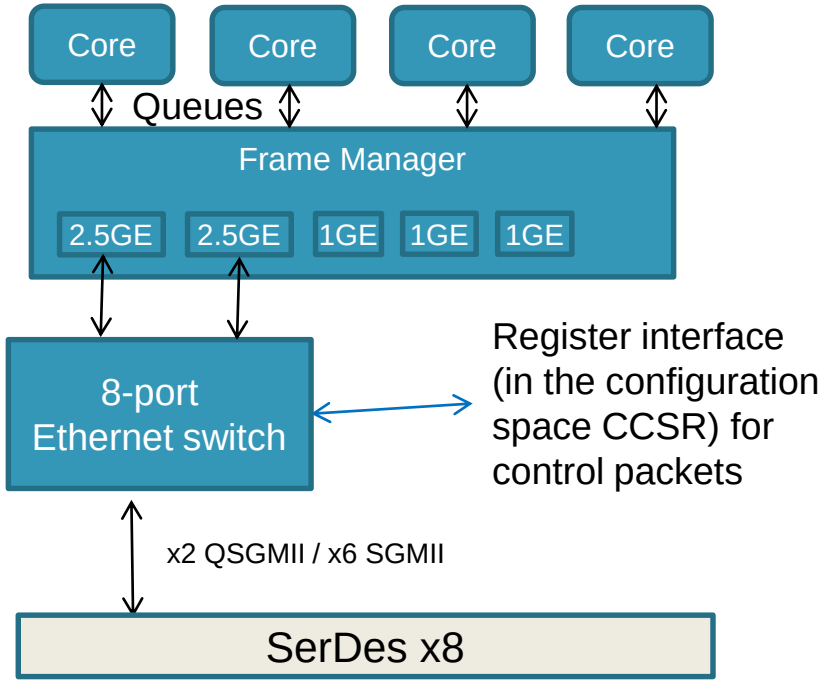
- Introduction
  - Block Diagram
  - Market Trend
- **QorIQ T1040 processor features**
  - Ethernet Switch
  - Serdes
  - Clocking
  - Power Management
- Collaterals
- Conclusion

QorIQ T1040: Gigabit Ethernet Switch

- Advanced Features
  - Priority flow control - lossless
  - Lower latency and shared buffer management
  - Advanced classification, shaping and policing
- Power savings
  - With support for latest standards including IEEE 802.3az Energy Efficient Ethernet (EEE)
- Cost savings
  - Through switch integration, low-pin count QSGMII connectivity and port count / cost optimization
- Increased ROI - Lower TTM and high re-use
  - Integrated solution kit with software reuse potential
- Support for Full featured L2 software stacks



Ethernet Switch Interface with Frame Manager



- 8 L2-switch ports + 3 FMAN ports
- 2 ports of Ethernet switch is connected to FMAN and operating 2.5 Gbps (aggregating to 5 Gbps)

OR

- 8 L2-switch ports + 4 FMAN ports. 1 port of Ethernet switch is connected to FMAN @ 2.5 Gbps.

Control packets are queued on the Ethernet Switch CPU-register interface and can be accessed (receive and transmit) through any e5500 core. This space is memory mapped in T1040 (CCSR space).

QorIQ T104x SERDES

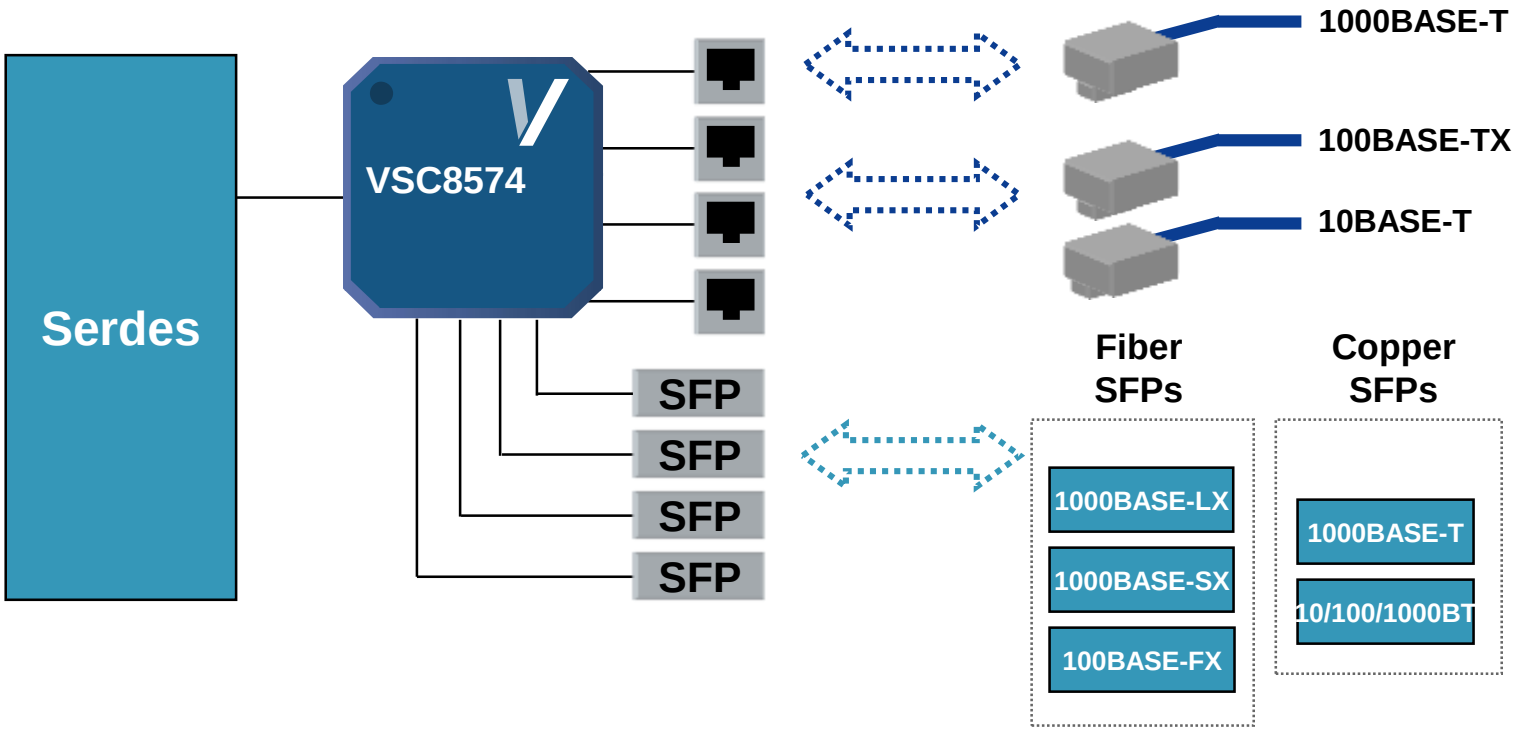
- QorIQ T104x device supports single 8 lane SerDes.

- There are two PLL's in the SerDes.
  - PLL1 provides clocking for lanes A:H and Ethernet switch
  - PLL2 provides clocking for Lanes C:H

  - QoriQ T104x device supports the following network protocols through SerDes
    - QSGMII (T1040, T1020 only)
    - 1000 Base-KX
    - SGMII 2.5G (T1042, T1022 only)
    - SGMII

QSGMII (Quad Serial Gigabit Media Independent Interface)

- The **QSGMII** is a method of combining four **SGMII** lines into a 5Gbit/s interface.
- **QSGMII** uses significantly fewer signal lines than four **SGMII** busses



QorIQ T1040/20 SerDes Lane Multiplexing

With Ethernet switch

SRDS_PRTCL_S1 RCW[128:135]	Lane A	Lane B	Lane C	Lane D	Lane E	Lane F	Lane G	Lane H	Parallel Port Availability
69	PCIe1 (5/2.5)	SGMII (m3)	QSGMII (s1-4)	QSGMII (s5-8)	PCIe2 (5/2.5)	PCIe3 (5/2.5)	SGMII (m4)	SATA1	**RGMII (FMAN MAC#5) RGMII (FMAN MAC#2, MAC#5**
66	PCIe1 (5/2.5)	SGMII (m3)	QSGMII (s1-4)	QSGMII (s5-8)	PCIe2 (5/2.5)	PCIe3 (5/2.5)	PCIe4 (5/2.5)	SATA1	**2 RGMII (FMAN MAC #4 & #5)**
67	PCIe1 (5/2.5)	SGMII (m3)	QSGMII (s1-4)	QSGMII (s5-8)	PCIe2 (5/2.5)	PCIe3 (5/2.5)	PCIe4 (5/2.5)	SGMII (m5)	**1 RGMII (FMAN MAC #4)**
60	PCIe1 (5/2.5)	SGMII (m3)	QSGMII (s1-4)	QSGMII (s5-8)	PCIe2 (5/2.5)				**2 RGMII (FMAN MAC #4 & #5)**
8D	PCIe1 (5/2.5)	SGMII (s3)	SGMII (s1)	SGMII (s2)	PCIe2 (5/2.5)	SGMII (s6)	SGMII (s4)	SGMII (s5)	**2 RGMII (FMAN MAC #4 & #5)**
89	PCIe1 (5/2.5)	SGMII (s3)	SGMII (s1)	SGMII (s2)	PCIe2 (5/2.5)	PCIe3 (5/2.5)	SGMII (s4)	SATA1	**2 RGMII (FMAN MAC #4 & #5)**

- Ethernet switch connects with FMAN using MAC#1 and/or MAC#2
- MAC#2 used as additional RGMII port if Ethernet switch connected through MAC#1 only
- MAC#1 and MAC#2 are 2.5G ports.

LEGEND
"mn" indicates MAC# from FMan
"sn" indicates MAC# from Ethernet switch

QorIQ T1042/22 SerDes Lane Multiplexing

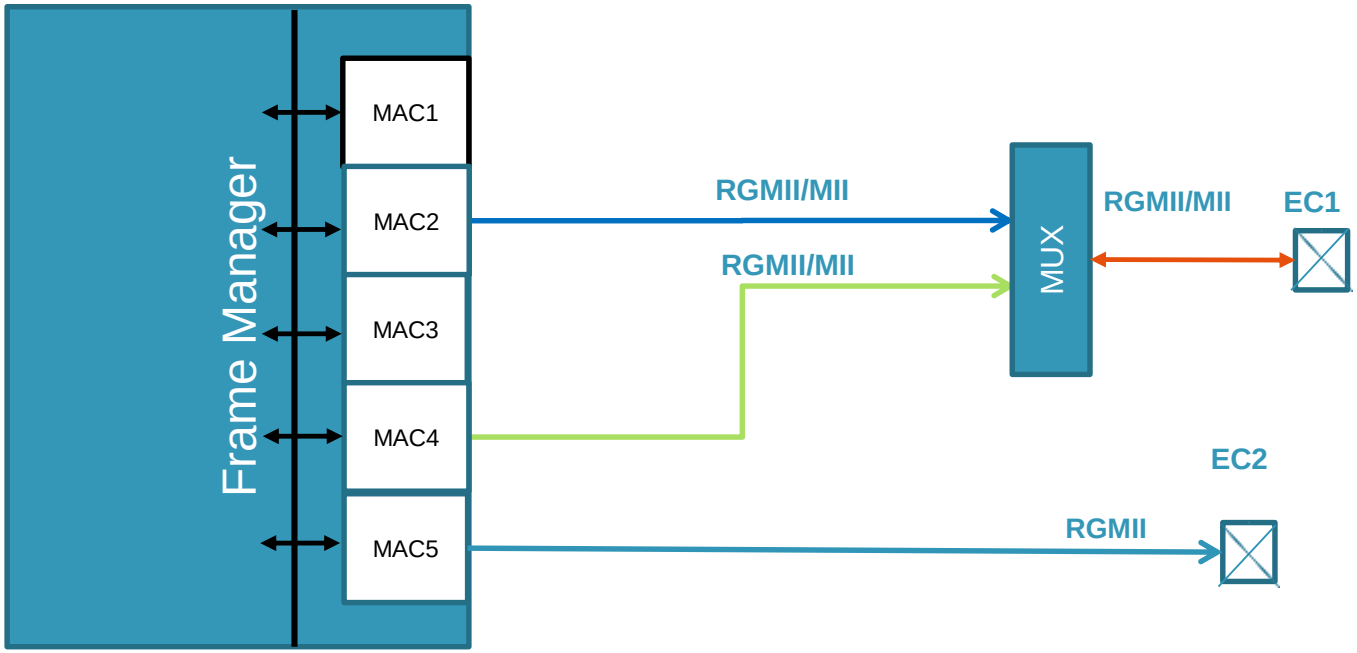
Without Ethernet switch

SRDS_PRTCL_S1 RCW[128:135]	Lane A	Lane B	Lane C	Lane D	Lane E	Lane F	Lane G	Lane H	Parallel Port availability
86	PCIe1 (5/2.5)	SGMII (m3)	SGMII (m1)	SGMII (m2)	PCIe2 (5/2.5)	PCIe3 (5/2.5)	PCIe4 (5/2.5)	SATA1	2 RGMII (FMAN MAC #4 & #5)
87	PCIe1 (5/2.5)	SGMII (m3)	SGMII (m1)	SGMII (m2)	PCIe2 (5/2.5)	PCIe3 (5/2.5)	PCIe4 (5/2.5)	SGMII (m5)	1 RGMII (FMAN MAC #4)
A7	PCIe1 (5/2.5)	SGMII (m3)	SGMII (m1) 2.5G	SGMII (m2) 2.5G	PCIe2 (5/2.5)	PCIe3 (5/2.5)	PCIe4 (5/2.5)	SGMII (m5)	1 RGMII (FMAN MAC #4)
AA	PCIe1 (5/2.5)	SGMII (m3)	SGMII (m1) 2.5G	SGMII (m2) 2.5G	PCIe2 (5/2.5)	PCIe3 (5/2.5)	SGMII (m4)	SGMII (m5)	0 RGMII
40	PCIe1 (5/2.5)		SGMII (m1)	SGMII (m2)	PCIe2 (5/2.5)				2 RGMII (FMAN MAC #4 & #5)
06	PCIe1 (5/2.5)				PCIe2 (5/2.5)	PCIe3 (5/2.5)	PCIe4 (5/2.5)	SATA1	2 RGMII (FMAN MAC #4 & #5)
08	PCIe1 (5/2.5)				PCIe2 (5/2.5)	PCIe3 (5/2.5)	SATA2	SATA1	2 RGMII (FMAN MAC #4 & #5)
8F	PCIe1 (5/2.5)	SGMII (m3)	SGMII (m1)2.5G	SGMII (m2)2.5G			SGMII (m4)	SGMII (m5)	0 RGMII
85	PCIe1 (5/2.5)	SGMII (m3)	SGMII (m1)	SGMII (m2)	PCIe2 (5/2.5)		SGMII (m4)	SGMII (m5)	0 RGMII
A5	PCIe1 (5/2.5)	SGMII (m3)	SGMII (m1) 2.5G	SGMII (m2) 2.5G	PCIe2 (5/2.5)		SGMII (m4)	SGMII (m5)	0 RGMII
00	PCIe1 (5/2.5)				PCIe2 (5/2.5)				2 RGMII (FMAN MAC #4 & #5)

LEGEND
"mn" indicates MAC# from FMan

Ethernet Parallel Interfaces on QorIQ T104x Processors

- 2x RGMII or 1x MII interface supported.
- MII/RGMII selection for EC1 via RCW**[EC1]** field.
- MAC2 or MAC4 selection for EC1 via RCW**[MAC2_GMII_SEL**] field
- RGMII interface enabled for EC2 via RCW**[EC2]** field.



USB PHY

- Supports Dual on-chip integrated USB PHY
- Supports USB 2.0
- Works on 24MHz clock (non spread spectrum) on the SOC's USBCLK pin
- Can also work on an internal reference clock (system clock at 100MHz) which can be pre divided to obtain 20 MHz reference clock

DIU

- QorIQ T1040 has the same DIU programming model as QorIQ P1022 with the following differences

Feature	P1022 DIU	T1040 DIU
Data Interface	24 bit RGB	12 bit dual data rate RGB
Pin multiplexing	Multiplexed with eLBC	Multiplexed with QUICC Engine
Platform to pixel clock frequency ratio	≥ 3	≥ 4
Maximum pixel clock	133MHz	150MHz

eSDHC New Features

- Supports SDXC cards
  - Up to 2TB space
- Supports cards with UHS-I speed grade
  - Ultra high speed grade
    - SDR12, SDR25, SDR50, SDR104, DDR50
  - UHS-I cards work on 1.8V signaling
  - On board dual voltage regulators are needed to support UHS-I cards because card initialization happens at 3.3V and regular operations happen at 1.8V
  - SD controller provides a signal to control the voltage regulator. The signal is controlled via SDHC_VS pin
- eMMC 4.5 support (HS200, DDR)
- All modes of SD3.0, eMMC 4.4 and eMMC4.5 are supported except 8 bit DDR for eMMC.

QorIQ T1040 DDR Controller Features

- Legacy Features:
  - Support for 32/ 64 bit DDR3L and DDR4 SDRAM with ECC
  - Chip-Select interleaving support
  - Support for unbuffered and registered DIMMs, single-ranked, dual-ranked, and quad-ranked DIMMs
- DDR4 Specific Features:
  - New JEDEC POD12 interface standard (1.2V)
  - Support for 4 bank groups
  - DBI (Data Bus Inversion) feature
  - Command Address (CA Parity)
  - CRC for data bus
  - CAL mode (CS to Command Address Latency)
  - Low power auto self-refresh

Core, PAMU, PME for QorIQ T1040 Processors

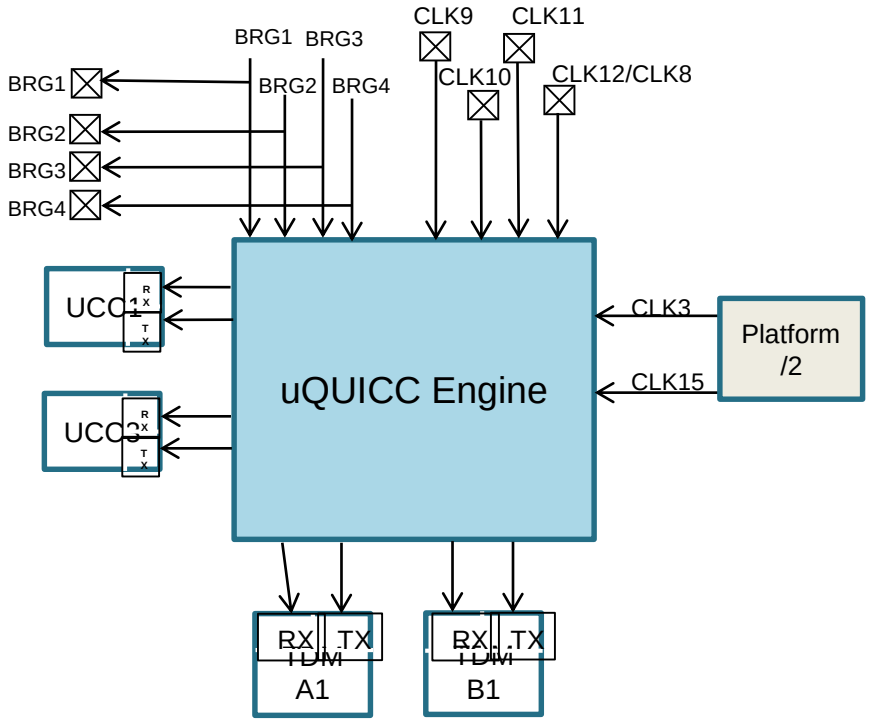
- QorIQ T1040 has 64-bit core with backside L2 cache of size 256KB
- e5500 Backside L2 cache can significantly improve performance
  - Much lower L2 latency
  - 36-bit physical address support

Core	L2 Latency	Dhrystone DMIPS/MHz
e500v2 (Frontside L2)	23 core cycles	2.4
e5500 (Backside L2)	12 core cycles	3.0

- Single PAMU catering to all the I/O's (PAACT entries are 128)
- Pattern Matching engine (2.2) supports 16,384 patterns as compared to 32K pattern support in PME 2.0

QUICC Engine in QorIQ T1040 Processors

- Supports one uQE block
- 64MHz SYSCLK support for ProfiBUS
- Support for two TDM [TDMA, TDMB] and two UCC [UCC1, UCC3]
- Protocols:
  - HDLC, Transparent
  - Synchronous UART
  - ProfiBUS
  - TDM/SI
- UCC1 signals are multiplexed with TDMA signals
- UCC3 signals are multiplexed with TDMB signals



What is VID?

- VID is a specific method of selecting the optimum voltage-level to guarantee performance and power targets.
- QorIQ device contains fuse block registers defining required voltage level. This eFUSE definition is accessed through the Fuse Status Register (DCFG_FUSESR).
- Customer software will read the VID value from factory-set efuse values and configure regulator values appropriately.
- **For T1040, the core VDD/VDDC value will range from 0.97V to 1.025V in 12.5mV steps**

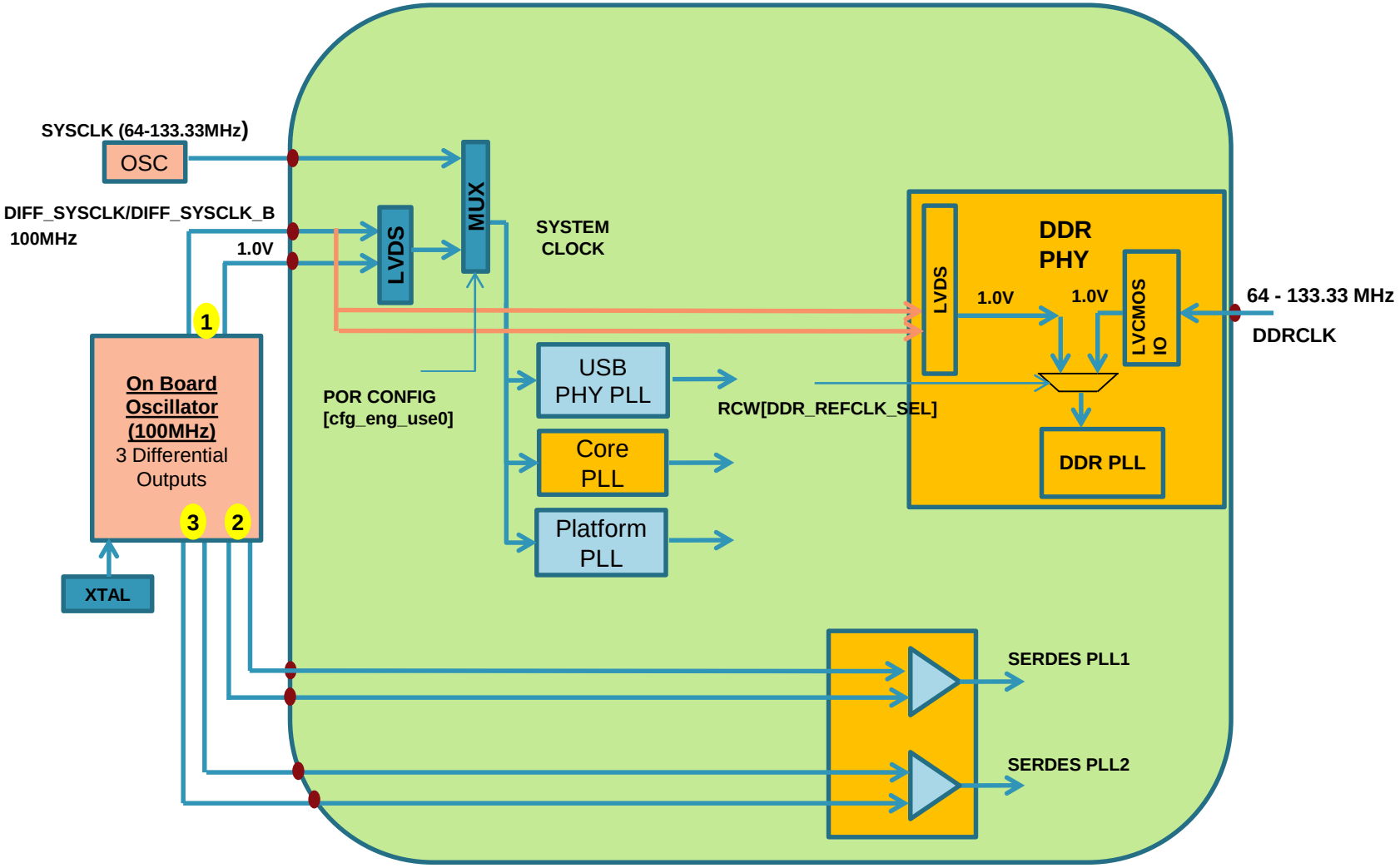
Power Pins	Power Islands on T1040
VDD	Switchable Core and Platform
VDDC	Always ON core and Platform Supply
USB_SVDD	USB supply

Start up voltage	1.025 ± 30mV
During normal operation	VID ± 30mV

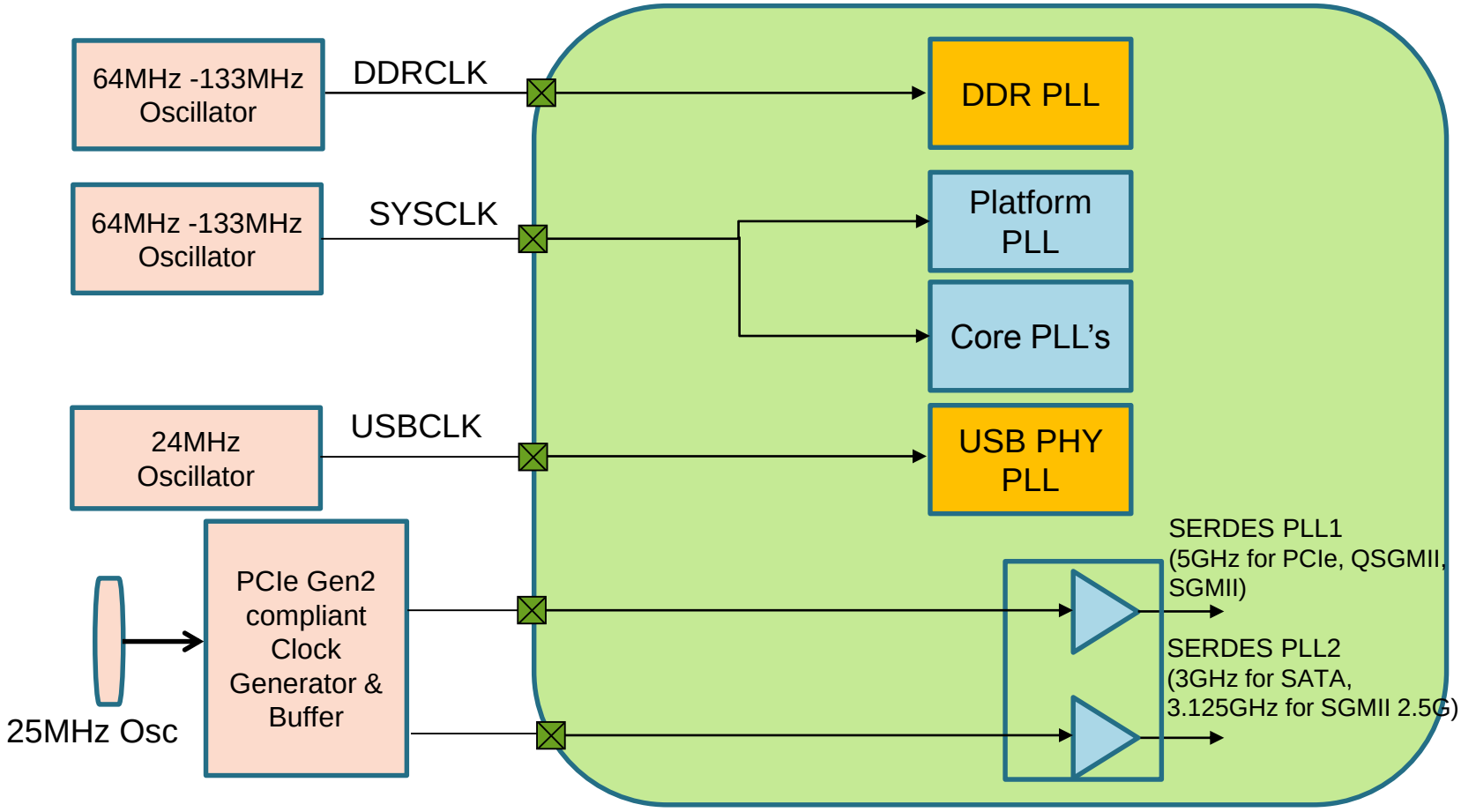
QorIQ T1040 Clock Signals

Signal	Function	Range
SYSCLK	Single ended primary clock input	64MHz to 133MHz
DIFF_SYSCLK/ DIFF_SYSCLK_B	Differential primary clock input	100MHz
DDRCLK	Reference clock for DDR controller	64MHz to 133MHz
USBCLK	Clock input to the USB PHY's	24MHz
SD1_REF_CLKn_P/ SD1_REF_CLKn_N	Clock input to High speed Serial interfaces	100MHz, 125MHz

“Single Oscillator Source ” clock Mode



Multiple reference clock mode (Legacy mode)



QorIQ T1040 Power States

e5500 States: Run, Doze and Nap

Each core can independently support each state

Core activity state	CPU State	Processor Clocks	Snoops Responded	Interrupts Responded	Comments
PH00	Run	On	Yes	Yes	Core clock adaption can be enabled
PH10	Doze	On	Yes	Yes	Core stops dispatching new instructions
PH15	Nap	Off (Except time base)	No	Yes	Flush data cache before entering

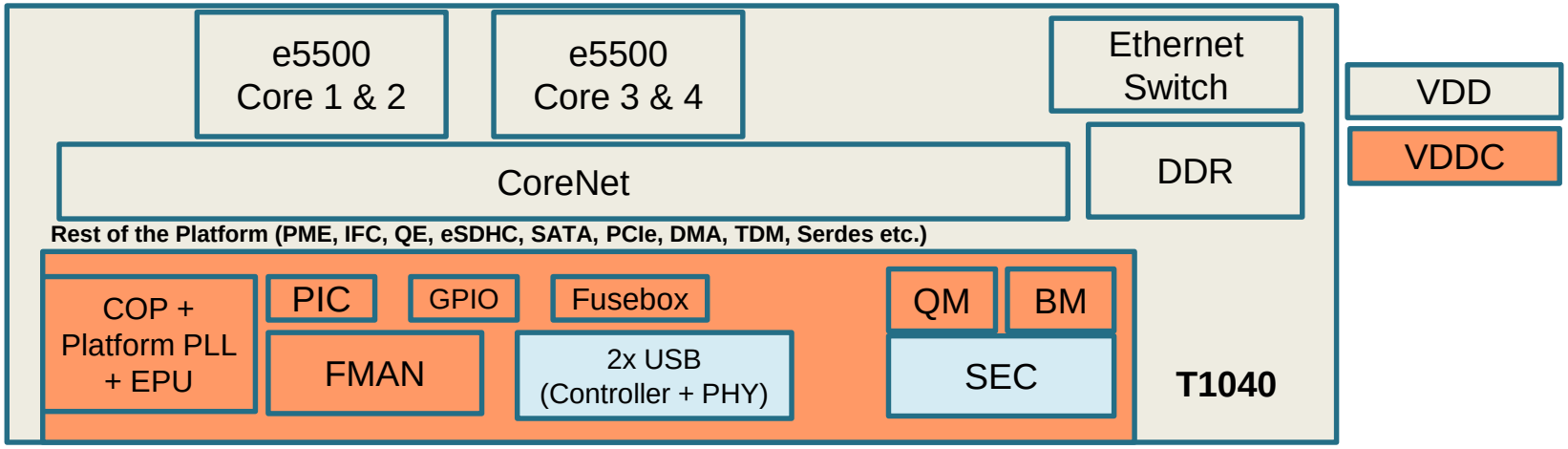
QorIQ T1040 SoC Power Management States

QorIQ T1040 Device (SoC) states: LPM10, LPM20, LPM35, Deep Sleep

SOC RCPM state	Equivalent P1022 State	Device Clocks	ASLEEP Asserted	Comments
LPM10	---	On	No	Software configured variant of the 'full ON' state where some cores are placed in a lower power state
LPM20	Sleep	Cores in Nap, time base stopped	Yes	Only modules required for wakeup will have a running clock.
LPM35	Deep Sleep	Only the blocks in ON domain have clock running.	Yes	Only used for entry to deep sleep
Deep Sleep				Power is removed from a major portion of SOC

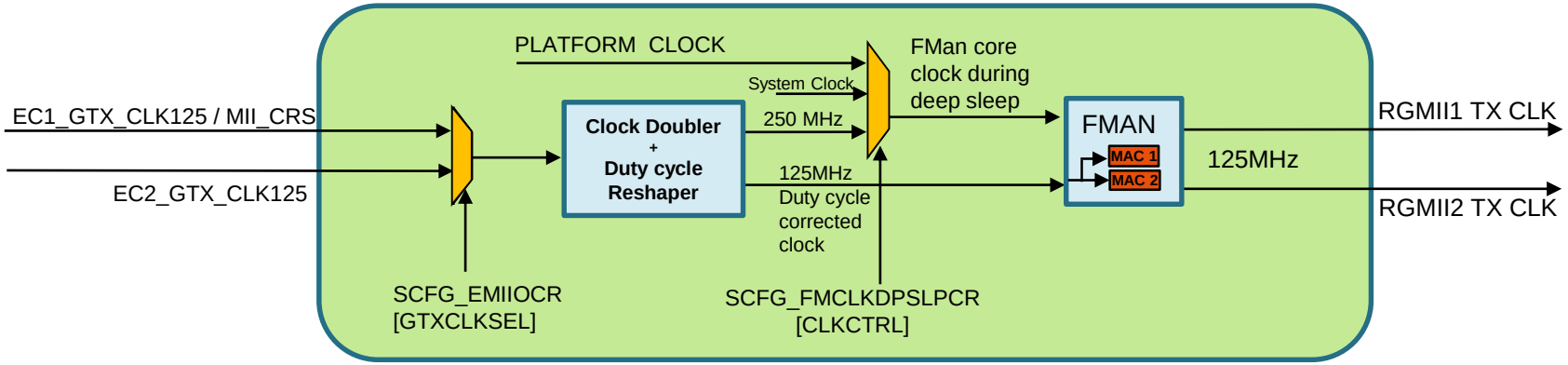
QorIQ T1040 Deep Sleep

- A major portion of the QorIQ T1040 processor is switched OFF including the cores and DDR Controller.
- Only the blocks needed to detect wakeup and sequence the chip out of deep sleep are ON.
- QorIQ T1040 responds to incoming wake-up events, from Ethernet interface, USB or GPIO interrupt, while consuming very little power.



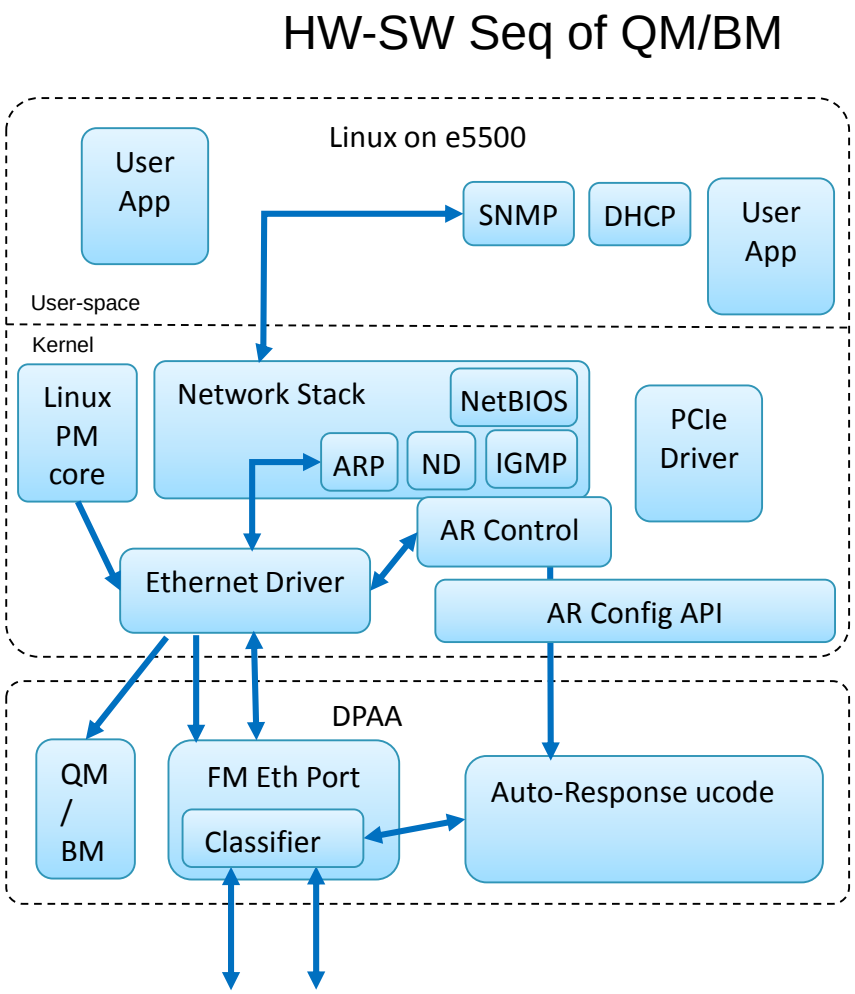
- VDD is switchable supply
- VDDC is always ON
- USB and SEC block can optionally be in ON/OFF domain

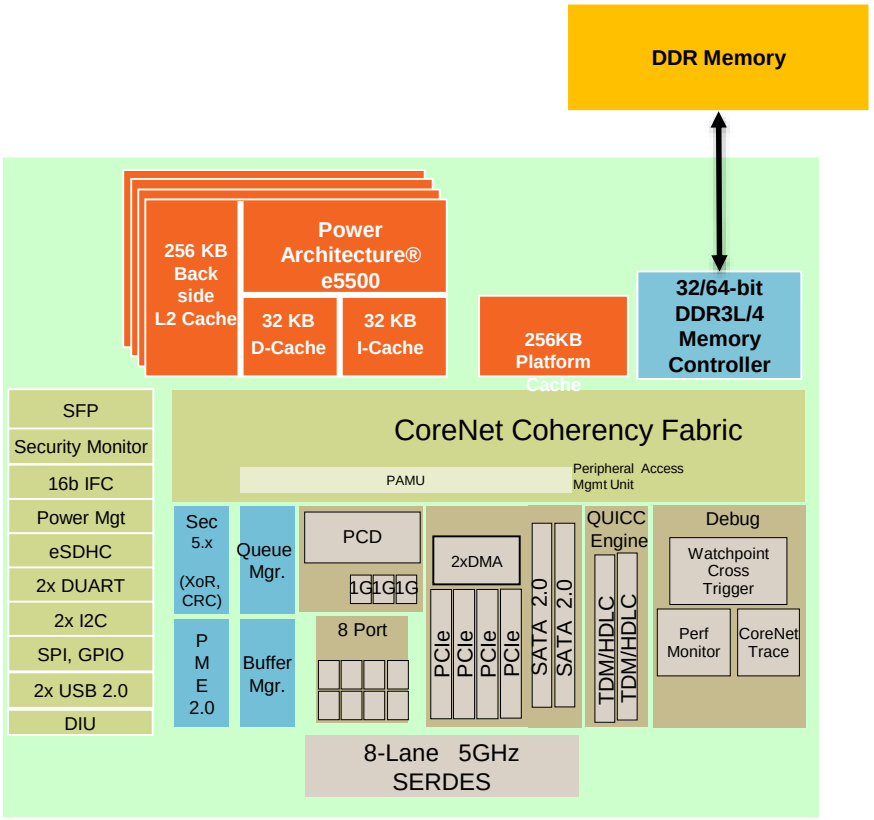
Clocking in Deep sleep mode (check with Anju)



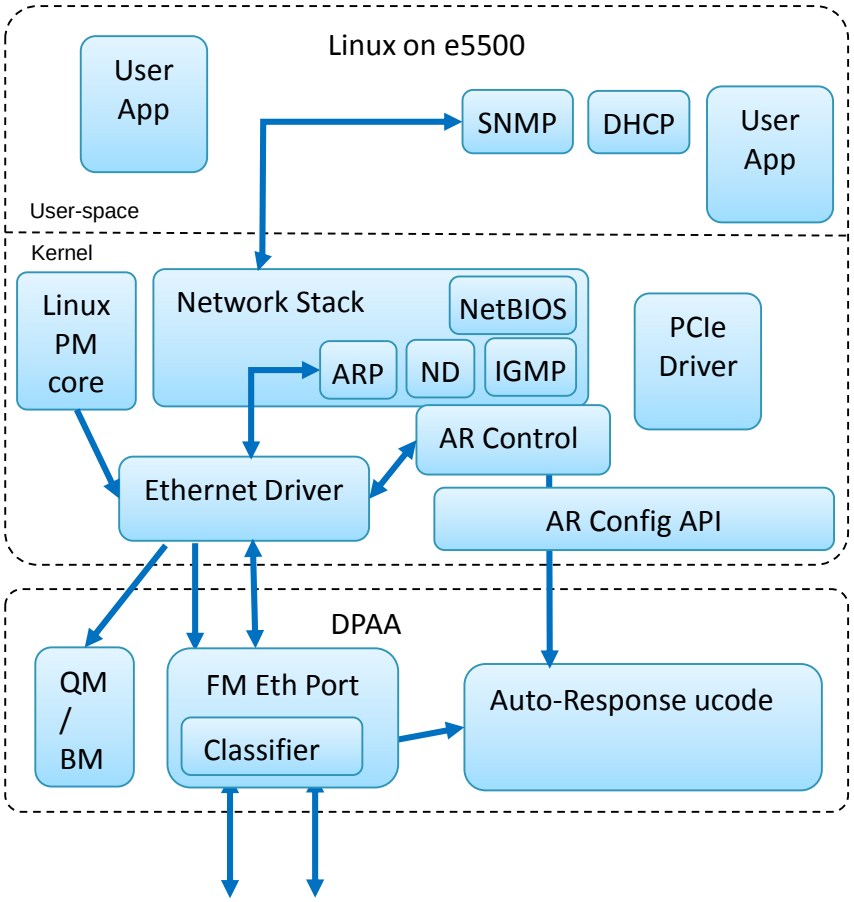
- Deep Sleep operation switches platform clock to system reference clock
- Frame Manager is ON during Deep sleep for Auto response.
- Frame Manager is clocked with 2* 125MHz RGMII_GTXCLK from PHY
- MII mode requires Frame Manager to be clocked with System clock

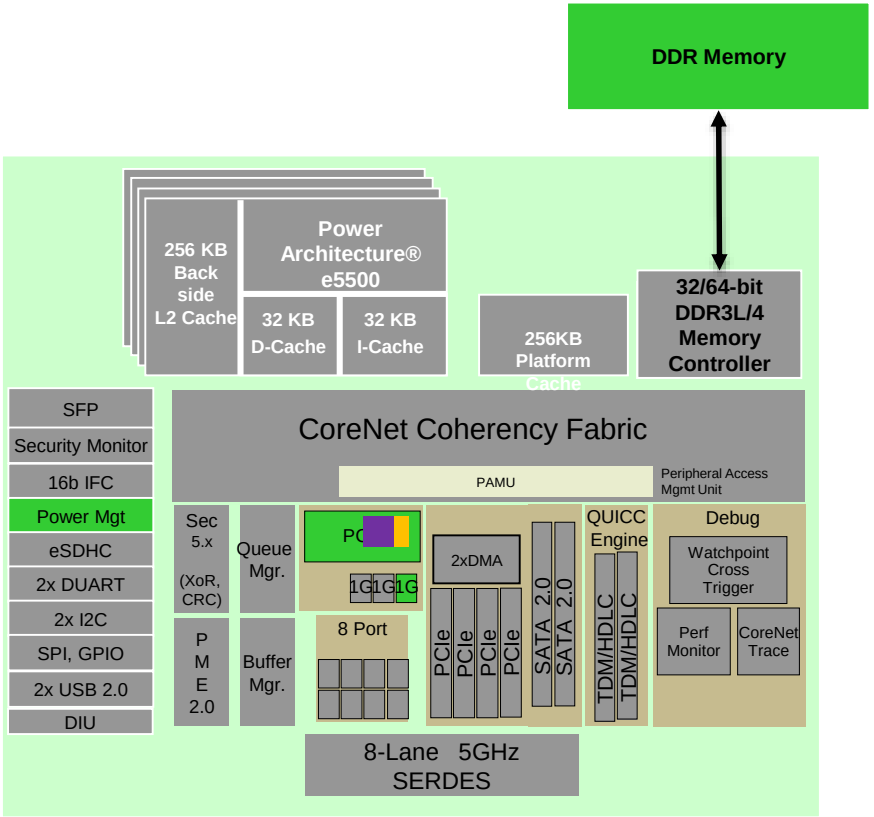
QorIQ T1040 Deep Sleep





QorIQ T1040 Deep Sleep Auto-response and wakeup





Session Request

Ping/ARP/IGMP Packet

Deep sleep related

- VDD and VDDC can be powered through separate regulators
- VDDC should ramp before/along with VDD
- Lossless mode supported for RGMII
- FMAN works on SYSCLK for MII mode and may not be lossless
- EVT_B2 aka power enable, should not be sampled when PORESET_B is asserted. There should be an on board pull up on this signal.
- USB and SEC block can optionally be switched ON/OFF in deep sleep, board level considerations required
- EPU and NPC resources are not available as Debug

SDHC related

- RCW loading from SD interface using voltage translators is not supported

Agenda

- Introduction
  - Block Diagram
  - Market Trend
- QorIQ T1040 processor features
  - Ethernet Switch
  - Serdes
  - Clocking
  - Power Management
- **Collaterals**
- Conclusion

Collaterals / Documentation

- **On the Core:**
  - e5500 core Reference Manual (Rev4 , 2013)

- **On the SoC device:**
  - QorIQ T104x Processor Fact-sheet and Product brief
  - HW Spec Rev D
  - Reference Manual Rev B
  - Advanced Debug and Performance Monitoring Reference Manual
  - QEIWRM
  - Errata-sheet Rev A
  - Application Notes
    - AN4773 - Migration Guide from T2081 to T1040

Agenda

- Introduction
  - Block Diagram
  - Market Trend
- QorIQ T1040 processor features
  - Ethernet Switch
  - Serdes
  - Clocking
  - Power Management
- Collaterals
- **Summary**

QorIQ T1 and T2 Families Extend Market Leadership

- **First 64-bit embedded processor with an integrated GbE switch**
  - Reduces system cost, design complexity and power
- **One of the industry's most scalable, pin-compatible family of devices**
  - Performance scalability with a common architecture
- **Energy efficiency and low power**
  - Designed to be compliant to European Code of Conduct, and EnergyStar energy consumption standards
- Ideal for **low- to mid-range** networking and industrial connectivity applications

Freescale's Comprehensive Ecosystem

Tools and Operating Systems	Virtualization	Application Software	Systems Integration & Services	Development Systems
freescale CodeWarrior	KVM	freescale VortiQa	RadiSys.	
criticalblue Accelerating Embedded Software	lxc Linux Containers	Elliptic Embedded Security you can Trust	MERCURY COMPUTER SYSTEMS	
ENEA	freescale	GWIND Bitdefender	ADVANTECH	
Green Hills SOFTWARE, INC.	Green Hills SOFTWARE, INC.	Broadweb	Portwell	
QNX	ENEA	MERCURY COMPUTER SYSTEMS	Lanner	
mentor embedded		One Convergence	EMERSON Network Power	
WIND RIVER	WIND RIVER	mocana	FLEXTRONICS	

Introducing The QorIQ LS2 Family

Breakthrough, software-defined approach to advance the world's new virtualized networks

New, high-performance architecture built with ease-of-use in mind

Groundbreaking, flexible architecture that abstracts hardware complexity and enables customers to focus their resources on innovation at the application level

Optimized for software-defined networking applications

Balanced integration of CPU performance with network I/O and C-programmable datapath acceleration that is right-sized (power/performance/cost) to deliver advanced SoC technology for the SDN era

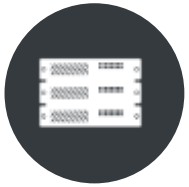
Extending the industry's broadest portfolio of 64-bit multicore SoCs

Built on the ARM® Cortex®-A57 architecture with integrated L2 switch enabling interconnect and peripherals to provide a complete system-on-chip solution

QorIQ LS2 Family

Key Features

SDN/NFV Switching



Data Center

Wireless Access

Unprecedented performance and ease of use for smarter, more capable networks

High performance cores with leading interconnect and memory bandwidth

- 8x ARM Cortex-A57 cores, 2.0GHz, 4MB L2 cache, w Neon SIMD
- 1MB L3 platform cache w/ECC
- 2x 64b DDR4 up to 2.4GT/s

A high performance datapath designed with software developers in mind

- New datapath hardware and abstracted acceleration that is called via standard Linux objects
- 40 Gbps Packet processing performance with 20Gbps acceleration (crypto, Pattern Match/RegEx, Data Compression)
- Management complex provides all init/setup/teardown tasks

Leading network I/O integration

- 8x1/10GbE + 8x1G, MACSec on up to 4x 1/10GbE
- Integrated L2 switching capability for cost savings
- 4 PCIe Gen3 controllers, 1 with SR-IOV support
- 2 x SATA 3.0, 2 x USB 3.0 with PHY

www.Freescale.com