



High-Precision Measurement Using Kinetis M Series MCUs

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Session Objectives

- Understand electricity meter block diagram and major functionalities
- Familiarize with Kinetis M series MCUs
- Become familiar with Freescale electricity meter reference designs, HW/SW development tools and algorithms offering
- Mastering MCU programming...

Tutorial

- Ideal Hilbert Transformer

Kinetis M series products are designed for next-generation of the metrology applications. The cost-effective Kinetis M series MCUs combine a sophisticated analog front end (AFE), hardware tamper detection and low-power operation to enable the design of secure, high-accuracy 1-, 2- and 3-phase electricity metering solutions. Freescale also provides proven 1-, 2-, and 3-phase hardware reference designs with complex metrology firmware satisfying 0.1% measurement accuracy and all ESD requirements. Traditional smart metering designs typically employ two chips to separate user billing software from the main application code, as required by WELMEC, OIML and other global standards. However, Kinetis M series MCUs handle this task with a single chip due to their on-chip memory protection unit, peripheral bridge, protected GPIO and DMA controller. To guard against external tampering, M series MCUs include active and passive tamper pins with automatic time stamping throughout, including on the independent real-time clock (iRTC). In addition, a random number generator enables faster, easier implementation of encryption algorithms than software implementations...

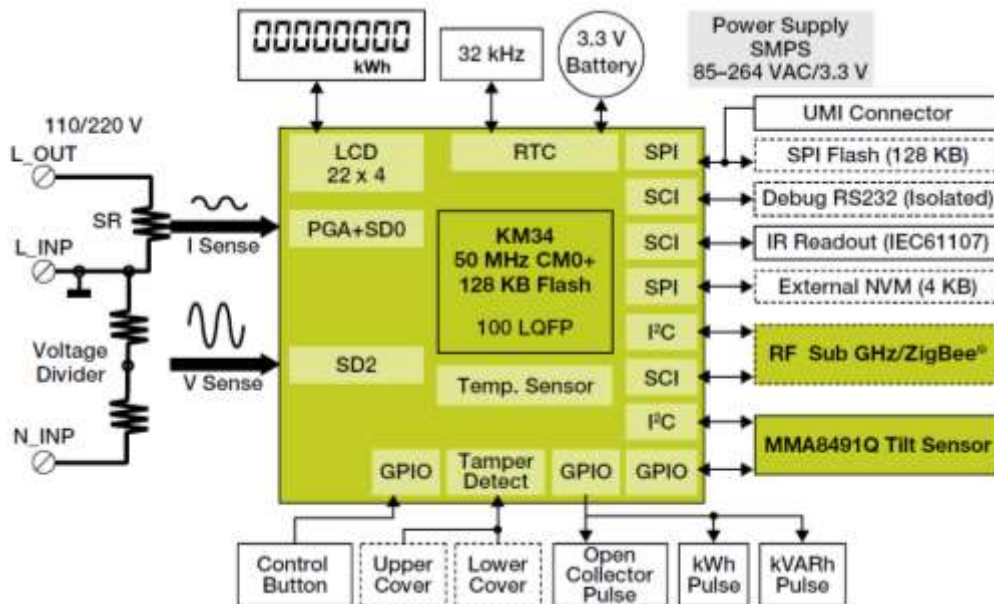


Agenda

- ✓ Introduction to electricity metering
 - Kinetis M series MCUs
 - Electricity metering algorithms
 - Electricity meter reference designs
 - Kinetis M development tools
 - Mastering MCU programming...
 - References

Electricity Meter Block Diagram

MEASURE → PROCESS → DISPLAY



• Measure

- Electricity meters must measure phase voltages and phase currents consumed by connected load
- Measurement linearity of 0.1% over 2000:1 dynamic range.
- Shunt resistors, current transformers or Rogowski coils can be connected.

• Process

- Accurate calculation of the active and reactive energies
- Time keeping with accuracy better than $\pm 0.5s/day$ needed for billing purposes
- Tamper processing ensures security
- Load profiles and parameters storage

• Display

- LCD display allows visual inspection
- HMI (control button) allows system configuration
- IR / RF communication allows download of data for utility companies and automatic meter reading



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Core

- CM0+ core Up to 50MHz
- Separate FLL post-scalers for Flash and Core clocks.
- Dedicated PLL for $\Sigma\Delta$ modulator clock
- 4ch DMA
- Memory Protection Unit
- Single 32kHz Crystal operation
 - MHz Crystal optional

Security & Encryption

- Programmable 16/32-bit CRC
- IRTC w/ tamper detection
 - 3 Tamper pins (operating on battery)
- Random Number Generator (NIST: SP800-90)
 - AES Encryption (via software library)
- Memories
 - Up to 128 KB Program Flash
 - 16 KB SRAM

Analog

- 4x24 bit $\Sigma\Delta$ after averaging (2xPGA) highly accurate supporting EN 50470-1, EN 50470-3, IEC 62053-21, IEC 62053-22 and IEC 62053-23, optimized for shunt sensor ($\geq 50\Omega$).
- 0.1% error in active and reactive energy over a dynamic range of 2000 to 1
- Internal 1.2V reference voltage (33 ppm/ $^{\circ}\text{C}$)
- 12-ch 16-bit SAR for auxiliary measurement
- 2x analog comparator

Serial Communications

- 2x SPI
- 4x UART
 - All combined with Quad Timer & HSCMP for IR
 - 2 support ISO7816
 - All support flow control
- 2x I2C
 - All UARTs and SPIs are 3V compatible while 1 UART and 1 SPI are both 3V and 5V compatible (open drain configuration)

Peripheral XBAR

- Remapping peripheral IOs
- UART selection for IR

Timer/PWM/Clock

- Quad Timer (total 4 universal timers)
- 2x PIT
- 1x Watchdog Timer (windowed, independently clocked)
- 1x EWM (External Watchdog Monitor)
- 1x LPTimer

LCD Display

- Up to 288 segment LCD, up to 8 backplanes

WakeUp Unit

- Group selected GPIOs (16), LPTIM, RTC (+tamper pins), HSCMP, SCI, Brownout and POR sources to wake up from Power Gated STOP mode

GPIO

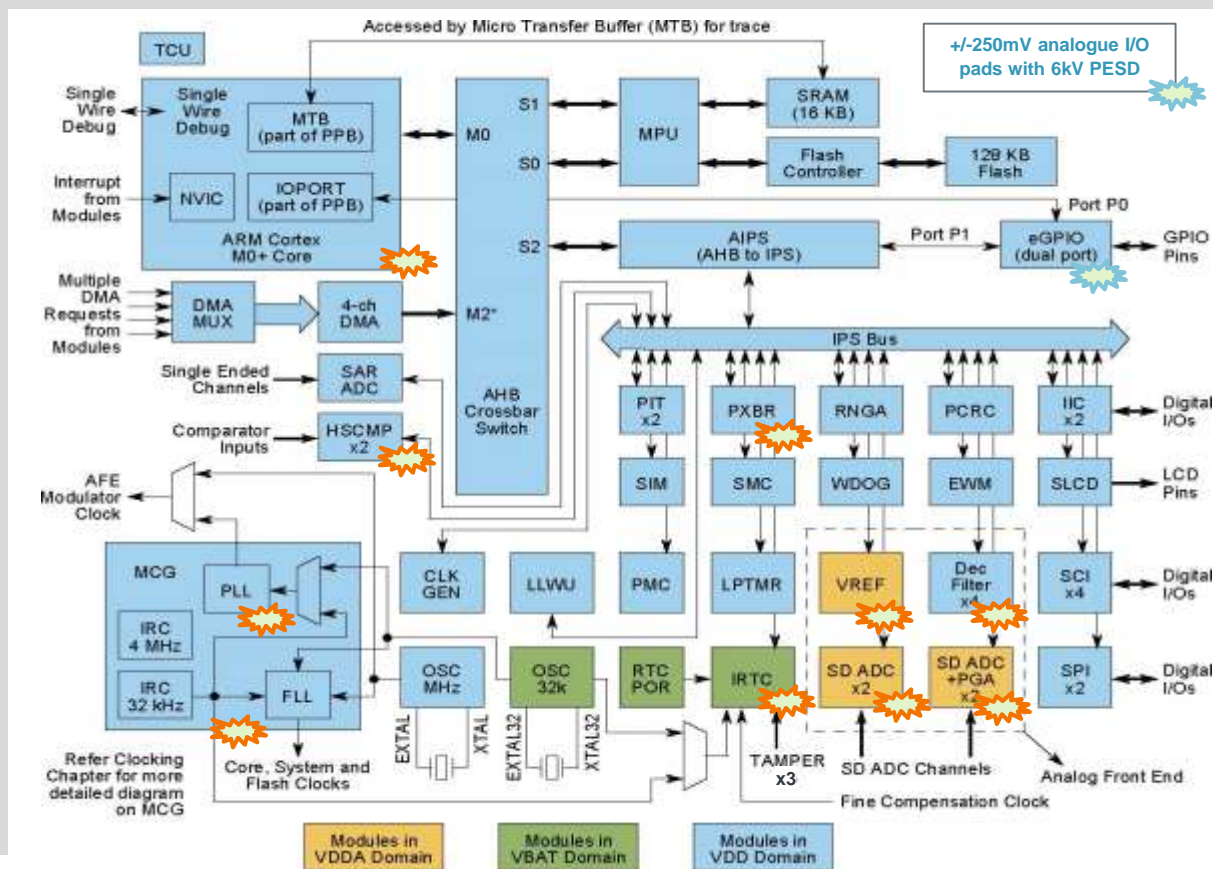
- Up to 68 with push pull, pull up/down select
- Up to 8 GPIO with filter
- Support for interruption on any edge
- Single cycle access for all GPIOs (Rapid GPIO)

Power Modes & Clock

- Many low power modes supported
- 2.7V to 3.6V Operating voltage with AFE
- 1.71V to 3.6V Operating voltage without AFE
- 1.71V-3.6V IRTC VBAT supply
- 32kHz or 4 MHz internal clock source
- 32.768kHz crystal oscillator

Package

- 100 LQFP, 64 LQFP and 44 LGA options
- -40 $^{\circ}\text{C}$ ~ +85 $^{\circ}\text{C}$ Temp



Analogue Subsystem (Overview)

1.2V Voltage Reference

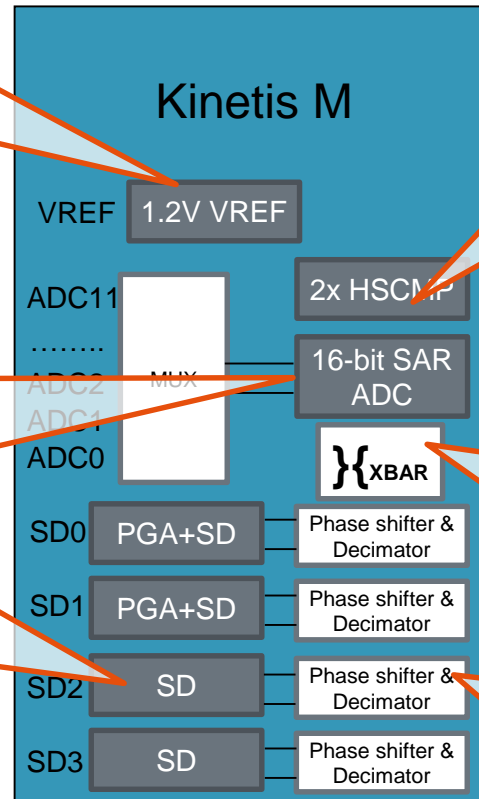
- Generates accurate reference voltage shared between PGA, SD ADC, SAR ADC and HSCMP

16-bit SAR ADC

- Conversion speed up to 818 ksp/s
- 12 single ended channels
- 4 result registers
- variety of triggering options

24-bit SD ADC and PGA

- Conversion speed up to 101 ksp/s on four channels
- Four SD ADC channels (two PGA)
- SW and HW triggering



High-Speed Comparator

- Two comparators, each with
- 6-bit DAC to provide selectable voltage reference
- Accepts a +/-250mV input signal range

Inter-peripheral Crossbar Switch

- Allows programmable digital interconnections between specific modules
- 33 input x 33 output multiplexer
- Interrupt or DMA request

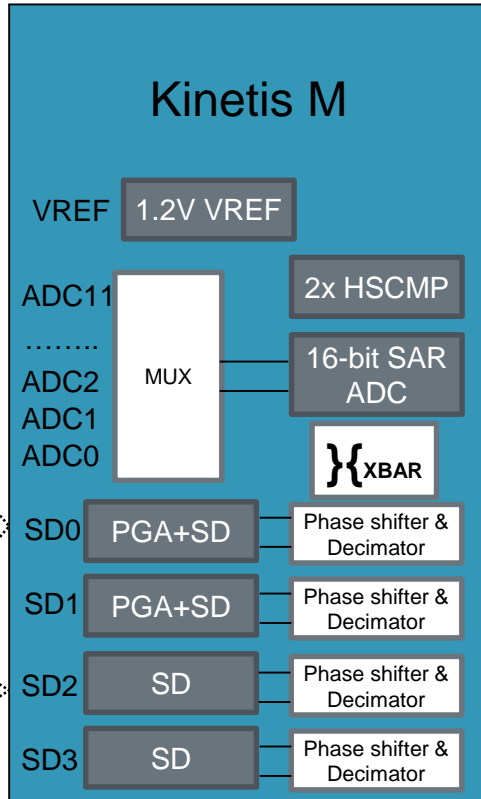
Phase Shifter and Decimator

- Phase shift compensation with resolution of 0.003° @ 50 Hz line frequency
- Capability to connect external galvanic ally isolated SD modulators

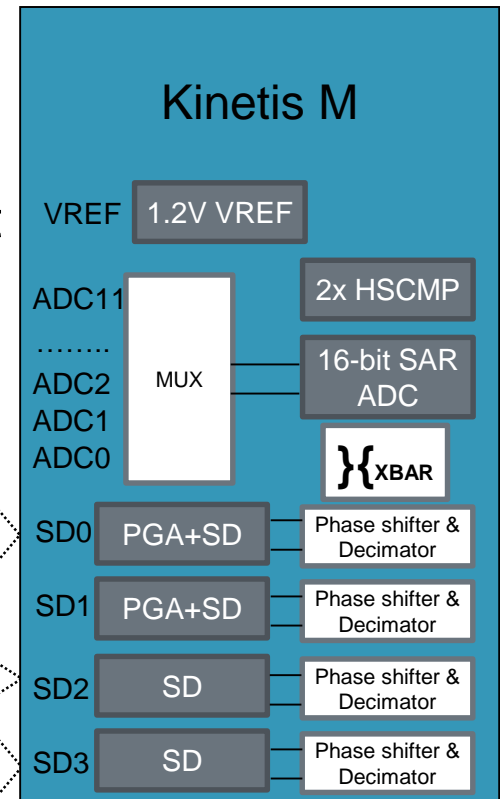
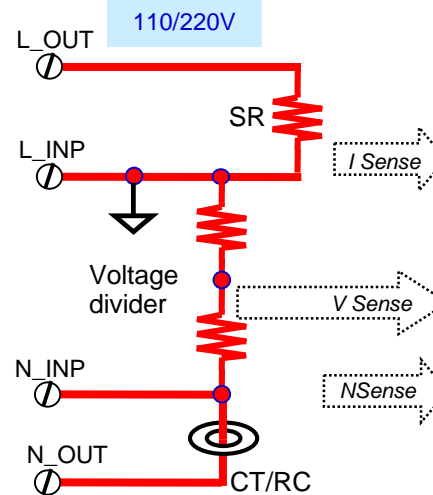
Kinetis M analogue and digital blocks allow realization most of electricity meter use-cases.

Analogue Subsystem (Electricity Meter Use-Cases)

- 1-Phase



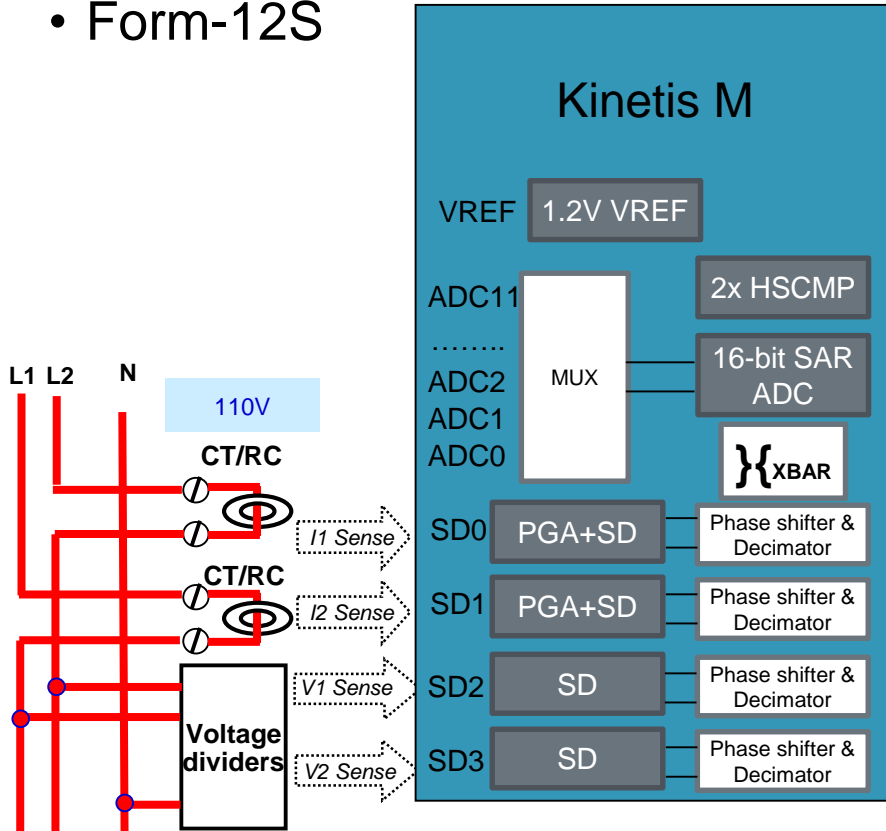
- 1-Phase with neutral current measurement



- All measurements performed by SD ADC
- Shunt resistor measurements amplified by Programmable Gain Amplifier (PGA)
- Phase shift between phase voltage and phase current measurements compensated by Phase Shifter block.

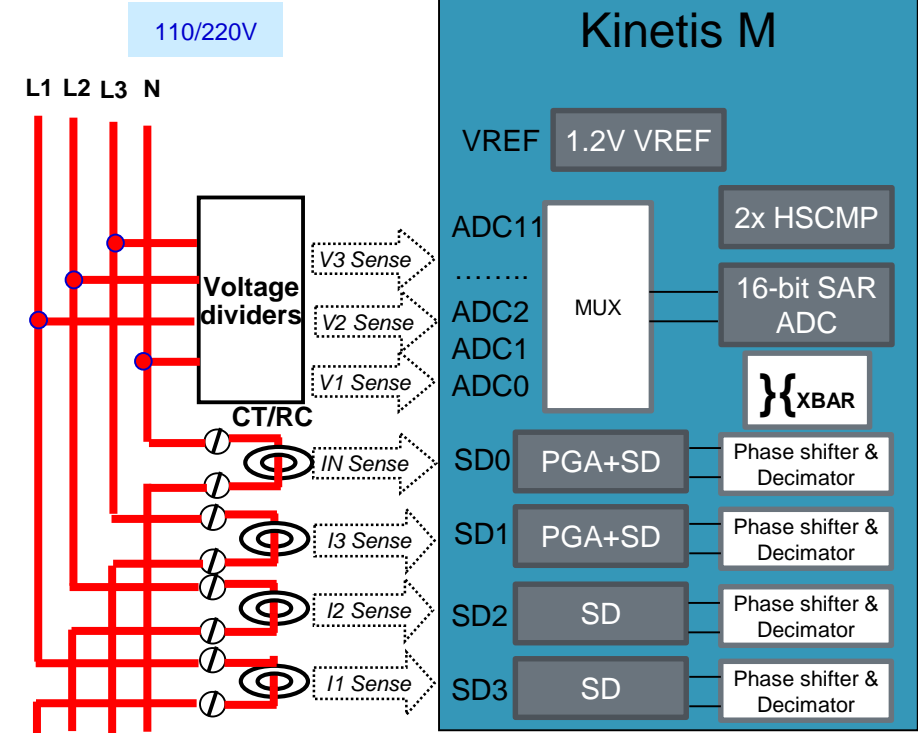
Analogue Subsystem (Electricity Meter Use-Cases – Cont'd)

• Form-12S



- All measurements performed by SD ADC
- Rogowski coil measurement optionally amplified by Programmable Gain Amplifier (PGA)
- Phase shift between phase voltage and phase current measurements compensated by Phase Shifter block.

• 3-Phase with neutral current measurement

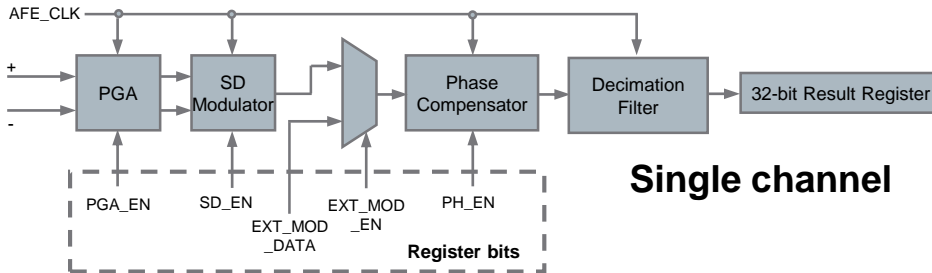


- Phase and neutral current measurement performed by SD ADC
- Phase voltage measurement performed by 16-bit SAR ADC
- Phase shift between phase voltage and phase current measurements compensated either numerically a FIR filter or by hardware using Quad Timer channels.

Analogue Subsystem (SD ADC and PGA)

• Blocks

- Four channels with 24-bit SD ADC (two PGAs)
- Phase Shifter & Decimator
- CPU/DMA Interface



• Electrical parameters

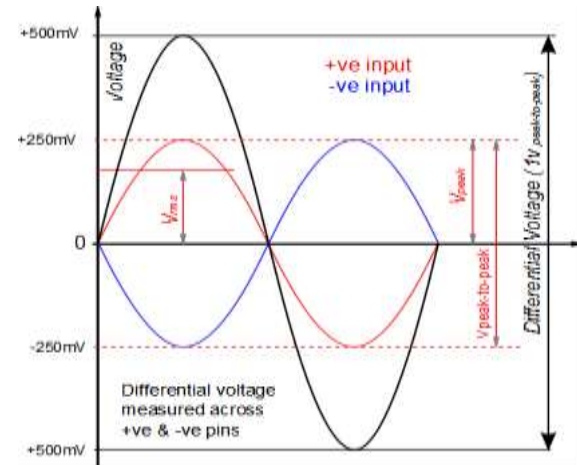
- Full operating voltage range: 2.7V to 3.6V
- **± 250 mV** (1 V_{P-P} differential, 0.5 V_{P-P} single ended) input range for both single ended and differential inputs
- Common mode voltage range of 0 to 0.8V
- SD modulator Signal-to-Noise Ratio:
 - Normal mode: 92dB @ ($F_s=6.144$ MHz, $OSR=2048$)
 - Low power mode: 82dB @ ($F_s=0.768$ MHz, $OSR=256$)

Operation Mode	PGA	Signal range (mV peak-peak)	SNR (dB @ $OSR=2048$)	Current (mA)
Normal	ON	31 (gainx32)	64 (74)	4.0
Low Power	ON	31 (gainx32)	52 (62)	3.1
Normal	OFF	1000	92	1.4
Low Power	OFF	1000	82	0.5

• Features

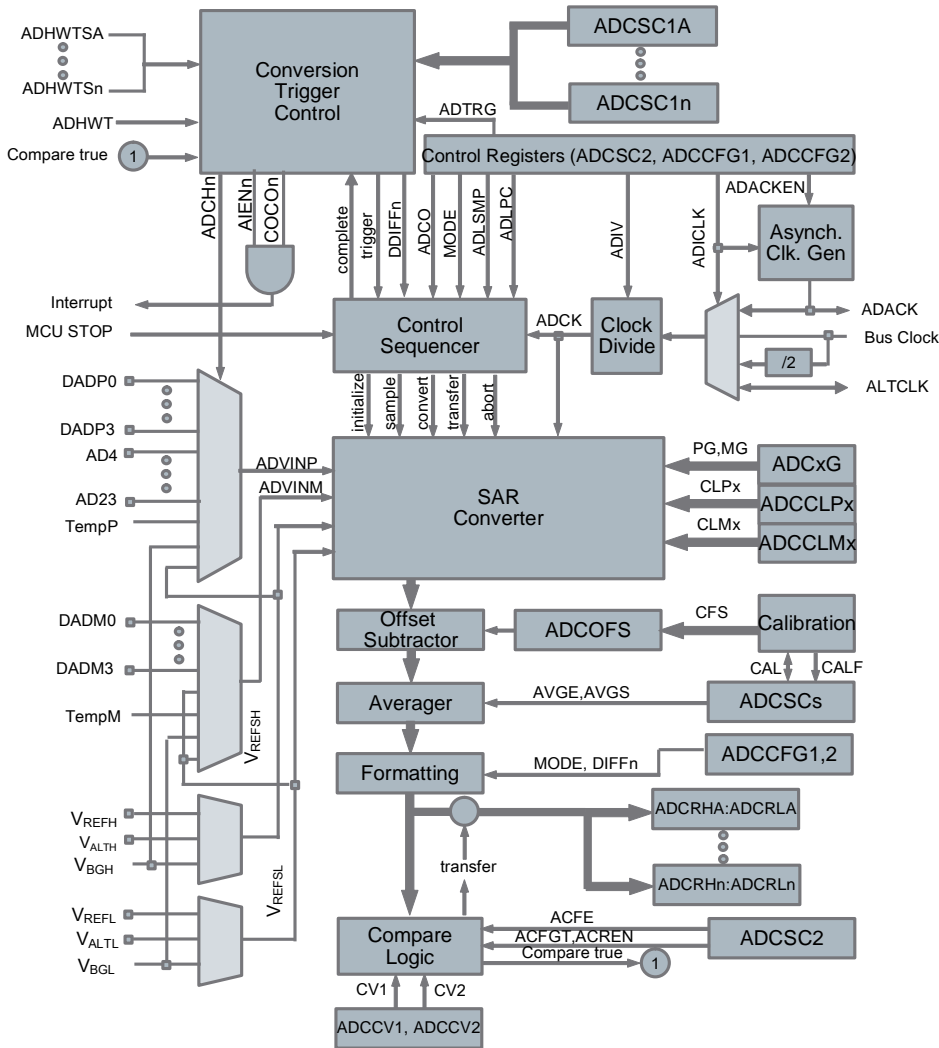
- Supports single and continuous conversions
- Support both software and hardware triggering
- Output sampling rates: 3 kHz, 6 kHz, 12 kHz, 24 kHz, 48 kHz, and 96 kHz
- Gain programmable from 1x to 32x
- **Dynamic phase shift compensation**
- Synchronized start operation
- Option to generate interrupt or DMA request on conversion complete

• SD ADC measurement range



VLPR	VLPW	STOP	VLPS	VLLSx
FF			FF (PLL disabled)	OFF

Analogue Subsystem (16-bit SAR ADC)



• Blocks

- Single 16-bit SAR ADC
- Four result registers allows measurement up to four samples without interrupt service
- Selectable voltage reference: SAR_VDDA, 1.0V bandgap from PMC, 1.2V VREF (from off-chip or internal source)

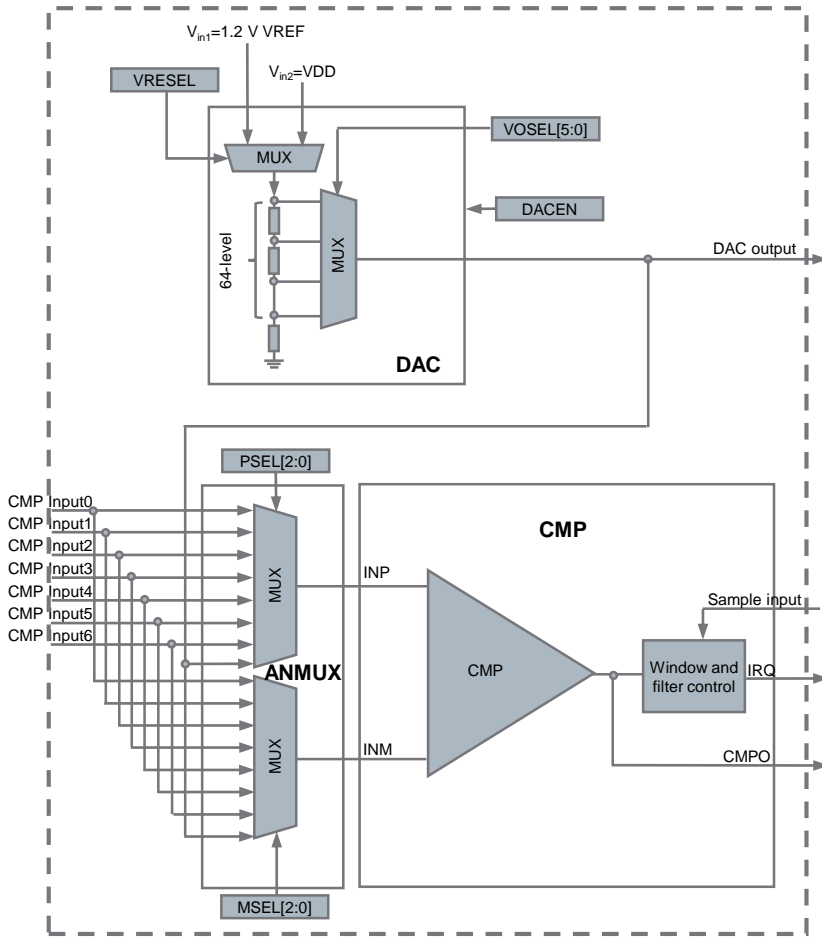
• Features

- Output Modes: single-ended 16-bit, 12-bit, 10-bit and 8-bit modes
- Output in right-justified unsigned format for single-ended
- Single or continuous conversion (automatic return to idle after single conversion)
- Configurable sample time and conversion speed/power
- Input clock selectable from up to four sources
- Programmable operation in some low-power modes for lower noise operation
- Asynchronous clock source for lower noise operation with option to output the clock
- Selectable asynchronous hardware conversion trigger with hardware channel select
- Automatic compare with interrupt for less-than, greater-than or equal-to, within range, or out-of-range, programmable value
- Temperature sensor
- Conversion rate up to 818ksps (≤ 12 -bit mode)
- Hardware average function
- Self-Calibration mode

VLPR	VLPW	STOP	VLPS	VLLSx
FF		FF (ADC internal clock only)		OFF



Analogue Subsystem (High-speed Comparator)



- 1) High-Speed Comparison mode
- 2) Low-Speed Comparison mode
- 3) OFF in VLLS0

• Blocks

- Two comparators
- Up to six external inputs and internal 6-bit DAC reference.
- Selectable voltage reference: VDD or 1.2V VREF (from off-chip or internal source)

• Features

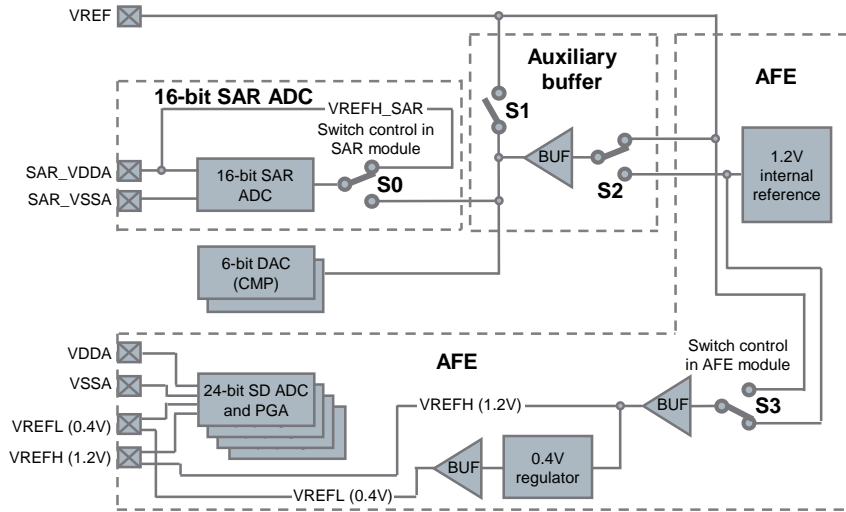
- CMP1 can accept a +/-250mV input with input common-mode voltage: 0 to 0.8V for both single ended and differential channels
- Continuous and sampled modes
- Programmable filter and hysteresis (5 .. 30 mV)
- Propagation delay from 20ns (high speed mode)
- CMP and 6-bit DAC sub-block supports trigger mode operation by LPTMR. Trigger sequence enables the CMP and DAC prior to performing compare and capturing the output

• Signal assignments

CMP Signals	CMP0	CMP1
CMP Input0	PTD0/CMP0P0/PXBAR_IN2/LLWU_P11/SCI0_RxD	PTB6/CMP1P0/LCD37
CMP Input1	PTD2/CMP0P1/PXBAR_IN3/LLWU_P10/SPI0_SCK/SCI1_RxD	PTC1/CMP1P1/LCD40/SCI3_CTS
CMP Input2	PTE6/CMP0P2/PXBAR_IN5/LLWU_P5/SWD_IO/I2C0_SCL/SCI2_RxD	SDADP2/CMP1P2
CMP Input3	PTC3/CMP0P3/LLWU_P13/LCD42/SCI3_RxD	SDADM2/CMP1P3
CMP Input4	PTD7/CMP0P4/PXBAR_IN4/LLWU_P7/I2C0_SCL/SCI3_RxD	SDADP3/CMP1P4
CMP Input5	PTI0/CMP0P5/PXBAR_IN8/SP1_MISO/SP1_MOSI/SCI1_RxD	SDADM3/CMP1P5
CMP Input6	Reserved	Reserved
CMP Input7	6-bit DAC reference	6-bit DAC reference
CMP Output0	PTA5/CMP0OUT/LLWU_P14/LCD29	PTD5/AD4/CMP1OUT/SP1_MISO/SCI1_RTS
CMP Output1	PTE4/CMP0OUT/LLWU_P7/SCI0_TxD/EWM_OUT	PTF2/CMP1OUT/LPTIM2/LLWU_P6/LCD2

VLPR	VLPW	STOP	VLPS	VLLSx
FF			HS ¹ / LS ² Compare	LS Compare ³

Analogue Subsystem (1.2V Voltage Reference)



Switch **S1** is meant for outputting 1.2V VREF on the device pin. When using externally supplied VREF, this switch should be open.

• Features

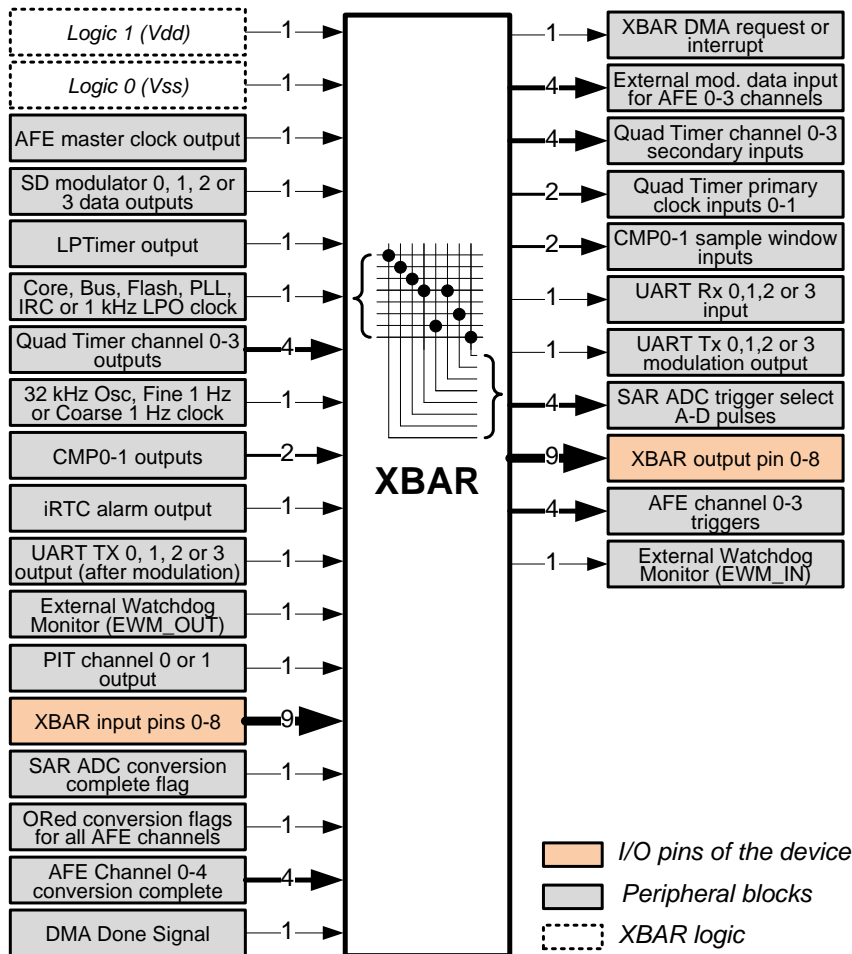
- Option to use internal or external voltage reference source
- Generates accurate reference voltage shared between 24-bit SD ADCs, PGAs, 16-bit SAR ADC, and CMPs
- Generates 1.2V and 0.4V voltages
- Low VREF gain drift over temperature of 33 ppm/C° (typ.)
- Programmable trim register with 0.5 mV steps
- Programmable mode of operation
 - Off
 - Bandgap enabled/standby (output buffer disabled)
 - Low power buffer mode (output buffer enabled)
 - High power buffer mode (output buffer enabled)

• Reference control switches

Switch Position				16-bit SAR ADC Reference	6-bit DAC (CMP) Reference	24-bit SD ADC and PGA Reference	VREF Pin Output
S0	S1	S2	S3				
UP	ON	DOWN	DOWN	3.3V SAR_VDDA	1.2V VREF Internal	1.2V VREF Internal	1.2V VREF Internal
UP	OFF	DOWN	DOWN	3.3V SAR_VDDA	1.2V VREF Internal	1.2V VREF Internal	-
DOWN	ON	DOWN	DOWN	1.2V VREF Internal	1.2V VREF Internal	1.2V VREF Internal	1.2V VREF Internal
DOWN	OFF	DOWN	DOWN	1.2V VREF Internal	1.2V VREF Internal	1.2V VREF Internal	-
UP	OFF	DOWN	UP	3.3V SAR_VDDA	1.2V VREF Internal	1.2V VREF External	-
UP	OFF	UP	DOWN	3.3V SAR_VDDA	1.2V VREF External	1.2V VREF Internal	-
DOWN	OFF	UP	UP	1.2V VREF External	1.2V VREF External	1.2V VREF External	-

VLPR	VLPW	STOP	VLPS	VLLSx
FF (low power buffer mode)				OFF

Analogue Subsystem (Peripheral Crossbar)



• Features

- Allows programmable interconnection between specific device modules
- **33 input x 33 output multiplexer**
- **Any input can be connected to any output**
- Edge detection with associated interrupt or DMA request generation for one output (XBAR_OUT0)

• Application use-cases

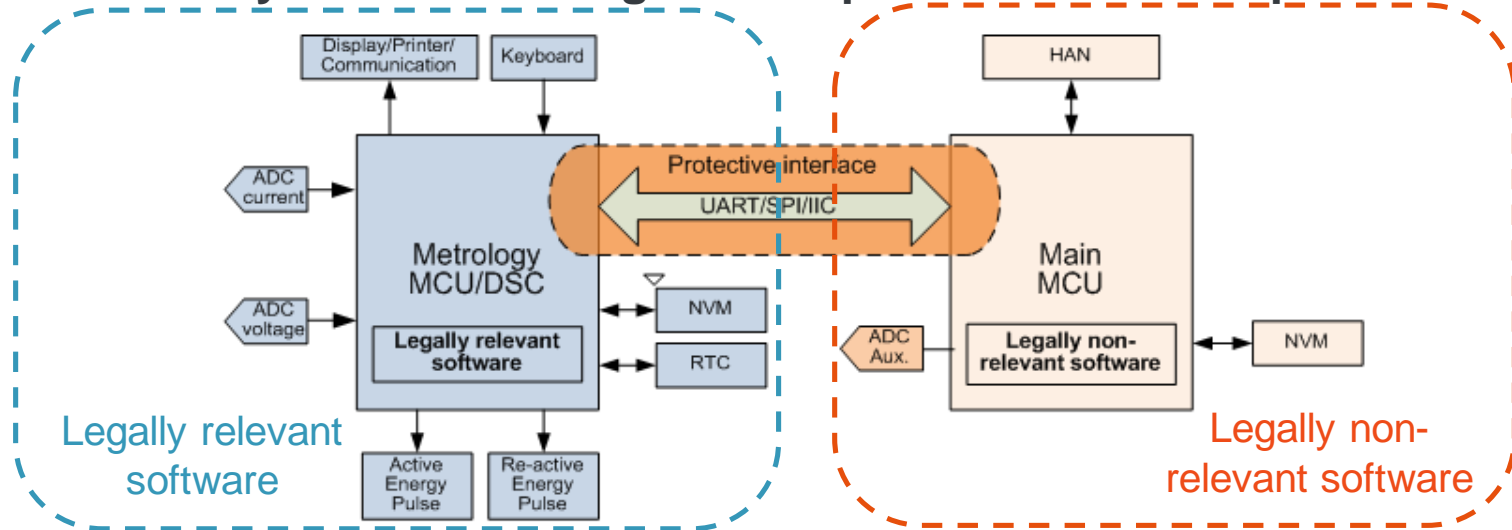
- SCI baud rate detection
- Monitoring internal signals
- Interfacing external SD modulators
- Triggering of SAR & SD ADC conversions
- IR communication support
- RTC Clock correction
- Supplying external signals to peripherals

VLPR	VLPW	STOP	VLPS	VLLSx
FF		Static (configured signal paths are fully functional but register states are retained)		OFF

Code Separation Technique in Metrology Applications

- **Legally relevant** software shall run in privileged mode exclusively preventing other software functions to influence its execution.
- Memory sections for **legally relevant** software, parameters and variables storage shall be protected against reading, writing and execution (R/W/E) from other software routines.
- On-chip peripherals controlled by the **legally relevant** software shall not be influenced by other software routines.

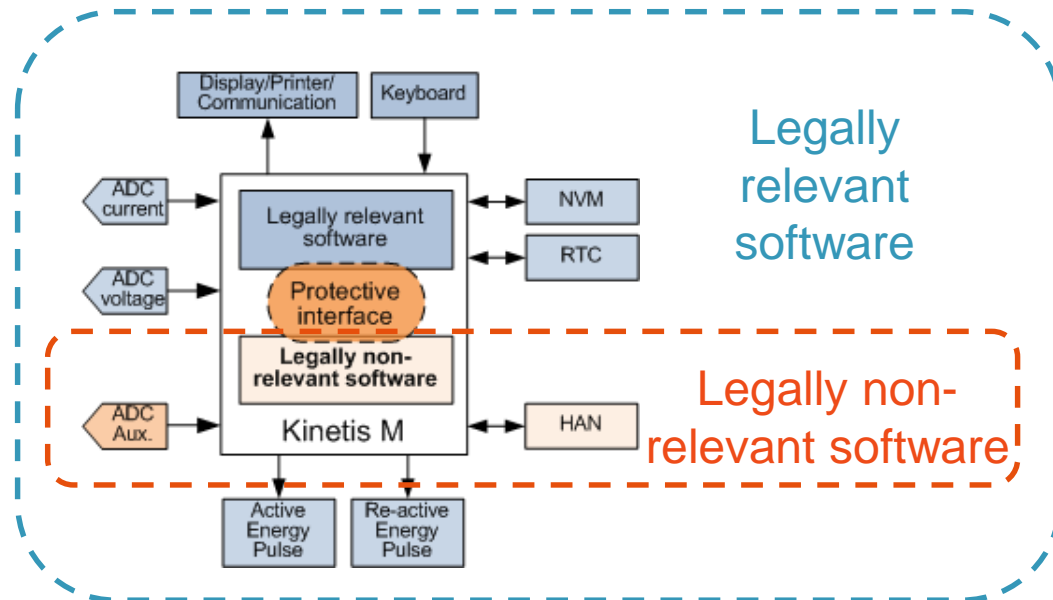
Traditional ways of maintaining code separation → two chip solution:



Literature: OIML D31, "General Requirements for Software Controlled Measuring Instruments", edition 2008: http://www.oiml.org/en/files/pdf_d/d031-e08.pdf
- WELMEC 7.2, "Software Guide (Measuring Instruments Directive 2004/22/EC)": http://www.welmec.org/fileadmin/user_files/publications/7-2_Issue4.pdf

Kinetis M Series MCUs - Single Chip Solution

- **Kinetis M platform** supports access permissions for privileged secure, user secure and user non-secure mode. These permission attributes can be either forced on a per bus master basis or inherited from the reference.
- Read, write and execute accesses to on-chip memories are protected by the **Memory Protection Unit (MPU)**.
- Read and write accesses to on-chip peripherals are handled by **Peripheral Bridge (AIPS-Lite)**. GPIO pins can also be accessed via the core's fast **IOPORT** (private bus supporting 1-cycle loads and stores).



Kinetis M Series MCUs – Legally Relevant/Non-relevant Software Separation HW Support

Miscellaneous Control Module (MCM)

Forces and enables control attributes for “CM0+” and “DMA” masters. Supports privileged secure and user secure/non-secure access modes.

Kinetis M Platform*

Supports privileged and user access modes.

DMA Controller Module

Conducts accesses to on-chip memory with either fixed or inherited access attributes. Supports privileged secure and user secure/non-secure access modes on a per channel basis.

Peripheral Bridge (AIPS-Lite)

Performs on-chip peripheral register space access control based on access attributes of each bus cycle.

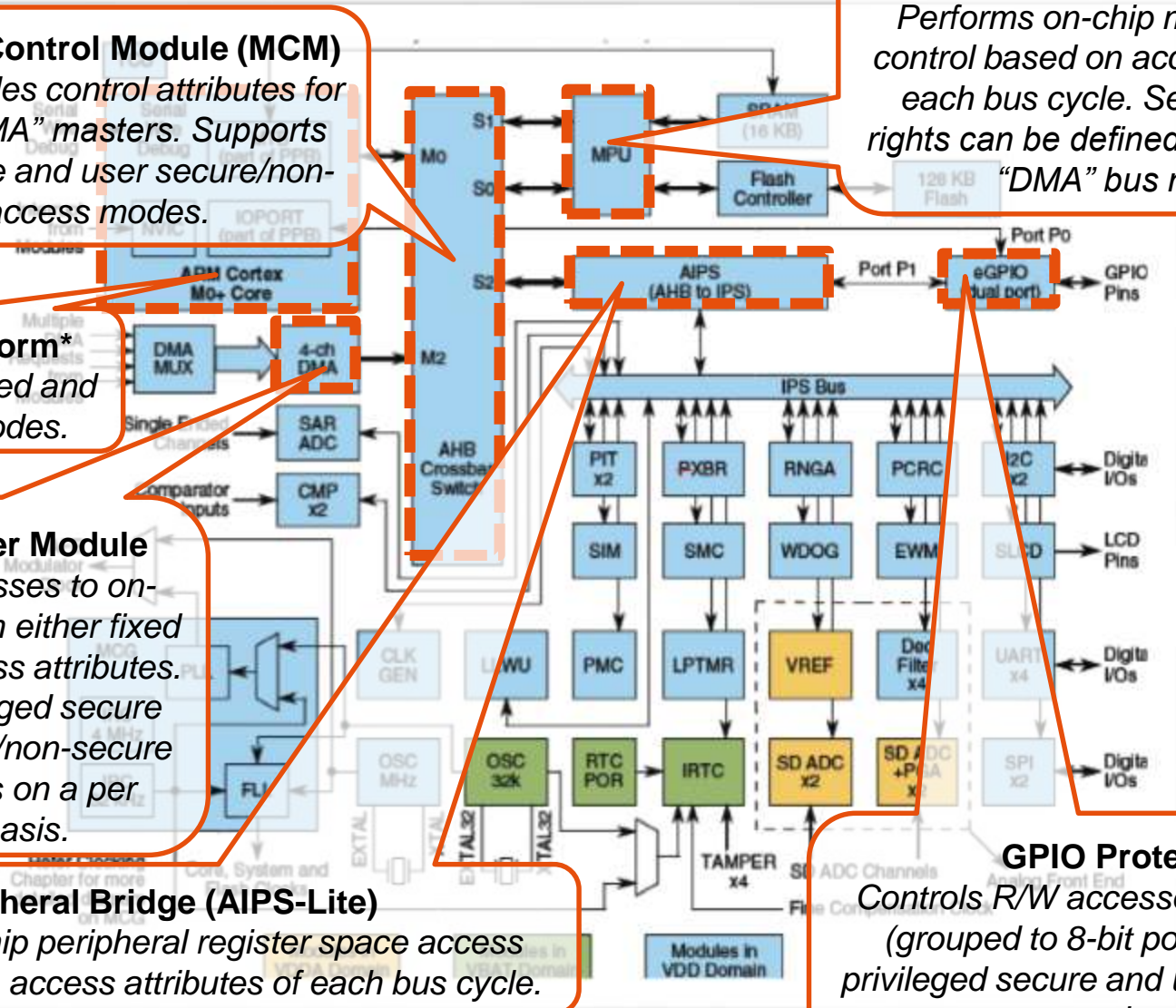
Memory Protection Unit (MPU)

Performs on-chip memory access control based on access attributes of each bus cycle. Separate access rights can be defined for “CM0+” and “DMA” bus masters.

GPIO Protection

Controls R/W accesses to GPIO pins (grouped to 8-bit ports). Supports privileged secure and user secure/non-secure access modes based on access attributes of each bus cycle.

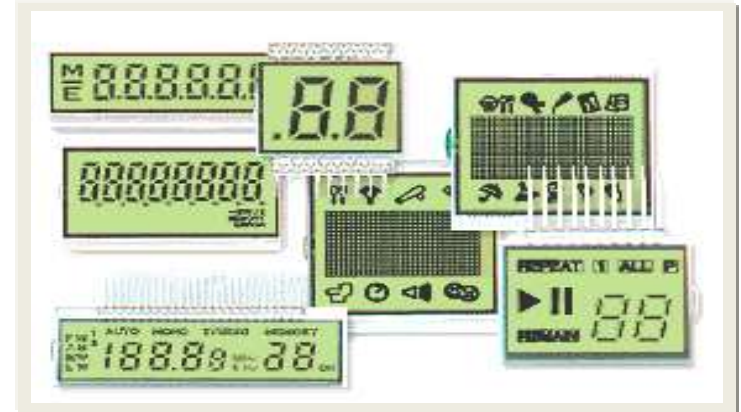
* The processor core supports privileged and user modes of execution. The platform adds the concepts of a processID register that supports the 3-state privilege model: privileged, user secure, user non-secure.





Segment LCD Controller

- **Segment fault detection capability**
 - Hardware support for segment LCD display errors
- **Up to by 8 multiplexing**
 - Fewer pins required to drive LCD segments
 - Up to 40 front plane signals (up to 4x40)
 - Up to 8 back planes signals (up to 8x36)
- **Low power blinking mode**
 - LCD glass blink capability in low power modes
 - Alternate display feature can be activated to display alternate data (i.e. blink flow in m³ and time)
- **Front and back plane re-assignment**
 - Any LCD pin can be a front plane or backplane pin or GPIO function
- **Internal charge pump provides voltage required to power LCD glass**
 - Internally regulated voltage for constant contrast across MCU VDD
 - Trim register for software contrast control
 - Drive for 3V LCD glass



Async operation = Fully functional with alternate clock source, provided the selected clock source remains enabled

VLPR	VLPW	Stop	VLPS	VLLSx
FF	FF	Async operation	Async operation	Async operation ¹

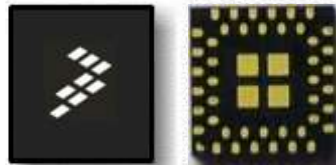
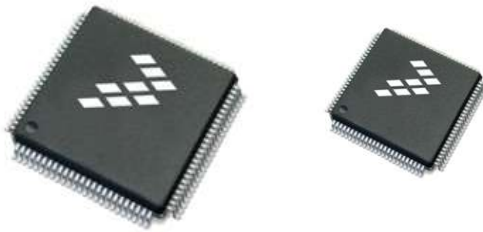


Low-Power Modes

Typical Power Modes in an embedded system		Power Modes	Recovery Time	Target Typical I _{dd} Range
Run	<p><u>Leading Dynamic Power</u></p> <ul style="list-style-type: none"> ARM Cortex M0+ core Innovative low-power process technology (C90TFS) Low-power focused platform design 	Run (AMO)	-	≥ 6.17mA @50MHz
		VLPR (AMO)	-	≥ 248uA @ 2MHz
		Wait (AMO)	-	≥ 3.81mA @50MHz
		VLPW (AMO)	4us	≥ 162uA @ 2MHz
Wait		Stop	4.31us	312 uA
		VLPS	4.31us	8.56 uA
Stop	<p><u>Freescale Adds Low Leakage Wake-up Unit</u></p> <ul style="list-style-type: none"> Enables complete shut-down of core logic, including WIC, further reducing leakage currents in all low power modes Supports 16 external input pins and 5 internal modules as wakeup sources, <i>extend the low power wakeup capability of internal modules to even lower power modes.</i> Wakeup inputs are activated in VLLSx modes 	VLLS3	143us	1.98 uA
		VLLS2	144us	1.24 uA
		VLLS1	239us	891 nA
		VLLS0	239us	357 nA
		VBAT	<ul style="list-style-type: none"> RTC operational on battery VDD/VDDA are not powered 	Standby

Package Options & Device Features

100 LQFP **64 LQFP**
14 x 14 mm² **10 x 10 mm²**



44 LGA
5 x 5 mm²

Configuration/Module	Packages		
	100 LQFP (14 x 14 mm ²)	64 LQFP (10 x 10 mm ²)	44 LGA (5 x 5 mm ²)
Core, Platform and Debug			
DMA	4 ch		
MPU	yes		
Peripheral XBAR (I/O supported)	yes		
Single Wire Debug (SWD)	yes		
System Security and Integrity			
Cyclic redundancy check (CRC)	yes		
RNGA (Random Number Generator)	yes		
Watchdog timer	yes		
External Watchdog Monitor	yes		
Passive (Active) Tamper Pins	3 (one pair)	1 (NA)	1 (NA)
Embedded Memory			
Flash memory (KB)	128/64		
RAM (KB)	16		
Clock Generator			
MCG	FLL, Internal OSC (32 kHz or 4/2 MHz), PLL		
Real Time Clock (32 kHz OSC)	yes		
Timer/PWM			
QuadTimer	4 ch		
Low power timer (LPTMR)	1		
Periodic Interrupt Timer(PIT)	2		
Communication Interfaces			
UART	4	4	2
SPI	2		
I2C	2	2	1
Analog			
24-bit Analog Front End (PGA)	4 (2)	3 (2)	4 (2)
16-bit SAR ADC	12 ch	6 ch	5 ch
1.2V VREF	yes		
CMP (Number of Channels)	2 (12)	2 (8)	2 (6)
Human Machine Interface			
Segmented LCD	4x40 (8x36)	4x24 (8x20)	NA
Total GPIO pins	68	38	20



Kinetis M Series MCU Advantages for Electricity Metering

Needs	Kinetis M Solution
Computation	Lowest power Cortex-M0+ core (32x32 multiply in 1 cycle) up to 48MHz.
Low Power	Less than 124.4uA/MHz VLPR Current ¹ Down to 357nA @VLLS0 (POR disabled) ² Low Power Boot with less than 2.33mA peak current ³
User Interface	Up to 4x40 (8x36) segment LCD driver operating in all low power modes.
Communication	Up to 4 UARTS, 2 SPIs and 2 IIC.
Memory Scalability	From 64 KB to 128 KB of Flash. 16 KB of RAM Program longword execution time (65us)
Time Keeping	Auto compensated RTC with high speed calibration, 5 ppm accuracy, 0.88 ppm resolution of the 1Hz pulse output and operating in all low power modes.
Analog Modules	Highest linearity and resolution AFE with 4x24bit SD with 92 dB SNR Low VREF gain drift over temperature of 33ppm/°C Combined gain temperature drift of the PGA, SD ADC and Internal 1.2 VREF blocks (150ppm/°C) High Speed 16-bit SAR ADC and CMP.
Security	Passive and active tamper pins. HW support for legally relevant software separation. Random Number Generator (NIST: SP800-90)
Robustness	I/O pads withstanding 4 kV ESD and 6 kV PESD

¹) Typ. 248.8uA @ 2 MHz core, system, bus clock, and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.

²) If independent RTC including 32 kHz oscillator operates then device consumes additional 1.3uA from VBAT terminal.

³) Measured for 1.7ms linear supply voltage ramp with 3.26 V steady-state value; main function executed in 4.1 ms from applying supply voltage.

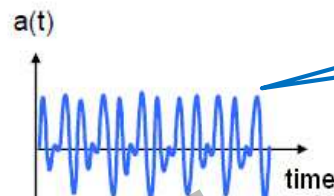
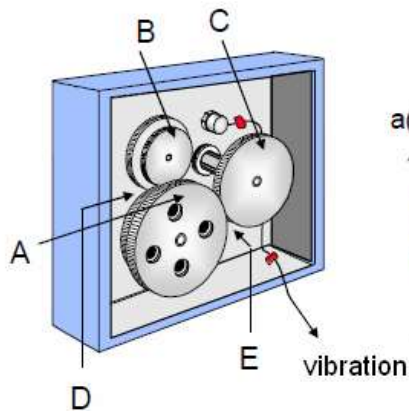


Agenda

- Introduction to electricity metering
- Kinetis M series MCUs
- ✓ Electricity metering algorithms
- Electricity meter reference designs
- Kinetis M development tools
- Mastering MCU programming...
- References

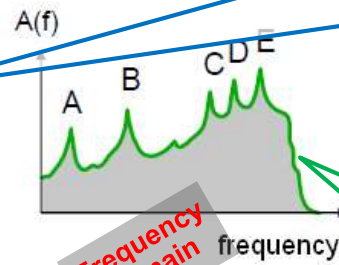
Freescale Algorithms for Electricity Metering

- Electricity meter vendors require algorithms supporting calculations that adhere to either IEC/MID or ANSI C12 standards.
- Freescale offers algorithms that calculates metering quantities in either time or frequency domain



Time domain

- each events are mixed together in the time domain



Frequency domain

- each events are separated in frequency domain

Filter-based metering algorithm

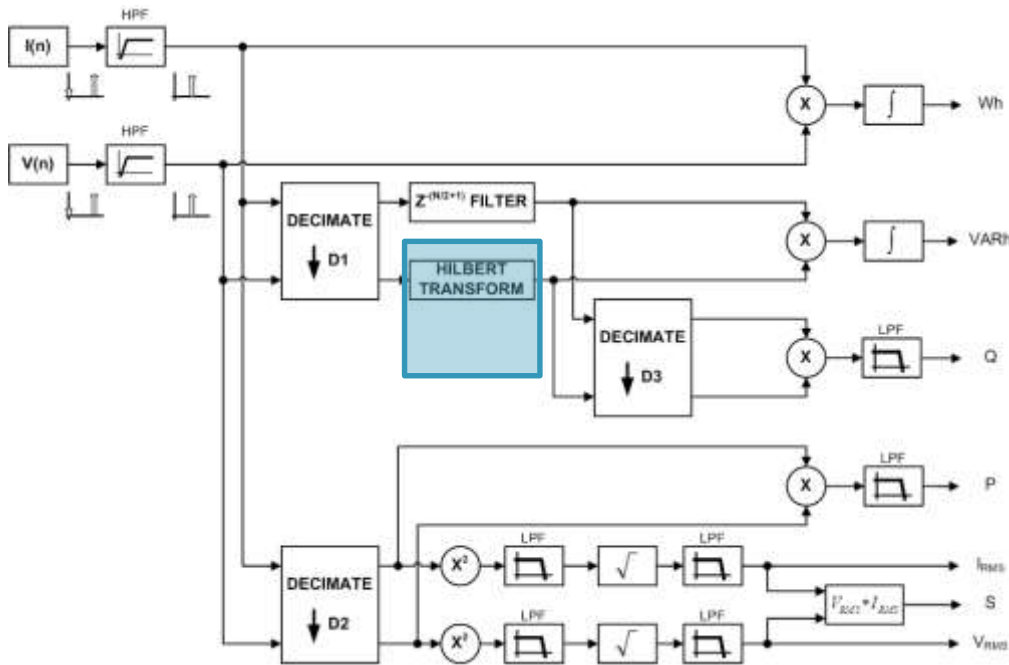
- processes signals in time domain
- leverages IIR filters
- based on elementary 32/64-bit fractional arithmetic

FFT-based metering algorithm

- processes signals in frequency domain
- leverages DFT computation
- based on elementary 32/64-bit fractional arithmetic

An algorithm must be seen to be believed. - Donald Knuth

Filter-based Metering Algorithm – Block Diagram

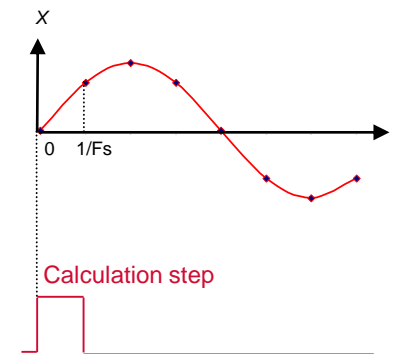
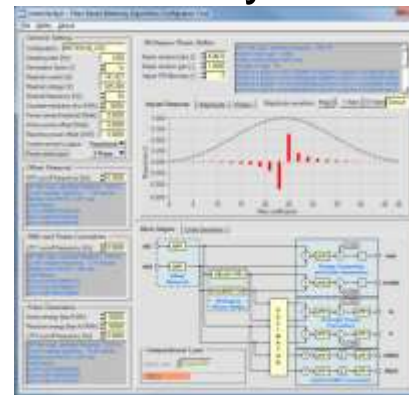


- Executes when power meter is supplied from the mains
- Uses high-pass and low-pass IIR filters
- Hilbert filter is used for computing reactive power and energy
- Software configuration tool is available to setup structure, filter coefficients, and generate C-header file.
- Active energy counter updated at every calculation step.

where: “Fs” is sampling frequency
 “D3” is decimation ratio calculated as D1-D2+1
 “N” is order of the Hilbert Transformation Filter.

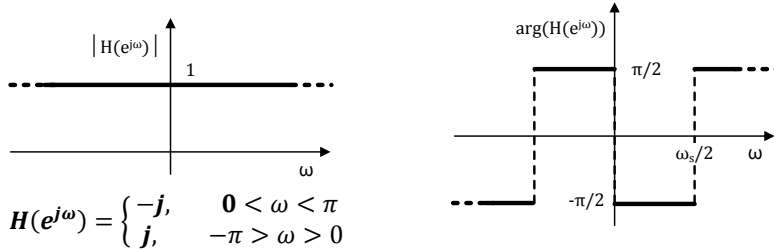
Time domain

For more information see AN4265

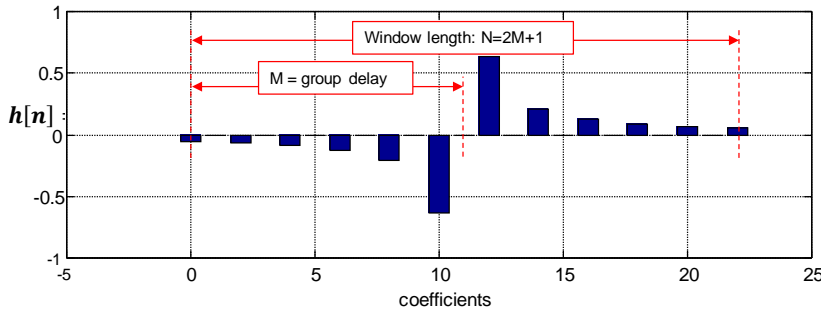


Filter-based Metering Algorithm – Hilbert Transformer

• Magnitude and phase response



• FIR Approximation impulse response of the ideal Hilbert Transformer

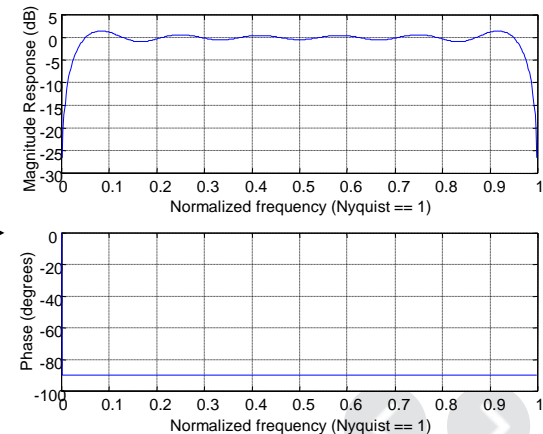
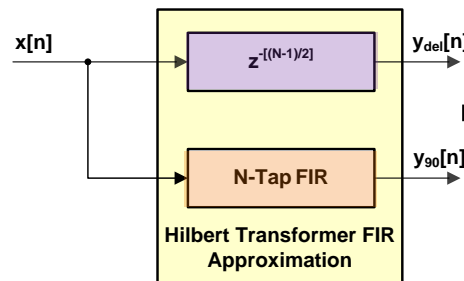


$$h[n] = \begin{cases} \frac{I_0\{\beta\sqrt{(1 - [(n - n_d)/n_d]^2)}\}}{I_0\{\beta\}} \frac{2 \sin^2(\pi(n - n_d)/2)}{\pi(n - n_d)}, & 0 \leq n \leq N - 1 \\ 0, & \text{others} \end{cases}$$

• Equations and practical implementation for N=23, M=11 and \beta=0.

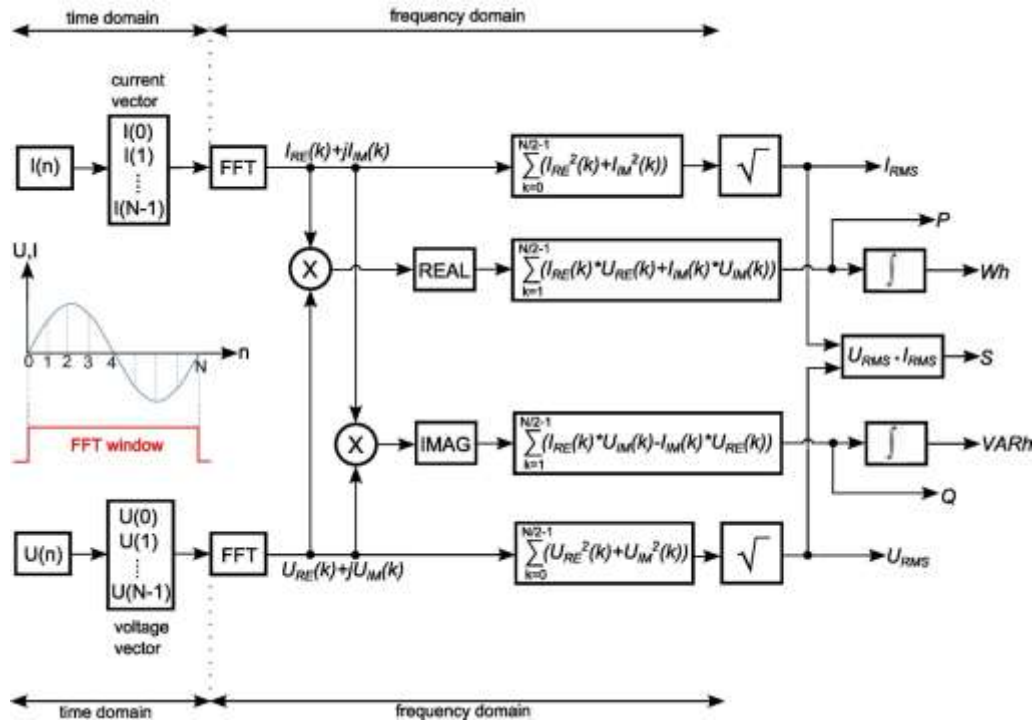
$$y_{del}[n] = 1.0 * x[n-11]$$

$$y_{90}[n] = -0.0579 * x[n] - 0.0707 * x[n-2] - 0.0909 * x[n-4] - 0.1273 * x[n-6] - 0.2122 * x[n-8] - 0.6366 * x[n-10] + 0.6366 * x[n-12] + 0.2122 * x[n-14] + 0.1273 * x[n-16] + 0.0909 * x[n-18] + 0.0707 * x[n-20] + 0.0579 * x[n-22]$$



- Uses a special FIR filter for shifting a phase voltage waveform by 90°
- Ideal Hilbert transformer FIR approximation impulse response computed with the help of **ideal Hilbert transformer impulse response** and **Kaiser Window coefficients**.
- Hilbert transformer FIR approximation block design is fully automated by the software configuration tool.

FFT Metering Algorithm – Block Diagram



- Number of samples (N) must be power-of-two (32,64,128,etc.)
- Ensures that processed samples represent full signal period
- Use linear interpolation technique to generate exactly power-of-two samples on a metering device with SD ADC for entire signal period.
- Sampling frequency must be at least 2x or higher than the maximum frequency included in input signal.

Where:

“N” is number of samples

“RE” is real part of the vector

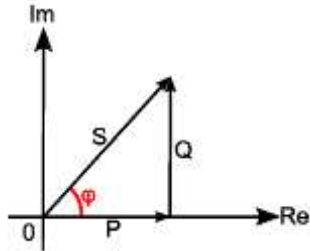
“IM” is imaginary part of the vector

For more information see **AN4255** and **AN4847**

FFT Metering Algorithm - Computation

Complex power (in Cartesian form) is defined as :

$$\sum_{k=1}^{\frac{N}{2}-1} (I_{RE}(k) - jI_{IM}(k)) \cdot (U_{RE}(k) + jU_{IM}(k)) = \sum_{k=1}^{\frac{N}{2}-1} (I_{RE}(k) \cdot U_{RE}(k) + I_{IM}(k) \cdot U_{IM}(k) + jU_{IM}(k) \cdot I_{RE}(k) - jU_{RE}(k) \cdot I_{IM}(k))$$



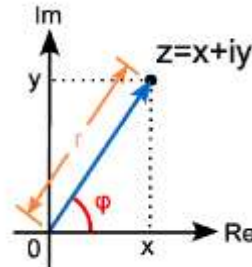
Real part of complex power:
Active power

Imaginary part of complex power:
Reactive power

Root Mean Square computing (in Cartesian form) is defined as :

$$I_{RMS} = \sqrt{\sum_{k=1}^{\frac{N}{2}-1} (I_{RE}^2(k) + I_{IM}^2(k))}$$

$$U_{RMS} = \sqrt{\sum_{k=1}^{\frac{N}{2}-1} (U_{RE}^2(k) + U_{IM}^2(k))}$$



Where: $I_{RE}(k), U_{RE}(k)$ are real parts of k -th harmonics of input current/voltage
 $I_{IM}(k), U_{IM}(k)$ are imaginary parts of k -th harmonics of input current/voltage

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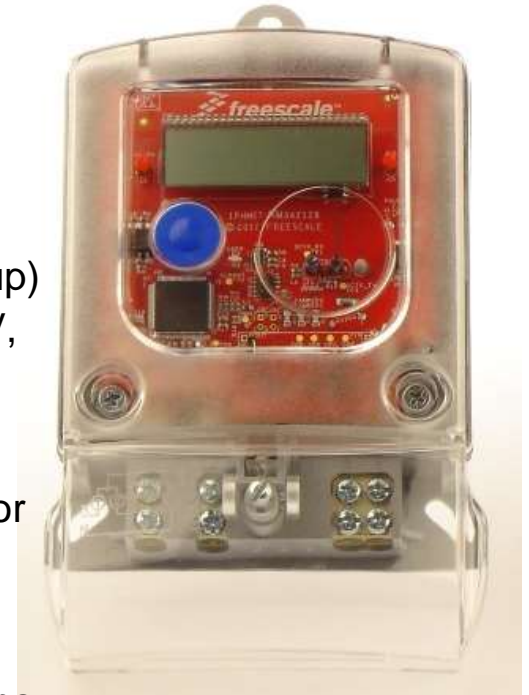
1-Phase Power Meter Reference Design with Shunt Resistor

Features

- **5 to 120A** current range (nominal current is 5A; peak current is 154A).
85 to 264V, 50/60 Hz voltage range
- **Accuracy class: B or C (active energy EN50470-3) and 3% or 2% (reactive energy EN62053-23)**
- Line frequency measurement (for precision zero-cross detection)
- Cost-effective **shunt-resistor** sensing circuit implementation
- Low-power modes including the use of **built-in RTC** (Li-battery back-up)
- **4x22 segment LCD**, including charge pump (values shown on LCD: V, A, W, Var, VA, kWh, kVarh, $\cos \phi$, Hz, time, date)
- **An upper and lower tamper meter cover monitoring with time stamp**
- **IEC1107 infrared hardware interface & Isolated (4kV) RS232** port for monitoring & SW upgrade
- **LED pulse** outputs (kWh, kVarh)
- **EMC proven** design (EN61000-4-2, EN610004-4)
- RF connector supporting SubGHz or 2.4 GHz 802.15.4 communications
- Xtrinsic 3-axis low power tilt sensor for electronics tamper detection (optional)

Software provided

- Application framework, Filter-based metering algorithms



100 LQFP
14 x 14 mm²



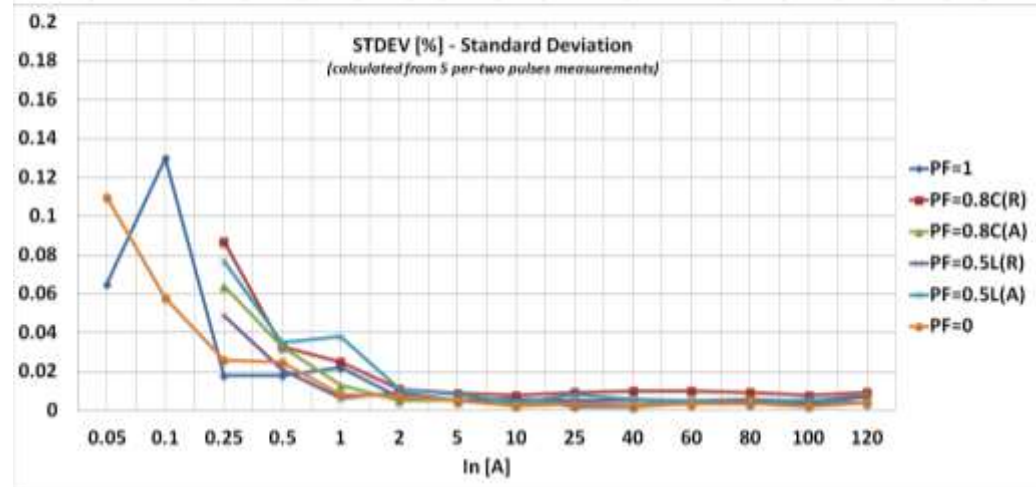
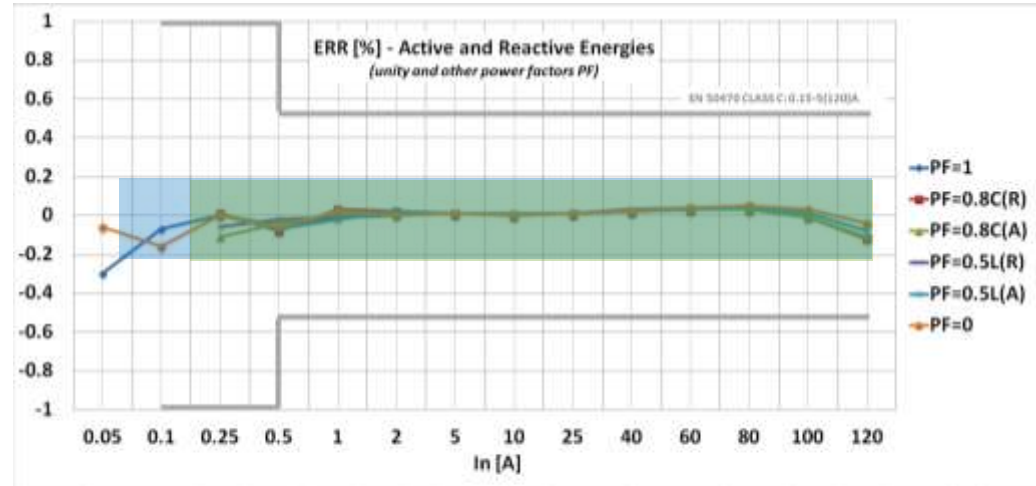
1-Phase Power Meter RD

– Performance

- Complies with active energy EN50470 Class C: 0.15-5(120)A
- MCU clocked by 12.288MHz
- Uses 140 $\mu\Omega$ shunt resistor



Courtesy of
Zhongshan Weiqi Electronic



PGA	SD Modulator Mode/Clock Rate	OSR	Measurement Bandwidth (kHz)	MCU Power Consumption (mA)	Performance (PF=1)	Performance (All PF)
x16	Normal / 6.144 MHz	1024	3.0	10.88	+/-0.2% @ 0.075→120A (1600:1)	+/-0.2% @ 0.25→120A (480:1)



2-Phase Power Meter Reference Design with CTs

Features

- Current Class: **CL200** (TA=30A, Max. Current **200A**, Starting Current **50mA**)
- Nominal Voltage: **120VAC ± 20%**, Nominal Frequency: **60Hz ± 10%**
- Accuracy class: **ANSI C12.20, Class 0.2**
- Default Watt-hour (VAR-hour) constant: **$K_h=0.2$** (range from 0.001 to 10)
- Line frequency measurement (for precision **zero-cross** detection)
- Current Sensor: Current Transformer (**CTR 2000:1**), type **CHEM 9912192**
- Low-power modes including the use of **built-in RTC** (Li-battery back-up)
- **8x20 segment LCD** including charge pump and one user LED
- **LED pulse** outputs (kWh, kVARh) and optically isolated pulse output (via an optocoupler)
- Electronic tamper detection via a magnetometer **MAG3110** and an accelerometer **MMA8491Q**
- **ANSI C12.18-2006** Infrared Interface, optically isolated **RS232** serial interface (optional only)
- RF communication supporting **2.4 GHz IEEE 802.15.4** or **900MHz RF Mesh IEEE 802.15.4g/e + WPAN/IPv6** connectivity
- Enclosure according to ANSI C12.10-2004, **Form 12S** (or Form2S)

Software provided

- Application framework, FFT-based metering algorithms



100 LQFP
14 x 14 mm²

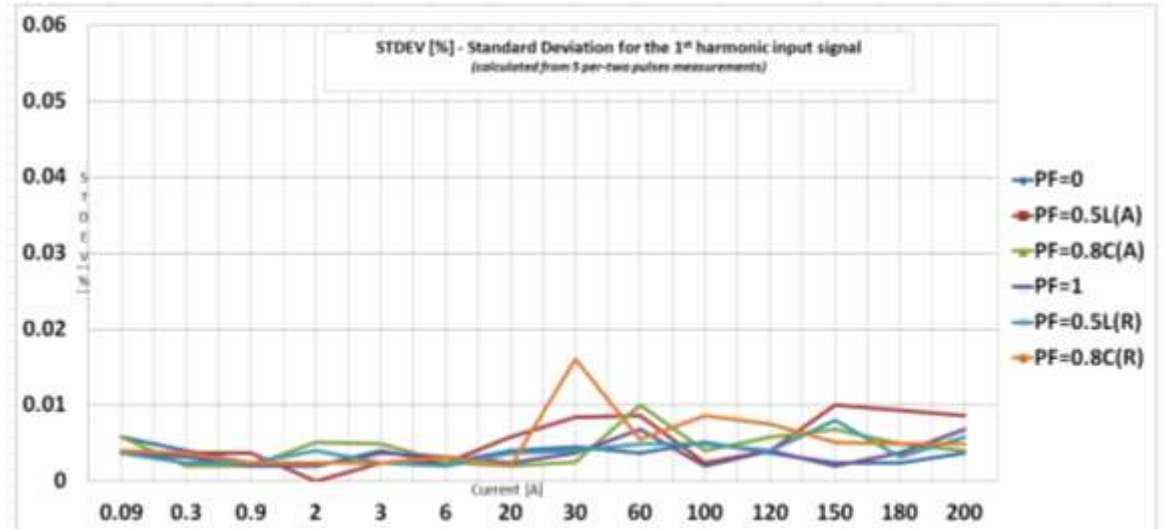
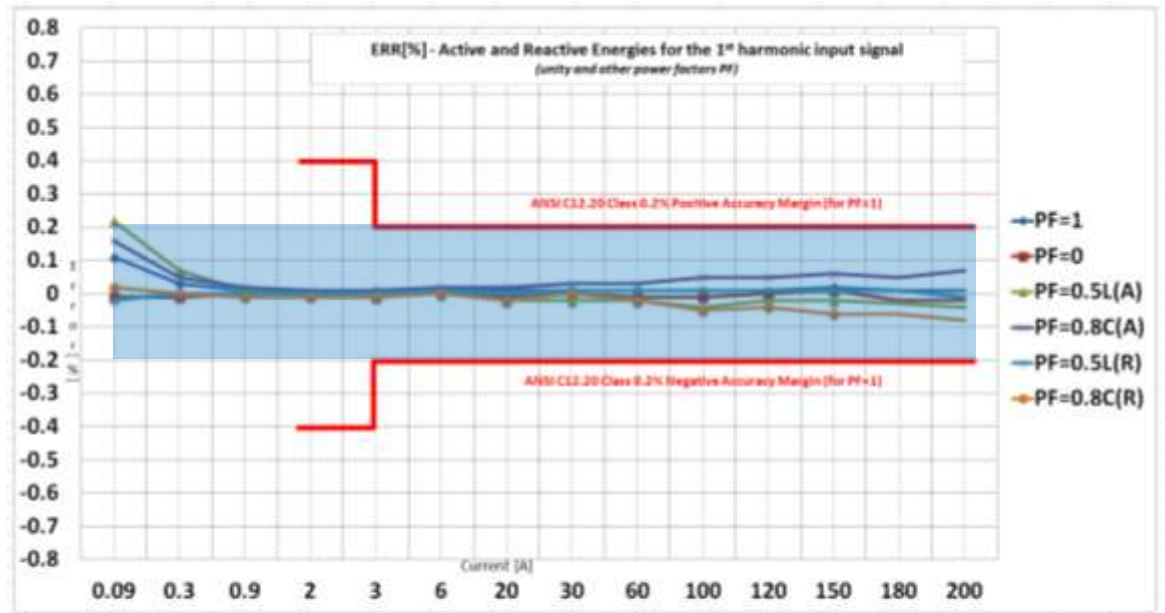


2-Phase Power Meter RD – Performance

- Complies with active energy ANSI C12.20 Class 0.2% (30)200A
- MCU clocked by 48MHz
- Uses current transformers



Courtesy of VACUUMSCHMELZE



PGA	SD Modulator Mode/Clock Rate	OSR	Measurement Bandwidth (kHz)	MCU Power Consumption (mA)	Performance (PF=1)	Performance (All PF)
off	Normal / 6.144 MHz	1024	3.0	16.3	+/-0.2% @ 0.090→200A (2222:1)	

3-Phase Power Meter Reference Design with CTs

Features

- 5(100)A current range, nominal current is 5A, peak current is 100 A
- Tested with range 0 – 240A (320A)
- Four quadrant measurement
- 85V...264V, 50/60Hz voltage range
- Active and Reactive energy accuracy IEC50470-3 Class C, 0.2%
- Line frequency measurement (for precision zero-cross detection)
- Current transformers sensing circuit implementation
- Cost-effective bill of materials (BOM)
- Low-power modes effectively implemented, including the use of the built-in RTC
- LCD display, 4x44 segments including charge pump
- Values shown on the LCD: V,A,W,Var,VA, kWh, kVarh, Hz
- Magnetic field electronic Tamper detection via ELECTRONIC TAMPER MAG3110 sensor and tamper buttons
- Built-in user push-button
- LEDs pulse outputs (kWh, kVARh)
- IEC1107 infrared hardware interface or Optically isolated RS232 interface
- Communication interface connector, could be use for (I2C Daughter Card) for connection to a ZigBee® network

Software provided

- Application framework, Filter-based metering algorithms



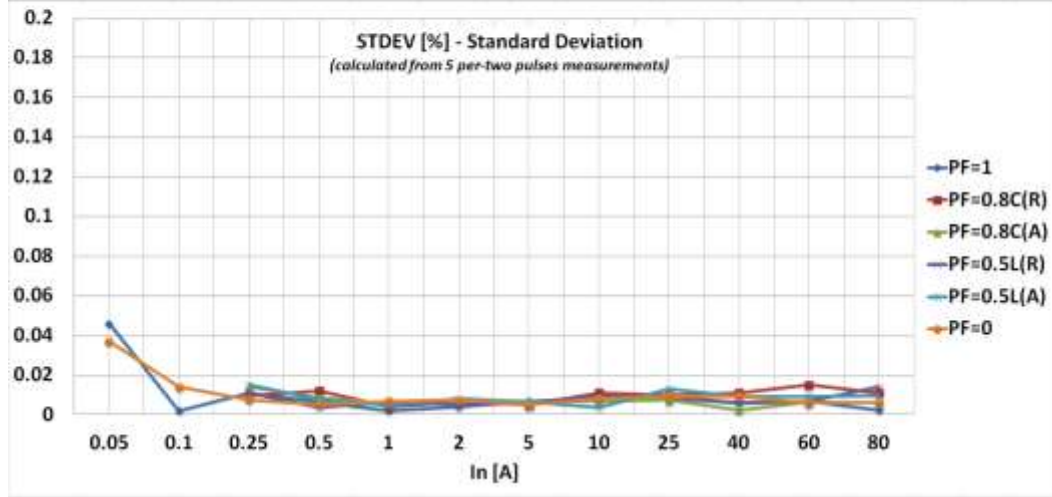
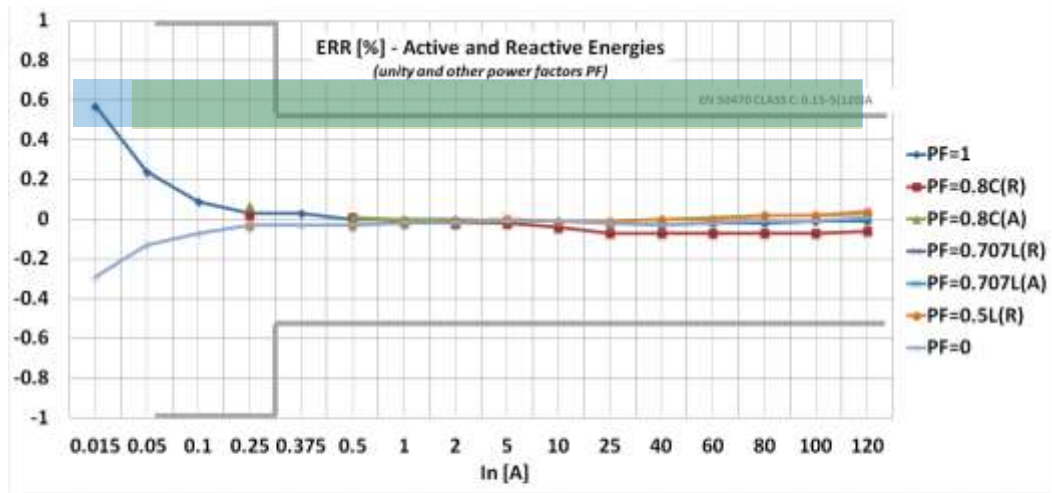
100 LQFP
14 x 14 mm²



3-Phase Power Meter RD – Performance

- Complies with active energy EN50470 Class C: 0.15-5(120)A

- MCU clocked by 48MHz
- Uses current transformers



PGA	SD Modulator Mode/Clock Rate	OS R	Measurement Bandwidth (kHz)	MCU Power Consumption (mA)	Performance (PF=1)	Performance (All PF)
off	Normal / 6.144 MHz	1024	3.0	18.00	+/-0.1% @ 0.100→120A (1200:1)	+/-0.1% @ 0.25→120A (480:1)



3-Phase Power Meter Solution Based On Kinetis KM14/KL36 MCUs

Features

- 5 to 60A current range ($I_b = 5A, I_{max} = 60A$)
- 135 to 600V, 50/60 Hz voltage range
- Accuracy class: active power 0.5S, reactive power 2S
- 5ppm accuracy RTC over full temp range(-40~110°C)
- Hardware line frequency measurement
- Various low-power modes applicable for metering
- 8x32 segment LCD
- tamper meter cover monitoring with time stamp
- infrared hardware interface & 2 Isolated RS485 port
- LED pulse outputs (KWH, KVAH, MFUNC)
- Isolated electrical pulse outputs (KWH, KVAH, MFUNC)
- Xtrinsic 3-axis low power tilt sensor for electronics tamper detection (optional)
- Various external memory interface(EEPROM,Flash)
- Cost effective two layer PCB board & BOM
- EMC proven design (ESD $\pm 15kV$, EFT $\pm 6KV$)

Software provided

- Application framework, Filter-based metering algorithms, FFT metering algorithms (optional)



44 LGA
5 x 5 mm²



3-Phase Power Meter RD – Performance

Accuracy

Type:X-3PH-KM14Z64 Current : 5(60)A Class : 0.5 Constant : 400imp/kWh Temp : 25°C																					
Number	Asset	Error%																			
		1.0				0.8L				0.5L				0.8C				0.5C			
		I _{max}	I _b	0.1I _b	0.01I _b	I _{max}	I _b	0.1I _b	0.01I _b	I _{max}	I _b	0.1I _b	0.01I _b	I _{max}	I _b	0.1I _b	0.01I _b	I _{max}	I _b	0.1I _b	0.01I _b
1	Test001	0.000	0.064	0.038	0.025	0.050	0.033	0.040	0.000	-0.100	0.007	0.026	-0.021	0.025	0.060	0.055	0.015	0.138	0.085	0.064	0.009
2	Test002	-0.019	0.033	0.044	0.083	0.088	0.043	0.049	0.097	-0.075	0.030	0.050	0.130	-0.025	0.040	0.046	0.090	0.125	0.050	0.045	0.106
3	Test003	-0.044	-0.004	0.013	-0.001	0.000	0.034	0.025	0.012	-0.050	0.005	0.050	0.021	0.013	0.000	0.009	-0.024	0.013	0.010	-0.028	-0.065

EMC

Freescale internal and 3 party test result:

- Passed over ± 6 kv level EFT
- Passed over ± 15 KV Contact ESD

3-Phase Power Meter Solution

Features

- 5 to 60A current range ($I_b = 5A$, $I_{max} = 60A$)
- 90 to 288V, 50/60 Hz voltage range
- Accuracy class: active power 0.5S, reactive power 1S
- Full four-quadrant import-export metering
- Hardware line frequency measurement – on any available phase
- Various low-power modes applicable for metering
- 4x24 segment LCD
- Various tampers supported with time stamp and electrical conditions
- Optically isolated hardware interface for communication
- LED pulse outputs (kWh, kVAh/kVAh)
- External memory interface(EEPROM)
- Cost effective two layer PCB board & BOM
- Capacitive power supply
- EMC proven design (ESD $\pm 35kV$)

Software provided

- Application framework, DFT metering algorithms for fundamental computation



100 LQFP
14 x 14 mm²



3-Phase Power Meter RD – Performance

- Complies with IS 13779: Class 1

Accuracy

Type:X-3PH-MKM34Z128CLL5 Current : 5(60)A Class : 0.5 Constant : 800imp/kWh Temp : 25°C												
Load	Error%											
	1.0				0.5L				0.5C			
	I _{max}	4lb	1lb	0.05lb	I _{max}	4lb	1lb	0.05lb	I _{max}	4lb	1lb	0.05lb
Error	-0.134	-0.029	-0.014	-0.004	-0.465	-0.408	0.064	0.221	0.200	0.311	0.021	-0.169

- MCU clocked by 12.288MHz

EMC

Freescale internal and 3 party test result:

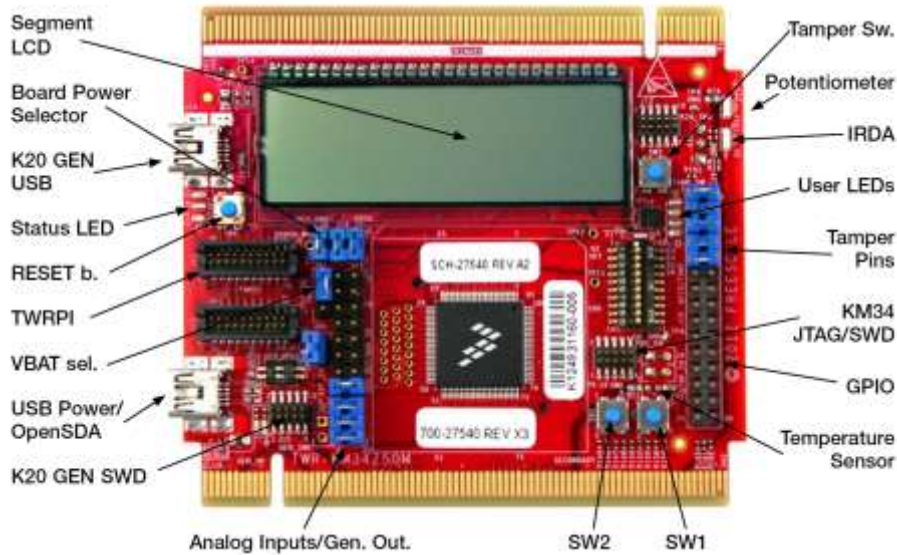
- Passed over ± 35 kV level PESD

SD Modulator Mode/Clock Rate	OSR	Measurement Bandwidth (kHz)	MCU Power Consumption (mA)	Performance (PF=1)	Performance (All PF)
Normal / 6.144 MHz	1024	3.0	8.4	+/-0.2% @ 0.100→90A (900:1)	+/-0.4% @ 0.100→90A (900:1)

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TWR-KM34Z50M Board



- 3.3V operation from USB
- Large 160-segment glass LCD
- **Onboard OpenSDA debugger**
- Headers for direct GPIO and ADC access
- Anti tamper tilt (3-axis acc.) sensor MMA8491Q
- External Tamper pins
- PB switches and LEDs
- RTC Battery
- **Onboard 6-channel waveform generator for emulation AC waveforms.**
- IRDA support
- NTC temperature sensor
- Tower system compatible
- TWRPI sensor interface

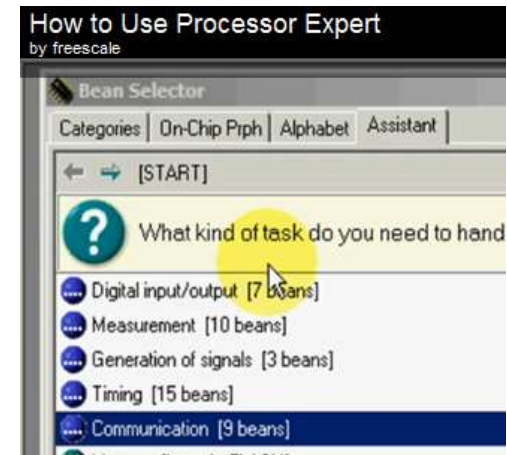
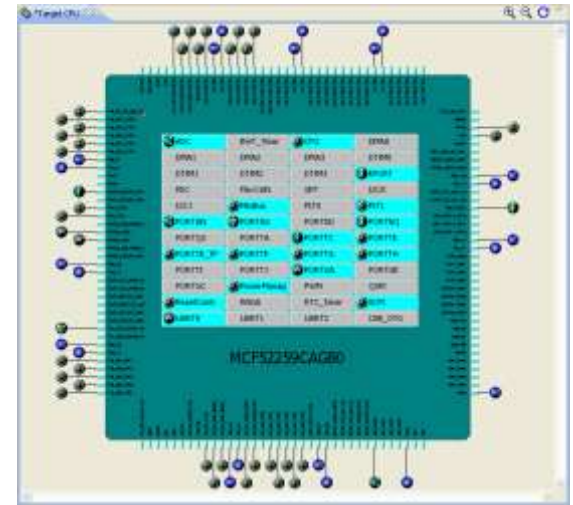
Kinetis MCUs: Broad Software Support

	Freescale CodeWarrior 	Keil (MDK) 	IAR (EWARM) 	Atollic (TrueSTUDIO) 	CrossWorks for ARM 
Kinetis Basic Device Support	Yes CW10.5	Yes v5.1	Yes V7.10	Yes V3.3	Yes V3.0.1
Processor Expert Support	Fully Integrated	Stand-alone Driver Suite (Eclipse) w/ MDK Eclipse Plug-in	Stand-alone Driver Suite / supported integration	Not available in current products	Not available in current products
Kinetis M Bare-metal Support	Yes	Yes	Yes	No	Yes
MQX Task Awareness	Yes (Professional Edition)	Yes	Yes	No	No
MTB Trace	Yes (Production Release)	Yes – with CMSIS-DAP and ULINK2	Yes – with J-jet and CMSIS-DAP	Yes	Yes
Free Version Limitations	Special Edition 64KB Debug	Lite 32KB	KickStart 16KB	Lite 8KB	No
Download Size	~1320MB	~278MB	~689MB	~500MB	~143MB

Processor Expert: Overview

- Easy-to-use GUI based tool to create a set of device drivers for your application very quickly and efficiently
- Driver code created exactly as you configure it. Not a “lowest common denominator” generic driver. You can take advantage of the precise features you want
- Header and source files created automatically. Prevents errors and conflicts between the drivers and the h/w
- Generated code tailored on configuration choices. Only functions you enable are implemented in code (size optimized)
- Processor Expert now available with support for IAR, Keil and GCC tool chains
- Training on www.freescale.com and www.youtube.com
- www.processorexpert.com

“You don’t have to sit down with over 1000-page data sheet and figure out where all the registers are and how to set everything up.”



FreeMASTER Run-Time Debugging Tool

Application control and monitor

Live graphs, variable watches, and graphical control page

Interfaces with Excel and Matlab

Supports:

- HCS08, HC12, HCS12 and HCS12X BDM
- 56F8000, 56F8100 and 56F8300 JTAG
- SCI driver (FMASTERSCIDRV) for all platforms

The screenshot displays the FreeMASTER interface for a DC Motor with Hall Sensors. The main window shows a speed gauge with a needle pointing to 815 rpm. To the right of the gauge are control buttons for Power (green circle), Fault (black circle), and Demo (yellow square). Below the gauge is a table of system parameters.

Name	Value	Unit
Required Speed	815	rpm
Ramp Output Speed	814	rpm
Actual Speed	815	rpm
Required DC-Bus Current	515	mA
Actual DC-Bus Current	79	mA
Applied Voltage	3951	mV
Revolution Counter	4508	
Direction	Incremental	ENUM
SC Saturation Flag	No Saturation	ENUM

At the bottom right of the interface, the text "RS232;COM1;speed=19200" is visible.



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 References

References

- Kinetis M Series MCUs, available on [freescale.com](https://www.freescale.com)
- Kinetis M Support for Distinct Separation of Legally Relevant Software (document [KINETISMWP](#))
- Filter-Based Algorithm for Metering Applications (document [AN4265](#))
- FFT-Based Algorithm for Metering Applications (document [AN4255](#))
- Using an FFT on the Sigma-Delta ADCs (document [AN4847](#))
- Kinetis-M One-Phase Power Meter Reference Design (document [DRM143](#))
- Kinetis M series MCUs One-Phase Power Meter Reference Design Introduction, available on [youtube.com](https://www.youtube.com).
- FreeMASTER Data Visualization and Calibration Software, available on [freescale.com](https://www.freescale.com).
- Kinetis M Bare-metal Software Drivers (document [KMSWDRVAPI](#))
- TWR-KM34Z50 Tower Module (document [TWRKM34Z50M](#))





www.Freescale.com