

Automotive MCU Advanced Driver Assistance Systems (**ADAS**) Product and Solution Update

APF-ACC-T1092

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Advanced Driver Assistance Systems



Autonomous
Self Driving
Cars

Automated
Predictive
Actuators

**Collision
Prediction**
Predictive and
Warning

**Collision
Avoidance**
Reactive
Systems

**Collision
Mitigation**
Passive
Systems



S32V/R – The Right Solution for Vision & Radar in ADAS



Robust

- Fully targeted at ISO26262
- Reliable, dependable automotive design and integration
- Embedded Security

Efficient

- Intelligent partitioning to optimize cost
- Dedicated Acceleration to improve performance
- Balanced Performance per Power

Flexible

- Simplify the experience!
 - Flexible, Open programming models
- Supported by off-the-shelf RTOS and tools
- Enabled by Industry leading EcoSystem

Freescale Future Ready: Robust, Efficient, Flexible solutions



MRD2001 77 GHz and MPC577xK

Industry's most comprehensive system-level solution for automotive radar systems

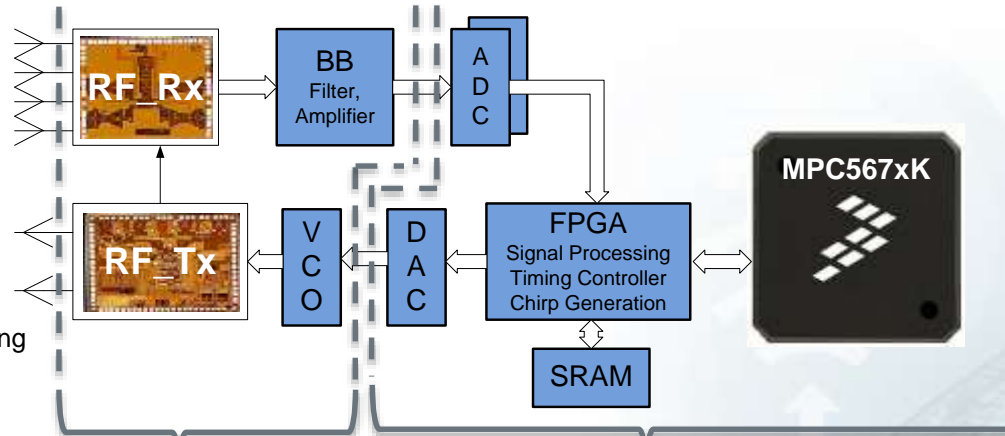
• Qorivva MPC577xK

- Replaces:

- 8 ADC
- 1 DAC
- 1 FPGA
- External SRAM
- General purpose MCU

- Enables:

- Significant PCB area saving
- Reduced assembly cost



Previous Generation

Next Generation

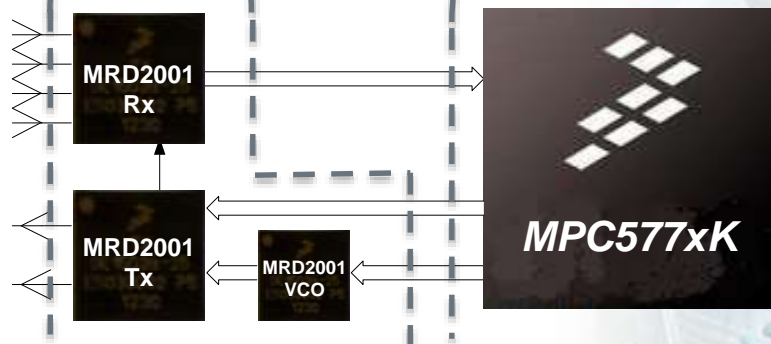
• MRD2001 77 GHz Chipset

- Replaces:

- Bare Die RF solutions with a RF Chipset based on RCP package technology
- Discrete Filter Components and Amplifiers

- Enables:

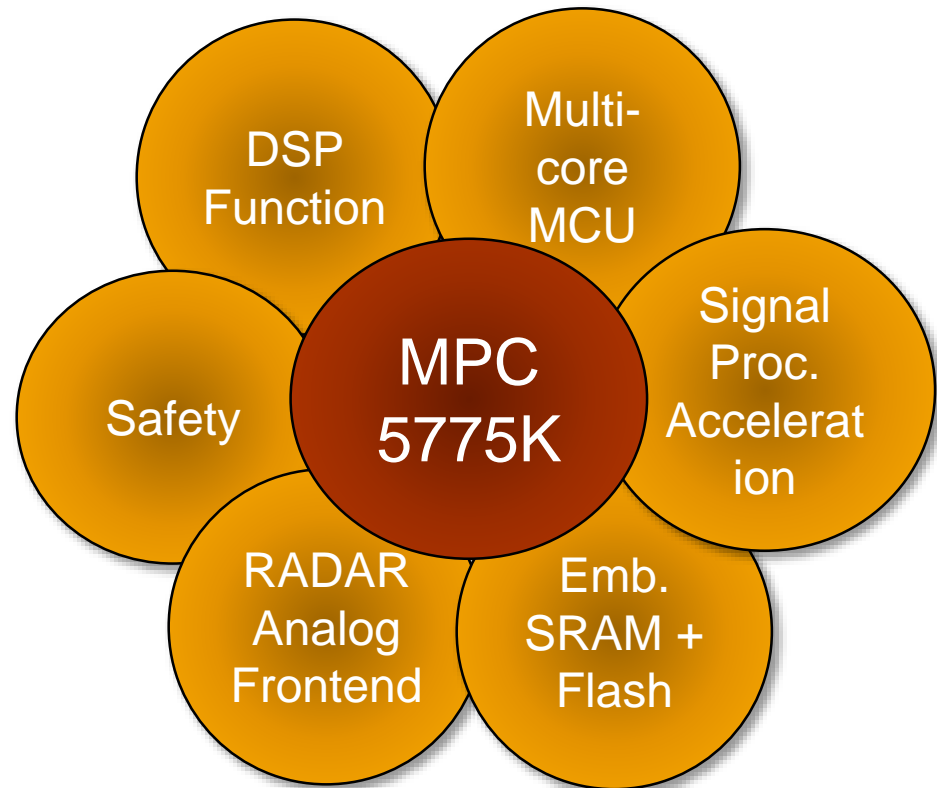
- Significantly lower assembly cost
- Lower PCB cost



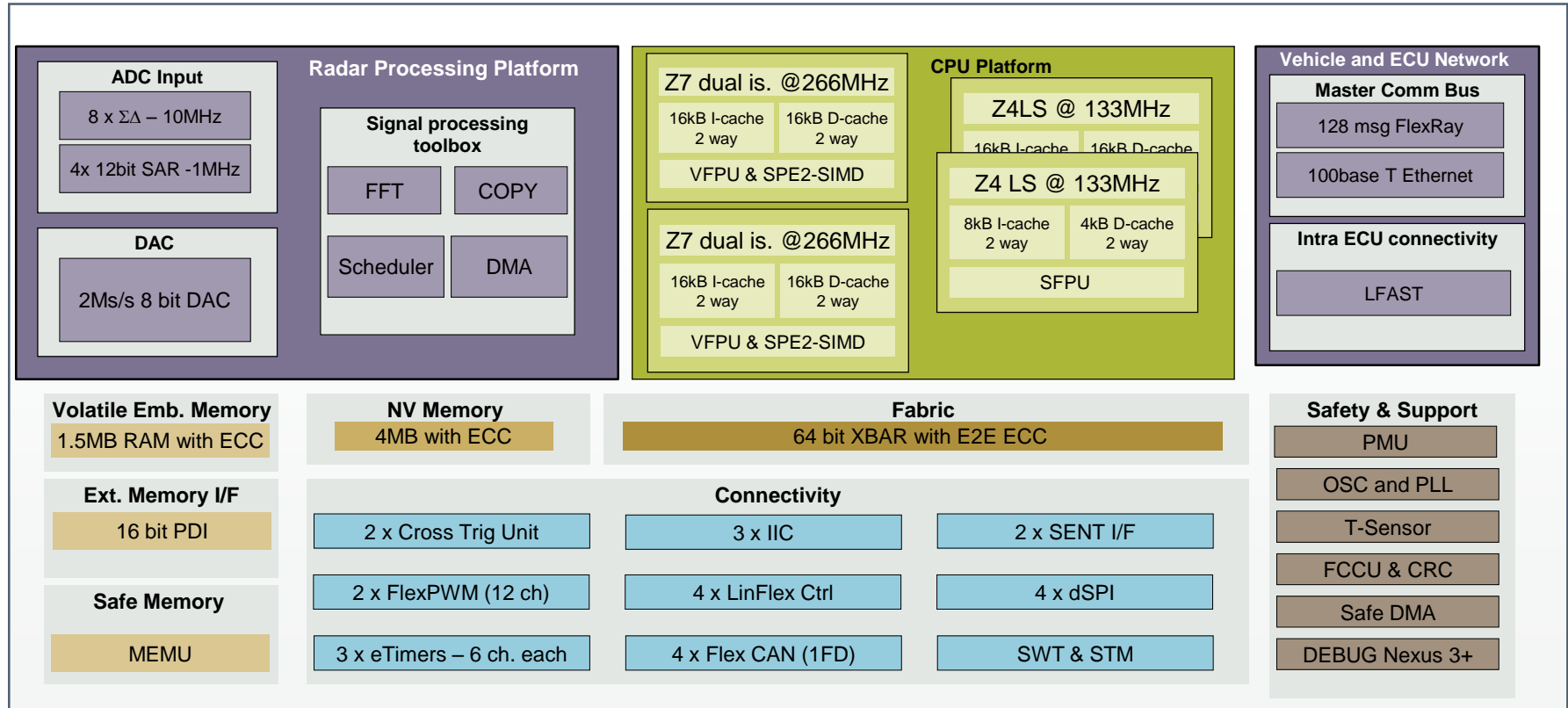


What MPC5775K Makes Unique

- Unique combination of DSP and MCU
- Acceleration for common signal processing tasks
- Multi-core architecture
 - 3 cores, 1 lock-stepped
- Embedded SRAM & Flash
- Automotive Interfaces
 - CAN/FR/ETHER
- Functional Safety up to ASIL-D
- Analog Frontend RADAR
 - ADCs, DAC, PLL



MPC5775K : 2x Z7 + 2x Z4LS – 4 MByte



Specifications:

- **CPU: 3x PPC: 2x Z7** 266 MHz Power dual issue with SPE2 and VFPU and Z4 133MHz in permanent lockstep
- **SPT:** FFT Accelerator, DMA
- **Analog:** Octal SD + 4 SAR, Ultra low jitter PLL, precision DAC
- **Package:** 356 PBGA – 0.8 mm pitch – 17 x 17 mm² body
- **Temp Range (Ta):** -40 to 125°C, 150 °C T_j, AEC-Q100 Grade 1
- **Main Supply:** 3.3V IO (5V SAR) and 1.2V Core (ext or PMU)

Key Features:

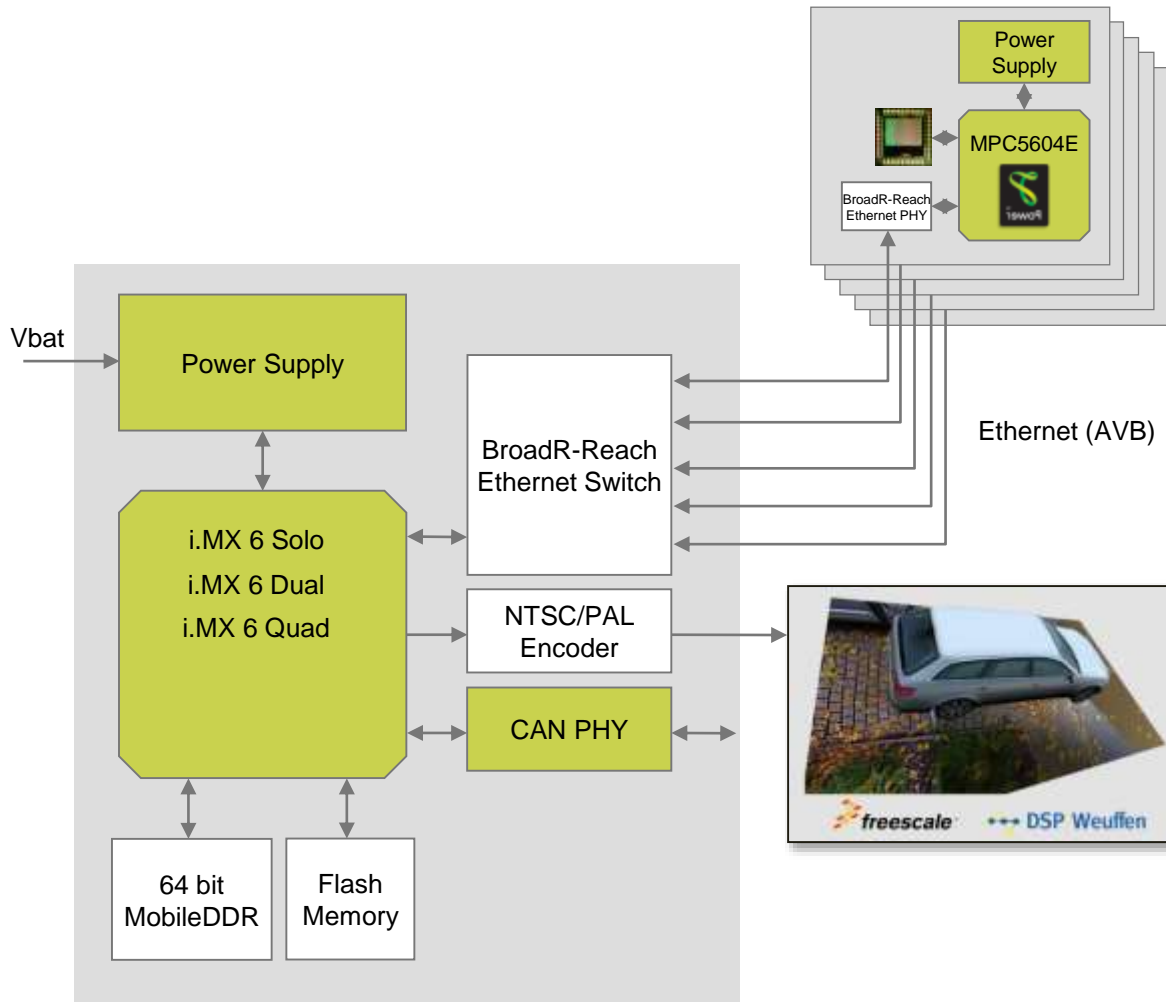
- **F. Safety:** developed as per ISO26262 with target ASIL-D
- **Safety Enablement:** Safety Manual and FMEDA
- **SPT:** Radix4/2, r2c, c2c, 50 MHz 16 bit twiddle, 24 bit results, Copy, Transpose
- **SRAM:** Multi ported SRAM Ctrl and 1.5MB SRAM with ECC
- **Top of Class Analogue IP:** PLL, DAC, OSC and SD ADC
- **SW Enablement:** QMS MCAL and/or Safe Mcal Asil B (D)

ADAS Communication Links

Analog (PAL / NTSC)	LVDS	Ethernet (AVB)
<ul style="list-style-type: none">✓ Low cost components, widely available✗ Shielded co-axial cabling required✗ Low resolution and color deviations✗ Accepted only for low-end rear view camera	<ul style="list-style-type: none">✓ Very high bandwidth (up to 1 Gbps)✗ Expensive shielding required✗ Costly manufacture of cable harness✗ EMC and quality issues	<ul style="list-style-type: none">✓ Low cost unshielded twisted pair cable✓ High bandwidth up to 250 Mbps full duplex✓ Widely adopted, ease of use

Ethernet is proven alternative to conventional video communication

Multi-Camera Panorama View Park Assist



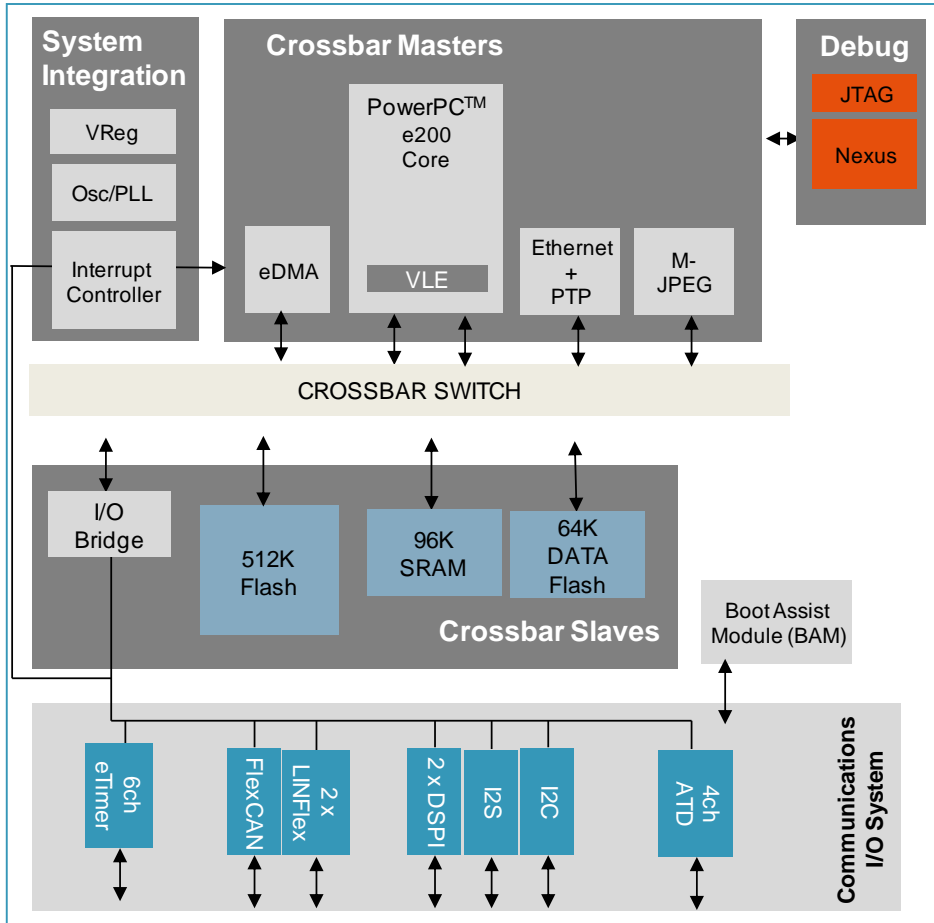
- **Challenge**

- LVDS based solution requires FPGA for multiplexing
- Separate DSP leads to high BOM cost

- **Solution**

- GPU efficiently does video stitching and rendering
- Fully integrated i.MX6 single to quad-core MPU with powerful GPU offers low BOM cost

Salsa 512K – MPC5604E



Core

- up to 64 MHz PowerPC ISA e200 zen0h core

Memory

- 512k byte Program Flash with ECC
- 4x16k byte Data Flash with ECC
- 96k byte SRAM with ECC

I/O

- 1 x MJPEG video encoder with image sensor interface supporting up to 1.2MPixel
- 1 x 10/100 Ethernet MAC incl. IEEE 1588 PTP support
- 1 x FlexCAN
- 2 x LinFlex
- 1 x I2C interface
- 1x I2S/I8S/TDM audio interface
- 2 x DSPI (4 independent chip selects each)
- 1 x eTimer (6 channels for general purpose)
- 1 x ADC (5V capable)
 - TBD Ch, 10bit, conversion time <1µsec

System

- PLL
- 16Ch eDMA
- 16MHz internal RC OSC
- 2 or 5 pin JTAG / Nexus Class 1
- 3.3V single supply
- 64 pin LQFP package

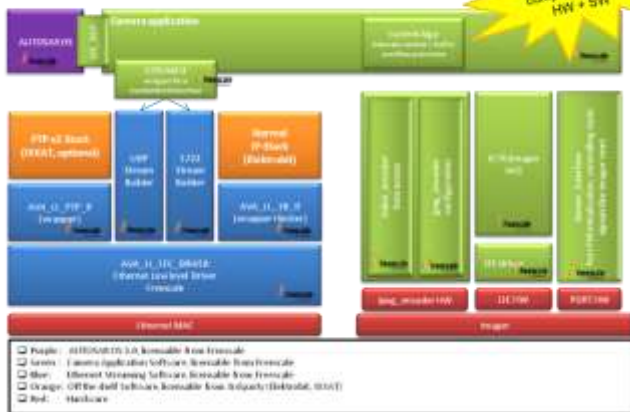
http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=MPC5604E&nodeId=01624606C1427E

First Production Ethernet Surround Camera System – SOP 2013 (Freescale MPC5604E + Ethernet Camera SW application)

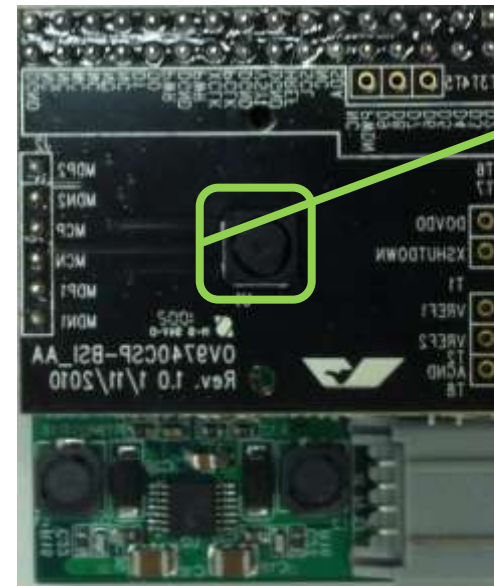
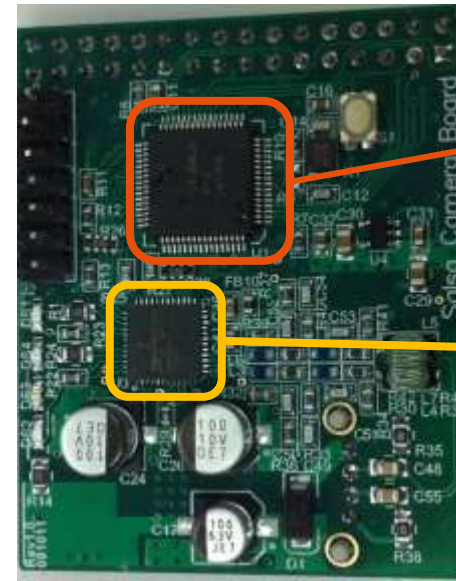
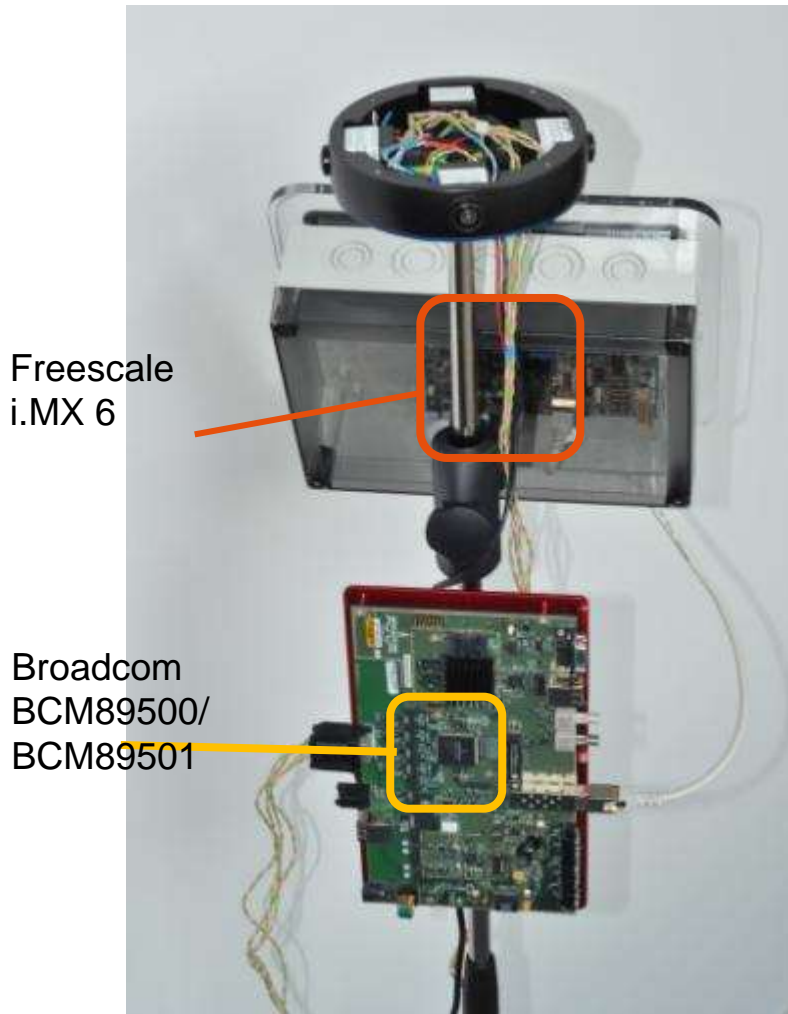


Freescale Software for Surround Camera Systems using MPC5604E

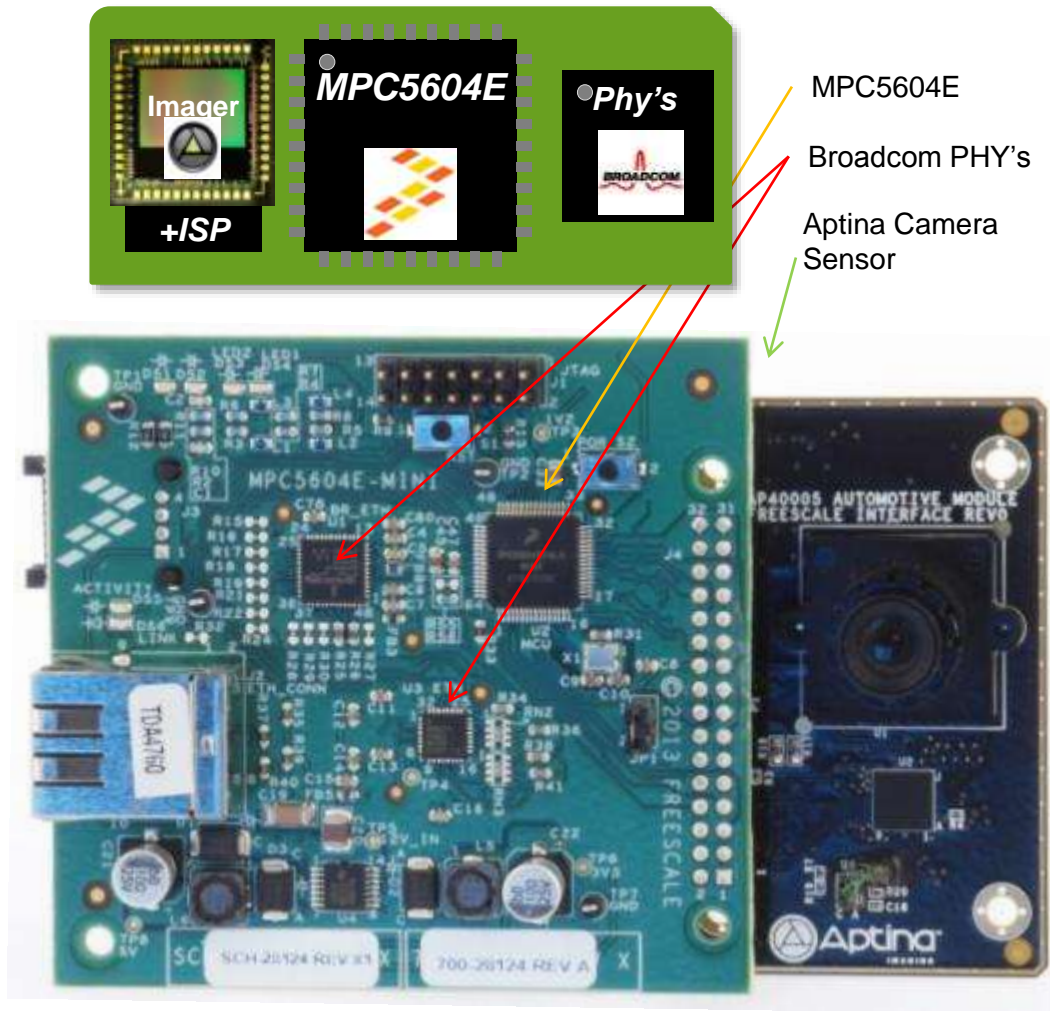
Freescale offers a complete Solution HW + SW



Surround View Demo



MPC5604EKIT



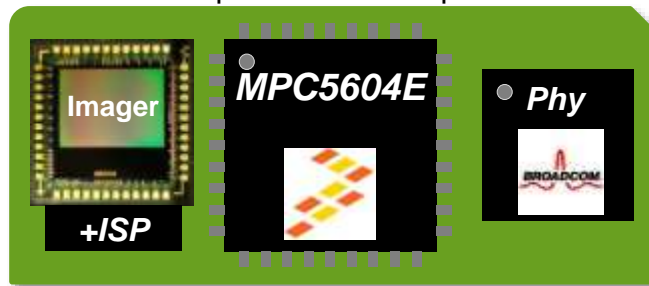
- **Complete Camera Dev Platform**
 - Freescale MPC5604E mini daughter card for video compression and transmission over Ethernet
 - Freescale Ethernet camera streaming software (for development purposes only)
 - Aptina Image Sensor and ISP daughter card (AP0132+AP0101)
 - Broadcom Ethernet PHYs supporting Broadreach and standard 100Mbps (BCM99810 and BCM5241)
- **MPC5604EKIT simplifies development**
 - Simplifies sourcing (purchase Kit from one vendor – Freescale)

MPC5606E – Automotive Ethernet Camera

Solution Today

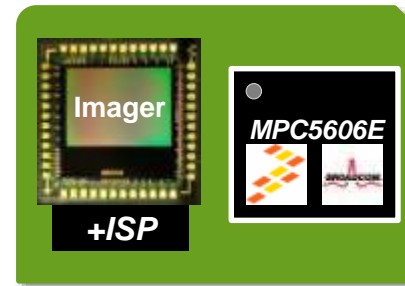
Salsa + BroadR-Reach PHY

- ✓LVDS Elimination
- ✓Ethernet proven in mass production



Integration:

Reduced PCB FootPrint



- ✓BroadRreach phy integrated through SiP (stacked die wire bond)
- ✓Small low cost package (8x8mm)
- ✓Cost, size, complexity reduction

- MPC5606E integrates the MPC5604E (from Freescale) and the BCM89810 (from Broadcom) dies into a single package
- MPC5606E performance and functionality is equivalent to the dual-chip solution
- Software from dual-chip solution reusable for MPC5606E
- MPC5606E significantly reduces PCB space
 - **Ideal for applications (i.e. camera module) that have tight space constraints**
 - **Package: 8mm x 8mm 121-pin BGA**
- Product Availability (from Freescale)
 - **Samples: Today**

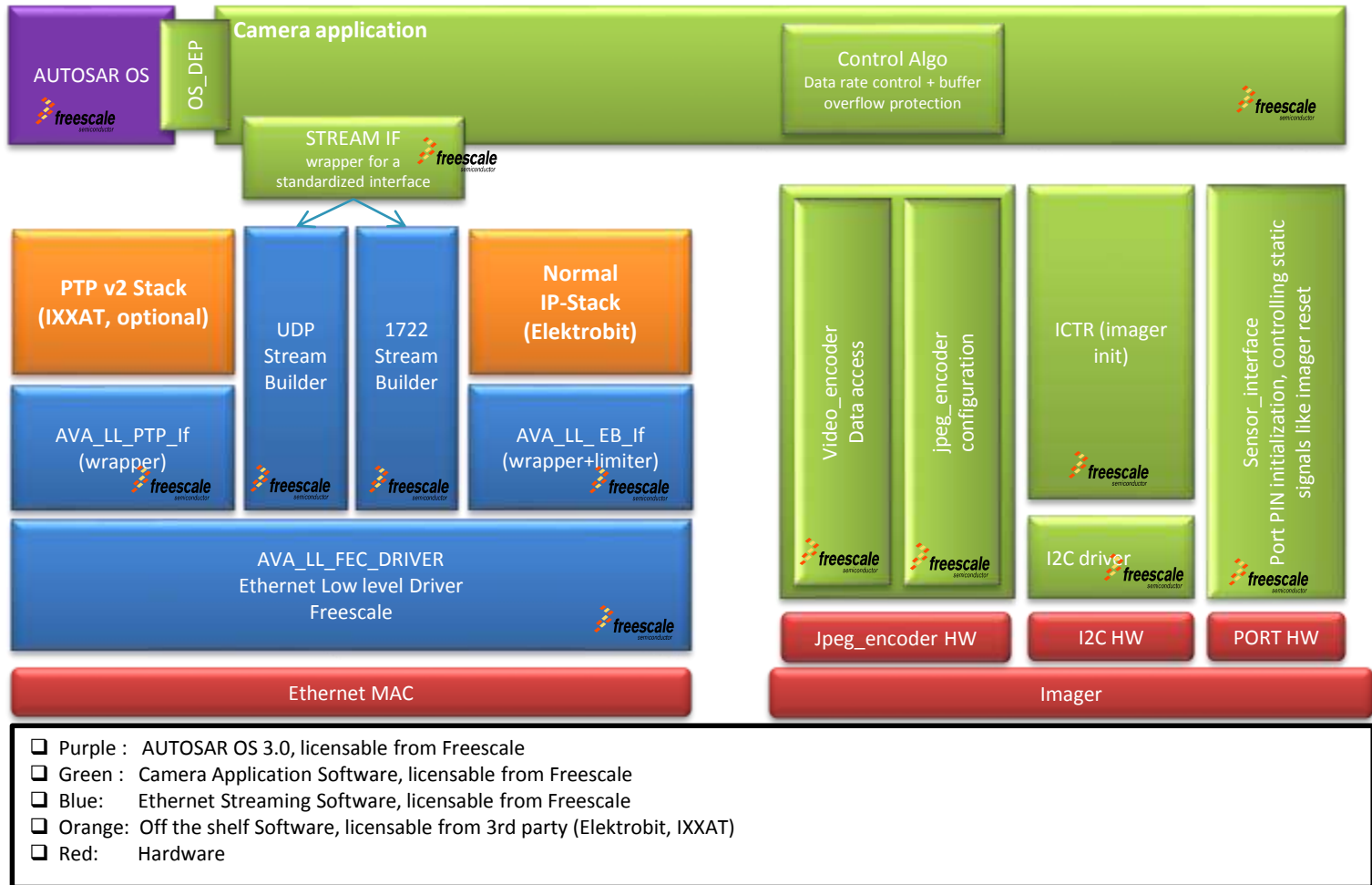
MPC5606EEVB



MPC5606EEVB is available now !



FreescalE Ethernet Camera Software



i.MX 6 Family



i.MX 6Solo

- Single ARM Cortex A9 at up to 800MHz auto / 1.0GHz consumer
- 256KB L2 cache, Neon, VFPv16, TrustZone
- 3D graphics with 1 shader up to 27MT/s, plus hardware X-acceleration engine
- External memory support up to 32bit DDR3 and LPDDR2



i.MX 6Dual

- Dual ARM Cortex A9 at 850MHz and 1GHz auto / 1.2GHz consumer
- 1 MB L2 cache, Neon, TrustZone
- 3D graphics with 4 shaders up to 176MT/s and OpenCL Embedded Profile support, plus hardware OpenVG and X-acceleration
- External memory support up to 64-bit DDR3 and 2-channel 32-bit LPDDR2
- Integrated SATA-II



i.MX 6Quad

- **Quad ARM Cortex A9 up to 1GHz**
- 1 MB L2 cache, Neon, TrustZone
- **3D graphics with 4 shaders up to 176MT/s and OpenCL Embedded Profile support**
- **OpenVG** accelerator for **overlays**
- External memory support up to **64-bit DDR3** and **2-channel 32-bit LPDDR2**
- **≥ 64 bit bus architecture**
- Integrated SATA-II



Common Features of the i.MX 6 Series Platform

- Pin compatible ARM Cortex A9 based solutions up to 1GHz per core for automotive and 1.2GHz per core for consumer
- HD 1080p encode and decode
- 3D video playback in high definition
- Integrated IO's that include HDMI v1.4, MIPI and LVDS display ports, MIPI camera, Gigabit Ethernet, multiple USB 2.0, PCI-Express, dual CAN controllers, MLB150/50/25 support
- Consumer, Industrial and Automotive temperature range qualifications
- SW support: Google Android™, Microsoft Windows® Embedded CE, Linux®,/Linaro™, QNX®, GENIVI™





SCP22xx Image Cognition Processors

Smart Camera Technology

Balances Performance and Power – APEX™ IP offers industry-leading performance per mwatt and delivers an ideal solution for image cognition processing

Mainstream Cost-effective Solution – Cost, power and size advantages enables smart camera technology into mainstream vehicles, improving auto safety features

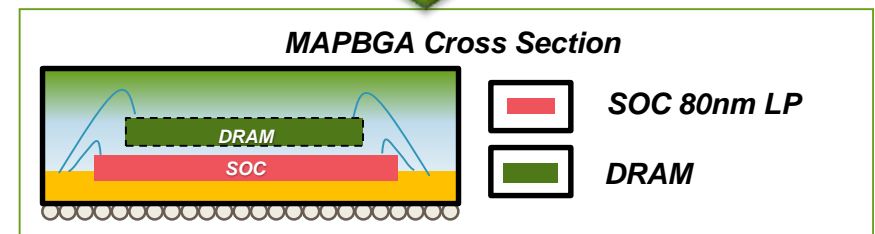
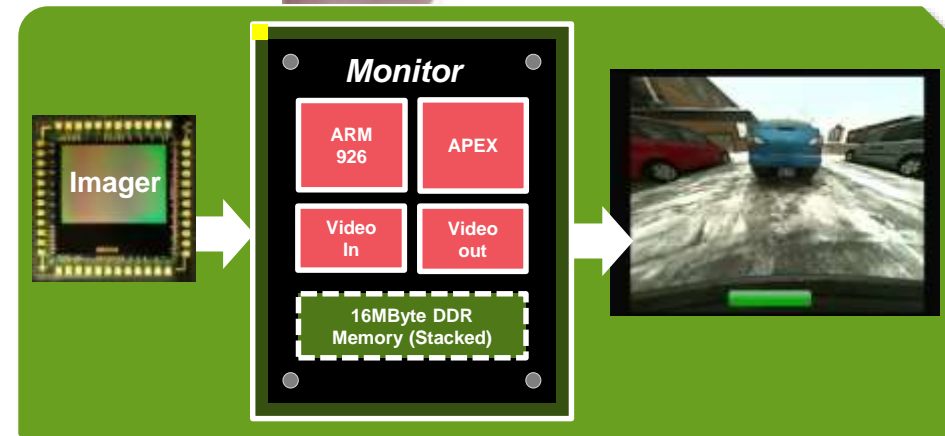
Delivers the Right Integration – Image cognition processor delivers the innovative technology required for smart automotive camera applications

Speeds Time to Market – Comprehensive solution including libraries, hardware and software development kits speeds time to market.

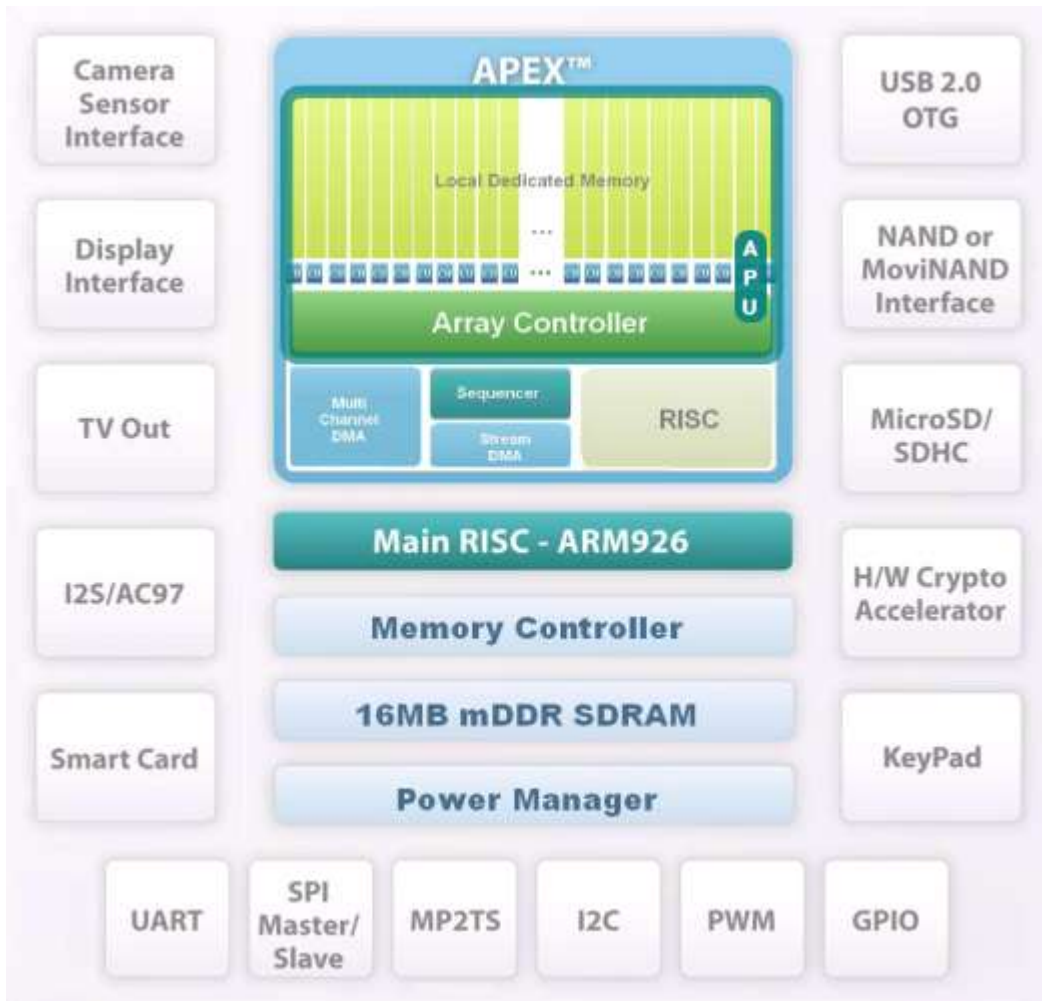


SCP2201/07 : “Value Add” for Smart Rear Camera

- Dedicated image processor for **Distance Measurement** and **Object detection**
- **1st generation array controller (Image Cognition Functionality)**
 - Massive Parallelism
 - Revolutionary data movement architecture
- Extra **high density** Memory (to 64MB)
- **Very low-power** (<300mW typ use case)
- SW enablement to provide:
 - Object Detection
 - Distance Estimation
 - Dynamic Overlay
 - Perspective and Lens Distortion Correction



Monitor (SCP220x) Image Cognition Processors

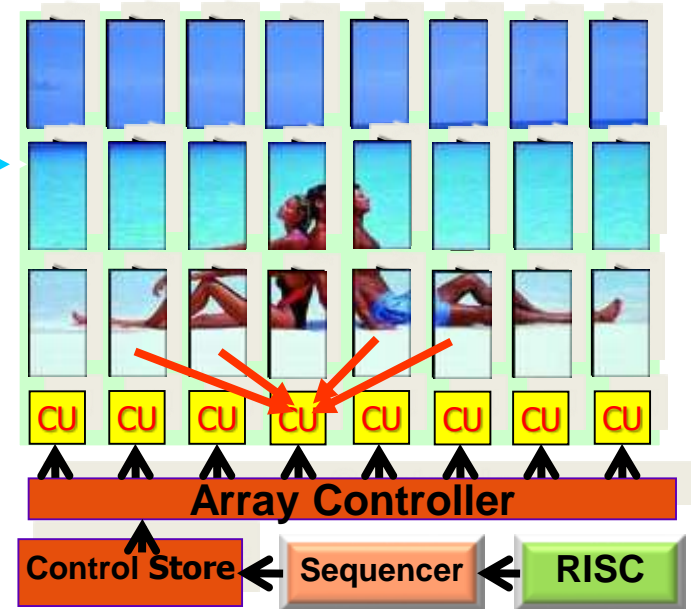
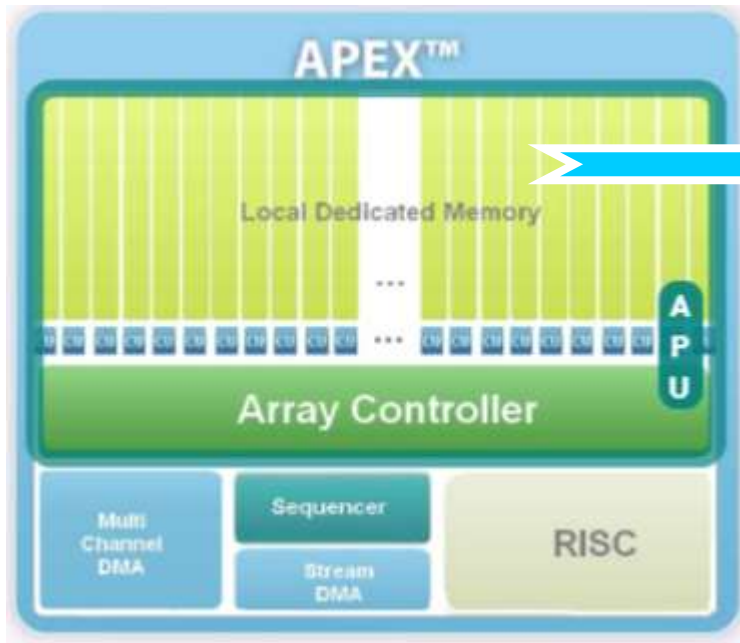


Key Features:

- Main RISC CPU :
ARM926EJ @350 MHz
- 1V Core, 1.8~3.3V IO
- APEX supports 34 billion operations per second (BOPs), or 2 billion MACs per second plus a 2nd slave scalar RISC (350MHz)
- Built-in dedicated overlay engine, rotation, supports alpha-blending and overlay
- Drives TFT LCDs directly
- BT656 sensor interface (YUV, 8/10 bit with separate H/VSync)
- Built in TV encoder/Video DAC (NTSC/PAL)
- Many peripherals integrated
- Multiple package options

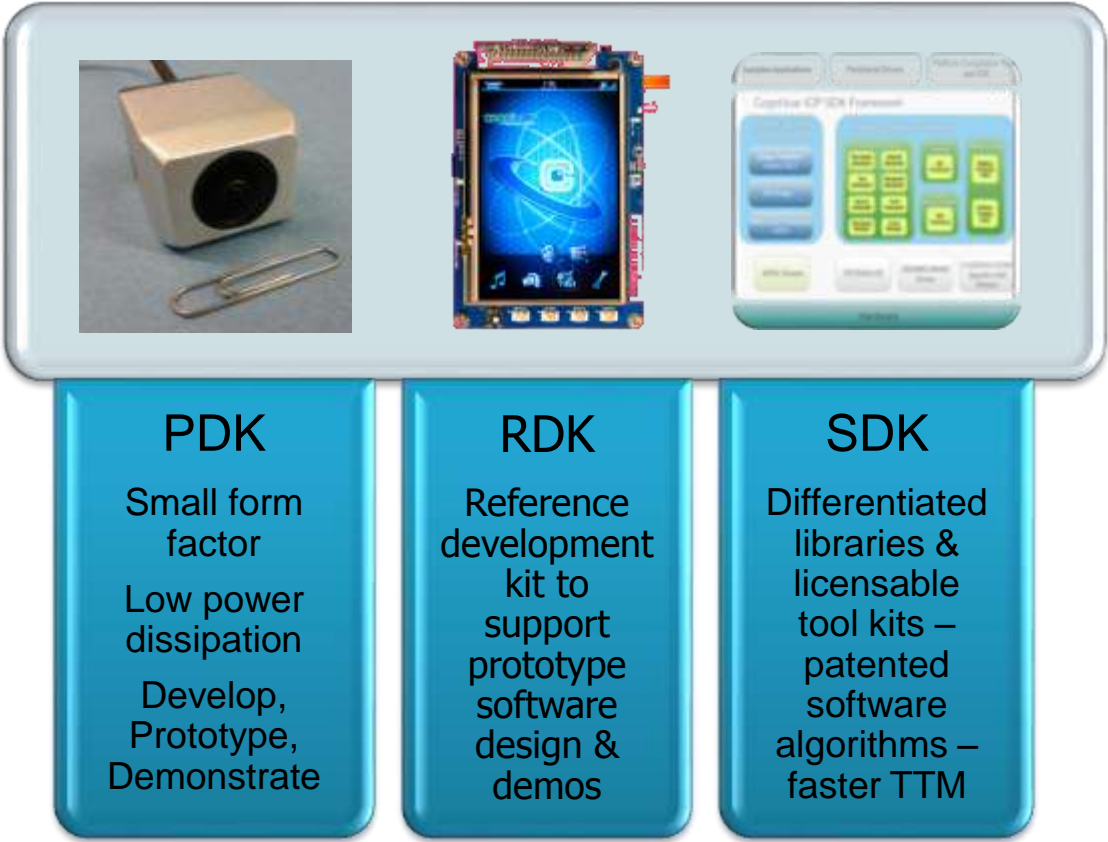
http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=SCP2200

APEX Technology – Massively Parallel



<i>Features</i>	<i>Benefits</i>
Array Processor Unit (APU)	Scalable and fully-programmable massively parallel SIMD processing core 96 16-bit processors in APEX-1 (up to 34Billion Ops/sec)
Data memory co-located within APUs	Minimizes access to off-chip memory to maximize performance efficiency and reduce power
Multi-channel, Stream-In, and Stream-Out DMAs	Data transfer operations are automatically sequenced to move data in and out of APEX efficiently – keeps APU fed
Multi-core	Various hardware blocks run in parallel with APU. Bit processing acceleration blocks (not shown) and RISC CPU are used for operations that map best to serial processing.

Vertical Platform Solution



Software development is a critical cost and factor in time to market

RearVue Application



Brand Name – S32 Simplified Automotive Naming

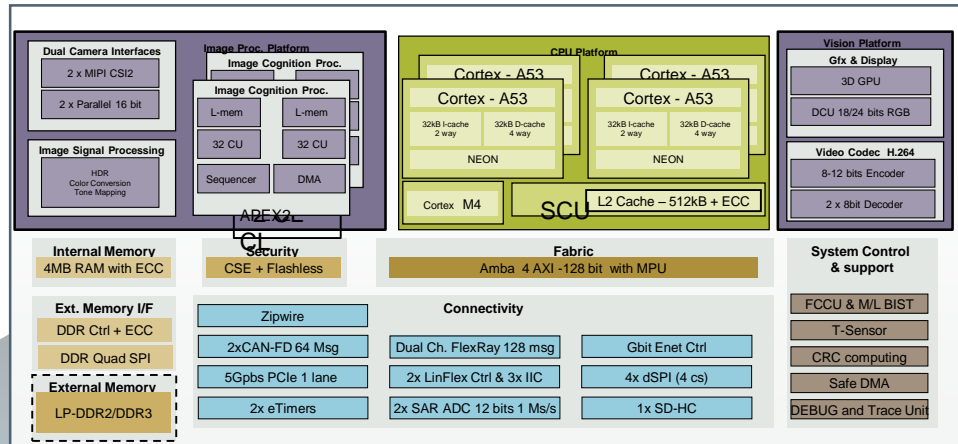
Existing Products

- ARM®-based processors
- Qorivva MCUs
- Power Architecture-based processors
- S12(X) MCUs
- S12 MagniV mixed-signal MCUs
- Image Cognition Processors
- Kinetis auto MCUs
- S08 MCUs
- ARM® Cortex-based MCUs
- MAC57Dxx MCUs
- Others ...

New Products

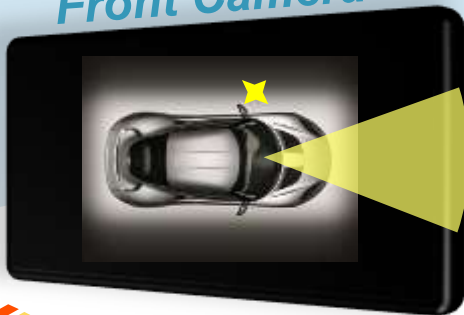


S32V200



S32V200 takes advantage of best in class image processing performance while satisfying the demand for ISO26262 functional safety. Enabled by an OPEN-CL program interface and supported by an broad software and tools ecosystem, the S32V200 achieves all this while keeping power and system cost at a minimum

Front Camera



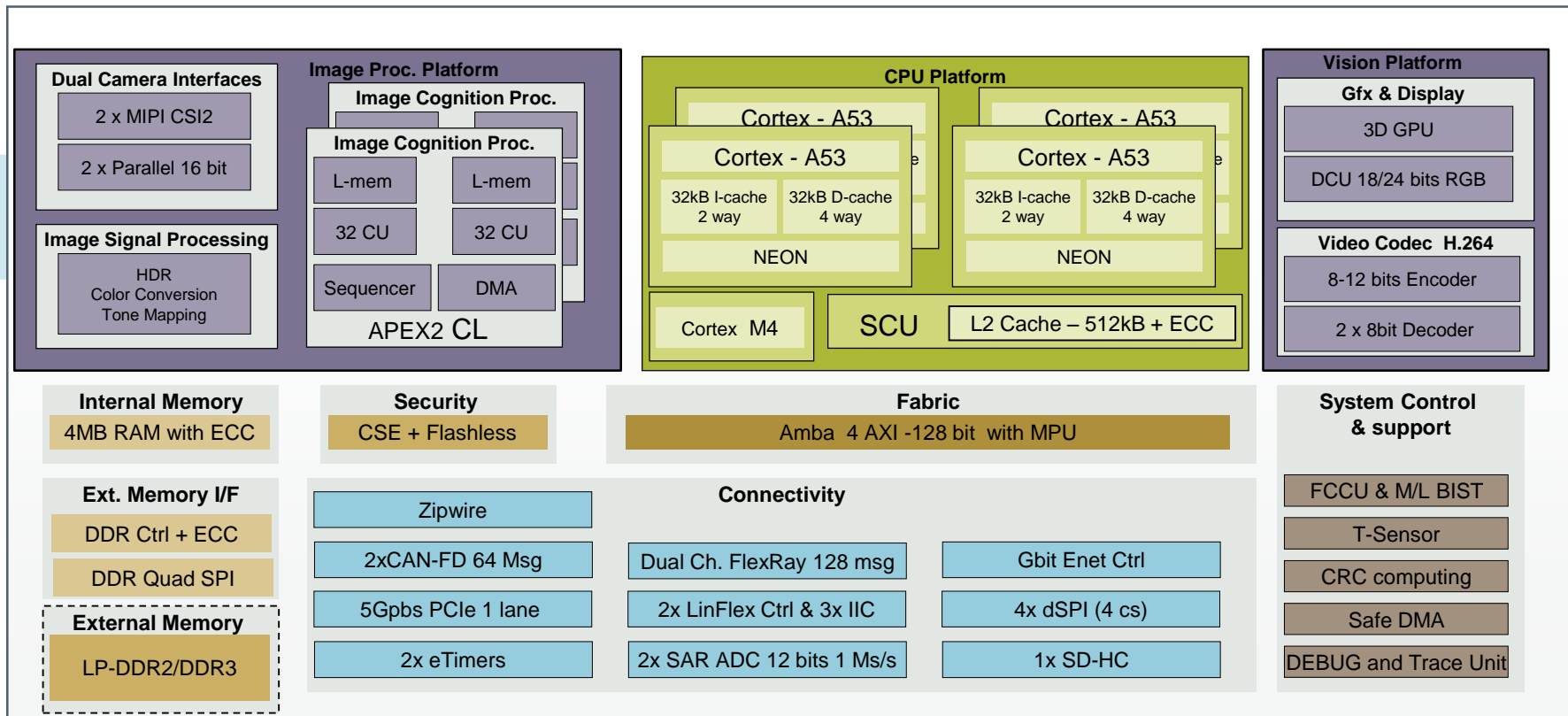
Surround View



Data Fusion



S32V234



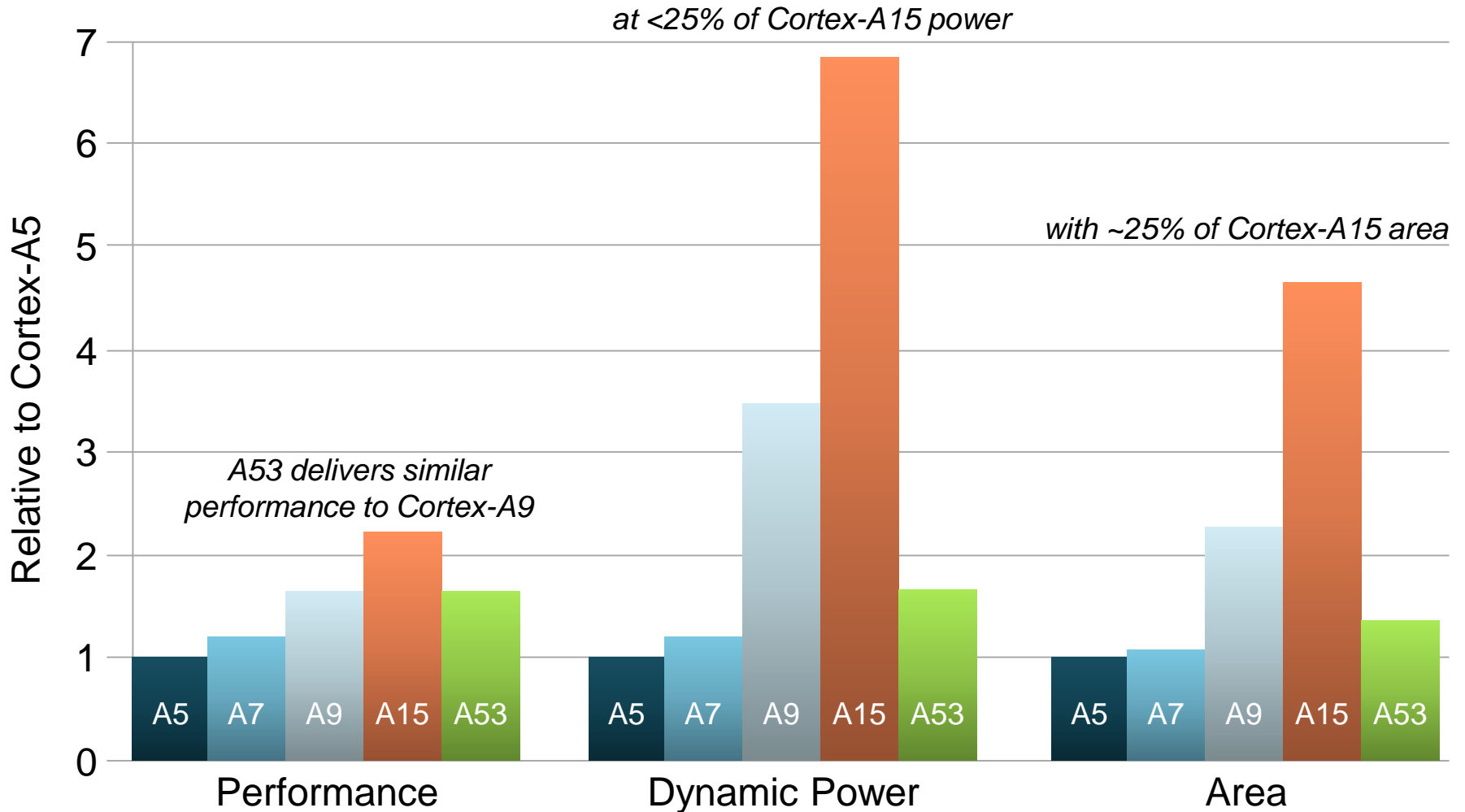
Specifications:

- **CPU1-4:** ARM Cortex-A53 @800MHz, L1/L2 cache with ECC & Neon
- **CPU5:** Cortex -M4 for IO control with I/D Cache and ECC
- **ICP:** 2 x APEX2 CL (MIMD APU-64 CU each) at 400MHz
- **GPU:** GC3000 from Vivante
- **Package:** 17x17FC-BGA
- **Temp Range (Ta):** -40 to 105°C, 125 °C Tj, AEC-Q100 Grade 2
- **Main Supply:** 3.3V IO and 0.94V Core - external PMU + DDR rails

Key Features:

- **F. Safety:** developed as per ISO26262 with target ASILB/C
- **SW Enablement:** OpenCL Tools for ICP, GPU, NEON.
- **Video Codec:** H.264 Encoder (8-12 bit) + Decoder (8 bit)
- **DRAM:** External LPDDR2 & DDR3 supported
- **Security:** SHE (almost) compliant Crypto Security Engine
- **Surround 3D:** 3D unified architecture. 19/38Gflops at 600MHz
- **Video dist. Network:** 2X Mipi CIS2 – 4 Virtual channels each
- **Connectivity:** Gbit Ethernet, PCIe, FD-Can & Flexray

Cortex-A53 Comparison



Performance is Specint2000 at synthesized frequency

Area is core with Neon + L1 cache, with L2 controller, MP1 configuration, no L2 RAM included

Power measured as Dhrystone at nominal voltage

Freescale S32V200 Processors: Building the Foundation

- Simplify The Experience

“It can take up to 50-man-years to move my ADAS vision application from one HW platform to another....”

Freescale customer



Key Freescale Eco-System Partnerships:

IP



- Announced in 2012
- Partnership to deliver image processing IP and software
- Enabled by OpenCL

RTOS Tools



- Announced May 2014
- Partnership to deliver RTOS & Toolchain
- Dependable, Reliable, Predictable

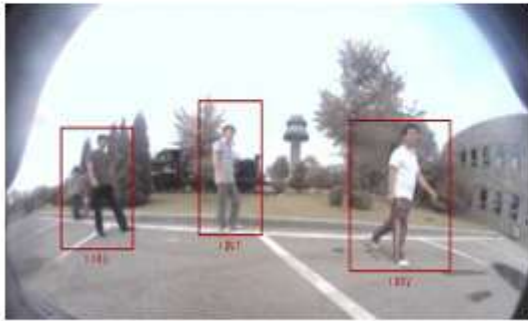
Software



- Announced May 2014
- Partnership to deliver algorithms, demo's and full vision applications



ADAS Demo Apps



Pedestrian
Detection



Traffic Sign
Detection

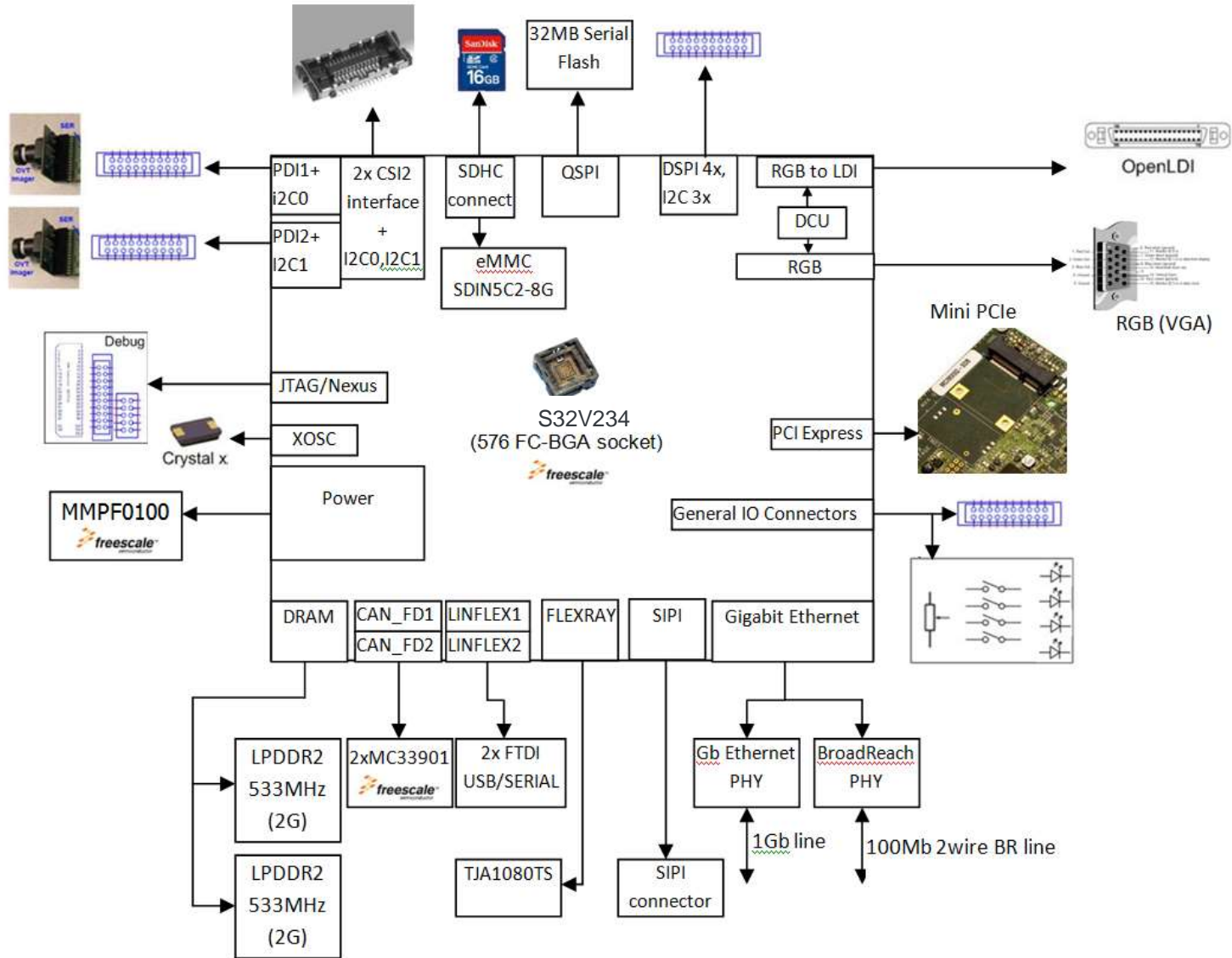


Lane
Detection

Demo App Selection:

- Popular ADAS Apps based on camera sensor
 - Important for traffic environment sensing.
 - Based on camera sensor, cheap and efficient
 - Challenges: robustness & real-time

S32V234 EVB – Available with first silicon





www.Freescale.com