Microcontroller Aware Hardware Design

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First, a story…

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At 259,000 Km

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What to do?

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HONDA

049
89.9.20

Throttle Position

→ Torque/ Speed

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ADC

PWM

Throttle Position

Torque/ Speed

With Great Power Comes Great Complexity

ADC

PWM

Throttle Position

ECU

Engine

Torque/ Speed

Exhaust Gas Oxygen

ADC

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With Great Power Comes Great Complexity

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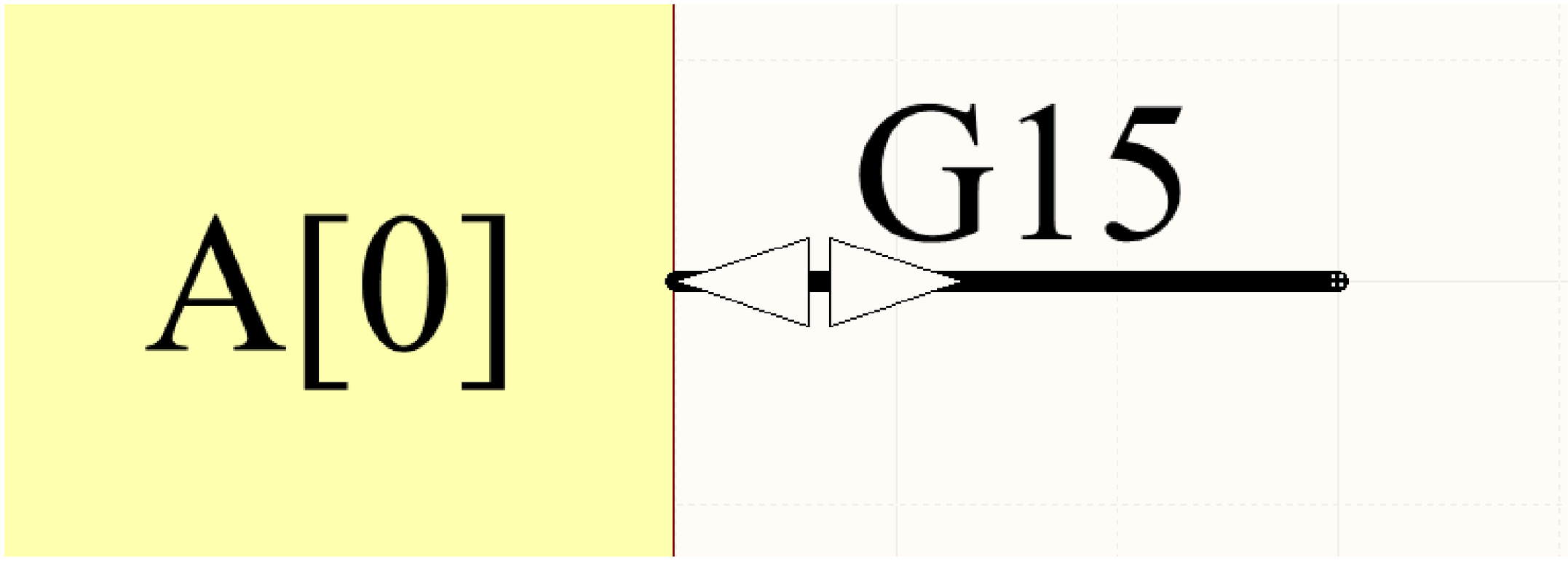
With Great Power Comes Great Complexity

Typical systems now consist of many inputs and control signals:

- Several ADC Channels for Throttle, MAP, Airflow, Oxygen, Temperature, Altitude Pressure, Pedal, Fuel Pressure, etc.
- Several Schmitt / Digital inputs for Speed, Gear, Vane-type Airflow, etc.
- Multiple PWM Channels and Timers for Injection control (esp. multi-point), Fuel Pump, Transmission and more…
- Inputs from other vehicle systems such as ABS, Gear Selector, Security, Air-Bag, Collision Detect/Avoidance.

Configurable Devices

The Humble Microcontroller and its GPIO pin…



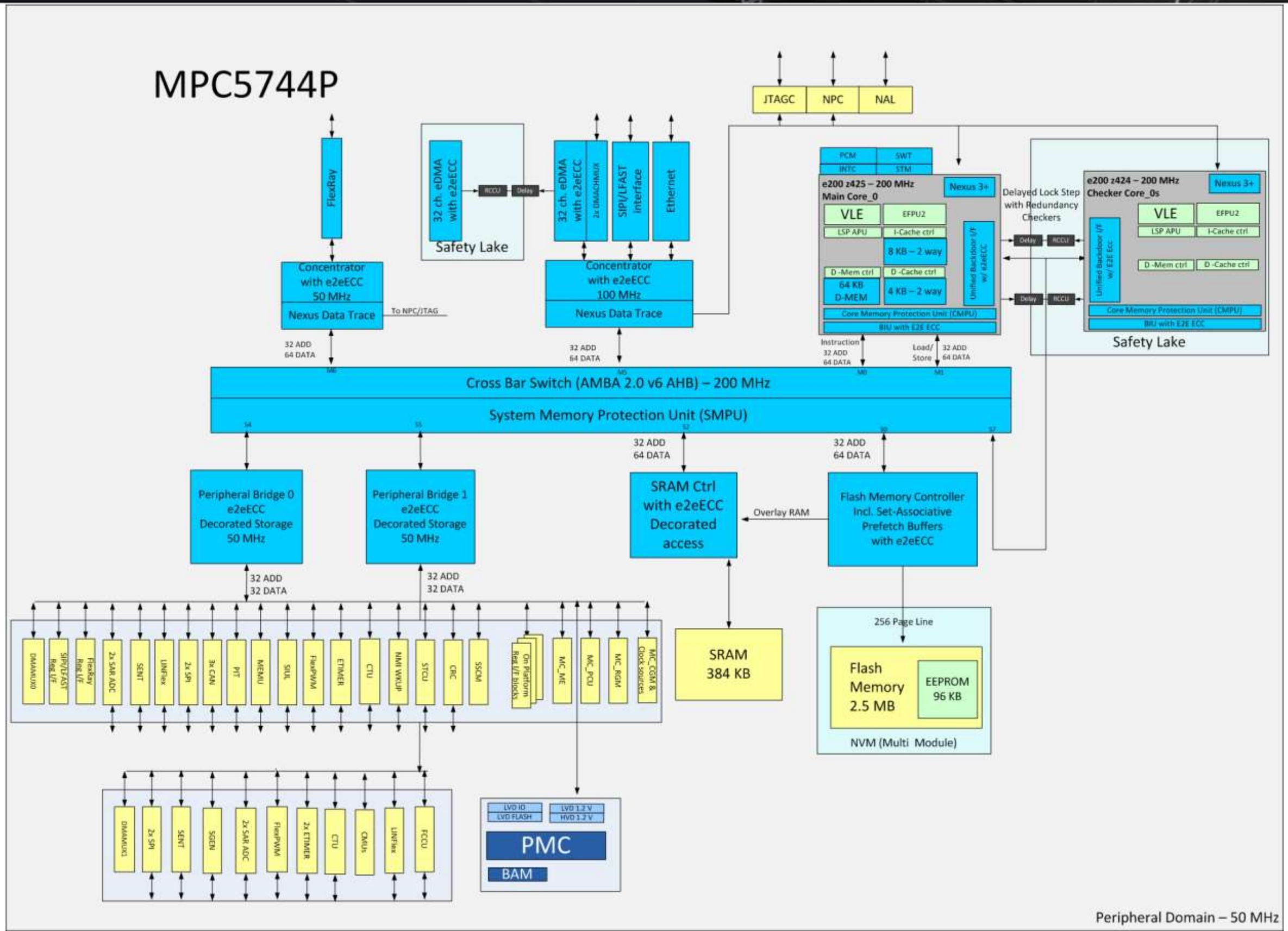
Configurable Devices

…is not so humble any more!

Table 8. Pin muxing (continued)

Port Pin	SIUL2 MSCR/ IMCR Number	MSCR/ IMCR SSS Value[1]	Signal	Module	Short Signal Description	Dir	LQFP144	BGA257
A[3]	MSCR[3]	0000 (Default)	GPIO[3]	SIUL2-GPIO[3]	General Purpose IO A[3]	I/O	92	G15
		0001	ETC3	eTimer_0	eTimer_0 Input/Output Data Channel 3	I/O		
		0010	CS0	DSPI2	DSPI 2 Peripheral Chip Select 0	I/O		
		0011	B3	FlexPWM_0	FlexPWM_0 Channel B Input/ Output 3	I/O		
		0100-1111	—	Reserved	—	—		
	IMCR[171]	0000 (Default)	ABS2	MC_RGM	RGM external boot mode 2	I		
	IMCR[62]	0010	ETC3	eTimer_0	eTimer_0 Input Data Channel 3	I/O		
	IMCR[49]	0001	CS0	DSPI2	DSPI 2 Peripheral Chip Select 0	I/O		
	IMCR[98]	0001	B3	FlexPWM_0	FlexPWM_0 Channel B Input/ Output 3	I/O		
	IMCR[176]	0001	REQ3	SIUL2	SIUL2 External Interrupt Source 3	I		

…With Great Power Comes Great Complexity



Configurable Devices

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	VSS_HV_IO	VSS_HV_IO	A[14]	A[9]	D[3]	JCOMP	H[12]	C[15]	VDD_HV_IO	I[3]	E[13]	J[1]	F[15]	H[13]	F[13]	VSS_HV_IO	VSS_HV_IO
B	VSS_HV_IO/VSS_LV_COR	VDD_HV_IO	F[3]	D[2]	B[6]	F[0]	D[4]	D[0]	VSS_HV_IO	E[14]	A[10]	B[3]	H[9]	C[10]	J[3]	VDD_HV_IO	VSS_HV_IO
C	I[15]	J[0]	VSS_HV_IO	FCCU_F[1]	A[13]	I[0]	H[10]	E[15]	H[11]	I[14]	J[2]	B[2]	H[6]	B[1]	VSS_HV_IO	B[0]	H[15]
D	A[6]	I[7]	A[15]	C[6]	N/C	EXT_POR_B	A[12]	VDD_HV_IO	VSS_HV_IO	A[11]	I[2]	F[14]	J[4]	VDD_HV_IO	VPP_TEST	A[4]	F[12]
E	F[4]	F[6]	D[1]	NMI_B	-	-	-	-	-	-	-	-	-	N/C	C[13]	G[3]	D[14]
F	F[5]	H[7]	H[5]	H[4]	-	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	-	C[14]	D[12]	G[4]	G[2]
G	MDO0	VDD_HV_IO	C[5]	A[7]	-	VDD_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR	-	B[4]	A[3]	J[8]	G[6]
H	A[8]	VSS_HV_IO	C[4]	A[5]	-	VDD_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR	-	G[12]	TMS	VDD_HV_FLA	TCK
J	C[7]	I[4]	F[8]	F[7]	-	VDD_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR	-	G[13]	H[1]	VDD_LV_NEXUS	B[5]
K	J[9]	F[10]	F[9]	I[8]	-	VDD_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR	-	G[15]	H[0]	VSS_LV_NEXUS	J[10]
L	H[8]	F[11]	I[9]	D[8]	-	VDD_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR	-	A[2]	G[14]	N/C	J[11]
M	VDD_HV_OSC	VDD_HV_IO	I[10]	D[5]	-	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	-	C[12]	I[6]	G[7]	G[5]
N	XTAL	VSS_HV_IO	D[9]	VSS_LV_PLL	-	-	-	-	-	-	-	-	-	G[8]	I[5]	VDD_LV_LFAST	VSS_LV_LFAST
P	VSS_HV_OSC	RESET_B	D[6]	VDD_LV_PLL	I[12]	I[13]	B[8]	J[5]	J[6]	J[7]	B[14]	A[0]	H[14]	G[9]	N/C	C[11]	D[11]
R	EXTAL	FCCU_F[0]	VSS_HV_IO	D[7]	B[7]	E[6]	VDD_HV_ADRE0	B[10]	VDD_HV_ADRE1	B[13]	B[15]	C[0]	BCTRL	N/C	VSS_HV_IO	D[10]	G[10]
T	VSS_HV_IO	VDD_HV_IO	I[1]	C[1]	E[5]	E[7]	VSS_HV_ADRE0	B[11]	VSS_HV_ADRE1	VDD_HV_ADV	E[10]	E[12]	E[0]	A[1]	G[11]	VDD_HV_IO	VSS_HV_IO
U	VSS_HV_IO	VSS_HV_IO	I[11]	E[4]	C[2]	E[2]	B[9]	B[12]	VSS_HV_ADV	E[9]	E[11]	N/C	N/C	VDD_HV_PMU/IO	N/C	VSS_HV_IO	VSS_HV_IO

How can we manage the complexity?

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Configurable Devices

The microcontroller IDE allows us to visually map these IO functions and peripherals to the device pins.

IDE Pin Configuration

TASKING Pin Mapper - myproject/myproject.pincfg - MPC Eclipse IDE vx.yrz

File Edit Navigate Search Project Debug Pin Mapper Window Help

Quick Access | TASKING C/C++ | TASKING Pin Mapper

myproject.pincfg

TASKING Pin Mapper - MPC574xP / MAPBGA257

Pin Selection | Pin Configuration

type filter text | Use tag: type new tag

- Ports
- Peripherals
- Other Pins

Pin Conflicts

0 items

Description	Module	Pin	Location

Package

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	VSS_HV_IO	VSS_HV_IO	A[14]	A[0]	D[3]	JCOMP	H[12]	C[15]	VDD_HV_IO	E[3]	E[13]	J[1]	F[16]	H[13]	F[13]	VSS_HV_IO	VSS_HV_IO
B	VSS_HV_IOVSS_LV_COR	VDD_HV_IO	F[3]	D[2]	B[6]	F[0]	D[4]	D[0]	VSS_HV_IO	E[14]	A[10]	B[3]	H[5]	C[10]	J[3]	VDD_HV_IO	VSS_HV_IO
C	I[15]	J[0]	VSS_HV_IO	FCCU_F[1]	A[13]	I[0]	H[10]	E[15]	H[11]	I[14]	J[2]	B[2]	H[6]	B[1]	VSS_HV_IO	B[0]	H[15]
D	A[6]	I[7]	A[15]	C[6]	N/C	EXT_POR_B	A[12]	VDD_HV_IO	VSS_HV_IO	A[11]	I[2]	F[14]	J[4]	VDD_HV_IO	VPP_TEST	A[4]	F[12]
E	F[4]	F[6]	D[1]	NMI_B										N/C	C[13]	G[3]	D[14]
F	F[5]	H[7]	H[5]	H[4]		VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR		C[14]	D[12]	G[4]	G[2]
G	MDO0	VDD_HV_IO	C[5]	A[7]		VDD_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR		B[4]	A[3]	J[8]	G[6]
H	A[8]	VSS_HV_IO	C[4]	A[5]		VDD_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR		G[12]	TMS	VDD_HV_FLA	TCK
J	C[7]	I[4]	F[8]	F[7]		VDD_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR		G[13]	H[1]	VDD_LV_NEXUS	B[5]
K	J[9]	F[10]	F[9]	I[8]		VDD_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR		G[15]	H[0]	VSS_LV_NEXUS	J[10]
L	H[9]	F[11]	I[9]	D[8]		VDD_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VSS_LV_COR	VDD_LV_COR		A[2]	G[14]	N/C	J[11]
M	VDD_HV_OSC	VDD_HV_IO	I[10]	D[5]		VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR	VDD_LV_COR		C[12]	I[0]	G[7]	G[5]
N	XTAL	VSS_HV_IO	D[9]	VSS_LV_PLL										G[8]	I[5]	VDD_LV_LFAST	VSS_LV_LFAST
P	VSS_HV_OSC	RESET_B	D[6]	VDD_LV_PLL	I[12]	I[13]	B[8]	J[5]	J[6]	J[7]	B[14]	A[0]	H[14]	G[9]	N/C	C[11]	D[11]
R	EXTAL	FCCU_F[0]	VSS_HV_IO	D[7]	B[7]	E[6]	VDD_HV_ADRE0	B[10]	VDD_HV_ADRE1	B[13]	B[15]	C[3]	BCTRL	N/C	VSS_HV_IO	D[10]	G[10]
T	VSS_HV_IO	VDD_HV_IO	I[1]	C[1]	E[5]	E[7]	VSS_HV_ADRE0	B[11]	VSS_HV_ADRE1	VDD_HV_ADV	E[10]	E[12]	E[0]	A[1]	G[11]	VDD_HV_IO	VSS_HV_IO
U	VSS_HV_IO	VSS_HV_IO	I[11]	E[4]	C[2]	E[2]	B[9]	B[12]	VSS_HV_ADV	E[9]	E[11]	N/C	N/C	VDD_HV_PMU/IO	N/C	VSS_HV_IO	VSS_HV_IO

MAPBGA 257 (Top View)

Connection status: Error | Warning | OK

Pin Configuration in the PCB Design

How can we manage this complexity for good PCB Design?

The traditional approaches:

- C… of Schematics leads to oversights:
  - …ned Pin Configuration is often not correctly …lected in hardware design.
  - …Variants of F… …signs often include un-needed …explai…
- Reference Bo… usually optimally designed for your particula… …arget application

Reference Design
- Eval Boards / Development Kits
- Application Notes

Develop Software
- Merge Reference Examples
- Add Custom Functions

Custom PCB
- Modify Reference Designs

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Pin Configuration in the PCB Design

How can we manage this complexity for good PCB Design?

The traditional approaches:

- T… eads to frustration:
  - …ed Pin Configuration is almost never correctly …n hardware design.
  - …ds PCB layout can cause unwanted pin onfiguration… …rocontroller.
  - Hardware de… …nds up requiring software …rounds… …other bugs, delaying software release.
  - IDE difficulty in… …ntegrating user-generated headers with startup code.
    - Can compl… …ke scri…

SCH/ PCB

- Application Notes
- Data Sheet Paranoia

Develop Wrappers

- Generate Spreadsheet
- Script-Jocky a Header File

Code / Fix

- Driver Dev.
- Find HW issues
- Converge on PCB Design

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Introduction to the TASKING Pin Mapper

The TASKING Pin Mapper will accelerate:

- Peripheral IO Selections
- Conflict Resolution
- Pin and Port Symbolic Naming
- Peripheral and GPIO wrappers generation
- PCB / Hardware design.

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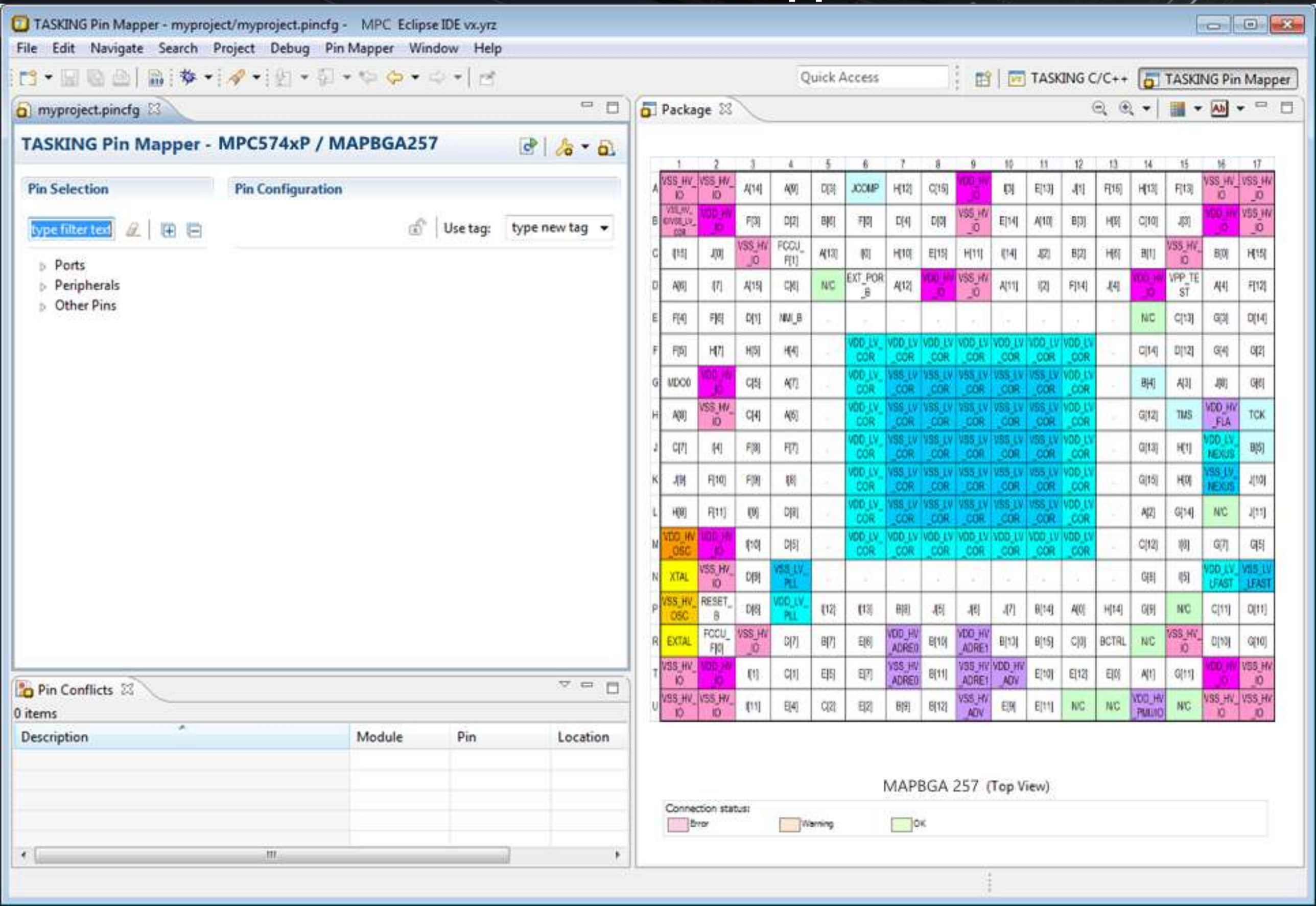
Introduction to the TASKING PinMapper



Peripherals

TASKING Pin Mapper - K64_Boo.pincfg - ARM Eclipse IDE v5.1r1

File Edit Navigate Search Project Debug Pin Mapper Window Help

Quick Access | TASKING C/C++ | TASKING Pin Mapper

K64_Boo.pincfg

TASKING Pin Mapper - MK64FN1M0CAJ12R / WLCSP-142

Pin Selection

type filter text

- PA
  - PA0
  - PA1
  - PA2
  - PA3
  - PA4
  - PA5
  - PA6
  - PA7
  - PA8
  - PA9
  - PA10
  - PA11
  - PA12
  - PA13
  - PA14
  - PA15
- DR

Pin Configuration

Use ta | new tag

Module name: PA3

Symbolic name:

Comment:

PA3 Configuration

Mode: Alternate function

Speed: High

Output type: Push-pull

Pull-up/Pull-down: No pull-up/no pull-dc

Chip input/output

PA3: ADC1_IN3

- None
- ADC1_IN3
- ADC2_IN3
- ADC3_IN3
- ETH_COL
- EXTI_EXTI3
- TIM2_CH4
- TIM5_CH4
- TIM9_CH2
- USART2_RX
- USB_OTG_HS_ULPI_D0
- GPIO

Pin Conflicts | Properties

Property	Valu

Package | Console

	1	2	3	4	5	6	7	8	9	10	11	
A	PTC4/ LLWU_P8	PTC7	PTC9	PTC12	PTC15	PTC17	PTD1	PTD5	PTD7	PTD9	PTD14	A
B	PTC3/ LLWU_P7	PTC6/ LLWU_P10	PTC8	PTC11/ LLWU_P11	PTC14	PTC18	PTD3	PTD6/ LLWU_P15	PTD8	PTD12	PTD15	B
C	PTC2	PTC5/ LLWU_P9	PTC10	PTC13	PTC16	PTD2/ LLWU_P13	PTD4/ LLWU_P14	PTD11	PTD13	PTE0	PTE3	C
D	PTB23	PTC0	PTC1/ LLWU_P6	PTB22	PTC19	PTD0/ LLWU_P12	PTD10	PTE1/ LLWU_P0	PTE2/ LLWU_P1	PTE4/ LLWU_P2	PTE5	D
E	PTB18	PTB19	PTB20	PTB21	VDD	VSS	PTE6	PTE7	PTE8	PTE9	PTE10	E
F	PTB16	PTB17	VDD	VSS	VSS	VDD	VDD	ADC0_DP1	PTE11	PTE12	VSS	F
G	PTB10	PTB11	PTB9	PTB8	VDD		VSS	ADC0_DM1	ADC0_DP0/ ADC1_DP3	VOUT33	USB0_DP	G
H	PTB7	PTB6	PTB5	PTB4	VSS	VSS	VDD	VDD	ADC0_DM0/ ADC1_DM3	VREGIN	USB0_DM	H
J	PTB3	PTB2	PTB1	PTB0/ LLWU_P5	PTA14	PTA11	PTA2	PTE27	RTC_ WAKEUP_B	ADC1_DP0/ ADC0_DP3	ADC1_DP1	J
K	PTA29	PTA28	PTA27	PTA26	PTA12	PTA8	PTA1	PTE25	ADC0_SE16/ CMP1_IN2/ ADC0_SE21	ADC1_DM0/ ADC0_DM3	ADC1_DM1	K
L	RESET_b	PTA24	PTA25	PTA16	PTA9	PTA5	PTA0	PTE24	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	VREFH	VDDA	L
M	PTA19	VSS	PTA17	PTA13/ LLWU_P4	PTA7	PTA4/ LLWU_P3	PTE28	VBAT	DAC1_OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_SE23	ADC1_SE16/ CMP2_IN2/ ADC0_SE22	VREFL	M
N	PTA18	VDD	PTA15	PTA10	PTA6	PTA3	PTE26	EXTAL32	XTAL32	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	VSSA	N
	1	2	3	4	5	6	7	8	9	10	11	

MK64FN1M0CAJ12R - WLCSP-142 (Top View)

Connection status:
Error Warning OK

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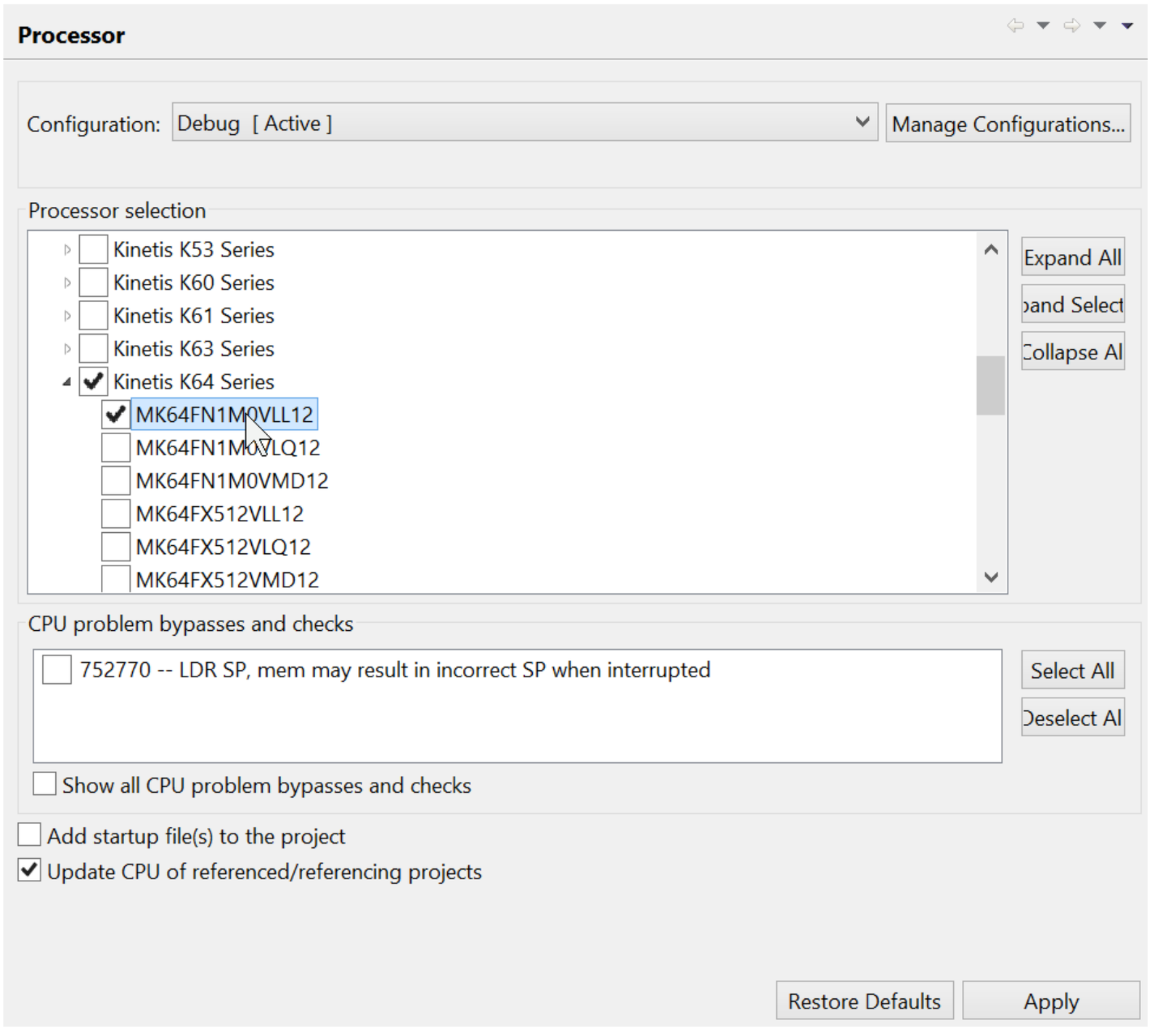
Package Selection



Package Selection happens when you begin a new embedded project, but can be changed later on when targeting a different processor variant:

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Add a Pin-Mapper Document to the Project

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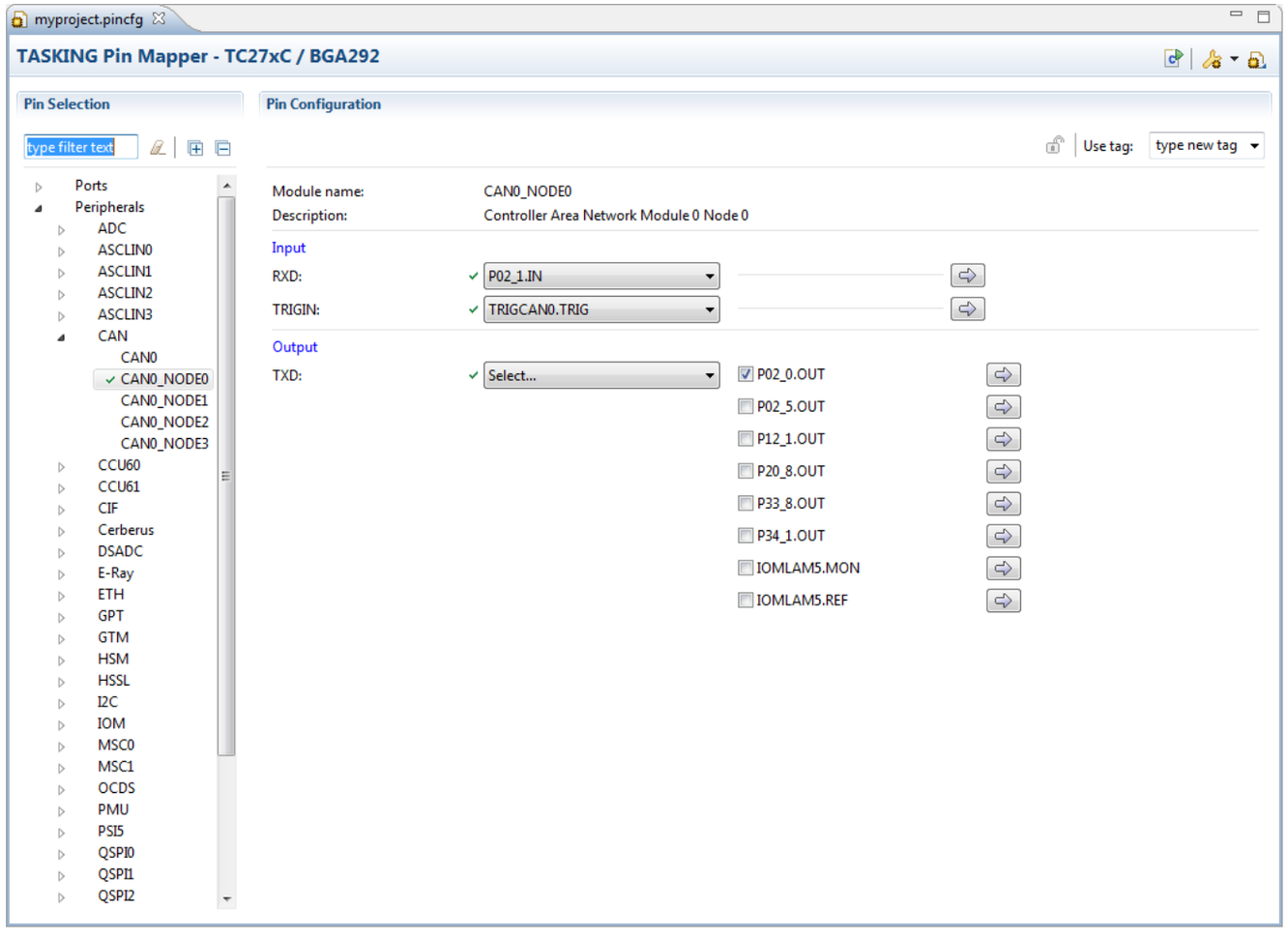

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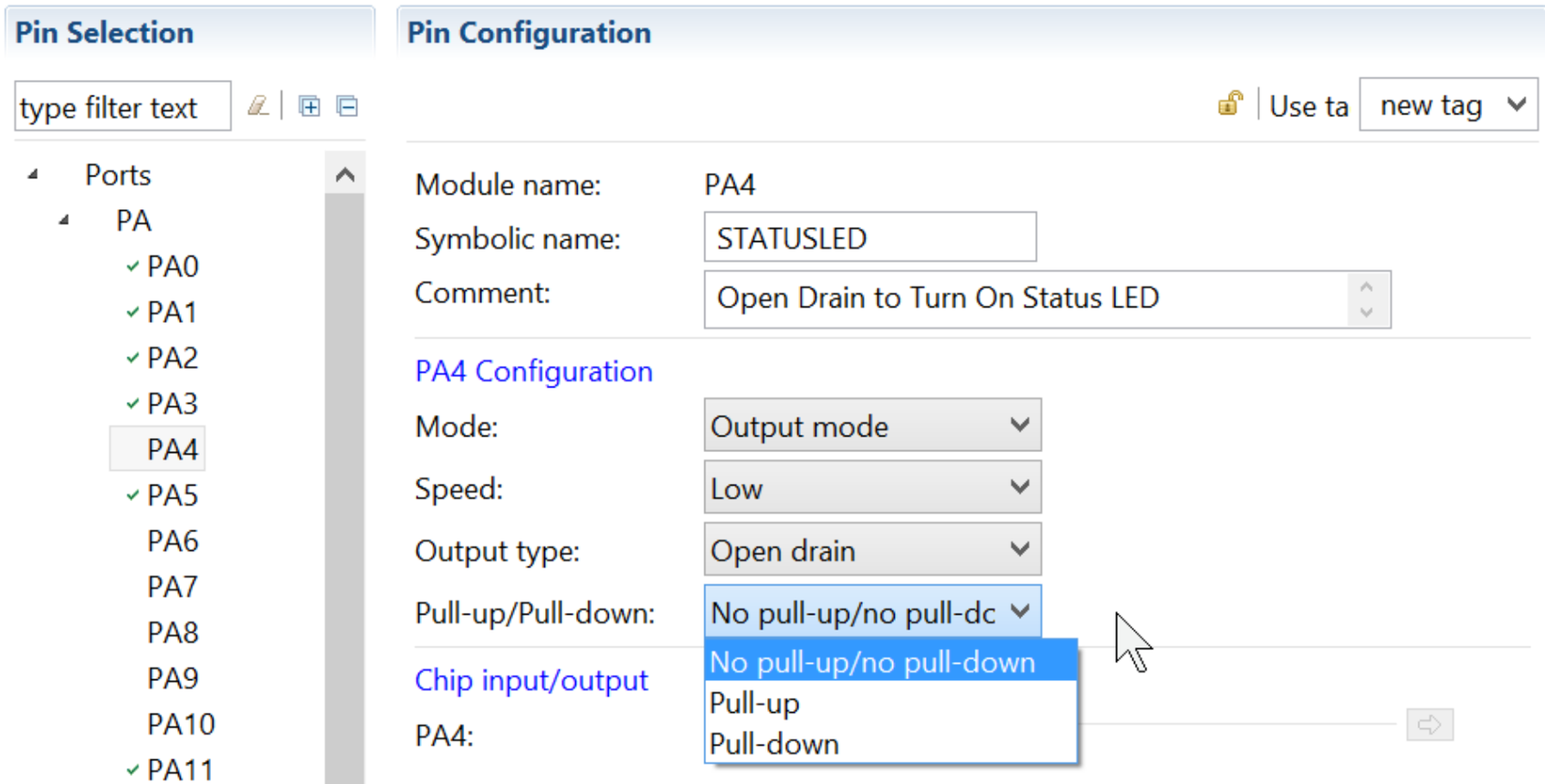
Pin Configuration - Ports



Symbolic name - Assign a user-defined symbol name to the port pin
Comment - Any user comments can be added here
Mode - This field sets the port mode register
Speed - Sets the port output speed register (2, 25, 50 or 100 MHz)
Output type - Sets the port output type register (push-pull or open drain)
Pull-up/Pull-down - Sets the port pull-up/pull-down
Chip input/output. Here you can make a pin connection

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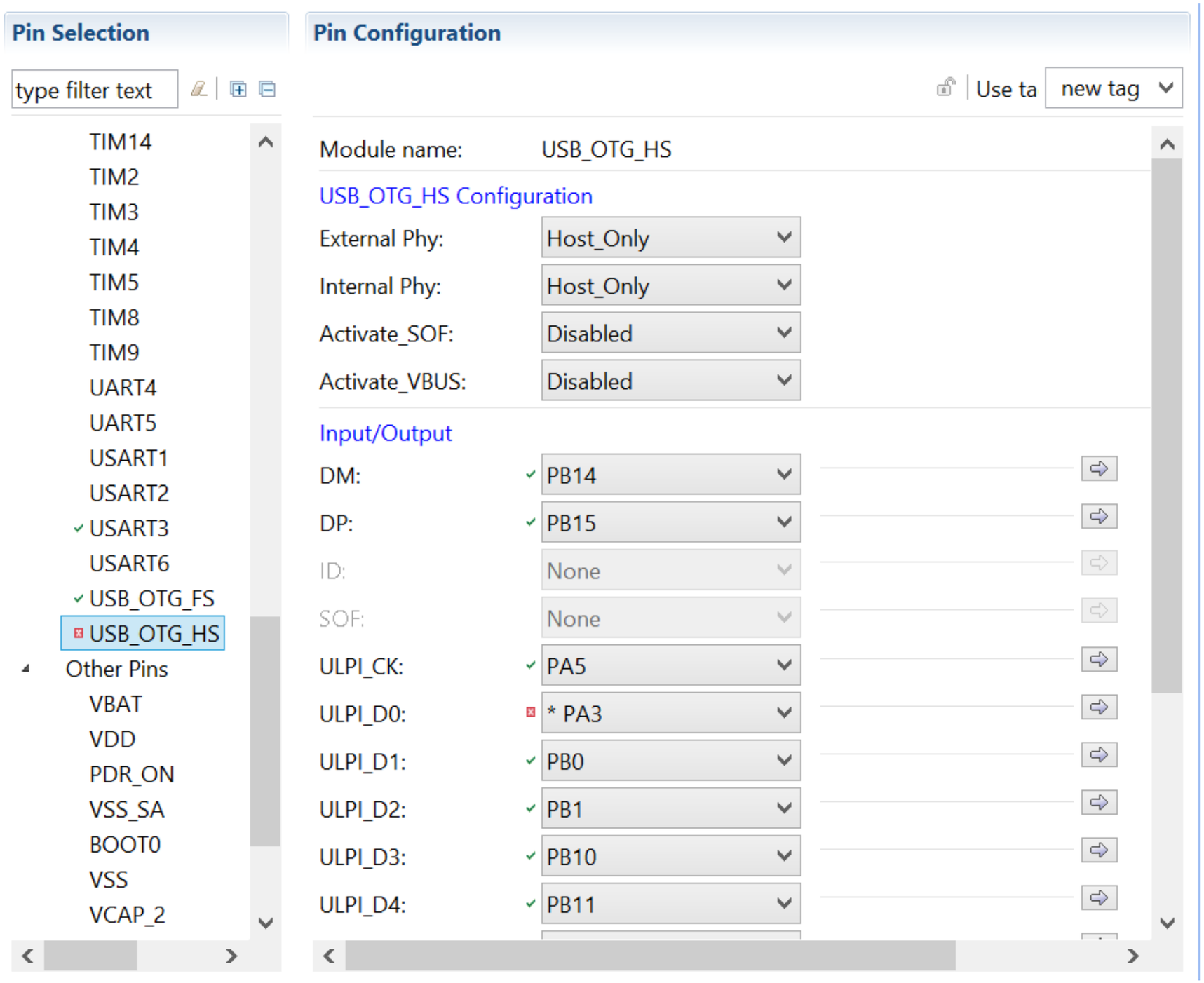
Pin Configuration - Peripheral

Module name - The name of the selected peripheral
Configuration. The configuration depends on the peripheral you selected
Input / Output - A list of port I/O functions (virtual pins)



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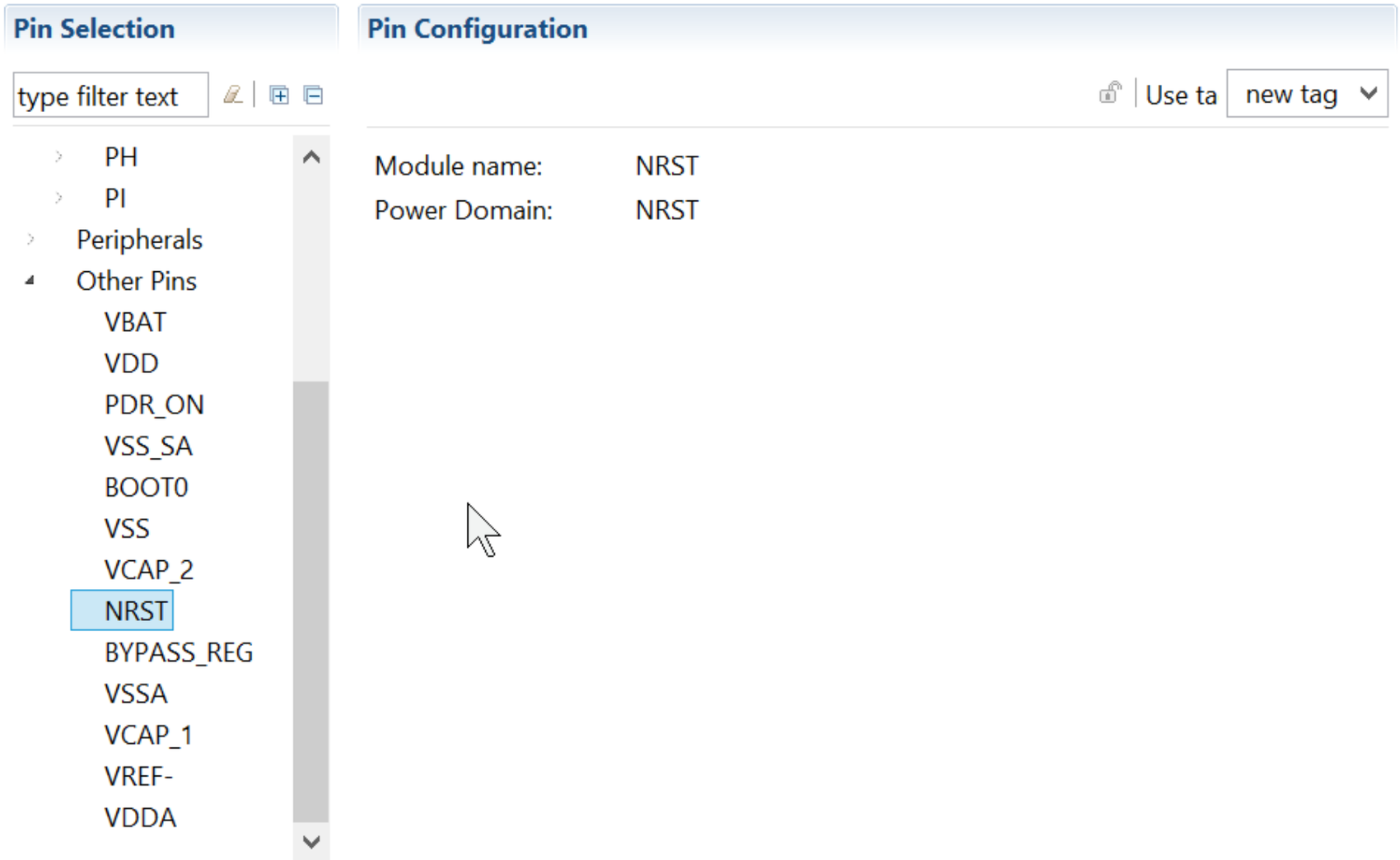
Pin Configuration - Other

Module name - The name of the selected other pin
Boot domain - The boot domain the pin uses
Power domain - The power domain the pin uses
Reset domain - The reset domain the pin uses



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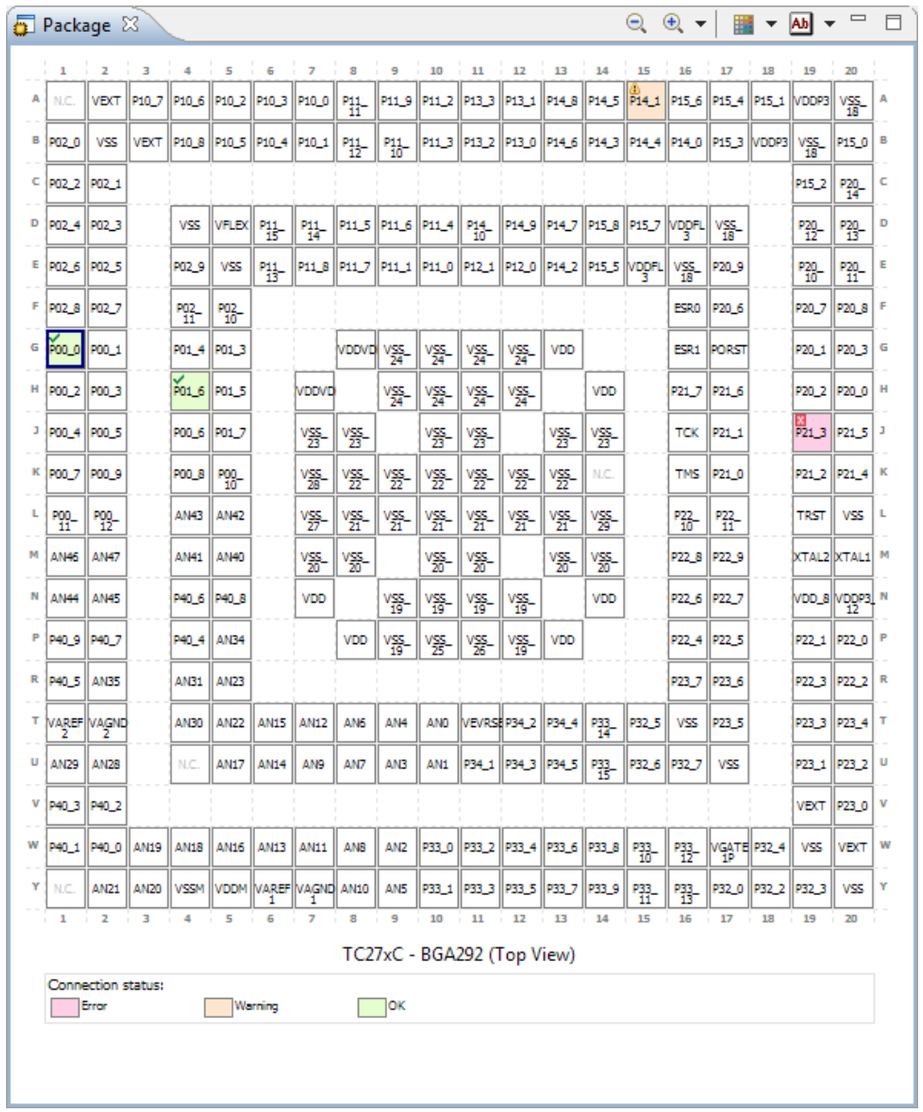
Package View

The Package view shows a graphical representation of a BGA



- **A square around a pin marks a selected pin; In the shown package pin P00_0 is selected**
- **A green check mark indicates that the pin has a valid connection; here P00_0 and P01_6**
- **A red cross indicates an error; P21_3 as an example**
- **A triangle with exclamation mark indicates a warning; P14_1 as an example**
- **When you click on a pin, the pin appears in the editor**

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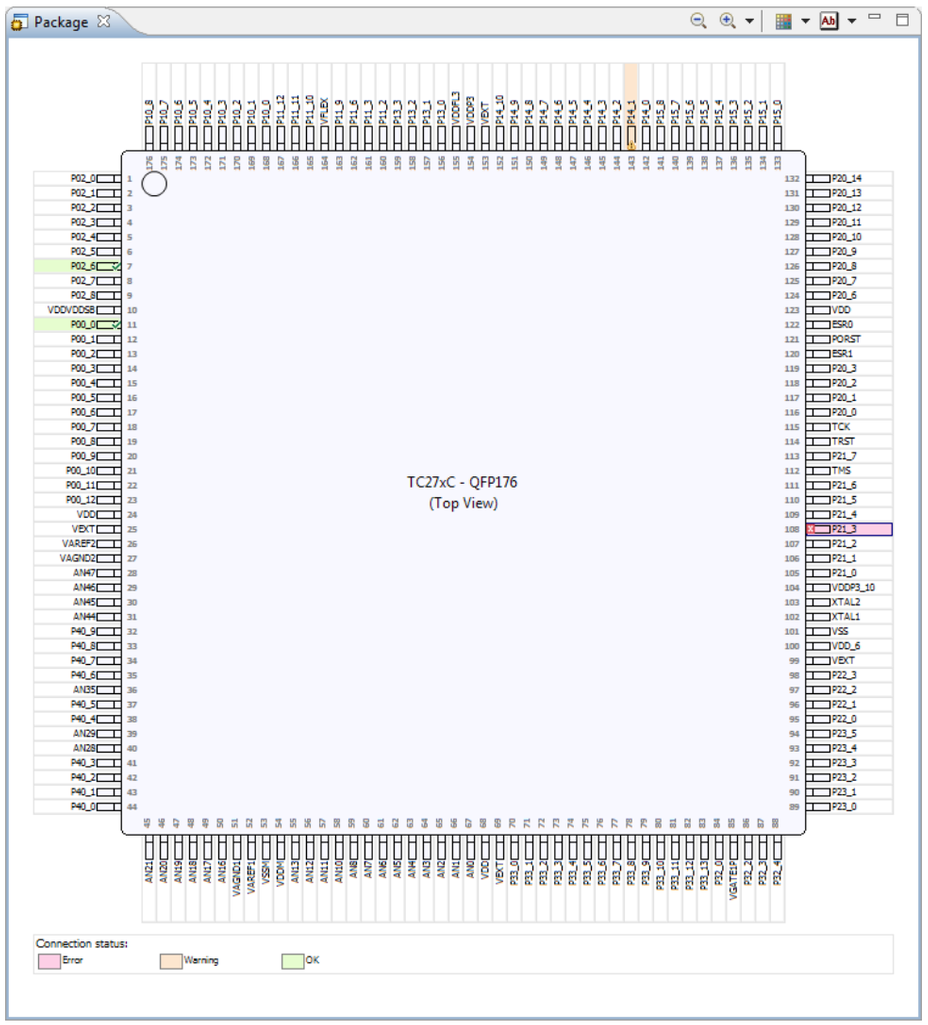
The Package View - QFP

Package View

The Package view shows a graphical representation of a QFP



- A square around a pin marks a selected pin; In the shown package pin P21_3 is selected
- A green check mark indicates that the pin has a valid connection; here P00_0 and P02_6
- A red cross indicates an error; P21_3 as an example
- A triangle with exclamation mark indicates a warning; P14_1 as an example
- When you click on a pin, the pin appears in the editor

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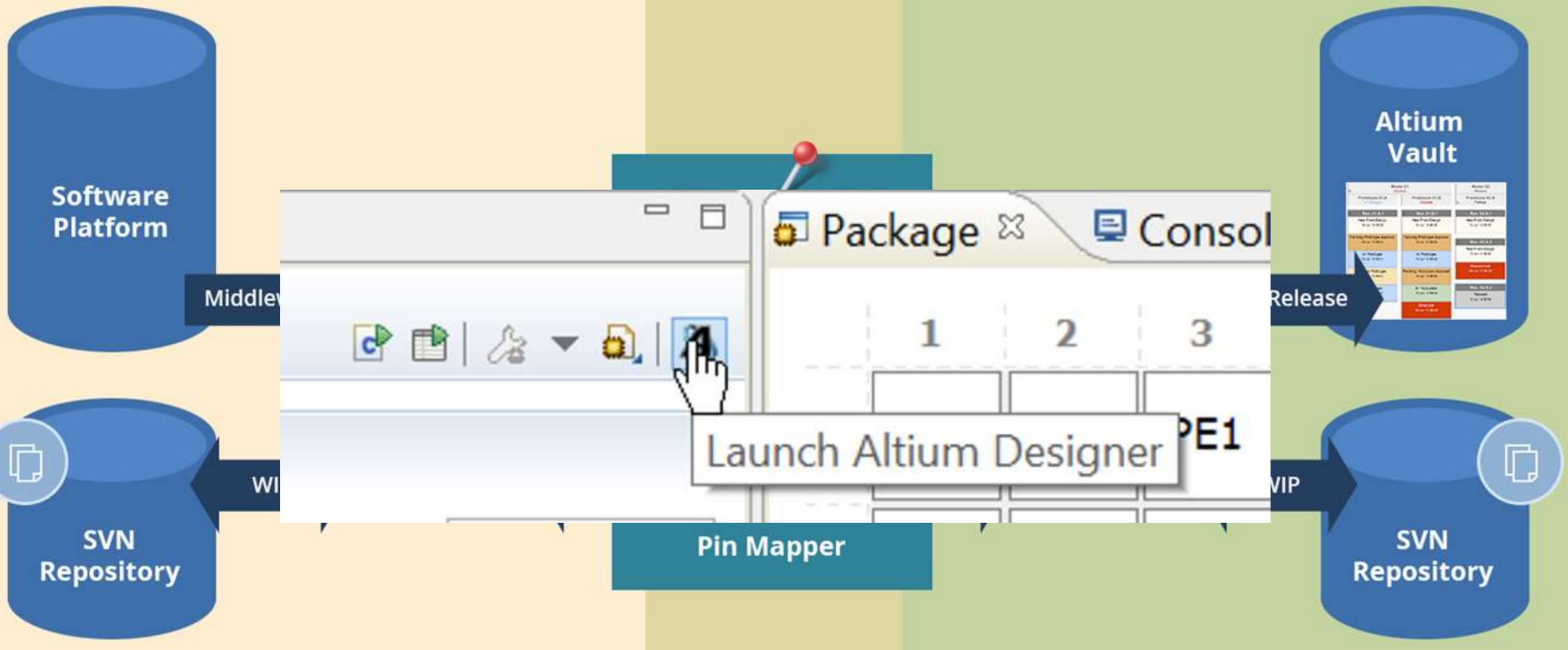
We can no longer work in Isolation

Software Design

Hardware Design



Microcontroller Device Information to configure assignment of Peripheral Module Signals to Physical Pins

Revision & Lifecycle Managed
Project Release including PCB & Firmware

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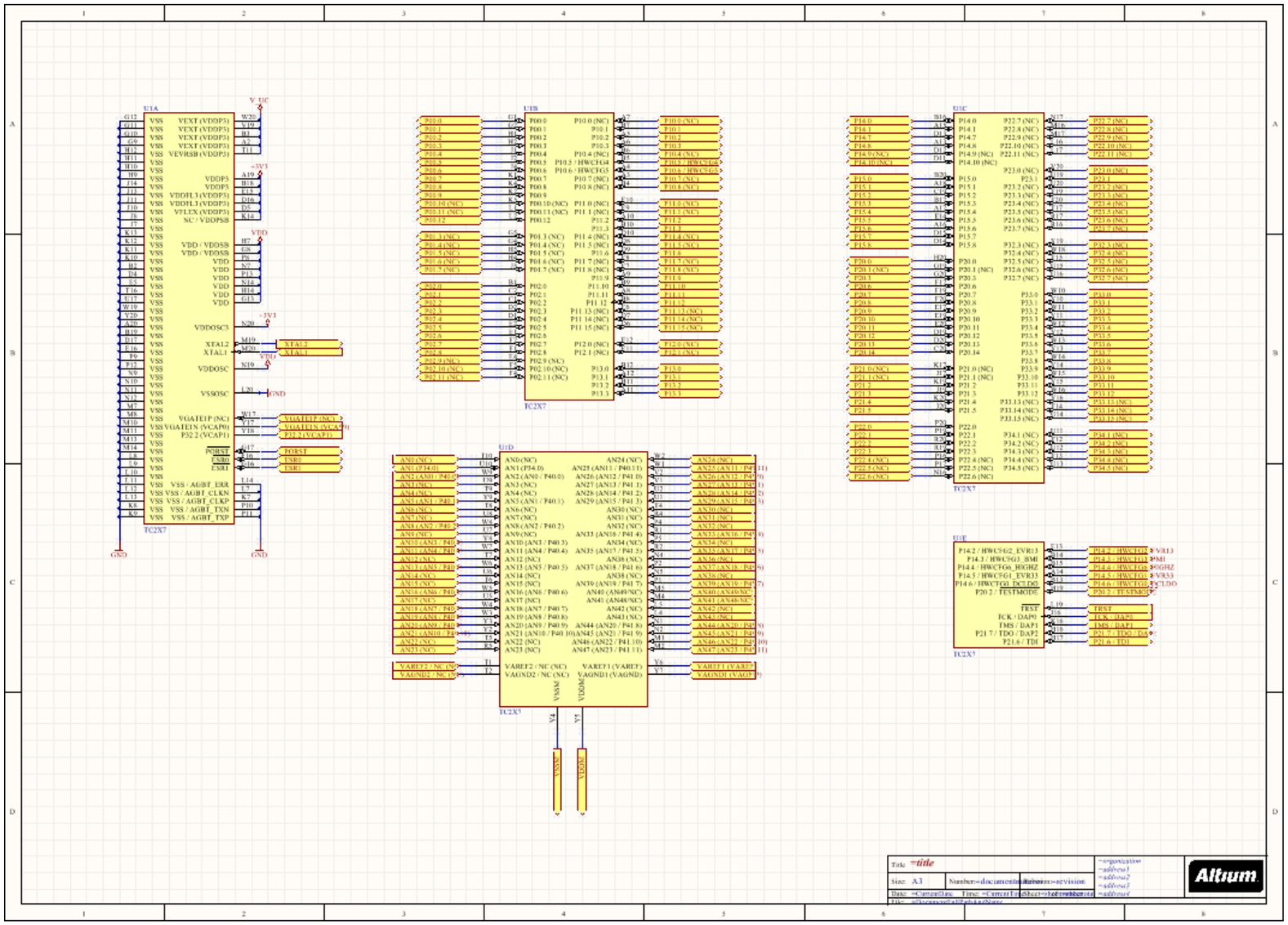
TASKING Pin Mapper – PCB Design Integration

Push changes to Embedded Schematic



- The Pin Mapper will Auto-generate the Schematic with the correct Pin signal names and Port grouping
- Power Pins and Boot options are also inserted
- Package view shows a graphical representation of the QFP package

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Pin Swapping

Once the bane of Embedded Developers…

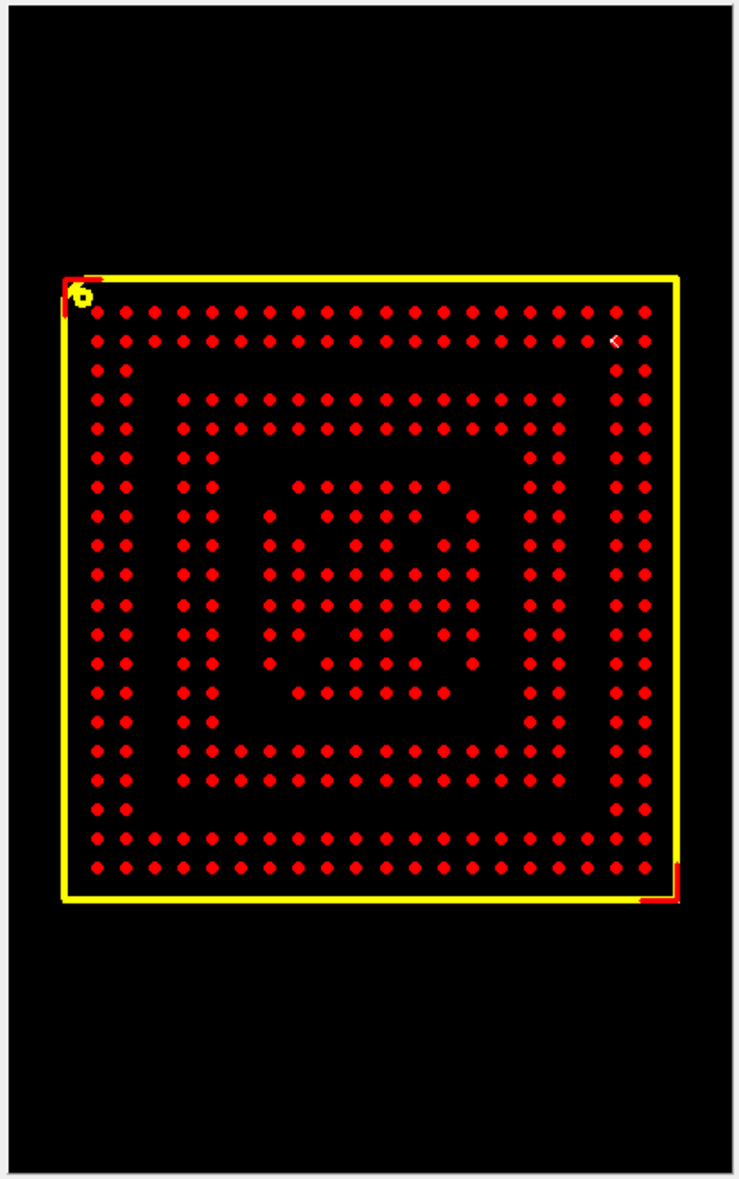
Pin Swapping at the PCB Level

Configure Pin Swapping For [U101 in Appl Kit TC2X7.PrjPcb / (No Configuration)]

Pin Swapping | Differential Pair Swapping | Part Swapping

Drag a column header here to group by that column

Pin Status					Swap D...
Designator	Pin Name	Net	Type	Part No.	Pin Group
W13	P33.6	P33.6	I/O	3	76
Y13	P33.7	P33.7	I/O	3	77
W14	P33.8	P33.8	I/O	3	78
Y14	P33.9	P33.9	I/O	3	79
W15	P33.10	P33.10	I/O	3	80
Y15	P33.11	P33.11	I/O	3	81
L4	AN43 (NC)	NetU101_L4	Input	4	91
L5	AN42 (NC)	NetU101_L5	Input	4	91
M1	AN46 (AN22 / P41.10)	NetU101_M1	Input	4	91
M2	AN47 (AN23 / P41.11)	NetU101_M2	Input	4	91
M4	AN41 (AN48/NC)	NetU101_M4	Input	4	91
M5	AN40 (AN49/NC)	NetU101_M5	Input	4	91
N4	AN36 (NC)	NetU101_N4	Input	4	91
N5	AN38 (NC)	NetU101_N5	Input	4	91
P4	AN32 (NC)	AN32(15)	Input	4	91
P5	AN34 (NC)	NetU101_P5	Input	4	91
R4	AN31 (NC)	NetU101_R4	Input	4	91
R5	AN23 (NC)	NetU101_R5	Input	4	91
T10	AN0 (NC)	AN0	Input	4	91
T4	AN30 (NC)	NetU101_T4	Input	4	91
T5	AN22 (NC)	VDD	Input	4	91
T6	AN15 (NC)	NetU101_T6	Input	4	91
T7	AN12 (NC)	NetU101_T7	Input	4	91
T8	AN6 (NC)	AN6(5)	Input	4	91
T9	AN4 (NC)	NetU101_T9	Input	4	91
U5	AN17 (NC)	AN17(14)	Input	4	91
U6	AN14 (NC)	NetU101_U6	Input	4	91
U7	AN9 (NC)	NetU101_U7	Input	4	91
U8	AN7 (NC)	NetU101_U8	Input	4	91
U9	AN3 (NC)	AN3	Input	4	91
W2	AN24 (NC)	AN24(12)	Input	4	91
P20	P22.0	P22.0	I/O	3	95
P19	P22.1	P22.1	I/O	3	96
R20	P22.2	P22.2	I/O	3	97
R19	P22.3	P22.3	I/O	3	98
M20	XTAL1	XTAL1	Input	1	102



FPGA Info None

OK Cancel

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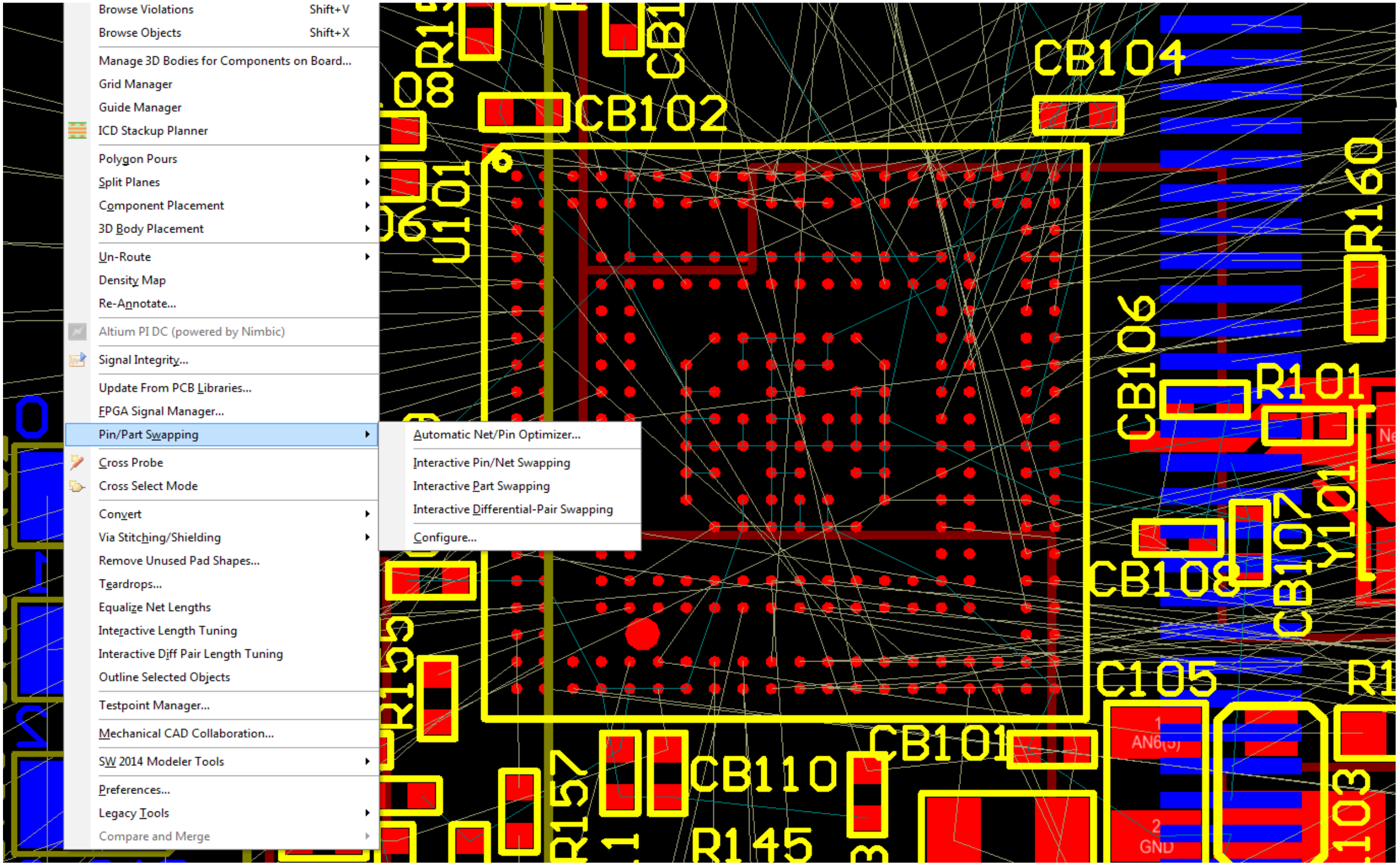
Pin Swapping at the PCB Level



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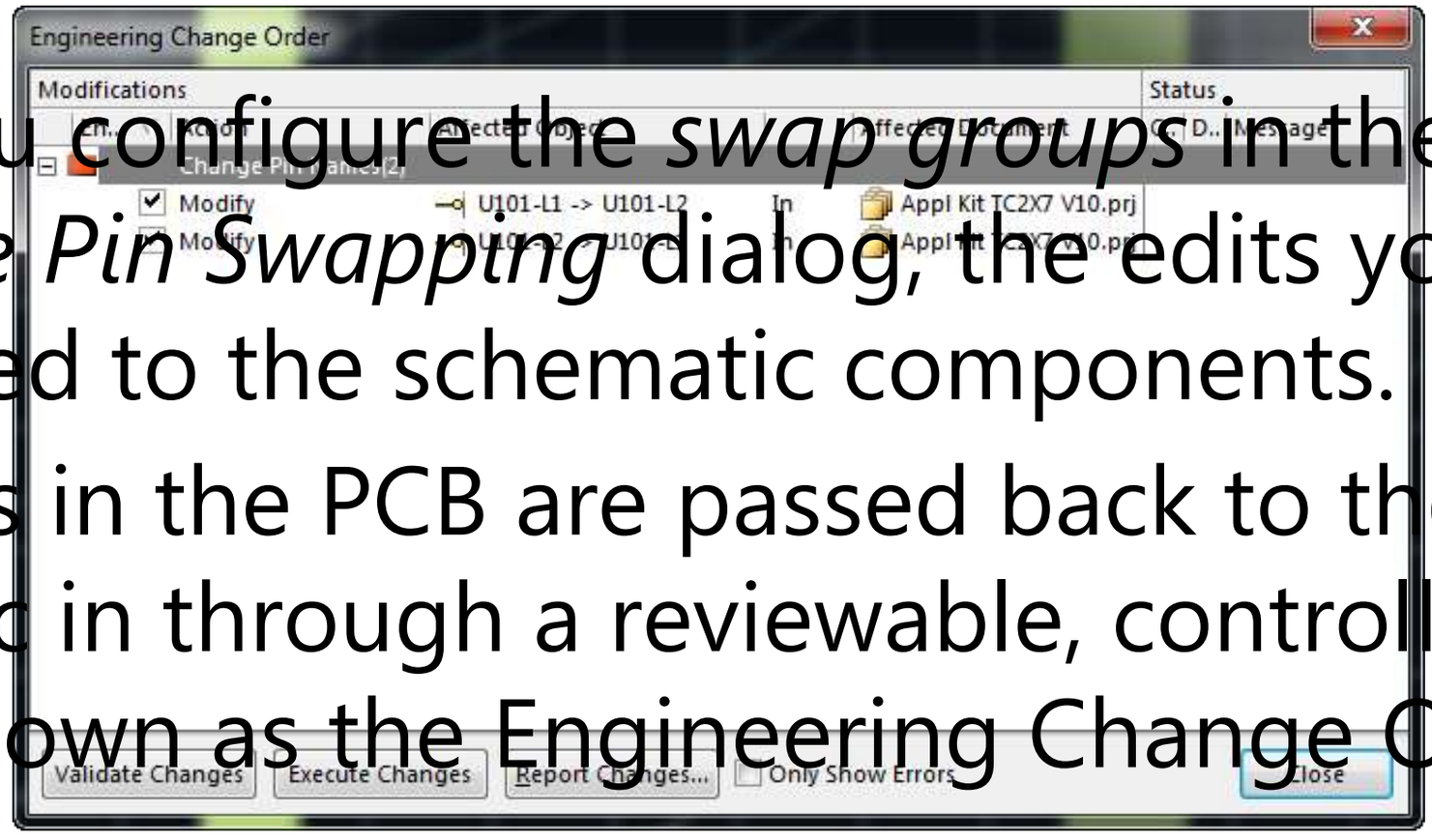
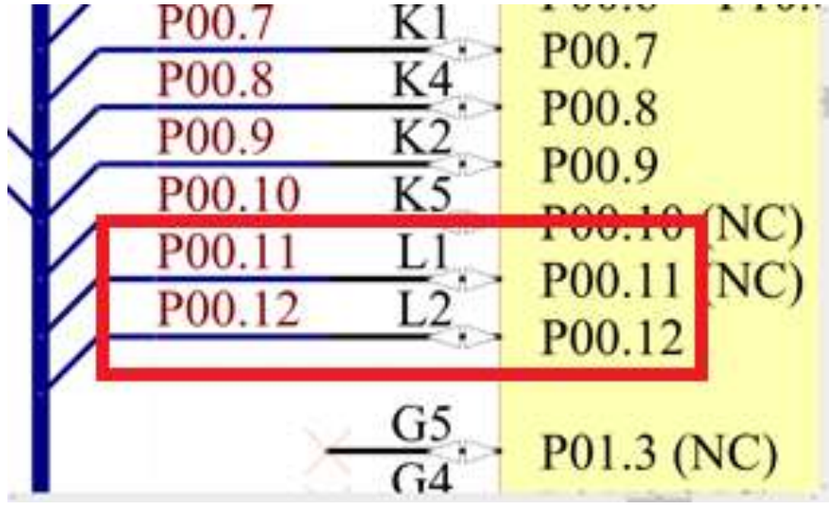
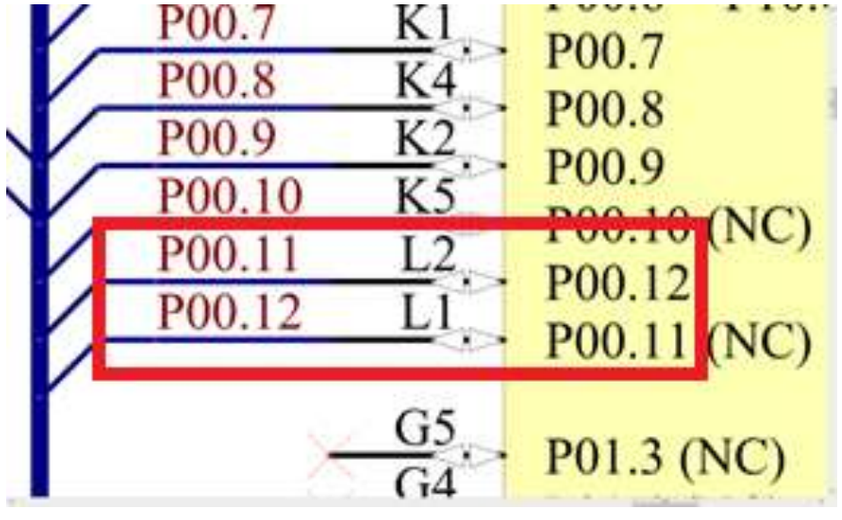
Pin Swapping Back-Annotates to Schematic

When you configure the *swap groups* in the *Configure Pin Swapping* dialog, the edits you make are applied to the schematic components.

Pin swaps in the PCB are passed back to the schematic in through a reviewable, controlled dialog known as the Engineering Change Order.







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PCB Signal Integrity Analysis

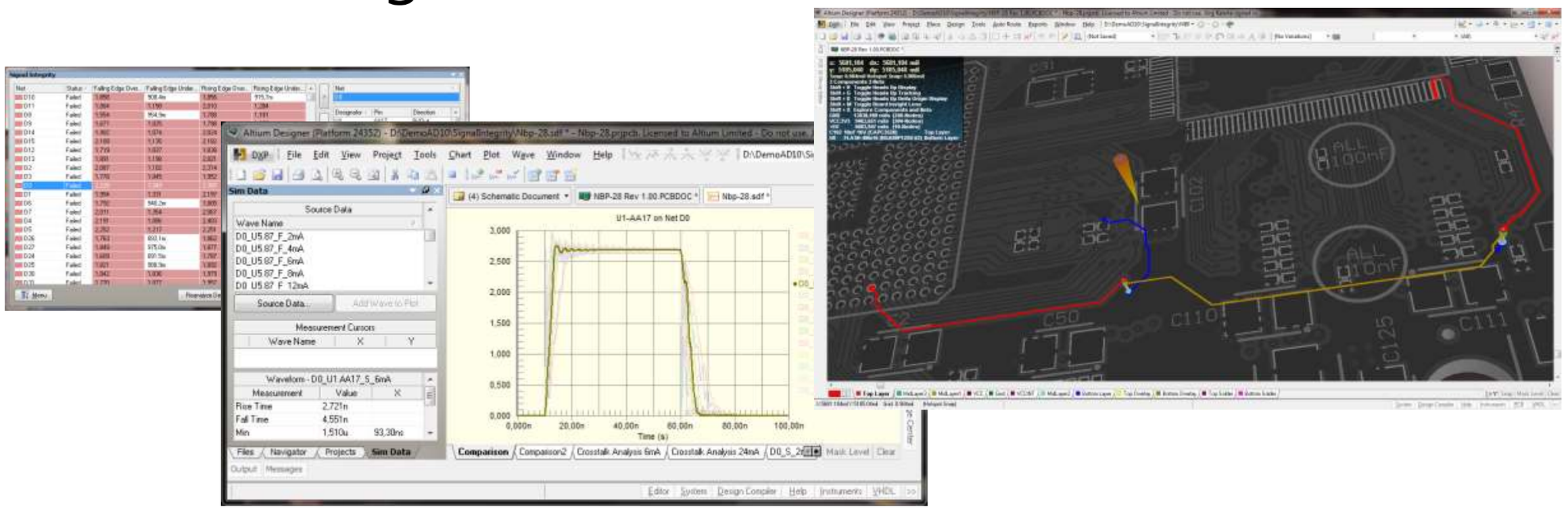
Proven Technology

- Transmission line calculations and I/O buffer models (IBIS)
- Industry-proven algorithms (Field-Solver)

Quickly explore potential solutions

- Cross-Probing / Highlighting SCH/PCB/SIM

Takes advantages of Unified Database



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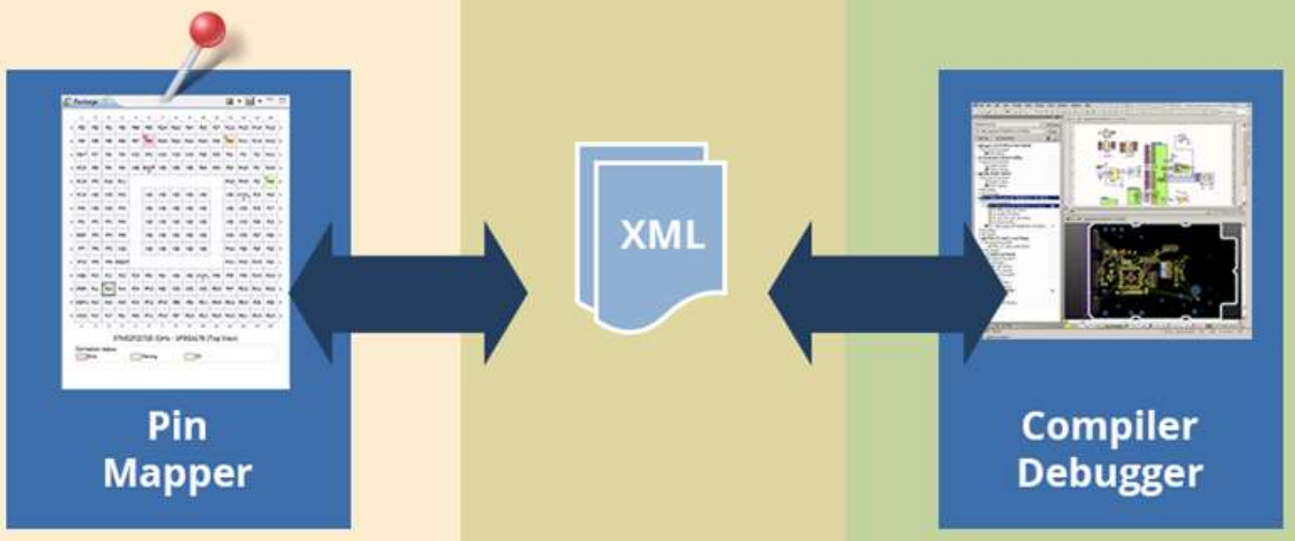
The Tasking Pin Mapper can be EXTENDED!

Software Design

Hardware Design



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Software

Talkin gless if
you d code,
driver ely use

*K64_boo.swpxmi

TASKING Software Platform - MK64FN1M0VLL12

Software Services

- Software Platform Builder
- Cortex-M Architecture
- Interrupt Management
- JSON Parser
- POSIX Message Queues
- POSIX Multi-threading
- POSIX Signals
- Software Timing Services

Device Stacks

- **Graphics Services** — GRAPHICS_1
- **SPFD5408 LCD Module Driver (parallel)** — DRV_SPFD5408_PAR_1
- **JPEG Decoder** — JPGDECODER_1

Pin Conflicts | Properties

POSIX Multi-threading

Property	Value	Type	Range / Prototype
Software Service Options			
Shared Memory	false	BOOLEAN	
DESTRUCTOR_ITERATIONS	4	UINT8	>= 4
KEYS_MAX	16	UINT16	16..128
THREADS_MAX	8	UINT8	>= 8
MAIN_STACK_SIZE	2048	UINT32	>= 512
MAIN_PRIORITY	32	UINT8	1..62
IDLE_STACK_SIZE	512	UINT32	>= 512
DEFAULT_STACK_SIZE	2048	UINT32	>= 512
SPORADIC_SERVER	false	BOOLEAN	
CPUTIME	false	BOOLEAN	
INTR_STACKSIZE	1024	UINT32	
CANCEL_SUPPORT	false	BOOLEAN	

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Software Platform Builder

- the *Software Platform Builder* is used to manage your Software Platform
- It is both a *graphical editor* and a *code generator*
- Collections of *software modules* are delivered as Software Platform *repositories*

Software Platform repository

- A Software Platform repository may contain any kind of software, but typical modules include interrupt services, timers, peripherals (hardware wrappers), drivers, kernel services (such as POSIX multithreading), device I/O, file system (FAT-Fs), networking (TCP/IP), graphical user interface (GUI), etc.


3000
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TASKING™
Embedded software development from Altium™

Support for the GTM-IP MCS

Programming the GTM / MCS

- The GTM is a timer module (containing MCS cores), present on several high-end microcontrollers for automotive, including Qorivva Power Architecture

- Traditionally the GTM is programmed in assembly, using assembler solutions from BOSCH (GCC based) or TASKING (VX-technology)

- 2013: Altium and BOSCH AE have investigated enhancements to the GTM core for making the development of an efficient C compiler possible

- 2014: Altium and BOSCH AE started the co-operation to develop a C compiler for the new GTM core level V3.x

- 2015: Altium releases C compiler for GTM V3.x

New TASKING C compiler for GTM / MCS

- Supports GTM-IP MCS core version V3
- ***Truly*** ISO-C99 compliant
  - Supports all ISO-C99 language features and C-library functions
  - Facilitates cost-efficient tool qualification against safety standards such as ISO 26262 and DO-330
- Based on TASKING's well known Viper "VX" compiler technology:
  - Similar to the C compilers for ARM (Kinetis) and Power Architecture (Qorivva), with industry proven stability
  - Perfectly suited for specialized cores, as proven through C compilers for other co-processor cores, targeting both efficiency and safety
  - ISO 26262 Support Program facilitates certification against various safety standards
- Data type characteristics match the MCS ISA
  - 24-bit integers, 48-bit longs, 32-bit float, ...
- Integrated static code analysis for MISRA C and CERT

New TASKING C compiler for GTM / MCS (cnt'd)

- Each MCS channel can be associated with an execution thread
  - Default register usage is limited to OREG registers
    - No need to suspend a subsequent channel
  - Optional use of XOREG registers
    - Improves execution speed at the cost of suspending a channel
- Emits debug information in DWARF 3 format
  - Facilitates symbolic C-level debugging
  - Supported by third party (in-circuit) debugger vendors

GTM / MCS Compiler Intrinsic Functions

- Provide access to MCS ISA features not addressable via ISO-C99
- Designed to optimize throughput over MCS busses
  - Compiler optimizations work efficiently with intrinsic functions
  - Function prototypes permit bus data to be accessible through function parameters and return values
- Supported operations:
  - GTM Time Base Unit Access
  - Trigger Registers Access
  - Bus Master Addressing

GTM-IP MCS Support

- Initial level of tool support for the GTM/MCS has been rolled out for multi-core MCU toolsets in 2011
- TASKING offers support for all versions of the GTM/MCS

Tool	GTM version		
	V1	V2	V3
Eclipse IDE	✓	✓	✓
Assembler	✓	✓	✓
Multi-core Linker	✓	✓	✓
C compiler			✓
Simulator / Debugger	✓	✓	✓

- C compiler support available in 2015
  - Initial (standalone) release available per April 21, 2015
  - Available prior to HW/silicon availability

Interoperability of MCS Tools

- MCS Embedded Applications Binary Interface
  - Facilitates interoperability between tools
  - DWARF-3 debug support for compatibility with debug solutions

- Assembly conversion utility
  - TASKING provides a utility to convert GNU based BOSCH MCS assembly to syntax used by the TASKING assembler

- Advanced Multi-core Linker
  - Supporting a multitude of output formats
    - ELF – Facilitates C-level symbolic debugging
    - Intel HEX or Motorola S-record format – For PROM programming
    - C-file with C-array – Supports “old-style” MCS to CPU interfacing

MCS Tool Support Availability

- All MCS tools are accessible from within the Eclipse IDE, as well as from the command line

- Full featured C and assembly level debugger
  - Runs within an Eclipse perspective
  - Interacts with fast instruction set simulator

- Support will be included in TASKING VX-toolsets:
  - Freescale Power Architecture - Qorivva MPC5xxxx series
  - STMicroelectronics Power Architecture - SPC5xx series

- MCS EABI is available from Bosch AE or Altium

MCS Tool Support Roll-out Plan

- April 2015:
  - Standalone C compiler for GTM / MCS
    - Intermediate solution until integration in the VX-toolsets for the appropriate CPUs
- Q3-4 2015:
  - Integration in the TASKING VX-toolset for Power Architecture

Subject to change. Proposed features may be implemented in earlier intermediate revisions, as well as postponed to later releases or rejected due to lack of customer interest or resources.

TASKING Information

- TASKING is an Altium brand
- TASKING Development Tools are available from Altium
  - Altium is a global organization, with 400+ employees
    - Sales and Support offices in Americas, Australia, China, Germany, Japan
  - TASKING product development is located in The Netherlands
  - Altium is listed on the Australian Stock Exchange: ASX:ALU
- TASKING Development Tools support many automotive and multi-market architectures from the world's leading semiconductor vendors, including:
  - ARM, Atmel, Cypress, Freescale, Infineon, NXP, ON Semiconductor, Renesas, Silicon Labs, STMicroelectronics, Texas Instruments
- More information: www.tasking.com
  - or: iwantacompiler@tasking.com

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Thank you for your attention